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## 9P750CGLF

**Category:** [Zero Delay Buffers](#)

**Generic Part:** [9P750](#)

**Market Group:** [PC CLOCK](#)

**Description:** [PC BUFFER](#)

Recommended Application: DDR Zero Delay Clock Buffer Product Description/Features:  $\hat{\epsilon}$  Low skew, low jitter PLL clock driver  $\hat{\epsilon}$  12 pairs of differential outputs support up to DDR400  $\hat{\epsilon}$  Outputs divided into 3 groups - Group A is reference - Groups B and C have default offsets from Group A, but also have skew programmable in steps relative to Group A - Skew step (unit) set via RSTEP resistor  $\hat{\epsilon}$  Static Phase Offset (SPO) of entire device can be programmed - RSPO sets overall SPO (analog delay) - I2C register settings allow fine tuning in steps defined by RSTEP  $\hat{\epsilon}$  Spread spectrum tolerant inputs  $\hat{\epsilon}$  2.5 V differential reference clock input Switching Characteristics:  $\hat{\epsilon}$  PEAK - PEAK jitter (>100MHz): <75ps  $\hat{\epsilon}$  CYCLE - CYCLE jitter (>100MHz): <65ps  $\hat{\epsilon}$  OUTPUT - OUTPUT skew: <50ps  $\hat{\epsilon}$  DUTY CYCLE: 49% - 51%  $\hat{\epsilon}$  Slew rate: 1V/ns - 2V/ns  $\hat{\epsilon}$  Input clock duty cycle: 40% - 60%



### Parameters

Package	TSSOP 48 (PAG48)
Voltage	3.3 V
Package	TSSOP 48
Speed	NA
Temperature	C
Status	Active
Sample	Yes
Minimum Order Quantity	76
Factory Order Increment	38

### Distributor Inventory

No Pricing information is available from our Distributors at this time.

### Documents

Type	Title	Size	Revision Date
Misc	PC Clocks Contact Info	61 KB	05/29/2007

### Package

Description	TSSOP 6.10 MM
Class	PLASTIC
Moisture Sensitivity Level (MSL)	1
Category	Green
Moisture Exposure Floor Life	Unlimited @ <30°C/85% RH
Peak Reflow Temperature	260°C
Rebake Conditions	NA
Length	12.5
Mark	G
Width	6.1
Pitch	0.5
Thickness	1.0
Status	Active