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# FDT86246L

## N-Channel PowerTrench<sup>®</sup> MOSFET

### 150 V, 2 A, 228 mΩ

#### Features

- Max  $r_{DS(on)}$  = 228 mΩ at  $V_{GS} = 10\text{ V}$ ,  $I_D = 2\text{ A}$
- Max  $r_{DS(on)}$  = 280 mΩ at  $V_{GS} = 4.5\text{ V}$ ,  $I_D = 1.8\text{ A}$
- High performance trench technology for extremely low  $r_{DS(on)}$
- High power and current handling capability in a widely used surface mount package
- Fast switching speed
- 100% UIL Tested
- RoHS Compliant

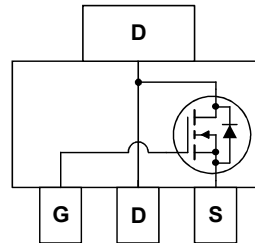
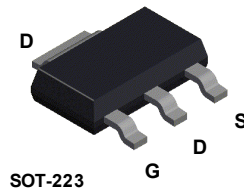


#### General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench<sup>®</sup> process that has been optimized for  $r_{DS(on)}$ , switching performance and ruggedness.

#### Applications

- Load Switch
- Primary Switch
- Buck/Boost Switch



#### MOSFET Maximum Ratings $T_C = 25\text{ °C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	150	V
$V_{GS}$	Gate to Source Voltage	±20	V
$I_D$	Drain Current -Continuous $T_A = 25\text{ °C}$ (Note 1a)	2	A
	-Pulsed (Note 4)	20	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	6	mJ
$P_D$	Power Dissipation $T_A = 25\text{ °C}$ (Note 1a)	2.2	W
	Power Dissipation $T_A = 25\text{ °C}$ (Note 1b)	1.0	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

#### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	12	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	55	

#### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
86246L	FDT86246L	SOT-223	13 "	12 mm	2500 units

## Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}, V_{GS} = 0\text{ V}$	150			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		110		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 120\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	0.8	1.6	2.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-5		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 2\text{ A}$		189	228	m $\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 1.8\text{ A}$		208	280	
		$V_{GS} = 10\text{ V}, I_D = 2\text{ A}, T_J = 125\text{ }^\circ\text{C}$		375	452	
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{ V}, I_D = 2\text{ A}$		7.3		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 75\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		238	335	pF
$C_{oss}$	Output Capacitance			20	30	pF
$C_{rss}$	Reverse Transfer Capacitance			2	5	pF
$R_g$	Gate Resistance		0.1	0.9	2.7	$\Omega$

### Switching Characteristics

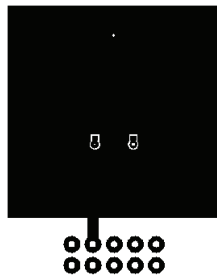
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 75\text{ V}, I_D = 2\text{ A}, V_{GS} = 10\text{ V}, R_{GEN} = 6\text{ }\Omega$		4.5	10	ns
$t_r$	Rise Time			1.3	10	ns
$t_{d(off)}$	Turn-Off Delay Time			11	20	ns
$t_f$	Fall Time			2	10	ns
$Q_{g(TOT)}$	Total Gate Charge		$V_{GS} = 0\text{ V to } 10\text{ V}$	4.5	6.3	nC
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\text{ V to } 4.5\text{ V}$	2.3	3.3	nC	
$Q_{gs}$	Total Gate Charge	$V_{DD} = 75\text{ V}, I_D = 2\text{ A}$		0.7		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			1.0		nC

### Drain-Source Diode Characteristics

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 2\text{ A}$ (Note 2)		0.8	1.3	V
$t_{rr}$	Reverse Recovery Time	$I_F = 2\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		44	71	ns
$Q_{rr}$	Reverse Recovery Charge			31	50	nC

#### NOTES:

- $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a) 55  $^\circ\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b) 118  $^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper

- Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0%.

- $E_{AS}$  of 6 mJ is based on starting  $T_J = 25\text{ }^\circ\text{C}$ ; N-ch: L = 3 mH,  $I_{AS} = 2\text{ A}, V_{DD} = 150\text{ V}, V_{GS} = 10\text{ V}$ . 100% test at L = 0.1 mH,  $I_{AS} = 7\text{ A}$ .

- Pulsed Id please refer to Fig 11 SOA graph for more details.

- Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted.

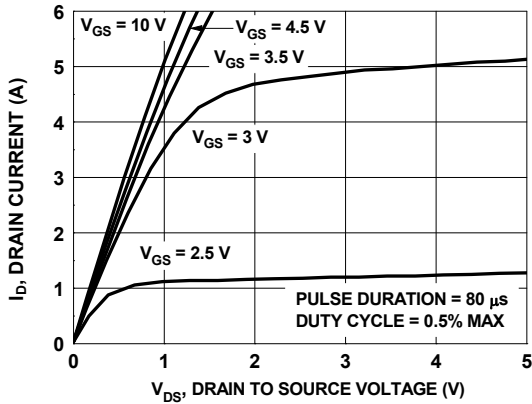


Figure 1. On Region Characteristics

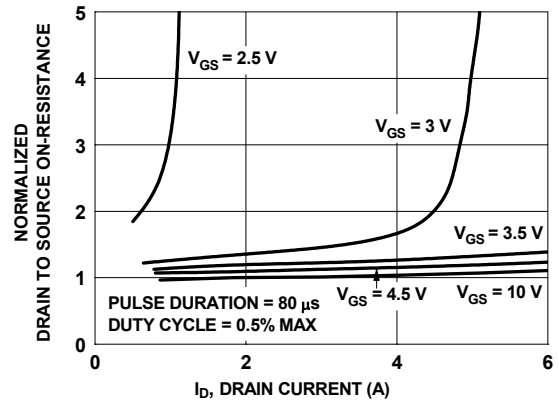


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

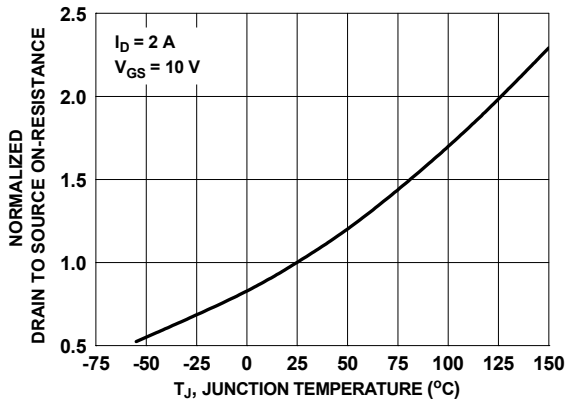


Figure 3. Normalized On Resistance vs. Junction Temperature

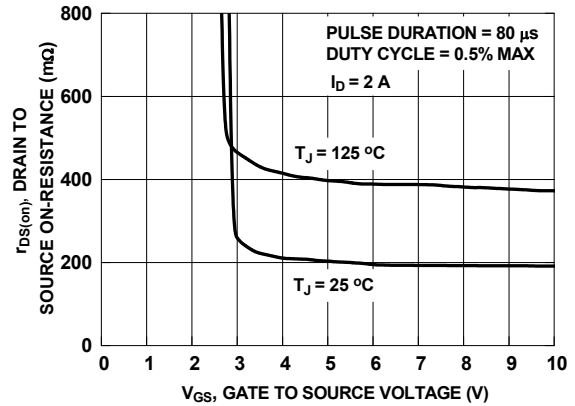


Figure 4. On-Resistance vs. Gate to Source Voltage

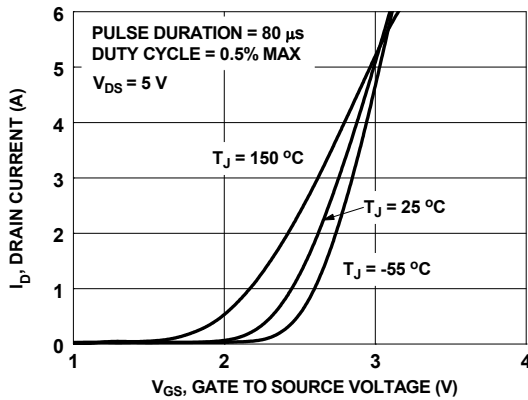


Figure 5. Transfer Characteristics

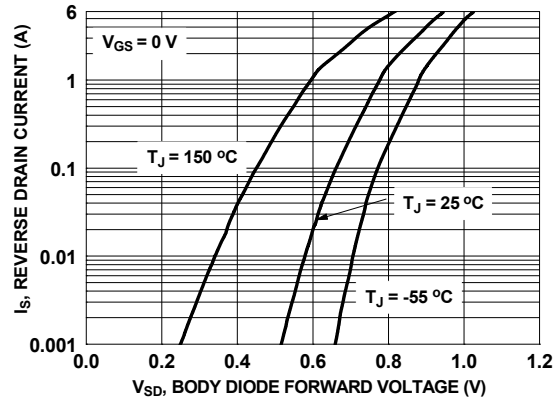
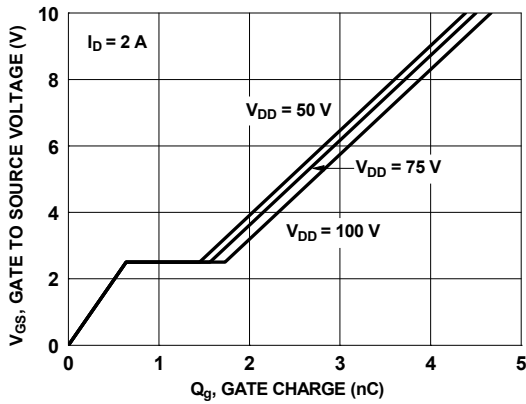
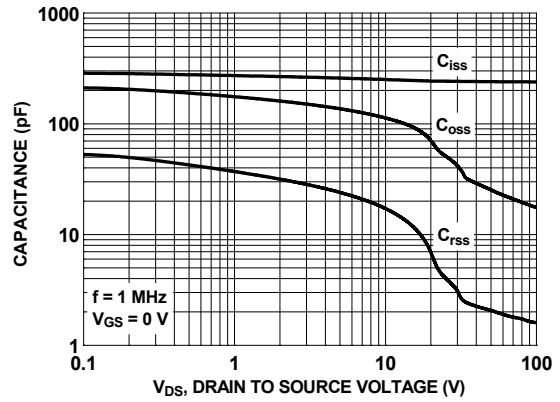


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

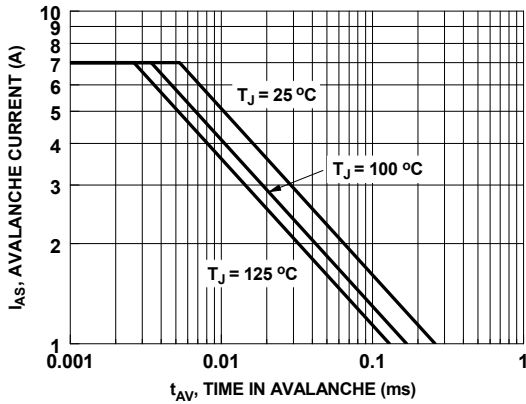
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted.



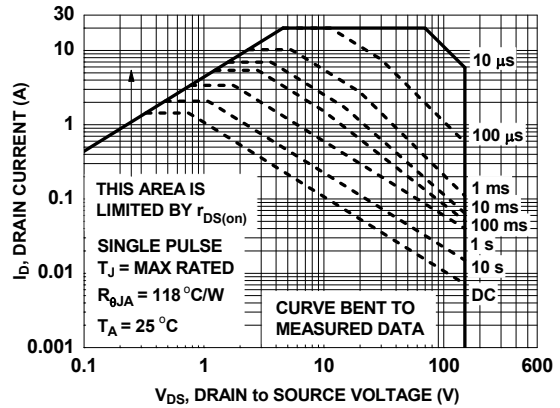
**Figure 7. Gate Charge Characteristics**



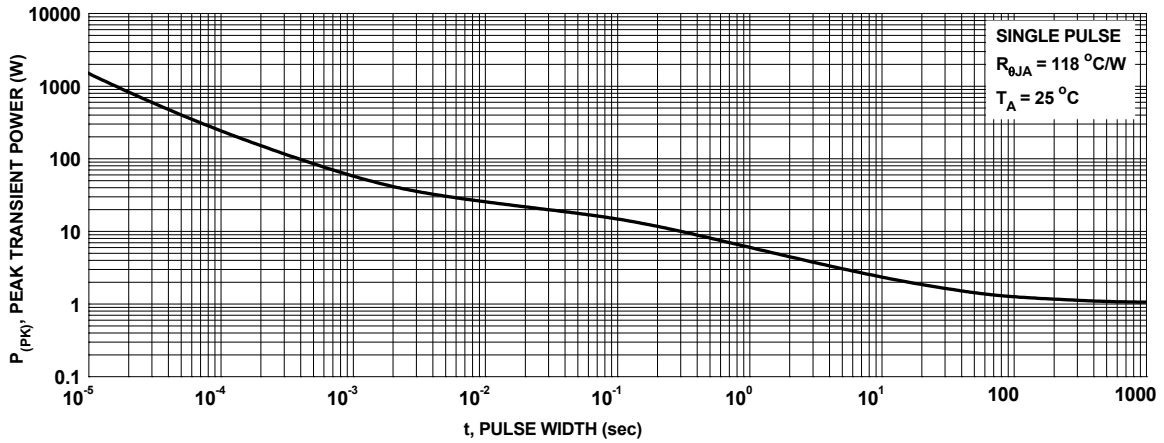
**Figure 8. Capacitance vs. Drain to Source Voltage**



**Figure 9. Unclamped Inductive Switching Capability**

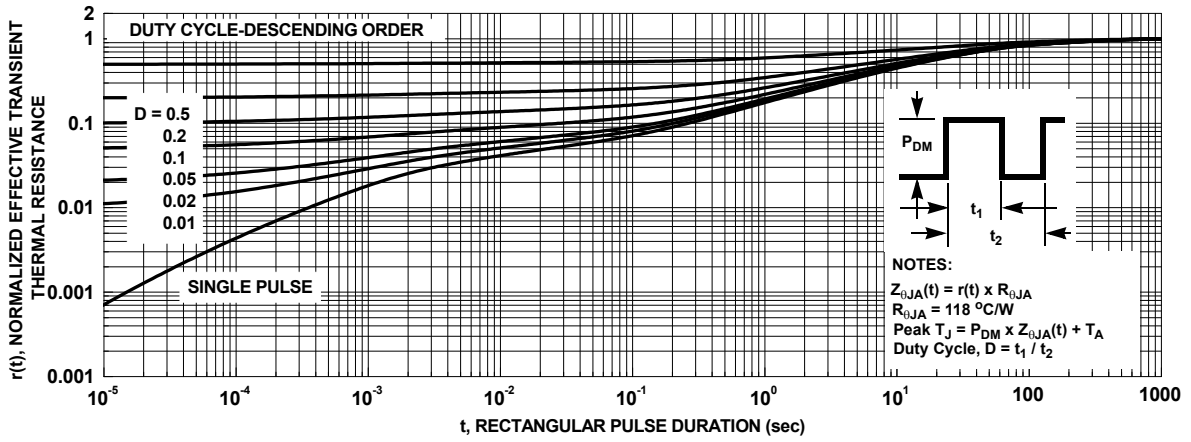


**Figure 10. Forward Bias Safe Operating Area**

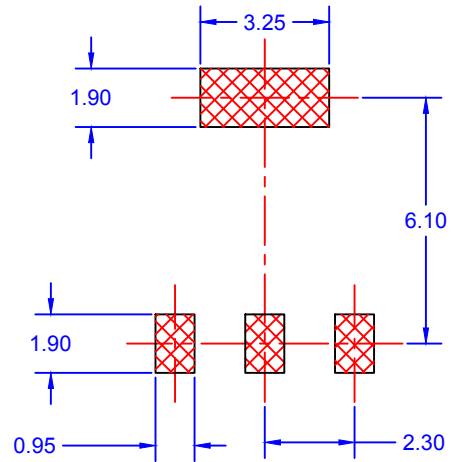
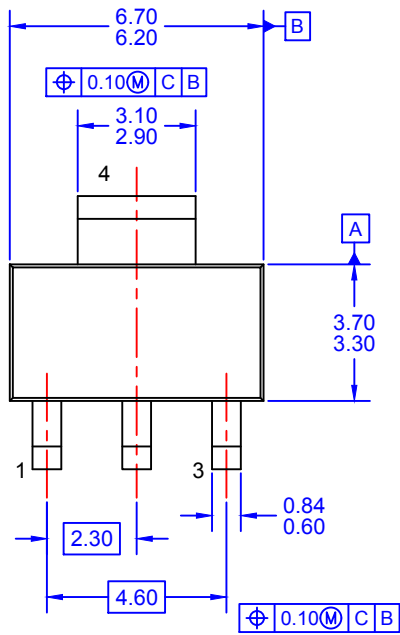


**Figure 11. Single Pulse Maximum Power Dissipation**

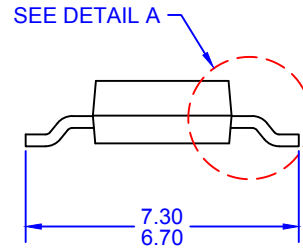
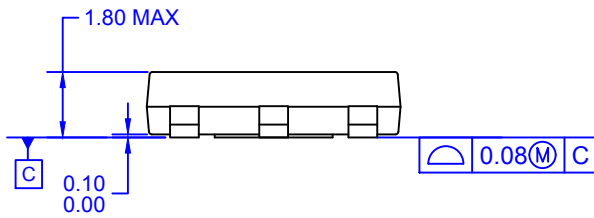
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted.



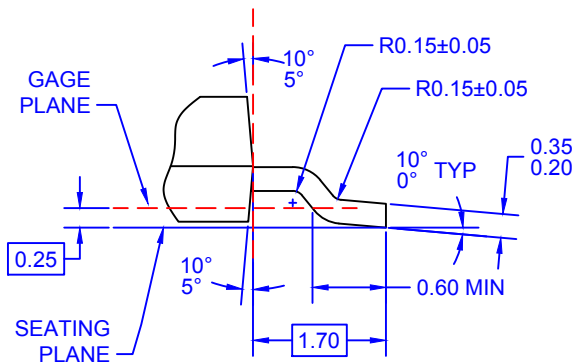
**Figure 12. Junction-to-Ambient Transient Thermal Response Curve**



LAND PATTERN RECOMMENDATION



- NOTES: UNLESS OTHERWISE SPECIFIED  
 A) DRAWING BASED ON JEDEC REGISTRATION TO-261C, VARIATION AA.  
 B) ALL DIMENSIONS ARE IN MILLIMETERS.  
 C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.  
 D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.  
 E) LANDPATTERN NAME: SOT230P700X180-4BN  
 F) DRAWING FILENAME: MKT-MA04AREV3



DETAIL A  
SCALE: 2:1



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