PIC18FXX2

PIC18FXX2 Rev. B3/B4 Silicon/Data Sheet Errata

The PIC18FXX2 Rev. B3/B4 parts you have received conform functionally to the Device Data Sheet (DS39564**B**), except for the anomalies described below.

All the issues listed here will be addressed in future revisions of the PIC18FXX2 silicon.

The following silicon errata apply only to PIC18FXX2 devices with these Device/Revision IDs:

Part Number	Device ID	Revision ID
PIC18F242	00 0100 100	00101
PIC18F252	00 0100 000	00101
PIC18F442	00 0100 101	00101
PIC18F452	00 0100 001	00101

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFFEh:3FFFFFh in the device's configuration space. They are shown in hexadecimal in the format "DEVID2 DEVID1".

1. Module: Program Memory

Data corruption may occur during a table write operation if a peripheral interrupt also occurs. This happens only when the interrupt enable bit (PIE or INTCON register) for the corresponding interrupt has also been set.

Work around

Before executing any table write instructions, disable ALL peripheral interrupts. This is best done by clearing all interrupt enable bits in the three Interrupt Control registers (INTCON, INTCON2 and INTCON3) and both Peripheral Interrupt Enable registers (PIE1 and PIE2). After the table write is complete, restore all INTCON and PIE registers to their pre-instruction state.

Date Codes that pertain to this issue:

All engineering and production devices.

2. Module: Data EEPROM

When reading the data EEPROM, the contents of the EEDATA register may become corrupted in the second instruction cycle after the RD bit (EECON1<0>) is set. The actual contents of the EEPROM remains unaffected.

Work around

To ensure the integrity of the contents of EEDATA, the register must be read in the instruction immediately following the setting of the RD bit. Use the `MOVF` or `MOVFF` instructions to do this (see Example 1).

Additionally, all interrupts must be disabled prior to the read instruction sequence. Interruptions of the sequence may have the same result of altering the contents of EEDATA.

EXAMPLE 1: SUGGESTED SEQUENCE FOR READING EEDATA

```
    •
    •
BCF    INTCON,GIEH ;disable interrupts
                   ;if using interrupts
BSF    EECON1,RD   ;start the read operation
MOVF   EEDATA,W    ;move the data out of
                   ;EEDATA
BSF    INTCON,GIEH ;enable interrupts
                   ;if using interrupts
    •
    •
```

Date Codes that pertain to this issue:

All engineering and production devices.

3. Module: Interrupts

Under certain conditions, the use of dual priority interrupts may cause a program instruction to be skipped entirely. This has only been observed when both of the following apply:

- Both high and low interrupts are enabled, and
- A high priority asynchronous interrupt occurs in the following cycle after any low priority interrupt.

The event causes the stack to get pushed twice and will eventually result in an overflow.

Work around

Two possible solutions are presented. Other solutions may exist.

1. Enable only high priority interrupts for all sources, both synchronous and asynchronous.
2. If it is necessary to use both high and low interrupt priorities:
   - Assign asynchronous interrupts as low priority only.

Note:	This does not apply to the INT0 (external) interrupt as it is always configured as a high priority interrupt.

   - Assign synchronous interrupts to both high and low priority, as needed.

Date Codes that pertain to this issue:

All engineering and production devices.

4. Module: Core (Program Memory Space)

Performing table read operations above the user program memory space (addresses over 1FFFFFh) may yield erroneous results at the extreme low end of the device's rated temperature range (-40°C).

This applies specifically to addresses above 1FFFFFh, including the user ID locations (200000h-200007h), the configuration bytes (300000h-30000Dh), and the device ID locations (3FFFFEh and 3FFFFFh). User program memory is unaffected.

Work around

Three possible work arounds are presented. Other solutions may exist.

1. Do not perform table read operations on areas above the user memory space at -40°C.
2. Insert `NOP` instructions (specifically, literal FFFFh) around any table read instructions. The suggested optimal number is 4 instructions before and 8 instructions after each table read. This may vary depending upon the particular application, and should be optimized by the user.

Date Codes that pertain to this issue:

All engineering and production devices.

5. Module: Core (Program Memory Space)

Note:	This issue applies **only** to PIC18F252 and PIC18F452 devices with 32K words of Flash program memory. PIC18F242 and PIC18F442 devices are **not** affected.

Under certain conditions, the execution of a table read instruction may yield erroneous results. This has been observed when a table read instruction and its read destination, as indicated by the Table Pointer registers, are on opposite sides of the 4000h program memory address boundary.

This behavior has not been observed when the instruction and its target both occur strictly within the same half of the program memory space.

Work around

Insert a data word of value FFFFh immediately following any table read instruction. This behaves as a `NOP` instruction when executed. Using the actual `NOP` instruction instead of a literal FFFFh may not have the same results.

This is a recommended solution. Others may exist.

Date Codes that pertain to this issue:

All engineering samples and devices with date codes up to and including 0252 (Year 2002, Work Week 52).

6. Module: Core (Program Memory Space)

Note: This issue applies **only** to PIC18F252 and PIC18F452 devices with 32K words of Flash program memory. PIC18F242 and PIC18F442 devices are **not** affected.

Under certain conditions, the execution of some control operations may yield unexpected results. This has been observed when any of the following instructions vector code execution across the 4000h program memory address boundary:

- CALL
- GOTO
- RETURN
- RETLW
- RETFIE

In addition, unexpected operation may result when an interrupt causes the device to jump across the 4000h boundary to the appropriate interrupt vector.

There are no known issues related to any of these instructions when execution occurs strictly above or below the 4000h address boundary.

Work around

Three possible solutions are presented. Others may exist. It is recommended to implement any one, or any combination of the three, as needed.

1. Insert a data word of value FFFFh as the first instruction in the destination of a CALL or GOTO.
2. Insert a data word of FFFFh at the interrupt vector address(es) (0008h and/or 0018h).
3. Insert a data word of value FFFFh immediately following any RETURN, RETLW, or RETFIE instruction.

In each of these instances, the literal data behaves as a NOP instruction when executed. Using the actual NOP instruction instead of a literal FFFFh may not have the same results.

Date Codes that pertain to this issue:

All engineering samples and devices with date codes up to and including 0252 (Year 2002, Work Week 52).

7. Module: Data EEPROM

When reading the data EEPROM, the contents of the EEDATA register may be corrupted if the RD bit (EECON1<0>) is set immediately following a write to the address byte (EEADR). The actual contents of the data EEPROM remain unaffected.

Work around

Do not set EEADR immediately before the execution of a read. Write to EEADR at least one instruction cycle before setting the RD bit. The instruction between the write to EEADR and the read can be any valid instruction including a NOP.

Date Codes that pertain to this issue:

All engineering and production devices.

8. Module: MSSP (All I²C™ and SPI™ Modes)

The Buffer Full (BF) flag bit of the SSPSTAT register (SSPSTAT<0>) may be inadvertently cleared even when the SSPBUF register has not been read. This will occur only when the following two conditions occur simultaneously:

- The four Least Significant bits of the BSR register are equal to 0Fh (BSR<3:0> = 1111) and
- Any instruction that contains C9h in its 8 Least Significant bits (i.e., register file addresses, literal data, address offsets, etc.) is executed.

Work around

All work arounds will involve setting the contents of BSR<3:0> to some value other than 0Fh.

In addition to those proposed below, other solutions may exist.

1. When developing or modifying code, keep these guidelines in mind:
   - Assign 12-bit addresses to all variables. This allows the assembler to know when Access Banking can be used.
   - Do not set the BSR to point to Bank 15 (BSR = 0Fh).
   - Allow the assembler to manipulate the access bit present in most instructions. Accessing the SFRs in Bank 15 will be done through the Access Bank. Continue to use the BSR to select all GPR Banks.
2. If accessing a part of Bank 15 is required and the use of Access Banking is not possible, consider using indirect addressing.
3. If pointing the BSR to Bank 15 is unavoidable, review the absolute file listing. Verify that no instructions contain C9h in the 8 Least Significant bits while the BSR points to Bank 15 (BSR = 0Fh).

Date Codes that pertain to this issue:

All engineering and production devices.

9. Module: MSSP (SPI, Slave Mode)

In its current implementation, the $\overline{SS}$ (Slave Select) control signal generated by an external master processor may not be successfully recognized by the PIC® microcontroller operating in Slave Select mode (SSPM3:SSPM0 = 0100). In particular, it has been observed that faster transitions (those with shorter fall-times) are more likely to be missed than than slower transitions.

Work around

Insert a series resistor between the source of the $\overline{SS}$ signal and the corresponding $\overline{SS}$ input line of the microcontroller. The value of the resistor is dependent on both the application system's characteristics and process variations between microcontrollers. Experimentation and thorough testing is encouraged.

This is a recommended solution. Others may exist.

Date Codes that pertain to this issue:

All engineering and production devices.

10. Module: Core (Instruction Set)

The Decimal Adjust W register instruction, DAW, may improperly clear the Carry bit (STATUS<0>) when executed.

Work around

Test the Carry bit state before executing the DAW instruction. If the Carry bit is set, increment the next higher byte to be added using an instruction such as INCFSZ (this instruction does not affect any Status flags, and will not overflow a BCD nibble). After the DAW instruction has been executed, process the Carry bit normally (see Example 2).

EXAMPLE 2: PROCESSING THE CARRY BIT DURING BCD ADDITIONS

```
MOVLW   0x80        ; .80 (BCD)
ADDLW   0x80        ; .80 (BCD)

BTFSC   STATUS,C    ; test C
INCFSZ  byte2       ; inc next higher LSB
DAW
BTFSC   STATUS,C    ; test C
INCFSZ  byte2       ; inc next higher LSB

This is repeated for each DAW instruction.
```

11. Module: Timer1 Oscillator

After the system clock source for the microcontroller is switched from the primary oscillator to the Timer1 oscillator, an increase in system current consumption may occur.

Work around

None

Date Codes that pertain to this issue:

All engineering and production devices.

12. Module: Reset

It has been observed that in certain Reset conditions, including power-up, the first GOTO instruction at address 0x0000 may not be executed. This occurrence is rare and affects very few applications.

To determine if your system is affected, test a statistically significant number of applications across the operating temperature, voltage and frequency ranges of the application. Affected systems will repeatably fail normal testing. Systems not affected will continue to not be affected over time.

Work around

Insert a NOP instruction at address 0x0000.

Date Codes that pertain to this issue:

All engineering and production devices.

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS39564**B**), the following clarifications and corrections should be noted.

1. Module: DC Characteristics

Some of the maximum values for parameters D022A and D022B shown in **Section 22.1 "DC Characteristics"** of the Device Data Sheet have changed (modified text in bold):

22.1 DC Characteristics: PIC18FXX2 (Industrial, Extended) PIC18LFXX2 (Industrial)

PIC18LFXX2 (Industrial)			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial				
PIC18FXX2 (Industrial, Extended)			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
		Module Differential Current					
D022A	ΔIBOR	**Brown-out Reset**	—	29	**40**	μA	VDD = 2.0V, +25°C
		PIC18LFXX2	—	29	45	μA	VDD = 2.0V, -40°C to +85°C
			—	33	50	μA	VDD = 4.2V, -40°C to +85°C
D022A		**Brown-out Reset**	—	36	**45**	μA	VDD = 4.2V, +25°C
		PIC18FXX2	—	36	50	μA	VDD = 4.2V, -40°C to +85°C
			—	36	65	μA	VDD = 4.2V, -40°C to +125°C
D022B	ΔILVD	**Low Voltage Detect**	—	29	**40**	μA	VDD = 2.0V, +25°C
		PIC18LFXX2	—	29	45	μA	VDD = 2.0V, -40°C to +85°C
			—	33	50	μA	VDD = 4.2V, -40°C to +85°C
D022B		**Low Voltage Detect**	—	33	**45**	μA	VDD = 4.2V, +25°C
		PIC18FXX2	—	33	50	μA	VDD = 4.2V, -40°C to +85°C
			—	33	65	μA	VDD = 4.2V, -40°C to +125°C

Legend: Shading of rows is to assist in readability of the table.

Note 1: This is the limit to which VDD can be lowered in Sleep mode, or during a device Reset, without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.
The test conditions for all IDD measurements in active Operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD
$\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

3: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in hi-impedance state and tied to VDD or VSS, and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR,...).

4: For RC osc configuration, current through REXT is not included. The current through the resistor can be estimated by the formula Ir = VDD/2REXT (mA) with REXT in kΩ.

2. Module: Packaging (Pinout and Product Identification)

PIC18F442 and PICF452 devices are now offered in 44-pin, near chip-scale micro lead frame packages (commonly known as “QFN”). This packaging type has been added to the product line since the latest revision of the Device Data Sheet.

The addition of this option requires the following additions to the Device Data Sheet (DS39564**B**). The referenced figures and tables follow this text.

1. The **“Pin Diagrams”** on pages 2-3 of the Data Sheet are amended with the addition of the 44-pin QFN pinout, shown in Figure 1.
2. Table 1-3 of **Section 1.0 “Overview”** is replaced with an updated version which adds a column for QFN pin assignments. A row is also added for previously unlisted NC pins. All new information is indicated in **bold**.
3. **Section 24.1 “Package Marking Information”** is amended to include a marking template and example for 44-pin QFN devices. These are shown in Figure 2.
4. **Section 24.2 (Package Details”** is amended to include the mechanical drawing of the 44-pin QFN package following the existing drawings, shown in Figure 3.
5. In the **“PIC18F442/452 Product Identification System”** (page 329), the “Package” options are amended to include the new line item:

   ML = QFN

   For the sake of completeness, it is also noted that the package designation “MLF” is now replaced by “QFN” in all occurrences throughout the Device Data Sheet. “MLF” should be considered an obsoleted term.

FIGURE 1: PINOUT DIAGRAM FOR PIC18F442/452, 44-PIN QFN PACKAGE

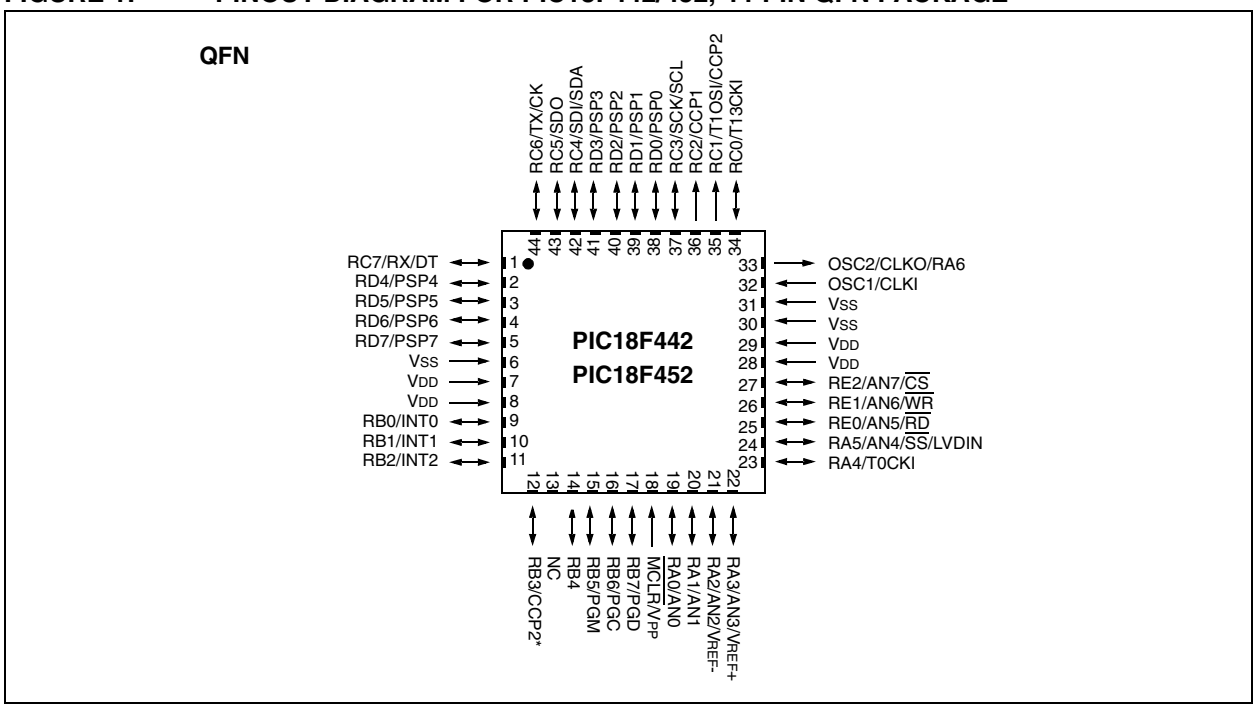


FIGURE 2: PACKAGE MARKING TEMPLATE FOR PIC18F442/452, 44-PIN QFN

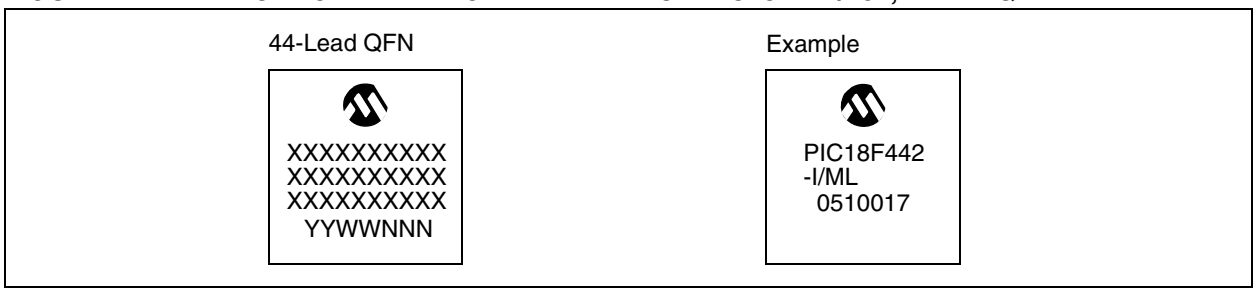


TABLE 1-3: PIC18F4X2 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	DIP	PLCC	QFN	TQFP			
$\overline{MCLR}$/VPP	1	2	**18**	18			Master Clear (input) or high voltage ICSP™ programming enable pin.
$\overline{MCLR}$					I	ST	Master Clear (Reset) input. This pin is an active low Reset to the device.
VPP					I	ST	High-Voltage ICSP programming enable pin.
NC	—		**32**		—	—	These pins should be left unconnected.
OSC1/CLKI	13	14	**33**	30			Oscillator crystal or external clock input.
OSC1					I	ST	Oscillator crystal input or external clock source input. ST buffer when configured in RC mode, CMOS otherwise.
CLKI					I	CMOS	External clock source input. Always associated with pin function OSC1. (See related OSC1/CLKI, OSC2/CLKO pins.)
OSC2/CLKO/RA6	14	15		31			Oscillator crystal or clock output.
OSC2					O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
CLKO					O	—	In RC mode, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
RA6					I/O	TTL	General Purpose I/O pin.
							PORTA is a bidirectional I/O port.
RA0/AN0	2	3	**19**	19			
RA0					I/O	TTL	Digital I/O.
AN0					I	Analog	Analog input 0.
RA1/AN1	3	4	**20**	20			
RA1					I/O	TTL	Digital I/O.
AN1					I	Analog	Analog input 1.
RA2/AN2/VREF-	4	5	**21**	21			
RA2					I/O	TTL	Digital I/O.
AN2					I	Analog	Analog input 2.
VREF-					I	Analog	A/D Reference Voltage (Low) input.
RA3/AN3/VREF+	5	6	**22**	22			
RA3					I/O	TTL	Digital I/O.
AN3					I	Analog	Analog input 3.
VREF+					I	Analog	A/D Reference Voltage (High) input.
RA4/T0CKI	6	7	**23**	23			
RA4					I/O	ST/OD	Digital I/O. Open-drain when configured as output.
T0CKI					I	ST	Timer0 external clock input.
RA5/AN4/$\overline{SS}$/LVDIN	7	8	**24**	24			
RA5					I/O	TTL	Digital I/O.
AN4					I	Analog	Analog input 4.
$\overline{SS}$					I	ST	SPI™ Slave Select input.
LVDIN					I	Analog	Low-Voltage Detect input.
RA6							(See the OSC2/CLKO/RA6 pin.)

Legend: TTL = TTL compatible input
CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels
I = Input
O = Output
P = Power
OD = Open Drain (no P diode to VDD)

TABLE 1-3: PIC18F4X2 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	DIP	PLCC	QFN	TQFP			
							PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs.
RB0/INT0	33	36	**9**	8			
RB0					I/O	TTL	Digital I/O.
INT0					I	ST	External Interrupt 0.
RB1/INT1	34	37	**10**	9			
RB1					I/O	TTL	Digital I/O.
INT1					I	ST	External Interrupt 1.
RB2/INT2	35	38	**11**	10			
RB2					I/O	TTL	Digital I/O.
INT2					I	ST	External Interrupt 2.
RB3/CCP2	36	39	**12**	11			
RB3					I/O	TTL	Digital I/O.
CCP2					I/O	ST	Capture2 input, Compare2 output, PWM2 output.
RB4	37	41	**14**	14	I/O	TTL	Digital I/O. Interrupt-on-change pin.
RB5/PGM	38	42	**15**	15			
RB5					I/O	TTL	Digital I/O. Interrupt-on-change pin.
PGM					I/O	ST	Low-Voltage ICSP™ programming enable pin.
RB6/PGC	39	43	**16**	16			
RB6					I/O	TTL	Digital I/O. Interrupt-on-change pin.
PGC					I/O	ST	In-Circuit Debugger and ICSP programming clock pin.
RB7/PGD	40	44	**17**	17			
RB7					I/O	TTL	Digital I/O. Interrupt-on-change pin.
PGD					I/O	ST	In-Circuit Debugger and ICSP programming data pin.

Legend: TTL = TTL compatible input
CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels
I = Input
O = Output
P = Power
OD = Open Drain (no P diode to V_{DD})

TABLE 1-3: PIC18F4X2 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	DIP	PLCC	QFN	TQFP			
							PORTC is a bidirectional I/O port.
RC0/T1OSO/T1CKI	15	16	**34**	32			
RC0					I/O	ST	Digital I/O.
T1OSO					O	—	Timer1 oscillator output.
T1CKI					I	ST	Timer1/Timer3 external clock input.
RC1/T1OSI/CCP2	16	18	**35**	35			
RC1					I/O	ST	Digital I/O.
T1OSI					I	CMOS	Timer1 oscillator input.
CCP2					I/O	ST	Capture2 input, Compare2 output, PWM2 output.
RC2/CCP1	17	19	**36**	36			
RC2					I/O	ST	Digital I/O.
CCP1					I/O	ST	Capture1 input/Compare1 output/ PWM1 output.
RC3/SCK/SCL	18	20	**37**	37			
RC3					I/O	ST	Digital I/O.
SCK					I/O	ST	Synchronous serial clock input/output for SPI™ mode.
SCL					I/O	ST	Synchronous serial clock input/output for I^2C™ mode.
RC4/SDI/SDA	23	25	**42**	42			
RC4					I/O	ST	Digital I/O.
SDI					I	ST	SPI Data In.
SDA					I/O	ST	I^2C Data I/O.
RC5/SDO	24	26	**43**	43			
RC5					I/O	ST	Digital I/O.
SDO					O	—	SPI Data Out.
RC6/TX/CK	25	27	**44**	44			
RC6					I/O	ST	Digital I/O.
TX					O	—	USART Asynchronous Transmit.
CK					I/O	ST	USART Synchronous Clock (see related RX/DT).
RC7/RX/DT	26	29	**1**	1			
RC7					I/O	ST	Digital I/O.
RX					I	ST	USART Asynchronous Receive.
DT					I/O	ST	USART Synchronous Data (see related TX/CK).

Legend: TTL = TTL compatible input
CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels
I = Input
O = Output
P = Power
OD = Open Drain (no P diode to VDD)

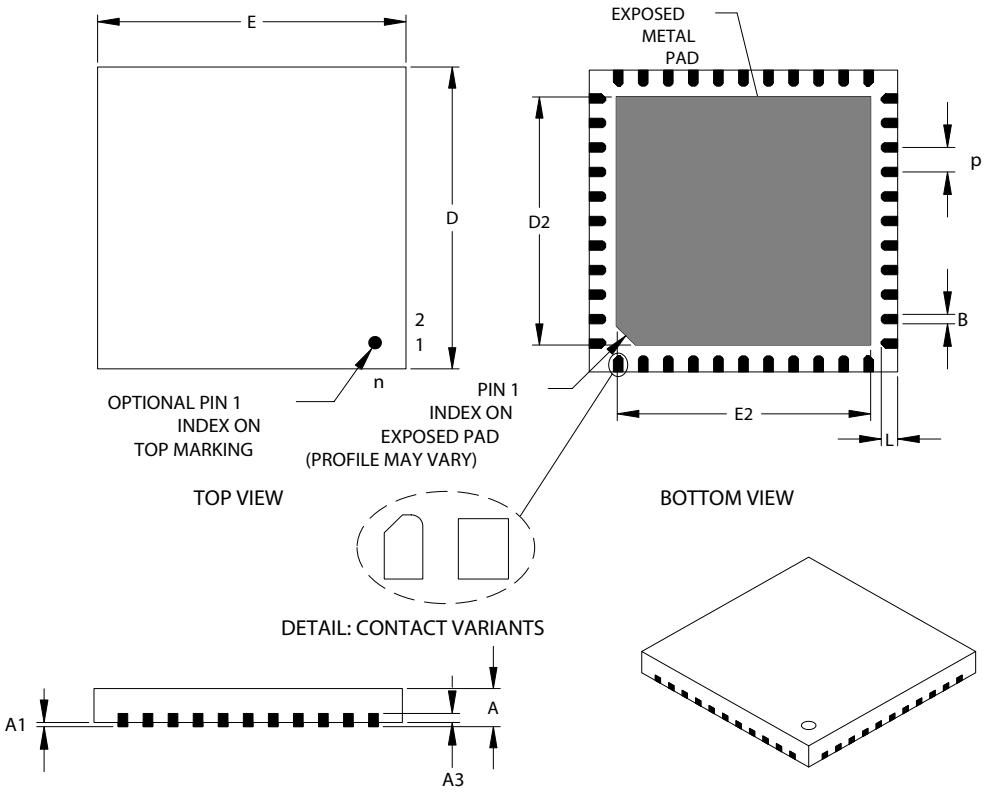
TABLE 1-3: PIC18F4X2 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	DIP	PLCC	QFN	TQFP			
							PORTD is a bidirectional I/O port, or a Parallel Slave Port (PSP) for interfacing to a microprocessor port. These pins have TTL input buffers when PSP module is enabled.
RD0/PSP0	19	21	**38**	38	I/O	ST TTL	Digital I/O. Parallel Slave Port Data.
RD1/PSP1	20	22	**39**	39	I/O	ST TTL	Digital I/O. Parallel Slave Port Data.
RD2/PSP2	21	23	**40**	40	I/O	ST TTL	Digital I/O. Parallel Slave Port Data.
RD3/PSP3	22	24	**41**	41	I/O	ST TTL	Digital I/O. Parallel Slave Port Data.
RD4/PSP4	27	30	**2**	2	I/O	ST TTL	Digital I/O. Parallel Slave Port Data.
RD5/PSP5	28	31	**3**	3	I/O	ST TTL	Digital I/O. Parallel Slave Port Data.
RD6/PSP6	29	32	**4**	4	I/O	ST TTL	Digital I/O. Parallel Slave Port Data.
RD7/PSP7	30	33	**5**	5	I/O	ST TTL	Digital I/O. Parallel Slave Port Data.
							PORTE is a bidirectional I/O port.
RE0/$\overline{RD}$/AN5 RE0 $\overline{RD}$ AN5	8	9	**25**	25	I/O	 ST TTL Analog	 Digital I/O. Read control for parallel slave port (see also $\overline{WR}$ and $\overline{CS}$ pins). Analog input 5.
RE1/$\overline{WR}$/AN6 RE1 $\overline{WR}$ AN6	9	10	**26**	26	I/O	 ST TTL Analog	 Digital I/O. Write control for parallel slave port (see $\overline{CS}$ and $\overline{RD}$ pins). Analog input 6.
RE2/$\overline{CS}$/AN7 RE2 $\overline{CS}$ AN7	10	11	**27**	27	I/O	 ST TTL Analog	 Digital I/O. Chip Select control for parallel slave port (see related $\overline{RD}$ and $\overline{WR}$). Analog input 7.
V_{SS}	12, 31	13, 34	**6, 30, 31**	6, 29	P	—	Ground reference for logic and I/O pins.
V_{DD}	11, 32	12, 35	**7, 8, 28, 29**	7, 28	P	—	Positive supply for logic and I/O pins.
NC	**—**	**1, 17, 28**	**13**	**12, 13, 33, 34**	**—**	**—**	**These pins are not internally connected. They should be left unconnected.**

Legend: TTL = TTL compatible input
CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels
I = Input
O = Output
P = Power
OD = Open Drain (no P diode to V_{DD})

FIGURE 3: 44-PIN QFN PACKAGE

44-Lead Plastic Quad Flat No Lead Package (ML) 8x8 mm Body (QFN)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Contacts	n		44			44	
Pitch	p		.026 BSC [1]			0.65 BSC [1]	
Overall Height	A	.031	.035	.039	0.80	0.90	1.00
Standoff	A1	.000	.001	.002	0	0.02	0.05
Base Thickness	A3		.010 REF [2]			0.25 REF [2]	
Overall Width	E	.309	.315	.321	7.85	8.00	8.15
Exposed Pad Width	E2	.246	.268	.274	6.25	6.80	6.95
Overall Length	D	.309	.315	.321	7.85	8.00	8.15
Exposed Pad Length	D2	.246	.268	.274	6.25	6.80	6.95
Contact Width	B	.008	.013	.013	0.20	0.33	0.35
Contact Length	L	.014	.016	.019	0.35	0.40	0.48

*Controlling Parameter

Notes:

1. BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   See ASME Y14.5M
2. REF: Reference Dimension, usually without tolerance, for information purposes only.
   See ASME Y14.5M

JEDEC equivalent: M0-220

Drawing No. C04-103

Revised 3-14-05

REVISION HISTORY

Rev A Document (4/2002)

First revision of this document, silicon issues 1 (Program Memory) and 2 (Data EEPROM) and data sheet issues 1 (Interrupts), 2 and 3 (USART) and 4 (Program Memory).

Rev B Document (7/2002)

Added silicon issues 3 and 4 (Interrupts and Core - Program Memory Space).

Rev C Document (10/2002)

All data sheet issues were removed. Added silicon issues 5, 6 and 7 (Core - Program Memory Space and Data EEPROM).

Rev D Document (1/2003)

Updated date code information for silicon issues 5 and 6 (Core - Program Memory Space), and added data sheet issue 1 (DC Characteristics). Rev. B4 Silicon was included along with Rev. B3 Silicon in this document revision.

Rev E Document (3/2003)

Updated silicon issue 6 (Core - Program Memory Space). Added silicon issues 8, 9 and 10 (MSSP and Core - Instruction Set) and data sheet clarification 2 (Packaging - Pinout and Product Identification).

Rev F Document (7/2003)

Added silicon issue 11 (Timer1 Oscillator).

Rev G Document (05/2005)

Added silicon issue 12 (Reset).

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