

**ISO/IEC 7816-3**    **ISO/IEC 7816-12**


## DESCRIPTION

The Teridian 73S8009CN is the world's first single-chip smart card electrical interface circuit that supports all types of smart cards: 5V, 3V and 1.8V, including traditional ISO-7816-3 asynchronous and synchronous type 1 and type 2, as well as USB, ISO-7816-12 cards.

The 73S8009CN is ideally suited for applications such as desktop computers, laptops and general purpose smart card readers that require low power operation from a single 2.7V to 6.5V power supply voltage source. A power down mode ("OFF" mode) is available and exhibits a 10nA typical current consumption.

The circuit provides control, conversion and regulation of power for the smart card. In addition, the circuit provides a 3.3V-regulated voltage that is used as an internal digital supply voltage to the host interface. It is also made available to supply power to some external circuitry (a host controller for instance).

For asynchronous and synchronous smart card operation, the signals for RST, CLK, I/O and auxiliary signals AUX1 and AUX2 are directly controlled from the host processor and are level-shifted by the circuit to the selected  $V_{CC}$  value. For more design flexibility, the host processor is responsible for handling the signal timing for smart card activation and de-activation under normal conditions.

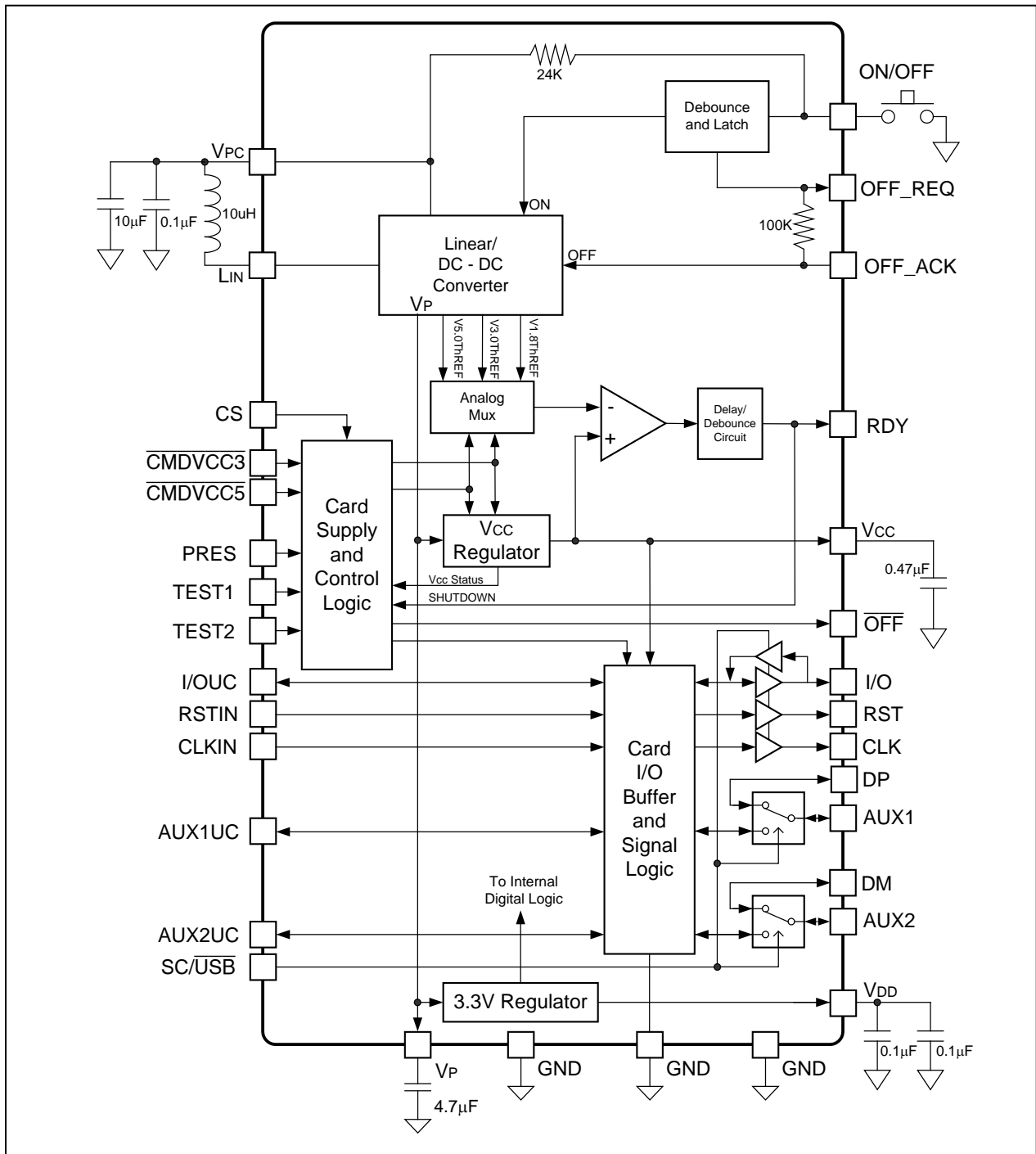
The power management circuitry allows operation from a single power supply source  $V_{PC}$  (2.7V to 6.5V).  $V_{PC}$  is converted using an inductive, step-up power converter to the intermediate voltage,  $V_P$ .  $V_P$  is used by linear voltage regulators and switches internal to the IC to create the voltages  $V_{DD}$  and as required,  $V_{CC}$ .  $V_{DD}$  is used by the 73S8009CN and is also made available for the companion host processor circuit or for other external circuits.

The 73S8009CN features an ON/OFF pin suitable to connect to a "push-on/push-off" main system switch. When the 73S8009CN is "OFF," the typical current drawn from  $V_{PC}$  is 10nA. For applications that do not implement any ON/OFF system switch, the ON/OFF input pin can be driven from a digital output of the host processor.

## FEATURES

- Smart Card Interface:
  - Smart card voltage  $V_{CC}$ :
    - Selectable: 1.8V, 3V or 5V
    - Generated by an internal voltage regulator
    - Provides up to 65mA to 3V and 5V cards and up to 40mA to 1.8V cards
  - ISO-7816-3 card emergency deactivation
  - Voltage supervisor detects voltage drop on  $V_{CC}$  (card supply)
  - True card over-current detection 150mA max.
  - 1 input for a card presence detection switch
  - Auxiliary I/O lines for synchronous and ISO-7816-12 USB card support
  - Proper isolation of smart card signals depending on smart card type
  - Card CLK clock frequency up to 20MHz
  - 6kV ESD and short circuit protection on the card interface
- System Controller Interface:
  - Digital logic level: 3.3V
  - 5 signal images of the card signals (RSTIN, CLKIN, I/OUC, AUX1UC and AUX2UC)
  - 1 control signal to switch between synchronous / asynchronous and ISO-7816-12 USB smart card modes
  - 2 inputs activate and select the card voltage ( $\overline{CMDVCC5}$  and  $\overline{CMDVCC3}$ )
  - 2 outputs, interrupt to the system controller ( $\overline{OFF}$  and RDY), to inform the system controller of the card presence / faults and status of the interface
  - 1 Chip Select input
  - 2 handshaking signals (OFF\_REQ, OFF\_ACK) for proper shutdown sequencing of all smart card signals
- ON/OFF Input for a Main System Switch
- DC-DC Step-up Converter:
  - Generates an intermediary voltage  $V_P$
  - Requires a single 10 $\mu$ H Inductor (rated for 400mA maximum peak current)
- $V_{DD}$  power supply output available to power up external circuitry: 3.3V  $\pm$ 0.3V, 40mA
- Industrial temperature range (-40 °C to +85 °C)
- Small format QFN32 package: 5x5mm
- RoHS compliant (6/6) lead-free package

**FUNCTIONAL DIAGRAM**



**Figure 1: 73S8009CN Block Diagram**

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## 1 Pinout

The 73S8009CN is supplied as a 32-pin QFN package.

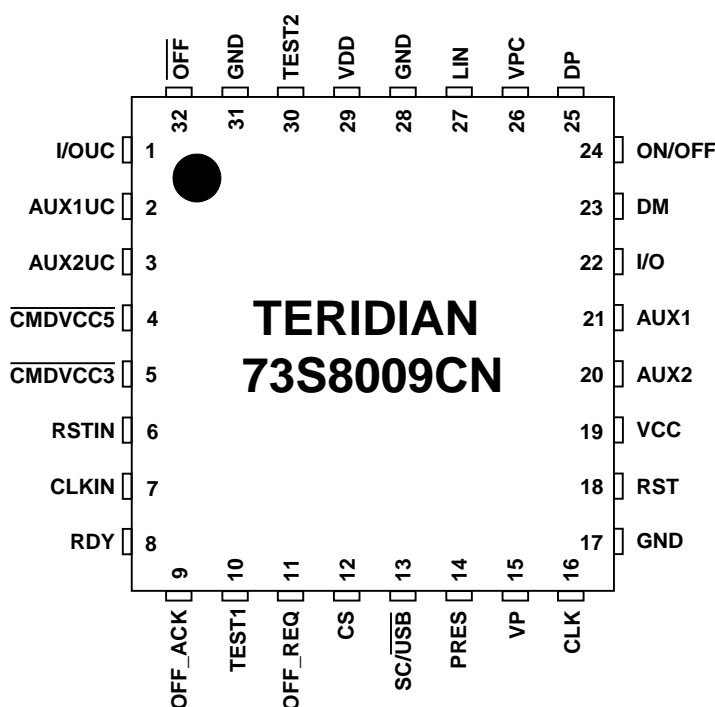


Figure 2: 73S8009CN 32-Pin QFN Pinout

Table 1 describes the pin functions for the device.

Table 1: 73S8009CN Pin Definitions

Pin Name	Pin Number	Type	Equivalent Circuit	Description
<b>Card Interface</b>				
I/O	22	IO	Figure 17	Card I/O: Data signal to/from smart card. Includes an 11kΩ pull-up resistor to $V_{CC}$ . Will be tri-stated when $\overline{SC/USB}$ is set low.
AUX1	21	IO	Figure 17	AUX1: Auxiliary data signal to/from smart card for synchronous smart card operation. Smart card USB DP signal for ISO-7816-12 USB smart card operation. Includes an 11kΩ pull-up resistor to $V_{CC}$ for synchronous / asynchronous operation only.
AUX2	20	IO	Figure 17	AUX2: Auxiliary data signal to/from smart card for synchronous smart card operation. Smart card USB DM signal for ISO-7816-12 USB smart card operation. Includes an 11kΩ pull-up resistor to $V_{CC}$ for synchronous / asynchronous operation only.
RST	18	O	Figure 16	Card reset: provides reset (RST) signal to card. RST is the pass through signal on RSTIN. Internal control logic will hold RST low when card is not activated or $V_{CC}$ is too low. Will be tri-stated when $\overline{SC/USB}$ is set low.

Pin Name	Pin Number	Type	Equivalent Circuit	Description
CLK	16	O	Figure 15	Card clock: provides clock signal (CLK) to card. CLK is the pass through of the signal on pin CLKIN. Internal control logic will hold CLK low when card is not activated or VCC is too low. Will be tri-stated when SC/ $\overline{\text{USB}}$ is set low.
PRES	14	I	Figure 19	Smart card Presence switch: Active high indicates card is present. Smart card activation will not be permitted unless PRES is active.
VCC	19	PSO	Figure 13	Card power supply – logically controlled by sequencer, output of LDO regulator. Requires an external 0.47 $\mu$ F low ESR filter capacitor to GND.
GND	17	GND	–	Card ground.
<b>Host Processor Interface</b>				
CS	12	I	Figure 19	Chip Select. When CS = 1, the control and signal pins are configured normally. When CS is set low, $\overline{\text{CMDVCC5}}$ , RSTIN, and $\overline{\text{CMDVCC3}}$ are latched. I/OUC, AUX1UC, and AUX2UC are set to high-impedance pull-up mode and do not pass data to or from the smart card. Signals RDY and $\overline{\text{OFF}}$ are disabled to prevent a low output and the internal pull-up resistors are disconnected. Should be tied to VDD when a single 73S8009CN is used.
$\overline{\text{OFF}}$	32	O	Figure 12	Interrupt signal to the processor. Active Low - Multi-function indicating fault conditions and card presence. Open drain output configuration – It includes an internal 20k $\Omega$ pull-up to V <sub>DD</sub> . Pull-up is disabled in Power down state and CS = 0 modes.
I/OUC	1	IO	Figure 18	System controller data I/O to/from the card. Includes an 11k $\Omega$ pull-up resistor to V <sub>DD</sub> .
AUX1UC	2	IO	Figure 18	System controller auxiliary data I/O to/from the card for synchronous / asynchronous operation mode. Connection to AUX1 is opened when SC/ $\overline{\text{USB}}$ is low. Includes an 11k $\Omega$ pull-up resistor to V <sub>DD</sub> .
AUX2UC	3	IO	Figure 18	System controller auxiliary data I/O to/from the card for synchronous / asynchronous operation mode. Connection to AUX2 is opened when SC/ $\overline{\text{USB}}$ is low. Includes an 11k $\Omega$ pull-up resistor to V <sub>DD</sub> .
SC/ $\overline{\text{USB}}$	13	I	Figure 19	Smart Card Interface enable, USB interface disable. Pin is provided with a weak pull-up. When high, the 73S8009CN operates in synchronous / asynchronous operation mode. When low, CLK, RST I/O, AUX1, and AUX2 are tri-stated. Pin AUX1 is connected to pin DP and pin AUX2 is connected to pin DM.
DP	25	IO	Figure 14	USB D+ connection to / from USB controller. When SC/ $\overline{\text{USB}}$ is set low, this pin is electrically connected to the AUX1 pin, otherwise it is isolated.

Pin Name	Pin Number	Type	Equivalent Circuit	Description															
DM	23	IO	Figure 14	USB D- connection to / from USB controller. When SC/ $\overline{\text{USB}}$ is set low, this pin is electrically connected to the AUX1 pin, otherwise it is isolated.															
$\overline{\text{CMDVCC5}}$ $\overline{\text{CMDVCC3}}$	4 5	I I	Figure 19	Logic low on one or both of these pins will cause the LDO regulator to ramp the V <sub>CC</sub> supply to the smart card and smart card interface to the value described in the following table: <table border="1"> <thead> <tr> <th><math>\overline{\text{CMDVCC5}}</math></th> <th><math>\overline{\text{CMDVCC3}}</math></th> <th>V<sub>CC</sub> Output Voltage</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1.8V</td> </tr> <tr> <td>0</td> <td>1</td> <td>5.0V</td> </tr> <tr> <td>1</td> <td>0</td> <td>3.0V</td> </tr> <tr> <td>1</td> <td>1</td> <td>V<sub>CC</sub> Off</td> </tr> </tbody> </table> Note: See Card Power Supply and Voltage Supervision for more details.	$\overline{\text{CMDVCC5}}$	$\overline{\text{CMDVCC3}}$	V <sub>CC</sub> Output Voltage	0	0	1.8V	0	1	5.0V	1	0	3.0V	1	1	V <sub>CC</sub> Off
$\overline{\text{CMDVCC5}}$	$\overline{\text{CMDVCC3}}$	V <sub>CC</sub> Output Voltage																	
0	0	1.8V																	
0	1	5.0V																	
1	0	3.0V																	
1	1	V <sub>CC</sub> Off																	
RSTIN	6	I	Figure 19	Reset Input: This signal is the reset command to the card.															
RDY	8	O	Figure 12	Signal to controller indicating the 73S8009CN is ready because V <sub>CC</sub> is above the required value after $\overline{\text{CMDVCC5}}$ and/or $\overline{\text{CMDVCC3}}$ is asserted low. A 20k $\Omega$ pull-up resistor to V <sub>DD</sub> is provided internally. Pull-up is disabled in Power down state and CS=0 modes.															
ON/OFF	24	I	Figure 11	Power control pin. Connected to normally open SPST switch to ground. Closing switch for duration greater than de-bounce period will turn 73S8009CN circuit "on". If the 73S8009CN is "on," closing the switch will turn 73S8009CN to "off" state after the de-bounce period and OFF_REQ/OFF_ACK handshake. Can be controlled by a host processor digital output.															
OFF_REQ	11	O	Figure 19	Digital output. Request to the host system controller to turn the 73S8009CN off. If ON_OFF switch is closed (to ground) for de-bounce duration and circuit is "on," OFF_REQ will go high (request to turn OFF). Connected to OFF_ACK via 100k $\Omega$ internal resistor.															
OFF_ACK	13	I	Figure 19	Setting OFF_ACK high will power "off" all analog functions and disconnect the 73S8009CN from V <sub>PC</sub> . The pin has an internal 100k $\Omega$ resistor connection to OFF_REQ so that when not connected or no host interaction is required, the Acknowledge will be true and the circuit will turn "off" after the deactivation sequence is completed.															
<b>Miscellaneous</b>																			
CLKIN	7	I	Figure 19	Clock signal source for the card clock.															
TEST1	10	–	–	Factory test pin. This pin must be tied to GND.															
TEST2	30	–	–	Factory test pin. This pin must be tied to GND.															

Pin Name	Pin Number	Type	Equivalent Circuit	Description
<b>Power Supply and Ground</b>				
VDD	29	PSO	Figure 13	System interface supply voltage output and supply voltage for companion controller circuit (40mA maximum source capability). Requires a minimum of two 0.1 $\mu$ F capacitors to ground for proper decoupling.
VPC	26	PSI	Figure 13	Power supply source for main voltage converter circuit. A 10 $\mu$ F and a 0.1 $\mu$ F ceramic capacitor must be connected to this pin.
LIN	27	PSI	Figure 13	Connection to 10 $\mu$ H inductor for internal step up converter. Note: inductor must be rated for 400mA maximum peak current.
VP	15	PSO	Figure 13	Intermediate output of main converter circuit. Requires an external 4.7 $\mu$ F low ESR filter capacitor to GND.
GND	28, 31	GND	–	Ground.



## 2 Electrical Specifications

This section provides the following:

- Absolute maximum ratings
- Recommended operating conditions
- Smart card interface requirements
- Digital signals characteristics
- Voltage / temperature fault detection circuits
- Thermal characteristics

### 2.1 Absolute Maximum Ratings

Table 2 lists the maximum operating conditions for the 73S8009CN. Permanent device damage may occur if absolute maximum ratings are exceeded. Exposure to the extremes of the absolute maximum rating for extended periods may affect device reliability.

**Table 2: Absolute Maximum Device Ratings**

Parameter	Rating
Supply Voltage $V_{PC}$	-0.5 to 7.0 VDC
$V_{DD}$	-0.5 to 4.0 VDC
Input Voltage for Digital Inputs	-0.3 to ( $V_{DD} + 0.5$ ) VDC
Storage Temperature	-65 to 150°C
Pin Voltage (except card interface)	-0.3 to ( $V_{DD} + 0.5$ ) VDC
Pin Voltage (card interface)	-0.3 to ( $V_{CC} + 0.3$ ) VDC
Pin Voltage, LIN pin	0.3 to 6.5 VDC
ESD Tolerance – Card interface, DP and DM pins	+/- 6kV
ESD Tolerance – Other pins	+/- 2kV
Pin Current, except LIN	$\pm 200$ mA
Pin Current, LIN	+ 500 mA in, -200 mA out

### 2.2 Recommended Operating Conditions

Function operation should be restricted to the recommended operating conditions specified in Table 3.

**Table 3: Recommended Operating Conditions**

Parameter	Rating
Supply voltage $V_{PC}$	2.7 to 6.5 VDC
Ambient operating temperature	-40°C to +85°C

## 2.3 Smart Card Interface Requirements

Table 4 lists the 73S8009CN Smart Card interface requirements.

**Table 4: DC Smart Card Interface Requirements**

Symbol	Parameter	Condition	Min	Nom	Max	Unit
<b>Card Power Supply (<math>V_{CC}</math>) Regulator</b>						
<b>General Conditions: <math>-40^{\circ}\text{C} &lt; 85^{\circ}\text{C}</math>, <math>2.7\text{ V} &lt; V_{PC} &lt; 6.5\text{ V}</math></b>						
$V_{CC}$	Card supply voltage including ripple and noise	Inactive mode	-0.1	–	0.1	V
		Inactive mode $I_{CC} = 1\text{mA}$	-0.1	–	0.4	V
		Active mode; $I_{CC} < 65\text{mA}$ ; 5V	4.65	–	5.25	V
		Active mode; $I_{CC} < 65\text{mA}$ ; 3V	2.85	–	3.15	V
		Active mode; $I_{CC} < 40\text{mA}$ ; 1.8V	1.68	–	1.92	V
		Active mode; single pulse of 100mA for 2 $\mu\text{s}$ ; 5 volt, fixed load = 25mA	4.6	–	5.25	V
		Active mode; single pulse of 100mA for 2 $\mu\text{s}$ ; 3V, fixed load = 25mA	2.76	–	3.15	V
		Active mode; current pulses of 40nAs with peak $ I_{CC}  < 200\text{mA}$ , $t < 400\text{ns}$ ; 5V	4.6	–	5.25	V
		Active mode; current pulses of 40nAs with peak $ I_{CC}  < 200\text{mA}$ , $t < 400\text{ns}$ ; 3V	2.7	–	3.15	V
		Active mode; current pulses of 20nAs with peak $ I_{CC}  < 100\text{mA}$ , $t < 400\text{ns}$ ; 1.8V	1.62	–	1.92	V
$V_{CCrip}$	$V_{CC}$ ripple	$f_{RIPPLE} = 20\text{KHz} - 200\text{MHz}$		–	350	mV
$I_{CCmax}$	Card supply output current	Static load current, $V_{CC} > 1.65$		–	40	mA
		Static load current, $V_{CC} > 4.6$ or 2.7 volts as selected		–	65	mA
$I_{CCF}$	$I_{CC}$ fault current	Class A, B (5V and 3V)	75	–	150	mA
		Class C (1.8V)	55	–	130	mA
$V_S$	$V_{CC}$ slew rate, rise and fall	$C = 0.5\mu\text{F}$	0.10	0.30	0.70	V/ $\mu\text{s}$
$V_{rdy}$	$V_{CC}$ ready voltage (RDY = 1)	5V operation, $V_{CC}$ rising	4.6	–	–	V
		3V operation, $V_{CC}$ rising	2.75	–	–	V
		1.8V operation, $V_{CC}$ rising	1.65	–	–	V
$V_{CCF}$	RDY = 0 ( $V_{CC}$ voltage supervisor threshold)	$V_{CC} = 5\text{V}$	–	–	4.6	V
$C_{VPC}$	External filter cap for $V_{PC}$		8.0	10.0	12.0	$\mu\text{F}$
$C_{vp}$	External filter cap for VP		2.0	4.7	6.8	$\mu\text{F}$
$C_F$	External filter capacitor ( $V_{CC}$ to GND)	$C_F$ should be ceramic with low ESR ( $< 100\text{m}\Omega$ ).	0.2	0.47	1.0	$\mu\text{F}$
$C_{VDD}$	VDD filter capacitor		0.2	–	1.0	$\mu\text{F}$

Symbol	Parameter	Condition	Min	Nom	Max	Unit
<b>Interface Requirements – Data Signals: I/O, AUX1, AUX2, and host interfaces: I/OUC, AUX1UC, AUX2UC, DP, DM. I<sub>SHORTL</sub>, I<sub>SHORTH</sub>, and V<sub>INACT</sub> requirements do not pertain to I/OUC, AUX1UC, AUX2UC</b>						
V <sub>OH</sub>	Output level, high (I/O, AUX1, AUX2)	I <sub>OH</sub> = 0	0.9 * V <sub>CC</sub>	–	V <sub>CC</sub> +0.1	V
V <sub>OH</sub>	Output level, high (I/OUC, AUX1UC, AUX2UC)	I <sub>OH</sub> = -40μA	0.75 V <sub>CC</sub>	–	V <sub>CC</sub> +0.1	V
		I <sub>OH</sub> = 0	0.9 V <sub>DD</sub>	–	V <sub>DD</sub> +0.1	V
V <sub>OL</sub>	Output level, low (I/O, AUX1, AUX2)	I <sub>OH</sub> = -40μA	0.75 V <sub>DD</sub>	–	V <sub>DD</sub> +0.1	V
		I <sub>OL</sub> =1mA	–	–	0.15 *V <sub>CC</sub>	V
V <sub>OL</sub>	Output level, low (I/OUC, AUX1UC, AUX2UC)	I <sub>OL</sub> =1mA	–	–	0.3	V
V <sub>IH</sub>	Input level, high (I/O, AUX1, AUX2)		0.6 * V <sub>CC</sub>	–	V <sub>CC</sub> +0.30	V
V <sub>IH</sub>	Input level, high (I/OUC, AUX1UC, AUX2UC)		0.6 * V <sub>DD</sub>	–	V <sub>DD</sub> +0.30	V
V <sub>IL</sub>	Input level, low (I/O, AUX1, AUX2)		-0.15	–	0.2 * V <sub>CC</sub>	V
V <sub>IL</sub>	Input level, low (I/OUC, AUX1UC, AUX2UC)		-0.15	–	0.2 * V <sub>DD</sub>	V
V <sub>INACT</sub>	Output voltage when outside of session	I <sub>OL</sub> = 0	–	–	0.1	V
		I <sub>OL</sub> = 1mA	–	–	0.3	V
I <sub>LEAK</sub>	Input leakage	V <sub>IH</sub> = V <sub>CC</sub>	–	–	10	μA
I <sub>float</sub>	Input current	Input current with SC/USB = 0	-2	–	+2	μA
I <sub>IL</sub>	Input current, low (I/O, AUX1, AUX2)	V <sub>IL</sub> = 0	–	–	0.65	mA
I <sub>IL</sub>	Input current, low (I/OUC, AUX1UC, AUX2UC)	V <sub>IL</sub> = 0	–	–	0.7	mA
I <sub>SHORTL</sub>	Short circuit output current	For output low, shorted to V <sub>CC</sub> through 33Ω	–	–	15	mA
I <sub>SHORTH</sub>	Short circuit output current	For output high, shorted to ground through 33Ω	–	–	15	mA
t <sub>R</sub> , t <sub>F</sub>	Output rise time, fall times	For I/O, AUX1, AUX2, C <sub>L</sub> = 80pF, 10% to 90%. For I/OUC, AUX1UC, AUX2UC, C <sub>L</sub> =50Pf, 10% to 90%.	–	–	100	ns
t <sub>IR</sub> , t <sub>IF</sub>	Input rise, fall times		–	–	1	μs
R <sub>PU</sub>	Internal pull-up resistor	Output stable for >200ns	8	11	14	kΩ
FD <sub>MAX</sub>	Maximum data rate		–	–	1	MHz
T <sub>FDIO</sub>	Delay, I/O to I/OUC, AUX1 to AUX1UC, AUX2 to AUX2UC, I/OUC to I/O, AUX1UC to AUX1, AUX2UC to AUX2 (respectively falling edge to falling edge and rising edge to rising edge)	Edge from master to slave, measured at 50%	60	100	200	ns
T <sub>RDIO</sub>			–	15	–	ns
C <sub>IN</sub>	Input capacitance		–	–	10	pF
I <sub>usb</sub> off	Input current USB off	0 < V <sub>dm</sub> , V <sub>dp</sub> < 3.3V, V <sub>CC</sub> =5V, SC/USB = 1	-2	–	+2	μA
R <sub>switch</sub>	Resistance D to Aux	0 < V <sub>dm</sub> , V <sub>dp</sub> < 3.3V, V <sub>CC</sub> =5V, SC/USB = 0	0.5	2	6	Ω

Symbol	Parameter	Condition	Min	Nom	Max	Unit
<b>Reset and Clock for card interface, RST, CLK</b>						
V <sub>OH</sub>	Output level, high	I <sub>OH</sub> = -200μA	0.9 * V <sub>CC</sub>	–	V <sub>CC</sub>	V
V <sub>OL</sub>	Output level, low	I <sub>OL</sub> = 200μA	0	–	0.15 * V <sub>CC</sub>	V
V <sub>INACT</sub>	Output voltage when outside of session	I <sub>OL</sub> = 0	–	–	0.1	V
I <sub>float</sub>	Input current	I <sub>OL</sub> = 1mA	–	–	0.3	V
		Input current with SC/USB = 0, open circuited	-5	–	+5	μA
I <sub>RST_LIM</sub>	Output current limit, RST		–	–	30	mA
I <sub>CLK_LIM</sub>	Output current limit, CLK		–	–	70	mA
t <sub>R</sub> , t <sub>F</sub>	Output rise time, fall time	C <sub>L</sub> = 35pF for CLK, 10% to 90%	–	–	12	ns
		C <sub>L</sub> = 200pF for RST, 10% to 90%	–	–	100	ns
δ	Duty cycle for CLK	C <sub>L</sub> = 35pF, F <sub>CLK</sub> ≤ 20MHz, CLKIN duty cycle is 48% to 52%.	45	–	55	%

## 2.4 Digital Signals Characteristics

Table 5 lists the 73S8009CN digital signals characteristics.

**Table 5: Digital Signals Characteristics**

Symbol	Parameter	Condition	Min	Nom	Max	Unit
<b>Digital I/O</b> (except for I/OUC, AUX1UC, AUX2UC; see Smart Card Interface Requirements for those specifications)						
V <sub>IL</sub>	Input Low Voltage		-0.3	–	0.8	V
V <sub>ILOFFACK</sub>	Input low voltage for OFF_ACK pin	OFF_REQ pin = VDD	-0.3	–	0.7	V
V <sub>IH</sub>	Input High Voltage		1.8	–	V <sub>DD</sub> + 0.3	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2mA		–	0.45	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -1mA	V <sub>DD</sub> - 0.45	–		V
R <sub>OUT</sub>	Pull-up resistor; OFF, RDY		14	20	26	kΩ
R <sub>ACK</sub>	Resistor between OFF_REQ and OFF_ACK		70	100	130	kΩ
I <sub>IL1</sub>	Input Leakage Current	GND < V <sub>IN</sub> < V <sub>DD</sub>	–	–	5	μA
t <sub>SL</sub>	Time from CS goes high to interface active		50	–	–	ns
t <sub>DZ</sub>	Time from CS goes low to interface inactive, Hi-Z		50	–	–	ns
t <sub>IS</sub>	Set-up time, control signals to CS rising edge		50	–	–	ns
t <sub>SI</sub>	Hold time, control signals from CS rising edge		–	–	50	ns
t <sub>ID</sub>	Set-up time, control signals to CS fall		50	–	–	ns
t <sub>DI</sub>	Hold time, control signals from CS fall		–	–	50	ns

## 2.5 DC Characteristics

Table 6 lists the DC characteristics.

**Table 6: DC Characteristics**

Symbol	Parameter	Condition	Min	Nom	Max	Unit
V <sub>DD</sub>	V <sub>DD</sub> Voltage	2.7V < V <sub>PC</sub> < 6.5V, I <sub>V<sub>DD</sub>EXT</sub> < 40mA.	3.0	3.3	3.6	V
I <sub>V<sub>DD</sub>EXT</sub>	V <sub>DD</sub> Current to External Load		–	–	40	mA
I <sub>V<sub>PC</sub></sub>	Supply Current	V <sub>PC</sub> = 2.7V, V <sub>CC</sub> off, I <sub>DD</sub> = 0	–	1.7	–	mA
		V <sub>PC</sub> = 3.3V, V <sub>CC</sub> off, I <sub>DD</sub> = 0	–	1.1	–	mA
		V <sub>PC</sub> = 5.0V, V <sub>CC</sub> off, I <sub>DD</sub> = 0	–	0.7	–	mA
		OFF mode	–	0.01	1	μA

## 2.6 Voltage / Temperature Fault Detection Circuits

Table 7 lists the voltage /temperature fault detection circuits.

**Table 7: Voltage / Temperature Fault Detection Circuits**

Symbol	Parameter	Condition	Min	Nom	Max	Unit
I <sub>DDmax</sub>	VDD over-current limit		40	–	100	mA
I <sub>CCF</sub>	Card overcurrent fault		80	–	150	mA
I <sub>CCF1P8</sub>	Card overcurrent fault	V <sub>CC</sub> = 1.8V	60	–	130	mA

## 2.7 Thermal Characteristics

Table 8 lists the thermal characteristics.

**Table 8: Thermal Characteristics**

Symbol	Parameter	Condition	Min	Nom	Max	Unit
T <sub>j</sub>	Junction temperature		–	–	125	°C
θ <sub>ja</sub>	Thermal Resistance, Junction-to-Ambient		–	70	–	°C/W
θ <sub>jc</sub>	Thermal Resistance, Junction-to-case		–	6	–	°C/W

## 3 Applications Information

This section provides general usage information for the design and implementation of the 73S8009CN. The documents listed in Related Documentation provide more detailed information.

### 3.1 Example 73S8009CN Schematics

Figure 3 shows a typical application schematic for the implementation of the 73S8009CN with a main system switch. Figure 4 shows a typical application schematic for the implementation of the 73S8009CN without a main system switch. Note that minor changes may occur to the reference material from time to time and the reader is encouraged to contact Teridian for the latest information.

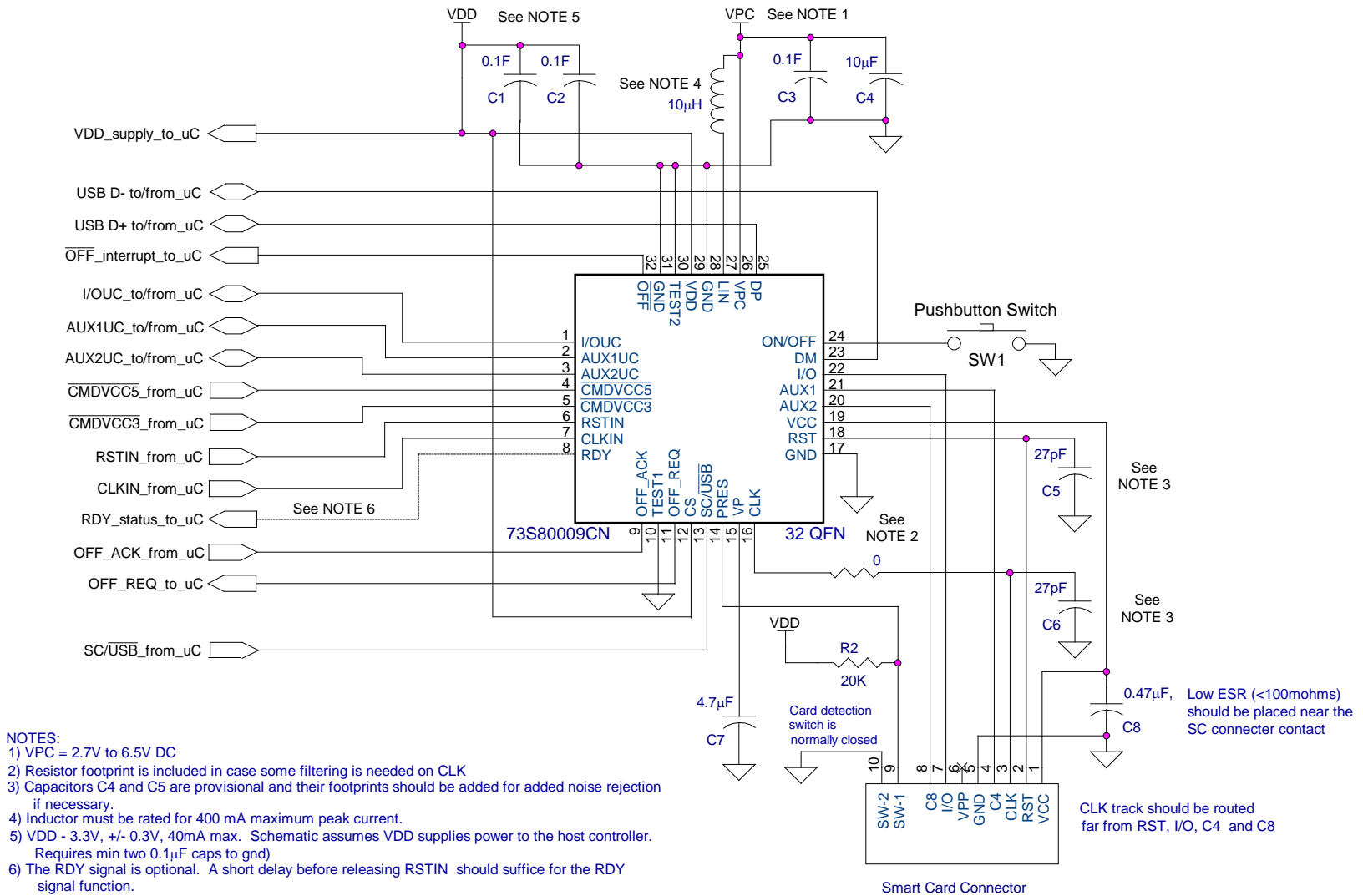


Figure 3: Typical 73S8009CN Application Schematic with a Main System Switch

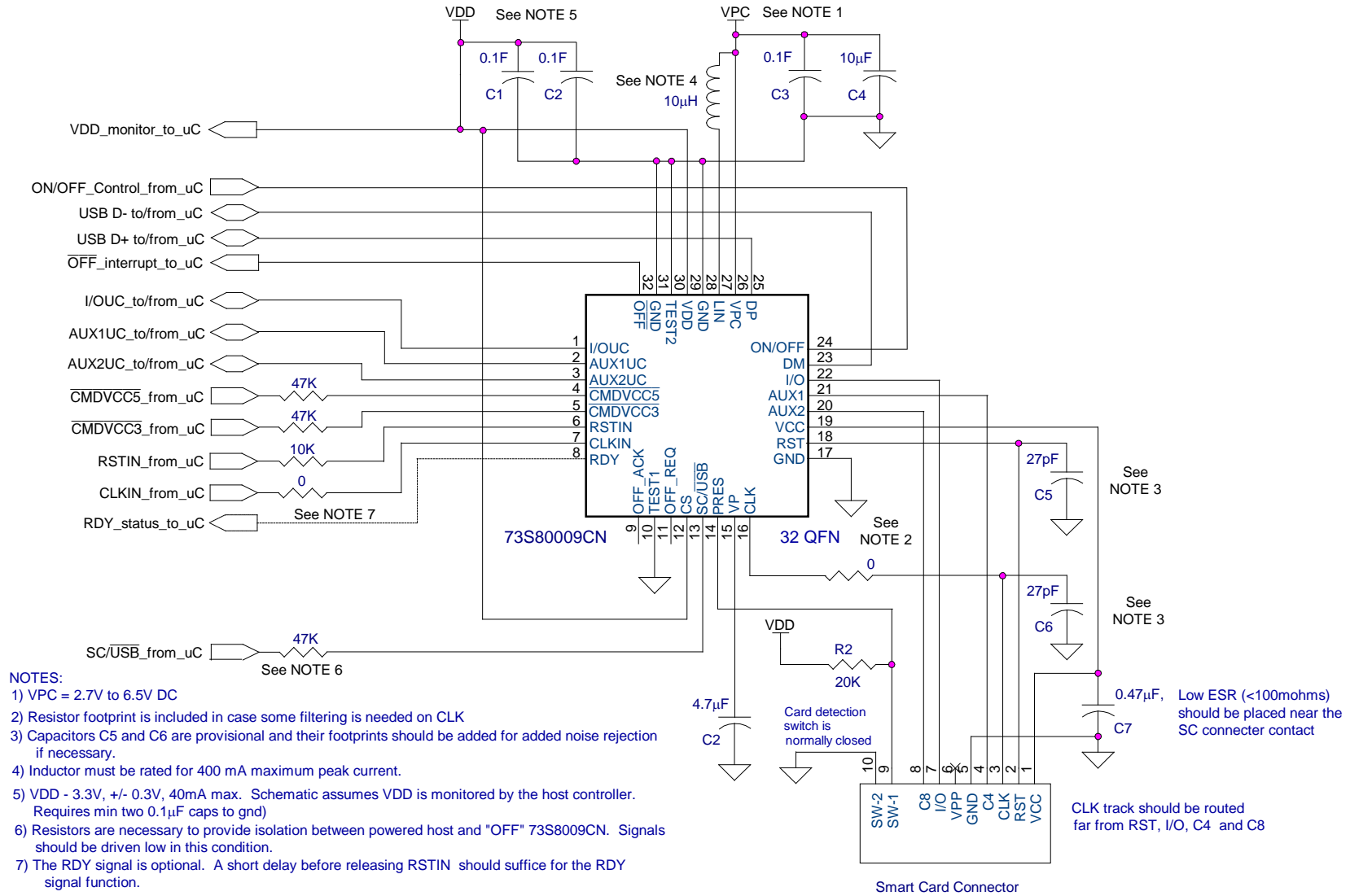


Figure 4: Typical 73S8009CN Application Schematic without a Main System Switch

### 3.2 Power Supply and Converter

The 73S8009CN power supply and converter circuitry takes power from the  $V_{PC}$  input pin. The power supplied to  $V_{PC}$  pin is converted to the voltage  $V_P$  utilizing an inductive, step-up converter. A series power inductor (nominal value =  $10\mu\text{H}$ ) is connected from pin  $V_{PC}$  to pin  $LIN$ , and a  $10\mu\text{F}$  and a  $0.1\mu\text{F}$  filter capacitor must be connected to  $V_{PC}$ . Note: When the  $V_{PC}$  input voltage exceeds the nominal  $V_P$  voltage (approximately 5.5V), the switching operation of the converter stops and the converter acts as a pass through for  $V_{PC}$  to  $V_P$ . Switching operation will automatically resume when  $V_{PC}$  falls below the nominal  $V_P$  voltage.

$V_P$  requires a  $4.7\mu\text{F}$  filter capacitor and will have a nominal value of 5.5 volts during normal operation.  $V_P$  is used by the smart card interface circuits (CLK, RST, I/O, AUX1, and AUX2) and is the source of the regulated smart card supply  $V_{CC}$ .  $V_{CC}$  can be selected for values of 5V, 3V, and 1.8V.

The power supply output  $V_{DD}$  is also produced from  $V_P$ .  $V_{DD}$  is used by the 73S8009CN circuit for logic, input / output buffering with the host. In addition,  $V_{DD}$  can be used as a 3.3V regulated power supply for some external circuitry provided that no more than 40mA is needed (simultaneously to the 65mA current drawn from  $V_{CC}$ ).

### 3.3 Interface Function - ON/OFF Modes

A power ON/OFF function is provided such that the circuit will be inoperative during the "OFF" state, consuming minimum current from  $V_{PC}$ .

Option 1: 73S8009CN supplies host/system power controlled by push button ON/OFF switch:

Refer to Figure 3 for a typical electrical schematic when using an ON/OFF system switch.

The ON/OFF pin shall be connected to an SPST switch to ground. If the circuit is OFF and the switch is closed for a de-bounce period of approximately 100ms, the circuit shall go into the "ON" state wherein all functions are operating in normal fashion. If the circuit is in the "ON" state and the ON/OFF pin is connected to ground for a period greater than the de-bounce period, OFF\_REQ will be asserted high and held regardless of the state of ON/OFF. Typically, the OFF\_REQ signal is presented to a host controller that will assert OFF\_ACK high when it has completed all shutdown activities. When OFF\_ACK is set high, the circuit will de-activate the smart card interface if required and turn off all analog functions and the  $V_{DD}$  supply for the logic and companion circuits. The OFF\_ACK pin is connected internally to OFF\_REQ with a resistor such that if OFF\_ACK is unconnected, the action of OFF\_REQ will assert OFF\_ACK high. In this configuration, the circuit shall go into the "OFF" state immediately if the interface is deactivated or immediately after deactivation if previously activated.. The default state upon application of power to  $V_{PC}$  is the "OFF". Note that at any time, the controller may assert OFF\_ACK and the 73S8009CN will go into the "OFF" state (regardless of activity on the ON/OFF main system switch).

Option 2: ON/OFF status driven from the host processor (no system switch):

Refer to Figure 4 for a typical electrical schematic when controlling the ON/OFF pin via host control.

The ON/OFF pin can be connected to a host digital control signal to turn the 73S8009CN on or off. The host should monitor the  $V_{DD}$  supply to determine when the switch debounce time has been achieved so the 73S8009CN can switch states (ON or OFF). When the 73S8009CN is OFF, the host should drive the ON/OFF pin low to initiate the turn ON process. The signal must remain low until the  $V_{DD}$  supply voltage goes to 3.3V. The 73S8009CN is now ON and the ON/OFF pin should be driven back high. To turn off the 73S8009CN, the host should drive the ON/OFF signal low until the  $V_{DD}$  supply goes to 0V. The 73S8009CN is now OFF and the ON/OFF pins should be driven back high. See Note 6.



**Important Notes:**

1. When the host is not powered by the  $V_{DD}$  supply of the 73S8009CN, special care must be taken as the host signals going to the 73S8009CN can be active when the device is powered OFF. This can create issues such as excessive current drain on the control signals and potentially prohibit proper turn ON of the 73S8009CN. Series resistors on the input signals (except the ON/OFF input) are recommended to provide isolation and prevent any potential problems. The recommended value of these resistors is 47k $\Omega$ . It is also necessary for the host to set these input signals to the low state (except for ON/OFF) when the 73S8009CN is OFF. False activation of the card is possible if the  $\overline{CMDVCC3}$  or  $\overline{CMDVCC5}$  inputs are low (with a card inserted) when the 73S8009CN is powered ON. For this reason, the proper sequencing of the 73S8009CN is required. The  $\overline{CMDVCC3}$  or  $\overline{CMDVCC5}$  inputs must be set high immediately before the ON/OFF input is taken low to turn on the 73S8009CN. The time between setting the  $\overline{CMDVCC3}$  or  $\overline{CMDVCC5}$  inputs high and the setting of the ON/OFF input set low should be kept to a minimum as the  $\overline{CMDVCC3}$  or  $\overline{CMDVCC5}$  inputs, when set high with the 73S8009CN OFF, will draw significant current under these conditions. The 47k $\Omega$  series resistors will mitigate this current draw. However, some additional current will be drawn through the resistors to the  $\overline{CMDVCC3}$  or  $\overline{CMDVCC5}$  inputs during this time so it should be kept to a minimum.
2. For applications where ON/OFF is controlled by the host, the OFF\_REQ and OFF\_ACK signals do not need to be connected to the host. When the OFF\_ACK pin is left unconnected, the 73S8009CN will turn off properly by the action of the internal resistor connection to OFF\_REQ.
3. If the host is capable of selectively monitoring the I/O line, it can be used in place of the  $V_{DD}$  supply monitor as it is tied to the  $V_{DD}$  supply through a pull up resistor when the smart card interface is not activated.
4. When the 73S8009CN is powered OFF, the host will not be able to detect a card event (card insertion/removal). If this function is necessary, then the host must monitor the card connector switch separately.
5. For systems that do not use  $V_{DD}$  to power the host controller, the host interface signals must operate at 3.3V as the 73S8009CN digital logic operates off the  $V_{DD}$  (3.3V) supply regardless of the value of the  $V_{PC}$  supply.
6. The ON/OFF pin is internally pulled up to  $V_{PC}$  through a 24k $\Omega$  resistor. Special care must be taken if the host signal controlling the ON/OFF signal is running at a voltage different from  $V_{PC}$ . If this is the case, then either the host control signal must be a maximum  $V_{PC}$  supply tolerant open drain output or an external circuit should provide some isolation between the host control signal and the ON/OFF pin.
7. For those systems that require low power operation or are battery operated, the host controller circuit firmware should place the 73S8009CN in the OFF state if no card activity is required.

### 3.4 System Controller Interface

Five separate digital inputs and two outputs allow direct control of the card interface from the host:

- Pin CS: Chip select control.
- Pin  $\overline{\text{CMDVCC3}}$  and/or  $\overline{\text{CMDVCC5}}$ : When low, starts an activation sequence.
- Pin RSTIN: controls the card RST signal.
- Pin  $\overline{\text{SC/USB}}$ : Routes AUXx signals to AUXxUC or USB Dx pins and provides proper tri-stating functionality.
- Pin RDY: Indicates when smart card power supply is stable and ready.
- Pin OFF: Indicator of card presence and any card fault conditions.

Interrupt output to the host: When the card is not activated, the  $\overline{\text{OFF}}$  pin informs the host about the card presence only (Low = No card in the reader, high = card inserted). When  $\overline{\text{CMDVCC}}$  ( $\overline{3/5}$  signals) is/are set low (card activation sequence requested from the host), low level on  $\overline{\text{OFF}}$  means a fault has been detected (e.g. card removal during card session, or voltage fault, or thermal / over-current fault) that automatically initiates a deactivation sequence. The smart card pass through signals are enabled when the RDY conditions are met.

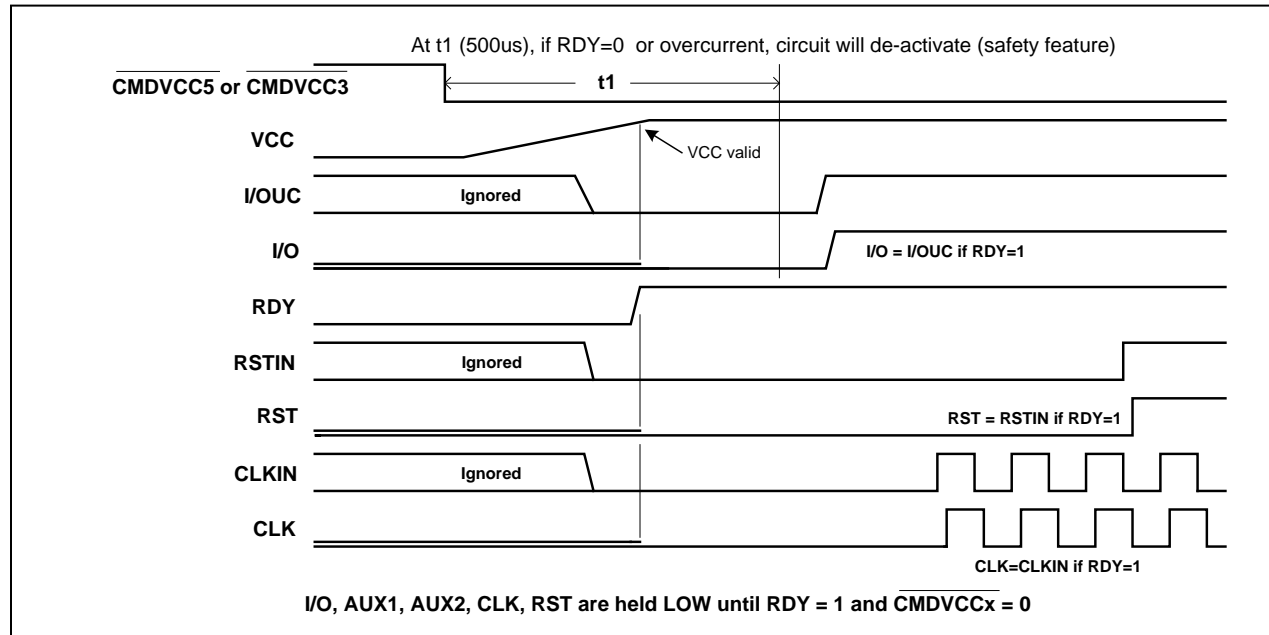
### 3.5 Card Power Supply and Voltage Supervision

The 73S8009CN smart card interface IC incorporates an LDO voltage regulator for the card power supply,  $V_{\text{CC}}$  ( $V_{\text{P}}$  to  $V_{\text{CC}}$  conversion uses an internal LDO). The voltage output is controlled by the digital input sequence of  $\overline{\text{CMDVCC3}}$  and  $\overline{\text{CMDVCC5}}$ . This regulator is able to provide either 1.8V, 3V or 5V card voltage sourced from the  $V_{\text{P}}$  power supply. Internal digital circuitry is also powered by the  $V_{\text{P}}$  power supply (except for the ON/OFF circuitry which is powered from  $V_{\text{PC}}$ ). A voltage supervisor checks the value of the voltage  $V_{\text{CC}}$ . A card deactivation sequence is forced upon fault detected by voltage supervisor, overcurrent condition, or card removal event. The voltage regulator can provide a card current of 65mA in compliance with EMV 4.1 for 3-V and 5-V cards. The signals  $\overline{\text{CMDVCC3}}$  and  $\overline{\text{CMDVCC5}}$  control the turn-on, output voltage value, and turn-off of  $V_{\text{CC}}$ . When either signal is asserted low,  $V_{\text{CC}}$  will ramp to the selected value or if both signals are asserted low (within 400ns of each other),  $V_{\text{CC}}$  will ramp to 1.8V. These signals are edge triggered. If  $\overline{\text{CMDVCC5}}$  is asserted low (to command  $V_{\text{CC}}$  to be 5V) and at a much later time (greater than 2 $\mu\text{s}$ , typically),  $\overline{\text{CMDVCC3}}$  is asserted low, it will be ignored (and vice versa.)

At the assertion (low) of either or both  $\overline{\text{CMDVCC}}$  ( $\overline{3/5}$  signals),  $V_{\text{CC}}$  will rise to the requested value. When  $V_{\text{CC}}$  rises to an acceptable value, and stays above that value for approximately 20 $\mu\text{s}$ , RDY will be set high. Approximately 510 $\mu\text{s}$  after the fall of  $\overline{\text{CMDVCC}}$  ( $\overline{3/5}$ ), the circuit will check to see if  $V_{\text{CC}}$  is at or above the required minimum value (indicated by RDY=1) and if not, will begin an emergency deactivation sequence. During the 510 $\mu\text{s}$  time, card removal, or de-assertion of  $\overline{\text{CMDVCC}}$  ( $\overline{3/5}$ ) shall also initiate an emergency deactivation sequence. The circuit provides over-current protection and limits  $I_{\text{CC}}$  to 150mA, maximum for self-protection. When an over-current condition is sensed, the circuit will invoke a deactivation sequence.

### 3.6 Activation and De-activation Sequence

The host controller is fully responsible for the activation sequencing of the smart card signals CLK, RST, I/O, AUX1 and AUX2. All these signals are held low by the 73S8009CN when the card is in the de-activated state. Upon card activation (the fall of  $\overline{\text{CMDVCC}}(\overline{3/5})$ ), all the signals are held low by the 73S8009CN until RDY goes high. The host should set the signals RSTIN, I/OUC, CLKIN, AUX1UC and AUX2UC low prior to activating the card and allow RDY to go high before transitioning any of these signals. In order to initiate activation, the card must be present and  $\overline{\text{OFF}}$  must be high.



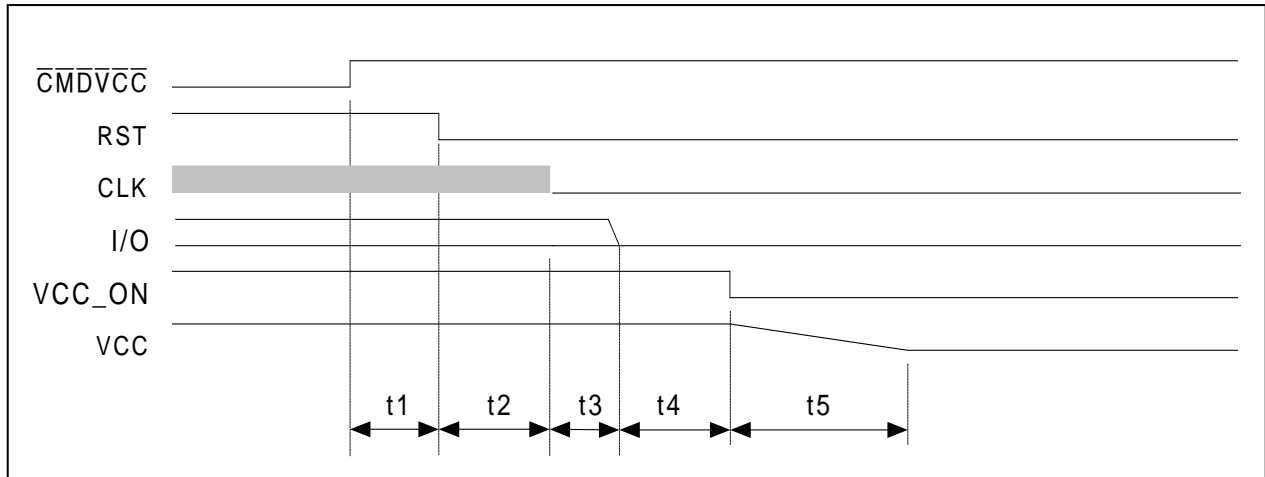
**Figure 5: Activation Sequence**

Deactivation is initiated either by the system controller by setting both  $\overline{\text{CMDVCC}}(\overline{3/5})$  high, or automatically in the event of hardware faults or assertion of the OFF\_ACK signal. Hardware faults are over-current, under-voltage, and card extraction during the session. The host can manage the I/O signals, CLKIN, RSTIN, and  $\overline{\text{CMDVCC}}(\overline{3/5})$  to create other de-activation sequences for non-emergency situations.

The following steps show the deactivation sequence and the timing of the card control signals when the system controller sets the  $\overline{\text{CMDVCC}}(x)B$  high:

1. RST goes low at the end of time t1.
2. De-assert CLK at the end of time t2.
3. I/O goes low at the end of time t3. Exit reception mode.
4. De-assert internal VCC\_ON at the end of time t4. After a delay, VCC is de-asserted.

Note: Since the 73S8009CN does not control the waveshape of CLK (it is determined by the input from the host CLKIN), there is no guarantee that the duty cycle of the last CLK high pulse will conform to duty cycle requirements during an emergency deactivation.



**Figure 6: Deactivation Sequence**

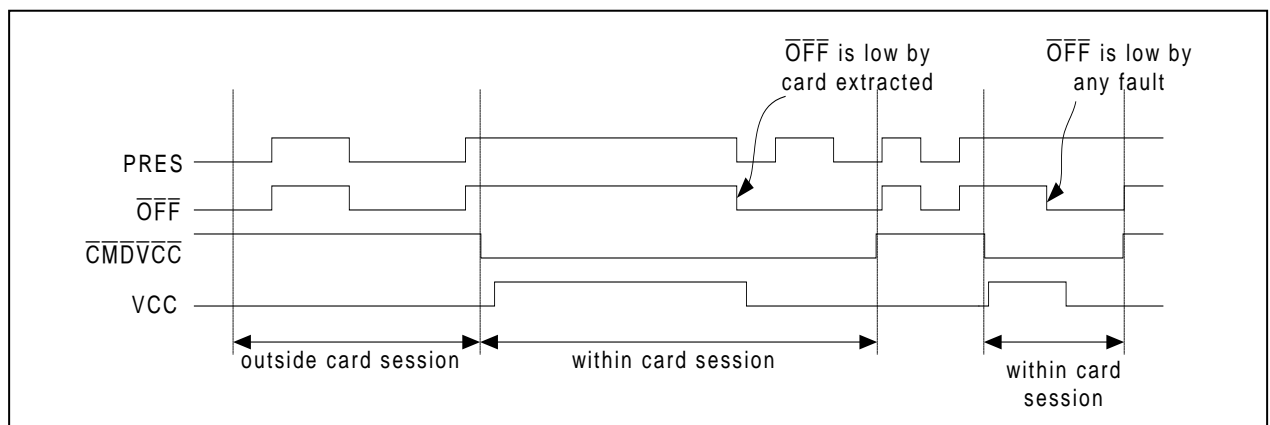
### 3.7 $\overline{\text{OFF}}$ and Fault Detection

There are two different cases that the system controller can monitor the  $\overline{\text{OFF}}$  signal: to query regarding the card presence outside card sessions, or for fault detection during card sessions.

Outside a card session: In this condition,  $\overline{\text{CMDVCC3}}$  ( $\overline{3/5}$ ) are always high,  $\overline{\text{OFF}}$  is low if the card is not present, and high if the card is present. Because it is outside a card session, no fault detection can occur and it will not act upon the  $\overline{\text{OFF}}$  signal. No deactivation is required during this time.

During a card session:  $\overline{\text{CMDVCC3}}$  and/or  $\overline{\text{CMDVCC5}}$  is always low, and  $\overline{\text{OFF}}$  falls low if the card is extracted or if any fault detection is detected. At the same time that  $\overline{\text{OFF}}$  is set low, the sequencer starts the deactivation process and the host should stop all transitions on the signal lines.

Figure 4 shows the timing diagram for the signals  $\overline{\text{CMDVCC3}}$  ( $\overline{3/5}$ ),  $\overline{\text{PRES}}$ , and  $\overline{\text{OFF}}$  during a card session and outside the card session.



**Figure 7:  $\overline{\text{OFF}}$  Activity**

### 3.8 Chip Selection

The CS pin allows multiple circuits to operate in parallel, driven from the same host control bus. When CS is high, the pins RSTIN,  $\overline{\text{CMDVCC5}}$ ,  $\overline{\text{CMDVCC3}}$  and CLKIN control the chip as described. The pins I/OUC, AUX1UC, and AUX2UC have 11k $\Omega$  pull-up resistors and operate to transfer data to the smart card via I/O, AUX1, and AUX2 when the smart card is activated. The signals  $\overline{\text{OFF}}$  and RDY have 20k $\Omega$  pull-up resistors.

When CS goes low, the states of the pins RSTIN,  $\overline{\text{CMDVCC5}}$ ,  $\overline{\text{CMDVCC3}}$ , and CLKIN are latched and held internally. The pull-up for pins I/OUC, AUX1UC, and AUX2UC become a very weak pull-up of approximately 3 microamperes. No transfer of data is possible between I/OUC, AUX1UC, AUX2UC and the smart-card signals I/O, AUX1, and AUX2. The signals  $\overline{\text{OFF}}$  and RDY are set to high impedance and the internal pull-up resistors of 20k $\Omega$  are disconnected. With regard to de-activation, CS does not affect the operation of the fault sensing circuits and card sense input. CS does not affect the action of SC/ $\overline{\text{USB}}$ .

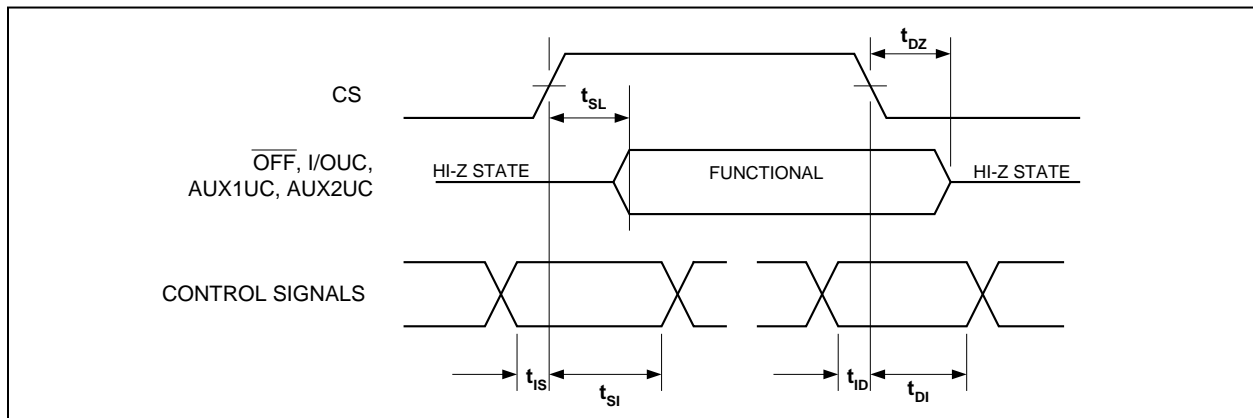


Figure 8: CS Timing Definitions

### 3.9 I/O Circuitry and Timing

The states of the I/O, AUX1, and AUX2 pins are low after power on reset and they are in high when the activation sequencer turns on the I/O reception state. See the Activation and De-activation Sequence section for more details on when the I/O reception is enabled. The states of I/OUC, AUX1UC, and AUX2UC are high after power on reset.

Within a card session and when the I/O reception state is turned on, the first I/O line on which a falling edge is detected becomes the input I/O line and the other becomes the output I/O line. When the input I/O line rising edge is detected, then both I/O lines return to their neutral state. Figure 6 shows the state diagram of how the I/O and I/OUC lines are managed to become input or output.

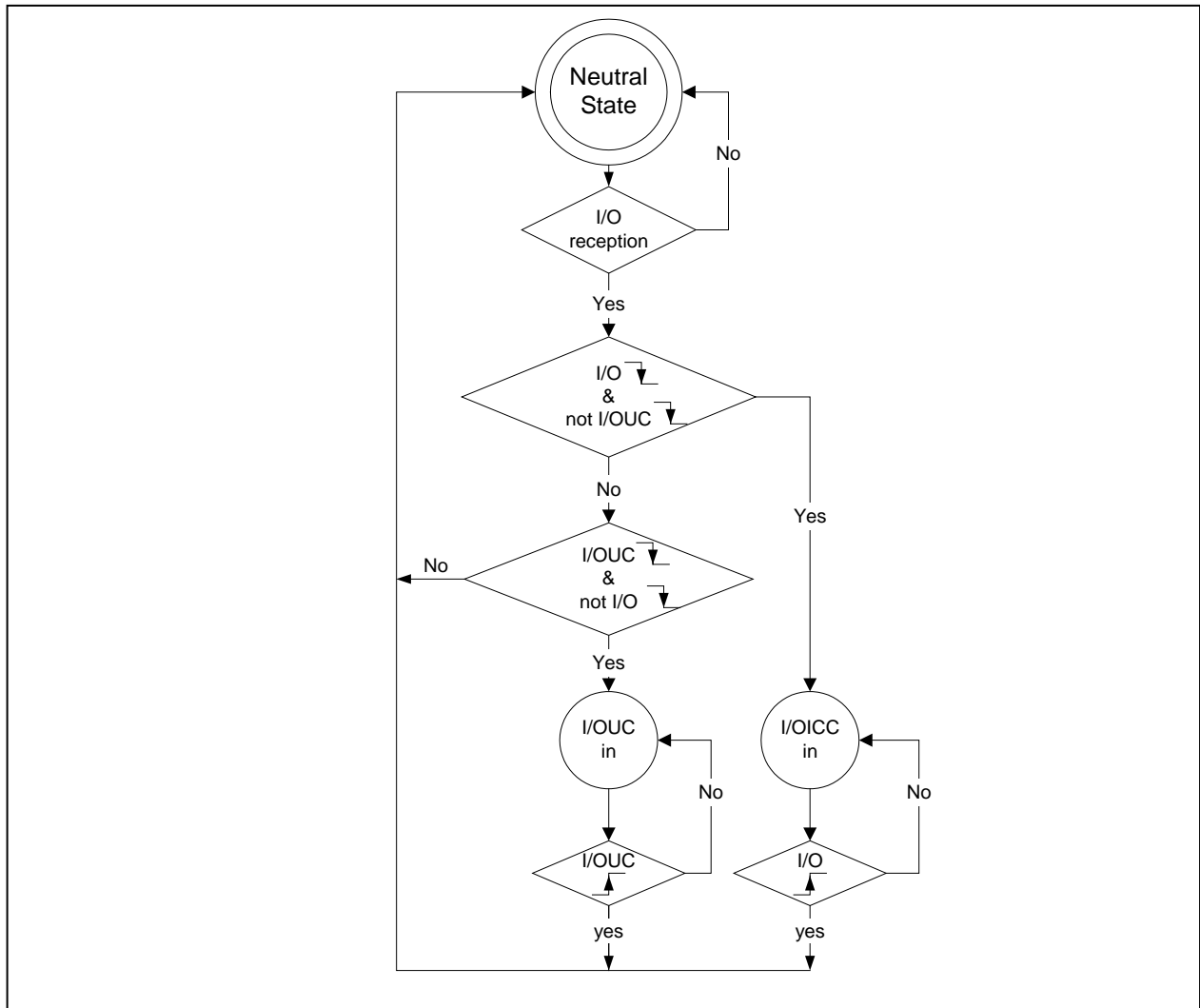
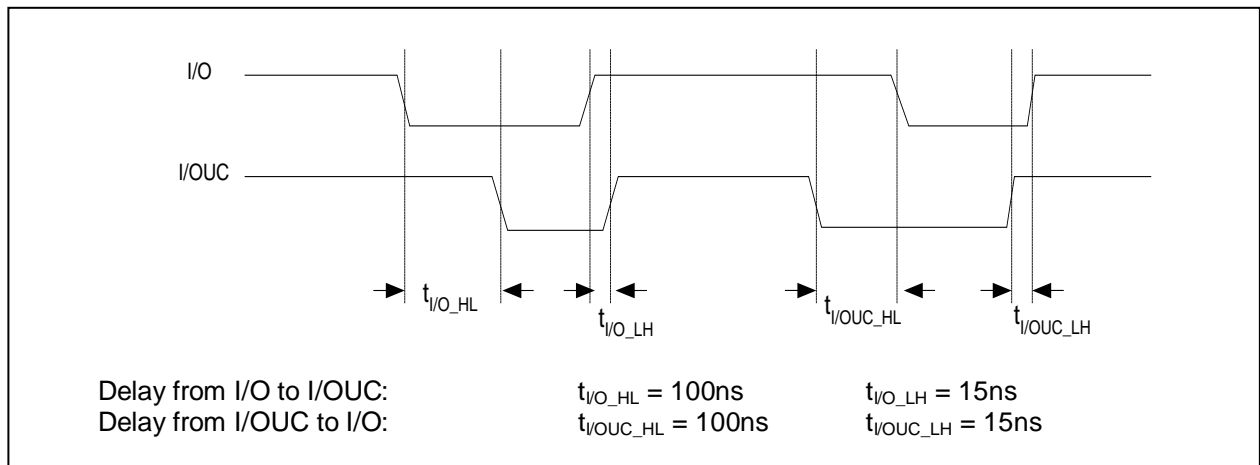


Figure 9: I/O and I/OUC State Diagram

The delay between the I/O signals is shown in Figure 10.



**Figure 10: I/O – I/OUC Delays - Timing Diagram**

## 4 Equivalent Circuits

This section provides illustrations of circuits equivalent to those described in the Pinout section.

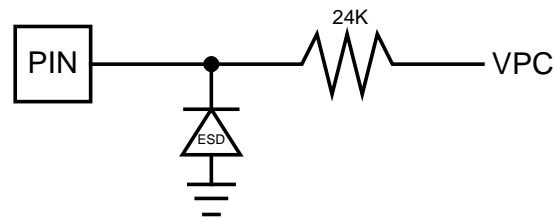


Figure 11: On\_Off Pin

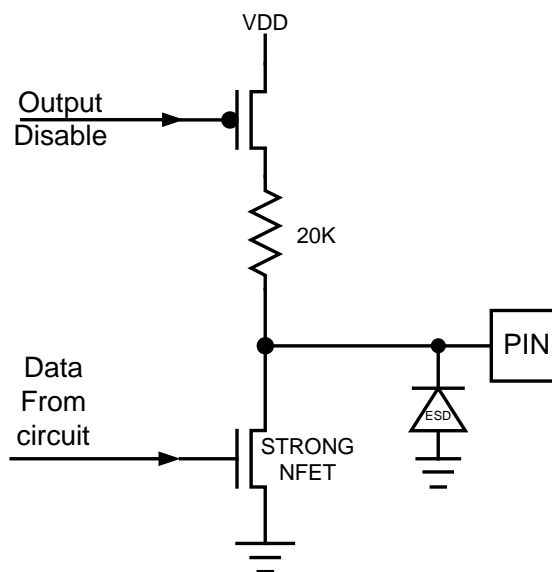


Figure 12: Open Drain type –  $\overline{\text{OFF}}$  and RDY

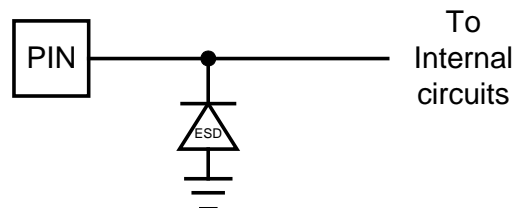


Figure 13: Power Input/Output Circuit, VDD, LIN, VPC, VCC, VP



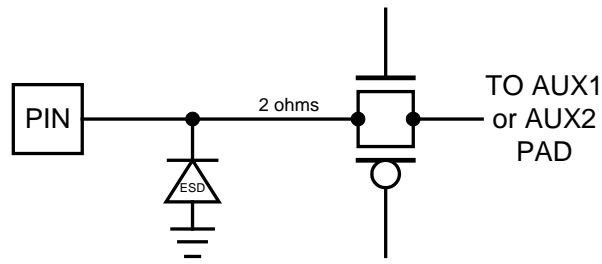


Figure 14: USB – DM, DP Pins

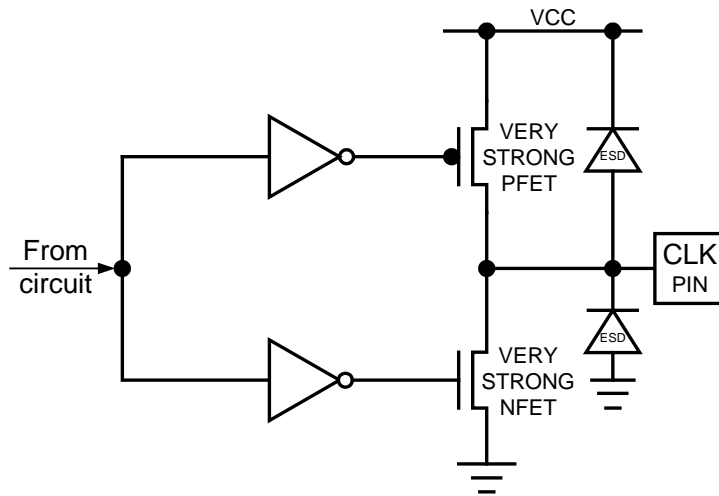


Figure 15: Smart Card CLK Driver Circuit

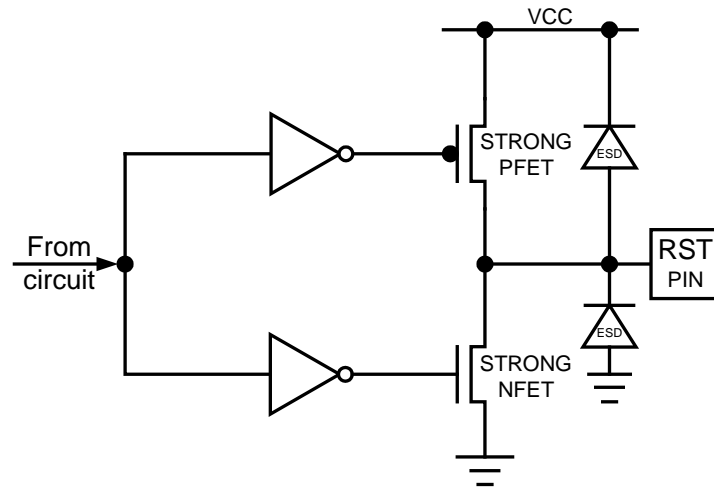


Figure 16: Smart Card RST Driver Circuit

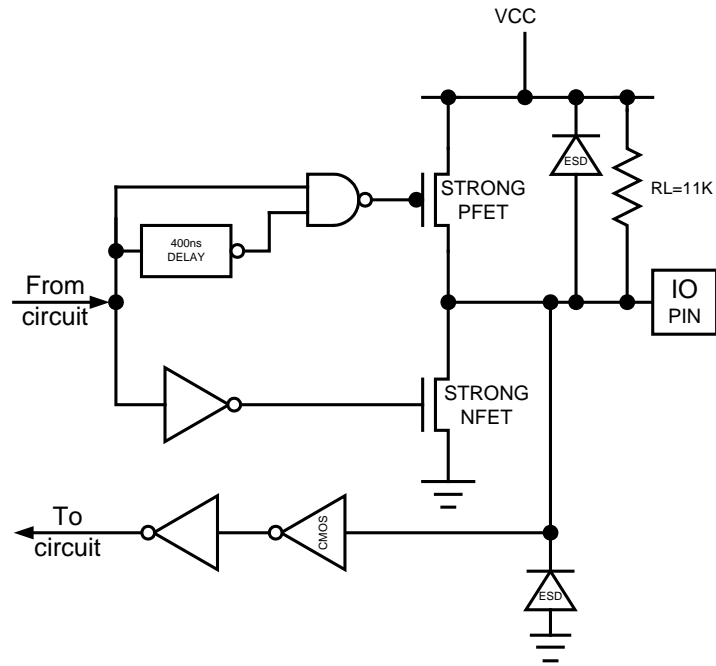


Figure 17: Smart Card IO, AUX1, and AUX2 Interface Circuit

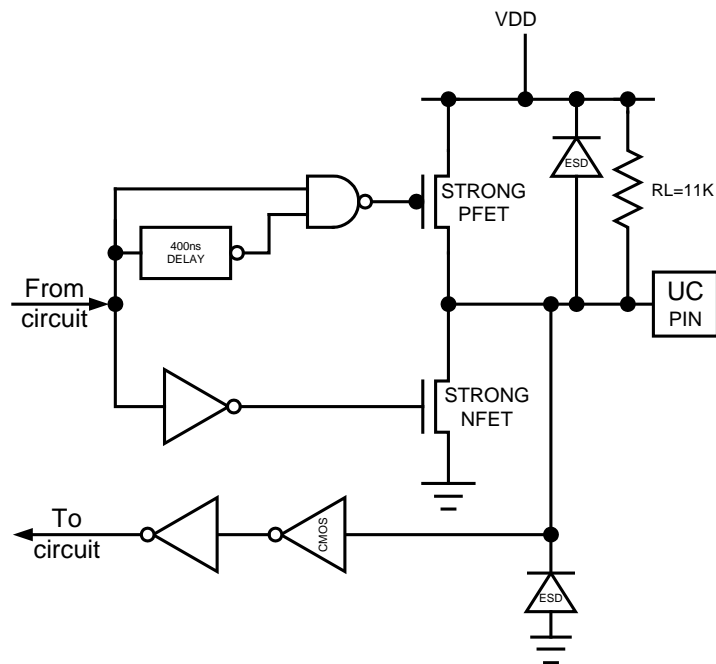
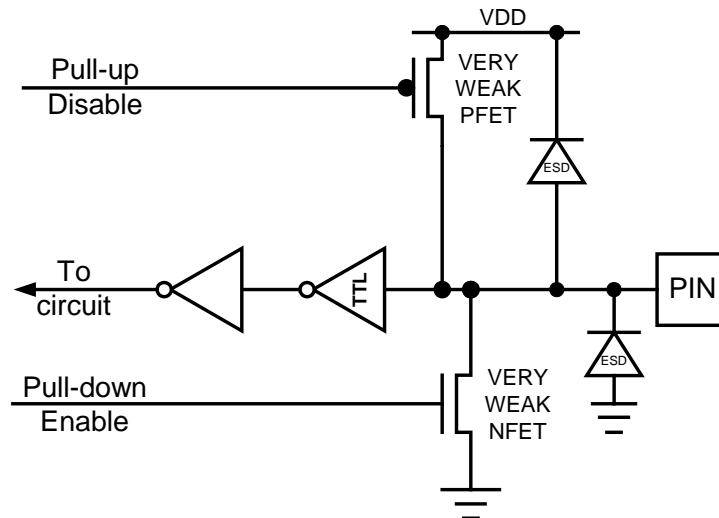
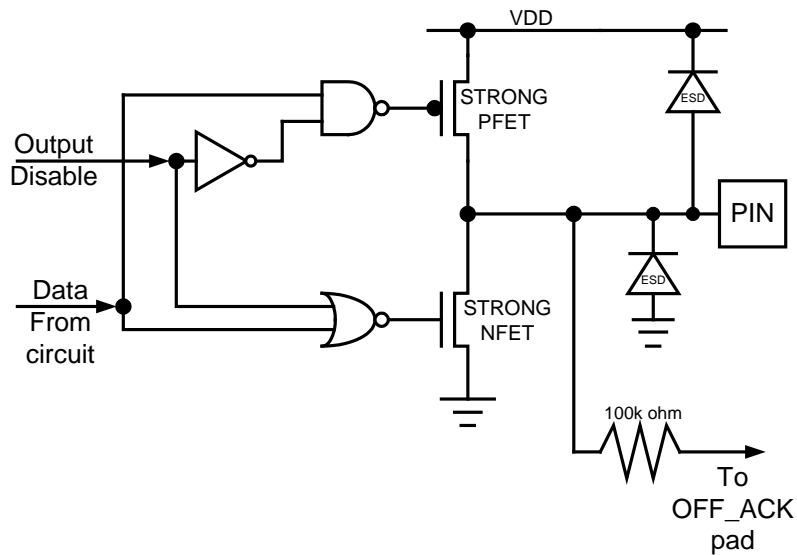


Figure 18: Smart Card IOUC, AUX1UC and AUX2UC Interface Circuit



Note: Pins  $\overline{\text{CMDVCC5}}$ ,  $\overline{\text{CMDVCC3}}$ ,  $\overline{\text{CS}}$ ,  $\overline{\text{SC/USB}}$  have the pull-up enabled.  
 Pins  $\overline{\text{RSTIN}}$ ,  $\overline{\text{CLKIN}}$ ,  $\overline{\text{PRES}}$ ,  $\overline{\text{EXT\_RST}}$  have the pull-down enabled.  
 Pin  $\overline{\text{OFF\_ACK}}$  has a 100k $\Omega$  resistor connected to pin  $\overline{\text{OFF\_REQ}}$  internally.

**Figure 19: General Input Circuit**



Notes: Strong PFET or NFET is approximately 100 $\Omega$   
 Very strong PFET or NFET is approximately 50 $\Omega$   
 Medium strength PFET is approximately 1k $\Omega$   
 Very weak PFET or NFET is approximately 1M $\Omega$   
 The diodes represent ESD protection devices that will conduct current if forward biased.

**Figure 20: OFF\_REQ Interface Circuit**

### 5 Mechanical Drawing

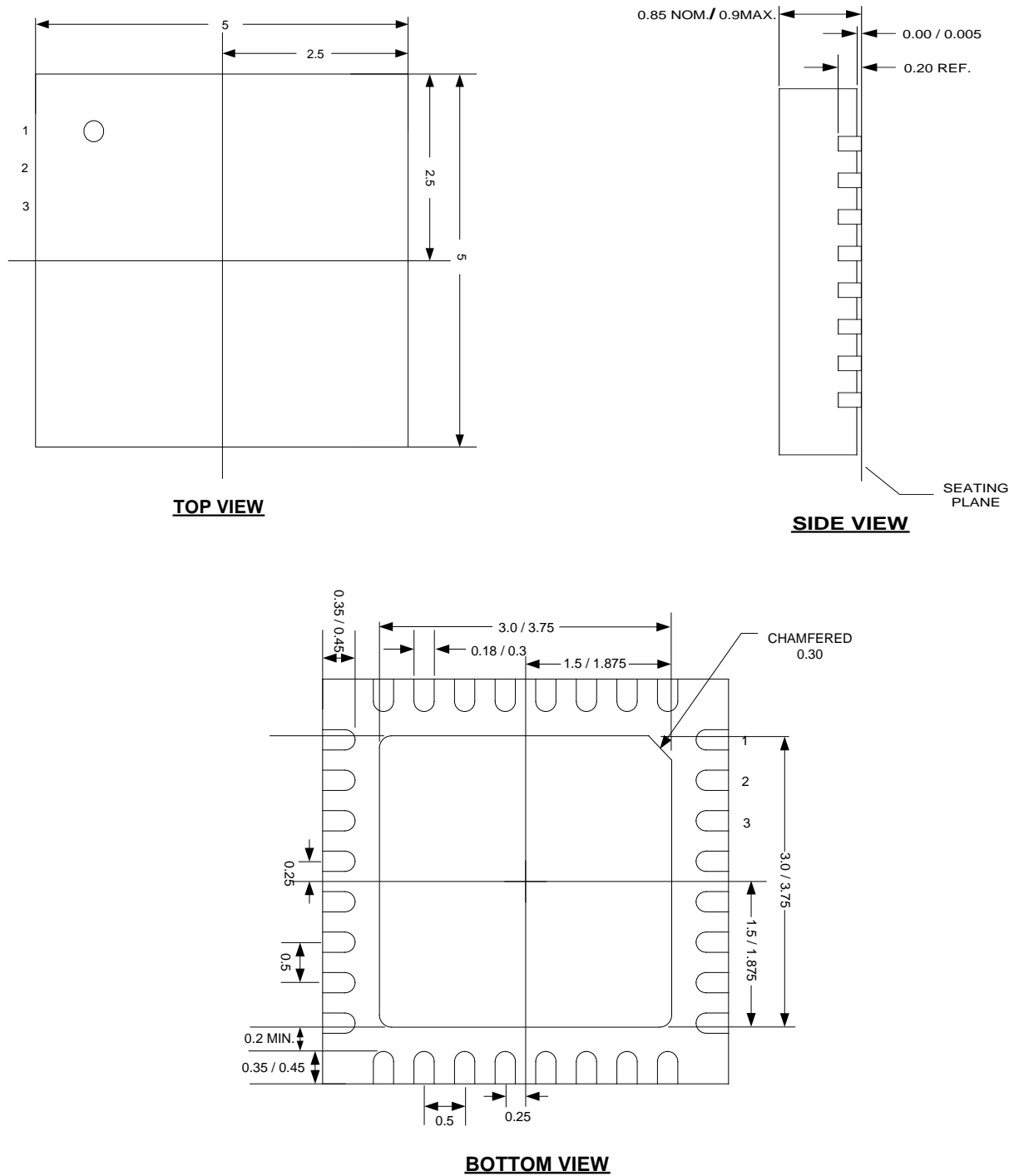


Figure 21: 32-Pin QFN Package Dimensions

## 6 Ordering Information

Table 9 lists the order numbers and packaging marks used to identify 73S8009CN products.

**Table 9: Order Numbers and Packaging Marks**

Part Description	Order Number	Packaging Mark
73S8009CN-32QFN 32-pin Lead-Free QFN	73S8009CN-32IM/F	S8009CN
73S8009CN-32QFN 32-pin Lead-Free QFN Tape / Reel	73S8009CN-32IMR/F	S8009CN

## 7 Related Documentation

The following 73S8009CN document is available from Teridian Semiconductor Corporation:

*73S8009CN 32QFN Demo Board User's Guide*

## 8 Contact Information

For more information about Teridian Semiconductor products or to check the availability of the 73S8009CN, contact us at:

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## Revision History

Revision	Date	Description
1.0	10/23/2007	First publication.
1.1	11/6/2007	Added the Related Documentation section and the Contact Information section. Miscellaneous editorial changes. Change the name of the " $\overline{SC\_USB}$ " pin to " $\overline{SC/USB}$ ".
1.2	1/21/2008	Changed the dimension of the bottom view 32-pin QFN package.
1.3	1/31/2008	Added Section 2.5, DC Characteristics.
1.4	8/28/2009	Corrected the document number from "DS_8009CN_001" to "DS_8009CN_026".

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