

## Features

- Temperature range:
  - Commercial: 0 °C to 70 °C
  - Automotive-A: -40 °C to 85 °C
- High speed
  - $t_{AA} = 15$  ns
- Low active power
- Low CMOS standby power
  - 2.75 mW (max.)
- 2.0 V data retention (400  $\mu$ W at 2.0 V retention)
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  features
- Available in Pb-free and non Pb-free 44-pin TSOP II and molded 44-pin (400-Mil) SOJ packages

## Functional Description

The CY7C1041BN is a high-performance CMOS static RAM organized as 262,144 words by 16 bits.

Writing to the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Write Enable (WE) inputs LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>), is written into the location specified on the address pins (A<sub>0</sub> through A<sub>17</sub>). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O<sub>8</sub> through I/O<sub>15</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>17</sub>).

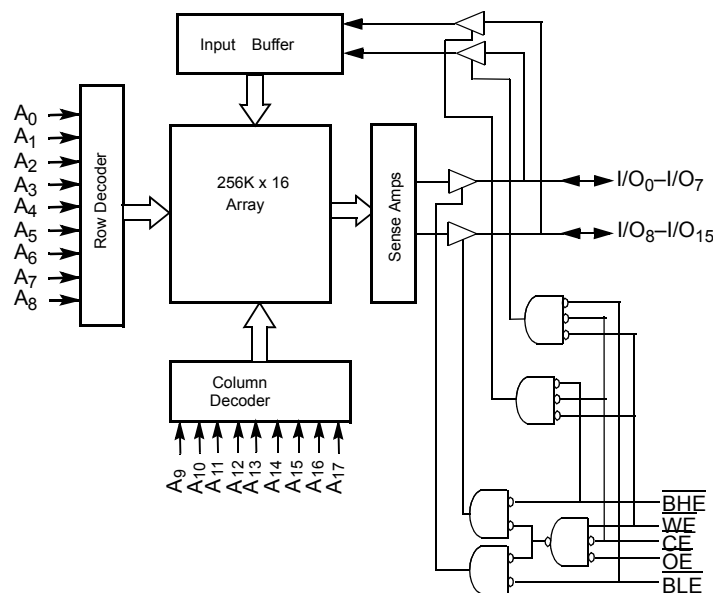
Reading from the device is accomplished by taking Chip Enable (CE) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins will appear on I/O<sub>0</sub> to I/O<sub>7</sub>. If Byte High Enable (BHE) is LOW, then data from memory will appear on I/O<sub>8</sub> to I/O<sub>15</sub>. See the truth table at the back of this data sheet for a complete description of read and write modes.

The input/output pins (I/O<sub>0</sub> through I/O<sub>15</sub>) are placed in a high-impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), the BHE and BLE are disabled (BHE, BLE HIGH), or during a write operation ( $\overline{CE}$  LOW, and WE LOW).

The CY7C1041BN is available in a standard 44-pin 400-mil-wide body width SOJ and 44-pin TSOP II package with center power and ground (revolutionary) pinout.

For a complete list of related documentation, click [here](#).

## Logic Block Diagram



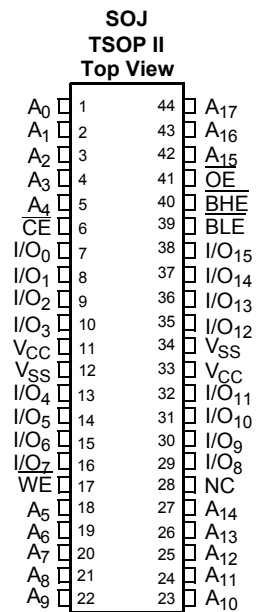
## Contents

<b>Selection Guide</b> .....	<b>3</b>	<b>Ordering Information</b> .....	<b>11</b>
<b>Pin Configurations</b> .....	<b>3</b>	Ordering Code Definitions .....	11
<b>Maximum Ratings</b> .....	<b>4</b>	<b>Package Diagram</b> .....	<b>12</b>
<b>Operating Range</b> .....	<b>4</b>	<b>Acronyms</b> .....	<b>13</b>
<b>Electrical Characteristics</b> .....	<b>4</b>	<b>Document Conventions</b> .....	<b>13</b>
<b>Capacitance</b> .....	<b>5</b>	Units of Measure .....	13
<b>AC Test Loads and Waveforms</b> .....	<b>5</b>	<b>Document History Page</b> .....	<b>14</b>
<b>Data Retention Characteristics</b> .....	<b>5</b>	<b>Sales, Solutions, and Legal Information</b> .....	<b>15</b>
<b>Data Retention Waveform</b> .....	<b>5</b>	Worldwide Sales and Design Support .....	15
<b>Switching Characteristics</b> .....	<b>6</b>	Products .....	15
<b>Switching Waveforms</b> .....	<b>7</b>	PSoC@Solutions .....	15
<b>Truth Table</b> .....	<b>10</b>	Cypress Developer Community .....	15
		Technical Support .....	15

### Selection Guide

Description		-15	-20	Unit
Maximum access time		15	20	ns
Maximum operating current	Commercial	190	170	mA
	Automotive-A	–	190	–
Maximum CMOS standby current	Commercial	0.5	0.5	mA
	Automotive-A	–	6	

### Pin Configurations



**Maximum Ratings**

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

- Storage temperature ..... -65 °C to +150 °C
- Ambient temperature with power applied ..... -55 °C to +125 °C
- Supply voltage on V<sub>CC</sub> to relative GND<sup>[1]</sup> ..... -0.5 V to +7.0 V
- DC voltage applied to outputs in High Z State <sup>[1]</sup> ..... -0.5 V to V<sub>CC</sub> + 0.5 V

- DC input voltage <sup>[1]</sup> ..... -0.5 V to V<sub>CC</sub> + 0.5 V
- Current into outputs (LOW) ..... 20 mA

**Operating Range**

Range	Ambient Temperature <sup>[2]</sup>	V <sub>CC</sub>
Commercial	0 °C to +70 °C	5 V ± 0.5
Automotive-A	-40 °C to +85 °C	

**Electrical Characteristics**

Over the Operating Range

Parameter	Description	Test Conditions	-15		-20		Unit	
			Min	Max	Min	Max		
V <sub>OH</sub>	Output HIGH voltage	Min V <sub>CC</sub> , I <sub>OH</sub> = -4.0 mA	2.4	-	2.4	-	V	
V <sub>OL</sub>	Output LOW voltage	Min V <sub>CC</sub> , I <sub>OL</sub> = 8.0 mA	-	0.4	-	0.4	V	
V <sub>IH</sub> <sup>[1]</sup>	Input HIGH voltage	-	2.2	V <sub>CC</sub> + 0.5	2.2	V <sub>CC</sub> + 0.5	V	
V <sub>IL</sub> <sup>[1]</sup>	Input LOW voltage	-	-0.5	0.8	-0.5	0.8	V	
I <sub>IX</sub>	Input load current	GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	-1	+1	-1	+1	µA	
I <sub>OZ</sub>	Output leakage current	GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , Output Disabled	-1	+1	-1	+1	µA	
I <sub>CC</sub>	V <sub>CC</sub> operating supply current	Max V <sub>CC</sub> , f = f <sub>MAX</sub> = 1/t <sub>RC</sub>	Commercial	-	190	-	170	mA
			Automotive-A	-	-	-	190	mA
I <sub>SB1</sub>	Automatic CE power-down current – TTL inputs	Max V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$ , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>	-	40	-	40	mA	
I <sub>SB2</sub>	Automatic CE power-down current – CMOS inputs	Max V <sub>CC</sub> , $\overline{CE} \geq V_{CC} - 0.3$ V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3 V, or V <sub>IN</sub> ≤ 0.3 V, f = 0	Commercial	-	0.5	-	0.5	mA
			Automotive-A	-	-	-	6	mA

**Notes**

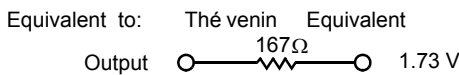
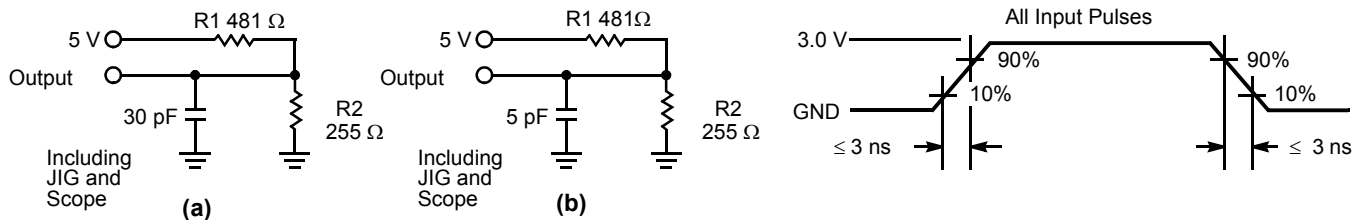
1. V<sub>IL</sub> (min.) = -2.0 V for pulse durations of less than 20 ns.
2. T<sub>A</sub> is the case temperature.

### Capacitance

Parameter <sup>[3]</sup>	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input capacitance	T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = 5.0 V	8	pF
C <sub>OUT</sub>	I/O capacitance		8	pF

### AC Test Loads and Waveforms

Figure 1. AC Test Loads and Waveforms



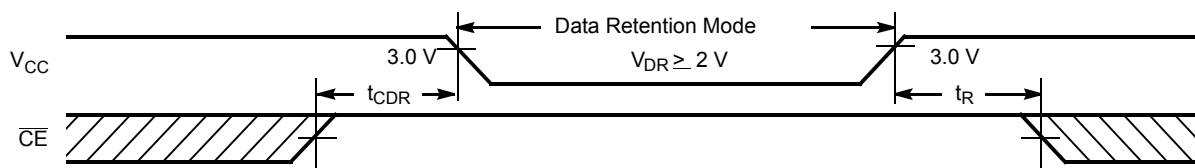
### Data Retention Characteristics

Over the Operating Range (Commercial only)

Parameter	Description	Conditions <sup>[4]</sup>	Min	Max	Unit
V <sub>DR</sub>	V <sub>CC</sub> for data retention	–	2.0	–	V
I <sub>CCDR</sub>	Data retention current	V <sub>CC</sub> = V <sub>DR</sub> = 2.0 V, CE ≥ V <sub>CC</sub> – 0.3 V, V <sub>IN</sub> ≥ V <sub>CC</sub> – 0.3 V or V <sub>IN</sub> ≤ 0.3 V	–	200	μA
t <sub>CDR</sub> <sup>[5]</sup>	Chip deselect to data retention time		0	–	ns
t <sub>R</sub> <sup>[6]</sup>	Operation recovery time		t <sub>RC</sub>	–	ns

### Data Retention Waveform

Figure 2. Data Retention Waveform



**Notes**

3. Tested initially and after any design or process changes that may affect these parameters.
4. No input may exceed V<sub>CC</sub> + 0.5 V.
5. Tested initially and after any design or process changes that may affect these parameters.
6. t<sub>r</sub> ≤ 3 ns for the -15 speed. t<sub>r</sub> ≤ 5 ns for the -20 and slower speeds.

## Switching Characteristics

Over the Operating Range

Parameter <sup>[7]</sup>	Description	-15		-20		Unit
		Min	Max	Min	Max	
<b>Read Cycle</b>						
$t_{power}$	$V_{CC}$ (typical) to the first access <sup>[8]</sup>	1	–	1	–	μs
$t_{RC}$	Read cycle time	15	–	20	–	ns
$t_{AA}$	Address to data valid	–	15	–	20	ns
$t_{OHA}$	Data hold from address change	3	–	3	–	ns
$t_{ACE}$	$\overline{CE}$ LOW to data valid	–	15	–	20	ns
$t_{DOE}$	$\overline{OE}$ LOW to data valid	–	7	–	8	ns
$t_{LZOE}$	$\overline{OE}$ LOW to low Z	0	–	0	–	ns
$t_{HZOE}$	$\overline{OE}$ HIGH to high Z <sup>[9, 10]</sup>	–	7	–	8	ns
$t_{LZCE}$	$\overline{CE}$ LOW to low Z <sup>[10]</sup>	3	–	3	–	ns
$t_{HZCE}$	$\overline{CE}$ HIGH to high Z <sup>[9, 10]</sup>	–	7	–	8	ns
$t_{PU}$	$\overline{CE}$ LOW to power-up	0	–	0	–	ns
$t_{PD}$	$\overline{CE}$ HIGH to power-down	–	15	–	20	ns
$t_{DBE}$	Byte enable to data valid	–	7	–	8	ns
$t_{LZBE}$	Byte enable to low Z	0	–	0	–	ns
$t_{HZBE}$	Byte disable to high Z	–	7	–	8	ns
<b>Write Cycle</b> <sup>[11, 12]</sup>						
$t_{WC}$	Write cycle time	15	–	20	–	ns
$t_{SCE}$	$\overline{CE}$ LOW to write end	12	–	13	–	ns
$t_{AW}$	Address setup to write end	12	–	13	–	ns
$t_{HA}$	Address hold from write end	0	–	0	–	ns
$t_{SA}$	Address setup to write start	0	–	0	–	ns
$t_{PWE}$	$\overline{WE}$ pulse width	12	–	13	–	ns
$t_{SD}$	Data setup to write end	8	–	9	–	ns
$t_{HD}$	Data hold from write end	0	–	0	–	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to low Z <sup>[13]</sup>	3	–	3	–	ns
$t_{HZWE}$	$\overline{WE}$ LOW to high Z <sup>[13, 14]</sup>	–	7	–	8	ns
$t_{BW}$	Byte enable to end of write	12	–	13	–	ns

### Notes

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified  $I_{OL}/I_{OH}$  and 30-pF load capacitance.
- This part has a voltage regulator which steps down the voltage from 5 V to 3.3 V internally.  $t_{power}$  time has to be provided initially before a read/write operation is started.
- $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with a load capacitance of 5 pF as in part (b) of Figure 1 on page 5. Transition is measured  $\pm 500$  mV from steady-state voltage.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW, and  $\overline{WE}$  LOW.  $\overline{CE}$  and  $\overline{WE}$  must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with a load capacitance of 5 pF as in part (b) of Figure 1 on page 5. Transition is measured  $\pm 500$  mV from steady-state voltage.

### Switching Waveforms

Figure 3. Read Cycle No. 1 [15, 16]

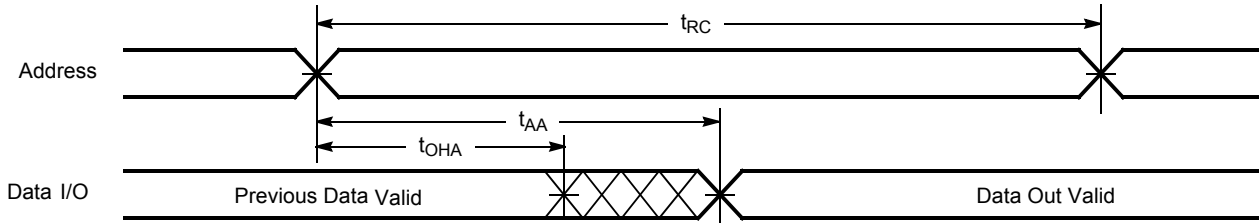
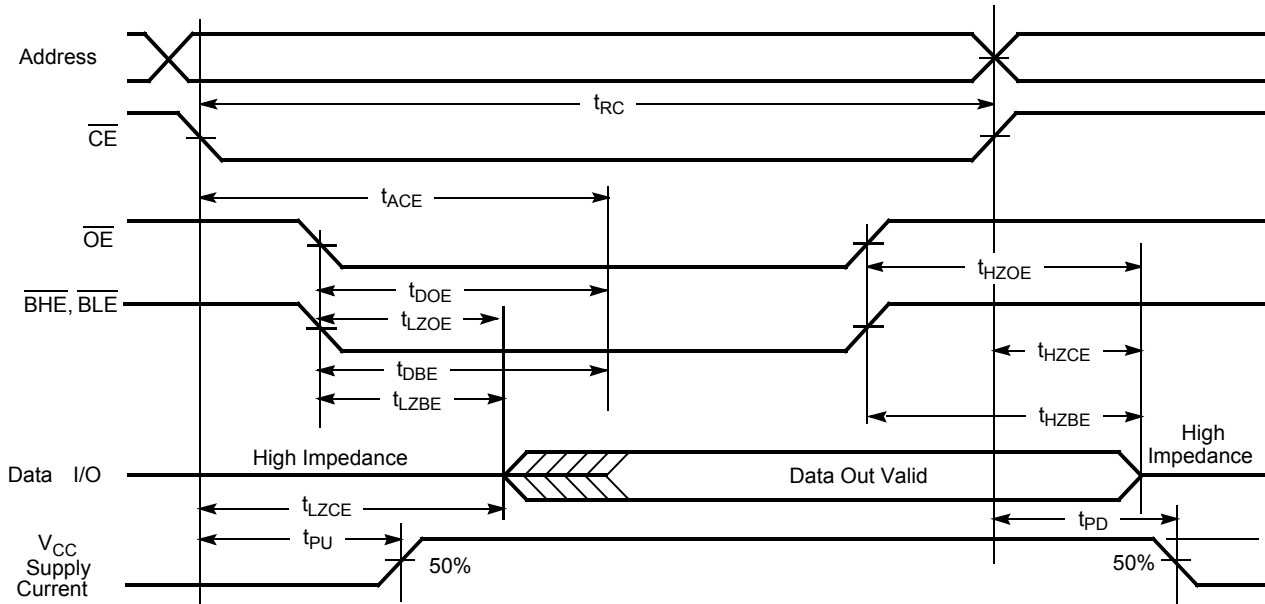


Figure 4. Read Cycle No. 2 ( $\overline{OE}$  Controlled) [16, 17]



**Notes**

- 15. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$ ,  $\overline{BHE}$ , and/or  $\overline{BLE}$  =  $V_{IL}$ .
- 16.  $\overline{WE}$  is HIGH for read cycle.
- 17. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

Switching Waveforms (continued)

Figure 5. Write Cycle No. 1 ( $\overline{\text{CE}}$  Controlled) [18, 19]

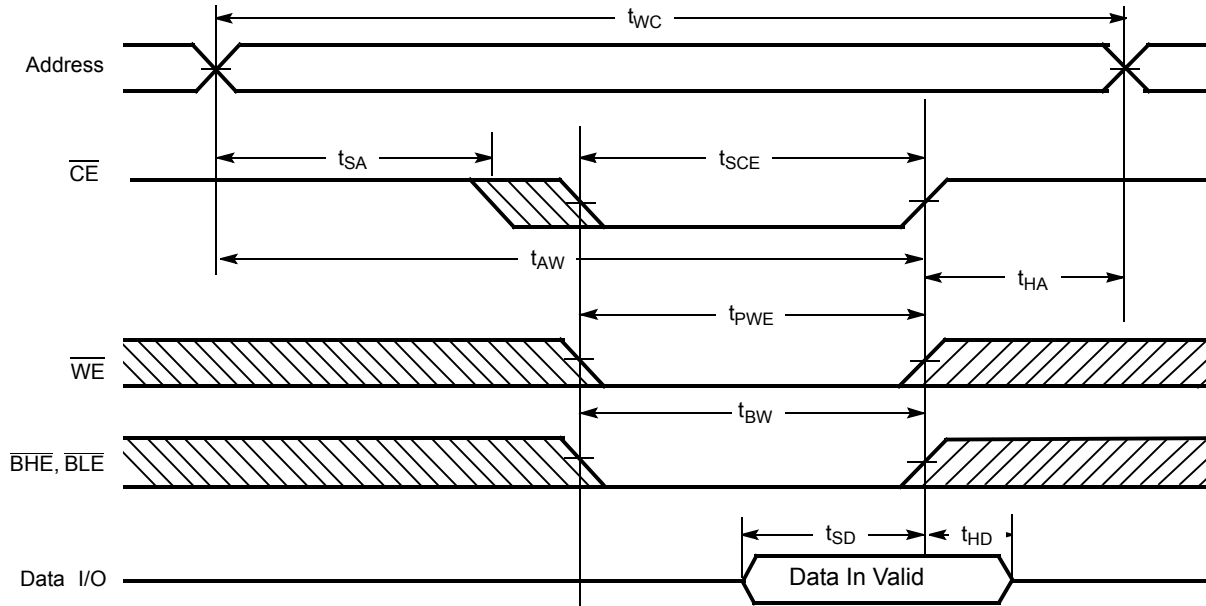
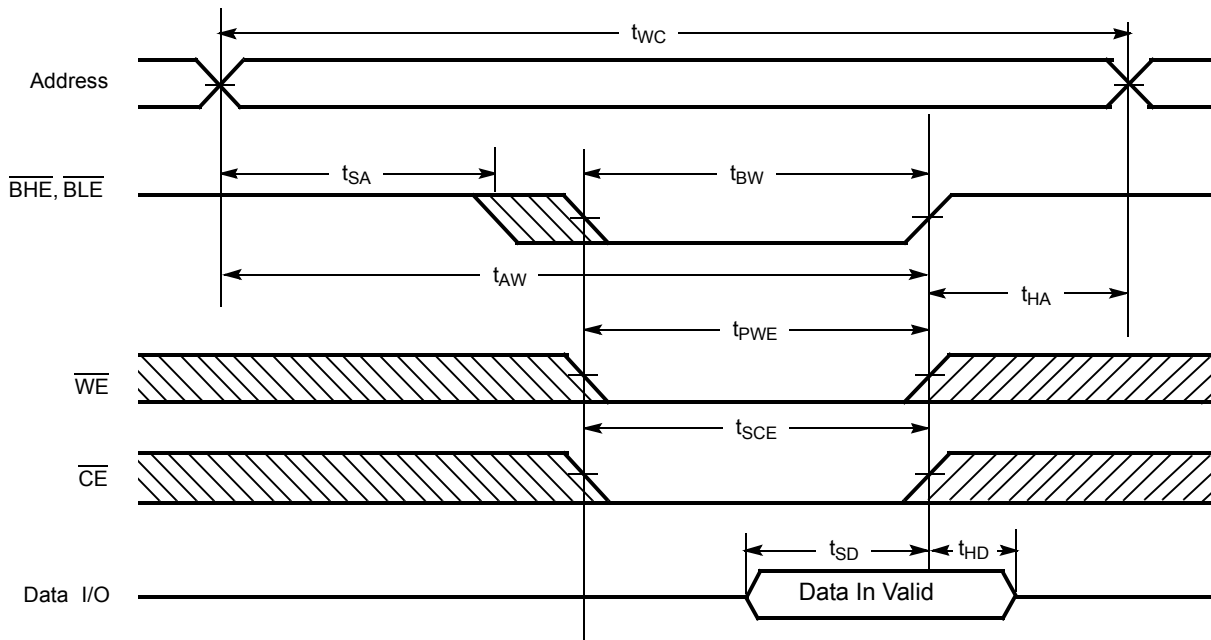


Figure 6. Write Cycle No. 2 ( $\overline{\text{BLE}}$  or  $\overline{\text{BHE}}$  Controlled)



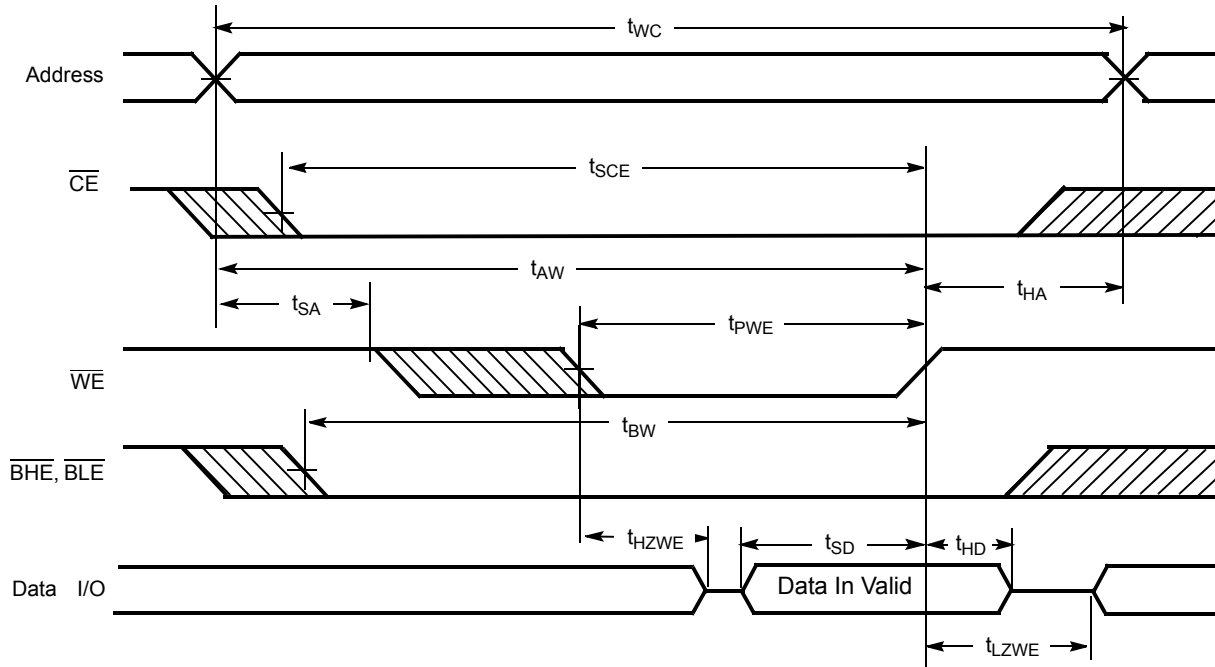
Notes

- 18. Data I/O is high impedance if  $\overline{\text{OE}}$  or  $\overline{\text{BHE}}$  and/or  $\overline{\text{BLE}} = V_{IH}$ .
- 19. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  going HIGH, the output remains in a high-impedance state.



Switching Waveforms (continued)

Figure 7. Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) <sup>[20]</sup>



Note

20. The minimum write cycle pulse width should be equal to the sum of  $t_{SD}$  and  $t_{HZWE}$ .

**Truth Table**

$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	$\overline{\text{BLE}}$	$\overline{\text{BHE}}$	I/O <sub>0</sub> –I/O <sub>7</sub>	I/O <sub>8</sub> –I/O <sub>15</sub>	Mode	Power
H	X	X	X	X	High Z	High Z	Power-down	Standby (I <sub>SB</sub> )
L	L	H	L	L	Data out	Data out	Read all bits	Active (I <sub>CC</sub> )
L	L	H	L	H	Data out	High Z	Read lower bits only	Active (I <sub>CC</sub> )
L	L	H	H	L	High Z	Data out	Read upper bits only	Active (I <sub>CC</sub> )
L	X	L	L	L	Data in	Data in	Write all bits	Active (I <sub>CC</sub> )
L	X	L	L	H	Data in	High Z	Write lower bits only	Active (I <sub>CC</sub> )
L	X	L	H	L	High Z	Data in	Write upper bits only	Active (I <sub>CC</sub> )
L	H	H	X	X	High Z	High Z	Selected, Outputs disabled	Active (I <sub>CC</sub> )
L	X	X	H	H	High Z	High Z	Selected, output disabled	Active (I <sub>CC</sub> )

## Ordering Information

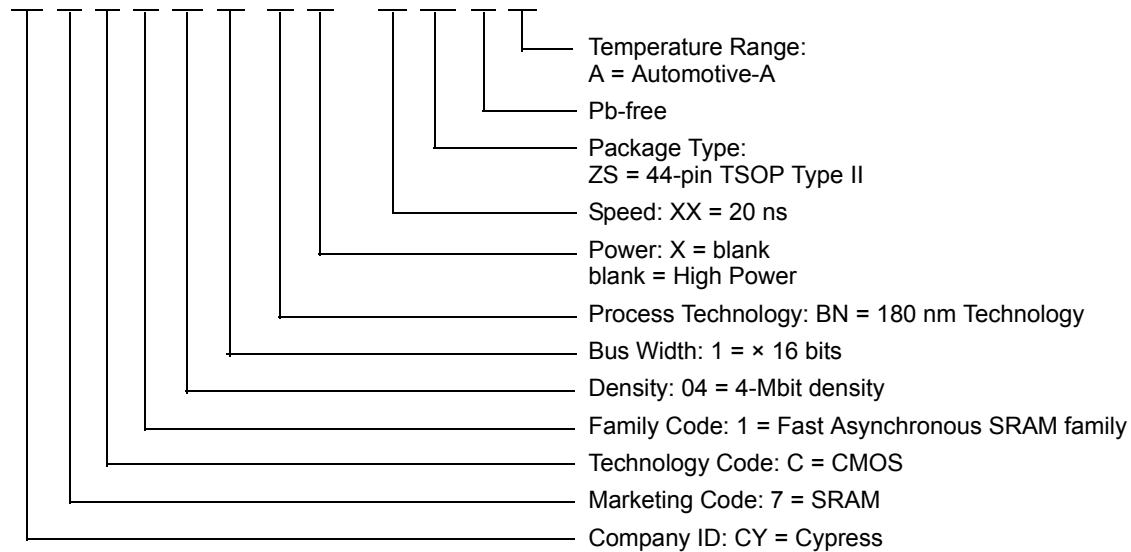
Cypress offers other versions of this type of product in many different configurations and features. The following table contains only the list of parts that are currently available. For a complete listing of all options, visit the Cypress website at <http://www.cypress.com> and refer to the product summary page at <http://www.cypress.com/products> or contact your local sales representative.

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives and distributors. To find the office closest to you, visit us at <http://www.cypress.com/go/datasheet/offices>.

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CY7C1041BN-20ZSXA	51-85087	44-pin TSOP Type II	Automotive-A

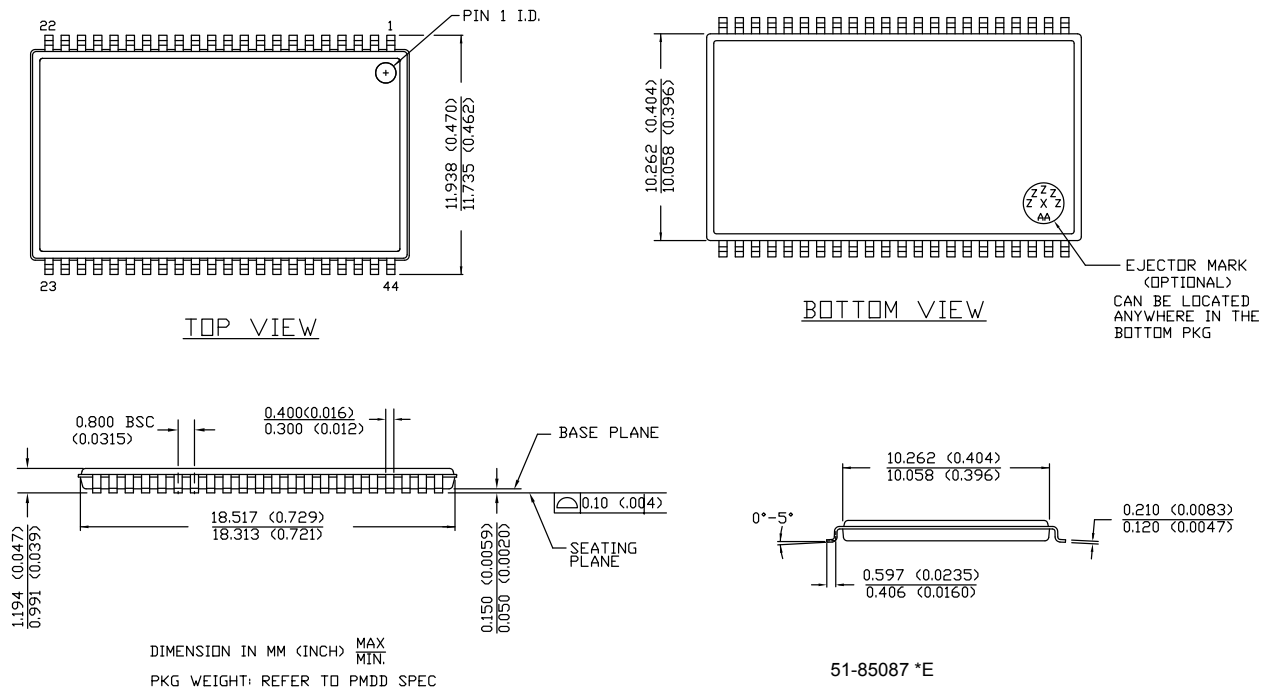
## Ordering Code Definitions

CY 7 C 1 04 1 BN X - XX XX X X



Package Diagram

Figure 8. 44-pin TSOP Z44-II Package Outline, 51-85087



## Acronyms

Acronym	Description
BHE	Byte High Enable
BLE	Byte Low Enable
CE	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
OE	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
WE	Write Enable

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
mA	milliampere
mV	millivolt
mW	milliwatt
ns	nanosecond
pF	picofarad
V	volt
W	watt

## Document History Page

Document Title: CY7C1041BN, 256K × 16 Static RAM Document Number: 001-06496				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	424111	NXR	See ECN	New data sheet.
*A	498575	NXR	See ECN	Added Automotive-A Temperature Range related information in all instances across the document. Updated <a href="#">Ordering Information</a> .
*B	2897061	AJU	03/22/10	Updated <a href="#">Ordering Information</a> : Removed obsolete parts. Updated <a href="#">Package Diagram</a> .
*C	2906679	NXR	04/07/10	Updated <a href="#">Ordering Information</a> : Removed inactive part CY7C1041BNL-20VXCT.
*D	3086674	PRAS	11/15/10	Updated <a href="#">Ordering Information</a> : Removed inactive parts (CY7C1041BN-15ZXI, CY7C1041BN-15VXI). Added <a href="#">Ordering Code Definitions</a> . Added <a href="#">Acronyms</a> .
*E	3232637	PRAS	04/20/2011	Updated <a href="#">Electrical Characteristics</a> : Changed unit for I <sub>IX</sub> and I <sub>OZ</sub> parameters from mA to μA. Added <a href="#">Units of Measure</a> . Updated to new template.
*F	3383869	TAVA	09/26/2011	Removed Industrial Temperature Range related information in all instances across the document. Replaced “Commercial-L” with “Commercial” in all instances across the document. Rearranged sections for better clarity. Updated <a href="#">Switching Waveforms</a> : Modified the notes in figures under Read cycle and Write cycle sections. Updated <a href="#">Package Diagram</a> .
*G	4113666	VINI	09/04/2013	Updated <a href="#">Package Diagram</a> : spec 51-85087 – Changed revision from *D to *E. Updated to new template. Completing Sunset Review.
*H	4545523	VINI	10/20/2014	Updated <a href="#">Features</a> : Removed “1540 mW (max.)” under “Low active power”. Updated <a href="#">Truth Table</a> : Added a row in the last to show what happens when both $\overline{BLE}$ and $\overline{BHE}$ are high. Completing Sunset Review.
*I	4576406	VINI	01/16/2015	Updated <a href="#">Functional Description</a> : Added “For a complete list of related documentation, click <a href="#">here</a> .” at the end. Updated <a href="#">Switching Waveforms</a> : Added Note 20 and referred the same note in <a href="#">Figure 7</a> .
*J	5508709	VINI	11/03/2016	Updated <a href="#">Ordering Information</a> : Updated part numbers. Updated to new template. Completing Sunset Review.

## Sales, Solutions, and Legal Information

### Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

#### Products

ARM® Cortex® Microcontrollers	<a href="http://cypress.com/arm">cypress.com/arm</a>
Automotive	<a href="http://cypress.com/automotive">cypress.com/automotive</a>
Clocks & Buffers	<a href="http://cypress.com/clocks">cypress.com/clocks</a>
Interface	<a href="http://cypress.com/interface">cypress.com/interface</a>
Internet of Things	<a href="http://cypress.com/iot">cypress.com/iot</a>
Lighting & Power Control	<a href="http://cypress.com/powerpsoc">cypress.com/powerpsoc</a>
Memory	<a href="http://cypress.com/memory">cypress.com/memory</a>
PSoC	<a href="http://cypress.com/psoc">cypress.com/psoc</a>
Touch Sensing	<a href="http://cypress.com/touch">cypress.com/touch</a>
USB Controllers	<a href="http://cypress.com/usb">cypress.com/usb</a>
Wireless/RF	<a href="http://cypress.com/wireless">cypress.com/wireless</a>

#### PSoC® Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#)

#### Cypress Developer Community

[Forums](#) | [Projects](#) | [Video](#) | [Blogs](#) | [Training](#) | [Components](#)

#### Technical Support

[cypress.com/support](http://cypress.com/support)

© Cypress Semiconductor Corporation, 2006-2016. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit [cypress.com](http://cypress.com). Other names and brands may be claimed as property of their respective owners.