FAIRCHILD SEMICONDUCTOR®

October 2007

FMS6408
Precision Triple Video Filter Driver for RGB and YUV Signals

Features

- 7.6MHz 5th order RGB/YUV/YC CV filters
- 50dB stopband attenuation at 27MHz on all outputs
- Better than 0.5dB flatness to 4.2MHz on all outputs
- No external frequency selection components or clocks
- AC coupled inputs and AC or DC coupled outputs
- Supports both NTSC and PAL luminance bandwidth
- Continuous time, low-pass filters for video anti-aliasing or reconstruction applications
- <1% differential gain with 0.5° differential phase on all channels
- Integrated DC restore circuitry with low tilt

Applications

- Cable Set-top Boxes
- Satellite Set-top Boxes
- Terrestrial Set-top Boxes
- DVD Players
- Personal Video Recorders (PVR)
- Video-On-Demand (VOD)

Description

The FMS6408 provides three video signal paths; including a two-input MUX, a video filter, and a 6dB gain output driver. The filter bandwidth supports RGB and YUV signals in NTSC or PAL formats.

The video filters approximate a 5th-order Butterworth low-pass characteristic optimized for minimum overshoot and flat group delay to provide excellent image quality. Four different peaking options are available. The video filters can be bypassed if desired.

In a typical application, the RGB or YUV DAC outputs are AC coupled into the filters through the input MUX. All channels have DC restore circuitry to clamp the DC input levels during video sync. The clamp pulse derived from the selected Y input controls three independent feedback clamps. All outputs are capable of driving $2V_{pp}$, AC or DC coupled, into either a single (150Ω) or dual (75Ω) video load. The FMS6408 clamp levels can be factory programmed for YUV / RGB (250mV for all channels), YC / YPbPr (250mV on channel 1 and 1.125V on channels 2 and 3) or YC CV (250mV on channels 1 and 3 and 1.125V on channel 2).

Ordering Information

Part Number	Clamping Mode	Peaking Mode (dB)	Y_{OUT} Level (mV)	U_{OUT} Level (V)	Package	Packing Method
FMS6408MTC141	YPbPr/YC	0	250	1.125	14-Lead, Thin Shrink Small Outline Package (TSSOP)	94 Units Tube
FMS6408MTC141X	YPbPr/YC	0	250	1.125	14-Lead, Thin Shrink Small Outline Package (TSSOP)	2500 Units Tape and Reel
FMS6408MTC142	YPbPr/YC	0.4	250	1.125	14-Lead, Thin Shrink Small Outline Package (TSSOP)	94 Units Tube
FMS6408MTC143	YPbPr/YC	0.9	250	1.125	14-Lead, Thin Shrink Small Outline Package (TSSOP)	94 Units Tube
FMS6408MTC143X	YPbPr/YC	0.9	250	1.125	14-Lead, Thin Shrink Small Outline Package (TSSOP)	2500 Units Tape and Reel

Continued on following page…

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Ordering Information (Continued)

Part Number	Clamping Mode	Peaking Mode (dB)	Y_{OUT} Level (mV)	U_{OUT} Level (V)	Package	Packing Method
FMS6408MTC144	YPbPr/YC	1.3	250	1.125	14-Lead, Thin Shrink Small Outline Package (TSSOP)	94 Units Tube
FMS6408MTC145	YUV/RGB	0	250	250	14-Lead, Thin Shrink Small Outline Package (TSSOP)	94 Units Tube
FMS6408MTC146	YUV/RGB	0.4	250	250	14-Lead, Thin Shrink Small Outline Package (TSSOP)	94 Units Tube
FMS6408MTC147	YUV/RGB	0.9	250	250	14-Lead, Thin Shrink Small Outline Package (TSSOP)	94 Units Tube
FMS6408MTC148	YUV/RGB	1.3	250	250	14-Lead, Thin Shrink Small Outline Package (TSSOP)	94 Units Tube
FMS6408MTC149	YC/CV	0	250	1.125	14-Lead, Thin Shrink Small Outline Package (TSSOP)	94 Units Tube
FMS6408MTC1410	YC/CV	0.4	250	1.125	14-Lead, Thin Shrink Small Outline Package (TSSOP)	94 Units Tube
FMS6408MTC1411	YC/CV	0.9	250	1.125	14-Lead, Thin Shrink Small Outline Package (TSSOP)	94 Units Tube
FMS6408MTC1412	YC/CV	1.3	250	1.125	14-Lead, Thin Shrink Small Outline Package (TSSOP)	94 Units Tube

Notes:

1. All packages are Pb-free per JEDEC J-STD-020B standard.
2. Factory programming options allow a single die to be configured for multiple operating modes.

Block Diagram

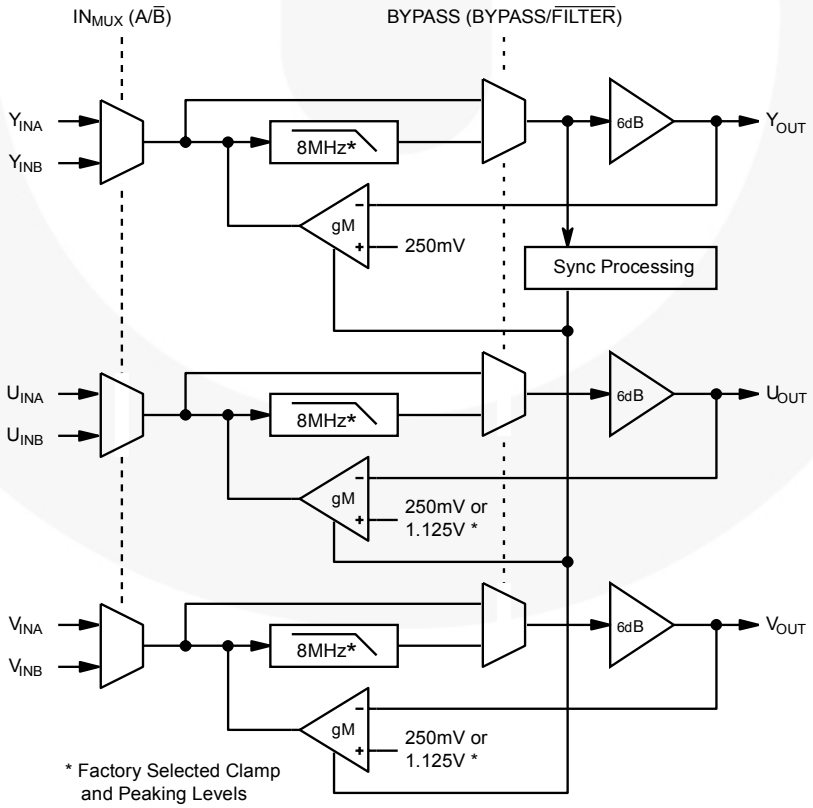

Figure 1. Block Diagram

Pin Configuration

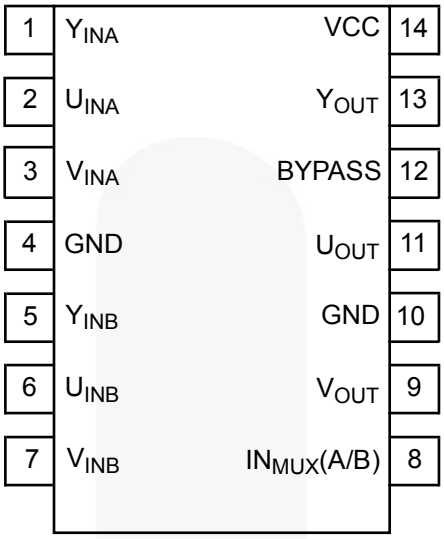

Figure 2. Pin Configuration

Pin Definitions

Pin#	Name	Type	Description
1	Y_{INA}	Input	Y (Luminance) or Green input A, must be connected to a signal that includes sync
2	U_{INA}	Input	U or Blue input A
3	V_{INA}	Input	V or Red input A
4	GND	Input	Must be tied to ground, do not float
5	Y_{INB}	Input	Y (Luminance) or Green input B, must be connected to a signal that includes sync
6	U_{INB}	Input	U or Blue input B
7	V_{INB}	Input	V or Red input B
8	$IN_{MUX}(A/\overline{B})$	Input	MUX select, A = ‘1’, B = ‘0’, must be externally tied high or low
9	V_{OUT}	Output	V or Red output
10	GND	Input	Must be tied to ground; do not float
11	U_{OUT}	Output	U or Blue output
12	BYPASS(Bypass/Filter)	Input	Filter bypass, BYPASS = ‘1’, FILTER = ‘0’, must be externally tied high or low
13	Y_{OUT}	Output	Y or Green output
14	VCC	Input	+5V supply

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Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	-0.3	6	V
	Analog and Digital	-0.3	V_{CC} + 0.3	V
	Output Current, Any One Channel (Do not exceed)		50	mA
R_S	Input Source Resistance		300	Ω

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_A	Temperature Range	-40		+85	°C
V_{CC}	V_{CC} Range	+4.75	+5.00	+5.25	V

Reliability Information

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_J	Junction Temperature			+150	°C
T_{STG}	Storage Range Temperature	-65		+150	°C
T_L	Lead Temperature (Soldering, 10 Seconds)			+300	°C
Θ_{JA}	Thermal Resistance; JEDEC Standard Multi-layer Test Boards, in Still Air		90		°C/W

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Electrical Characteristics

T_C = 25˚C, V_I = 1V_{PP}, V_{CC} = 5.0V; all inputs AC coupled with 0.1µF; all outputs AC coupled with 220µF into 150Ω, referenced to 400kHz, 0dB peaking option; unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{CC}	Supply Current(3)	V_{CC} no load		52	86	mA
V_I	Input Voltage Maximum			1.4		V_{PP}
V_{IL}	Digital Input Low(3)	Bypass, A_NB	0		0.8	V
V_{IH}	Digital Input High(3)	Bypass, A_NB	2.0		V_{CC}	V
V_{CLAMP}	Clamp Voltage(4)	YUV/RGB/CV Inputs		250		mV
		PbPr/C Inputs		1.125		V
PSRR	Power Supply Rejection Ratio	DC		-40		dB

Notes:
3. 100% tested at 25°C.
4. Mode selection for YUV/RGB vs. PbPr/YC vs. YC CV operation based on factory programming.

AC Electrical Characteristics

T_C = 25˚C, V_I = 1V_{PP}, V_{CC} = 5.0V; all inputs AC coupled with 0.1µF; all outputs AC coupled with 220µF into 150Ω, referenced to 400kHz, 0dB peaking option; unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
A_{PB}	Passband Response(5)	4.2MHz	-0.5	0		dB
AV_{LF}	Low Frequency Gain (All Channels)(5)	at 400kHz	5.6	5.9	6.2	dB
ΔAV_{HF}	Delta High Frequency at 5MHz (All Channels)(6)	0dB Peaking Option		0.3		dB
		0.4dB Peaking Option		0.7		dB
		0.9dB Peaking Option		1.2		dB
		1.3dB Peaking Option		1.6		dB
f_C	-3dB Bandwidth	All Channels		7.6		MHz
f_{SBh}	Stopband Rejection (All Channels)(5)	at 27MHz	48	52		dB
dG	Differential Gain	All Channels		0.2		%
dθ	Differential Phase	All Channels		0.5		°
THD	Total Harmonic Distortion	at 3.58MHz		0.2		%
SNR	SNR All Channels (NTC7 Weighted)	4.2MHz Lowpass, 100kHz Highpass		75		dB
H_{DIST}	Line-Time Distortion	18µs, 100 IRE Bar		TBD		%
V_{DIST}	Field-Time Distortion	130 Lines, 18µs, 100 IRE Bar		TBD		%
t_{pd}	Propagation Delay (All Channels)	400kHz		65		ns
GD	Group Delay (All Channels)	to 3.58MHz (NTSC)		14		ns
t_{SKEW}	tpdSkew Between Any 2 Channels	at 400kHz		2		ns
$A_{V(match)}$	Channel Gain Matching(5)	400kHz		0	5	%
T_{CLAMP}	Clamp Response Time (All Channels)	Settled to 10mV, Initial Condition 0V		5		ms
X_{TALK}	Crosstalk (Channel-to-Channel)	at 1.0MHz		-65		dB
IN_{MUXISO}	Input MUX Isolation	at 1.0MHz		-85		dB
f_{1dBWB}	Bypass Mode -1dB Bandwidth	1.4Vpp Output All Channels		25		MHz

Notes:
5. 100% tested at 25°C.
6. Peaking Options boost gain by 0dB, 0.4dB, 0.9dB, or 1.3dB from 4.2MHz to 5MHz based on factory programming.

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Typical Performance Characteristics

T_C = 25°C, V_I = 1V_{pp}, V_{CC} = 5.0V; all inputs AC coupled with 0.1µF; all outputs AC coupled with 220µF into 150Ω, referenced to 400kHz, 0dB peaking option; unless otherwise noted.

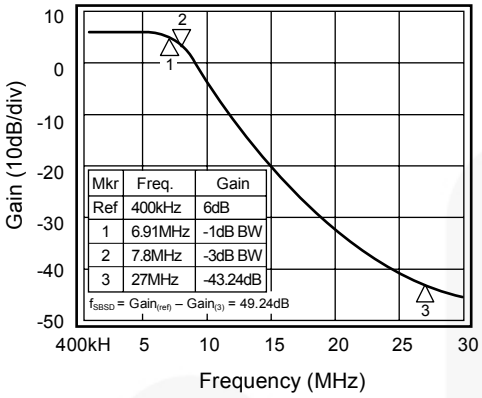

Figure 3. SD Frequency Response

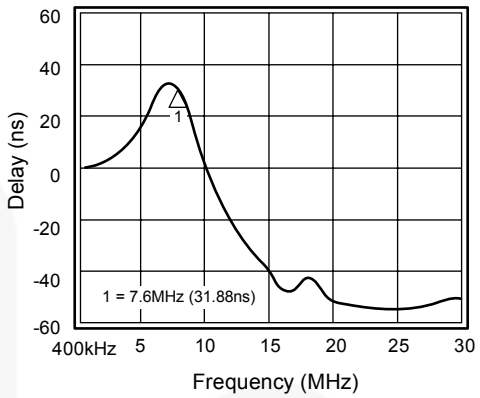

Figure 4. SD Group vs. Frequency

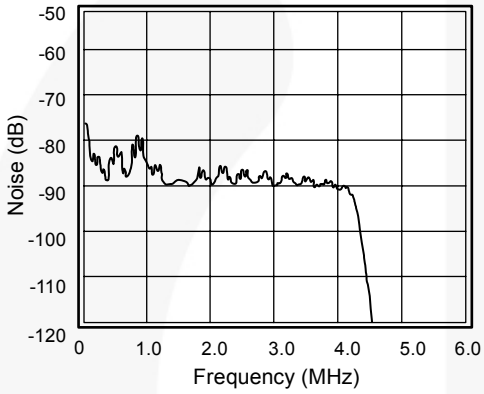

Figure 5. SD Noise vs. Frequency

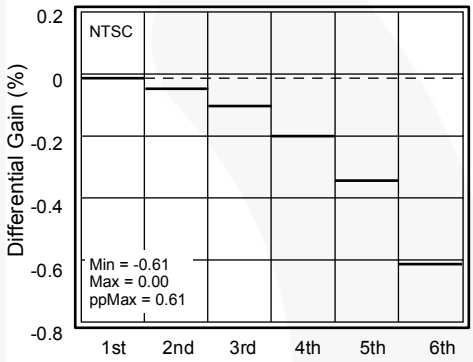

Figure 6. SD Differential Gain

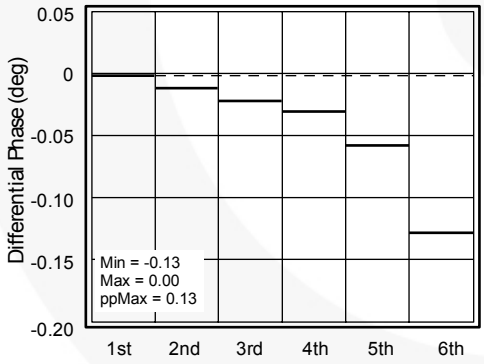

Figure 7. SD Differential Phase

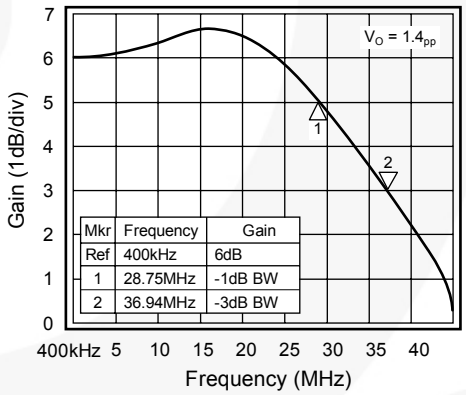

Figure 8. Bypass Mode Frequency Response

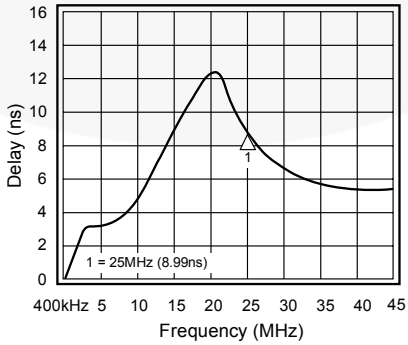

Figure 9. Bypass Mode Group Delay vs. Frequency

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Functional Description

Introduction

This product is a three-channel monolithic continuous time video filter designed for reconstructing YUV, YC CV, or RGB signals from a video D/A source. Inputs should be AC coupled while outputs can be either AC or DC coupled. The reconstruction filters approximate a 5^{th}-order Butterworth response, optimized for minimum overshoot and flat group delay. This provides a maximally flat response in terms of delay and amplitude. Each of the three outputs is capable of driving $2V_{PP}$ into 75Ω loads.

All channels are clamped during the sync interval to set the appropriate DC output level. Sync tip clamping greatly reduces the effective input time constant, allowing the use of small, low-cost input coupling capacitors. The input settles to 10mV in 2ms for typical DC shifts present in the video signal.

In most applications, the input coupling capacitors are 0.1µF. The inputs typically sink 1µA of current during active video. For YUV signals, this translates into a 2mV tilt in a horizontal line at the Y output. During sync, the clamp restores this leakage current by sourcing an average of 20µA over the clamp interval. Any change in the coupling capacitor values affects the amount of tilt per line. Any reduction in tilt comes with an increase in settling time.

Inputs

The inputs are typically be driven by either a low-impedance source of $1V_{pp}$ or the output of a 75Ω terminated line driven by the output of a current DAC. In either case, the inputs must be capacitively coupled to allow the sync-detect and DC-restore circuitry to operate properly.

Outputs

The outputs are low-impedance voltage drivers that can handle either a single or dual load. A single load consists of a 75Ω-series termination resistor feeding a 75Ω-terminated line for a total load at the part of 150Ω. Even when two loads are present (75Ω) the driver produces a full $2V_{PP}$ signal at its output pin. The driver can also be used to drive an AC coupled single or dual load. When driving a dual load, either output functions if the other output connection is inadvertently shorted, providing these loads are AC coupled.

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Typical Application Diagrams

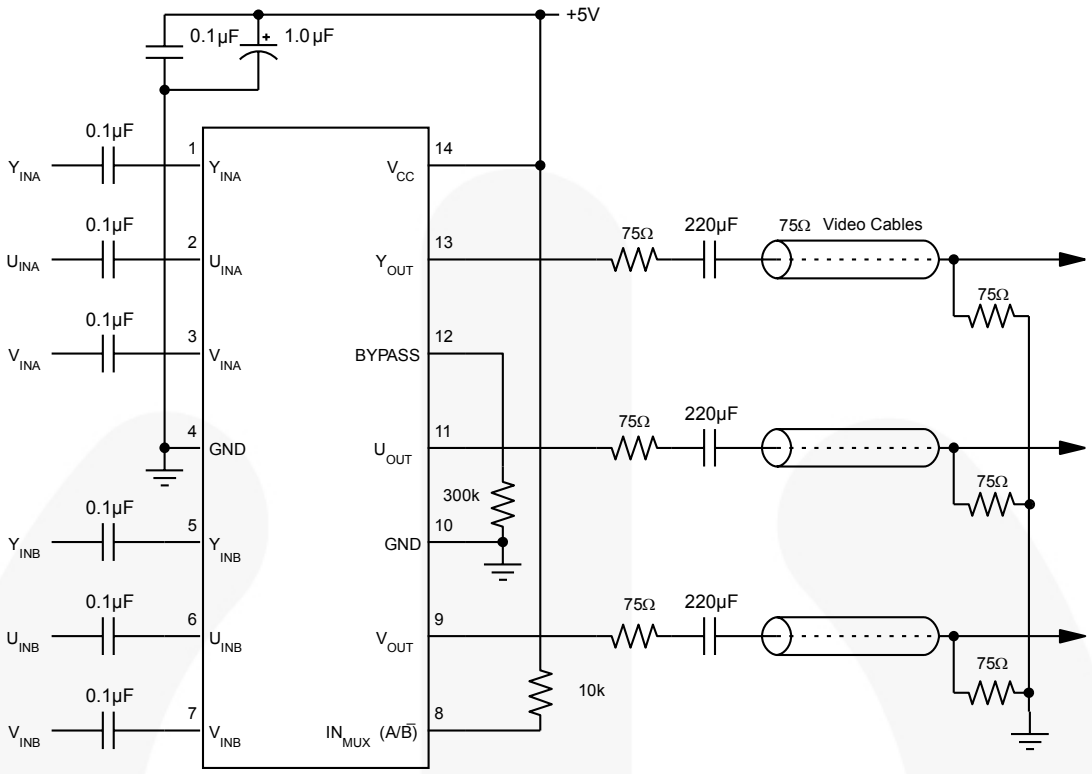

Figure 10. AC-Couples YUV Line Driver with Single Video Loads

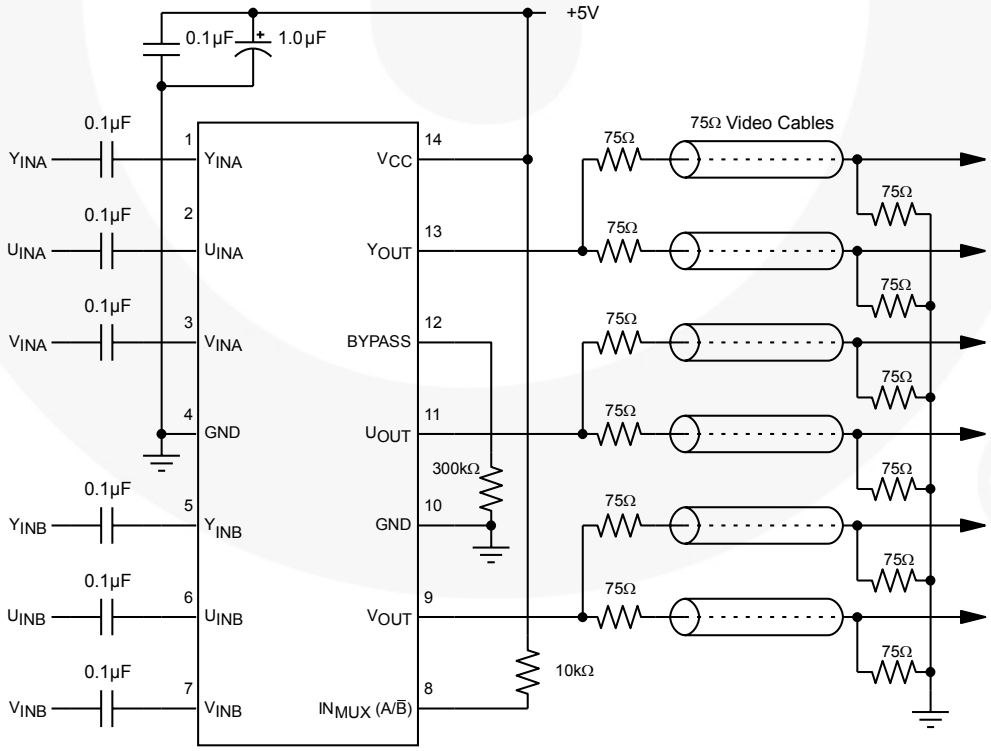

Figure 11. DC-Couples YUV Line Driver with Dual Video Loads

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Application Notes

Introduction

The FMS6408 can drive dual 75Ω loads, where each load consists of a 75Ω resistor in series with a 75Ω termination resistor in the driven device. This presents a 150Ω load to the output, so two similar loads in parallel look like 75Ω from the output to ground. In some cases, it may be desirable to drive a single load on one or more outputs with a dual load on the remaining outputs. This is an acceptable loading condition, but can cause a slight degradation in gain matching.

Device Power Dissipation

The FMS6408 specifications provide a quiescent no-load supply current of 52mA (typical). With a nominal 5V supply, this results in a power dissipation of 260mW. The overall power dissipation can be significantly affected by the applied load, particularly in DC-coupled applications. To calculate the total power dissipation the typical output voltages and the loading must be known.

The highest power dissipation occurs for YUV video signals DC-coupled into dual video loads *(refer to Figure 3).*

Assume a video signal on the Y channel that averages 50% luminance with an output voltage of 1.55V, then calculate the load current:

$$I_{LOAD}(Y) = 1.55V / 75\Omega = 20.6mA \quad (1)$$

The device dissipation due to this load is the internal voltage drop multiplied by the load current:

$$P_D(Y) = (5V - 1.55V) \bullet 20.6mA = 71mW \quad (2)$$

The average DC level for the U and V channels is set by the clamp circuit to 1.125V. The signal is symmetrical about this voltage, therefore:

$$I_{LOAD}(U) = 1.125V / 75\Omega = 15mA \quad (3)$$

The device dissipation due to this load is the internal voltage drop multiplied by the load current:

$$P_D(U) = (5V - 1.125V) \bullet 15mA = 58.125mW \quad (4)$$

Since the U and the V power dissipation are approximately the same, the total dissipation due to load can be estimated by:

$$P_D(load) = P(Y) + 2 \bullet P(U) = 71mW + 2 \bullet 58.125mW = 187.55mW \quad (5)$$

This brings the typical total device power dissipation to 260mW (quiescent power) + 187.55mW (load power) or 447.55mW. It is advisable to calculate the highest possible power dissipation using worst-case quiescent supply current and the maximum allowable power supply voltage. This result should be used when calculating the die temperature rise with the supplied θ_{JA}, thermal resistance value.

Field Time Distortion

In applications with AC-coupled outputs, the AC-coupling capacitors dominate the field time distortion. Performance is specified with 220µF coupling capacitors; if better performance is desired, the capacitors may be increased or the outputs may be DC-coupled.

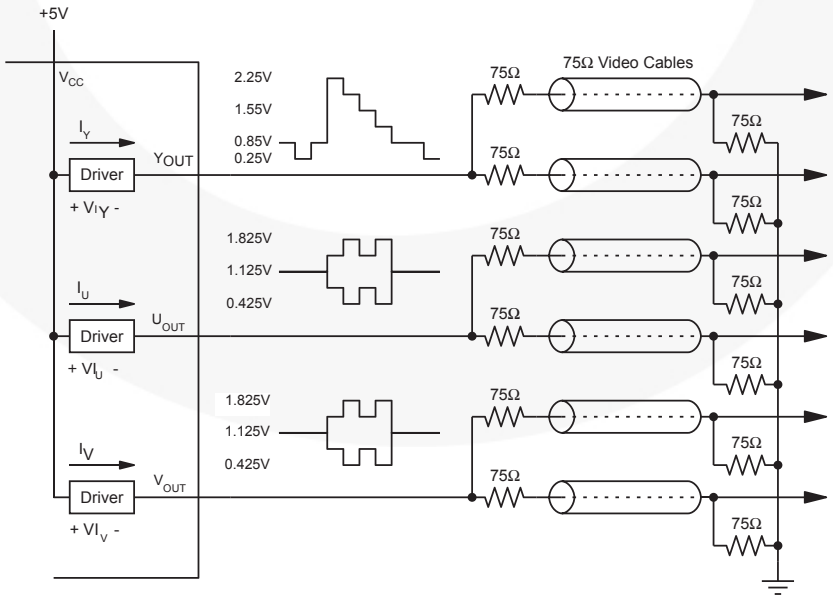

Figure 12. YUV Video Signals that are DC-Coupled into Dual Video Loads

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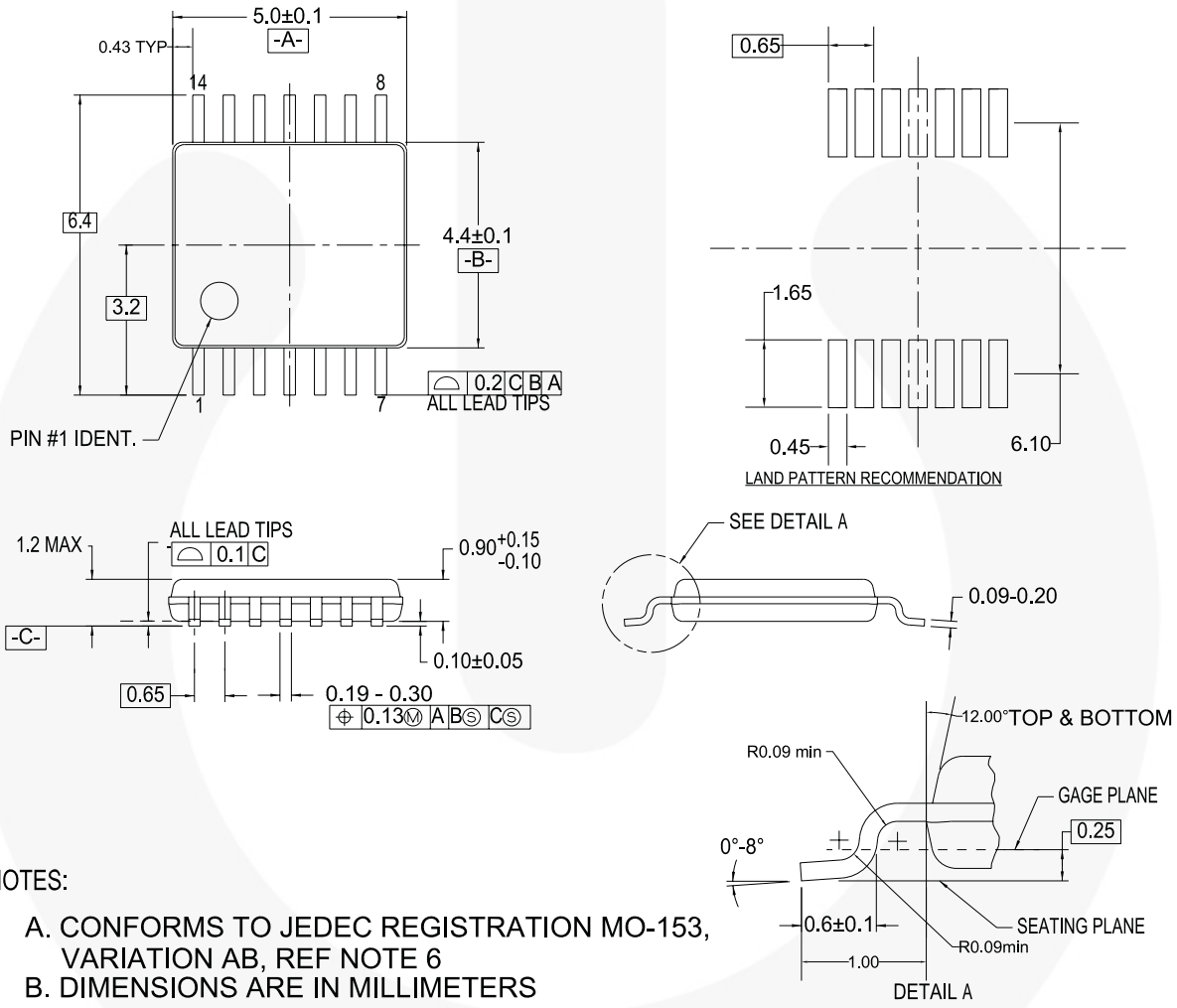
Package Dimensions

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
C	REVISE & REDRAW ON PRO/E PER CURRENT STD; CORRECT DET CALLOUT FROM D TO A	11099	08/21/95	MS/
C1	CHANGE TO (FSPM) DRAWING		4-6-98	FEITAN
C2	ADDED NOTES SECTION, ADDED RADIUS DIMS, MOLDED BODY ANGLE DIMS, AND FILENAME		6-12-98	H.ALLEN
C3	CHANGED TITLE, ADDED TITLE		6-23-98	H.ALLEN
D	CHANGED REVISION LEVEL ONLY		11/12/04	H.ALLEN
6	UPDATED LAND PATTERN		9 JULY 07	L.HUEBENER



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6
B. DIMENSIONS ARE IN MILLIMETERS
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982
E. LANDPATTERN STANDARD: SOP65P640X110-14M
F. DRAWING FILE NAME: MTC14REV6

APPROVALS	DATE
DRAWN L.HUEBENER	9 JULY 07
DFTG, CHK.	
ENGR, CHK.	

FAIRCHILD SEMICONDUCTOR™

14LD, TSSOP, JEDEC MO-153, 4.4MM WIDE

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-MTC14	6

PROJECTION INCH (MM)

DO NOT SCALE DRAWING | SHEET 1 of 1

Figure 13. 14-Lead, Thin Shrink Small Outline Package (TSSOP)

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Power247®
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Power-SPM™
PowerTrench®
Programmable Active Droop™
QFET®
QS™
QT Optoelectronics™
Quiet Series™
RapidConfigure™
SMART START™
SPM®
STEALTH™
SuperFET™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild Semiconductor. The datasheet is printed for reference information only.

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