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PLLs WITH INTEGRATED VCO - MICROWAVE APPLICATIONS EVALUATION BOARD OPERATING GUIDE

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v01.0910

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1.0 Applicable Products

HMC764LP6CE, HMC765LP6CE, HMC783LP6CE, HMC807LP6CE

2.0 Introduction

This Operating Guide covers the specified family of Hittite fractional PLL with integrated VCO. The first portion lists the Evaluation Kit contents. The second portion describes how to operate the evaluation board.

3.0 Evaluation Kit

The Evaluation Kit contains the following contents:

- a. (1) Evaluation Board Part #:
    126791-HMC764LP6C or 127270-HMC765LP6C or
    127272-HMC783LP6C or 127283-HMC807LP6C

- b. (1) CD ROM Part # 121325

- c. (1) USB Controller Board # 122046

- d. (1) USB Cable # 690-00064-00

- e. (1) Control Cable # 595-00199-00

The CD ROM should include the followings files as a minimum:

- a. FTDI USB Drivers .zip file

- b. VB HMC PLL with Integrated VCO Controller Software

- c. PLL Design Software

- d. Evaluation Board Schematic

- e. Evaluation Board Operating Guide

- f. PLL with Integrated VCO Data Sheets

- g. PLL with Integrated VCO Operating Guide

- h. Recommended PLL Register Set Text File

- i. README Installation Guide

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4.0   Evaluation Board Operation

4.1   Configuration with On-Board Crystal Oscillator

The evaluation board of Hittite fractional PLL with integrated VCO should be set up as shown in the Figure 1. It should be noted that very low noise PLL with Integrated VCOs are sensitive to noisy power supplies. The evaluation board provides on-board regulators to isolate the +5.5V supply from the PLL analog and digital +3.3V supplies, the PLL Charge Pump +5V supply and the VCO +5V supply. The VCXO is also regulated separately to +3.3V from the +5.5V external supply.

The very low noise of the PLL with Integrated VCO requires a high quality test instrument to observe the phase noise or jitter. For this we recommend a signal analyzer such as the Agilent E5052B or equivalent. A high performance spectrum analyzer can be used as an alternative to the signal analyzer.

Figure 2 highlights the major components and connectors on the PLL with Integrated VCO evaluation Board.
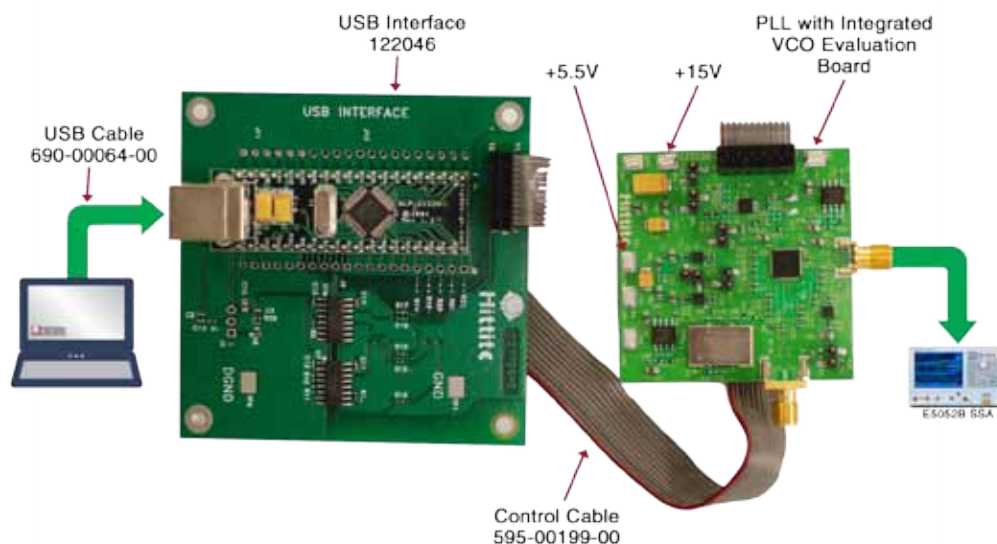

Figure 1. Typical Setup of PLL with Integrated VCO Evaluation Board

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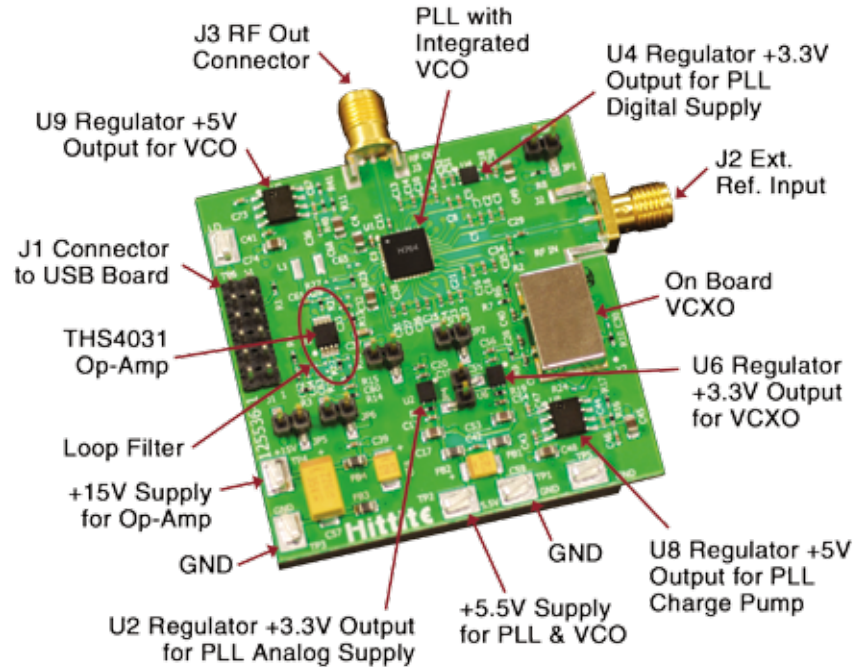*EVALUATION BOARD OPERATING GUIDE*

Figure 2. PLL with Integrated VCO Evaluation Board Major Components

4.2   Configuration with External Crystal Oscillator

If it is desired to use the evaluation board with an external crystal oscillator, disable the VCXO Regulator U6 by shorting JP4, and connect the external source to J2 as shown in Figure 3. If the external source has sufficient drive (see the reference sensitivity plots in datasheets) it is likely not necessary to remove C34, at the output of the on-board crystal oscillator, otherwise remove C34 from the board. The evaluation board has been tested with an external 100 MHz sine crystal with C34 in place with no measurable effects, however an external square wave oscillator may be more sensitive to mismatch caused by C34, hence if in doubt, remove C34.
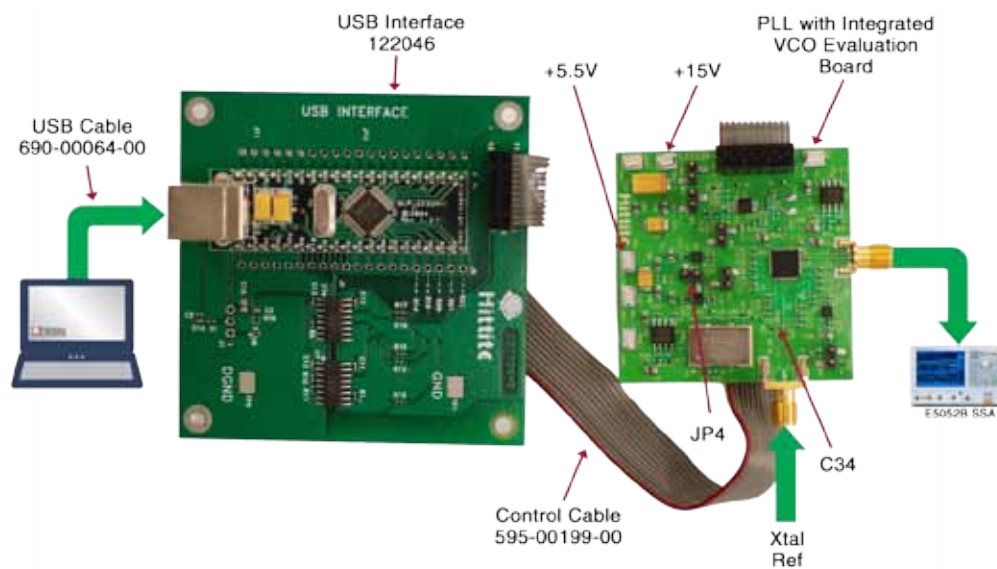

Figure 3. Typical Setup of the PLL with Integrated VCO Evaluation Board with External Crystal Oscillator

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4.3 Configuration with the Different Type of Loop Filters

Depending on the user requirements, different type of loop filters can be configured on the evaluation Board. A general schematic of loop filters is shown in Figure 4. It can be configured into most filter types, such as Passive, PassiveDC, ActiveA, ActiveC, etc. It should be noted that the default loop filter on the evaluation board is PassiveDC, and R23 is set to zero ohm, while R27, R28, C65 and L1 are open as they are optional. These components can be configured for a higher order filter to improve the spur performance; however, this can lead to loop instability if not be carefully designed.
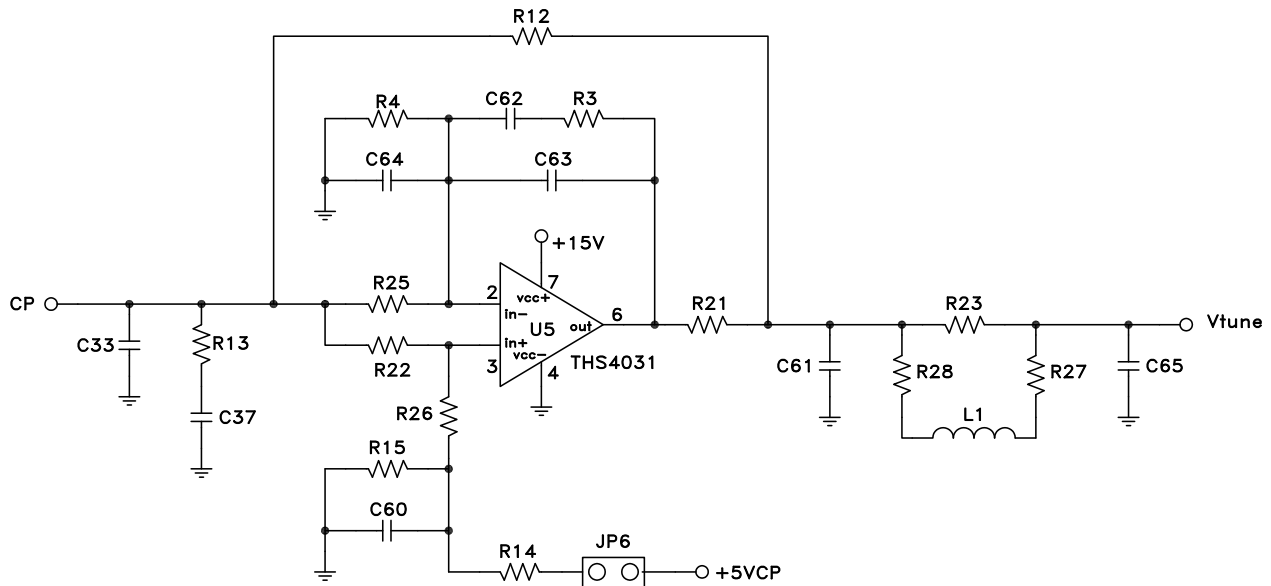

Figure 4. General Schematic of Loop Filter

Based on the general schematic above, the different type of loop filters can be configured as follows. It should be noted that the Op-amp is powered by a separate power supply, marked +15V.

![Hittite Microwave Corporation logo]

4.3.1   Passive Loop Filter

The Passive loop filter consists of C33, R13, C37, R12 and C61. It can be configured by removing R21, R22, R25, and leaving JP6 and +15V open.

It should be noted that the maximum VCO tuning voltage of the passive loop filter is limited by the charge pump power supply, for example, +5V.
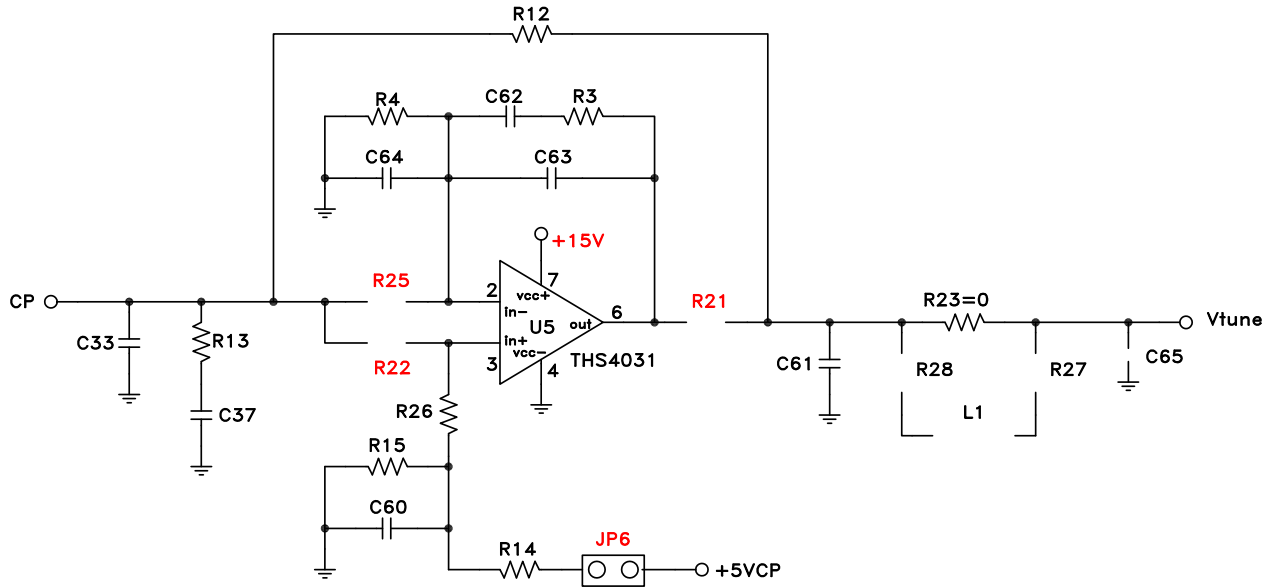

Figure 5. Passive Loop Filter

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4.3.2 PassiveDC Loop Filter (default)

The PassiveDC loop filter consists of C33, R13, C37, R3, R4, C64, R21, C61 and Op-amp U5. It can be configured by removing R12, R25, R26, C63, shorting R22, C62, leaving JP6 open, and powering +15V on.

It should be noted that when a single positive supply is applied to the Op-amp, the minimum VCO tuning voltage of the PassiveDC loop filter is limited by the common mode input voltage characteristic and the gain of the Op-amp. In order to avoid any problem in trying to utilize the VCO tuning voltage lower than 2V, a small negative supply voltage, for example –1V, should be applied to the negative supply Pin 4 of the Op-amp. Since Pin 4 is grounded on the evaluation board, it is difficult to change but can be implemented in the customer board design.
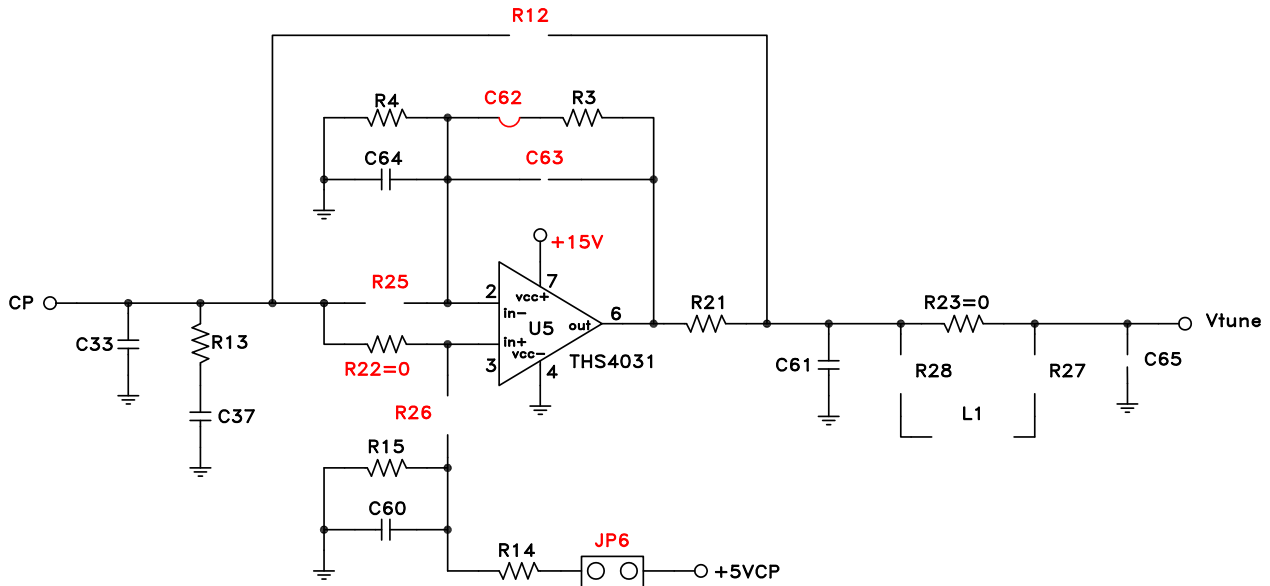

Figure 6. PassiveDC Loop Filter

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4.3.3 ActiveA Loop Filter

The ActiveA loop filter consists of C62, R3, C63, R21, C61, R14, R15, C60 and Op-amp U5. It can be configured by removing C33, C37, C64, R4, R12, R13, R22, shorting R25, R26, JP6, and powering +15V on.
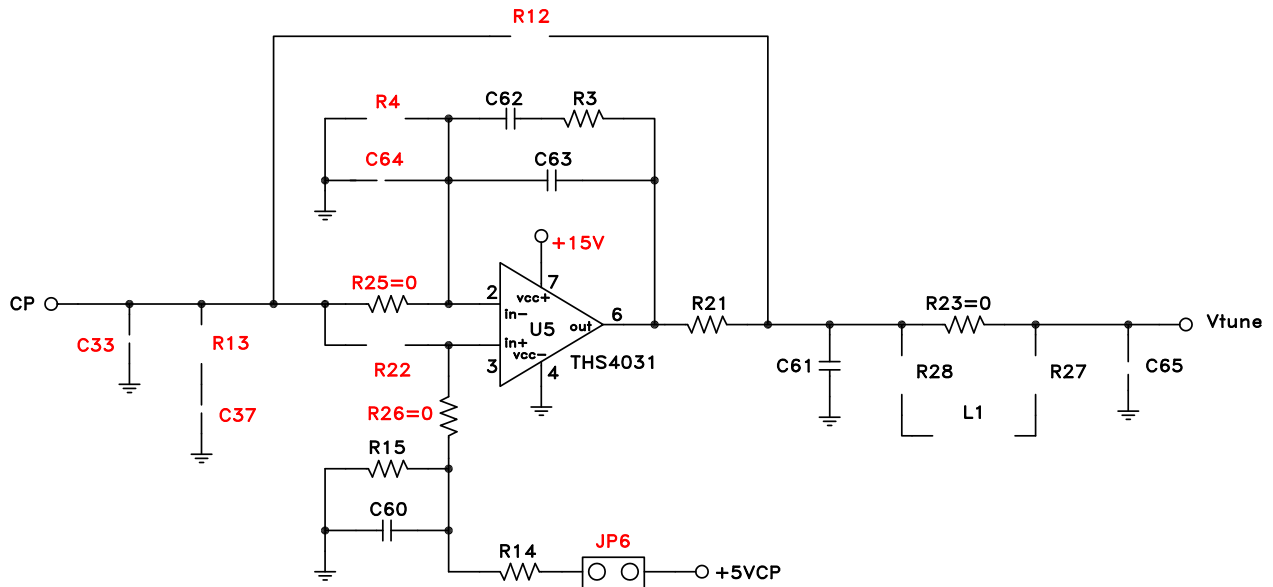
Figure 7. ActiveA Loop Filter

4.3.4 ActiveC Loop Filter

The ActiveC loop filter consists of C33, R25, C62, C63, R3, R21, C61, R14, R15, C60 and Op-amp U5. It can be configured by removing R4, R12, R13, R22, C37, C64, shorting R26, JP6, and powering +15V on.

It should be noted that the ActiveC loop filter is a very popular choice since it does not have the minimum or maximum Vtune limits as the Passive or PassiveDC filters do.
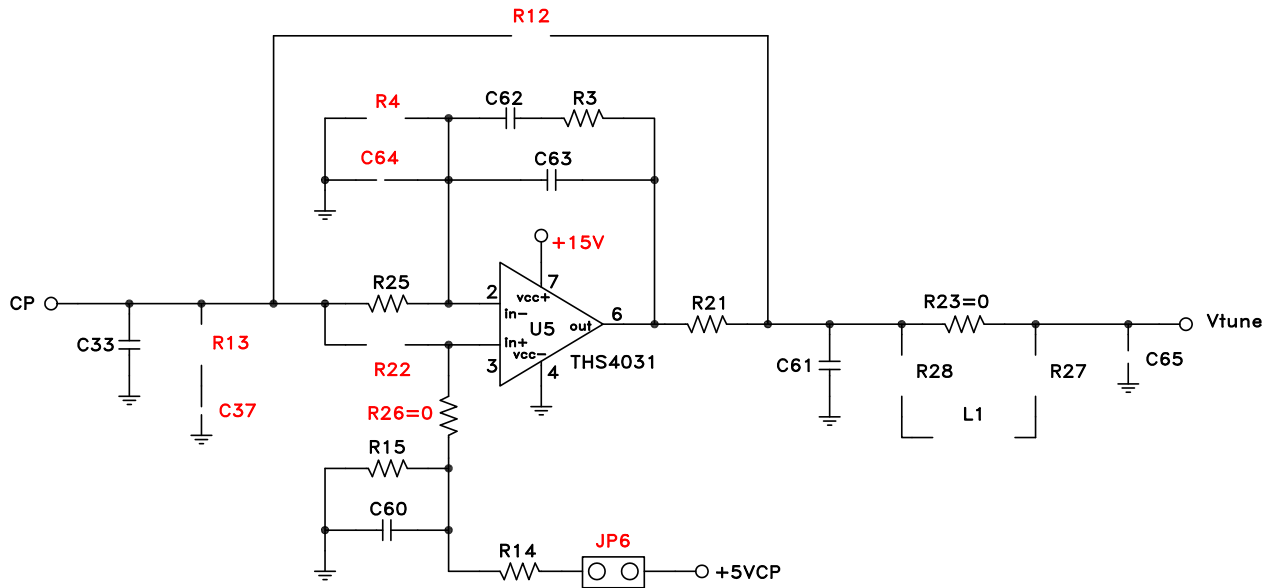
Figure 8. ActiveC Loop Filter

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5.0   Operating Procedure

Step 1. Read the "README" file for Microwave PLL with Integrated VCO on the CD for instruction.

Step 2. Setup the evaluation board as shown in Figure 1.

Step 3. Turn +5.5V and +15V supplies on.

Step 4. Launch the control program (located initial on the CD).

Step 5. From the drop down list, select the part under test, for example, HMC764LP6CE (See Figure 9).

Figure 9. Part Selection Menu

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Step 6. Click "Done" button, the main control window pops out as Figure 10 shown.

Step 7. Click "Load Reg File" button to load the register contents of the part (Figure 11).
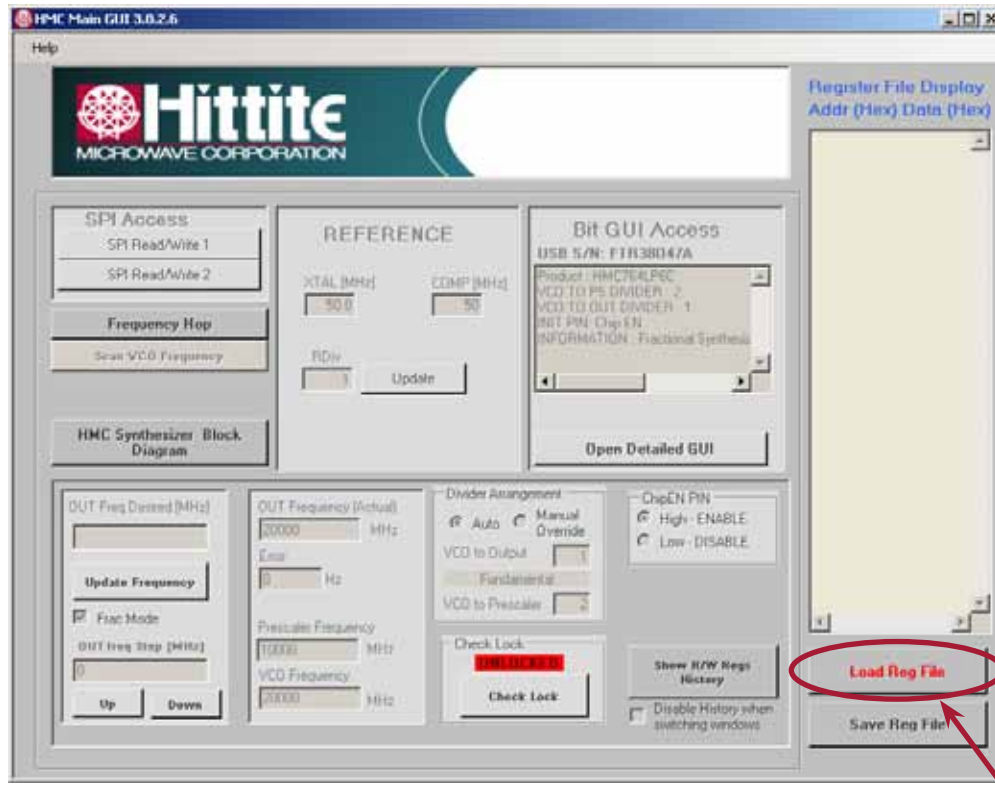

Load Register File

Figure 10. Main Control Window

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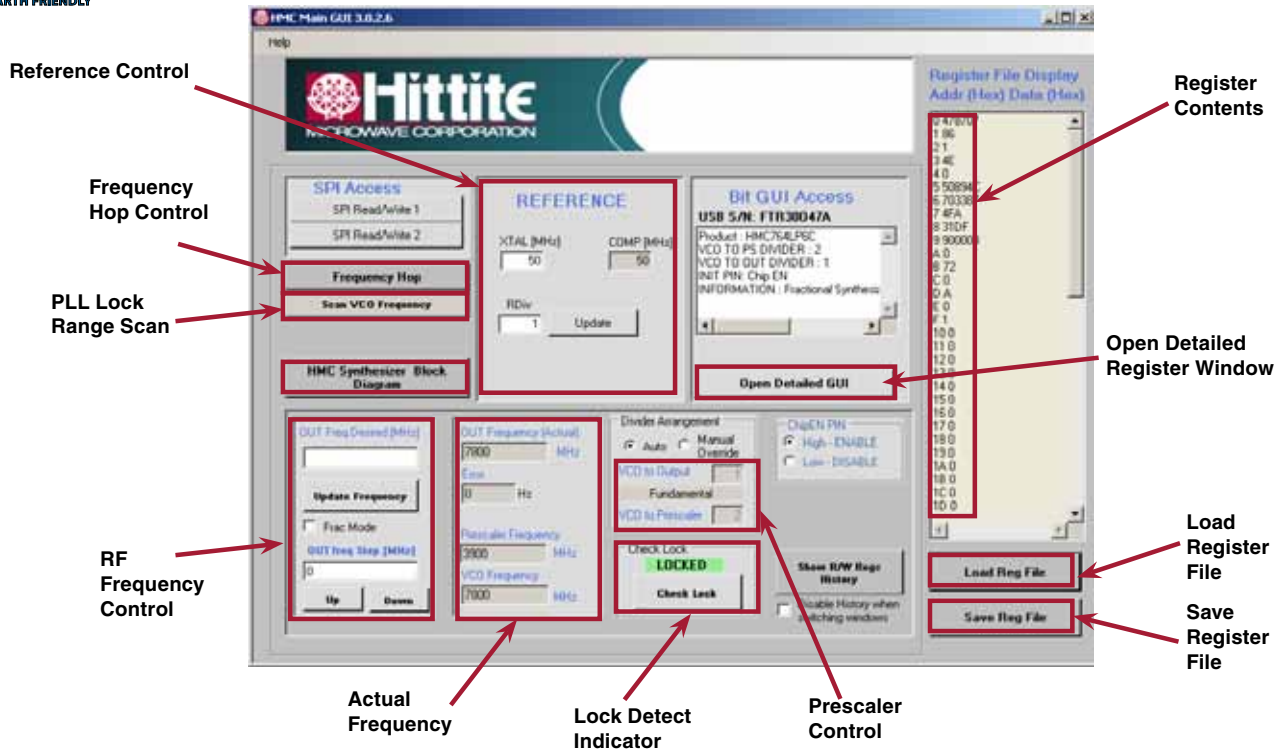

Figure 11. Main Control Window after Loading Register File

Step 8. Click "HMC PLL with Integrated VCO Block Diagram" button, the block diagram pops out as Figure 12 shown (optional to show the configuration but step not required to run the part).
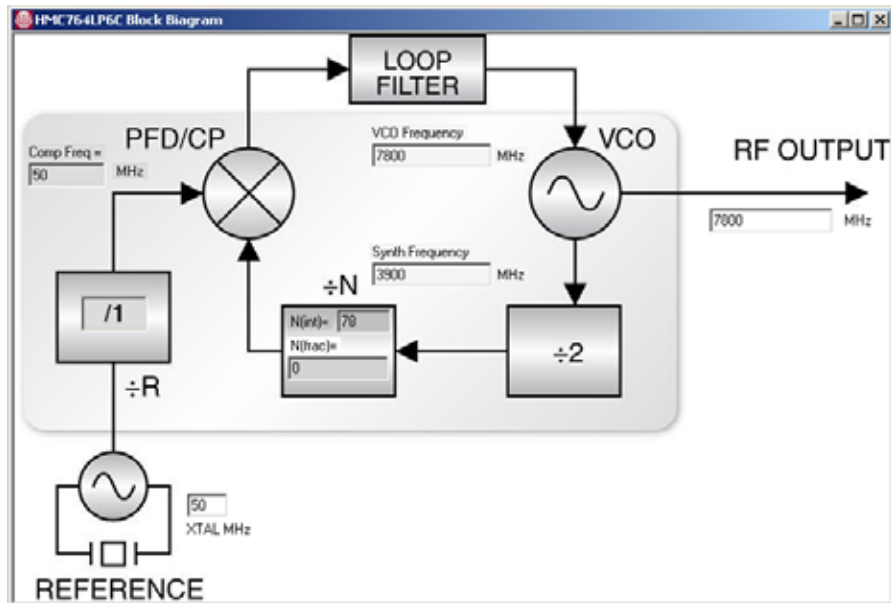

Figure 12. PLL with Integrated VCO Block Diagram

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Step 9. Set RF frequency in "RF Frequency Control" block.

For integer mode, type in the frequency desired, click "Update Frequency" button. For fractional mode, check "Frac Mode" box first. Then type in the frequency desired, click "Update Frequency" button. In order to optimize the phase noise and spur performances in fractional mode, user should click "Open Detailed GUI" button. The new detailed register control window pops out as shown in Figure 13. In the "Register 09: Charge Pump Currents" section, adjust "Dn Leak" current to optimize the phase noise and spur performances. Typically, 220 uA of current will give the optimum performances on phase noise and spurs.
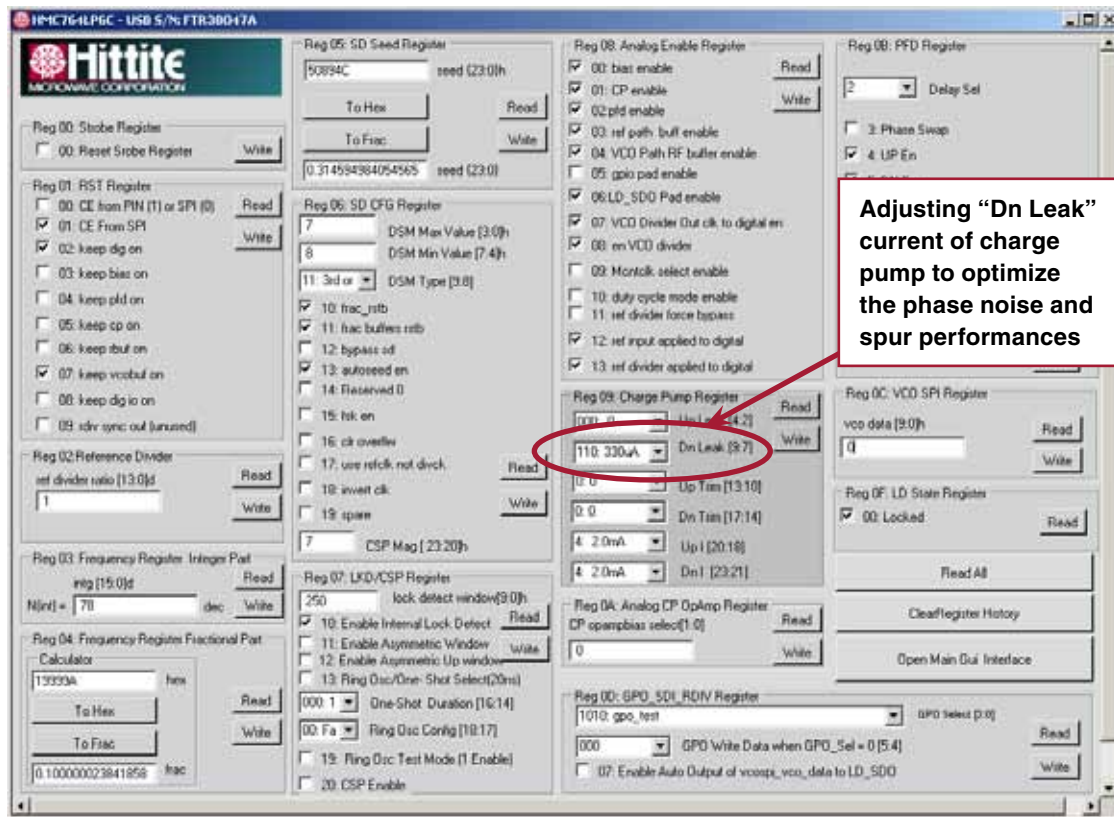

Figure 13. The Detailed Register Control Panel

Step 10. Scan the VCO frequency to find the PLL with Integrated VCO locked range ("Frac Mode" box must be checked). Click "Scan VCO Frequency" button in the main control panel (Figure 11). A new small window pops out as shown in Figure 14. Set "Start Freq", "Coarse Step" and " Freq Max Limit", click "Start Scan" button (refer to the specified Min/Max frequencies of the individual product data sheet, set "Start Freq" to Min frequency and set "Freq Max Limit" to 1 GHz above Max frequency). When the scan is finished, the PLL with Integrated VCO locked range will be shown in the window. As an example, Figure 15 shows the scan setting and scan result on HMC764LP6CE. Remember that the frequency lock range is greater than the specified frequency range and the phase noise or spurs will degrade outside of this specified window.

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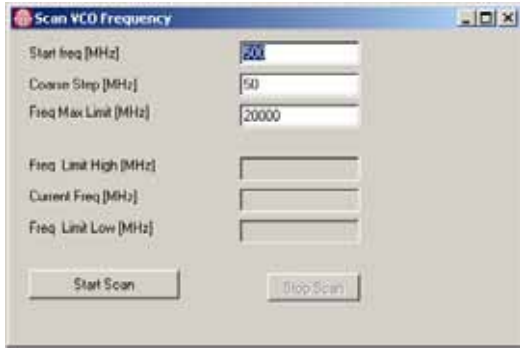**EVALUATION BOARD OPERATING GUIDE**

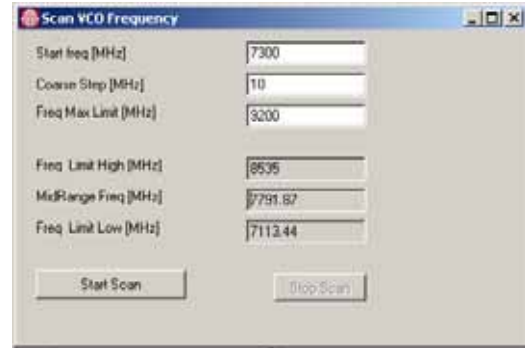*Figure 14. Default "Scan VCO Frequency" Window*

Figure 15. Scan Setting and Scan Result on HMC764LP6CE

Step 11. Run frequency hopping (optional).

Click "Frequency Hop" button in the main control panel (Figure 11). A new small window pops out as shown in Figure 16. Set "Frequency #1", "Frequency #2" and "Dwell Time" in this window. Then click "Start" button. The RF signal will switch between "Frequency #1" and "Frequency #2" in the defined "Dwell Time". Figure 17 shows a typical example of the "Frequency Hop" setting on the HMC764LP6CE. This function usually is used to find the frequency settling time of the PLL with Integrated VCO.
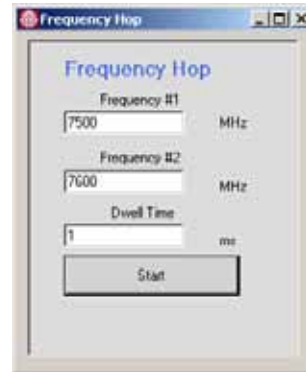

Figure 16. Default "Frequency Hop" Window

Figure 17. Typical Setting Example of Frequency Hop

Notes: