



# STPMS1

## Dual-channel 1-bit, 2 MHz, 1<sup>st</sup> order sigma-delta modulator with embedded PGA

### Features

- V<sub>CC</sub> supply range: 3.2 V - 5.5 V
- Two 1<sup>st</sup> order sigma-delta modulators
- Programmable chopper-stabilized low noise and low offset amplifier
- Supports 50-60 Hz AC watt meters
- Internal low-drop regulator at 3 V (typ.)
- Precision voltage reference: 1.23 V and 30 ppm/°C (typ.)

### Applications

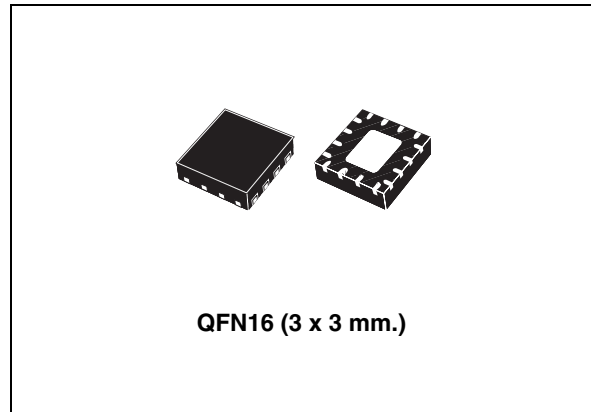
- Power metering
- Motor control
- Industrial process control
- Weight scale
- Pressure transducers

### Description

The STPMS1, also called a smart-sensor device, is an ASSP designed for effective measurement in power line systems utilizing the Rogowski coil, current transformer, or shunt principle. It is used in combination with the STPMC1 programmable poly-phase energy calculator IC, as a building block for single-phase or poly-phase energy meters. The STPMS1 is a mixed signal IC consisting of an analog and a digital section. The analog section consists of a pre-amplifier and two 1<sup>st</sup> order  $\Sigma\Delta$  modulator blocks, band-gap voltage reference, a low-drop voltage regulator, and DC buffers, while the digital section consists of a clock generator and output multiplexer. This device is designed for use in medium resolution

**Table 1. Device summary**

| Order code | Package          | Packaging           |
|------------|------------------|---------------------|
| STPMS1BPQR | QFN16 (3 x 3 mm) | 2500 parts per reel |



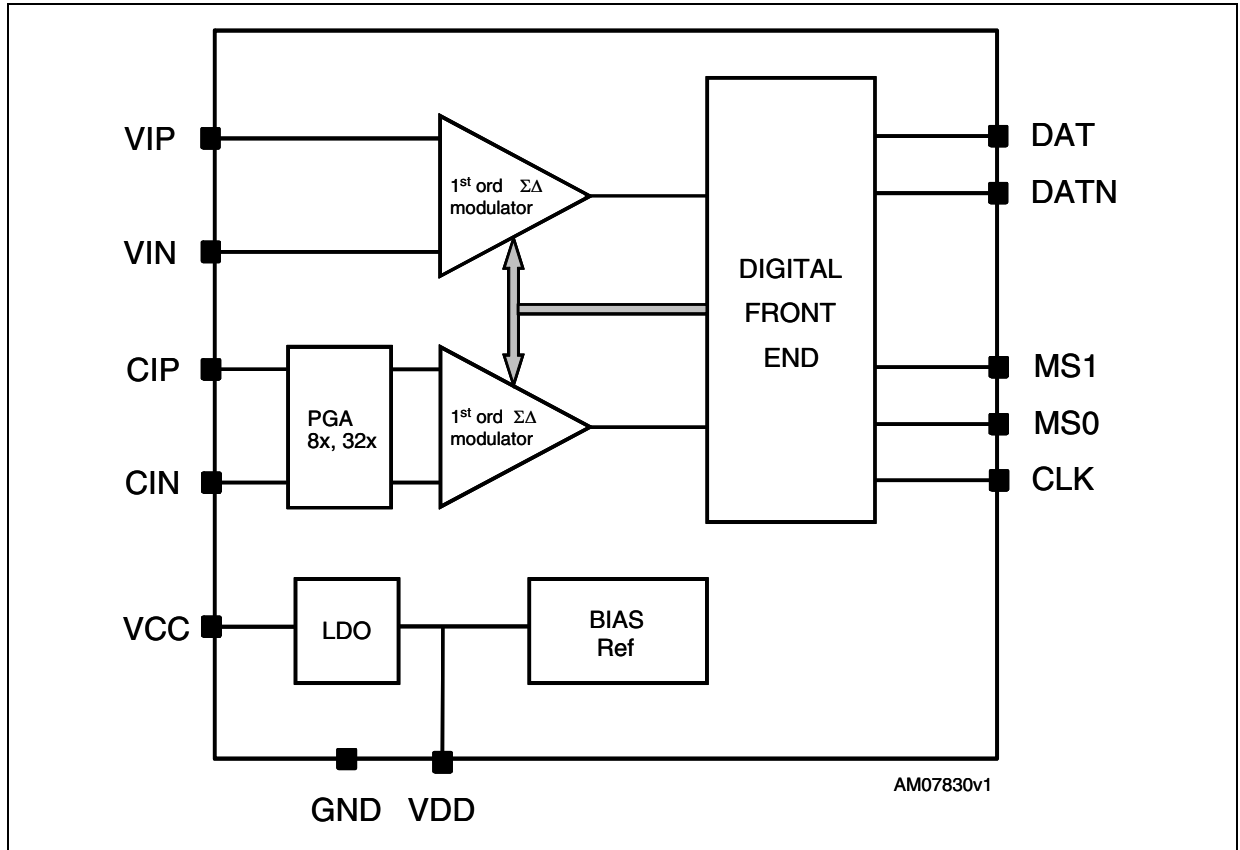
measurement applications when single or double inputs must be monitored at the same time.

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# 1 Schematic diagram

Figure 1. Block diagram



## 2 Pin configuration

Figure 2. Pin connection (top view)

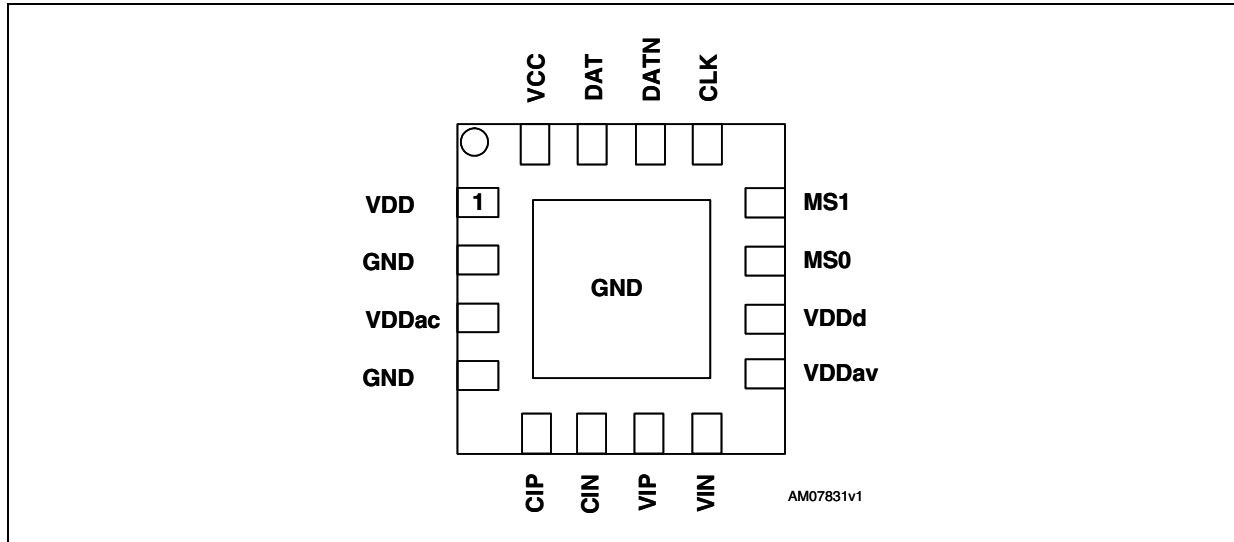


Table 2. Pin description

| Pin     | Symbol | Description   |
|---------|--------|---|
| 1       | VDD    | + 3.0 V output of LDO                               |
| 2       | GND    | Ground level for signals and pin protection         |
| 3       | VDDac  | Current channel modulator supply input              |
| 4       | GND    | Ground level for signals and pin protection         |
| 5       | CIP    | Current channel +                                   |
| 6       | CIN    | Current channel -                                   |
| 7       | VIP    | Voltage channel +                                   |
| 8       | VIN    | Voltage channel -                                   |
| 9       | VDDav  | Voltage channel modulator supply input              |
| 10      | VDDd   | Digital front-end supply input                      |
| 11      | MS0    | Input for configurator 0                            |
| 12      | MS1    | Input for configurator 1                            |
| 13      | CLK    | Input for external measurement clock                |
| 14      | DAT    | Output of multiplexed $\Sigma\Delta$ signal         |
| 15      | DATn   | Output of multiplexed $\Sigma\Delta$ signal negated |
| 16      | VCC    | Unregulated supply voltage                          |
| Exp PAD | GND    | Ground level for signals and pin protection         |

### 3 Electrical characteristics

**Table 3. Absolute maximum ratings**

| Symbol           | Parameter  | Value                        | Unit |
|------------------|--|------------------------------|------|
| V <sub>CC</sub>  | DC input voltage   | -0.3 to 6                    | V    |
| I <sub>PIN</sub> | Current on any pin (sink/source)                         | ±150                         | mA   |
| V <sub>ID</sub>  | Input voltage at digital pins (MS0, MS1, CLK, DAT, DATN) | -0.3 to V <sub>CC</sub> +0.3 | V    |
| V <sub>IA</sub>  | Input voltage at analog pins (VIP, VIN, CIP, CIN)        | -0.7 to 0.7                  | V    |
| ESD              | Human body model (all pins)                              | ±3.5                         | kV   |
| T <sub>OP</sub>  | Operating ambient temperature                            | -40 to 85                    | °C   |
| T <sub>J</sub>   | Junction temperature                                     | -40 to 150                   | °C   |
| T <sub>STG</sub> | Storage temperature range                                | -55 to 150                   | °C   |

*Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.*

**Table 4. Thermal data**

| Symbol            | Parameter                           | Value                | Unit |
|-------------------|-------------------------------------|----------------------|------|
| R <sub>thJA</sub> | Thermal resistance junction-ambient | 38.10 <sup>(1)</sup> | °C/W |

1. This value refers to a single-layer PCB, JEDEC standard test board.

## 4 General operating conditions

$V_{CC} = 5\text{ V}$ ,  $T_A = 25\text{ }^\circ\text{C}$ ,  $2.2\text{ }\mu\text{F}$  between  $V_{DD}$  and GND,  $100\text{ nF}$  between  $V_{CC}$  and GND,  $f_{CLK} = 2.048\text{ MHz}$  unless otherwise specified.

**Table 5. General operating conditions**

| Symbol                         | Parameter                           | Test conditions   | Min.  | Typ.  | Max.  | Unit                  |
|--------------------------------|-------------------------------------|---|-------|-------|-------|-----------------------|
| <b>General section</b>         |                                     |   |       |       |       |                       |
| $V_{CC}$                       | Operating supply voltage            |   | 3.165 |       | 5.5   | V                     |
| $I_{CC}$                       | Quiescent current                   | 1.049 MHz; $V_{CC}=3.165\text{ V}$ ; $C_L=100\text{ nF}$ , no loads   |       | 2.5   |       | mA                    |
| $V_{POR}$                      | Power on reset on $V_{CC}$          |   |       | 2.5   |       | V                     |
| $V_{DD}$                       | Regulated supply voltage            | 1.049 MHz; $V_{CC}=3.2\text{ V}$ ; $C_L=100\text{ nF}$ , no loads   | 2.85  | 3.00  | 3.15  | V                     |
| $I_{LATCH}$                    | Current injection latch-up immunity |   |       |       | 300   | mA                    |
| $f_{CLK}$                      | Nominal frequencies                 |   | 1.0   |       | 2.458 | MHz                   |
| <b>DC measurement accuracy</b> |                                     |   |       |       |       |                       |
|                                | Resolution                          |   | 11    |       | 16    | bit                   |
| INL                            | Integral non-linearity              | Result referred to a 13-bit resolution of CIP-CIN channel   |       | 0.35  |       | LSB                   |
|                                |                                     | Result referred to a 9-bit resolution of VIP-VIN channel  |       | 0.5   |       |                       |
| DNL                            | Differential linearity              | Result referred to a 13-bit resolution of CIP-CIN channel   |       | 0.2   |       | LSB                   |
|                                |                                     | Result referred to a 9-bit resolution of VIP-VIN channel  |       | 0.4   |       |                       |
|                                | Offset error                        | Result referred to a 13-bit resolution of CIP-CIN channel   |       | 0.15  |       | LSB                   |
|                                |                                     | Result referred to a 9-bit resolution of VIP-VIN channel  |       | 0.05  |       |                       |
|                                | Gain error                          | Result referred to a 13-bit resolution of CIP-CIN channel   |       | 0.05  |       | LSB/<br>$\mu\text{V}$ |
|                                |                                     | Result referred to a 9-bit resolution of VIP-VIN channel  |       | 0.001 |       |                       |
| NF                             | Noise floor                         | CIP-CIN channel, Gain 8x  |       | 115   |       | dB                    |
| $PSRR_{DC}$                    | Power supply DC rejection           | Voltage signal: $200\text{ mV}_{rms}/50\text{ Hz}$<br>Current signal: $10\text{ mV}_{rms}/50\text{ Hz}$<br>$f_{CLK}=2.048\text{ MHz}$<br>$V_{CC}=3.3\text{ V}\pm 10\%$ , $5\text{ V}\pm 10\%$ |       |       | 0.2   | %                     |

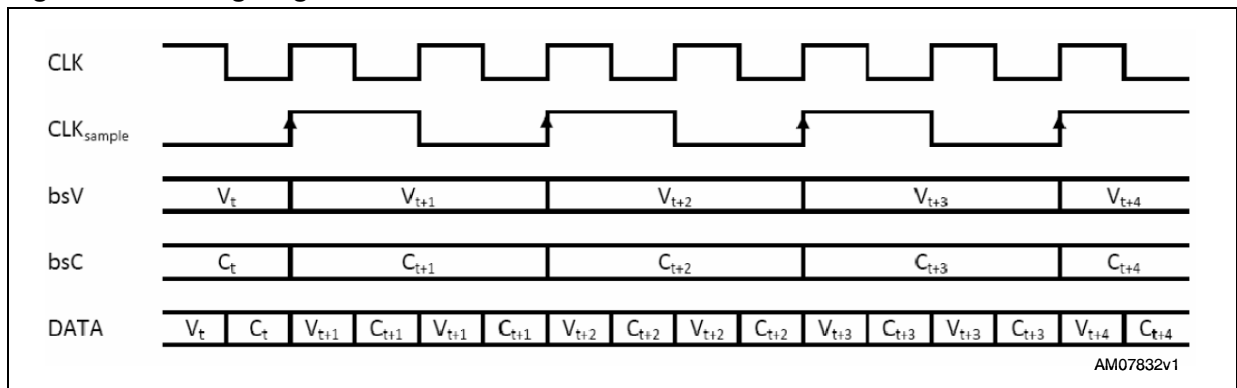
Table 5. General operating conditions (continued)

| Symbol  | Parameter                          | Test conditions   | Min.                    | Typ.                | Max.            | Unit |
|---|------------------------------------|---|-------------------------|---------------------|-----------------|------|
| <b>AC measurement accuracy</b>                |                                    |   |                         |                     |                 |      |
| SNR   | Signal to noise ratio              | CIP-CIN channel – $V_{in}=\pm 120$ mV @ 55 Hz<br>Gain 8x  |                         | 65                  |                 | dB   |
|   |                                    | VIP-VIN channel – $V_{in}=\pm 230$ mV @ 55 Hz   |                         | 50                  |                 |      |
| SINAD   | Signal to noise ratio + distortion | CIP-CIN channel – $V_{in}=\pm 120$ mV @ 55 Hz<br>Gain 8x  |                         | 65                  |                 | dB   |
|   |                                    | VIP-VIN channel – $V_{in}=\pm 230$ mV @ 55 Hz   |                         | 50                  |                 |      |
| THD   | Total harmonic distortion          | CIP-CIN channel – $V_{in}=\pm 120$ mV @ 55 Hz<br>Gain 8x  |                         | -80                 |                 | dB   |
|   |                                    | VIP-VIN channel – $V_{in}=\pm 230$ mV @ 55 Hz   |                         | -70                 |                 |      |
| SFDR  | Spurious free dynamic range        | CIP-CIN channel – $V_{in}=\pm 120$ mV @ 55 Hz<br>Gain 8x  |                         | 80                  |                 | dB   |
|   |                                    | VIP-VIN channel – $V_{in}=\pm 230$ mV @ 55 Hz   |                         | 50                  |                 |      |
| PSRR <sub>AC</sub>                            | Power supply AC rejection          | Voltage signal: 200 mV <sub>rms</sub> /50 Hz<br>Current signal: 10 mV <sub>rms</sub> /50 Hz<br>$f_{CLK}= 2.048$ MHz<br>$V_{CC}=3.3$ V+0.2 V <sub>rms</sub> 1 @ 100 Hz<br>$V_{CC}=5.0$ V+0.2 V <sub>rms</sub> 1 @ 100 Hz |                         |                     | 0.1             | %    |
| <b>Analog inputs (CIP, CIN, VIP, VIN)</b>     |                                    |   |                         |                     |                 |      |
| V <sub>MAX</sub>                              | Maximum input signal levels        | VIP-VIN channel   | -0.3                    |                     | +0.3            | V    |
|   |                                    | CIP-CIN channel<br>Gain 8X<br>Gain 32X  | -0.15<br>-0.035         |                     | +0.15<br>+0.035 | V    |
| f <sub>SPL</sub>                              | A/D sampling frequency             |   |                         | f <sub>CLK</sub> /2 |                 | Hz   |
| V <sub>off</sub>                              | Amplifier offset                   |   |                         |                     | ±20             | mV   |
| Z <sub>IP</sub>                               | VIP, VIN impedance                 | Over the total operating voltage range  | 200                     |                     | 400             | kΩ   |
| Z <sub>IN</sub>                               | CIP, CIN impedance                 | Over the total operating voltage range  |                         | 240                 |                 | kΩ   |
| G <sub>ERR</sub>                              | Current channel gain error         |   |                         | ±10                 |                 | %    |
| I <sub>ILV</sub>                              | Voltage channel leakage current    | V <sub>CC</sub> = 5.3 V, f <sub>CLK</sub> = 1.049 MHz   | -1                      |                     | 1               | μA   |
| I <sub>ILI</sub>                              | Current channel leakage current    |   | -1                      |                     | 1               |      |
|   |                                    | Input enabled   | -10                     |                     | 10              |      |
| <b>Digital I/O (CLK, DAT, DATn, MS0, MS1)</b> |                                    |   |                         |                     |                 |      |
| V <sub>IH</sub>                               | Input high voltage                 |   | 0.75<br>V <sub>CC</sub> |                     | 5.3             | V    |
| V <sub>IL</sub>                               | Input low voltage                  |   | -0.3                    |                     | 0.25V<br>CC     | V    |

**Table 5. General operating conditions (continued)**

| Symbol                           | Parameter               | Test conditions   | Min.         | Typ. | Max.  | Unit                    |
|----------------------------------|-------------------------|---|--------------|------|-------|-------------------------|
| $V_{OH}$                         | Output high voltage     | $I_O=-1\text{ mA}$ , $C_L=50\text{ pF}$ , $V_{CC}=3.2\text{ V}$ | $V_{CC}-0.4$ |      |       | V                       |
| $V_{OL}$                         | Output low voltage      | $I_O=+1\text{ mA}$ , $C_L=50\text{ pF}$ , $V_{CC}=3.2\text{ V}$ |              |      | 0.4   | V                       |
| $I_{UP}$                         | Pull up current         |   |              | 15   |       | $\mu\text{A}$           |
| $t_{TR}$                         | Transition time         | $C_{LOAD}=50\text{ pF}$   |              | 10   |       | ns                      |
| $t_L$                            | Latency                 | From 50 % of CLK to 50 % to DAT                                 |              | 40   |       | ns                      |
| <b>Clock input</b>               |                         |   |              |      |       |                         |
| $f_{CLK}$                        | Nominal frequencies     | Low precision   | 1.0          |      | 1.228 | MHz                     |
|                                  |                         | High precision  | 2.0          |      | 2.458 | MHz                     |
| <b>On chip reference voltage</b> |                         |   |              |      |       |                         |
| $V_{REF}$                        | Reference voltage       |   | 1.21         | 1.23 | 1.25  | V                       |
| $T_C$                            | Temperature coefficient | After calibration   |              | 30   | 50    | ppm/ $^{\circ}\text{C}$ |

**Figure 3. Timing diagram**



CLK - clock signal on CLK pin

CLK<sub>sample</sub> - sigma-delta sample frequency

bsV - sigma-delta bitstream of voltage signal

bsC - sigma-delta bitstream of current signal

DATA - multiplexed data of voltage and current signal on DAT pin



## 5 Application

The choice of external components in the transduction section of the application is a crucial point in the application design, affecting the precision and the resolution of the whole system.

Among the several considerations, a compromise must be found between the following needs:

1. Maximize the signal to noise ratio in the voltage and current channel
2. Choose the current to voltage conversion ratio  $K_s$  and the voltage divider ratio in a way that calibration can be achieved (see also the AN2299; *Fast digital calibration procedure for STPM01 based energy meters*, application note)
3. Choose  $K_s$  to take advantage of the whole current dynamic range according to desired maximum current and resolution.

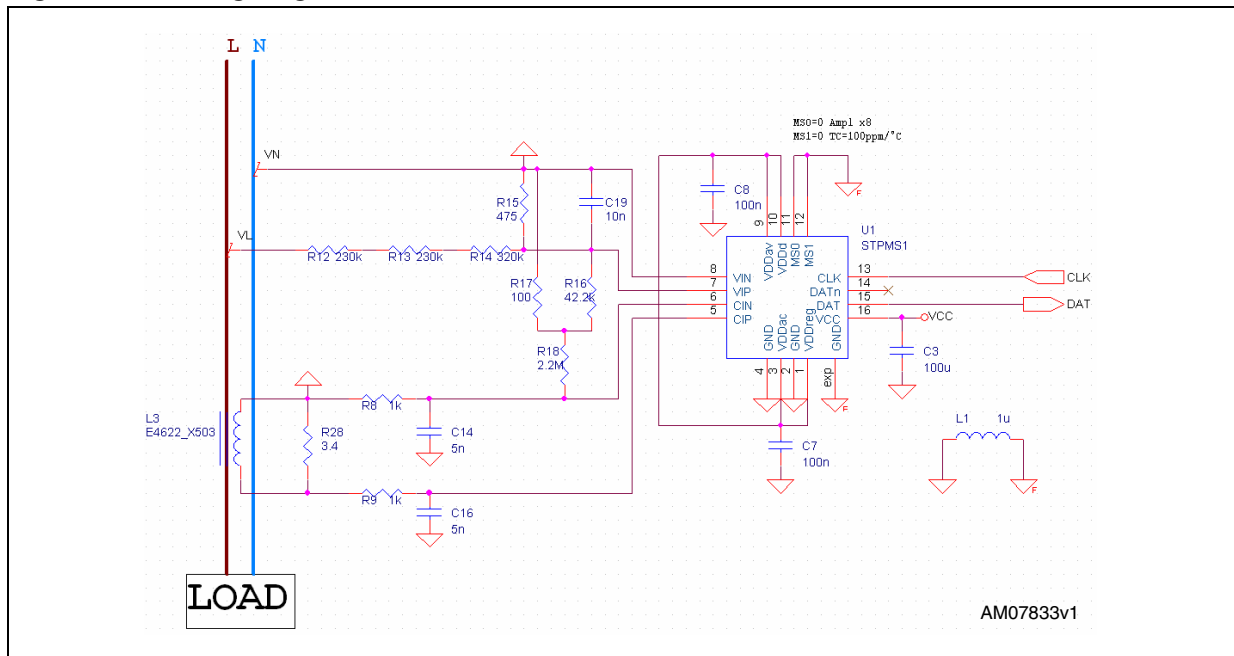
To maximize the signal to noise ratio of the current channel the voltage divider resistors ratio should be as close as possible to that shown in [Table 6](#).

[Figure 4](#) below shows a reference schematic for an application with the following properties:

- $P = 64000 \text{ imp/kWh}$
- $INOM = 5 \text{ A}$
- $IMAX = 60 \text{ A}$

Typical values for the current sensors sensitivity are indicated in [Table 6](#).

**Figure 4. Timing diagram**



**Table 6. Suggested external components in metering applications**

| Function               | Component        | Description                         | Value  | Tolerance |                            | Unit |
|------------------------|------------------|-------------------------------------|--------|-----------|----------------------------|------|
|                        | Calculator       | STPMC1                              | ---    | ---       | ---                        | ---  |
| Line voltage interface | Resistor divider | R to R ratio $V_{RMS}=230\text{ V}$ | 1:1650 | $\pm 1\%$ | 50 ppm/ $^{\circ}\text{C}$ | V/V  |
|                        |                  | R to R ratio $V_{RMS}=110\text{ V}$ | 1:830  |           |                            |      |
| Line current interface | Rogowski coil    | Current to voltage ratio $K_S$      | 0.15   | $\pm 5\%$ | 50 ppm/ $^{\circ}\text{C}$ | mV/A |
|                        | CT               |                                     | 1.7    | $\pm 5\%$ |                            |      |
|                        | Shunt            |                                     | 0.43   | $\pm 5\%$ |                            |      |

*Note: The above listed components refer to typical metering applications. However, STPMS1 operation is not limited to the choice of these external components.*

**Figure 5. Simplified application schematics for STPMC1 based energy metering**

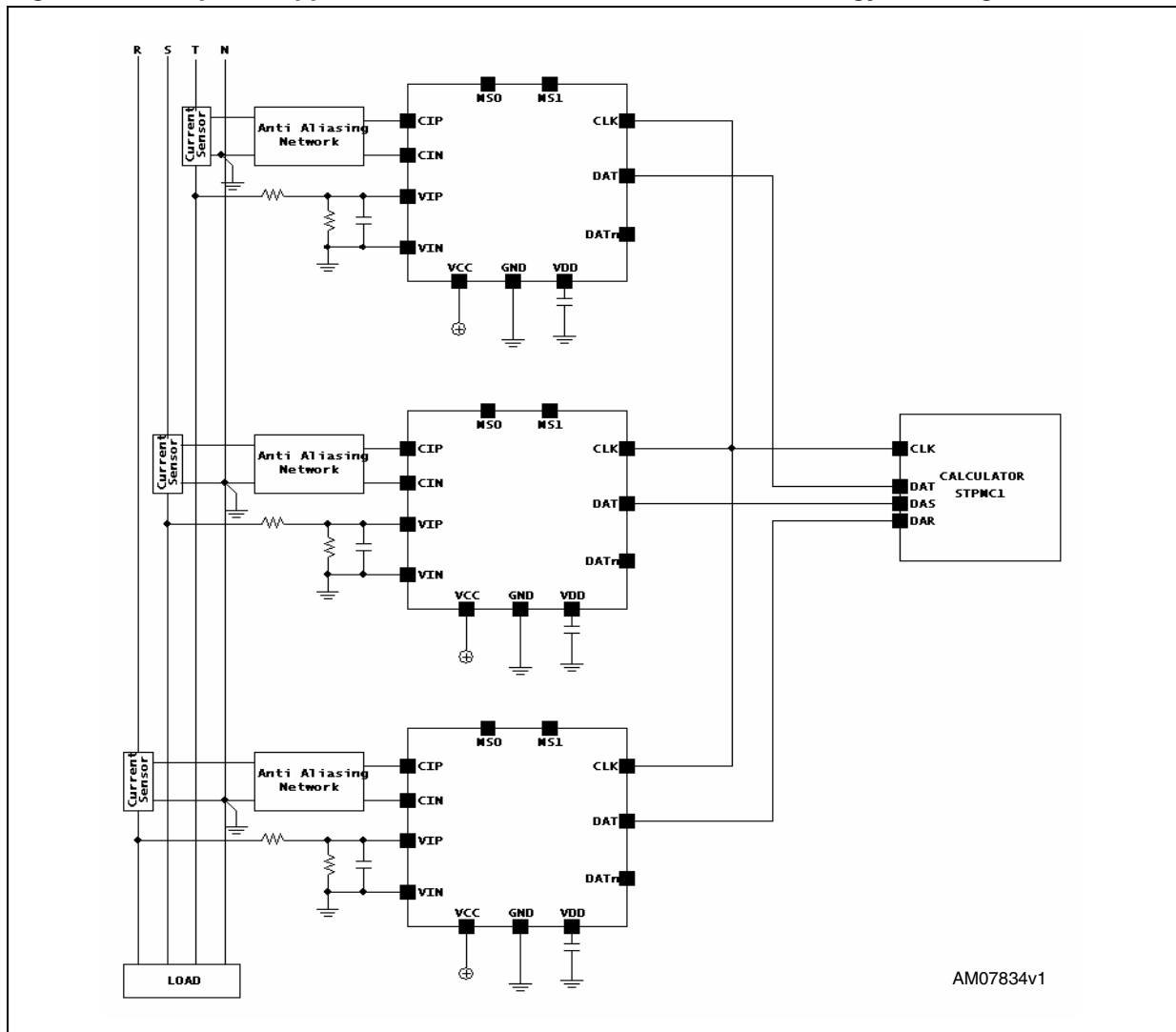
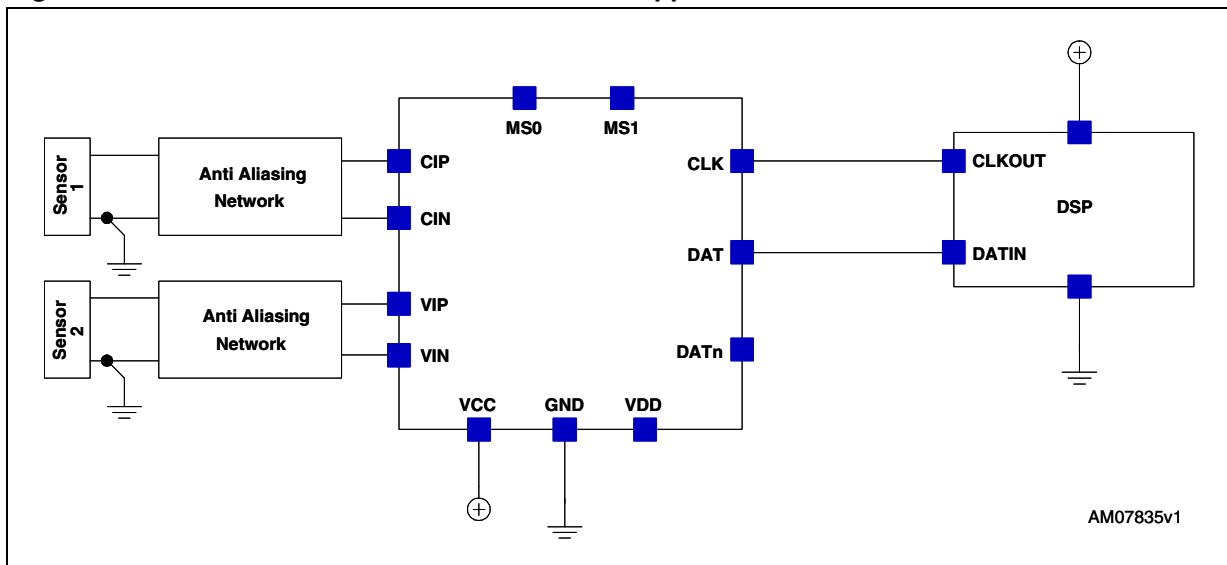


Figure 6. Connection schematic for DSP based applications



## 6 Terminology

### 6.1 Conventions

The lowest analog and digital power supply voltage is named GND which represents the system Ground. All voltage specifications for digital input/output pins are referred to GND.

Positive currents flow into a pin. Sinking current means that the current is flowing into the pin and then it is positive. Sourcing current means that the current is flowing out of the pin and then it is negative.

Timing specifications of a signal treated by a digital control part are relative to CLK. This signal is provided from the STPMC1 calculator IC of 1.024 MHz or of 2.048 MHz nominal frequency.

A positive logic convention is used in all equations.

### 6.2 Notation

Current and voltage signals are represented as  $u$  and  $i$ .

# 7 Typical performance characteristics

Figure 7. SNRH of CIP-CIN channel, gain 32x

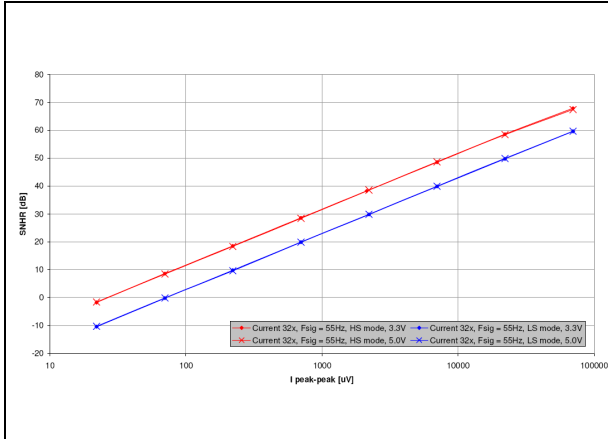


Figure 8. SNHR of CIP-CIN channel, gain 8x

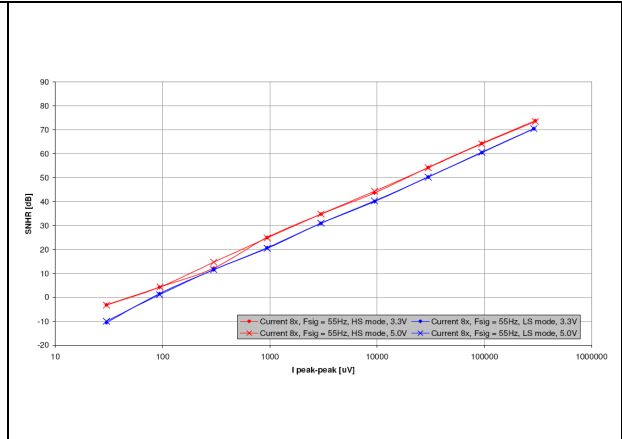


Figure 9. SNHR of VIP-VIN channel

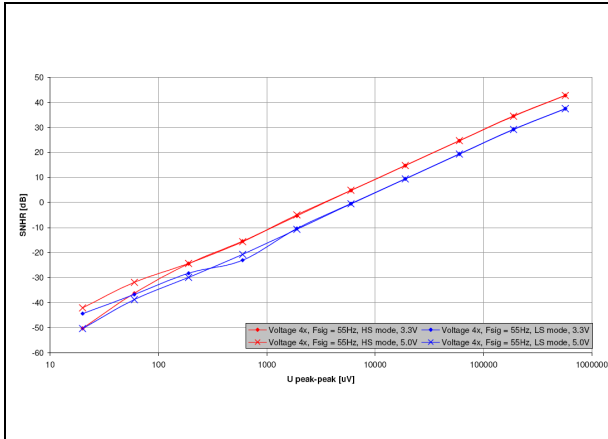


Figure 10. SINAD of CIP-CIN channel, gain 32x

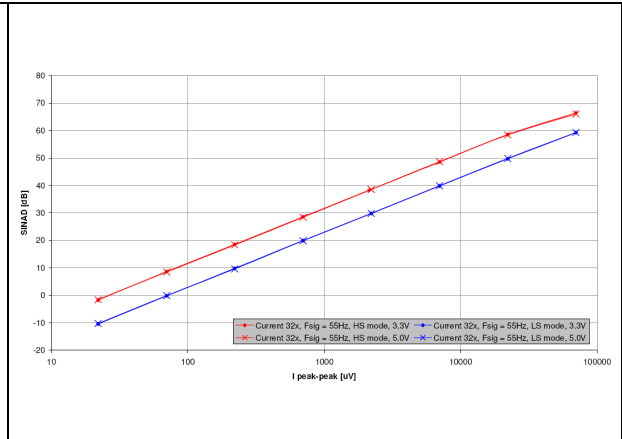


Figure 11. SINAD of CIP-CIN channel, gain 8x

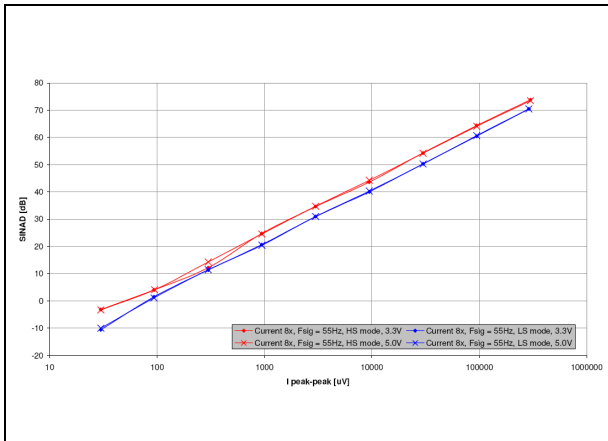


Figure 12. SINAD of VIP-VIN channel

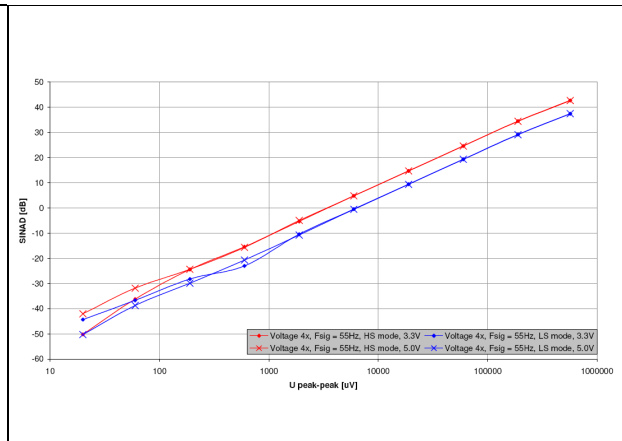


Figure 13. Relative gain error of CIP-CIN channel, gain 32x

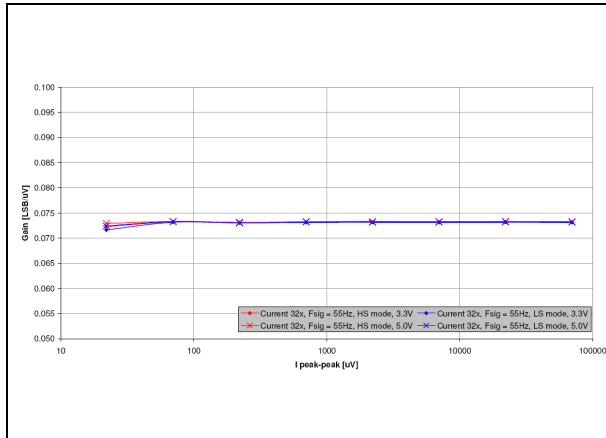


Figure 14. Relative gain error of CIP-CIN channel, gain 8x

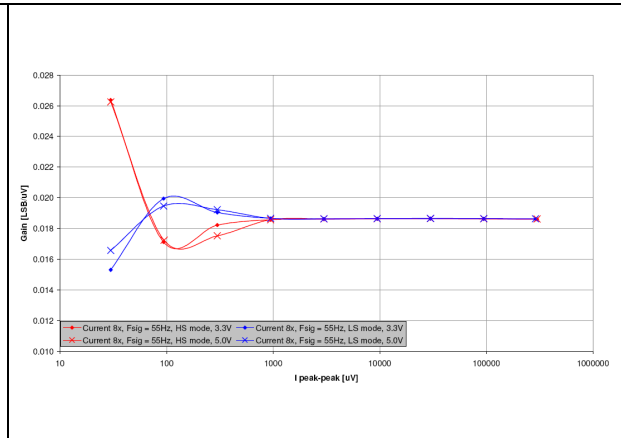


Figure 15. Relative gain error of VIP-VIN channel

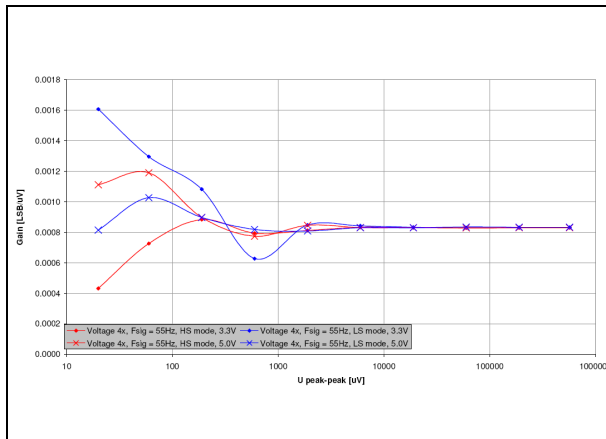
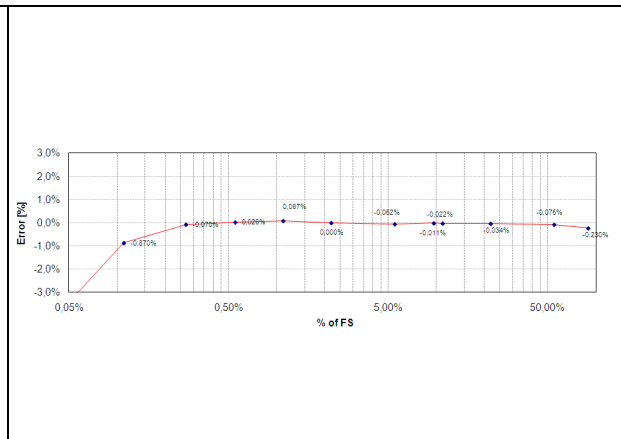


Figure 16. Accuracy over dynamic range



## 8 Theory of operation

### 8.1 General operation description

The STPMS1 performs first-order analog modulation of signals which have frequencies varying from DC to 2 kHz on two independent channels in parallel. There is a current channel for measuring line current and a voltage channel for measuring line voltage. The outputs of the converters provide two streams of digital ones and zeros which are therefore multiplexed in time to reduce the number of external connections.

The sampling and the data multiplexing are driven by an external clock signal, as it is used to strobe the analog inputs. The combination of one or more STPMS1s and an STPMC1 (which implements the digital filtering) constitutes a conversion system for energy metering applications.

The STPMS1 can also be used along with a DSP programmed to demultiplex the output bitstream and to implement the digital filtering as a medium resolution ADC system.

When used in energy metering applications, the voltage channel is connected externally and differentially to a line voltage divider which provides an analog signal proportional to the voltage  $u$ . The current channel is connected to a Rogowski coil, or to a current transformer (CT) or a shunt, which are used to interface the line current. The Rogowski coil provides an analog signal proportional to  $di/dt$ , while the shunt or CT provides an analog signal proportional to the current  $i$ . A CT differs from a shunt in sensitivity and phase error. There should be an anti-aliasing LP filter inserted between the sensors and the inputs of both channels of the STPMS1.

Internally, the differential voltage input related to the voltage channel is connected directly to the A/D converter, which implies an amplification of  $\times 4$ . On the other side, the differential voltage input related to the current channel is connected first to a configurable  $\times 2$  or  $\times 8$  pre-amplifier and the output of this pre-amplifier to the similar A/D converter ( $\times 4$  gain), which implies selectable pre-amplification of  $\times 8$  or  $\times 32$  and uses the same reference voltage.

A pair of digital inputs (MS0 and MS1) is used to configure the device.

### 8.2 Function description of the analog part

The supply pins for the analog part are  $V_{CC}$ ,  $V_{DD}$ ,  $V_{DDac}$ ,  $V_{DDav}$ ,  $V_{DDd}$ , and GND.

The GND pin also represents a reference point. The  $V_{DD}$  is an analog I/O pin of an internal +3.0 V low-drop voltage regulator, the  $V_{DDac}$  and  $V_{CCav}$  are the modulators supply inputs, while the  $V_{DDd}$  is the digital front-end supply input. A 100 nF capacitor should be connected between  $V_{DDxx}$  and GND. The input of the mentioned regulator is  $V_{CC}$  which powers also a band-gap, and bias generators.

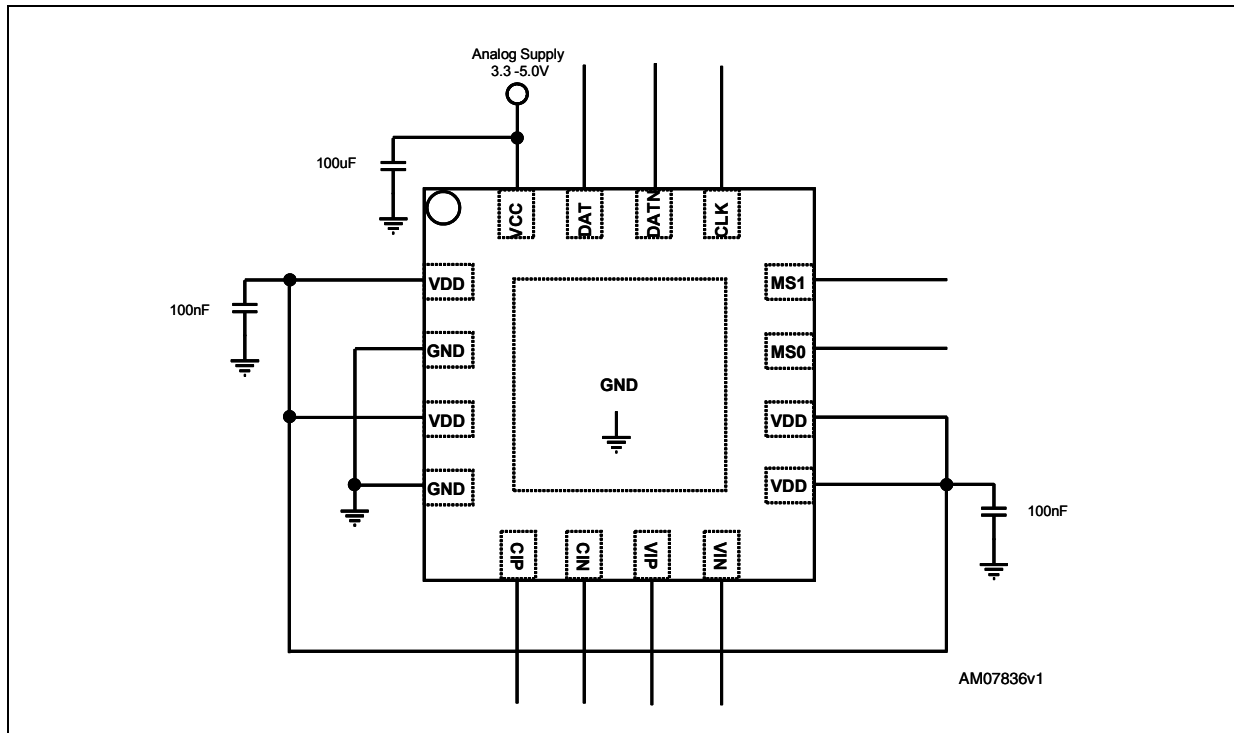
The analog part consists of several modules:

- Band-gap reference and bias generators
- +3 V low-drop regulator
- two DC buffer amplifiers
- two  $\Sigma\Delta$  AD converters
- control signal module

The band-gap voltage reference is used as the reference level source for the low-drop module and for the AD converters. This module produces several bias currents and voltages for all other analog modules.

The low-drop regulator generates the +3.0 V power supply level. This level is used to power the DC buffers, pre-amplifier, and AD converter pair in the analog part of the device and whole digital part. It is brought out as  $V_{DD}$  for external connections. As part of low-drop, there is a power on reset (POR) detection circuit, which blocks all functions of the STPMS1 by asserting the reset condition whenever a  $V_{CC}$  supply level is less than +2.5 V.

Figure 17. Power supply external connection scheme



In order to enable proper operation of the switched capacitor (SC) section of AD converters, two DC buffers are added to the device. One is buffering the voltage reference level and the other is buffering the level of value equal to  $(V_{DD}-V_{SS})/2$ .

The AD converter block is further split into a voltage and current channel. Each channel consists of a differential pre-amplifier, SC integrator, comparator, amplifier bias block, and all necessary switches. The voltage channel SC integrator has a gain of 2 and there is no pre-amplifier block. The current channel SC integrator has a gain of 2 or 8, which can be selected by MS0 input, and has a pre-amplifier with a gain of 4.

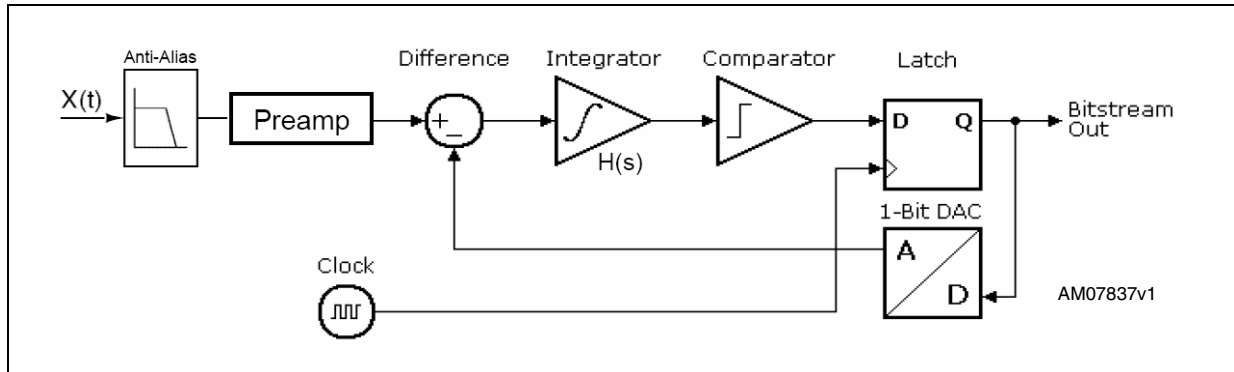
The amplitude of the input signal to the AD converter block must be kept less than  $0.45 V_{ref}$ .

The output of each channel is input to the digital module as  $\Sigma\Delta$  stream.

For the operation of the analog part, a set of five clock signals is provided from the digital module. These signals derive from the CLK signal. Two of them are used to run the conversion, the next one is used as the chopper signal for the voltage channel and the last two are used as chopper signals for the current channel. All these signals are connected to the control signal module, which consists of standard digital cells powered from an analog supply. It produces all the necessary signals and switch controls of the AD converters.



Figure 18. Block diagram of the modulator



### 8.3 Functional description of the digital part

A digital part is made up of:

- clock generator
- mode decoder
- time multiplex

The clock generator produces all five clocks for the analog module.

The mode decoder generates signals for controlling the temperature coefficient of the on-chip band-gap voltage reference and the amplification factor of the current channel, clock prescaler, and voltage channel enable.

Table 7. Modes of operation

| MS0 | Mode | Description |
|-----|------|-------------|
| 0   | 0    | ampl = 8    |
| 1   | 1    | ampl = 32   |

Table 8. Changing of band-gap voltage reference

| MS1  | Mode | Description     |
|------|------|-----------------|
| 0    | 0    | TC = 100 ppm/°C |
| CLK  | 1    | TC = 170 ppm/°C |
| NCLK | 2    | TC = 125 ppm/°C |
| 1    | 3    | TC = 190 ppm/°C |

The multiplex combines both  $\Sigma\Delta$  input signals for the analog module into one signal DAT which drives differential outputs DAT and DATn according to:

DAT= if CLK then bsV or else bsC

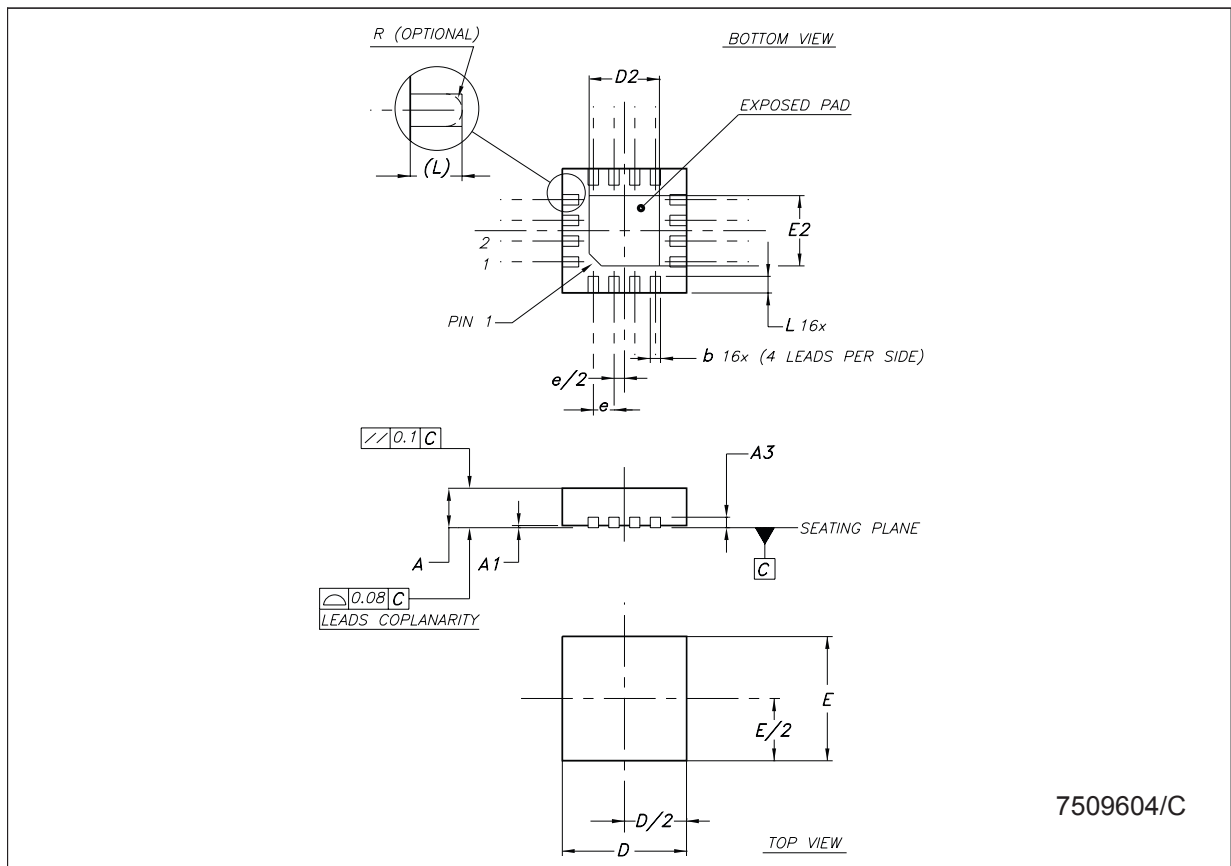
DATN = NOT(DAT).

## 9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at [www.st.com](http://www.st.com). ECOPACK is an ST registered trademark.

**QFN16 (3 x 3 mm.) mechanical data**

| Dim. | mm.  |      |      | inch. |       |       |
|------|------|------|------|-------|-------|-------|
|      | Min. | Typ. | Max. | Min.  | Typ.  | Max.  |
| A    | 0.80 | 0.90 | 1.00 | 0.031 | 0.035 | 0.039 |
| A1   | 0    |      | 0.05 |       |       | 0.002 |
| A3   |      | 0.20 |      |       | 0.008 |       |
| b    | 0.18 |      | 0.30 | 0.007 |       | 0.012 |
| D    | 2.90 | 3.00 | 3.10 | 0.114 | 0.118 | 0.122 |
| D2   | 1.50 |      | 1.80 | 0.059 |       | 0.071 |
| E    |      | 3.00 |      |       | 0.118 |       |
| E2   | 2.90 | 3.00 | 3.10 | 0.114 | 0.118 | 0.122 |
| e    |      | 0.50 |      |       | 0.020 |       |
| L    | 0.30 |      | 0.50 | 0.012 |       | 0.020 |



**Tape & reel QFNxx/DFNxx (3 x 3 mm.) mechanical data**

| Dim. | mm.  |      |      | inch. |       |       |
|------|------|------|------|-------|-------|-------|
|      | Min. | Typ. | Max. | Min.  | Typ.  | Max.  |
| A    |      |      | 180  |       |       | 7.087 |
| C    | 12.8 |      | 13.2 | 0.504 |       | 0.519 |
| D    | 20.2 |      |      | 0.795 |       |       |
| N    | 60   |      |      | 2.362 |       |       |
| T    |      |      | 14.4 |       |       | 0.567 |
| Ao   |      | 3.3  |      |       | 0.130 |       |
| Bo   |      | 3.3  |      |       | 0.130 |       |
| Ko   |      | 1.1  |      |       | 0.043 |       |
| Po   |      | 4    |      |       | 0.157 |       |
| P    |      | 8    |      |       | 0.315 |       |

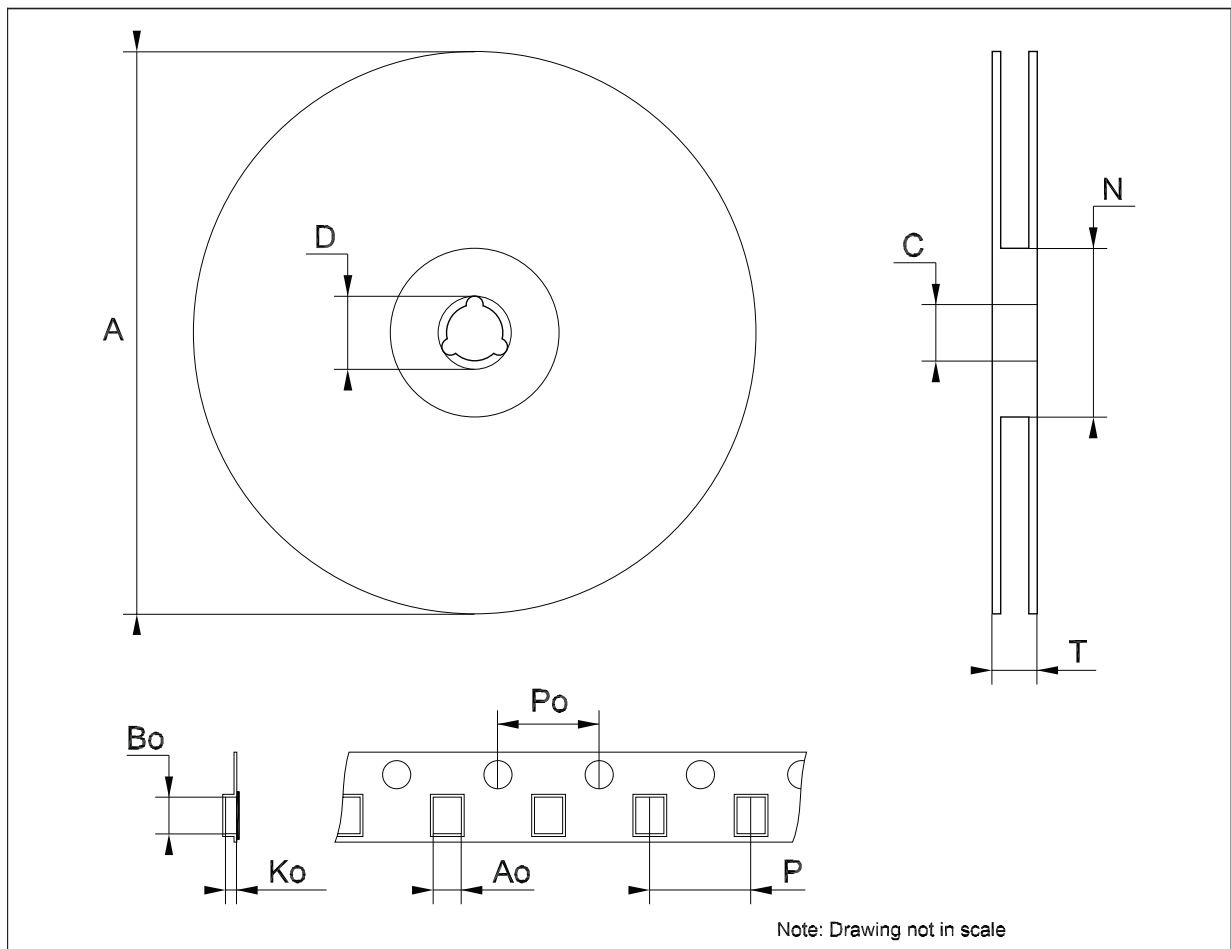
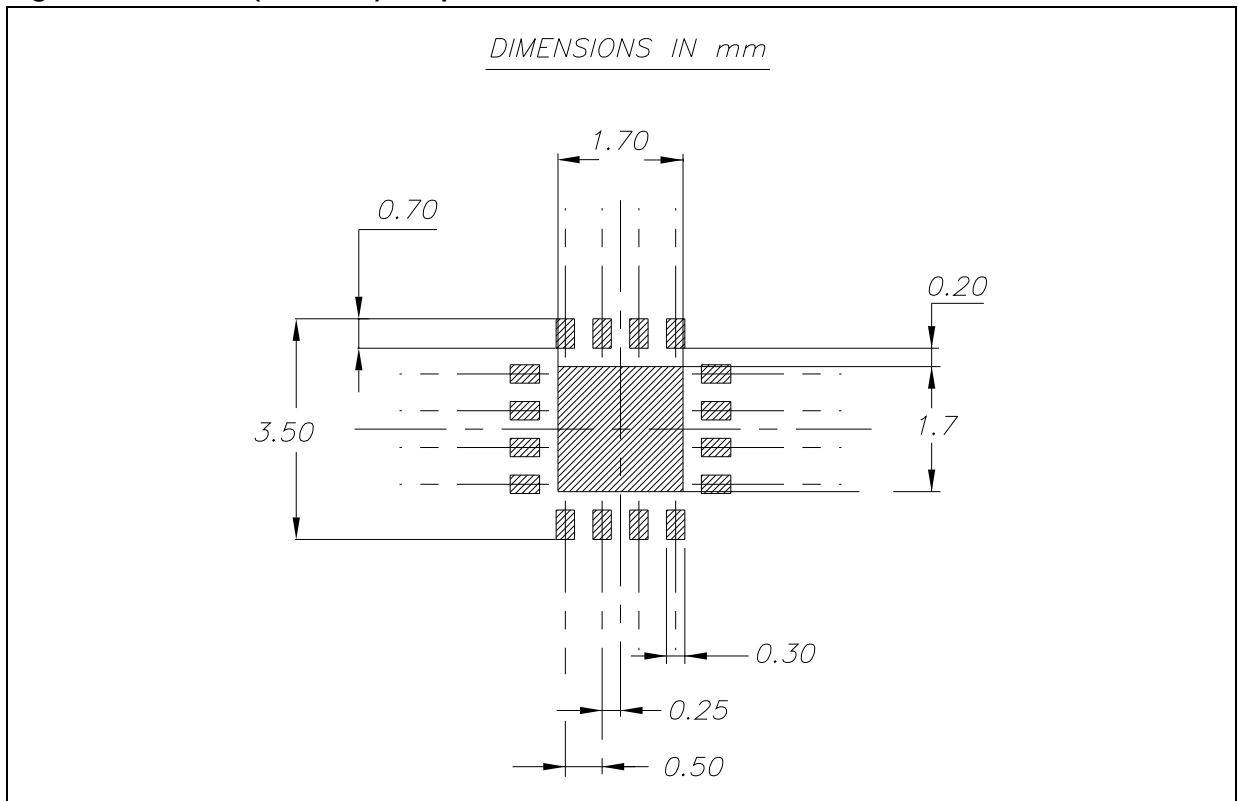


Figure 19. QFN16 (3 x 3 mm) footprint recommended data



## 10 Revision history

**Table 9. Document revision history**

| Date        | Revision | Changes  |
|-------------|----------|--|
| 23-Oct-2009 | 1        | Initial release.                               |
| 07-Oct-2010 | 2        | Data brief header removed from the cover page. |

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