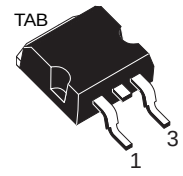
STB18NF30

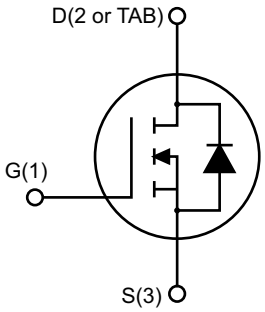
Automotive-grade N-channel 330 V, 160 mΩ typ., 18 A STripFET™ II Power MOSFET in a D²PAK package

Datasheet - production data



D²PAK

Figure 1. Internal schematic diagram



Features

Order code	V_{DSS}	$R_{DS(on)}$ max.	I_D
STB18NF30	330 V	180 mΩ	18 A

- Designed for automotive applications and AEC-Q101 qualified
- 100% avalanche tested
- 175 °C junction temperature

Applications

- Switching applications

Description

This Power MOSFET has been developed using STMicroelectronics' unique STripFET process, which is specifically designed to minimize input capacitance and gate charge. This renders the device suitable for use as primary switch in advanced high-efficiency isolated DC-DC converters for telecom and computer applications, and applications with low gate charge driving requirements.

Table 1. Device summary

Order code	Marking	Package	Packaging
STB18NF30	18NF30	D²PAK	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	330	V
V_{GS}	Gate-source voltage	±20	V
I_D(1)	Drain current (continuous) at T_C = 25 °C	18	A
	Drain current (continuous) at T_C = 100 °C	12	A
I_{DM}(2)	Drain current (pulsed)	72	A
P_{TOT}	Total dissipation at T_C = 25 °C	150	W
dv/dt(3)	Peak diode recovery voltage slope	10	V/ns
T_{stg}	Storage temperature	-55 to 175	°C
T_J	Operating junction temperature		

1. The value is rated according to $R_{thj\text{-}c}$.
2. Pulse is rated according to SOA.
3. $I_{SD} \leq 18$ A, di/dt $\leq$ 200 A/µs, $V_{DD} \leq 80\%V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	1	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb	30	

1. When mounted on 1 inch² FR-4, 2 Oz copper board.

Table 4. Avalanche data

Symbol	Parameter	Value	Unit
I_{AV}	Non-repetitive avalanche current	14	A
E_{AS}	Single pulse avalanche energy (starting T_J=25 °C, I_D=I_{AV}, V_{DD}=50 V)	200	mJ

2 Electrical characteristics

(T_{CASE}=25 °C unless otherwise specified).

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D=1 mA, V_{GS}=0	330	-		V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS}=330 V		-	1	µA
		V_{DS}=330 V,Tc=125 °C			50	µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS}=±20 V		-	±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}=V_{GS}, I_D= 250 µA	2	-	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS}=10 V, I_D=9 A		160	180	mΩ

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS}=25 V, f=1 MHz, V_{GS}=0 V	-	1650	-	pF
C_{oss}	Output capacitance		-	220		pF
C_{rss}	Reverse transfer capacitance		-	30		pF
Q_g	Total gate charge	V_{DD}=264 V, I_D=18 A, V_{GS}=10 V (see *Figure 14*)	-	44	-	nC
Q_{gs}	Gate-source charge		-	7	-	nC
Q_{gd}	Gate-drain charge		-	17	-	nC

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD}=165 V, I_D= 9 A, R_G= 4.70 Ω, V_{GS}=10 V (see *Figure 13*)	-	20	-	ns
t_r	Rise time		-	18	-	ns
$t_{d(off)}$	Turn-off delay time		-	145	-	ns
t_f	Fall time		-	45	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		18	A
I_{SDM}	Source-drain current (pulsed)		-		72	A
V_{SD}	Forward on voltage	I_{SD}=18 A, V_{GS}=0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD}=18 A, di/dt=100 A/µs, V_{DD}=100 V (see *Figure 15*)	-	180	400	ns
Q_{rr}	Reverse recovery charge		-	1.5		µC
I_{RRM}	Reverse recovery current		-	16		A
t_{rr}	Reverse recovery time	I_{SD}=18 A, di/dt=100 A/µs, V_{DD}=100 V, Tj=150 °C (see *Figure 15*)	-	210		ns
Q_{rr}	Reverse recovery charge		-	1.9		µC
I_{RRM}	Reverse recovery current		-	19		A

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

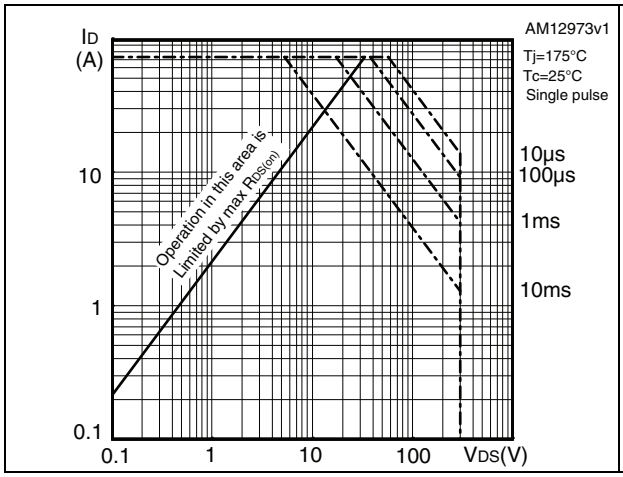


Figure 3. Thermal impedance

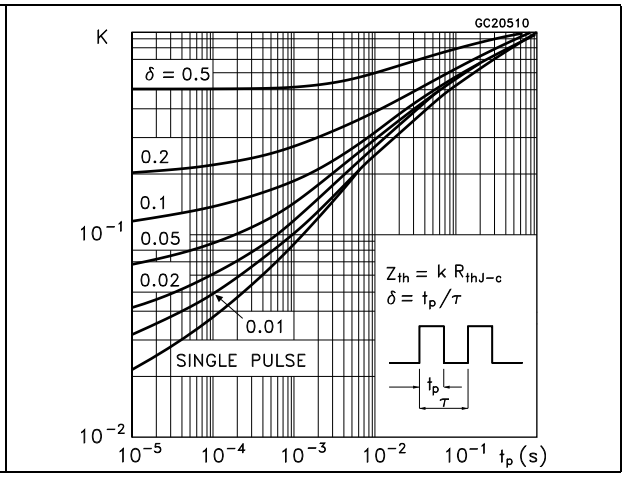


Figure 4. Output characteristics

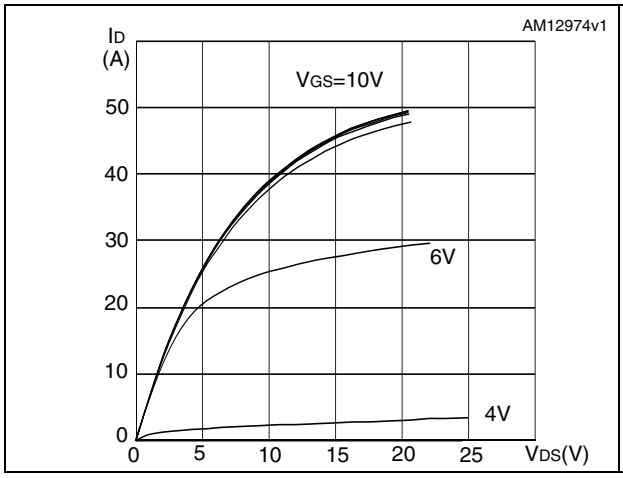


Figure 5. Transfer characteristics

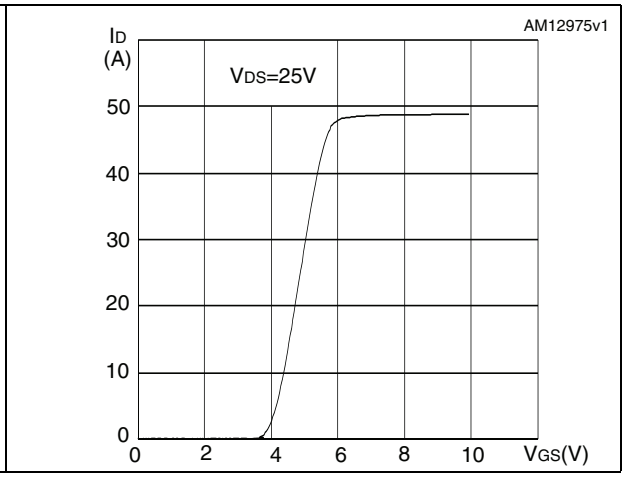


Figure 6. Normalized B_{VDSS} vs temperature

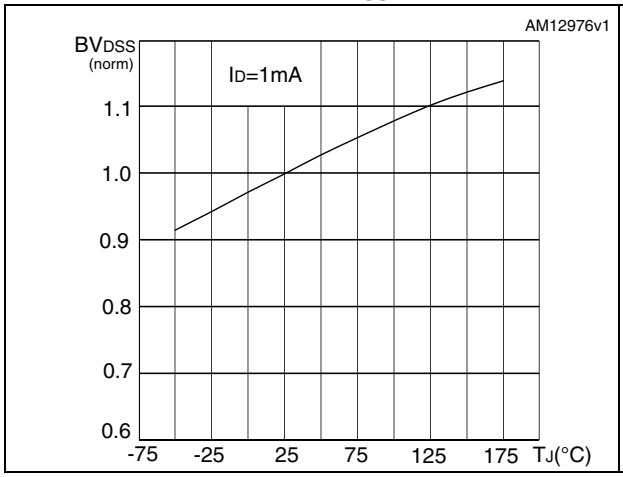


Figure 7. Static drain-source on-resistance

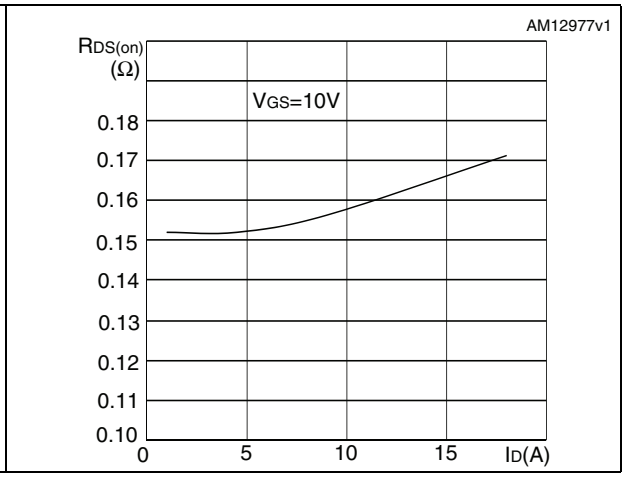


Figure 8. Gate charge vs gate-source voltage

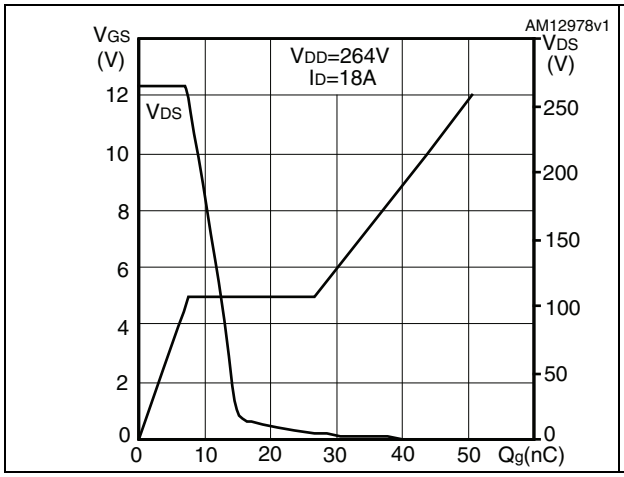


Figure 9. Capacitance variations

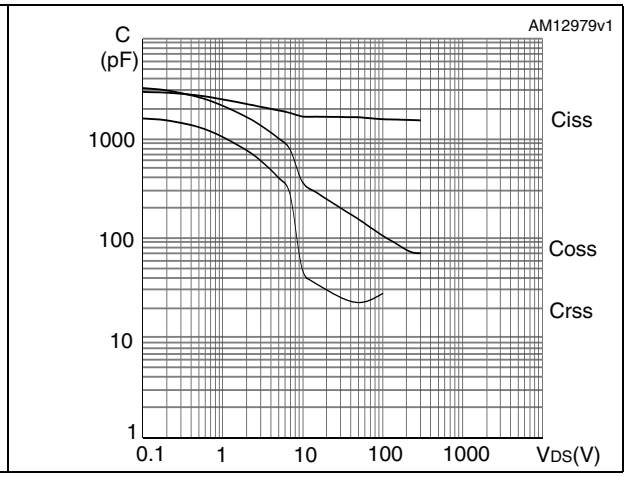


Figure 10. Normalized gate threshold voltage vs temperature

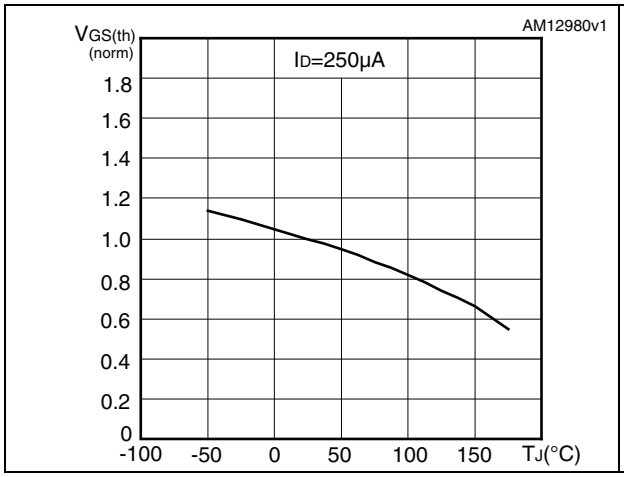


Figure 11. Normalized on-resistance vs temperature

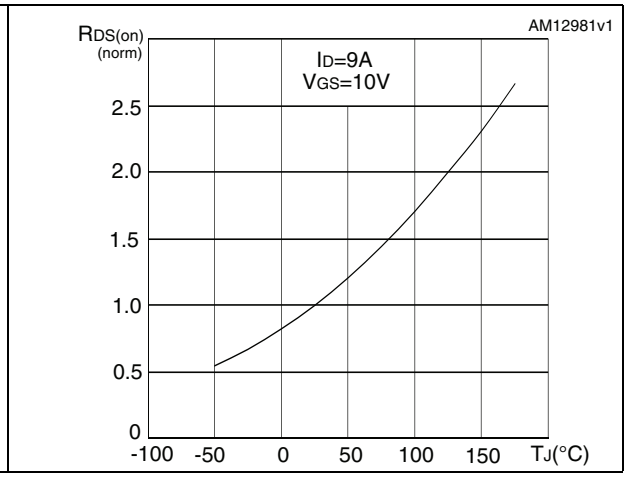
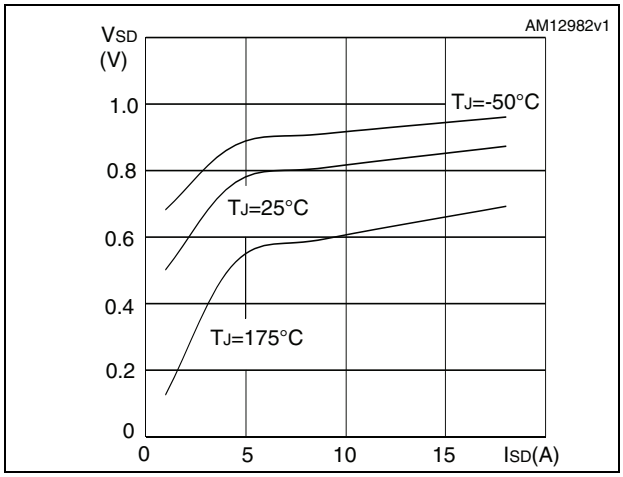


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

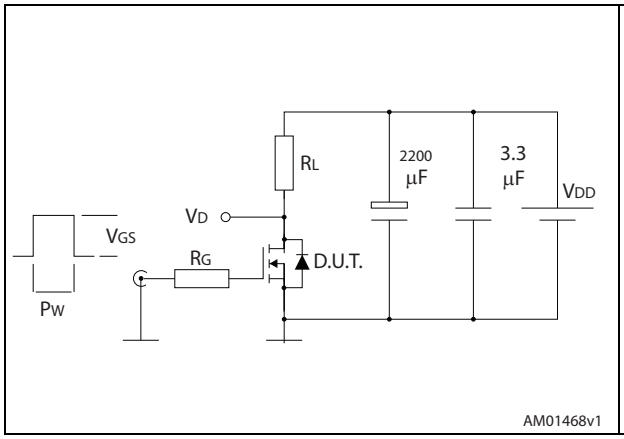


Figure 14. Gate charge test circuit

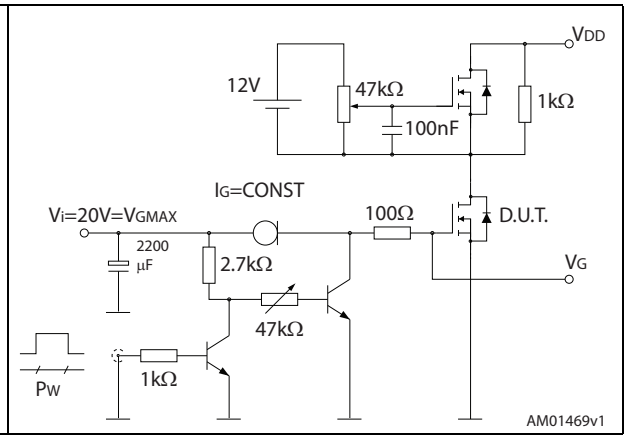


Figure 15. Test circuit for inductive load switching and diode recovery times

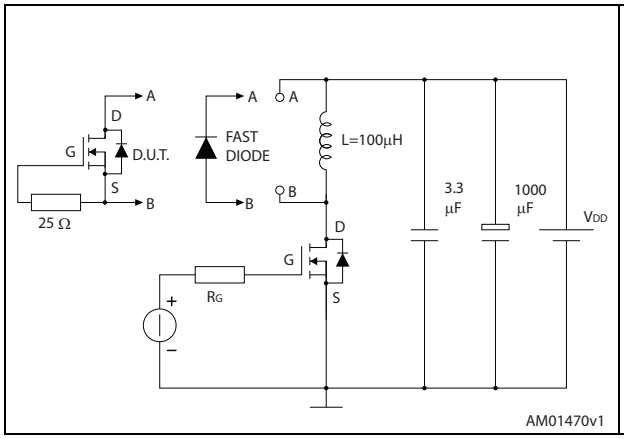


Figure 16. Unclamped inductive load test circuit

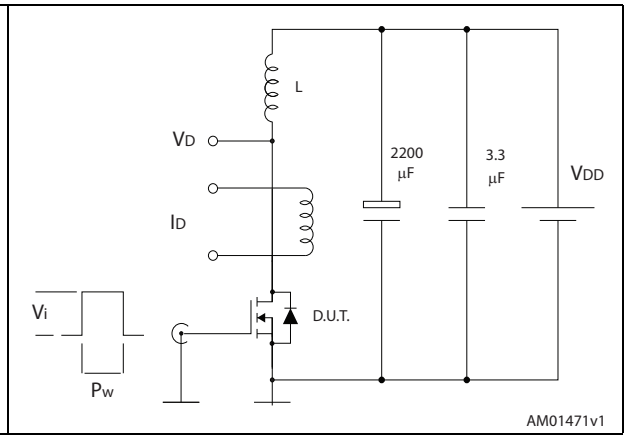


Figure 17. Unclamped inductive waveform

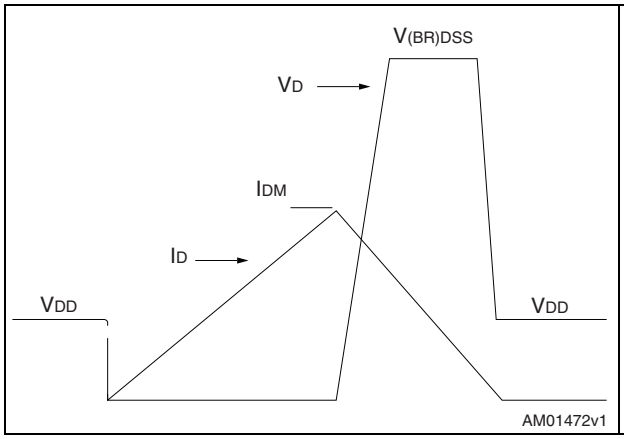
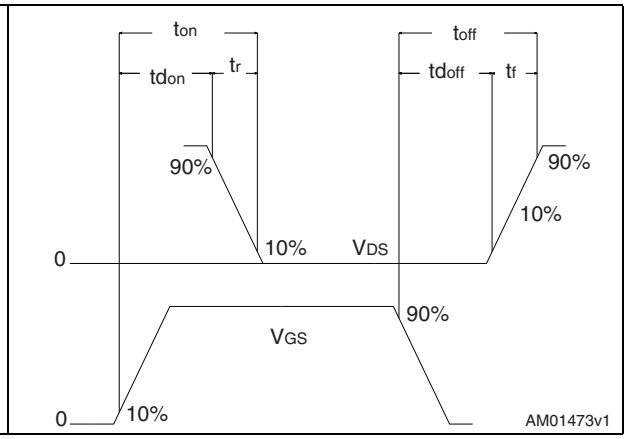


Figure 18. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.
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Table 9. D²PAK (TO-263) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50		
E	10		10.40
E1	8.50		
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 19. D²PAK (TO-263) drawing

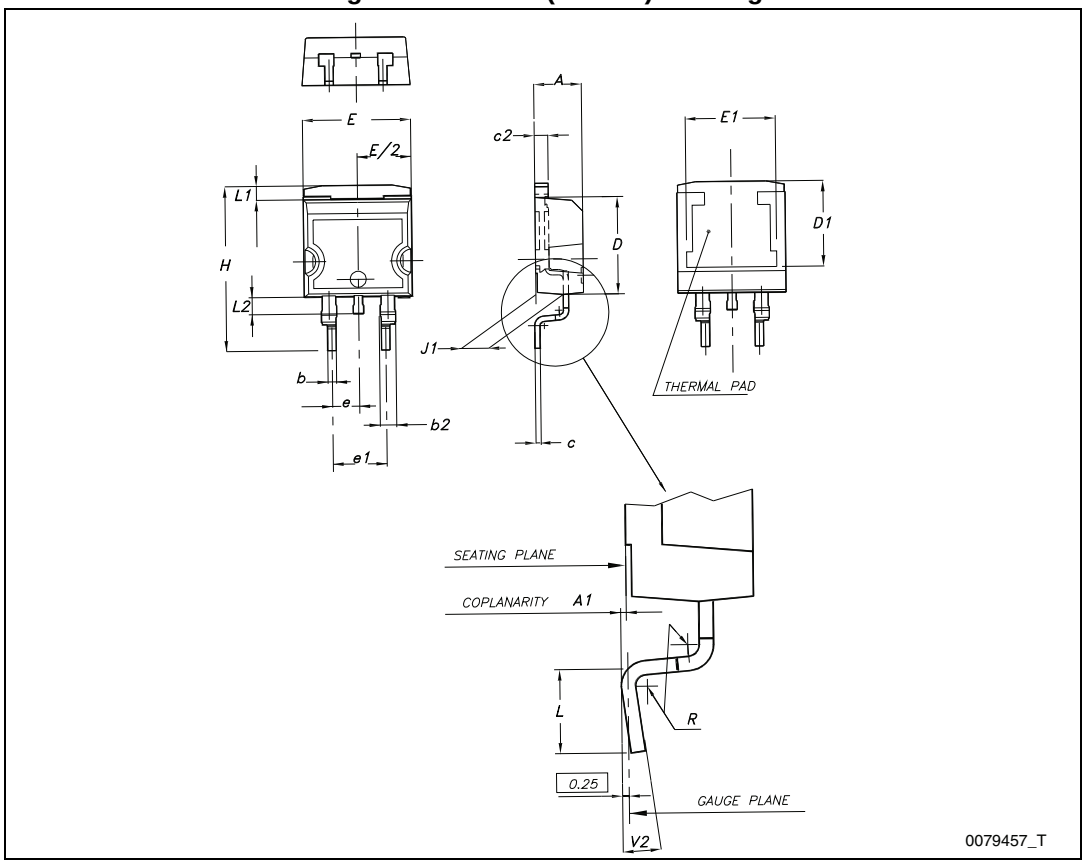
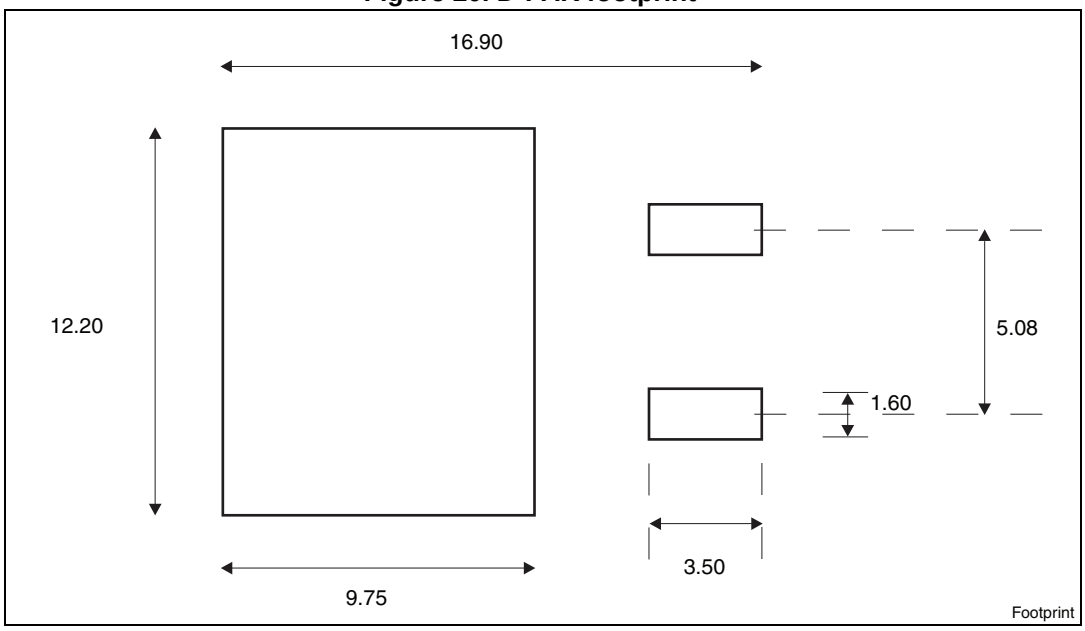


Figure 20. D²PAK footprint[a]



a. All dimension are in millimeters

5 Packaging mechanical data

Table 10. D²PAK (TO-263) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base qty		1000
P2	1.9	2.1	Bulk qty		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Figure 21. Tape

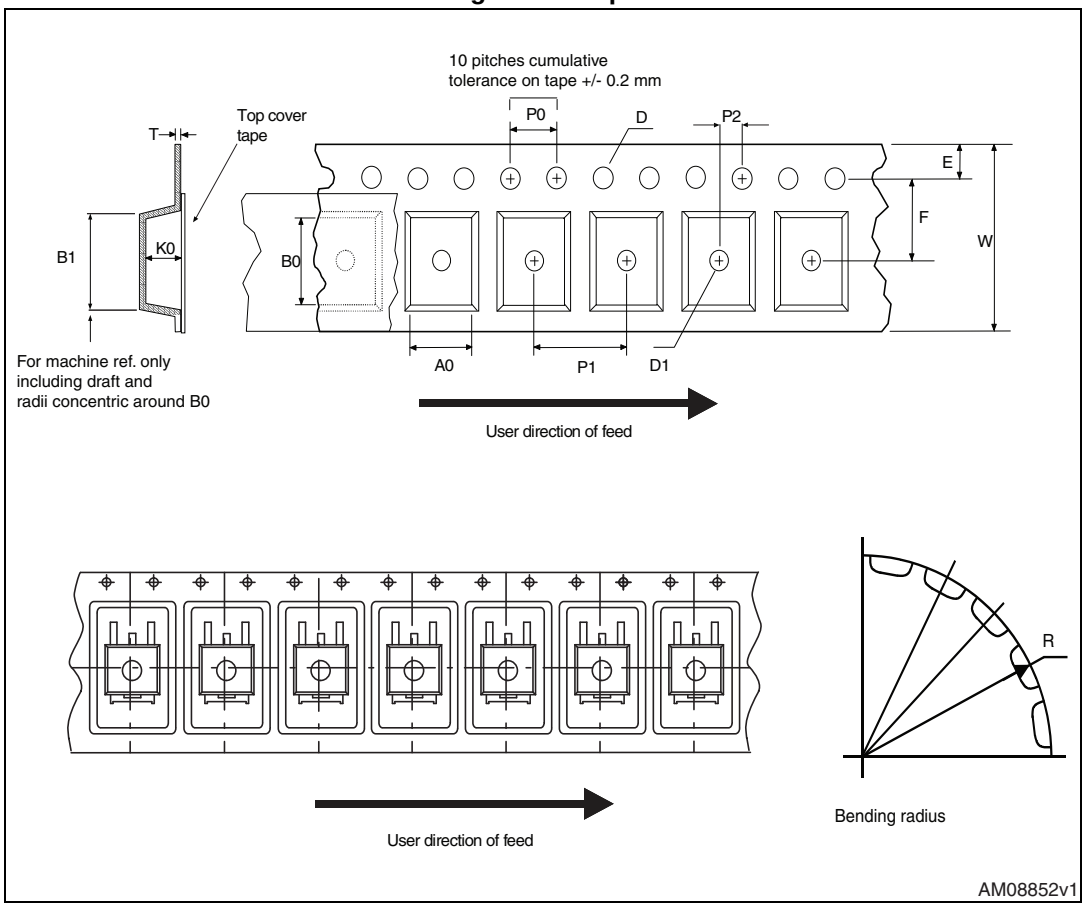
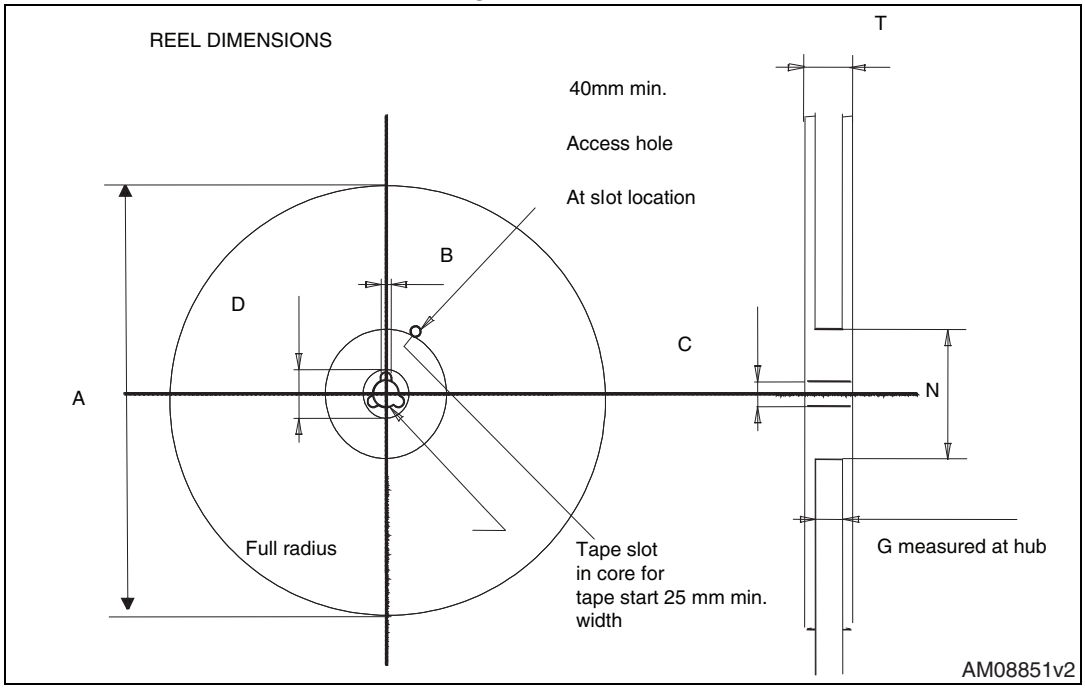


Figure 22. Reel



6 Revision history

Table 11. Document revision history

Date	Revision	Changes
13-Jan-2012	1	First release
23-May-2012	2	*Section 2.1: Electrical characteristics (curves)* has been added. Document status promoted from preliminary data to production data.
06-Aug-2013	3	– Updated: *Section 4: Package mechanical data* – Updated: *Figure 13*, *14*, *15* and *16* – Added: dv/dt in *Table 2* – Minor text changes

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