

Description

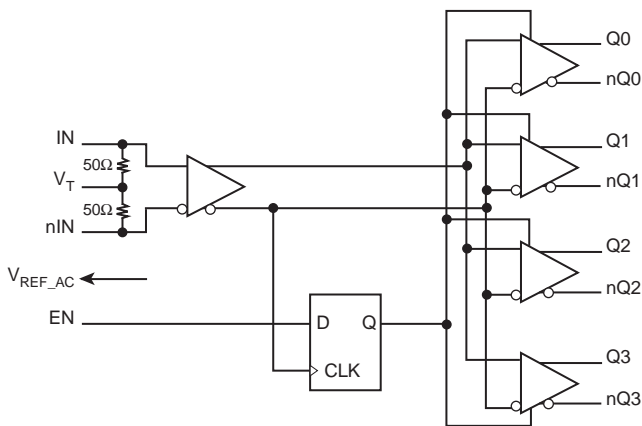
The 8S89832I is a high speed 1-to-4 Differential-to-LVDS Fanout Buffer. The 8S89832I is optimized for high speed and very low output skew, making it suitable for use in demanding applications such as SONET, 1 Gigabit and 10 Gigabit Ethernet, and Fibre Channel. The internally terminated differential input and V_{REF_AC} pin allow other differential signal families such as LVPECL, LVDS, and SSTL to be easily interfaced to the input with minimal use of external components. The device also has an output enable pin that may be useful for system test and debug purposes.

The 8S89832I is packaged in a small 3mm x 3mm 16-pin VFQFN package which makes it ideal for use in space-constrained applications.

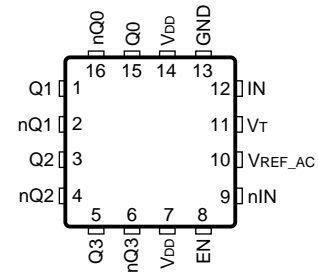
Features

- Four differential LVDS output pairs
- IN, nIN input pairs can accept the following differential input levels: LVPECL, LVDS, SSTL
- 50Ω internal input termination to V_T
- Maximum output frequency: 2GHz
- Output skew: 25ps (maximum)
- Part-to-part skew: 200ps (maximum)
- Propagation delay: 550ps (maximum)
- Additive phase jitter, RMS: 0.09ps (typical)
- Full 2.5V supply mode
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment



8S89832I
16-Lead VFQFN
3mm x 3mm x 0.925mm package body
K Package
Top View

Table 1. Pin Descriptions

| Number | Name | Type | | Description |
|--------|---------------------|--------|--------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1, 2 | Q1, nQ1 | Output | | Differential output pair. LVDS interface levels. |
| 3, 4 | Q2, nQ2 | Output | | Differential output pair. LVDS interface levels. |
| 5, 6 | Q3, nQ3 | Output | | Differential output pair. LVDS interface levels. |
| 7, 14 | V _{DD} | Power | | Positive supply pins. |
| 8 | EN | Input | Pullup | Synchronizing clock enable. When LOW, Qx outputs will go LOW and nQx outputs will go HIGH on the next LOW transition at IN inputs. Input threshold is V _{DD} /2V. Includes a 37kΩ pullup resistor. Default state is HIGH when left floating. The internal latch is clocked on the falling edge of the input signal IN. See Table 3A LVTTTL / LVCMOS interface levels. |
| 9 | nIN | Input | | Inverting differential clock input. 50Ω internal input termination to V _T . |
| 10 | V _{REF_AC} | Output | | Reference voltage for AC-coupled applications. |
| 11 | V _T | Input | | Termination input. |
| 12 | IN | Input | | Non-inverting differential clock input. 50Ω internal input termination to V _T . |
| 13 | GND | Power | | Power supply ground. |
| 15, 16 | Q0, nQ0 | Output | | Differential output pair. LVDS interface levels. |

NOTE: *Pullup* refers to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

Table 2. Pin Characteristics

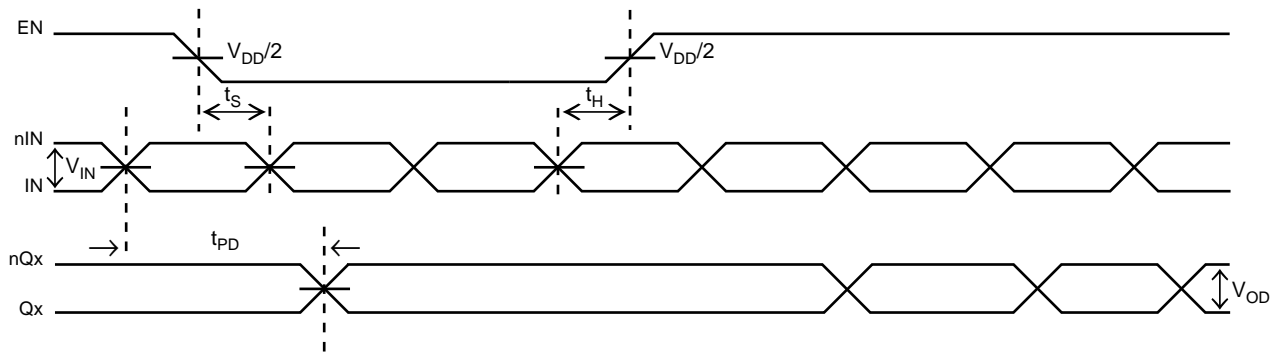
| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---------------------|-----------------------|-----------------|---------|---------|---------|-------|
| C _{IN} | Input Capacitance | | | 2 | | pF |
| R _{PULLUP} | Input Pullup Resistor | | | 37 | | kΩ |

Function Tables

Table 3A. Control Input Function Table

| Input | Outputs | |
|-------|---------------|----------------|
| EN | Q[0:3] | nQ[0:3] |
| 0 | Disabled; LOW | Disabled; HIGH |
| 1 | Enabled | Enabled |

NOTE: EN switches, the clock outputs are disabled or enabled following a falling input clock edge as shown in *Figure 1*.

Figure 1. EN Timing Diagram

Table 3B. Truth Table

| Inputs | | | Outputs | |
|--------|-----|----|------------|------------|
| IN | nIN | EN | Q[0:3] | nQ[0:3] |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| X | X | 0 | 0 (NOTE 1) | 1 (NOTE 1) |

NOTE 1: On next negative transition of the input signal (IN).

Absolute Maximum Ratings

Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item | Rating |
|------------------------------------------------------------------|--------------------------|
| Supply Voltage, V_{DD} | 4.6V |
| Inputs, V_I | -0.5V to $V_{DD} + 0.5V$ |
| Outputs, I_O Continuous Current Surge Current | 10mA 15mA |
| Input Current, I_N , nIN | $\pm 50mA$ |
| V_T Current, I_{VT} | $\pm 100mA$ |
| Input Sink/Source, I_{REF_AC} | $\pm 0.5mA$ |
| Operating Temperature Range, T_A | -40°C to +85°C |
| Package Thermal Impedance, θ_{JA} , (Junction-to-Ambient) | 74.7°C/W (0 mps) |
| Storage Temperature, T_{STG} | -65°C to 150°C |

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = 2.5V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|-------------------------|-----------------|---------|---------|---------|-------|
| V_{DD} | Positive Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| I_{DD} | Power Supply Current | | | | 95 | mA |

Table 4B. LVC MOS/LVTTL DC Characteristics, $V_{DD} = 2.5V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|--------------------|--------------------------------|---------|---------|----------------|---------|
| V_{IH} | Input High Voltage | | 1.7 | | $V_{DD} + 0.3$ | V |
| V_{IL} | Input Low Voltage | | -0.3 | | 0.7 | V |
| I_{IH} | Input High Current | $V_{DD} = V_{IN} = 2.625V$ | | | 10 | μA |
| I_{IL} | Input Low Current | $V_{DD} = 2.625V, V_{IN} = 0V$ | -150 | | | μA |

Table 4C. Differential DC Characteristics, $V_{DD} = 2.5V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------------|----------------------------------|-----------------|-----------------|-----------------|-----------------|----------|
| R_{IN} | Differential Input Resistance | IN, nIN | 40 | 50 | 60 | Ω |
| V_{IH} | Input High Voltage | IN, nIN | 1.2 | | V_{DD} | V |
| V_{IL} | Input Low Voltage | IN, nIN | 0 | | $V_{IH} - 0.15$ | V |
| V_{IN} | Input Voltage Swing; NOTE 1 | | 0.15 | | 1.2 | V |
| V_{DIFF_IN} | Differential Input Voltage Swing | | 0.3 | | | V |
| I_{IN} | Input Current; NOTE 2 | IN, nIN | | | 35 | mA |
| V_{REF_AC} | Reference Voltage | | $V_{DD} - 1.40$ | $V_{DD} - 1.35$ | $V_{DD} - 1.30$ | V |

 NOTE 1: V_{IL} should not be less than -0.3V.

NOTE 2: Guaranteed by design.

Table 4D. LVDS DC Characteristics, $V_{DD} = 2.5V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------|-----------------------------|-----------------|---------|---------|---------|-------|
| V_{OD} | Differential Output Voltage | | 247 | | 454 | mV |
| ΔV_{OD} | V_{OD} Magnitude Change | | | | 50 | mV |
| V_{OS} | Offset Voltage | | 1.125 | | 1.375 | V |
| ΔV_{OS} | V_{OS} Magnitude Change | | | | 50 | mV |

AC Electrical Characteristics

Table 5. AC Characteristics, $V_{DD} = 2.5V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|--------------|---------------------------------------------------------------------------|---------------------------------------------|---------|---------|---------|-------|
| f_{OUT} | Operating Frequency | | | | 2 | GHz |
| t_{PD} | Propagation Delay; (Differential) NOTE 1 | | 300 | | 550 | ps |
| $t_{sk(o)}$ | Output Skew; NOTE 2, 3 | | | | 25 | ps |
| $t_{sk(pp)}$ | Part-to-Part Skew; NOTE 3, 4 | | | | 200 | ps |
| f_{jit} | Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section | 200MHz, Integration Range: 12kHz - 20MHz | | 0.09 | | ps |
| t_s / t_H | Clock Enable Setup Time | EN to IN, nIN | 300 | | | ps |
| t_R / t_F | Output Rise/Fall Time | 20% to 80% | 50 | | 235 | ps |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

All parameters are measured at ≤ 1.5 GHz unless otherwise noted.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.

Measured at the output differential cross points.

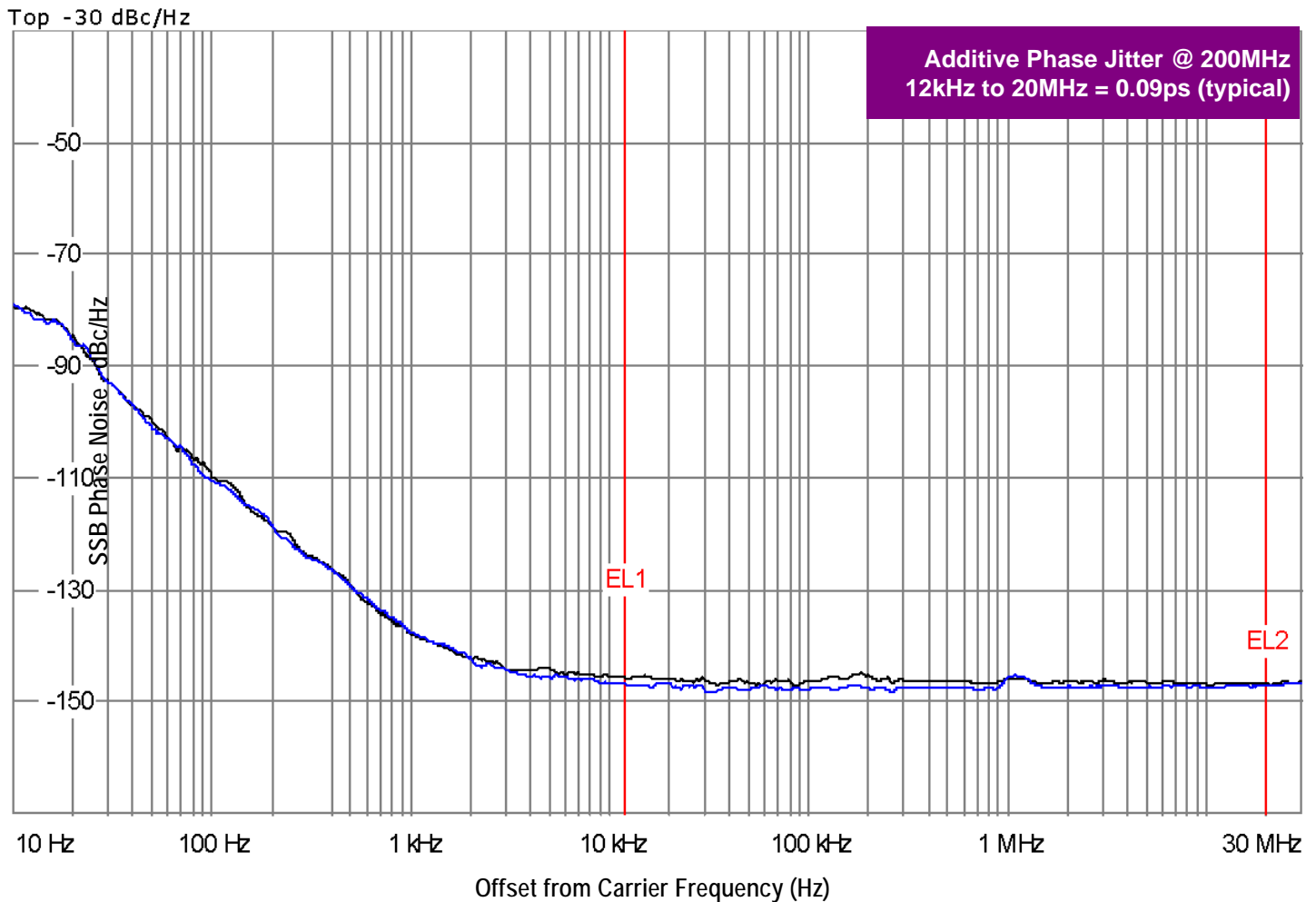
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise***. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the

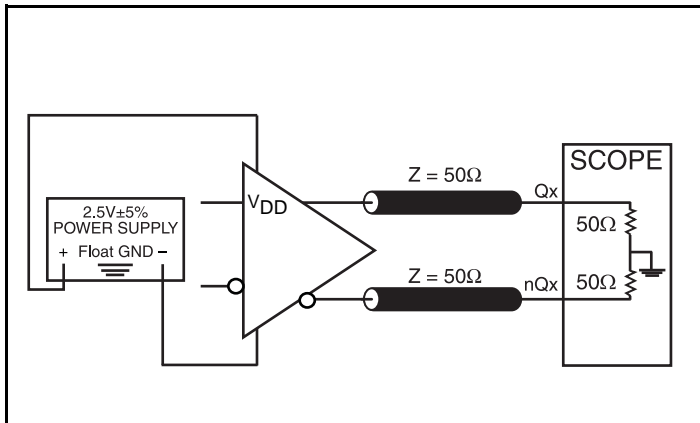
fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



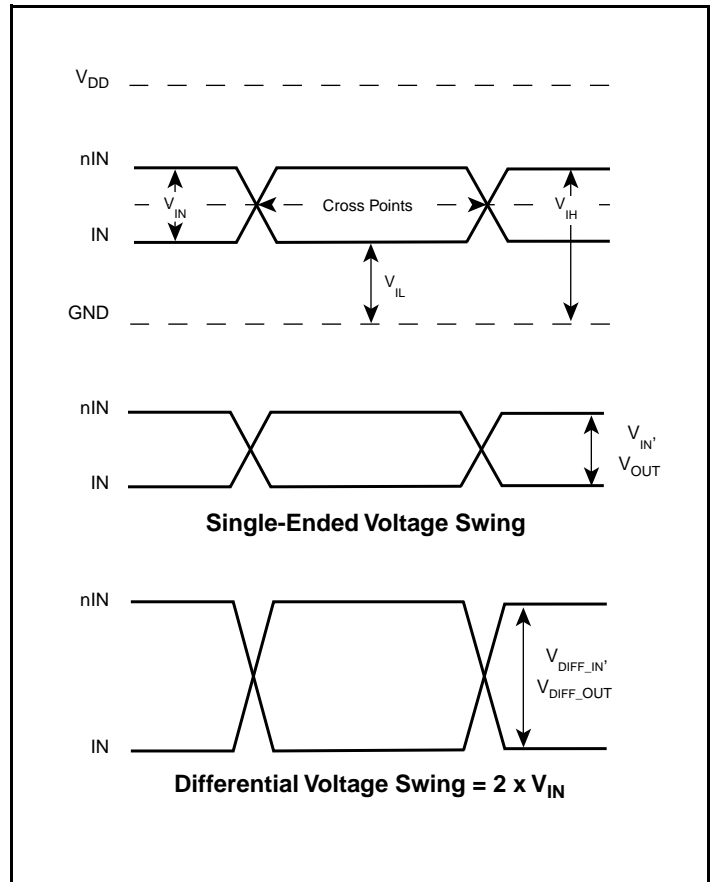
As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

The source generator "IFR2042 10kHz – 56.4GHz Low Noise Signal Generator as external input to an Agilent 8133A 3GHz Pulse Generator".

Parameter Measurement Information

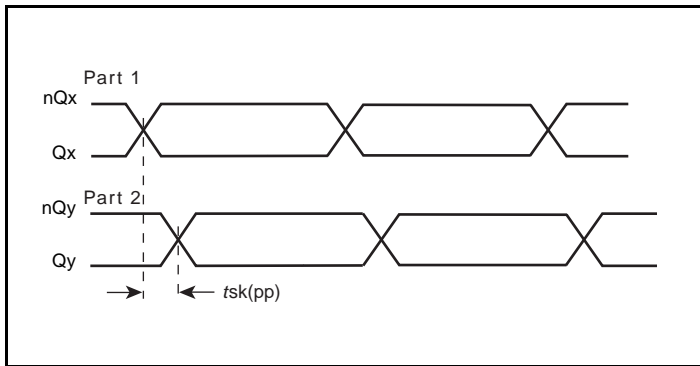


LVDS Output Load AC Test Circuit



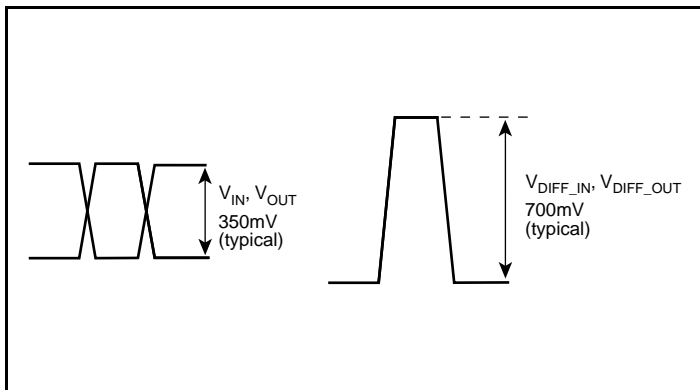
Single-Ended Voltage Swing

Differential Voltage Swing = 2 x V_{IN}

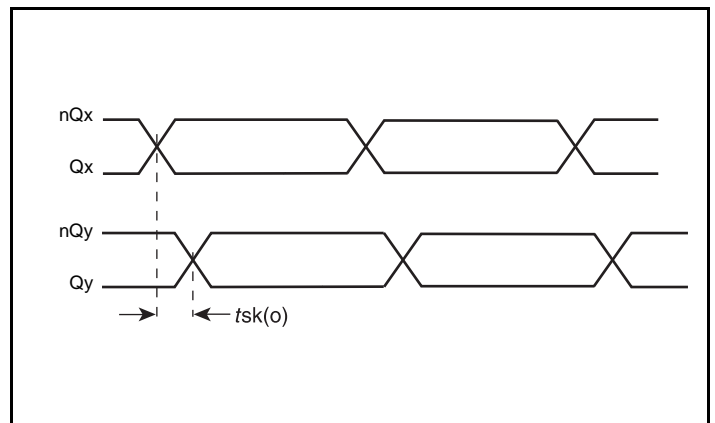


Part-to-Part Skew

Differential Input Level

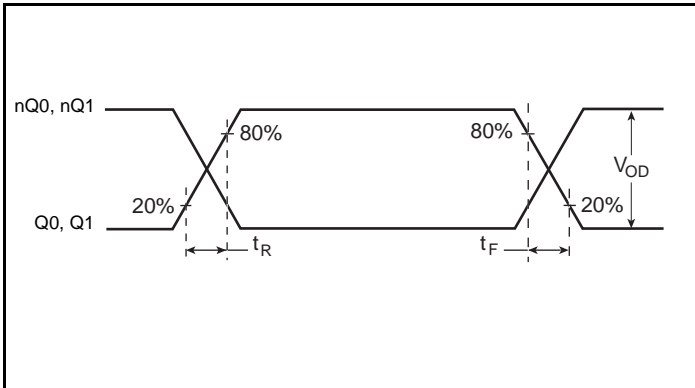


Single-Ended & Differential Input, Output Voltage Swing

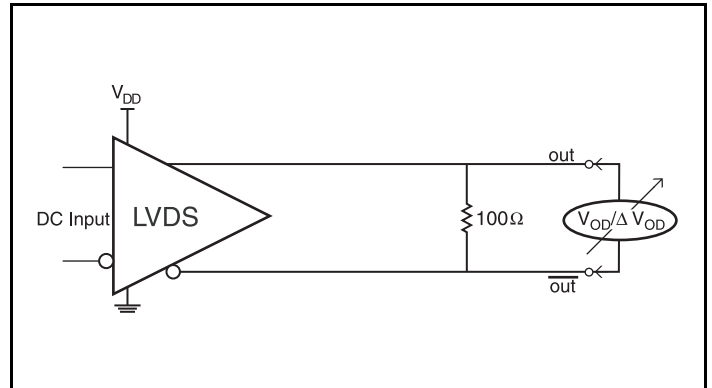


Output Skew

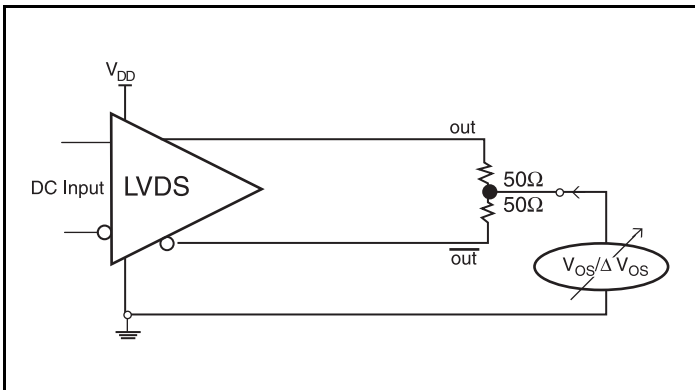
Parameter Measurement Information, continued



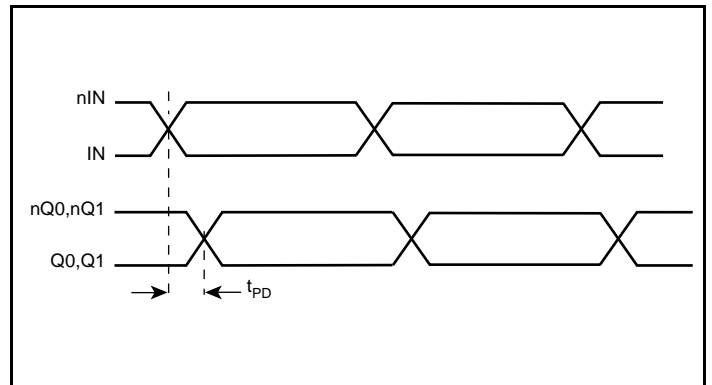
Output Rise/Fall Time



Differential Output Voltage Setup



Offset Voltage Setup



Propagation Delay

Application Information

Recommendations for Unused Output Pins

Outputs

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, we recommend that there is no trace attached.

2.5V LVPECL Input with Built-In 50Ω Termination Interface

The IN/nIN with built-in 50Ω terminations accept LVDS, LVPECL, SSTL and other differential signals. Both differential signals must meet the V_{PP} and V_{CMR} input requirements. Figures 2A to 2D show interface examples for the IN/nIN with built-in 50Ω termination input driven by the most common driver types. The input interfaces

suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

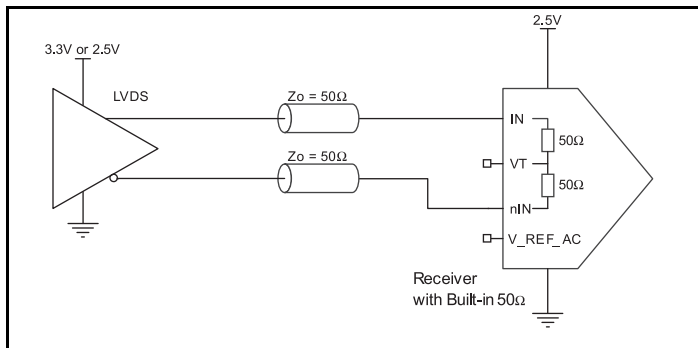


Figure 2A. IN/nIN Input with Built-In 50Ω Driven by an LVDS Driver

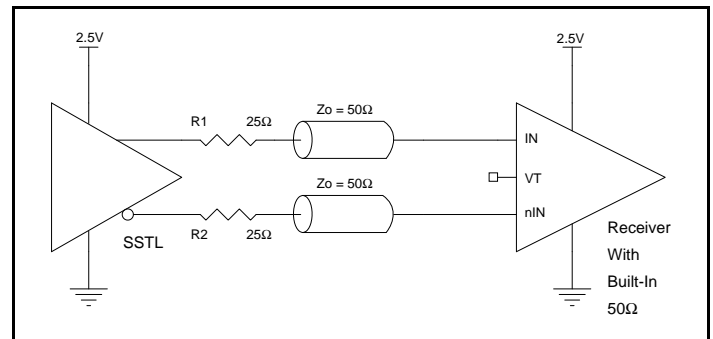


Figure 2B. IN/nIN Input with Built-In 50Ω Driven by an SSTL Driver

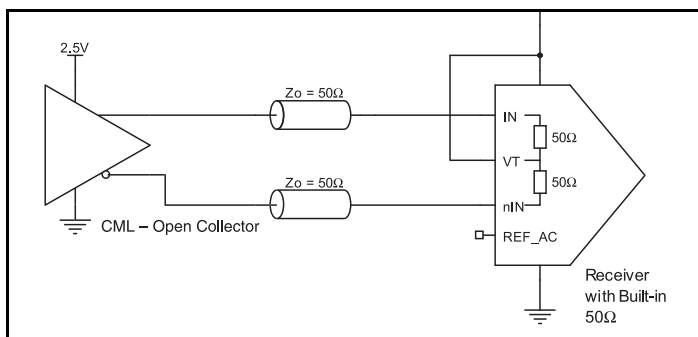


Figure 2C. IN/nIN Input with Built-In 50Ω Driven by a CML Driver

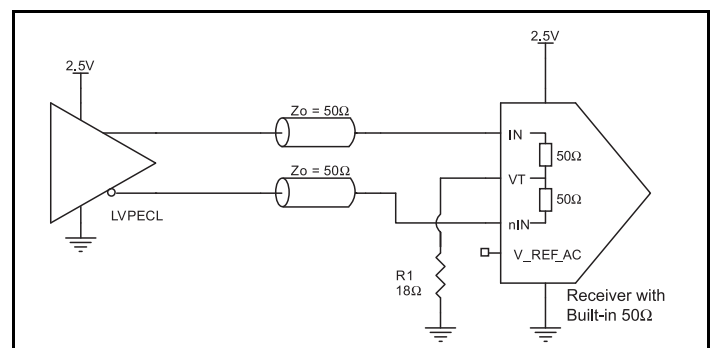


Figure 2D. IN/nIN Input with Built-In 50Ω Driven by an LVPECL Driver

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 3*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as "heat pipes". The number of vias (i.e. "heat pipes") are application specific

and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor's Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.

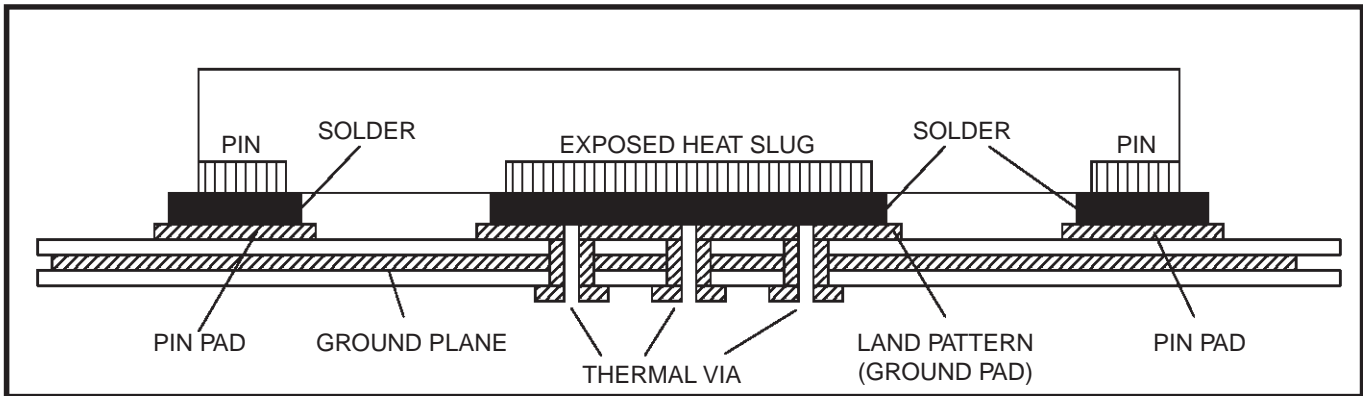


Figure 3. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

2.5V LVDS Driver Termination

Figure 4 shows a typical termination for LVDS driver in characteristic impedance of 100Ω differential (50Ω single)

transmission line environment. For buffer with multiple LVDS driver, it is recommended to terminate the unused outputs.

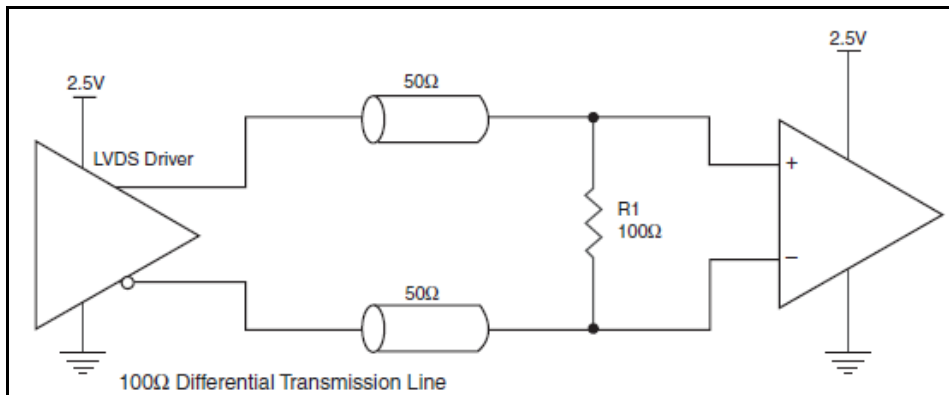


Figure 4. Typical LVDS Driver Termination

Power Considerations

This section provides information on power dissipation and junction temperature for the 8S89832I. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 8S89832I is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for $V_{DD} = 2.5V + 5\% = 2.625V$, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)_{MAX} = $V_{DD_MAX} * I_{DD_MAX} = 2.625V * 95mA = 249.375mW$

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, T_j , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 74.7°C/W per Table 6 below.

Therefore, T_j for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ\text{C} + 0.249\text{W} * 74.7^\circ\text{C/W} = 103.6^\circ\text{C}. \text{ This is well below the limit of } 125^\circ\text{C}.$$

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 16 Lead VFQFN Forced Convection

| Meters per Second | θ_{JA} by Velocity | | |
|---------------------------------------------|---------------------------|----------|----------|
| | 0 | 1 | 2.5 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 74.7°C/W | 65.3°C/W | 58.5°C/W |

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 16 Lead VFQFN

| Meters per Second | θ_{JA} by Velocity | | |
|---------------------------------------------|---------------------------|----------|----------|
| | 0 | 1 | 2.5 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 74.7°C/W | 65.3°C/W | 58.5°C/W |

Transistor Count

The transistor count for 8S89832I is: 339

Pin compatible with SY89832U.

This device is pin and function compatible and a suggested replacement for 889832.

Package Outline Drawings

The package outline drawings are located in the last section of this document. The package information is the most current data available and is subject to change without notice or revision of this document.

Ordering Information

Table 9. Ordering Information

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|-------------------|---------|---------------------------|--------------------|---------------|
| 8S89832AKILF | 832A | "Lead-Free" 16 Lead VFQFN | Tube | -40°C to 85°C |
| 8S89832AKILFT | 832A | "Lead-Free" 16 Lead VFQFN | Tape & Reel | -40°C to 85°C |

Revision History

| Revision Date | Description of Change |
|--------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| September 22, 2017 | Updated the package outline drawings; however, no mechanical changes Completed other minor improvements |
| January 27, 2016 | Removed ICS from part numbers where needed. General Description - Deleted ICS chip. Ordering Information - Deleted quantity from tape and reel. Deleted LF note below table. Updated header and footer. |
| January 11, 2010 | Parameter Measurement Information - updated <i>Differential Input Level</i> diagram. |



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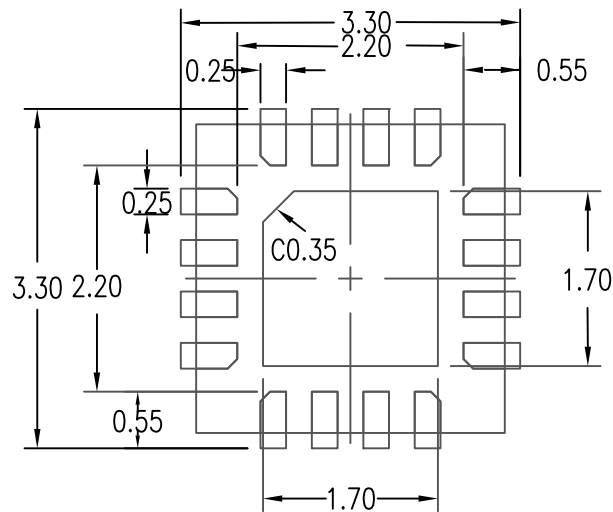
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RECOMMENDED LAND PATTERN

NOTES:

1. ALL DIMENSIONS ARE IN mm.ANGLES IN DEGREES
2. TOP DOWN VIEW-AS VIEWED ON PCB
3. LAND PATTERN RECOMMENDATION IS PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN

| Package Revision History | | |
|--------------------------|---------|-------------------|
| Date Created | Rev No. | Description |
| Aug 15, 2017 | Rev 03 | Update Epad Range |
| Jul 28, 2017 | Rev 02 | New format |