# SE95

## Ultra high accuracy digital temperature sensor and thermal watchdog

Rev. 07 — 2 September 2009 Product data sheet

## 1. General description

The SE95 is a temperature-to-digital converter using an on-chip band gap temperature sensor and Sigma Delta analog-to-digital conversion technique. The device is also a thermal detector providing an overtemperature detection output.

The SE95 contains a number of data registers accessed by a controller via the 2-wire serial $I^2C$-bus interface:

- Configuration register (Conf) to store the device settings such as sampling rate, device operation mode, OS operation mode, OS polarity, and OS fault queue
- Temperature register (Temp) to store the digital Temp reading
- Set-point registers (Tos and Thyst) to store programmable overtemperature shutdown and hysteresis limits
- Identification register (ID) to store manufacturer numbers

The device includes an open-drain output (pin OS) which becomes active when the temperature exceeds the programmed limits. There are three selectable logic address pins (pins A2 to A0) so that eight devices can be connected on the same bus without address conflict.

The SE95 can be configured for different operation conditions. It can be set in normal mode to periodically monitor the ambient temperature, or in shutdown mode to minimize power consumption. The OS output operates in either of two selectable modes: OS comparator mode and OS interrupt mode. Its active state can be selected as either HIGH or LOW. The fault queue that defines the number of consecutive faults in order to activate the OS output is programmable as well as the set-point limits.

The temperature register always stores a 13-bit two's complement data giving a temperature resolution of 0.03125 °C. This high temperature resolution is particularly useful in applications of measuring precisely the thermal drift or runaway. For normal operation and compatibility with the LM75A, only the 11 MSBs are read, with a resolution of 0.125 °C to provide the accuracies specified. To be compatible with the LM75, read only the 9 MSBs.

The device is powered-up in normal operation mode with the OS in comparator mode, temperature threshold of 80 °C and hysteresis of 75 °C, so that it can be used as a stand-alone thermostat with those pre-defined temperature set points. The conversion rate is programmable, with a default of 10 conversions/s.

## 2. Features

- Pin-for-pin replacement for industry standard LM75/LM75A
- Specification of a single part over supply voltage from 2.8 V to 5.5 V
- Small 8-pin package types: SO8 and TSSOP8 (MSOP8)
- $I^2C$-bus interface to 400 kHz with up to 8 devices on the same bus
- Supply voltage from 2.8 V to 5.5 V
- Temperature range from −55 °C to +125 °C
- 13-bit ADC that offers a temperature resolution of 0.03125 °C
- Temperature accuracy of ± 1 °C from −25 °C to +100 °C
- Programmable temperature threshold and hysteresis set points
- Supply current of 7.0 µA in shutdown mode for power conservation
- Stand-alone operation as thermostat at power-up
- ESD protection exceeds 1000 V for Human Body Model (HBM) per JESD22-A114 and 150 V for Machine Model (MM) per JESD22-A115
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA

## 3. Applications

- System thermal management
- Personal computers
- Electronics equipment
- Industrial controllers

## 4. Ordering information

**Table 1. Ordering information**

| Type number | Package | | | |
|---|---|---|---|---|
| | Temperature range | Name | Description | Version |
| SE95D | −55 °C to +125 °C | SO8 | plastic small outline package; 8 leads; body width 3.9 mm | SOT96-1 |
| SE95DP | −55 °C to +125 °C | TSSOP8 | plastic thin shrink small outline package; 8 leads; body width 3 mm | SOT505-1 |
| SE95U | −55 °C to +125 °C | - | wafer | - |

# 5. Block diagram

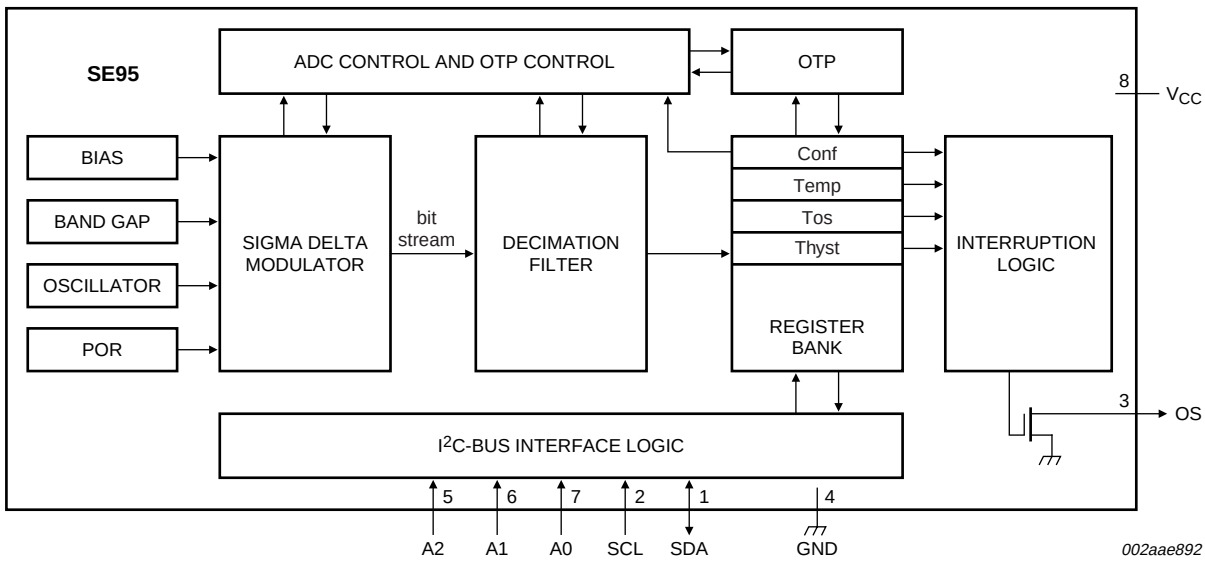



**Fig 1. Block diagram of SE95**

# 6. Pinning information

## 6.1 Pinning

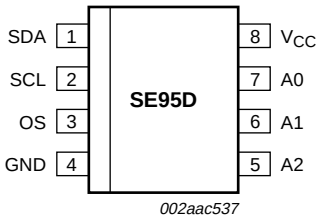



**Fig 2. Pin configuration for SO8**

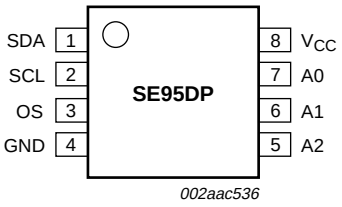



**Fig 3. Pin configuration for TSSOP8**

## 6.2 Pin description

**Table 2. Pin description**

| Symbol | Pin | Description |
|---|---|---|
| SDA | 1 | $I^2C$-bus serial bidirectional data line digital I/O; open-drain |
| SCL | 2 | $I^2C$-bus serial clock digital input |
| OS | 3 | overtemperature shutdown output; open-drain |
| GND | 4 | ground; to be connected to the system ground |
| A2 | 5 | user-defined address bit 2 digital input |

**Table 2. Pin description** *...continued*

| Symbol | Pin | Description |
|---|---|---|
| A1 | 6 | user-defined address bit 1 digital input |
| A0 | 7 | user-defined address bit 0 digital input |
| $V_{CC}$ | 8 | supply voltage |

# 7. Functional description

## 7.1 General operation

The SE95 uses the on-chip band gap sensor to measure the device temperature with a resolution of 0.03125 °C and stores the 13-bit two's complement digital data, resulting from 13-bit analog to digital conversion, into register Temp. Register Temp can be read at any time by a controller on the $I^2C$-bus. Reading temperature data does not affect the conversion in progress during the read operation.

The device can be set to operate in either mode: normal or shutdown mode. In normal operation mode, by default, the temperature-to-digital conversion is executed every 100 ms and register Temp is updated at the end of each conversion. In shutdown mode, the device becomes idle, data conversion is disabled and register Temp holds the latest result; however, the device $I^2C$-bus interface is still active and register write/read operation can be performed. The device operation mode is controlled by programming bit SHUTDOWN of register Conf. The temperature conversion is initiated when the device is powered up or returned to normal mode from shutdown mode.

In addition, at the end of each conversion in normal mode, the temperature data (or Temp) in register Temp is automatically compared with the overtemperature shutdown threshold data (or Tos) stored in register Tos, and the hysteresis data (or Thyst) stored in register Thyst, in order to set the state of the device OS output accordingly. The registers Tos and Thyst are write/read capable, and both operate with 9-bit two's complement digital data. To match with this 9-bit operation, register Temp uses only the 9 MSB bits of its 13-bit data for the comparison.

The device temperature conversion rate is programmable and can be chosen to be one of the four values: 0.125, 1.0, 10, and 30 conversions/s. The default conversion rate is 10 conversions/s. Furthermore, the conversion rate is selected by programming bits RATEVAL[1:0] of register Conf as shown in Table 6. Note that the average supply current as well as the device power consumption increase with the conversion rate.

The way that the OS output responds to the comparison operation depends upon the OS operation mode selected by configuration bit OS_COMP_INT, and the user-defined fault queue defined by configuration bits OS_F_QUE[1:0].

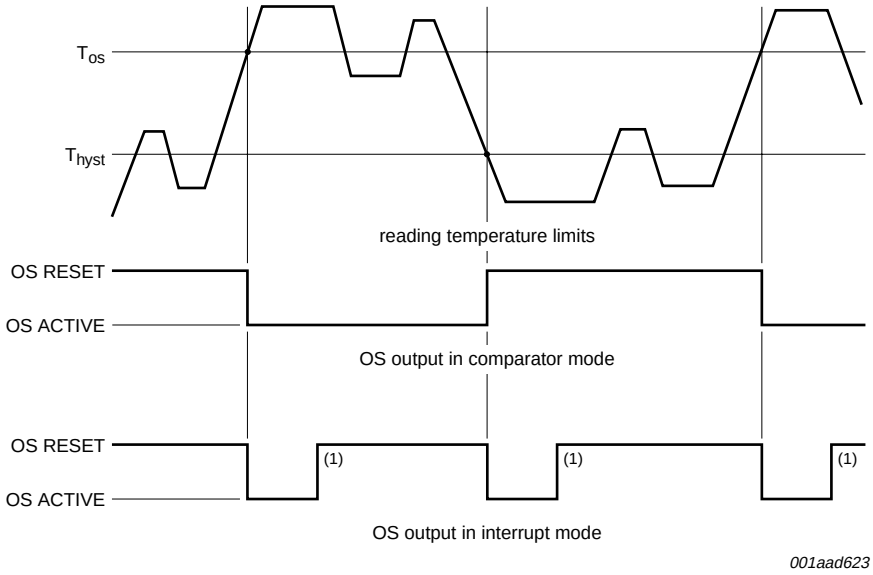
In OS comparator mode, the OS output behaves like a thermostat. It becomes active when the temperature exceeds $T_{os}$, and is reset when the temperature drops below $T_{hyst}$. Reading the device registers or putting the device into shutdown mode does not change the state of the OS output. The OS output in this case can be used to control cooling fans or thermal switches.

In OS interrupt mode, the OS output is used for thermal interruption. When the device is powered-up, the OS output is first activated only when Temp exceeds $T_{os}$; then it remains active indefinitely until being reset by a read of any register. Once the OS output has been activated by crossing $T_{os}$ and then reset, it can be activated again only when Temp drops below $T_{hyst}$; then again, it remains active indefinitely until being reset by a read of any register. The OS interrupt operation would be continued in this sequence: $T_{os}$ trip, reset, $T_{hyst}$ trip, reset, $T_{os}$ trip, reset, $T_{hyst}$ trip, reset, and etc. Putting the device into shutdown mode also resets the OS output.

In both cases, comparator mode and interrupt mode, the OS output is activated only if a number of consecutive faults, defined by the device fault queue, has been met. The fault queue is programmable and stored in bits OS_F_QUE[1:0], of register Conf. Also, the OS output active state is selectable as HIGH or LOW by setting accordingly the bit OS_POL of register Conf.

At power-up, the device is put into normal operation mode, register Tos is set to 80 °C, register Thyst is set to 75 °C, OS active state is selected LOW and the fault queue is equal to 1. The data reading of register Temp is not available until the first conversion is completed in about 33 ms.

The OS response to the temperature is illustrated in Figure 4.




(1) OS is reset by either reading register or putting the device in shutdown mode. Assumed that the fault queue is met at each $T_{os}$ and $T_{hyst}$ crossing point.

**Fig 4. OS response to temperature**

## 7.2 OS output and polarity

The OS output is an open-drain output and its state represents results of the device watchdog operation as described in Section 7.1. In order to observe this output state, an external pull-up resistor is needed. The resistor should be as large as possible, up to 200 kΩ, to minimize the Temp reading error due to internal heating by the high OS sinking current.

The OS output active state can be selected as HIGH or LOW by programming bit OS_POL of register Conf: setting bit OS_POL to logic 1 selects OS active HIGH and setting to logic 0 sets OS active LOW. At power-up, bit OS_POL is equal to logic 0 and the OS active state is LOW.

## 7.3 OS comparator and interrupt modes

As described in Section 7.1, the OS output responds to the result of the comparison between register Temp data and the programmed limits, in registers Tos and Thyst, in different ways depending on the selected OS mode: OS comparator or OS interrupt. The OS mode is selected by programming bit OS_COMP_INT of register Conf: setting bit OS_COMP_INT to logic 1 selects the OS interrupt mode, and setting to logic 0 selects the OS comparator mode. At power-up, bit OS_COMP_INT is equal to logic 0 and the OS comparator is selected.

The main difference between the two modes is that in OS comparator mode, the OS output becomes active when Temp has exceeded $T_{os}$ and reset when Temp has dropped below $T_{hyst}$, reading a register or putting the device into shutdown mode does not change the state of the OS output; while in OS interrupt mode, once it has been activated either by exceeding $T_{os}$ or dropping below $T_{hyst}$, the OS output will remain active indefinitely until reading a register or putting the device into shutdown mode occurs, then the OS output is reset.

Temperature limits $T_{os}$ and $T_{hyst}$ must be selected so that $T_{os} > T_{hyst}$. Otherwise, the OS output state will be undefined.

## 7.4 OS fault queue

Fault queue is defined as the number of faults that must occur consecutively to activate the OS output. It is provided to avoid false tripping due to noise. Because faults are determined at the end of data conversions, fault queue is also defined as the number of consecutive conversions returning a temperature trip. The value of fault queue is selectable by programming the two bits OS_F_QUE[1:0] in register Conf. Notice that the programmed data and the fault queue value are not the same. Table 3 shows the one-to-one relationship between them. At power-up, fault queue data = 00 and fault queue value = 1.

**Table 3. Fault queue table**

| Fault queue data | | Fault queue value |
|---|---|---|
| OS_F_QUE[1] | OS_F_QUE[0] | Decimal |
| 0 | 0 | 1 |
| 0 | 1 | 2 |
| 1 | 0 | 4 |
| 1 | 1 | 6 |

### 7.5 Shutdown mode

The device operation mode is selected by programming bit SHUTDOWN of register Conf. Setting bit SHUTDOWN to logic 1 will put the device into shutdown mode. Resetting bit SHUTDOWN to logic 0 will return the device to normal mode.

In shutdown mode, the device draws a small current of approximately 7.5 μA and the power dissipation is minimized; the temperature conversion stops, but the $I^2C$-bus interface remains active and register write/read operation can be performed. If the OS output is in comparator mode, then it remains unchanged. In interrupt mode, the OS output is reset.

### 7.6 Power-up default and power-on reset

The SE95 always powers-up in its default state with:

- Normal operation mode
- OS comparator mode
- $T_{os}$ = 80 °C
- $T_{hyst}$ = 75 °C
- OS output active state is LOW
- Pointer value is logic 0

When the power supply voltage is dropped below the device power-on reset level of approximately 1.9 V (POR) and then rises up again, the device will be reset to its default condition as listed above.

## 8. $I^2C$-bus serial interface

The SE95 can be connected to a compatible 2-wire serial interface $I^2C$-bus as a slave device under the control of a controller or master device, using two device terminals, SCL and SDA. The controller must provide the SCL clock signal and write/read data to and from the device through the SDA terminal. Note that if the $I^2C$-bus common pull-up resistors have not been installed as required for $I^2C$-bus, then an external pull-up resistor, approximately 10 kΩ, is needed for each of these two terminals. The bus communication protocols are described in Section 8.7 “Protocols for writing and reading the registers”.

### 8.1 Slave address

The SE95 slave address on the $I^2C$-bus is partially defined by the logic applied to the device address pins A2, A1 and A0. Each pin is typically connected either to GND for logic 0, or to $V_{CC}$ for logic 1. These pins represent the three LSB bits of the device 7-bit address. The other four MSB bits of the address data are preset to 1001 by hard wiring inside the SE95. Table 4 shows the device's complete address and indicates that up to 8 devices can be connected to the same bus without address conflict. Because the input pins SCL, SDA and A2 to A0, are not internally biased, it is important that they should not be left floating in any application.

0Ch is a reserved address for SMBus Alert Response Address (ARA). This is an optional command from the SMBus specification to allow SMBus devices to respond to an SMBus master with their slave device if they are generating an interrupt. The SE95 will send a

false alert if the address 0Ch is sent and cannot be active on the I²C-bus if this address is used. Consider using the SE98 since it supports SMBus ARA as well as time-out features and provides ±1 °C accuracy.

**Table 4. Address table**

| MSB | | | | | | LSB |
|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 1 | A2 | A1 | A0 |

## 8.2 Register list

The SE95 contains 7 data registers. The registers can be 1 byte or 2 bytes wide, and are defined in Table 5. The registers are accessed by the value in the content of the pointer register during I²C-bus communication. The types of registers are: read only, read/write, and reserved for manufacturer use. Note that when reading a two-byte register, the host must provide enough clock pulses as required by the I²C-bus protocol (see Section 8.7) for the device to completely return both data bytes. Otherwise the device may hold the SDA line in LOW state, resulting in a bus hang condition.

**Table 5. Register table**

| Register name | Pointer value | R/W | POR state | Description |
|---|---|---|---|---|
| Conf | 01h | R/W | 00h | configuration register: contains a single 8-bit data byte; to set an operating condition |
| Temp | 00h | read only | N/A | temperature register: contains two 8-bit data bytes; to store the measured Temp |
| Tos | 03h | R/W | 5000h | overtemperature shutdown threshold register: contains two 8-bit data bytes; to store the overtemperature shutdown limit; default $T_{os}$ = 80 °C |
| Thyst | 02h | R/W | 4B00h | hysteresis register: contains two 8-bit data bytes; to store the hysteresis limit; bit 7 to bit 0 are also used in OTP (One Time Programmable) test mode to supply OTP write data; default $T_{hyst}$ = 75 °C |
| ID | 05h | read only | A1h | identification register: contains a single 8-bit data byte for the manufacturer ID code |
| Reserved | 04h | N/A | N/A | reserved |
| Reserved | 06h | N/A | N/A | reserved |

## 8.3 Register pointer

The register pointer or pointer byte is an 8-bit data byte that is equivalent to the register command in the I²C-bus definitions and is used to identify the device register to be accessed for a write or read operation. Its values are listed as pointer values in Table 5. For the device register I²C-bus communication, the pointer byte may or may not need to be included within the command as illustrated in the I²C-bus protocol figures in Section 8.7.

The command statements for writing data to a register must always include the pointer byte; while the command statements for reading data from a register may or may not include it. To read a register that is different from the one that has been recently read, the pointer byte must be included. However, to re-read a register that has been recently read, the pointer byte may not have to be included in the reading.

At power-up, the pointer value is preset to logic 0 for register Temp; users can then read the temperature without specifying the pointer byte.

## 8.4 Configuration register

The Configuration (Conf) register is a read/write register and contains an 8-bit non-complement data byte that is used to configure the device for different operating conditions. Table 6 shows the bit assignments of this register.

**Table 6. Conf register**

*Legend: * = default value.*

| Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|
| 7 | reserved | R/W | 0* | reserved for manufacturer's use |
| 6 and 5 | RATEVAL[1:0] | R/W | | sets the conversion rate |
| | | | 00* | 10 conversion/s |
| | | | 01 | 0.125 conversion/s |
| | | | 10 | 1 conversion/s |
| | | | 11 | 30 conversion/s |
| 4 and 3 | OS_F_QUE[1:0] | R/W | | OS fault queue programming |
| | | | 00* | queue value = 1 |
| | | | 01 | queue value = 2 |
| | | | 10 | queue value = 4 |
| | | | 11 | queue value = 6 |
| 2 | OS_POL | R/W | | OS polarity selection |
| | | | 0* | OS active LOW |
| | | | 1 | OS active HIGH |
| 1 | OS_COMP_INT | R/W | | OS operation mode selection |
| | | | 0* | OS comparator |
| | | | 1 | OS interrupt |
| 0 | SHUTDOWN | R/W | 0 | operation mode |
| | | | 0* | normal |
| | | | 1 | shutdown |

## 8.5 Temperature register

The Temperature (Temp) register holds the digital result of temperature measurement or monitor at the end of each analog to digital conversion. This register is read only and contains two 8-bit data bytes consisting of one Most Significant Byte (MSByte) and one Least Significant Byte (LSByte). However, only 13 bits of those two bytes are used to store the Temp data in two's complement format with the resolution of 0.03125 °C. Table 7 shows the bit arrangement of the Temp data in the data bytes.

**Table 7. Temp register**

| MSByte | | | | | | | | LSByte | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

When reading register Temp, all 16 bits of the two data bytes (MSByte and LSByte) must be collected and then the two's complement data value according to the desired resolution must be selected for the temperature calculation. Table 8 shows the example for 11-bit two's complement data value, Table 9 shows the example for 13-bit two's complement data value.

**Table 8. Example 11-bit two's complement Temp register**

| MSByte | | | | | | | | LSByte | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | X | X | X | X | X |

**Table 9. Example 13-bit two's complement register**

| MSByte | | | | | | | | LSByte | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | X | X | X |

When converting into the temperature the proper resolution must be used as listed in Table 10 using either one of these two formulae:

1. If the Temp data MSB = 0, then: Temp (°C) = +(Temp data) × value resolution
2. If the Temp data MSB = 1, then: Temp (°C) = –(two's complement Temp data) × value resolution

**Table 10. Temp data and Temp value resolution**

| Data resolution | Value resolution |
|---|---|
| 8 bit | 1.0 °C |
| 9 bit | 0.5 °C |
| 10 bit | 0.25 °C |
| 11 bit | 0.125 °C |
| 12 bit | 0.0625 °C |
| 13 bit | 0.03125 °C |

Table 11 shows some examples of the results for the 11-bit calculations.

**Table 11. Temp register value**

| 11-bit binary (two's complement) | Hexadecimal value | Decimal value | Value |
|---|---|---|---|
| 011 1111 1000 | 3F8 | 1016 | +127.000 °C |
| 011 1111 0111 | 3F7 | 1015 | +126.875 °C |
| 011 1111 0001 | 3F1 | 1009 | +126.125 °C |
| 011 1110 1000 | 3E8 | 1000 | +125.000 °C |
| 000 1100 1000 | 0C8 | 200 | +25.000 °C |
| 000 0000 0001 | 001 | 1 | +0.125 °C |
| 000 0000 0000 | 000 | 0 | 0.000 °C |
| 111 1111 1111 | 7FF | –1 | –0.125 °C |
| 111 0011 1000 | 738 | –200 | –25.000 °C |
| 110 0100 1001 | 649 | –439 | –54.875 °C |
| 110 0100 1000 | 648 | –440 | –55.000 °C |

Obviously, for 9-bit Temp data application in replacing the industry standard LM75, just use only 9 MSB bits of the two bytes and disregard 7 LSB of the LSByte. The 9-bit Temp data with 0.5 °C resolution of the SE95 is defined exactly in the same way as for the standard LM75 and it is here similar to the Tos and Thyst registers.

## 8.6 Overtemperature shutdown threshold and hysteresis registers

These two registers, are write/read registers, and also called set-point registers. They are used to store the user-defined temperature limits, called overtemperature shutdown threshold (Tos) and hysteresis temperature (Thyst), for the device watchdog operation. At the end of each conversion the Temp data will be compared with the data stored in these two registers in order to set the state of the device OS output; see Section 7.1.

Each of the set-point registers contains two 8-bit data bytes consisting of one MSByte and one LSByte the same as register Temp. However, only 9 bits of the two bytes are used to store the set-point data in two's complement format with the resolution of 0.5 °C. Table 12 and Table 13 show the bit arrangement of the Tos data and Thyst data in the data bytes.

Notice that because only 9-bit data are used in the set-point registers, the device uses only the 9 MSB of the Temp data for data comparison.

**Table 12. Tos register**

| MSByte | | | | | | | | LSByte | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | X | X | X | X | X | X | X |

**Table 13. Thyst register**

| MSByte | | | | | | | | LSByte | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | X | X | X | X | X | X | X |

When a set-point register is read, all 16 bits are provided to the bus and must be collected by the controller to complete the bus operation. However, only the 9 most significant bits should be used and the 7 LSB of the LSByte are equal to zero and should be ignored.

Table 14 shows examples of the limit data and value.

**Table 14. Tos and Thyst register**

| 11-bit binary (two's complement) | Hexadecimal value | Decimal value | Value |
|---|---|---|---|
| 0 1111 1010 | 0FA | 250 | 125.0 °C |
| 0 0011 0010 | 032 | 50 | 25.0 °C |
| 0 0000 0001 | 001 | 1 | 0.5 °C |
| 0 0000 0000 | 000 | 0 | 0.0 °C |
| 1 1111 1111 | 1FF | –1 | –0.5 °C |
| 1 1100 1110 | 1CE | –50 | –25.0 °C |
| 1 1001 0010 | 192 | –110 | –55.0 °C |

## 8.7 Protocols for writing and reading the registers

The communication between the host and the SE95 must follow the rules strictly as defined by the $I^2C$-bus management. The protocols for SE95 register read/write operations are illustrated in Figure 5 to Figure 10 together with the following definitions:

1. Before a communication, the $I^2C$-bus must be free or not busy. It means that the SCL and SDA lines must both be released by all devices on the bus, and they become HIGH by the bus pull-up resistors.
2. The host must provide SCL clock pulses necessary for the communication. Data is transferred in a sequence of 9 SCL clock pulses for every 8-bit data byte followed by 1-bit status of the acknowledgement.
3. During data transfer, except the START and STOP signals, the SDA signal must be stable while the SCL signal is HIGH. It means that the SDA signal can be changed only during the LOW duration of the SCL line.
4. S: START signal, initiated by the host to start a communication, the SDA goes from HIGH-to-LOW while the SCL is HIGH.
5. RS: RE-START signal, same as the START signal, to start a read command that follows a write command.
6. P: STOP signal, generated by the host to stop a communication, the SDA goes from LOW-to-HIGH while the SCL is HIGH. The bus becomes free thereafter.
7. W: write bit, when the write/read bit is in a write command.
8. R: read bit, when the write/read bit is logic 1 in a read command.
9. A: device acknowledge bit, returned by the SE95. It is logic 0 if the device works properly and logic 1 if not. The host must release the SDA line during this period in order to give the device the control on the SDA line.
10. A': master acknowledge bit, not returned by the device, but set by the master or host in reading 2-byte data. During this clock period, the host must set the SDA line to LOW in order to notify the device that the first byte has been read for the device to provide the second byte onto the bus.
11. NA: not-acknowledge bit. During this clock period, both the device and host release the SDA line at the end of a data transfer, the host is then enabled to generate the stop signal.
12. In a write protocol, data is sent from the host to the device and the host controls the SDA line, except during the clock period when the device sends the device acknowledgement signal to the bus.
13. In a read protocol, data is sent to the bus by the device and the host must release the SDA line during the time that the device is providing data onto the bus and controlling the SDA line, except during the clock period when the master sends the master acknowledgement signal to the bus.

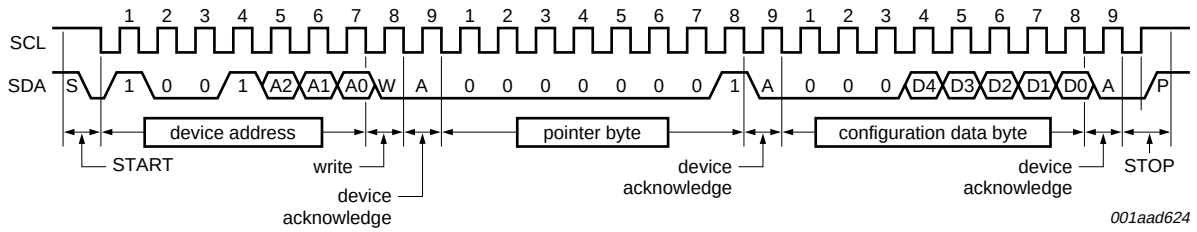



**Fig 5. Write configuration register (1-byte data)**

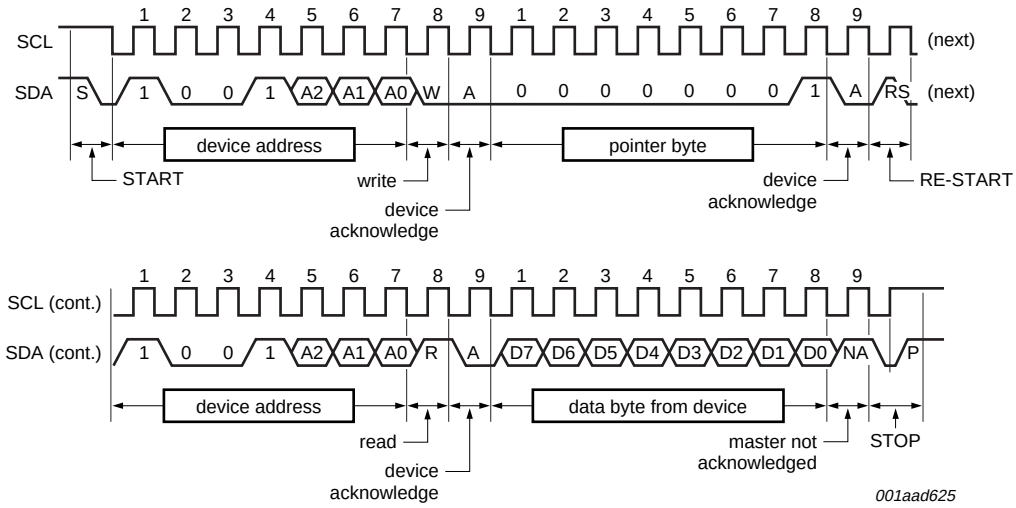



**Fig 6. Read configuration register including pointer byte (1-byte data)**

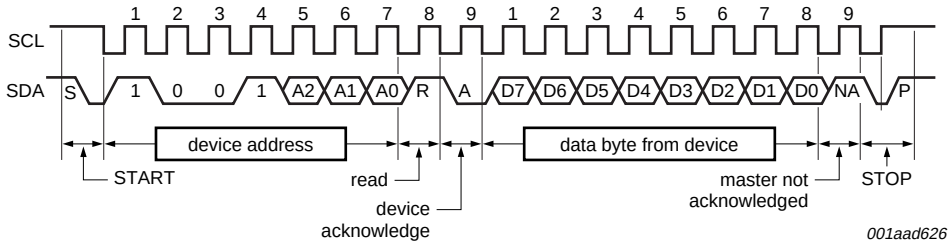



**Fig 7. Read configuration register with preset pointer (1-byte data)**

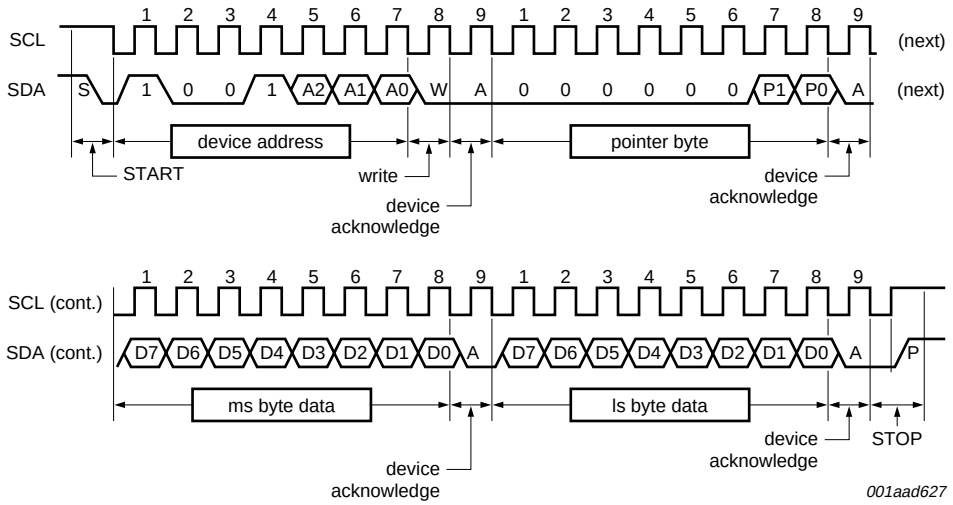



**Fig 8. Write Tos or Thyst register (2-byte data)**

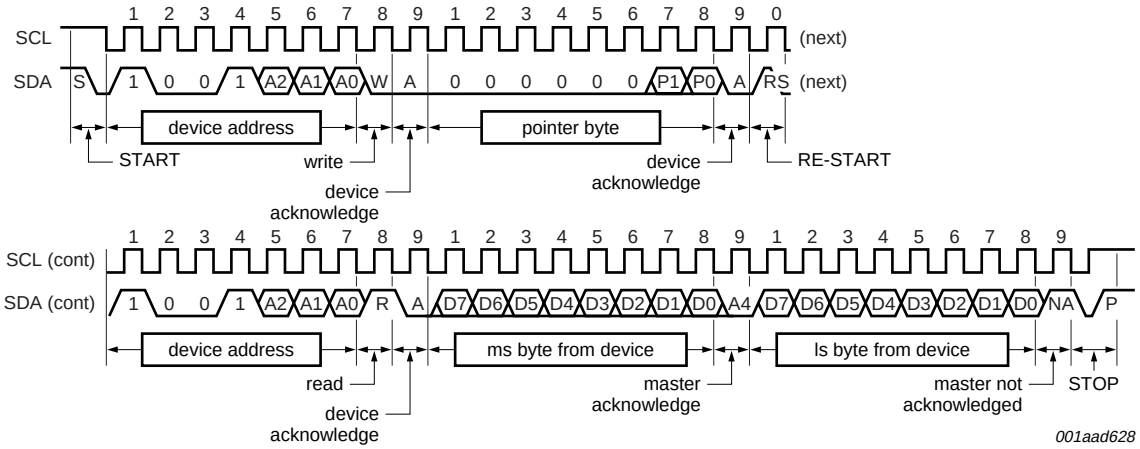



**Fig 9. Read Temp, Tos or Thyst register including pointer byte (2-byte data)**

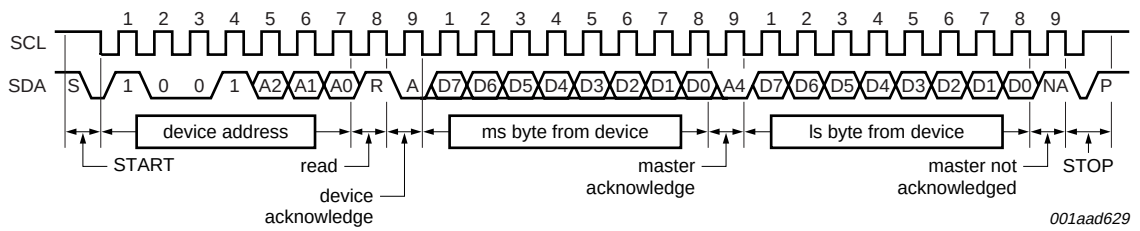



**Fig 10. Read Temp, Tos or Thyst register with preset pointer (2-byte data)**

# 9. Limiting values

**Table 15. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | –0.3 | +6.0 | V |
| $V_{I(SCL)}$ | input voltage on pin SCL | | –0.3 | +6.0 | V |
| $V_{I(SDA)}$ | input voltage on pin SDA | | –0.3 | +6.0 | V |
| $V_{I(A0)}$ | input voltage on pin A0 | | –3.0 | $V_{CC}$ + 0.3 | V |
| $V_{I(A1)}$ | input voltage on pin A1 | | –3.0 | $V_{CC}$ + 0.3 | V |
| $V_{I(A2)}$ | input voltage on pin A2 | | –3.0 | $V_{CC}$ + 0.3 | V |
| $I_{I(PIN)}$ | input current on input pins | | –5.0 | +5.0 | mA |
| $I_{O(OS)}$ | output current on pin OS | | - | 10.0 | mA |
| $V_{O(OS)}$ | output voltage on pin OS | | –0.3 | +6.0 | V |
| $V_{ESD}$ | electrostatic discharge voltage | human body model | - | 1000 | V |
| | | machine model | - | 150 | V |
| $T_{stg}$ | storage temperature | | –65 | +150 | °C |
| $T_j$ | junction temperature | | - | 150 | °C |

# 10. Recommended operating conditions

**Table 16. Recommended operating characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | 2.8 | - | 5.5 | V |
| $T_{amb}$ | ambient temperature | | –55 | - | +125 | °C |

# 11. Static characteristics

**Table 17. Static characteristics**

*$V_{CC}$ = 2.8 V to 5.5 V, $T_{amb}$ = −55 °C to +125 °C; unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| $T_{acc}$ | temperature accuracy | $V_{CC}$ = 2.8 V to 3.6 V | [2] | | | | |
| | | $T_{amb}$ = −25 °C to +100 °C | | −1.0 | - | +1.0 | °C |
| | | $T_{amb}$ = −55 °C to +125 °C | | −2.0 | - | +2.0 | °C |
| | | $V_{CC}$ = 3.6 V to 5.5 V | [2] | | | | |
| | | $T_{amb}$ = −25 °C to +100 °C | | −2 | - | +2 | °C |
| | | $T_{amb}$ = −55 °C to +125 °C | | −3 | - | +3 | °C |
| $T_{res}$ | temperature resolution | 11-bit digital temperature data | | - | 0.125 | - | °C |
| $t_{conv(T)}$ | temperature conversion time | normal mode | | - | 33 | - | ms |
| $I_{CC}$ | supply current | normal mode: $I^2C$-bus inactive | | - | 150 | - | µA |
| | | normal mode: $I^2C$-bus active | | - | - | 1.0 | mA |
| | | shutdown mode | | - | 7.5 | - | µA |
| $V_{IH}$ | HIGH-level input voltage | digital pins | [3] | 0.7$V_{CC}$ | - | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | LOW-level input voltage | digital pins | [3] | −0.3 | - | +0.3$V_{CC}$ | V |
| $V_{I(hys)}$ | hysteresis of input voltage | pins SCL and SDA | | - | 300 | - | mV |
| | | pins A2 to A0 | | - | 300 | - | mV |
| $I_{IH}$ | HIGH-level input current | digital pins; $V_{IN}$ = $V_{CC}$ | [3] | −1.0 | - | +1.0 | µA |
| $I_{IL}$ | LOW-level input current | digital pins; $V_{IN}$ = 0 V | [3] | −1.0 | - | +1.0 | µA |
| $V_{OL}$ | LOW-level output voltage | pins SDA and OS; $I_{OL}$ = 3 mA | | - | - | 0.4 | V |
| | | $I_{OL}$ = 4 mA | | - | - | 0.8 | V |
| $I_{LO}$ | output leakage current | pins SDA and OS; $V_{OH}$ = $V_{CC}$ | | - | - | 10 | µA |
| $V_{POR}$ | power-on reset voltage | $V_{CC}$ supply below which the logic is reset | | 1.0 | - | 2.5 | V |
| OSQ | OS fault queue | programmable | [4] | 1 | - | 6 | |
| $T_{os}$ | overtemperature shutdown threshold | default value | | - | 80 | - | °C |
| $f_{sam}$ | sampling rate | programmable | | 0.125 | 10 | 30 | sample/s |
| $T_{hyst}$ | hysteresis temperature | default value | | - | 75 | - | °C |
| $C_i$ | input capacitance | digital pins | | - | 20 | - | pF |

[1] Typical values are at $V_{CC}$ = 3.3 V and $T_{amb}$ = 25 °C.

[2] Assumes a minimum 11-bit temperature reading.

[3] The digital pins are pin SCL, SDA and A2 to A0.

[4] Device analog-to-digital conversion.

# 12. Dynamic characteristics

**Table 18. Dynamic characteristics[1]**

*$V_{CC}$ = 2.8 V to 5.5 V, $T_{amb}$ = −55 °C to +125 °C; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $T_{CLK}$ | SCL clock period | see Figure 11 | 2.5 | - | - | µs |
| $t_{(SCL)H}$ | HIGH period of the SCL clock | | 0.6 | - | - | µs |
| $t_{(SCL)L}$ | LOW period of the SCL clock | | 1.3 | - | - | µs |
| $t_{HD;STA}$ | hold time (repeated) START condition | | 100 | - | - | ns |
| $t_{SU;DAT}$ | data set-up time | | 100 | - | - | ns |
| $t_{HD;DAT}$ | data hold time | | 0 | - | - | ns |
| $t_{SU;STO}$ | set-up time for STOP condition | | 100 | - | - | ns |
| $t_f$ | fall time | pins SDA and OS; $C_L$ = 400 pF; $I_{OL}$ = 3 mA | - | 250 | - | ns |

[1] These specifications are guaranteed by design and not tested in production.

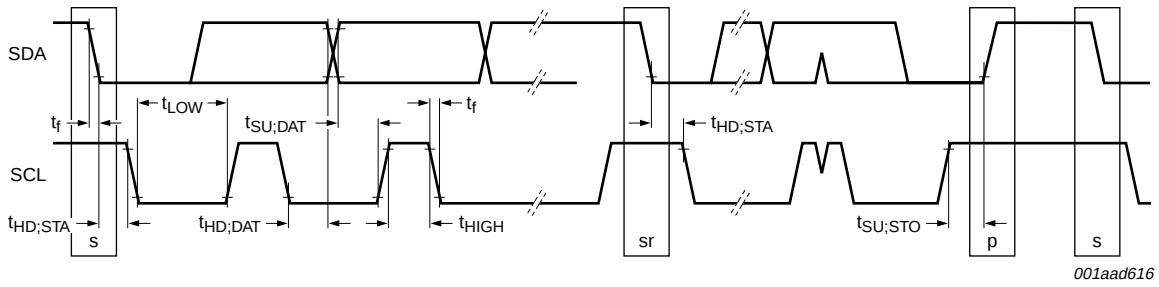



**Fig 11. Timing diagram**

## 13. Performance curves

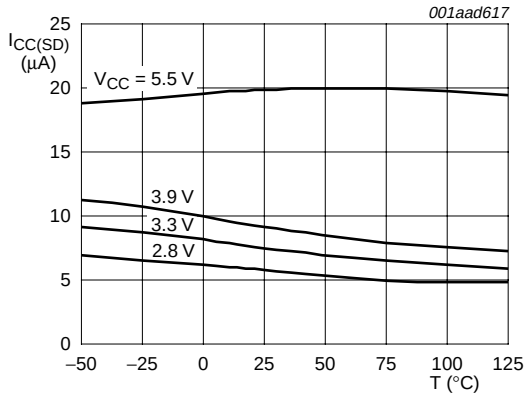



**Fig 12. Shutdown supply current as a function of temperature**

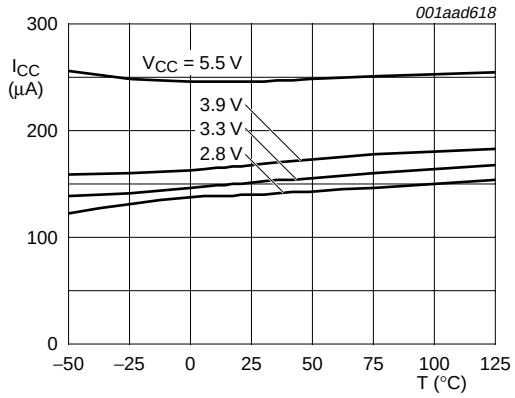



**Fig 13. Typical normal I²C-bus inactive supply current as a function of temperature**

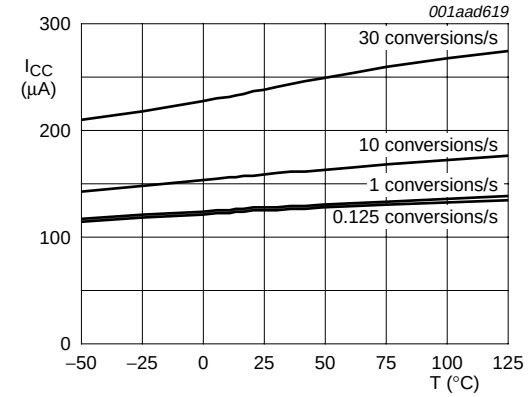



**Fig 14. Typical normal I²C-bus inactive supply current as a function of temperature**

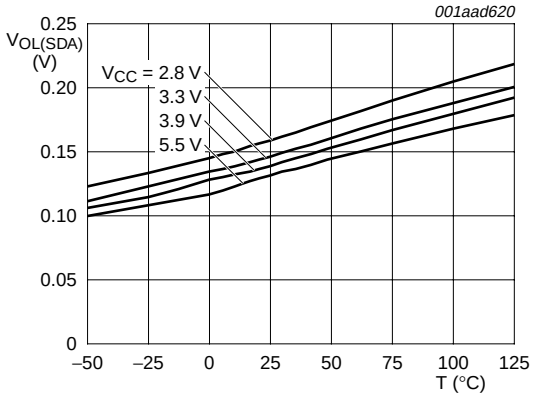



**Fig 15. Typical SDA $V_{OL}$ as a function of temperature**

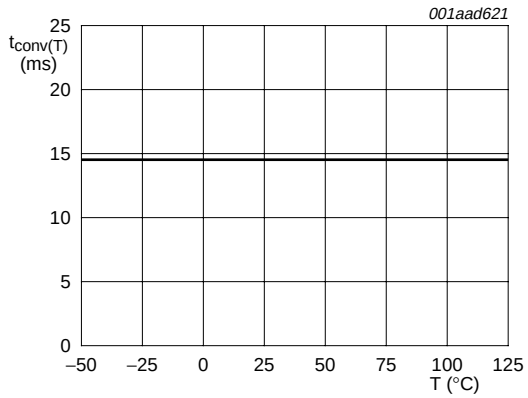



**Fig 16. Typical conversion time as a function of temperature**

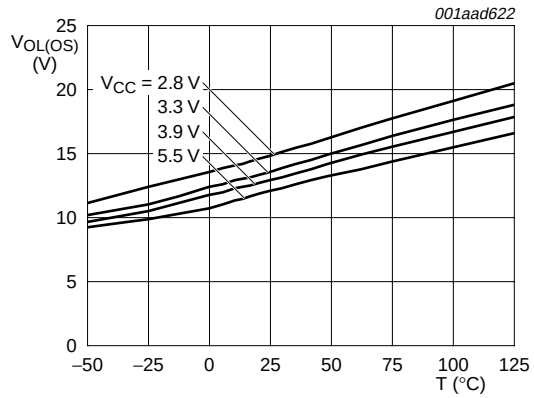



**Fig 17. Typical OS $V_{OL}$ as a function of temperature**

# 14. Application information

The SE95 is sensitive to power supplies with ramp-up time ≤2 ms and could NACK or hang the I²C-bus. In most applications the SE95 will function properly since power supplies have a >2 ms ramp-up time. If the power supply ramp-up time is ≤2 ms, use an RC network with R = 300 Ω and C = 10 µF, as shown in Figure 18, to add about 3 ms to the ramp-up time. The 10 µF capacitor is the same as the bypass capacitor that is typically used to prevent fluctuations on the power supply. The 300 Ω resistor will reduce the supply voltage by about 45 mV since the SE95 supply current is about 150 µA. Ensure the SE95 is the only device connected to the end of 300 Ω resistor since additional devices would draw more current and cause a larger voltage drop across the resistor.

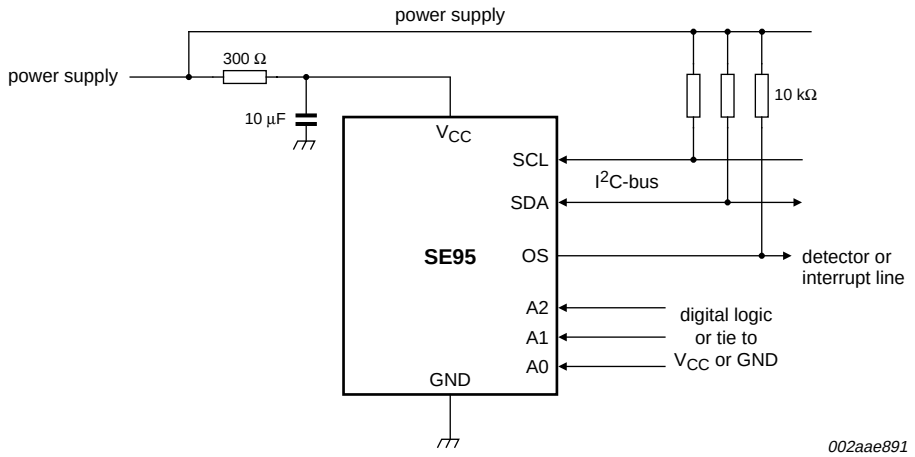
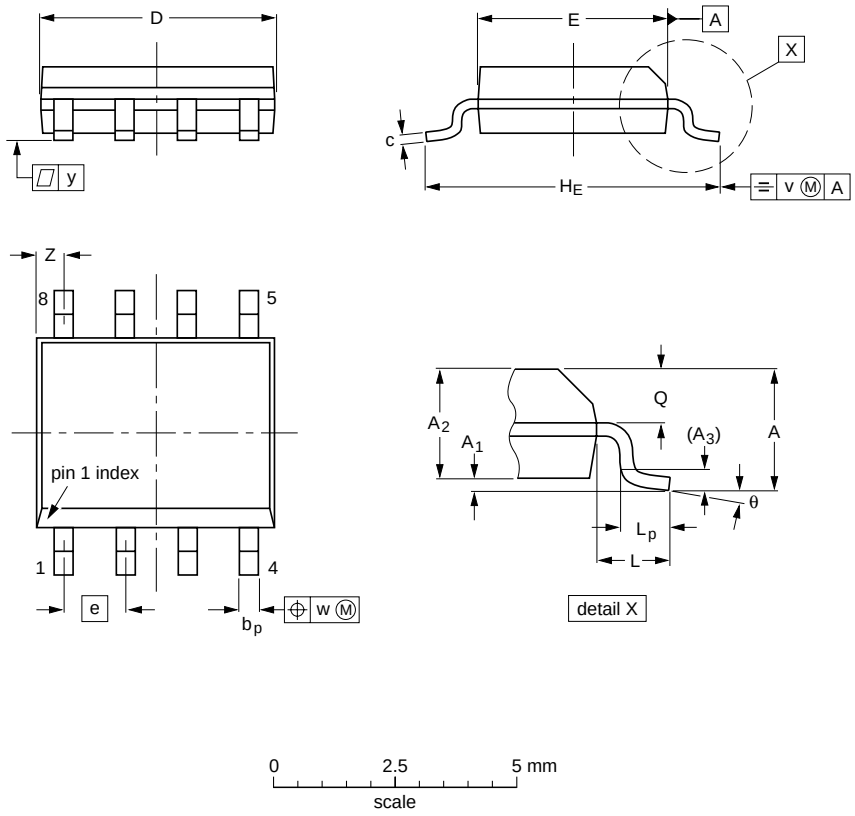



**Fig 18. Typical application circuit**

# 15. Package outline

**SO8: plastic small outline package; 8 leads; body width 3.9 mm** **SOT96-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(2)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.75 | 0.25<br>0.10 | 1.45<br>1.25 | 0.25 | 0.49<br>0.36 | 0.25<br>0.19 | 5.0<br>4.8 | 4.0<br>3.8 | 1.27 | 6.2<br>5.8 | 1.05 | 1.0<br>0.4 | 0.7<br>0.6 | 0.25 | 0.25 | 0.1 | 0.7<br>0.3 | $8^o$<br>$0^o$ |
| inches | 0.069 | 0.010<br>0.004 | 0.057<br>0.049 | 0.01 | 0.019<br>0.014 | 0.0100<br>0.0075 | 0.20<br>0.19 | 0.16<br>0.15 | 0.05 | 0.244<br>0.228 | 0.041 | 0.039<br>0.016 | 0.028<br>0.024 | 0.01 | 0.01 | 0.004 | 0.028<br>0.012 | |

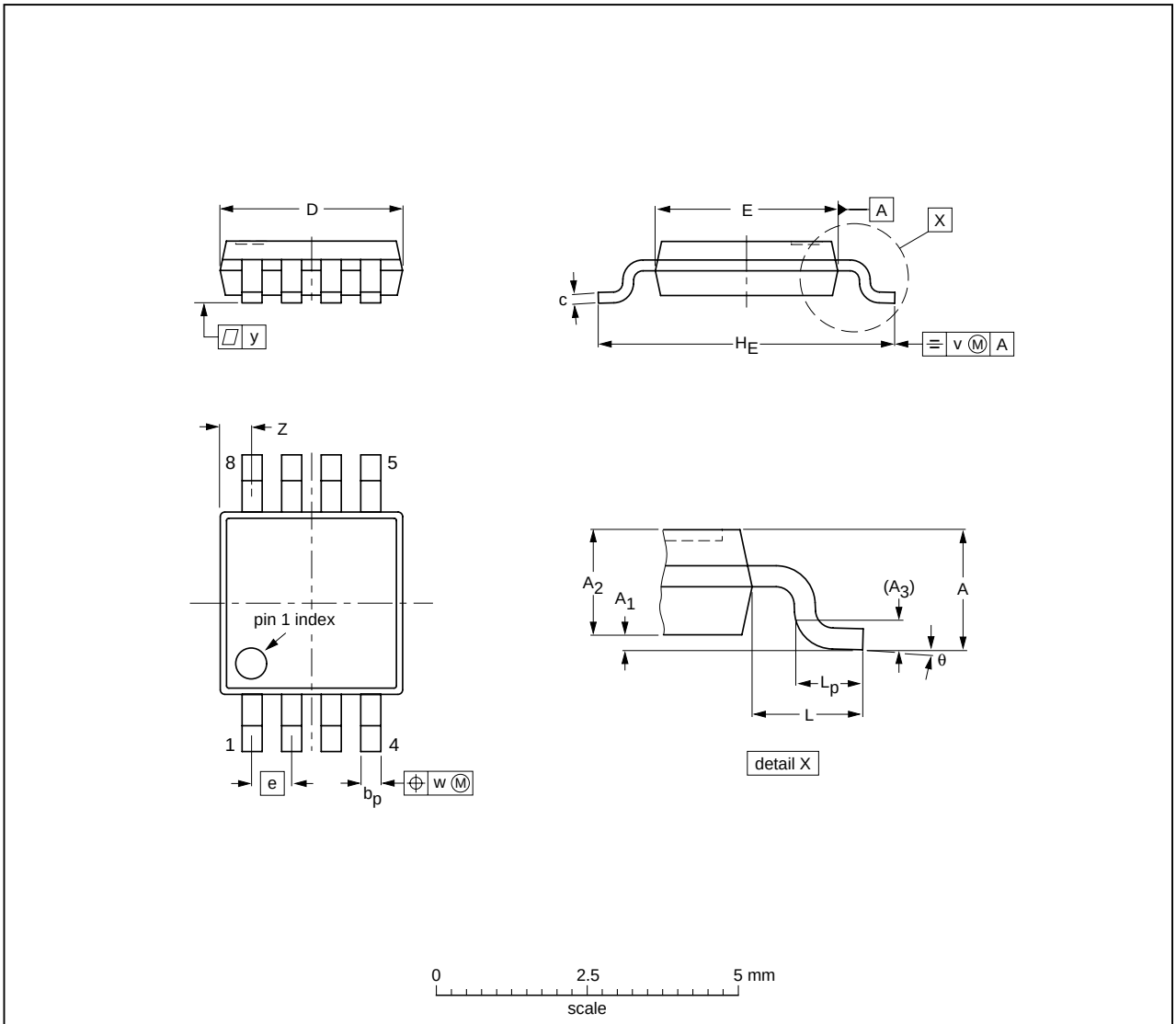
**Notes**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT96-1 | 076E03 | MS-012 | | | | ~~99-12-27~~<br>03-02-18 |

**Fig 19. Package outline SOT96-1 (SO8)**

**TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm** **SOT505-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(2)}$ | e | $H_E$ | L | $L_p$ | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1 | 0.15<br>0.05 | 0.95<br>0.80 | 0.25 | 0.45<br>0.25 | 0.28<br>0.15 | 3.1<br>2.9 | 3.1<br>2.9 | 0.65 | 5.1<br>4.7 | 0.94 | 0.7<br>0.4 | 0.1 | 0.1 | 0.1 | 0.70<br>0.35 | 6°<br>0° |

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT505-1 | | | | | | ~~99-04-09~~<br>03-02-18 |

**Fig 20. Package outline SOT505-1 (TSSOP8)**

# 16. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

## 16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

## 16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

## 16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

## 16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 21) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 19 and 20

**Table 19. SnPb eutectic process (from J-STD-020C)**

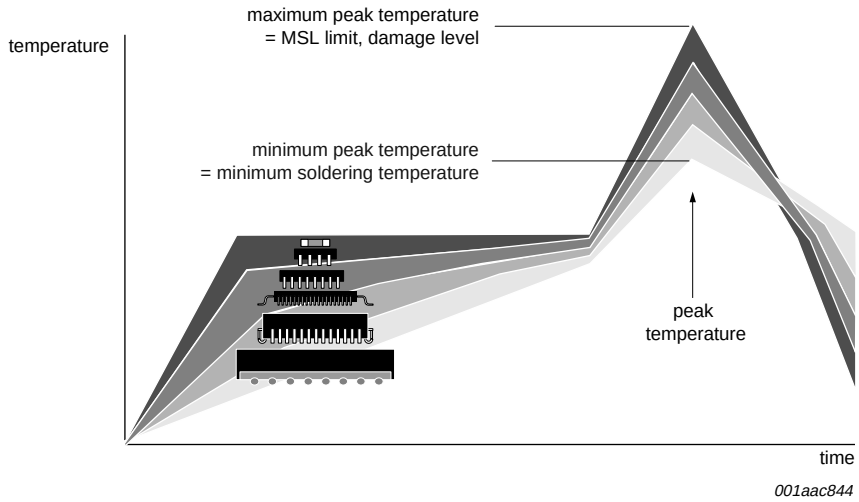
| Package thickness (mm) | Package reflow temperature (°C) | |
|---|---|---|
| | Volume ($mm^3$) | |
| | < 350 | ≥ 350 |
| < 2.5 | 235 | 220 |
| ≥ 2.5 | 220 | 220 |

**Table 20. Lead-free process (from J-STD-020C)**

| Package thickness (mm) | Package reflow temperature (°C) | | |
|---|---|---|---|
| | Volume ($mm^3$) | | |
| | < 350 | 350 to 2000 | > 2000 |
| < 1.6 | 260 | 260 | 260 |
| 1.6 to 2.5 | 260 | 250 | 245 |
| > 2.5 | 250 | 245 | 245 |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 21.




MSL: Moisture Sensitivity Level

**Fig 21. Temperature profiles for large and small components**

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

## 17. Abbreviations

**Table 21. Abbreviations**

| Acronym | Description |
|---|---|
| ADC | Analog-to-Digital Converter |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| $I^2C$-bus | Inter-Integrated Circuit bus |
| I/O | Input/Output |
| LSB | Least Significant Bit |
| LSByte | Least Significant Byte |
| MM | Machine Model |
| MSB | Most Significant Bit |
| MSByte | Most Significant Byte |
| OTP | One-Time Programmable |
| POR | Power-On Reset |
| SMBus | System Management Bus |

## 18. Revision history

**Table 22. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| SE95_7 | 20090902 | Product data sheet | - | SE95_6 |
| Modifications: | • Figure 1 “Block diagram of SE95”: changed from “AVD CONTOL” to “ADC CONTROL”<br>• Section 14 “Application information”:<br>– Added first paragraph<br>– Figure 18 “Typical application circuit” modified<br>• Added soldering information<br>• Added Section 17 “Abbreviations” | | | |
| SE95_6 | 20090604 | Product data sheet | - | SE95_5 |
| SE95_5 | 20071213 | Product data sheet | - | SE95_4 |
| SE95_4 | 20070212 | Product data sheet | - | SE95_3 |
| SE95_3<br>(9397 750 14388) | 20051212 | Product data sheet | - | SE95_2 |
| SE95_2<br>(9397 750 14163) | 20041005 | Objective specification | - | SE95_1 |
| SE95_1<br>(9397 750 10265) | 20031003 | Objective specification | - | - |

# 19. Legal information

## 19.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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## 21. Contents





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