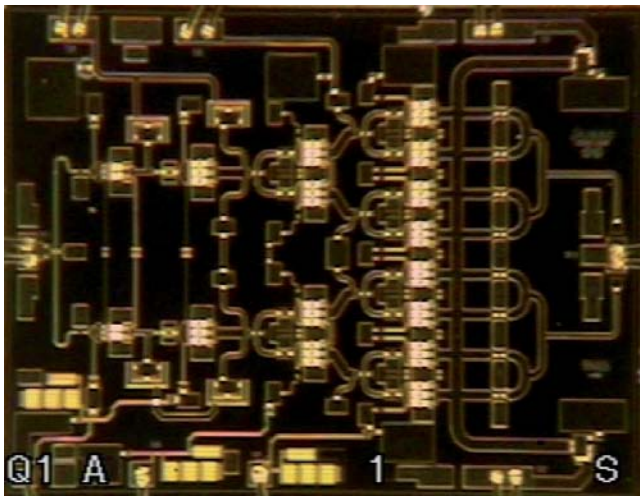
AMMC-6442

37 - 40 GHz 1W Power Amplifier

Data Sheet

Description

The AMMC-6442 is a 1W power amplifier MMIC die for use in transmitters that operate at frequencies between 37GHz and 40GHz. In the operational band, it provides typical 30 dBm of output power (P-1dB) and 23dB of small-signal gain. This MMIC is suitable for high linear applications, with typical performance of 37dBm OIP3 at 18dBm SCL output.



Chip Dimensions

Chip Size: 2650 x 2000 μm (100 x 80 mils)
Chip Size Tolerance: ± 10μm (±0.4 mils)
Chip Thickness: 100 ± 10μm (4 ± 0.4 mils)
Pad Dimensions: 100 x 100 μm (4 x 4 ± 0.4 mils)

Note:
1. This MMIC uses depletion mode pHEMT devices. Negative supply is used for DC gate biasing.

Features

- MMIC die using 4mil thickness
- 1 watt output power
- 50 Ω match on input and output
- ESD protection (50V MM, and 250V HBM)

Typical Performance (Vd=5V, Idsq=0.7A)

- Frequency range 37 to 40 GHz
- Small signal Gain of 23dB
- Output power @P-1 of 30dBm (Typ.)
- Output IP3 37dBm (Typ.) @Po=18dBm
- Input and Output return losses -8dB

Applications

- Point-to-Point Radio systems
- mmW Communications

Attention: Observe Precautions for handling electrostatic sensitive devices.
ESD Machine Model (Class A): 50V
ESD Human Body Model (Class 1A): 250V
Refer to Avago Application Note A004R: Electrostatic Discharge Damage and Control.

Absolute Maximum Ratings[1,2,3,4]

Symbol	Parameters	Unit	Max
V_d	Positive Supply Voltage[2]	V	5.5
V_g	Gate Supply Voltage	V	-2 to 0
P_D	Power Dissipation[2]	W	6
P_{in}	CW Input Power[2]	dBm	20
T_{ch}	Operating Channel Temp.[3,4]	°C	+150
T_{stg}	Storage Case Temp.	°C	-65 to +155
T_{max}	Maximum Assembly Temp (30 sec max)	°C	+260

Note:
1. Operation in excess of any one of these conditions may result in permanent damage to this device.
2. Combinations of supply voltage, drain current, input power, and output power shall not exceed P_D.
3. These ratings apply to each individual FET
4. The operating channel temperature will directly affect the device MTTF. For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.

DC Specifications/ Physical Properties [1]

Symbol	Parameters and Test Conditions	Unit	Min	Typ	Max
$I_{d(q)}$	Drain Supply Current (V_d=5 V, V_g set for $I_{d(q)}$Typical)	mA		700	
V_g	Gate Supply Operating Voltage ($I_{d(q)}$ = 700 (mA))	V	-1.3	-1	-0.7
θ_{ch-bs}	Thermal Resistance (Channel-to-Base Plate)	°C/W		12	
T_{ch}	Channel Temperature	°C		150	

Note:
1. Assume die epoxied to evaluation RF module at 92.25°C base plate temperature.

RF Specifications [1, 2]

T_A= 25°C, V_{dd} = 5.0 V, I_{dq} =0.7 A, V_g = -1V, Z_o=50 Ω

Symbol	Parameters and Test Conditions	Units	Minimum	Typical	Maximum
Freq	Operational Frequency	GHz	37		40
Gain	Small-signal Gain [2]	dB	20	23	
P_{-1dB}	Output Power at 1dB [2] Gain Compression	dBm	28	30	
IM3	Relative third Order Inter-modulation Level Δf=20MHz, Po=+18dBm, SCL	dBc		37	
RL_{in}	Input Return Loss	dB		8	
RL_{out}	Output Return Loss	dB		8	
Isolation	Reverse Isolation	dB		50	

Note:
1. Small/Large -signal data measured at T_A = 25°C.
2. 100% on wafer RF test is done at frequency= 37, 38 and 40GHz.

Typical Performance (Measured data includes approximately 0.2nH bonding wire for RF input and RF output ports.)
(T_A = 25°C, Vdd = 5V, Idq = 0.7 A, V_g = -1 V, Z_{in} = Z_{out} = 50 Ω)

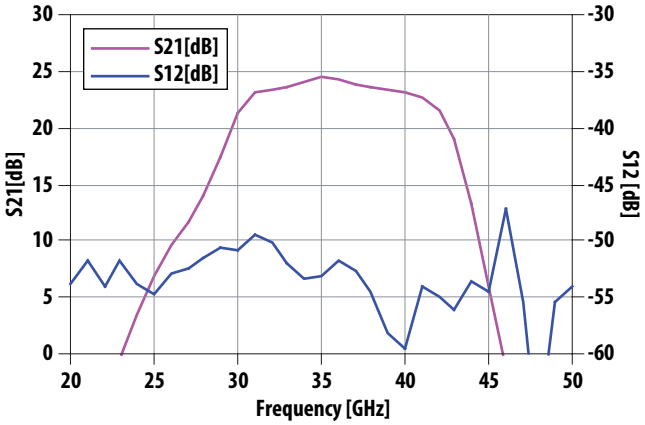


Figure 1. Typical gain and reverse Isolation

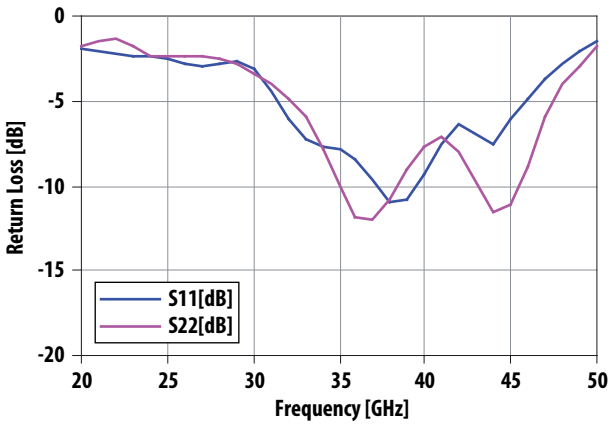


Figure 2. Typical return Loss (input and output)

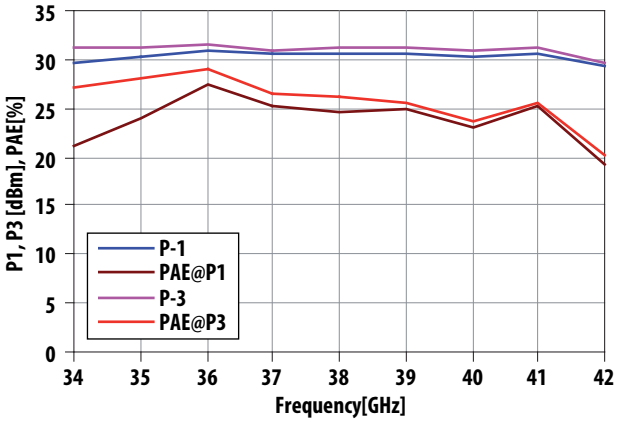


Figure 3. Typical output power (P-1 and P-3) vs. frequency

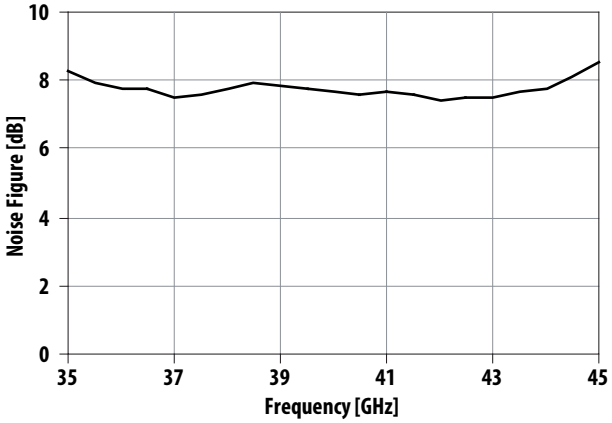


Figure 4. Typical noise figure

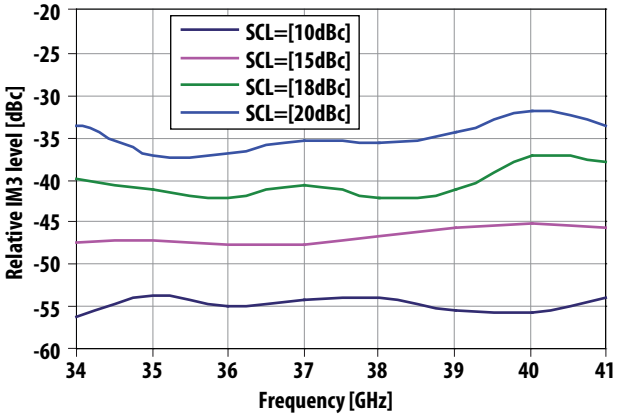


Figure 5. Typical third order inter-modulation product level vs. frequency at different single carrier output level (SCL)

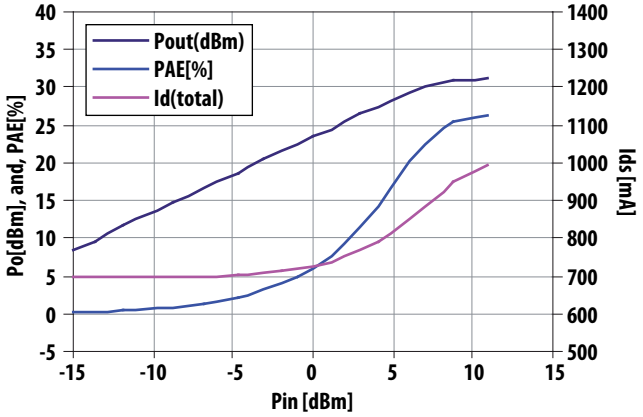


Figure 6. Typical output power, PAE, and drain current versus Input power at 38GHz

Typical over temperature dependencies (This test has been done by a chip-on-module environment.)
(T_A = 25°C, V_{dd} = 5 V, $I_{d(q)}$ = 0.7 A, Z_{in} = Z_{out} = 50 Ω)

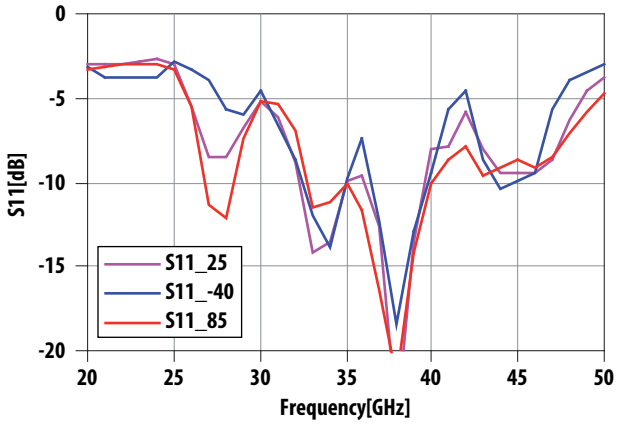


Figure 7. Typical S11 over temperature

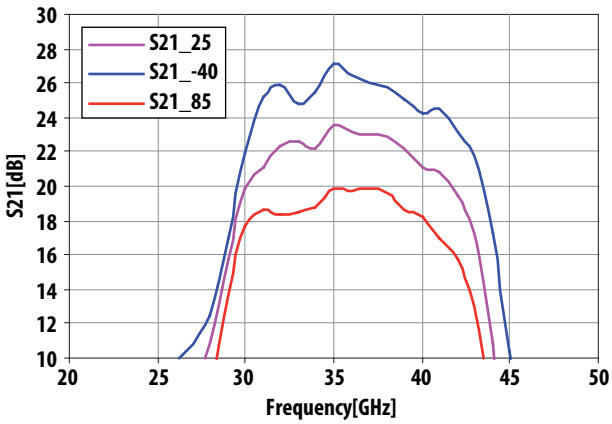


Figure 8. Typical Gain over temperature

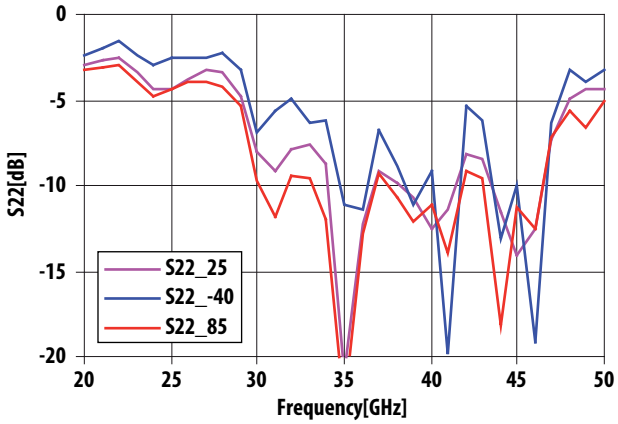


Figure 9. Typical S22 over temperature

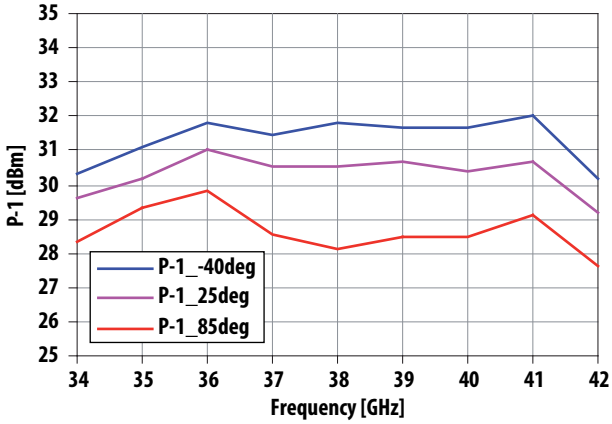


Figure 10. Typical P1 over temperature

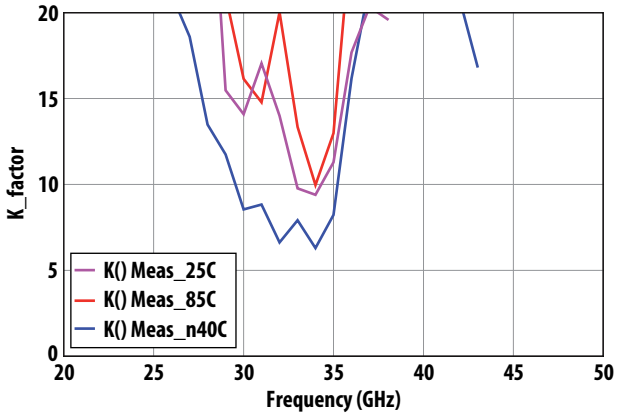


Figure 11. Typical K-factor over temperature

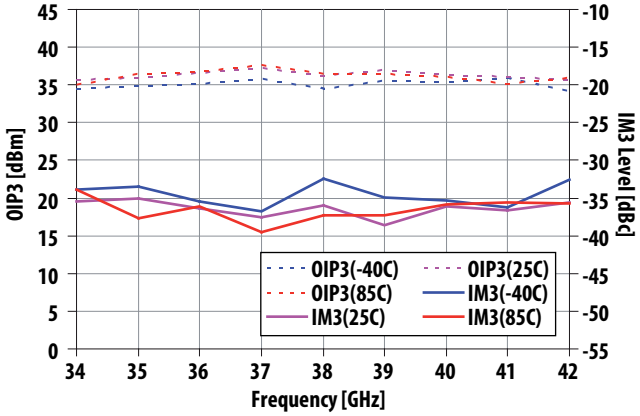


Figure 12. Typical IM3 level over temperature at Po=18dBm, SCL

Typical Scattering Parameters [1], (T_A = 25°C, V_d = 5 V, I_D = 0.7A, Z_{in} = Z_{out} = 50 Ω)

Freq	S11 [dB]	S11 Mag.	S11 Ang.	S21 [dB]	S21 Mag.	S21 Ang.	S12 [dB]	S12 Mag.	S12 Ang.	S22 [dB]	S22 Mag.	S22 Ang.
20	-1.98	0.80	-162.60	-23.67	0.07	-70.83	-53.79	2.04E-03	60.16	-1.76	0.82	42.11
21	-2.10	0.79	-172.27	-15.54	0.17	-118.13	-51.86	2.55E-03	43.77	-1.52	0.84	32.76
22	-2.20	0.78	177.22	-6.91	0.45	-177.73	-54.11	1.97E-03	12.05	-1.29	0.86	20.76
23	-2.35	0.76	164.63	-0.36	0.96	106.90	-51.77	2.58E-03	2.58	-1.72	0.82	7.75
24	-2.43	0.76	152.29	3.51	1.50	35.80	-53.86	2.03E-03	-15.98	-2.37	0.76	-0.32
25	-2.51	0.75	140.18	6.93	2.22	-30.19	-54.72	1.84E-03	-21.05	-2.44	0.76	-8.00
26	-2.79	0.73	127.42	9.58	3.01	-96.01	-52.80	2.29E-03	-30.10	-2.31	0.77	-17.39
27	-2.90	0.72	113.96	11.57	3.79	-156.30	-52.44	2.39E-03	-39.63	-2.38	0.76	-29.13
28	-2.77	0.73	98.12	14.02	5.02	148.66	-51.53	2.65E-03	-44.10	-2.58	0.74	-42.00
29	-2.64	0.74	80.74	17.48	7.48	91.27	-50.63	2.94E-03	-63.53	-2.86	0.72	-55.04
30	-3.06	0.70	60.69	21.20	11.48	23.71	-50.95	2.83E-03	-63.05	-3.43	0.67	-70.00
31	-4.42	0.60	38.62	23.10	14.28	-53.25	-49.48	3.36E-03	-84.29	-4.04	0.63	-86.88
32	-6.02	0.50	24.17	23.31	14.63	-123.77	-50.23	3.08E-03	-114.02	-4.90	0.57	-106.93
33	-7.22	0.44	12.92	23.55	15.04	172.04	-52.01	2.51E-03	-118.15	-5.99	0.50	-131.80
34	-7.75	0.41	-0.90	24.10	16.03	107.61	-53.34	2.15E-03	-145.73	-7.86	0.40	-164.40
35	-7.80	0.41	-17.10	24.48	16.74	40.77	-53.03	2.23E-03	169.78	-10.09	0.31	152.89
36	-8.41	0.38	-45.04	24.21	16.23	-25.74	-51.86	2.55E-03	158.04	-11.90	0.25	108.71
37	-9.59	0.33	-78.60	23.77	15.43	-90.78	-52.60	2.34E-03	131.86	-12.03	0.25	70.77
38	-11.03	0.28	-121.28	23.59	15.12	-154.92	-54.53	1.88E-03	84.13	-10.77	0.29	44.48
39	-10.87	0.29	-167.81	23.47	14.91	137.66	-58.23	1.23E-03	134.51	-9.02	0.35	20.62
40	-9.38	0.34	149.81	23.20	14.45	67.14	-59.62	1.04E-03	80.24	-7.65	0.41	-3.15
41	-7.55	0.42	115.59	22.60	13.49	-7.76	-54.15	1.96E-03	131.10	-7.17	0.44	-31.16
42	-6.41	0.48	85.95	21.52	11.92	-88.85	-54.99	1.78E-03	85.64	-7.97	0.40	-64.60
43	-6.92	0.45	63.21	19.07	8.98	-179.14	-56.12	1.56E-03	157.70	-9.80	0.32	-96.97
44	-7.55	0.42	57.34	13.35	4.65	91.28	-53.62	2.08E-03	124.82	-11.56	0.26	-139.97
45	-6.13	0.49	54.28	6.04	2.00	16.93	-54.40	1.91E-03	120.31	-11.18	0.28	171.25
46	-4.85	0.57	46.36	-1.24	0.87	-45.80	-47.20	4.36E-03	55.90	-8.94	0.36	124.43
47	-3.77	0.65	35.82	-8.39	0.38	-103.32	-55.39	1.70E-03	44.65	-5.98	0.50	91.95
48	-2.83	0.72	26.24	-15.48	0.17	-157.72	-67.79	4.08E-04	-34.88	-4.07	0.63	67.05
49	-2.10	0.78	17.00	-23.02	0.07	150.75	-55.43	1.69E-03	-89.47	-2.90	0.72	46.03
50	-1.44	0.85	7.21	-32.04	0.03	115.26	-53.98	2.00E-03	-1.66	-1.83	0.81	29.63

Note:
1. Data obtained with approximately 0.2nH bonding wire for RF in and RF out ports.

Application and Usage

Recommended quiescent DC bias condition for optimum power and linearity performances is Vd=5 volts with Vg (-1V) set for Id=700 mA. Minor improvements in performance are possible depending on applications. The quiescent drain current range is 500 to 900mA. Muting can be accomplished by setting Vg1, Vg2, and Vg3 to the pinch-off voltage Vp (-2V).

A typical DC bias configuration is shown in Figure 13. Vd3 can be biased from either side. The RF input and output are DC decoupled internally. No ground wires are needed since ground connections are made with plated through-holes to the backside of the device. Figure 14 illustrates a simplified schematic of the AMMC-6442 MMIC.

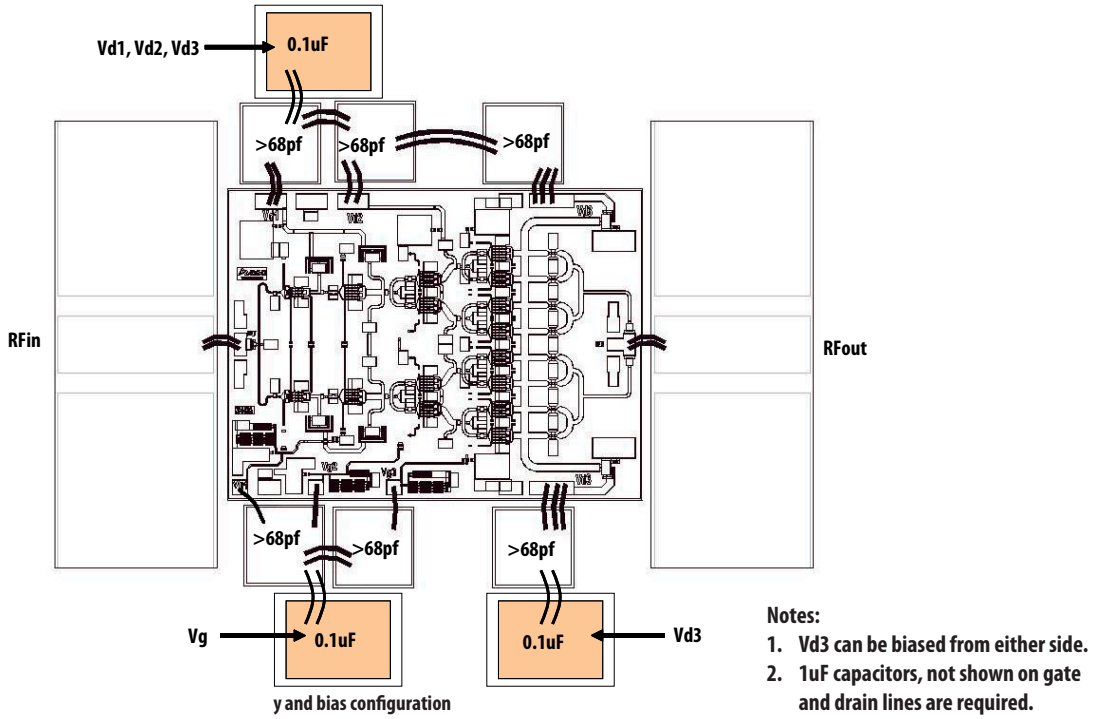


Figure 13. Typical Assembly and bias configuration

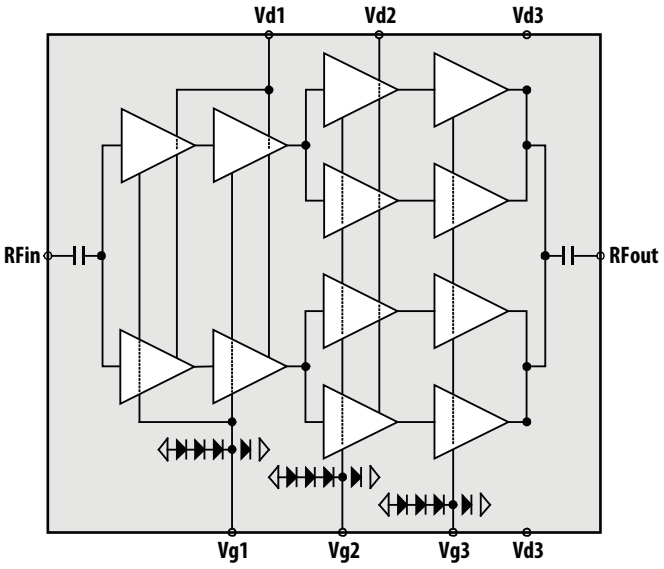


Figure 14. Schematic and recommended assemble example

Note: No RF performance degradation is seen due to ESD up to 250V HBM and 50V MM. The DC characteristics in general show increased leakage at lower ESD discharge voltages. The user is reminded that this device is ESD sensitive and needs to be handled with all necessary ESD protocols.

Recommended Assembly Techniques

The chip should be attached directly to the ground plane using electrically conductive epoxy (Note 1). For conductive epoxy, the amount should be just enough to provide a thin fillet around the bottom perimeter of the die. The ground plane should be free of any residue that may jeopardize electrical or mechanical attachment. Caution should be taken to not exceed the Absolute Maximum Rating for assembly temperature and time.

Thermo-sonic wedge bonding is the preferred method for wire attachment to the bond pads. To optimize performance for this device, the RF connections should be kept at approximately 9mils in length using 1mil gold bond wire. The recommended wire bonding stage temperature is 150±2˚C.

The chip is 100µm thick and should be handled with care. This chip has exposed air bridges on the top surface. Handle at the edges or with a custom collet, (do not pick up die with vacuum on die center).

This MMIC is static sensitive and ESD handling precautions should be taken.

For more detailed information, see Avago Application Note 54 "GaAs MMIC ESD, Die Attach and Bonding Guidelines."

Notes:
1. Sumitomo 1295SA silver epoxy is recommended.
2. Eutectic attach is not recommended any may jeopardize reliability of the device

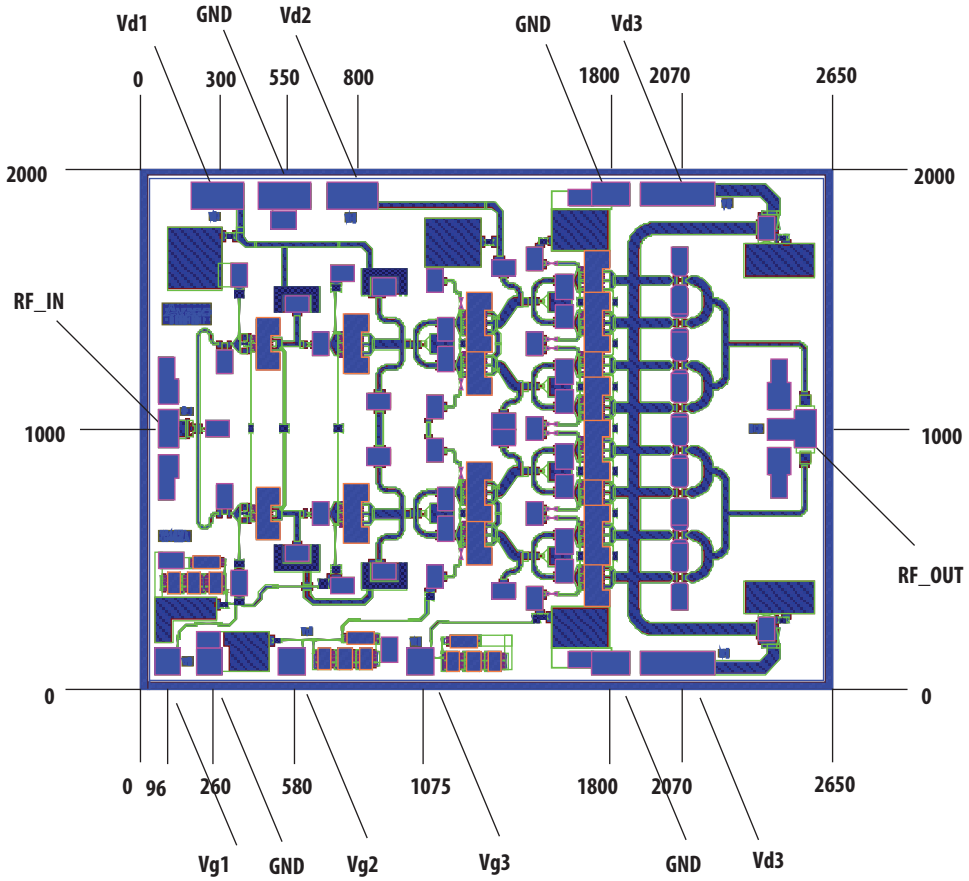


Figure 15. Die dimensions

Ordering Information:

AMMC-6442-W10 = 10 devices per tray
AMMC-6442-W50 = 50 devices per tray

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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