User's Manual

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R8C/3MU Group, R8C/3MK Group

User's Manual: Hardware

RENESAS MCU
R8C Family / R8C/3x Series

Renesas Electronics
www.renesas.com

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the MCU. It is intended for users designing application systems incorporating the MCU. A basic knowledge of electric circuits, logical circuits, and MCUs is necessary in order to use this manual.
The manual comprises an overview of the product; descriptions of the CPU, system control functions, peripheral functions, and electrical characteristics; and usage notes.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the R8C/3MU Group, R8C/3MK Group. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
Datasheet	Hardware overview and electrical characteristics	R8C/3MU Group, R8C/3MK Group Datasheet	R01DS0037EJ0100/ R01DS0038EJ0100
User's manual: Hardware	Hardware specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description Note: Refer to the application notes for details on using peripheral functions.	R8C/3MU Group, R8C/3MK Group User's Manual: Hardware	This User's manual
User's manual: Software	Description of CPU instruction set	R8C/Tiny Series Software Manual	REJ09B0001
Application note	Information on using peripheral functions and application examples Sample programs Information on writing programs in assembly language and C	Available from Renesas Electronics Web site.	
Renesas technical update	Product specifications, updates on documents, etc.		

2. Notation of Numbers and Symbols

The notation conventions for register names, bit names, numbers, and symbols used in this manual are described below.

(1) Register Names, Bit Names, and Pin Names
Registers, bits, and pins are referred to in the text by symbols. The symbol is accompanied by the word “register,” “bit,” or “pin” to distinguish the three categories.
Examples the PM03 bit in the PM0 register
P3_5 pin, VCC pin

(2) Notation of Numbers
The indication “b” is appended to numeric values given in binary format. However, nothing is appended to the values of single bits. The indication “h” is appended to numeric values given in hexadecimal format. Nothing is appended to numeric values given in decimal format.
Examples Binary: 11b
Hexadecimal: EFA0h
Decimal: 1234

3. Register Notation

The symbols and terms used in register diagrams are described below.

x.x.x XXX Register (Symbol)

Address XXXXh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	XXX7	XXX6	XXX5	XXX4	—	—	XXX1	XXX0
After Reset	0	0	0	0	0	0	0	0

*1

Bit	Symbol	Bit Name	Function	R/W
b0	XXX0	XXX bit	b1 b0 0 0: XXX 0 1: XXX 1 0: Do not set. 1 1: XXX	R/W
b1	XXX1			R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b3	—	Reserved bit	Set to 0.	R/W
b4	XXX4	XXX bit	Function varies according to the operating mode.	R/W
b5	XXX5			W
b6	XXX6			R/W
b7	XXX7	XXX bit	0: XXX 1: XXX	R

*2 *3

*1

R/W: Read and write.
R: Read only.
W: Write only.
—: Nothing is assigned.

*2

- Reserved bit

  Reserved bit. Set to specified value.

*3

- Nothing is assigned.

  Nothing is assigned to the bit. As the bit may be used for future functions, if necessary, set to 0.
- Do not set to a value.

  Operation is not guaranteed when a value is set.
- Function varies according to the operating mode.

  The function of the bit varies with the peripheral function mode. Refer to the register diagram for information on the individual modes.

4. List of Abbreviations and Acronyms

Abbreviation	Full Form
ACIA	Asynchronous Communication Interface Adapter
bps	bits per second
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
GSM	Global System for Mobile Communications
Hi-Z	High Impedance
IEBus	Inter Equipment Bus
I/O	Input/Output
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Non-Connection
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
SIM	Subscriber Identity Module
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator

Table of Contents

SFR Page Reference

Address	Register	Symbol	Page
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	36
0005h	Processor Mode Register 1	PM1	183
0006h	System Clock Control Register 0	CM0	112
0007h	System Clock Control Register 1	CM1	113
0008h	Module Standby Control Register	MSTCR	252, 358, 389
0009h	System Clock Control Register 3	CM3	114
000Ah	Protect Register	PRCR	143
000Bh	Reset Source Determination Register	RSTFR	36
000Ch	Oscillation Stop Detection Register	OCD	115
000Dh	Watchdog Timer Reset Register	WDTR	183
000Eh	Watchdog Timer Start Register	WDTS	183
000Fh	Watchdog Timer Control Register	WDTC	184
0010h			
0011h			
0012h			
0013h			
0014h			
0015h	High-Speed On-Chip Oscillator Control Register 7	FRA7	115
0016h			
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	184
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h	High-Speed On-Chip Oscillator Control Register 0	FRA0	116
0024h	High-Speed On-Chip Oscillator Control Register 1	FRA1	116
0025h	High-Speed On-Chip Oscillator Control Register 2	FRA2	117
0026h	On-Chip Reference Voltage Control Register	OCVREFCR	530
0027h			
0028h	Clock Prescaler Reset Flag	CPSRF	117
0029h	High-Speed On-Chip Oscillator Control Register 4	FRA4	118
002Ah	High-Speed On-Chip Oscillator Control Register 5	FRA5	118
002Bh	High-Speed On-Chip Oscillator Control Register 6	FRA6	118
002Ch			
002Dh			
002Eh			
002Fh	High-Speed On-Chip Oscillator Control Register 3	FRA3	118
0030h	Voltage Monitor Circuit Control Register	CMPA	49
0031h	Voltage Monitor Circuit Edge Select Register	VCAC	50
0032h			
0033h	Voltage Detect Register 1	VCA1	50
0034h	Voltage Detect Register 2	VCA2	51, 119
0035h			
0036h	Voltage Detection 1 Level Select Register	VD1LS	52
0037h			
0038h	Voltage Monitor 0 Circuit Control Register	VW0C	53
0039h	Voltage Monitor 1 Circuit Control Register	VW1C	54
003Ah	Voltage Monitor 2 Circuit Control Register	VW2C	55
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			

Address	Register	Symbol	Page
0040h			
0041h	Flash Memory Ready Interrupt Control Register	FMRDYIC	151
0042h			
0043h			
0044h			
0045h			
0046h	INT4 Interrupt Control Register	INT4IC	152
0047h	Timer RC Interrupt Control Register	TRCIC	151
0048h			
0049h	USB RESUME Interrupt Control Register	USBRSMIC	150
004Ah			
004Bh	UART2 Transmit Interrupt Control Register	S2TIC	150
004Ch	UART2 Receive Interrupt Control Register	S2RIC	150
004Dh	Key Input Interrupt Control Register	KUPIC	150
004Eh	A/D Conversion Interrupt Control Register	ADIC	150
004Fh	SSU Interrupt Control Register/IIC bus Interrupt Control Register	SSUIC/IICIC	151
0050h			
0051h	UART0 Transmit Interrupt Control Register	S0TIC	150
0052h	UART0 Receive Interrupt Control Register	S0RIC	150
0053h	UART1 Transmit Interrupt Control Register	S1TIC	150
0054h	UART1 Receive Interrupt Control Register	S1RIC	150
0055h	INT2 Interrupt Control Register	INT2IC	152
0056h	Timer RA Interrupt Control Register	TRAIC	150
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	150
0059h	INT1 Interrupt Control Register	INT1IC	152
005Ah	INT3 Interrupt Control Register	INT3IC	152
005Bh			
005Ch			
005Dh	INT0 Interrupt Control Register	INT0IC	152
005Eh	UART2 Bus Collision Detection Interrupt Control Register	U2BCNIC	150
005Fh			
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh	USB INT Interrupt Control Register	USBINTIC	150
006Ch	UART3 Receive Interrupt Control Register	S3RIC	150
006Dh	UART3 Transmit Interrupt Control Register	S3TIC	150
006Eh			
006Fh			
0070h			
0071h			
0072h	Voltage Monitor 1 Interrupt Control Register	VCMP1IC	150
0073h	Voltage Monitor 2 Interrupt Control Register	VCMP2IC	150
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

Note:
1. The blank regions are reserved. Do not access locations in these regions.

Address	Register	Symbol	Page
0080h	DTC Activation Control Register	DTCTL	195
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h	DTC Activation Enable Register 0	DTCEN0	194
0089h	DTC Activation Enable Register 1	DTCEN1	194
008Ah	DTC Activation Enable Register 2	DTCEN2	194
008Bh	DTC Activation Enable Register 3	DTCEN3	194
008Ch			
008Dh			
008Eh	DTC Activation Enable Register 6	DTCEN6	194
008Fh			
0090h			
0091h			
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h			
0099h			
009Ah			
009Bh			
009Ch			
009Dh			
009Eh			
009Fh			
00A0h	UART0 Transmit/Receive Mode Register	U0MR	301
00A1h	UART0 Bit Rate Register	U0BRG	301
00A2h	UART0 Transmit Buffer Register	U0TB	302
00A3h			
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	303
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	303
00A6h	UART0 Receive Buffer Register	U0RB	304
00A7h			
00A8h	UART2 Transmit/Receive Mode Register	U2MR	324
00A9h	UART2 Bit Rate Register	U2BRG	324
00AAh	UART2 Transmit Buffer Register	U2TB	325
00ABh			
00ACh	UART2 Transmit/Receive Control Register 0	U2C0	326
00ADh	UART2 Transmit/Receive Control Register 1	U2C1	327
00AEh	UART2 Receive Buffer Register	U2RB	328
00AFh			
00B0h	UART2 Digital Filter Function Select Register	URXDF	329
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h			
00B9h			
00BAh			
00BBh	UART2 Special Mode Register 5	U2SMR5	329
00BCh			
00BDh	UART2 Special Mode Register 3	U2SMR3	330
00BEh			
00BFh			

Address	Register	Symbol	Page
00C0h	A/D Register 0	AD0	531
00C1h			
00C2h	A/D Register 1	AD1	531
00C3h			
00C4h	A/D Register 2	AD2	531
00C5h			
00C6h	A/D Register 3	AD3	531
00C7h			
00C8h	A/D Register 4	AD4	531
00C9h			
00CAh	A/D Register 5	AD5	531
00CBh			
00CCh	A/D Register 6	AD6	531
00CDh			
00CEh	A/D Register 7	AD7	531
00CFh			
00D0h			
00D1h			
00D2h			
00D3h			
00D4h	A/D Mode Register	ADMOD	532
00D5h	A/D Input Select Register	ADINSEL	533
00D6h	A/D Control Register 0	ADCON0	534
00D7h	A/D Control Register 1	ADCON1	535
00D8h			
00D9h			
00DAh			
00DBh			
00DCh			
00DDh			
00DEh			
00DFh			
00E0h	Port P0 Register	P0	79
00E1h	Port P1 Register	P1	79
00E2h	Port P0 Direction Register	PD0	78
00E3h	Port P1 Direction Register	PD1	78
00E4h			
00E5h	Port P3 Register	P3	79
00E6h			
00E7h	Port P3 Direction Register	PD3	78
00E8h	Port P4 Register	P4	79
00E9h			
00EAh	Port P4 Direction Register	PD4	78
00EBh			
00ECh	Port P6 Register	P6	79
00EDh	Port P7 Register	P7	79
00EEh	Port P6 Direction Register	PD6	78
00EFh	Port P7 Direction Register	PD7	78
00F0h	Port P8 Register	P8	79
00F1h			
00F2h	Port P8 Direction Register	PD8	78
00F3h			
00F4h			
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00F8h			
00F9h			
00FAh			
00FBh			
00FCh			
00FDh			
00FEh			
00FFh			

Note:
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Address	Register	Symbol	Page
0100h	Timer RA Control Register	TRACR	213
0101h	Timer RA I/O Control Register	TRAIOC	213, 216, 219, 221, 223, 226
0102h	Timer RA Mode Register	TRAMR	214
0103h	Timer RA Prescaler Register	TRAPRE	214
0104h	Timer RA Register	TRA	215
0105h	LIN Control Register 2	LINCR2	425
0106h	LIN Control Register	LINCR	426
0107h	LIN Status Register	LINST	426
0108h	Timer RB Control Register	TRBCR	230
0109h	Timer RB One-Shot Control Register	TRBOCR	230
010Ah	Timer RB I/O Control Register	TRBIOC	231, 234, 238, 241, 245
010Bh	Timer RB Mode Register	TRBMR	231
010Ch	Timer RB Prescaler Register	TRBPRE	232
010Dh	Timer RB Secondary Register	TRBSC	232
010Eh	Timer RB Primary Register	TRBPR	233
010Fh			
0110h			
0111h			
0112h			
0113h			
0114h			
0115h			
0116h			
0117h			
0118h			
0119h			
011Ah			
011Bh			
011Ch			
011Dh			
011Eh			
011Fh			
0120h	Timer RC Mode Register	TRCMR	253
0121h	Timer RC Control Register 1	TRCCR1	254, 275, 284, 290
0122h	Timer RC Interrupt Enable Register	TRCIER	254
0123h	Timer RC Status Register	TRCSR	255
0124h	Timer RC I/O Control Register 0	TRCIOR0	256, 270, 276
0125h	Timer RC I/O Control Register 1	TRCIOR1	256, 271, 277
0126h	Timer RC Counter	TRC	257
0127h			
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0129h			
012Ah	Timer RC General Register B	TRCGRB	257
012Bh			
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012Eh	Timer RC General Register D	TRCGRD	257
012Fh			
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0133h	Timer RC Trigger Control Register	TRCADCR	259
0134h			
0135h			
0136h			
0137h			
0138h			
0139h			
013Ah			
013Bh			
013Ch			
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013Eh			
013Fh			
0140h			
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0159h			
015Ah			
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015Fh			

Note:
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Address	Register	Symbol	Page
0160h	UART1 Transmit/Receive Mode Register	U1MR	301
0161h	UART1 Bit Rate Register	U1BRG	301
0162h	UART1 Transmit Buffer Register	U1TB	302
0163h			
0164h	UART1 Transmit/Receive Control Register 0	U1C0	303
0165h	UART1 Transmit/Receive Control Register 1	U1C1	303
0166h	UART1 Receive Buffer Register	U1RB	304
0167h			
0168h	UART3 Transmit/Receive Mode Register	U3MR	301
0169h	UART3 Bit Rate Register	U3BRG	301
016Ah	UART3 Transmit Buffer Register	U3TB	302
016Bh	UART3 Transmit/Receive Control Register 0	U3C0	303
016Ch	UART3 Transmit/Receive Control Register 1	U3C1	303
016Dh	UART3 Receive Buffer Register	U3RB	304
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016Fh			
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0172h			
0173h			
0174h			
0175h			
0176h			
0177h			
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0190h			
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0192h			
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0195h	SS Transmit Data Register H	SSTDRH	
0196h	SS Receive Data Register L/IIC bus Receive Data Register	SSRDR/ ICDRR	360, 391
0197h	SS Receive Data Register H	SSRDRH	
0198h	SS Control Register H/IIC bus Control Register 1	SSCRH/ ICCR1	360, 392
0199h	SS Control Register L/IIC bus Control Register 2	SSCRL/ ICCR2	361, 393
019Ah	SS Mode Register/IIC bus Mode Register	SSMR/ ICMR	362, 394
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019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			
01B0h			
01B1h			
01B2h	Flash Memory Status Register	FST	565
01B3h			
01B4h	Flash Memory Control Register 0	FMR0	567
01B5h	Flash Memory Control Register 1	FMR1	570
01B6h	Flash Memory Control Register 2	FMR2	572
01B7h			
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			

Address	Register	Symbol	Page
01C0h	Address Match Interrupt Register 0	RMAD0	167
01C1h			
01C2h			
01C3h	Address Match Interrupt Enable Register 0	AIER0	167
01C4h	Address Match Interrupt Register 1	RMAD1	167
01C5h			
01C6h			
01C7h	Address Match Interrupt Enable Register 1	AIER1	167
01C8h			
01C9h			
01CAh			
01CBh			
01CCh			
01CDh			
01CEh			
01CFh			
01D0h			
01D1h			
01D2h			
01D3h			
01D4h			
01D5h			
01D6h			
01D7h			
01D8h			
01D9h			
01DAh			
01DBh			
01DCh			
01DDh			
01DEh			
01DFh			
01E0h	Pull-Up Control Register 0	PUR0	87
01E1h	Pull-Up Control Register 1	PUR1	87
01E2h	Pull-Up Control Register 2	PUR2	88
01E3h			
01E4h			
01E5h			
01E6h			
01E7h			
01E8h			
01E9h			
01EAh			
01EBh			
01ECh			
01EDh			
01EEh			
01EFh			
01F0h	Port P1 Drive Capacity Control Register	P1DRR	89
01F1h			
01F2h	Drive Capacity Control Register 0	DRR0	90
01F3h	Drive Capacity Control Register 1	DRR1	91
01F4h	Drive Capacity Control Register 2	DRR2	92
01F5h	Input Threshold Control Register 0	VLT0	92
01F6h	Input Threshold Control Register 1	VLT1	93
01F7h	Input Threshold Control Register 2	VLT2	93
01F8h	Comparator B Control Register 0	INTCMP	554
01F9h			
01FAh	External Input Enable Register 0	INTEN	161, 554
01FBh	External Input Enable Register 1	INTEN1	161
01FCh	INT Input Filter Select Register 0	INTF	162, 555
01FDh	INT Input Filter Select Register 1	INTF1	162
01FEh	Key Input Enable Register 0	KIEN	165
01FFh			

Address	Register	Symbol	Page
2C00h	DTC Transfer Vector Area		
2C01h	DTC Transfer Vector Area		
2C02h	DTC Transfer Vector Area		
2C03h	DTC Transfer Vector Area		
2C04h	DTC Transfer Vector Area		
2C05h	DTC Transfer Vector Area		
2C06h	DTC Transfer Vector Area		
2C07h	DTC Transfer Vector Area		
2C08h	DTC Transfer Vector Area		
2C09h	DTC Transfer Vector Area		
2C0Ah	DTC Transfer Vector Area		
:	DTC Transfer Vector Area		
:	DTC Transfer Vector Area		
2C3Ah	DTC Transfer Vector Area		
2C3Bh	DTC Transfer Vector Area		
2C3Ch	DTC Transfer Vector Area		
2C3Dh	DTC Transfer Vector Area		
2C3Eh	DTC Transfer Vector Area		
2C3Fh	DTC Transfer Vector Area		
2C40h	DTC Control Data 0	DTCD0	
2C41h			
2C42h			
2C43h			
2C44h			
2C45h			
2C46h			
2C47h			
2C48h	DTC Control Data 1	DTCD1	
2C49h			
2C4Ah			
2C4Bh			
2C4Ch			
2C4Dh			
2C4Eh			
2C4Fh			
2C50h	DTC Control Data 2	DTCD2	
2C51h			
2C52h			
2C53h			
2C54h			
2C55h			
2C56h			
2C57h			
2C58h	DTC Control Data 3	DTCD3	
2C59h			
2C5Ah			
2C5Bh			
2C5Ch			
2C5Dh			
2C5Eh			
2C5Fh			
2C60h	DTC Control Data 4	DTCD4	
2C61h			
2C62h			
2C63h			
2C64h			
2C65h			
2C66h			
2C67h			
2C68h	DTC Control Data 5	DTCD5	
2C69h			
2C6Ah			
2C6Bh			
2C6Ch			
2C6Dh			
2C6Eh			
2C6Fh			

Note:
1. The blank regions are reserved. Do not access locations in these regions.

Address	Register	Symbol	Page
2C70h	DTC Control Data 6	DTCD6	
2C71h			
2C72h			
2C73h			
2C74h			
2C75h			
2C76h			
2C77h			
2C78h	DTC Control Data 7	DTCD7	
2C79h			
2C7Ah			
2C7Bh			
2C7Ch			
2C7Dh			
2C7Eh			
2C7Fh			
2C80h	DTC Control Data 8	DTCD8	
2C81h			
2C82h			
2C83h			
2C84h			
2C85h			
2C86h			
2C87h			
2C88h	DTC Control Data 9	DTCD9	
2C89h			
2C8Ah			
2C8Bh			
2C8Ch			
2C8Dh			
2C8Eh			
2C8Fh			
2C90h	DTC Control Data 10	DTCD10	
2C91h			
2C92h			
2C93h			
2C94h			
2C95h			
2C96h			
2C97h			
2C98h	DTC Control Data 11	DTCD11	
2C99h			
2C9Ah			
2C9Bh			
2C9Ch			
2C9Dh			
2C9Eh			
2C9Fh			
2CA0h	DTC Control Data 12	DTCD12	
2CA1h			
2CA2h			
2CA3h			
2CA4h			
2CA5h			
2CA6h			
2CA7h			
2CA8h	DTC Control Data 13	DTCD13	
2CA9h			
2CAAh			
2CABh			
2CACh			
2CADh			
2CAEh			
2CAFh			

Address	Register	Symbol	Page
2CB0h	DTC Control Data 14	DTCD14	
2CB1h			
2CB2h			
2CB3h			
2CB4h			
2CB5h			
2CB6h			
2CB7h			
2CB8h	DTC Control Data 15	DTCD15	
2CB9h			
2CBAh			
2CBBh			
2CBCh			
2CBDh			
2CBEh			
2CBFh			
2CC0h	DTC Control Data 16	DTCD16	
2CC1h			
2CC2h			
2CC3h			
2CC4h			
2CC5h			
2CC6h			
2CC7h			
2CC8h	DTC Control Data 17	DTCD17	
2CC9h			
2CCAh			
2CCBh			
2CCCh			
2CCDh			
2CCEh			
2CCFh			
2CD0h	DTC Control Data 18	DTCD18	
2CD1h			
2CD2h			
2CD3h			
2CD4h			
2CD5h			
2CD6h			
2CD7h			
2CD8h	DTC Control Data 19	DTCD19	
2CD9h			
2CDAh			
2CDBh			
2CDCh			
2CDDh			
2CDEh			
2CDFh			
2CE0h	DTC Control Data 20	DTCD20	
2CE1h			
2CE2h			
2CE3h			
2CE4h			
2CE5h			
2CE6h			
2CE7h			
2CE8h	DTC Control Data 21	DTCD21	
2CE9h			
2CEAh			
2CEBh			
2CECh			
2CEDh			
2CEEh			
2CEFh			

Note:
1. The blank regions are reserved. Do not access locations in these regions.

Address	Register	Symbol	Page
2CF0h	DTC Control Data 22	DTCD22	
2CF1h			
2CF2h			
2CF3h			
2CF4h			
2CF5h			
2CF6h			
2CF7h			
2CF8h	DTC Control Data 23	DTCD23	
2CF9h			
2CFAh			
2CFBh			
2CFCh			
2CFDh			
2CFEh			
2CFFh			
2D00h			
:			
2DFFh			
2E00h	System Configuration Control Register	SYSCFG	441
2E01h			
2E02h			
2E03h			
2E04h	System Configuration Status Register 0	SYSSTS0	443
2E05h			
2E06h			
2E07h			
2E08h	Device State Control Register 0	DVSTCTR0	444
2E09h			
2E0Ah			
2E0Bh			
2E0Ch			
2E0Dh			
2E0Eh			
2E0Fh			
2E10h			
2E11h			
2E12h			
2E13h			
2E14h	CFIFO Port Register	CFIFO	447
2E15h			
2E16h			
2E17h			
2E18h			
2E19h			
2E1Ah			
2E1Bh			
2E1Ch			
2E1Dh			
2E1Eh			
2E1Fh			
2E20h	CFIFO Port Select Register	CFIFOSEL	448
2E21h			
2E22h	CFIFO Port Control Register	CFIFOCTR	450
2E23h			
2E24h			
2E25h			
2E26h			
2E27h			
2E28h			
2E29h			
2E2Ah			
2E2Bh			
2E2Ch			
2E2Dh			
2E2Eh			
2E2Fh			

Address	Register	Symbol	Page
2E30h	Interrupt Enable Register 0	INTENB0	452
2E31h			
2E32h	Interrupt Enable Register 1	INTENB1	454
2E33h			
2E34h			
2E35h			
2E36h	BRDY Interrupt Enable Register	BRDYENB	456
2E37h			
2E38h	NRDY Interrupt Enable Register	NRDYENB	457
2E39h			
2E3Ah	BEMP Interrupt Enable Register	BEMPENB	458
2E3Bh			
2E3Ch	SOF Output Configuration Register	SOFCFG	459
2E3Dh			
2E3Eh			
2E3Fh			
2E40h	Interrupt Status Register 0	INTSTS0	460
2E41h			
2E42h	Interrupt Status Register 1	INTSTS1	463
2E43h			
2E44h			
2E45h			
2E46h	BRDY Interrupt Status Register	BRDYSTS	466
2E47h			
2E48h	NRDY Interrupt Status Register	NRDYSTS	467
2E49h			
2E4Ah	BEMP Interrupt Status Register	BEMPSTS	468
2E4Bh			
2E4Ch	Frame Number Register	FRMNUM	469
2E4Dh			
2E4Eh			
2E4Fh			
2E50h	USB Address Register	USBADDR	470
2E51h			
2E52h			
2E53h			
2E54h	USB Request Type Register	USBREQ	471
2E55h			
2E56h	USB Request Value Register	USBVAL	472
2E57h			
2E58h	USB Request Index Register	USBINDX	473
2E59h			
2E5Ah	USB Request Length Register	USBLENG	474
2E5Bh			
2E5Ch	DCP Configuration Register	DCPCFG	475
2E5Dh			
2E5Eh	DCP Maximum Packet Size Register	DCPMAXP	476
2E5Fh			
2E60h	DCP Control Register	DCPCTR	477
2E61h			
2E62h			
2E63h			
2E64h	Pipe Window Select Register	PIPESEL	480
2E65h			
2E66h			
2E67h			
2E68h	Pipe Configuration Register	PIPECFG	481
2E69h			
2E6Ah			
2E6Bh			
2E6Ch	Pipe Max Packet Size Register	PIPEMAXP	483
2E6Dh			
2E6Eh	Pipe Period Control Register	PIPEPERI	484
2E6Fh			

Note:
1. The blank regions are reserved. Do not access locations in these regions.

Address	Register	Symbol	Page
2E70h			
2E71h			
2E72h			
2E73h			
2E74h			
2E75h			
2E76h	Pipe 4 Control Register	PIPE4CTR	485
2E77h			
2E78h	Pipe 5 Control Register	PIPE5CTR	485
2E79h			
2E7Ah	Pipe 6 Control Register	PIPE6CTR	485
2E7Bh			
2E7Ch	Pipe 7 Control Register	PIPE7CTR	485
2E7Dh			
2E7Eh			
2E7Fh			
2E80h			
:			
2E8Fh			
2E90h			
2E91h			
2E92h			
2E93h			
2E94h			
2E95h			
2E96h			
2E97h			
2E98h			
2E99h			
2E9Ah			
2E9Bh			
2E9Ch	Pipe 4 Transaction Counter Enable Register	PIPE4TRE	493
2E9Dh			
2E9Eh	Pipe 4 Transaction Counter Register	PIPE4TRN	494
2E9Fh			
2EA0h	Pipe 5 Transaction Counter Enable Register	PIPE5TRE	493
2EA1h			
2EA2h	Pipe 5 Transaction Counter Register	PIPE5TRN	494
2EA3h			
2EA4h			
2EA5h			
2EA6h			
2EA7h			
2EA8h			
2EA9h			
2EAAh			
2EABh			
2EACh			
2EADh			
:			
2ED0h			
2ED1h	Device Address 0 Configuration Register	DEVADD0	495
2ED2h			
2ED3h	Device Address 1 Configuration Register	DEVADD1	495
2ED4h			
2ED5h	Device Address 2 Configuration Register	DEVADD2	495
2ED6h			
2ED7h	Device Address 3 Configuration Register	DEVADD3	495
2ED8h			
2ED9h	Device Address 4 Configuration Register	DEVADD4	495
2EDAh			
2EDBh	Device Address 5 Configuration Register	DEVADD5	495
2EDCh			
2EDDh			
2ED0h			
:			
2EFFh			

Address	Register	Symbol	Page
2F00h	USB Module Control Register	USBMC	496
2F01h	PLL Control Register 0	PLC0	122
2F02h	PLL Control Register 1	PLC1	122
2F03h	PLL Division Control Register	PLDIV	123
2F04h			
2F05h			
2F06h			
2F07h			
2F08h			
2F09h			
2F0Ah			
2F0Bh			
2F0Ch			
2F0Dh			
2F0Eh			
2F0Fh			
2F10h	USB Pin Select Register 0	USBSR0	94
2F11h			
2F12h	UART3 Pin Select Register	U3SR	83, 306
2F13h			
2F14h			
2F15h			
2F16h			
2F17h			
2F18h			
2F19h			
2F1Ah			
2F1Bh			
2F1Ch			
2F1Dh			
2F1Eh			
2F1Fh			
:			
2FFFh			
:			
FFDBh	Option Function Select Register 2	OFS2	38, 179, 186
:			
FFFFh	Option Function Select Register	OFS	37, 56, 178, 185, 563

Note:
1. The blank regions are reserved. Do not access locations in these regions.

1. Overview

1.1 Features

The R8C/3MU Group, R8C/3MK Group of single-chip MCUs incorporates the R8C CPU core, employing sophisticated instructions for a high level of efficiency. With 1 Mbyte of address space, and it is capable of executing instructions at high speed. In addition, the CPU core boasts a multiplier for high-speed operation processing.
Power consumption is low, and the supported operating modes allow additional power control. These MCUs are designed to maximize EMI/EMS performance.
Integration of many peripheral functions, including multifunction timer and serial interface, reduces the number of system components.
The R8C/3MU Group, R8C/3MK Group has data flash (1 KB × 4 blocks) with the background operation (BGO) function.

1.1.1 Applications

Peripherals (USB applicable), audio components, cameras, televisions, household appliances, office equipment, communication devices, mobile devices, industrial equipment, and other applications.

1.1.2 Differences between Groups

Table 1.1 lists the Differences between Groups.
The explanations in the chapters which follow apply to the R8C/3MK Group only. Note the differences shown below.

Table 1.1 Differences between Groups

Item	R8C/3MU Group	R8C/3MK Group
Memory (ROM/RAM)	32 KB/4 KB, 64 KB/8 KB	64 KB/8 KB, 128 KB/10 KB
DTC (Data Transfer Controller)	Activation sources: 25 No DTC activation by A/D conversion interrupt	Activation sources: 26
USB Functions	Peripheral function	Host/peripheral function
A/D Converter	None	Supported

1.1.3 Specifications

Tables 1.2 and 1.3 outline the Specifications for R8C/3MU Group, R8C/3MK Group.

Table 1.2 Specifications for R8C/3MU Group, R8C/3MK Group (1)

Item	Function	Specification
CPU	Central processing unit	R8C CPU core • Number of fundamental instructions: 89 • Minimum instruction execution time: 50 ns (f(XIN) = 20 MHz, VCC = 2.7 to 5.5 V) 200 ns (f(XIN) = 5 MHz, VCC = 1.8 to 5.5 V) • Multiplier: 16 bits × 16 bits → 32 bits • Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits • Operation mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM, RAM, Data flash	Refer to **Table 1.4 Product List for R8C/3MU Group**, and **Table 1.5 Product List for R8C/3MK Group**.
Power Supply Voltage Detection	Voltage detection circuit	• Power-on reset • Voltage detection 3 (detection level of voltage detection 0 and voltage detection 1 selectable)
I/O Ports	Programmable I/O ports	• CMOS I/O ports: 30, selectable pull-up resistor • High current drive ports: 30
Clock	Clock generation circuits	• 4 circuits: XIN clock oscillation circuit, High-speed on-chip oscillator (with frequency adjustment function), Low-speed on-chip oscillator PLL frequency synthesizer • Oscillation stop detection: XIN clock oscillation stop detection function • Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16 • Low power consumption modes: Standard operating mode (XIN clock, PLL frequency synthesizer, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode
Interrupts		• Interrupt Vectors: 69 • External: 9 sources ($\overline{\text{INT}}$ × 5, key input × 4) • Priority levels: 7 levels
Watchdog Timer		• 14 bits × 1 (with prescaler) • Reset start selectable • Low-speed on-chip oscillator for watchdog timer selectable
DTC (Data Transfer Controller)	R8C/3MU Group	• 1 channel • Activation sources: 25 • Transfer modes: 2 (normal mode, repeat mode)
	R8C/3MK Group	• 1 channel • Activation sources: 26 • Transfer modes: 2 (normal mode, repeat mode)
Timer	Timer RA	8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RB	8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timer RC	16 bits × 1 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin)
Serial Interface	UART0, UART1, UART3	Clock synchronous serial I/O/UART × 3 channel
	UART2	Clock synchronous serial I/O, UART, multiprocessor communication function
Synchronous Serial Communication Unit (SSU)		1 (shared with I^2C bus)
I^2C bus		1 (shared with SSU)
LIN Module		Hardware LIN: 1 (timer RA, UART0)

Table 1.3 Specifications for R8C/3MU Group, R8C/3MK Group (2)

Item	Function	Specification
USB Functions	R8C/3MU Group	• USB 2.0 specification compliant, Full speed (12 Mbps) supported • USB function controller and USB transceiver incorporated • 5 pipes provided with individual FIFO Arbitrary EP numbers can be specified for PIPE4 to 7 • FIFO size (total 448 bytes: DCP (EP0) = 64 bytes, PIPE4 and PIPE5 = 128 bytes (64-byte double buffer), PIPE6 and PIPE7 = 64 bytes • Supported transfer: DCP = Control transfer IN/OUT, PIPE4 and PIPE5 = Bulk transfer IN/OUT, PIPE6 and PIPE7 = Interrupt transfer IN/OUT
	R8C/3MK Group	• USB 2.0 specification compliant, Full speed (12 Mbps) supported • USB Device Controller (UDC), transceiver for USB2.0 are incorporated, and on-chip USB transceiver • 5 pipes provided with individual FIFO Arbitrary EP numbers can be specified for PIPE4 to 7 • FIFO size (total 448 bytes): DCP (EP0) = 64 bytes, PIPE4 and PIPE5 = 128 bytes (64-byte double buffer), PIPE6 and PIPE7 = 64 bytes • Supported transfer: DCP = Control transfer IN/OUT, PIPE4 and PIPE5 = Bulk transfer IN/OUT, PIPE6 and PIPE7 = Interrupt transfer IN/OUT • When the host controller is selected Automatic scheduling for SOF and packet transmissions Programmable intervals for interrupt transfers
A/D Converter (1)		10-bit resolution × 10 channels, includes sample and hold function, with sweep mode
Comparator B		2 circuits
Flash Memory		• Programming and erasure voltage: VCC = 2.7 to 5.5 V • Programming and erasure endurance: 10,000 times (data flash) 1,000 times (program ROM) • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function • Background operation (BGO) function (data flash)
Operating Frequency/Supply Voltage		f(XIN) = 20 MHz (VCC = 2.7 to 5.5 V)(USB not used) f(XIN) = 5 MHz (VCC = 1.8 to 5.5 V)(USB not used)
Current consumption		Typ. 7.0 mA (VCC = 5.0 V, f(XIN) = 20 MHz) Typ. 3.5 mA (VCC = 3.0 V, f(XIN) = 10 MHz) Typ. 4.0 μA (VCC = 3.0 V, wait mode) Typ. 2.0 μA (VCC = 3.0 V, stop mode)
Operating Ambient Temperature		−20 to 85°C (N version)
Package		40-pin QFN Package code: PWQN0040KB-B (previous code: 40PJS-B)

Note:
1. Not available in the R8C/3MU Group.

1.2 Product List

Tables 1.4 and 1.5 list Product List for Each Group. Figures 1.1 and 1.2 show a Part Number, Memory Size, and Package of Each Group.

Table 1.4 Product List for R8C/3MU Group **Current of May 2011**

Part No.	ROM Capacity		RAM Capacity	Package Type	Remarks	
	Program ROM	Data flash				
R5F213M6UNNP	32 Kbytes	1 Kbyte × 4	4 Kbytes	PWQN0040KB-B	N version	
R5F213M8UNNP	64 Kbytes	1 Kbyte × 4	8 Kbytes	PWQN0040KB-B		
R5F213M6UNXXXNP	32 Kbytes	1 Kbyte × 4	4 Kbytes	PWQN0040KB-B	N version	Factory programming product (1)
R5F213M8UNXXXNP	64 Kbytes	1 Kbyte × 4	8 Kbytes	PWQN0040KB-B		

Note:
1. The user ROM is programmed before shipment.

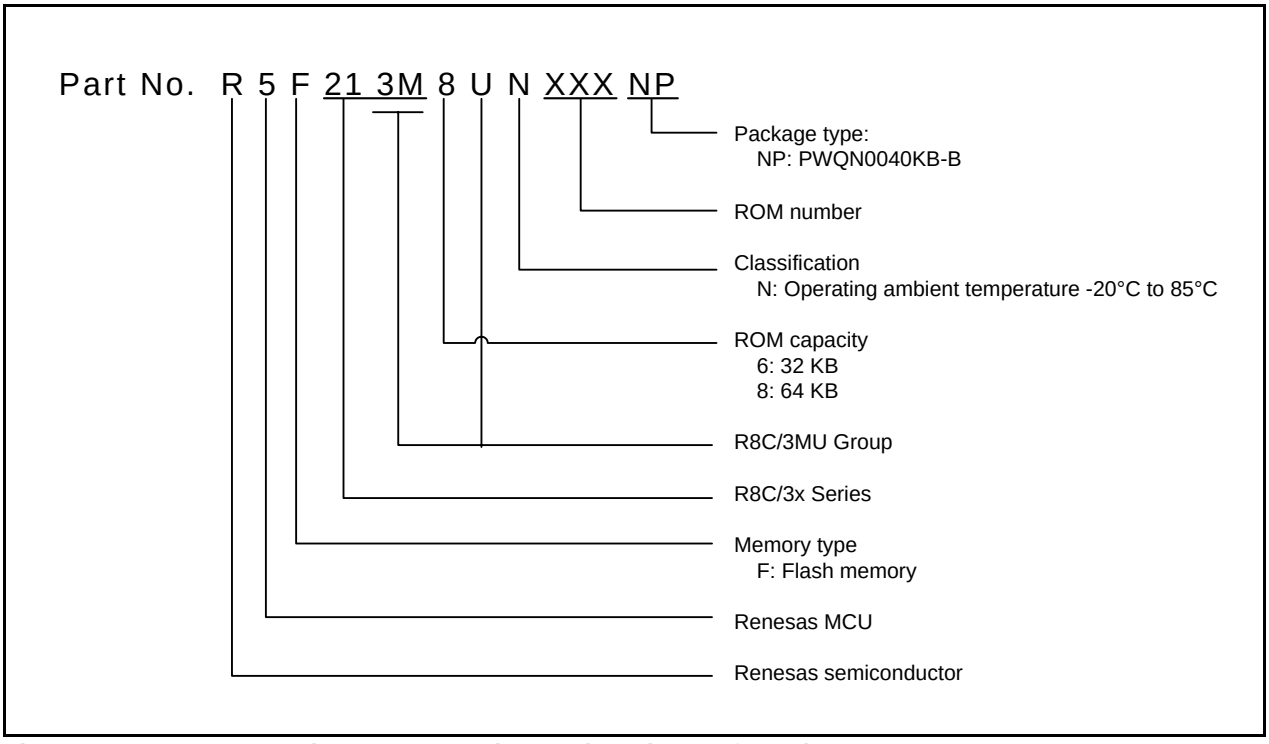


Figure 1.1 Part Number, Memory Size, and Package of R8C/3MU Group

Table 1.5 Product List for R8C/3MK Group **Current of May 2011**

Part No.	ROM Capacity		RAM Capacity	Package Type	Remarks	
	Program ROM	Data flash				
R5F213M8KNNP	64 Kbytes	1 Kbyte × 4	8 Kbytes	PWQN0040KB-B	N version	
R5F213MCKNNP	128Kbytes	1 Kbyte × 4	10 Kbytes	PWQN0040KB-B		
R5F213M8KNXXXNP	64Kbytes	1 Kbyte × 4	8 Kbytes	PWQN0040KB-B	N version	Factory programming product (1)
R5F213MCKNXXXNP	128Kbytes	1 Kbyte × 4	10 Kbytes	PWQN0040KB-B		

Note:
1. The user ROM is programmed before shipment.

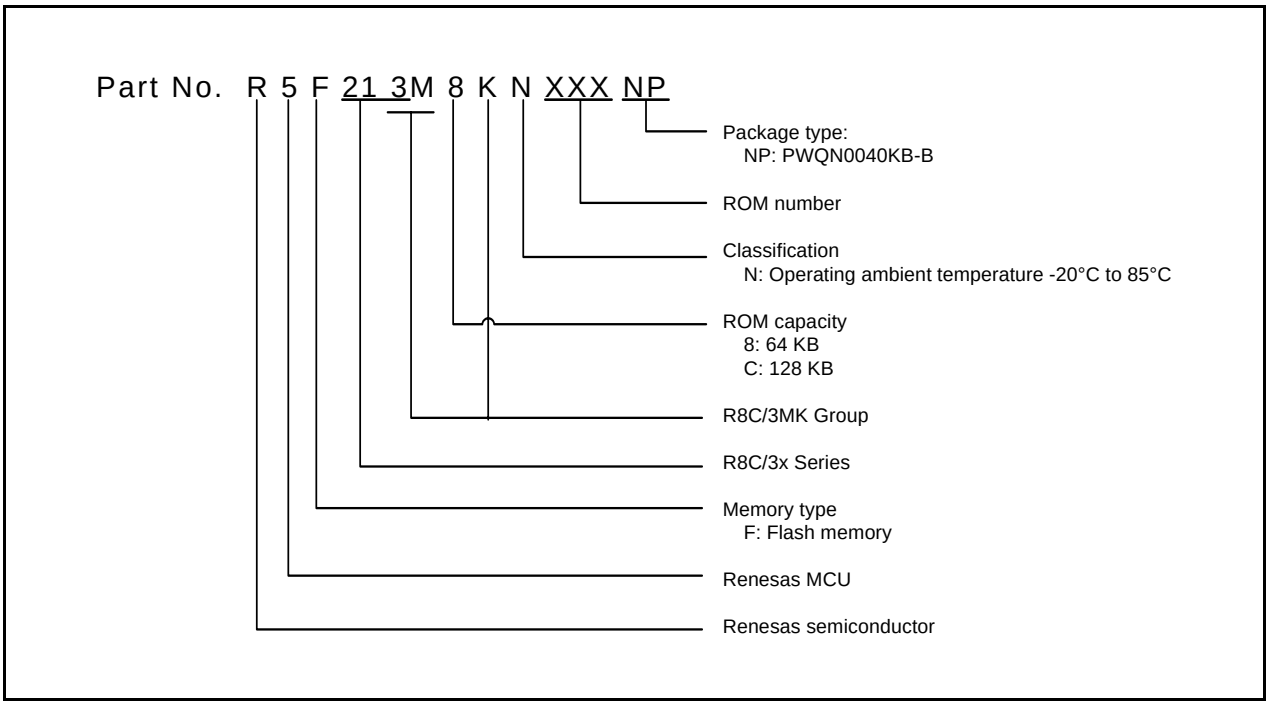


Figure 1.2 Part Number, Memory Size, and Package of R8C/3MK Group

1.3 Block Diagram

Figures 1.3 and 1.4 show Block Diagram of Each Group.

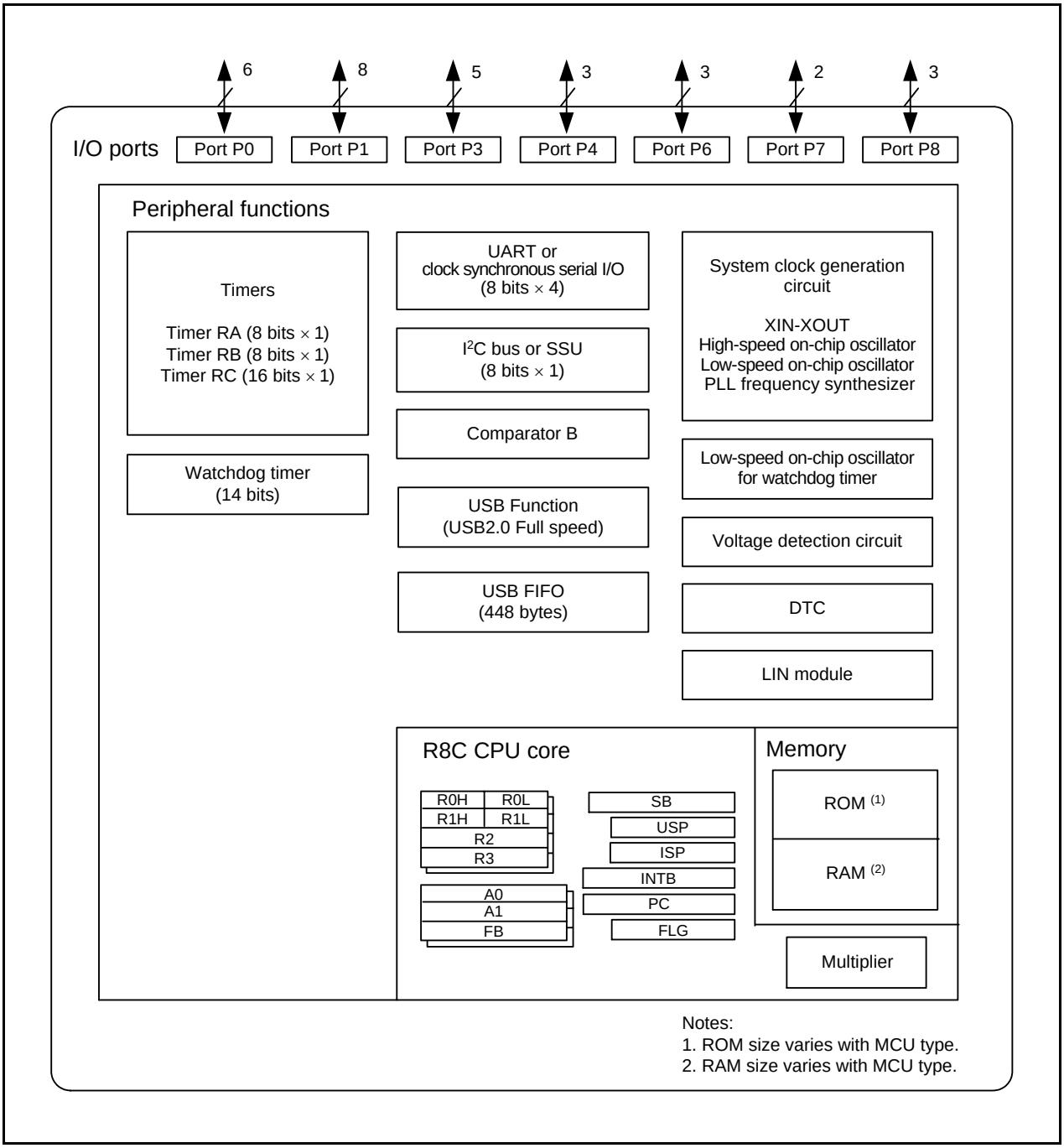


Figure 1.3 Block Diagram of R8C/3MU Group

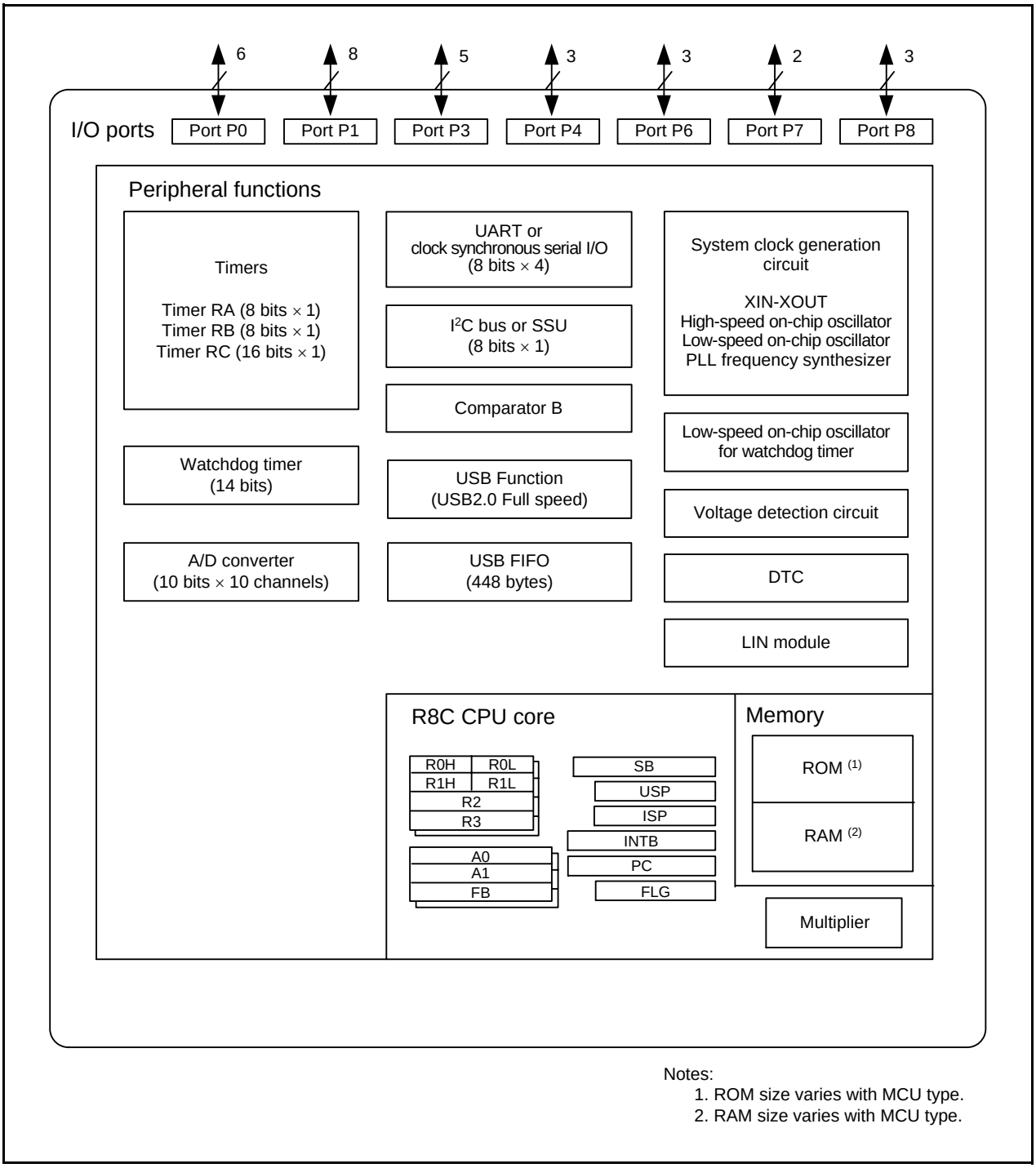
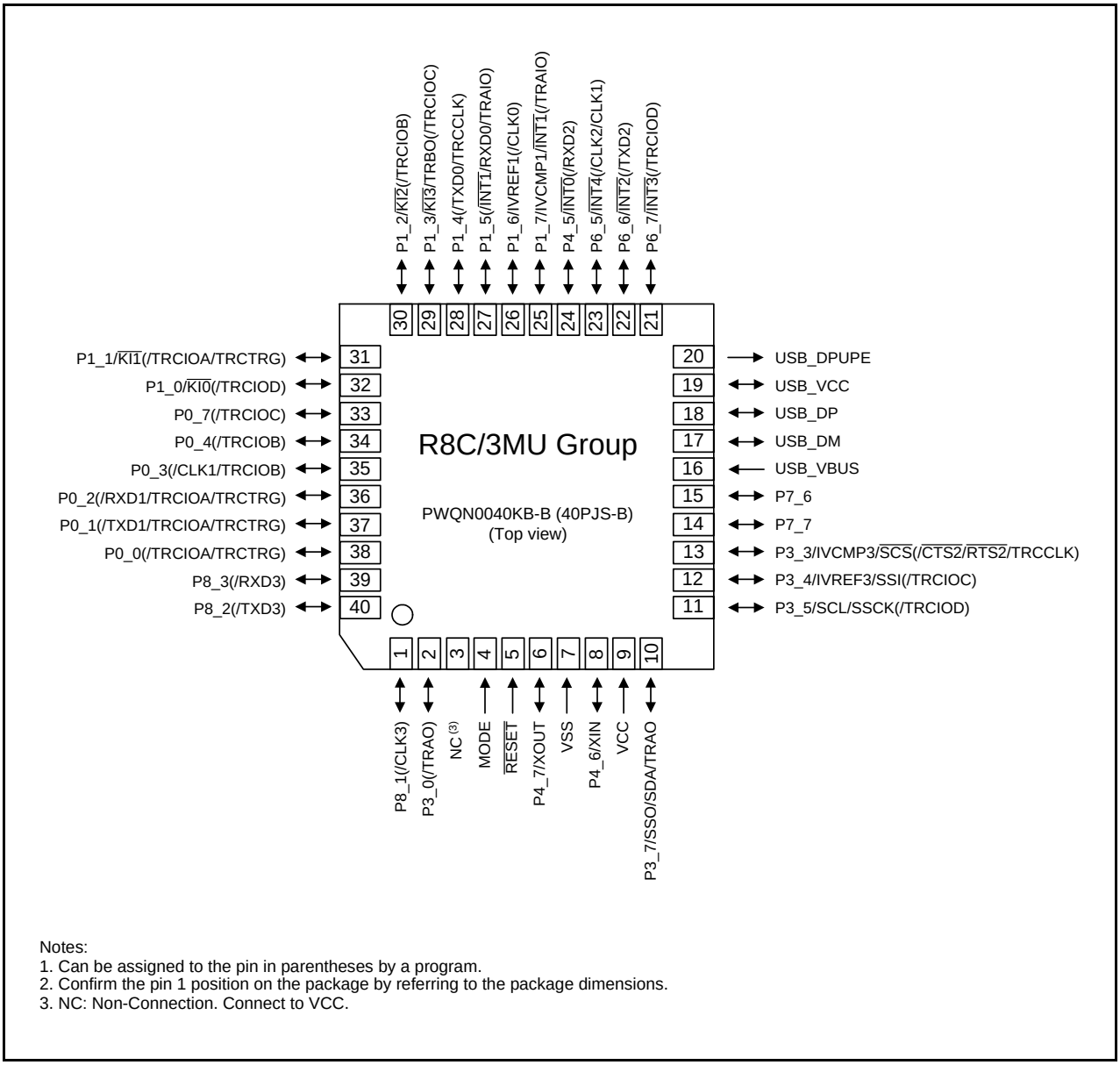


Figure 1.4 Block Diagram of R8C/3MK Group

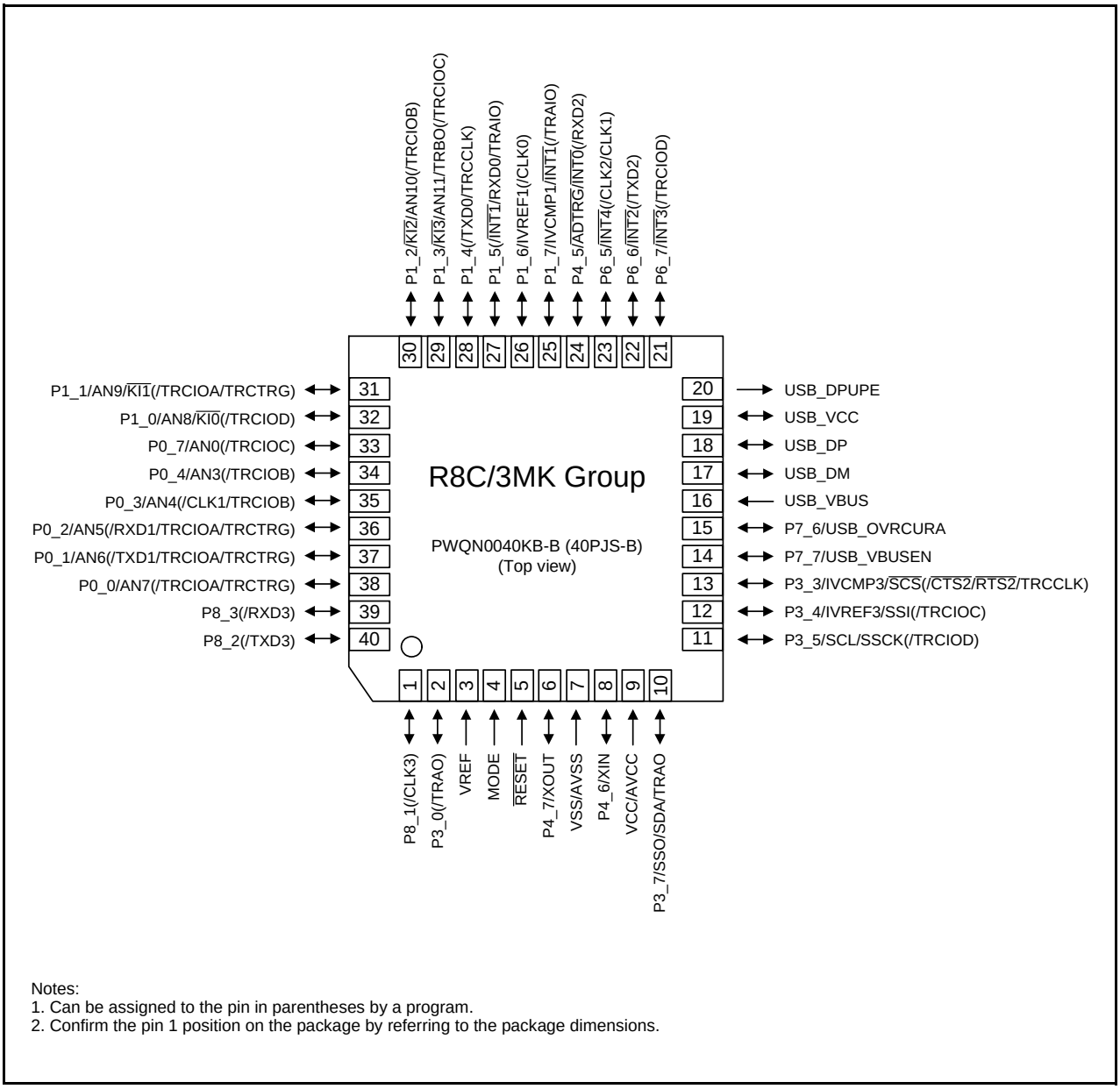
1.4 Pin Assignment

Figures 1.5 and 1.6 show Pin Assignment (Top View) of Each Group. Table 1.6 outlines the Pin Name Information by Pin Number.



Notes:
1. Can be assigned to the pin in parentheses by a program.
2. Confirm the pin 1 position on the package by referring to the package dimensions.
3. NC: Non-Connection. Connect to VCC.

Figure 1.5 Pin Assignment (Top View) of R8C/3MU Group



Notes:
1. Can be assigned to the pin in parentheses by a program.
2. Confirm the pin 1 position on the package by referring to the package dimensions.

Figure 1.6 Pin Assignment (Top View) of R8C/3MK Group

Table 1.6 Pin Name Information by Pin Number

Pin Number	Control Pin	Port	I/O Pin Functions for Peripheral Modules						
			Interrupt	Timer	Serial Interface	SSU	I^2C bus	USB	A/D Converter, Comparator B
1		P8_1			(CLK3)				
2		P3_0		(TRAO)					
3									VREF (2)
4	MODE								
5	$\overline{\text{RESET}}$								
6	XOUT	P4_7							
7	VSS/ AVSS (2)								
8	XIN	P4_6							
9	VCC/ AVCC (2)								
10		P3_7		TRAO		SSO	SDA		
11		P3_5		(TRCIOD)		SSCK	SCL		
12		P3_4		(TRCIOC)		SSI			IVREF3
13		P3_3		(TRCCLK)	($\overline{\text{CTS2}}$/ $\overline{\text{RTS2}}$)	$\overline{\text{SCS}}$			IVCMP3
14		P7_7						USB_VBUSEN (2)	
15		P7_6						USB_OVRCURA (2)	
16								USB_VBUS	
17								USB_DM	
18								USB_DP	
19								USB_VCC	
20								USB_DPUPE	
21		P6_7	$\overline{\text{INT3}}$	(TRCIOD)					
22		P6_6	$\overline{\text{INT2}}$		(TXD2)				
23		P6_5	$\overline{\text{INT4}}$		(CLK2/ CLK1)				
24		P4_5	$\overline{\text{INT0}}$		(RXD2)				$\overline{\text{ADTRG}}$ (2)
25		P1_7	$\overline{\text{INT1}}$	(TRAIO)					IVCMP1
26		P1_6			(CLK0)				IVREF1
27		P1_5	($\overline{\text{INT1}}$)	(TRAIO)	(RXD0)				
28		P1_4		(TRCCLK)	(TXD0)				
29		P1_3	$\overline{\text{KI3}}$	TRBO (/TRCIOC)					AN11 (2)
30		P1_2	$\overline{\text{KI2}}$	(TRCIOB)					AN10 (2)
31		P1_1	$\overline{\text{KI1}}$	(TRCIOA/ TRCTRG)					AN9 (2)
32		P1_0	$\overline{\text{KI0}}$	(TRCIOD)					AN8 (2)
33		P0_7		(TRCIOC)					AN0 (2)
34		P0_4		(TRCIOB)					AN3 (2)
35		P0_3		(TRCIOB)	(CLK1)				AN4 (2)
36		P0_2		(TRCIOA/ TRCTRG)	(RXD1)				AN5 (2)
37		P0_1		(TRCIOA/ TRCTRG)	(TXD1)				AN6 (2)
38		P0_0		(TRCIOA/ TRCTRG)					AN7 (2)
39		P8_3			(RXD3)				
40		P8_2			(TXD3)				

Notes:
1. Can be assigned to the pin in parentheses by a program.
2. This pin is not available in the R8C/3MU Group.

1.5 Pin Functions

Tables 1.7 and 1.8 list Pin Functions.

Table 1.7 Pin Functions (1)

Item	Pin Name	I/O Type	Description
Power supply input	VCC, VSS	—	Apply 1.8 to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS (2)	—	Power supply for the A/D converter. Connect a capacitor between AVCC and AVSS.
Reset input	$\overline{\text{RESET}}$	I	Input “L” on this pin resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
XIN clock input	XIN	I	These pins are provided for XIN clock generation circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins. (1) To use an external clock, input it to the XOUT pin and leave the XIN pin open.
XIN clock output	XOUT	I/O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT4}}$	I	$\overline{\text{INT}}$ interrupt input pins.
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Key input interrupt input pins.
Timer RA	TRAIO	I/O	Timer RA I/O pin.
	TRAO	O	Timer RA output pin.
Timer RB	TRBO	O	Timer RB output pin.
Timer RC	TRCCLK	I	External clock input pin.
	TRCTRG	I	External trigger input pin.
	TRCIOA, TRCIOB, TRCIOC, TRCIOD	I/O	Timer RC I/O pins.
Serial interface	CLK0, CLK1, CLK2, CLK3	I/O	Transfer clock I/O pins.
	RXD0, RXD1, RXD2, RXD3	I	Serial data input pins.
	TXD0, TXD1, TXD2, TXD3	O	Serial data output pins.
	$\overline{\text{CTS2}}$	I	Transmission control input pin.
	$\overline{\text{RTS2}}$	O	Reception control output pin.
SSU	SSI	I/O	Data I/O pin.
	$\overline{\text{SCS}}$	I/O	Chip-select signal I/O pin.
	SSCK	I/O	Clock I/O pin.
	SSO	I/O	Data I/O pin.
I^2C bus	SCL	I/O	Clock I/O pin.
	SDA	I/O	Data I/O pin.

I: Input O: Output I/O: Input and output

Notes:

1. Refer to the oscillator manufacturer for oscillation characteristics.
2. This pin is not available in the R8C/3MU Group.

Table 1.8 Pin Functions (2)

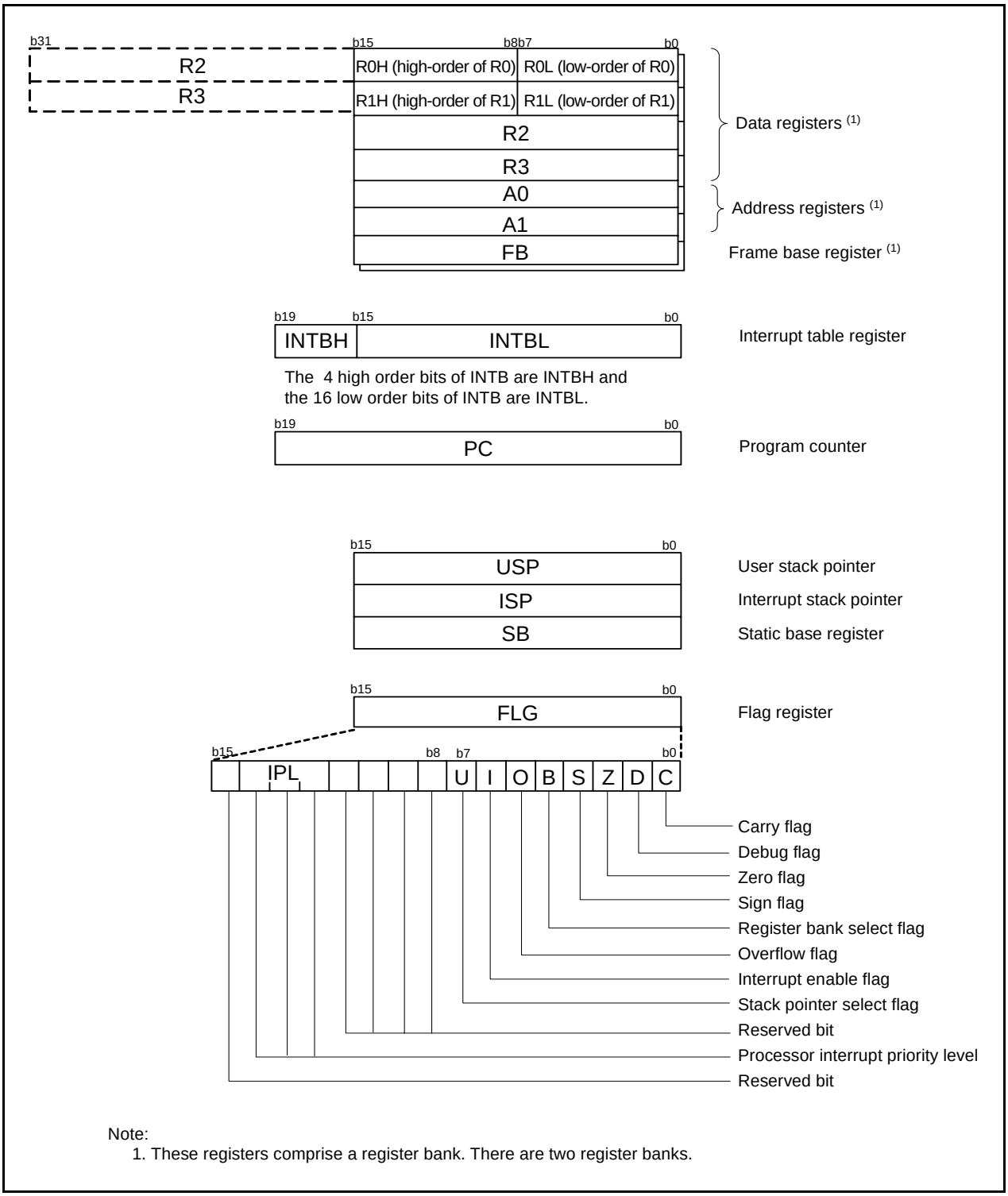
Item	Pin Name	I/O Type	Description
USB	USB_DP/USB_DM	I/O	D+/D- I/O pin of the USB on-chip transceiver. Connect this pin to the D+/D- pin of the USB bus.
	USB_VBUS	I	USB cable connection monitor pin. Connect this pin to VBUS of the USB bus. Whether VBUS is connected or disconnected can be detected during operation as a function.
	USB_VBUSEN (1)	O	VBUS (5 V) supply enable signal for external power supply chip.
	USB_OVRCURA (1)	I	External overcurrent detection signal should be connected to this pin. VBUS comparator signal should be connected to this pin when the USB host power supply chip is connected.
	USB_DPUPE	O	1.5 kΩ pull-up resistor control signal for USB D+ signal when operating as a function controller.
	USB_VCC	I/O	USB power supply pin.
Reference voltage input	VREF (1)	I	Reference voltage input pin to A/D converter.
A/D converter	AN0, AN3 to AN11 (1)	I	Analog input pins to A/D converter.
	$\overline{\text{ADTRG}}$ (1)	I	AD external trigger input pin.
Comparator B	IVCMP1, IVCMP3	I	Comparator B analog voltage input pins.
	IVREF1, IVREF3	I	Comparator B reference voltage input pins.
I/O port	P0_0 to P0_4, P0_7, P1_0 to P1_7, P3_0, P3_3 to P3_5, P3_7, P4_5 to P4_7, P6_5 to P6_7, P7_6, P7_7, P8_1 to P8_3	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program.

I: Input O: Output I/O: Input and output

Note:
1. This pin is not available in the R8C/3MU Group.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.



Note:
1. These registers comprise a register bank. There are two register banks.

Figure 2.1 CPU Registers

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the starting address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.
Interrupts are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.
The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has higher priority than IPL, the interrupt is enabled.

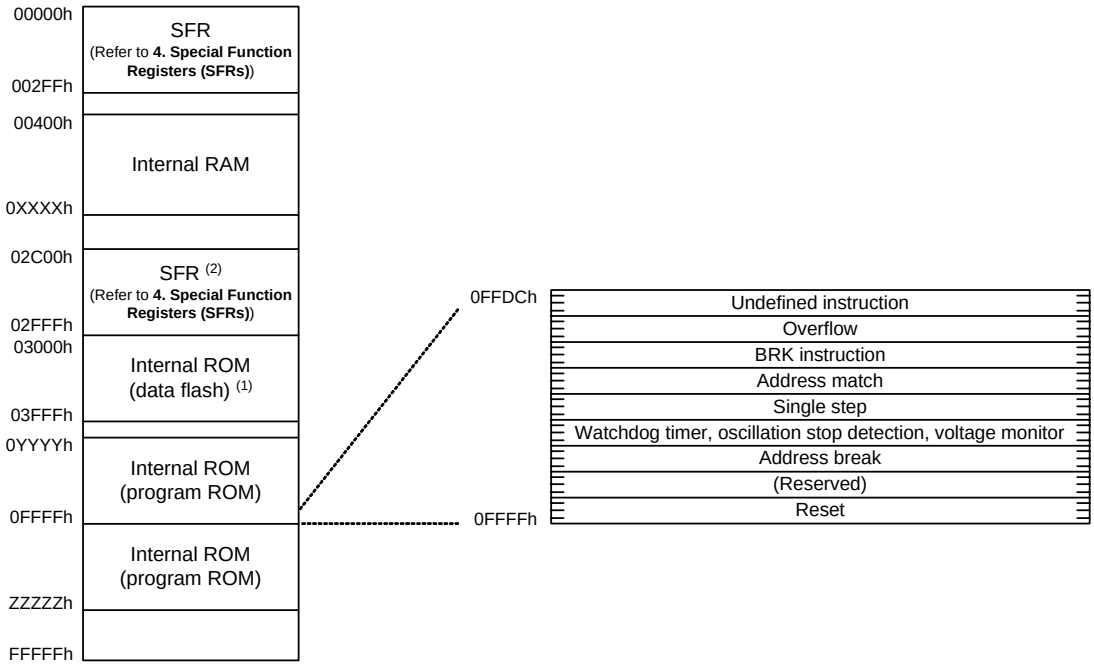
2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

3. Memory

3.1 R8C/3MU Group

Figure 3.2 is a Memory Map of R8C/3MU Group. The R8C/3MU Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. For example, a 64-Kbyte internal ROM area is allocated addresses 04000h to 13FFFh. The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.
The internal ROM (data flash) is allocated addresses 03000h to 03FFFh.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 8-Kbyte internal RAM area is allocated addresses 00400h to 023FFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh (the SFR areas for the DTC and other modules). Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.



Notes:
1. The data flash indicates block A (1 Kbyte), block B (1 Kbyte), block C (1 Kbyte), and block D (1 Kbyte).
2. The SFR areas for the DTC and other modules are allocated to addresses 02C00h to 02FFFh.
3. The blank areas are reserved and cannot be accessed by users.

Part Number	Internal ROM			Internal RAM	
	Size	Address 0YYYYh	Address ZZZZZh	Size	Address 0XXXXh
R5F213M6UNNP R5F213M6UNXXXNP	32 Kbytes	08000h	—	4 Kbytes	013FFh
R5F213M8UNNP R5F213M8UNXXXNP	64 Kbytes	04000h	13FFFh	8 Kbytes	023FFh

Figure 3.1 Memory Map of R8C/3MU Group

3.2 R8C/3MK Group

Figure 3.2 is a Memory Map of R8C/3MK Group. The R8C/3MK Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. A 64-Kbyte internal ROM area is allocated addresses 04000h to 13FFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.
The internal ROM (data flash) is allocated addresses 03000h to 03FFFh.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 8-Kbyte internal RAM area is allocated addresses 00400h to 023FFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
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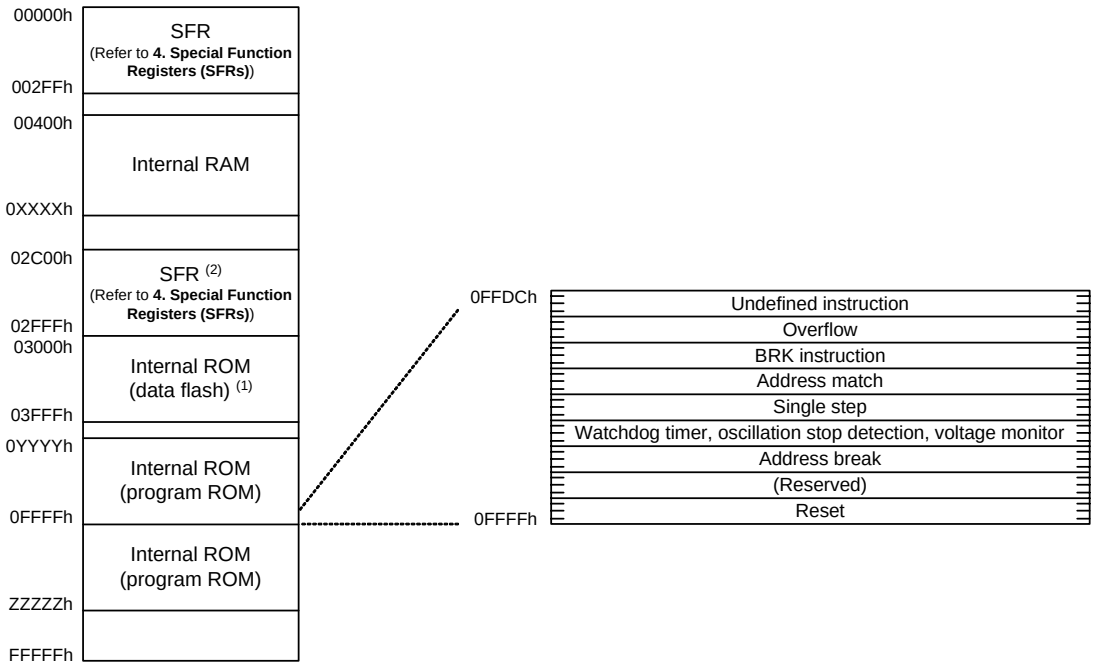


Notes:
1. The data flash indicates block A (1 Kbyte), block B (1 Kbyte), block C (1 Kbyte), and block D (1 Kbyte).
2. The SFR areas for the DTC and other modules are allocated to addresses 02C00h to 02FFFh.
3. The blank areas are reserved and cannot be accessed by users.

Part Number	Internal ROM			Internal RAM	
	Size	Address 0YYYYh	Address ZZZZZh	Size	Address 0XXXXh
R5F213M8KNNP R5F213M8KNXXXNP	64 Kbytes	04000h	13FFFh	8 Kbytes	023FFh
R5F213MCKNNP R5F213MCKNXXXNP	128 Kbytes	04000h	23FFFh	10 Kbytes	02BFFh

Figure 3.2 Memory Map of R8C/3MK Group

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.15 list the special function registers. Table 4.16 lists the ID Code Areas and Option Function Select Area.

Table 4.1 SFR Information (1) [1]

Address	Register	Symbol	After Reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	00101000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h	Module Standby Control Register	MSTCR	00h
0009h	System Clock Control Register 3	CM3	00h
000Ah	Protect Register	PRCR	00h
000Bh	Reset Source Determination Register	RSTFR	0XXXXXXXb [2]
000Ch	Oscillation Stop Detection Register	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDTC	00111111b
0010h			
0011h			
0012h			
0013h			
0014h			
0015h	High-Speed On-Chip Oscillator Control Register 7	FRA7	When shipping
0016h			
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h 10000000b [3]
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h	High-Speed On-Chip Oscillator Control Register 0	FRA0	00h
0024h	High-Speed On-Chip Oscillator Control Register 1	FRA1	When shipping
0025h	High-Speed On-Chip Oscillator Control Register 2	FRA2	00h
0026h	On-Chip Reference Voltage Control Register	OCVREFCR	00h
0027h			
0028h	Clock Prescaler Reset Flag	CPSRF	00h
0029h	High-Speed On-Chip Oscillator Control Register 4	FRA4	When shipping
002Ah	High-Speed On-Chip Oscillator Control Register 5	FRA5	When shipping
002Bh	High-Speed On-Chip Oscillator Control Register 6	FRA6	When shipping
002Ch			
002Dh			
002Eh			
002Fh	High-Speed On-Chip Oscillator Control Register 3	FRA3	When shipping
0030h	Voltage Monitor Circuit Control Register	CMPA	00h
0031h	Voltage Monitor Circuit Edge Select Register	VCAC	00h
0032h			
0033h	Voltage Detect Register 1	VCA1	00001000b
0034h	Voltage Detect Register 2	VCA2	00h [4] 00100000b [5]
0035h			
0036h	Voltage Detection 1 Level Select Register	VD1LS	00000111b
0037h			
0038h	Voltage Monitor 0 Circuit Control Register	VW0C	1100X010b [4] 1100X011b [5]
0039h	Voltage Monitor 1 Circuit Control Register	VW1C	10001010b

X: Undefined

Notes:

1. The blank areas are reserved and cannot be accessed by users.
2. The CWR bit in the RSTFR register is set to 0 after power-on and voltage monitor 0 reset. Hardware reset, software reset, or watchdog timer reset does not affect this bit.
3. The CSPROINI bit in the OFS register is set to 0.
4. The LVDAS bit in the OFS register is set to 1.
5. The LVDAS bit in the OFS register is set to 0.

Table 4.2 SFR Information (2) (1)

Address	Register	Symbol	After Reset
003Ah	Voltage Monitor 2 Circuit Control Register	VW2C	10000010b
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			
0040h			
0041h	Flash Memory Ready Interrupt Control Register	FMRDYIC	XXXXX000b
0042h			
0043h			
0044h			
0045h			
0046h	INT4 Interrupt Control Register	INT4IC	XX00X000b
0047h	Timer RC Interrupt Control Register	TRCIC	XXXXX000b
0048h			
0049h	USB RESUME Interrupt Control Register	USBRSMIC	XXXXX000b
004Ah			
004Bh	UART2 Transmit Interrupt Control Register	S2TIC	XXXXX000b
004Ch	UART2 Receive Interrupt Control Register	S2RIC	XXXXX000b
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register (3)	ADIC	XXXXX000b
004Fh	SSU Interrupt Control Register/IIC bus Interrupt Control Register (2)	SSUIC/IICIC	XXXXX000b
0050h			
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXXX000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXXX000b
0055h	INT2 Interrupt Control Register	INT2IC	XX00X000b
0056h	Timer RA Interrupt Control Register	TRAIC	XXXXX000b
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh			
005Ch			
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh	UART2 Bus Collision Detection Interrupt Control Register	U2BCNIC	XXXXX000b
005Fh			
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh	USB INT Interrupt Control Register	USBINTIC	XXXXX000b
006Ch	UART3 Transmit Interrupt Control Register	S3RIC	XXXXX000b
006Dh	UART3 Receive Interrupt Control Register	S3TIC	XXXXX000b
006Eh			
006Fh			
0070h			
0071h			
0072h	Voltage Monitor 1 Interrupt Control Register	VCMP1IC	XXXXX000b
0073h	Voltage Monitor 2 Interrupt Control Register	VCMP2IC	XXXXX000b
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

X: Undefined

Notes:

1. The blank areas are reserved and cannot be accessed by users.
2. Selectable by the IICSEL bit in the SSUIICSR register.
3. This register is not available in the R8C/3MU Group.

Table 4.3 SFR Information (3) (1)

Address	Register	Symbol	After Reset
0080h	DTC Activation Control Register	DTCTL	00h
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h	DTC Activation Enable Register 0	DTCEN0	00h
0089h	DTC Activation Enable Register 1	DTCEN1	00h
008Ah	DTC Activation Enable Register 2	DTCEN2	00h
008Bh	DTC Activation Enable Register 3	DTCEN3	00h
008Ch			
008Dh			
008Eh	DTC Activation Enable Register 6	DTCEN6	00h
008Fh			
0090h			
0091h			
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h			
0099h			
009Ah			
009Bh			
009Ch			
009Dh			
009Eh			
009Fh			
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h	UART2 Transmit/Receive Mode Register	U2MR	00h
00A9h	UART2 Bit Rate Register	U2BRG	XXh
00AAh	UART2 Transmit Buffer Register	U2TB	XXh
00ABh			XXh
00ACh	UART2 Transmit/Receive Control Register 0	U2C0	00001000b
00ADh	UART2 Transmit/Receive Control Register 1	U2C1	00000010b
00AEh	UART2 Receive Buffer Register	U2RB	XXh
00AFh			XXh
00B0h	UART2 Digital Filter Function Select Register	URXDF	00h
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h			
00B9h			
00BAh			
00BBh	UART2 Special Mode Register 5	U2SMR5	00h
00BCh			
00BDh	UART2 Special Mode Register 3	U2SMR3	000X0X0Xb
00BEh			
00BFh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.4 SFR Information (4) (1)

Address	Register	Symbol	After Reset
00C0h	A/D Register 0 (2)	AD0	XXh
00C1h			000000XXb
00C2h	A/D Register 1 (2)	AD1	XXh
00C3h			000000XXb
00C4h	A/D Register 2 (2)	AD2	XXh
00C5h			000000XXb
00C6h	A/D Register 3 (2)	AD3	XXh
00C7h			000000XXb
00C8h	A/D Register 4 (2)	AD4	XXh
00C9h			000000XXb
00CAh	A/D Register 5 (2)	AD5	XXh
00CBh			000000XXb
00CCh	A/D Register 6 (2)	AD6	XXh
00CDh			000000XXb
00CEh	A/D Register 7 (2)	AD7	XXh
00CFh			000000XXb
00D0h			
00D1h			
00D2h			
00D3h			
00D4h	A/D Mode Register (2)	ADMOD	00h
00D5h	A/D Input Select Register (2)	ADINSEL	11000000b
00D6h	A/D Control Register 0 (2)	ADCON0	00h
00D7h	A/D Control Register 1 (2)	ADCON1	00h
00D8h			
00D9h			
00DAh			
00DBh			
00DCh			
00DDh			
00DEh			
00DFh			
00E0h	Port P0 Register	P0	XXh
00E1h	Port P1 Register	P1	XXh
00E2h	Port P0 Direction Register	PD0	00h
00E3h	Port P1 Direction Register	PD1	00h
00E4h			
00E5h	Port P3 Register	P3	XXh
00E6h			
00E7h	Port P3 Direction Register	PD3	00h
00E8h	Port P4 Register	P4	XXh
00E9h			
00EAh	Port P4 Direction Register	PD4	00h
00EBh			
00ECh	Port P6 Register	P6	XXh
00EDh	Port P7 Register	P7	XXh
00EEh	Port P6 Direction Register	PD6	00h
00EFh	Port P7 Direction Register	PD7	00h
00F0h	Port P8 Register	P8	XXh
00F1h			
00F2h	Port P8 Direction Register	PD8	00h
00F3h			
00F4h			
00F5h			
00F6h			
00F7h			
00F8h			
00F9h			
00FAh			
00FBh			
00FCh			
00FDh			
00FEh			
00FFh			

X: Undefined

Notes:

1. The blank areas are reserved and cannot be accessed by users.
2. This register is not available in the R8C/3MU Group.

Table 4.5 SFR Information (5) (1)

Address	Register	Symbol	After Reset
0100h	Timer RA Control Register	TRACR	00h
0101h	Timer RA I/O Control Register	TRAIOC	00h
0102h	Timer RA Mode Register	TRAMR	00h
0103h	Timer RA Prescaler Register	TRAPRE	FFh
0104h	Timer RA Register	TRA	FFh
0105h	LIN Control Register 2	LINCR2	00h
0106h	LIN Control Register	LINCR	00h
0107h	LIN Status Register	LINST	00h
0108h	Timer RB Control Register	TRBCR	00h
0109h	Timer RB One-Shot Control Register	TRBOCR	00h
010Ah	Timer RB I/O Control Register	TRBIOC	00h
010Bh	Timer RB Mode Register	TRBMR	00h
010Ch	Timer RB Prescaler Register	TRBPRE	FFh
010Dh	Timer RB Secondary Register	TRBSC	FFh
010Eh	Timer RB Primary Register	TRBPR	FFh
010Fh			
0110h			
0111h			
0112h			
0113h			
0114h			
0115h			
0116h			
0117h			
0118h			
0119h			
011Ah			
011Bh			
011Ch			
011Dh			
011Eh			
011Fh			
0120h	Timer RC Mode Register	TRCMR	01001000b
0121h	Timer RC Control Register 1	TRCCR1	00h
0122h	Timer RC Interrupt Enable Register	TRCIER	01110000b
0123h	Timer RC Status Register	TRCSR	01110000b
0124h	Timer RC I/O Control Register 0	TRCIOR0	10001000b
0125h	Timer RC I/O Control Register 1	TRCIOR1	10001000b
0126h	Timer RC Counter	TRC	00h
0127h			00h
0128h	Timer RC General Register A	TRCGRA	FFh
0129h			FFh
012Ah	Timer RC General Register B	TRCGRB	FFh
012Bh			FFh
012Ch	Timer RC General Register C	TRCGRC	FFh
012Dh			FFh
012Eh	Timer RC General Register D	TRCGRD	FFh
012Fh			FFh
0130h	Timer RC Control Register 2	TRCCR2	00011000b
0131h	Timer RC Digital Filter Function Select Register	TRCDF	00h
0132h	Timer RC Output Master Enable Register	TRCOER	01111111b
0133h	Timer RC Trigger Control Register (2)	TRCADCR	00h
0134h			
0135h			
0136h			
0137h			
0138h			
0139h			
013Ah			
013Bh			
013Ch			
013Dh			
013Eh			
013Fh			

Notes:
1. The blank areas are reserved and cannot be accessed by users.
2. This register is not available in the R8C/3MU Group.

Table 4.6 SFR Information (6) (1)

Address	Register	Symbol	After Reset
0140h			
0141h			
0142h			
0143h			
0144h			
0145h			
0146h			
0147h			
0148h			
0149h			
014Ah			
014Bh			
014Ch			
014Dh			
014Eh			
014Fh			
0150h			
0151h			
0152h			
0153h			
0154h			
0155h			
0156h			
0157h			
0158h			
0159h			
015Ah			
015Bh			
015Ch			
015Dh			
015Eh			
015Fh			
0160h	UART1 Transmit/Receive Mode Register	U1MR	00h
0161h	UART1 Bit Rate Register	U1BRG	XXh
0162h	UART1 Transmit Buffer Register	U1TB	XXh
0163h			XXh
0164h	UART1 Transmit/Receive Control Register 0	U1C0	00001000b
0165h	UART1 Transmit/Receive Control Register 1	U1C1	00000010b
0166h	UART1 Receive Buffer Register	U1RB	XXh
0167h			XXh
0168h	UART3 Transmit/Receive Mode Register	U3MR	00h
0169h	UART3 Bit Rate Register	U3BRG	XXh
016Ah	UART3 Transmit Buffer Register	U3TB	XXh
016Bh			XXh
016Ch	UART3 Transmit/Receive Control Register 0	U3C0	00001000b
016Dh	UART3 Transmit/Receive Control Register 1	U3C1	00000010b
016Eh	UART3 Receive Buffer Register	U3RB	XXh
016Fh			XXh
0170h			
0171h			
0172h			
0173h			
0174h			
0175h			
0176h			
0177h			
0178h			
0179h			
017Ah			
017Bh			
017Ch			
017Dh			
017Eh			
017Fh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.7 SFR Information (7) (1)

Address	Register	Symbol	After Reset
0180h	Timer RA Pin Select Register	TRASR	00h
0181h	Timer RC Pin Select Register	TRBRCSR	00h
0182h	Timer RC Pin Select Register 0	TRCPSR0	00h
0183h	Timer RC Pin Select Register 1	TRCPSR1	00h
0184h			
0185h			
0186h			
0187h			
0188h	UART0 Pin Select Register	U0SR	00h
0189h	UART1 Pin Select Register	U1SR	00h
018Ah	UART2 Pin Select Register 0	U2SR0	00h
018Bh	UART2 Pin Select Register 1	U2SR1	00h
018Ch	SSU/IIC Pin Select Register	SSUIICSR	00h
018Dh			
018Eh	INT Interrupt Input Pin Select Register	INTSR	00h
018Fh	I/O Function Pin Select Register	PINSR	00h
0190h			
0191h			
0192h			
0193h	SS Bit Counter Register	SSBR	11111000b
0194h	SS Transmit Data Register L / IIC bus Transmit Data Register (2)	SSTDR / ICDRT	FFh
0195h	SS Transmit Data Register H (2)	SSTDRH	FFh
0196h	SS Receive Data Register L / IIC bus Receive Data Register (2)	SSRDR / ICDRR	FFh
0197h	SS Receive Data Register H (2)	SSRDRH	FFh
0198h	SS Control Register H / IIC bus Control Register 1 (2)	SSCRH / ICCR1	00h
0199h	SS Control Register L / IIC bus Control Register 2 (2)	SSCRL / ICCR2	01111101b
019Ah	SS Mode Register / IIC bus Mode Register (2)	SSMR / ICMR	00010000b / 00011000b
019Bh	SS Enable Register / IIC bus Interrupt Enable Register (2)	SSER / ICIER	00h
019Ch	SS Status Register / IIC bus Status Register (2)	SSSR / ICSR	00h / 0000X000b
019Dh	SS Mode Register 2 / Slave Address Register (2)	SSMR2 / SAR	00h
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			
01B0h			
01B1h			
01B2h	Flash Memory Status Register	FST	10000X00b
01B3h			
01B4h	Flash Memory Control Register 0	FMR0	00h
01B5h	Flash Memory Control Register 1	FMR1	00h
01B6h	Flash Memory Control Register 2	FMR2	00h
01B7h			
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			

X: Undefined

Notes:

1. The blank areas are reserved and cannot be accessed by users.
2. Selectable by the IICSEL bit in the SSUIICSR register.

Table 4.8 SFR Information (8) (1)

Address	Register	Symbol	After Reset
01C0h	Address Match Interrupt Register 0	RMAD0	XXh
01C1h			XXh
01C2h			0000XXXXb
01C3h	Address Match Interrupt Enable Register 0	AIER0	00h
01C4h	Address Match Interrupt Register 1	RMAD1	XXh
01C5h			XXh
01C6h			0000XXXXb
01C7h	Address Match Interrupt Enable Register 1	AIER1	00h
01C8h			
01C9h			
01CAh			
01CBh			
01CCh			
01CDh			
01CEh			
01CFh			
01D0h			
01D1h			
01D2h			
01D3h			
01D4h			
01D5h			
01D6h			
01D7h			
01D8h			
01D9h			
01DAh			
01DBh			
01DCh			
01DDh			
01DEh			
01DFh			
01E0h	Pull-Up Control Register 0	PUR0	00h
01E1h	Pull-Up Control Register 1	PUR1	00h
01E2h	Pull-Up Control Register 2	PUR2	00h
01E3h			
01E4h			
01E5h			
01E6h			
01E7h			
01E8h			
01E9h			
01EAh			
01EBh			
01ECh			
01EDh			
01EEh			
01EFh			
01F0h	Port P1 Drive Capacity Control Register	P1DRR	00h
01F1h			
01F2h	Drive Capacity Control Register 0	DRR0	00h
01F3h	Drive Capacity Control Register 1	DRR1	00h
01F4h	Drive Capacity Control Register 2	DRR2	00h
01F5h	Input Threshold Control Register 0	VLT0	00h
01F6h	Input Threshold Control Register 1	VLT1	00h
01F7h	Input Threshold Control Register 2	VLT2	00h
01F8h	Comparator B Control Register 0	INTCMP	00h
01F9h			
01FAh	External Input Enable Register 0	INTEN	00h
01FBh	External Input Enable Register 1	INTEN1	00h
01FCh	INT Input Filter Select Register 0	INTF	00h
01FDh	INT Input Filter Select Register 1	INTF1	00h
01FEh	Key Input Enable Register 0	KIEN	00h
01FFh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.9 SFR Information (9) (1)

Address	Register	Symbol	After Reset
2C00h	DTC Transfer Vector Area		XXh
2C01h	DTC Transfer Vector Area		XXh
2C02h	DTC Transfer Vector Area		XXh
2C03h	DTC Transfer Vector Area		XXh
2C04h	DTC Transfer Vector Area		XXh
2C05h	DTC Transfer Vector Area		XXh
2C06h	DTC Transfer Vector Area		XXh
2C07h	DTC Transfer Vector Area		XXh
2C08h	DTC Transfer Vector Area		XXh
2C09h	DTC Transfer Vector Area		XXh
2C0Ah	DTC Transfer Vector Area		XXh
:	DTC Transfer Vector Area		XXh
:	DTC Transfer Vector Area		XXh
2C3Ah	DTC Transfer Vector Area		XXh
2C3Bh	DTC Transfer Vector Area		XXh
2C3Ch	DTC Transfer Vector Area		XXh
2C3Dh	DTC Transfer Vector Area		XXh
2C3Eh	DTC Transfer Vector Area		XXh
2C3Fh	DTC Transfer Vector Area		XXh
2C40h	DTC Control Data 0	DTCD0	XXh
2C41h			XXh
2C42h			XXh
2C43h			XXh
2C44h			XXh
2C45h			XXh
2C46h			XXh
2C47h			XXh
2C48h	DTC Control Data 1	DTCD1	XXh
2C49h			XXh
2C4Ah			XXh
2C4Bh			XXh
2C4Ch			XXh
2C4Dh			XXh
2C4Eh			XXh
2C4Fh			XXh
2C50h	DTC Control Data 2	DTCD2	XXh
2C51h			XXh
2C52h			XXh
2C53h			XXh
2C54h			XXh
2C55h			XXh
2C56h			XXh
2C57h			XXh
2C58h	DTC Control Data 3	DTCD3	XXh
2C59h			XXh
2C5Ah			XXh
2C5Bh			XXh
2C5Ch			XXh
2C5Dh			XXh
2C5Eh			XXh
2C5Fh			XXh
2C60h	DTC Control Data 4	DTCD4	XXh
2C61h			XXh
2C62h			XXh
2C63h			XXh
2C64h			XXh
2C65h			XXh
2C66h			XXh
2C67h			XXh
2C68h	DTC Control Data 5	DTCD5	XXh
2C69h			XXh
2C6Ah			XXh
2C6Bh			XXh
2C6Ch			XXh
2C6Dh			XXh
2C6Eh			XXh
2C6Fh			XXh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.10 SFR Information (10) (1)

Address	Register	Symbol	After Reset
2C70h	DTC Control Data 6	DTCD6	XXh
2C71h			XXh
2C72h			XXh
2C73h			XXh
2C74h			XXh
2C75h			XXh
2C76h			XXh
2C77h			XXh
2C78h	DTC Control Data 7	DTCD7	XXh
2C79h			XXh
2C7Ah			XXh
2C7Bh			XXh
2C7Ch			XXh
2C7Dh			XXh
2C7Eh			XXh
2C7Fh			XXh
2C80h	DTC Control Data 8	DTCD8	XXh
2C81h			XXh
2C82h			XXh
2C83h			XXh
2C84h			XXh
2C85h			XXh
2C86h			XXh
2C87h			XXh
2C88h	DTC Control Data 9	DTCD9	XXh
2C89h			XXh
2C8Ah			XXh
2C8Bh			XXh
2C8Ch			XXh
2C8Dh			XXh
2C8Eh			XXh
2C8Fh			XXh
2C90h	DTC Control Data 10	DTCD10	XXh
2C91h			XXh
2C92h			XXh
2C93h			XXh
2C94h			XXh
2C95h			XXh
2C96h			XXh
2C97h			XXh
2C98h	DTC Control Data 11	DTCD11	XXh
2C99h			XXh
2C9Ah			XXh
2C9Bh			XXh
2C9Ch			XXh
2C9Dh			XXh
2C9Eh			XXh
2C9Fh			XXh
2CA0h	DTC Control Data 12	DTCD12	XXh
2CA1h			XXh
2CA2h			XXh
2CA3h			XXh
2CA4h			XXh
2CA5h			XXh
2CA6h			XXh
2CA7h			XXh
2CA8h	DTC Control Data 13	DTCD13	XXh
2CA9h			XXh
2CAAh			XXh
2CABh			XXh
2CACh			XXh
2CADh			XXh
2CAEh			XXh
2CAFh			XXh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.11 SFR Information (11) (1)

Address	Register	Symbol	After Reset
2CB0h	DTC Control Data 14	DTCD14	XXh
2CB1h			XXh
2CB2h			XXh
2CB3h			XXh
2CB4h			XXh
2CB5h			XXh
2CB6h			XXh
2CB7h			XXh
2CB8h	DTC Control Data 15	DTCD15	XXh
2CB9h			XXh
2CBAh			XXh
2CBBh			XXh
2CBCh			XXh
2CBDh			XXh
2CBEh			XXh
2CBFh			XXh
2CC0h	DTC Control Data 16	DTCD16	XXh
2CC1h			XXh
2CC2h			XXh
2CC3h			XXh
2CC4h			XXh
2CC5h			XXh
2CC6h			XXh
2CC7h			XXh
2CC8h	DTC Control Data 17	DTCD17	XXh
2CC9h			XXh
2CCAh			XXh
2CCBh			XXh
2CCCh			XXh
2CCDh			XXh
2CCEh			XXh
2CCFh			XXh
2CD0h	DTC Control Data 18	DTCD18	XXh
2CD1h			XXh
2CD2h			XXh
2CD3h			XXh
2CD4h			XXh
2CD5h			XXh
2CD6h			XXh
2CD7h			XXh
2CD8h	DTC Control Data 19	DTCD19	XXh
2CD9h			XXh
2CDAh			XXh
2CDBh			XXh
2CDCh			XXh
2CDDh			XXh
2CDEh			XXh
2CDFh			XXh
2CE0h	DTC Control Data 20	DTCD20	XXh
2CE1h			XXh
2CE2h			XXh
2CE3h			XXh
2CE4h			XXh
2CE5h			XXh
2CE6h			XXh
2CE7h			XXh
2CE8h	DTC Control Data 21	DTCD21	XXh
2CE9h			XXh
2CEAh			XXh
2CEBh			XXh
2CECh			XXh
2CEDh			XXh
2CEEh			XXh
2CEFh			XXh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.12 SFR Information (12) (1)

Address	Register	Symbol	After Reset
2CF0h	DTC Control Data 22	DTCD22	XXh
2CF1h			XXh
2CF2h			XXh
2CF3h			XXh
2CF4h			XXh
2CF5h			XXh
2CF6h			XXh
2CF7h			XXh
2CF8h	DTC Control Data 23	DTCD23	XXh
2CF9h			XXh
2CFAh			XXh
2CFBh			XXh
2CFCh			XXh
2CFDh			XXh
2CFEh			XXh
2CFFh			XXh
2D00h			
:			
2DFFh			
2E00h	System Configuration Control Register	SYSCFG	00h
2E01h			00h
2E02h			
2E03h			
2E04h	System Configuration Status Register 0	SYSSTS0	00000X00b
2E05h			XX000000b
2E06h			
2E07h			
2E08h	Device State Control Register 0	DVSTCTR0	00h
2E09h			00h
2E0Ah			
2E0Bh			
2E0Ch			
2E0Dh			
2E0Eh			
2E0Fh			
2E10h			
2E11h			
2E12h			
2E13h			
2E14h	CFIFO Port Register	CFIFO	00h
2E15h			00h
2E16h			
2E17h			
2E18h			
2E19h			
2E1Ah			
2E1Bh			
2E1Ch			
2E1Dh			
2E1Eh			
2E1Fh			
2E20h	CFIFO Port Select Register	CFIFOSEL	00h
2E21h			00h
2E22h	CFIFO Port Control Register	CFIFOCTR	00h
2E23h			00h
2E24h			
2E25h			
2E26h			
2E27h			
2E28h			
2E29h			
2E2Ah			
2E2Bh			
2E2Ch			
2E2Dh			
2E2Eh			
2E2Fh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.13 SFR Information (13) (1)

Address	Register	Symbol	After Reset
2E30h	Interrupt Enable Register 0	INTENB0	00h
2E31h			00h
2E32h	Interrupt Enable Register 1 (2)	INTENB1	00h
2E33h			00h
2E34h			
2E35h			
2E36h	BRDY Interrupt Enable Register	BRDYENB	00h
2E37h			00h
2E38h	NRDY Interrupt Enable Register	NRDYENB	00h
2E39h			00h
2E3Ah	BEMP Interrupt Enable Register	BEMPENB	00h
2E3Bh			00h
2E3Ch	SOF Output Configuration Register	SOFCFG	00h
2E3Dh			00h
2E3Eh			
2E3Fh			
2E40h	Interrupt Status Register 0	INTSTS0	X0000000b
2E41h			X0000000b
2E42h	Interrupt Status Register 1 (2)	INTSTS1	00h
2E43h			XX0X0000b
2E44h			
2E45h			
2E46h	BRDY Interrupt Status Register	BRDYSTS	00h
2E47h			00h
2E48h	NRDY Interrupt Status Register	NRDYSTS	00h
2E49h			00h
2E4Ah	BEMP Interrupt Status Register	BEMPSTS	00h
2E4Bh			00h
2E4Ch	Frame Number Register	FRMNUM	00h
2E4Dh			00h
2E4Eh			
2E4Fh			
2E50h	USB Address Register	USBADDR	00h
2E51h			00h
2E52h			
2E53h			
2E54h	USB Request Type Register	USBREQ	00h
2E55h			00h
2E56h	USB Request Value Register	USBVAL	00h
2E57h			00h
2E58h	USB Request Index Register	USBINDX	00h
2E59h			00h
2E5Ah	USB Request Length Register	USBLENG	00h
2E5Bh			00h
2E5Ch	DCP Configuration Register	DCPCFG	00h
2E5Dh			00h
2E5Eh	DCP Max Packet Size Register	DCPMAXP	40h
2E5Fh			00h
2E60h	DCP Control Register	DCPCTR	00h
2E61h			00h
2E62h			
2E63h			
2E64h	Pipe Window Select Register	PIPESEL	00h
2E65h			00h
2E66h			
2E67h			
2E68h	Pipe Configuration Register	PIPECFG	00h
2E69h			00h
2E6Ah			
2E6Bh			
2E6Ch	Pipe Max Packet Size Register	PIPEMAXP	00h
2E6Dh			00h
2E6Eh	Pipe Period Control Register (2)	PIPEPERI	00h
2E6Fh			00h

X: Undefined

Notes:

1. The blank areas are reserved and cannot be accessed by users.
2. This register is not available in the R8C/3MU Group.

Table 4.14 SFR Information (14) (1)

Address	Register	Symbol	After Reset
2E70h			
2E71h			
2E72h			
2E73h			
2E74h			
2E75h			
2E76h	Pipe 4 Control Register	PIPE4CTR	00h
2E77h			00h
2E78h	Pipe 5 Control Register	PIPE5CTR	00h
2E79h			00h
2E7Ah	Pipe 6 Control Register	PIPE6CTR	00h
2E7Bh			00h
2E7Ch	Pipe 7 Control Register	PIPE7CTR	00h
2E7Dh			00h
2E7Eh			
2E7Fh			
2E80h			
:			
2E8Fh			
2E90h			
2E91h			
2E92h			
2E93h			
2E94h			
2E95h			
2E96h			
2E97h			
2E98h			
2E99h			
2E9Ah			
2E9Bh			
2E9Ch	Pipe 4 Transaction Counter Enable Register	PIPE4TRE	00h
2E9Dh			00h
2E9Eh	Pipe 4 Transaction Counter Register	PIPE4TRN	00h
2E9Fh			00h
2EA0h	Pipe 5 Transaction Counter Enable Register	PIPE5TRE	00h
2EA1h			00h
2EA2h	Pipe 5 Transaction Counter Register	PIPE5TRN	00h
2EA3h			00h
2EA4h			
2EA5h			
2EA6h			
2EA7h			
2EA8h			
2EA9h			
2EAAh			
2EABh			
2EACh			
2EADh			
:			
2ECFh			
2ED0h	Device Address 0 Configuration Register (2)	DEVADD0	00h
2ED1h			00h
2ED2h	Device Address 1 Configuration Register (2)	DEVADD1	00h
2ED3h			00h
2ED4h	Device Address 2 Configuration Register (2)	DEVADD2	00h
2ED5h			00h
2ED6h	Device Address 3 Configuration Register (2)	DEVADD3	00h
2ED7h			00h
2ED8h	Device Address 4 Configuration Register (2)	DEVADD4	00h
2ED9h			00h
2EDAh	Device Address 5 Configuration Register (2)	DEVADD5	00h
2EDBh			00h
2EDCh			
2EDDh			
:			
2EFFh			

X: Undefined

Notes:

1. The blank areas are reserved and cannot be accessed by users.
2. This register is not available in the R8C/3MU Group.

Table 4.15 SFR Information (15) (1)

Address	Register	Symbol	After Reset
2F00h	USB Module Control Register	USBMC	00X10000b
2F01h	PLL Control Register 0	PLC0	0010X000b
2F02h	PLL Control Register 1	PLC1	00001100b
2F03h	PLL Division Control Register	PLDIV	00001011b
2F04h			
2F05h			
2F06h			
2F07h			
2F08h			
2F09h			
2F0Ah			
2F0Bh			
2F0Ch			
2F0Dh			
2F0Eh			
2F0Fh			
2F10h	USB Pin Select Register 0	USBSR0	00h
2F11h			
2F12h	UART3 Pin Select Register	U3SR	00h
2F13h			
2F14h			
2F15h			
2F16h			
2F17h			
2F18h			
2F19h			
2F1Ah			
2F1Bh			
2F1Ch			
2F1Dh			
2F1Eh			
2F1Fh			
:			
2FFFh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.16 ID Code Areas and Option Function Select Area

Address	Area Name	Symbol	After Reset
:			
FFDBh	Option Function Select Register 2	OFS2	(Note 1)
:			
FFDFh	ID1		(Note 2)
:			
FFE3h	ID2		(Note 2)
:			
FFEBh	ID3		(Note 2)
:			
FFEFh	ID4		(Note 2)
:			
FFF3h	ID5		(Note 2)
:			
FFF7h	ID6		(Note 2)
:			
FFFBh	ID7		(Note 2)
:			
FFFFh	Option Function Select Register	OFS	(Note 1)

Notes:

1. The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the option function select area. If the block including the option function select area is erased, the option function select area is set to FFh.
   When blank products are shipped, the option function select area is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the option function select area is the value programmed by the user.
2. The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the ID code areas. If the block including the ID code areas is erased, the ID code areas are set to FFh.
   When blank products are shipped, the ID code areas are set to FFh. They are set to the written value after written by the user.
   When factory-programming products are shipped, the value of the ID code areas is the value programmed by the user.

5. Resets

The following resets are implemented: hardware reset, power-on reset, voltage monitor 0 reset, watchdog timer reset, and software reset.
Table 5.1 lists the Reset Names and Sources and Figure 5.1 shows a Block Diagram of Reset Circuit.

Table 5.1 Reset Names and Sources

Reset Name	Source
Hardware reset	Input voltage of $\overline{\text{RESET}}$ pin is held “L”
Power-on reset	VCC rises
Voltage monitor 0 reset	VCC falls (monitor voltage: Vdet0)
Watchdog timer reset	Underflow of watchdog timer
Software reset	Write 1 to PM03 bit in PM0 register

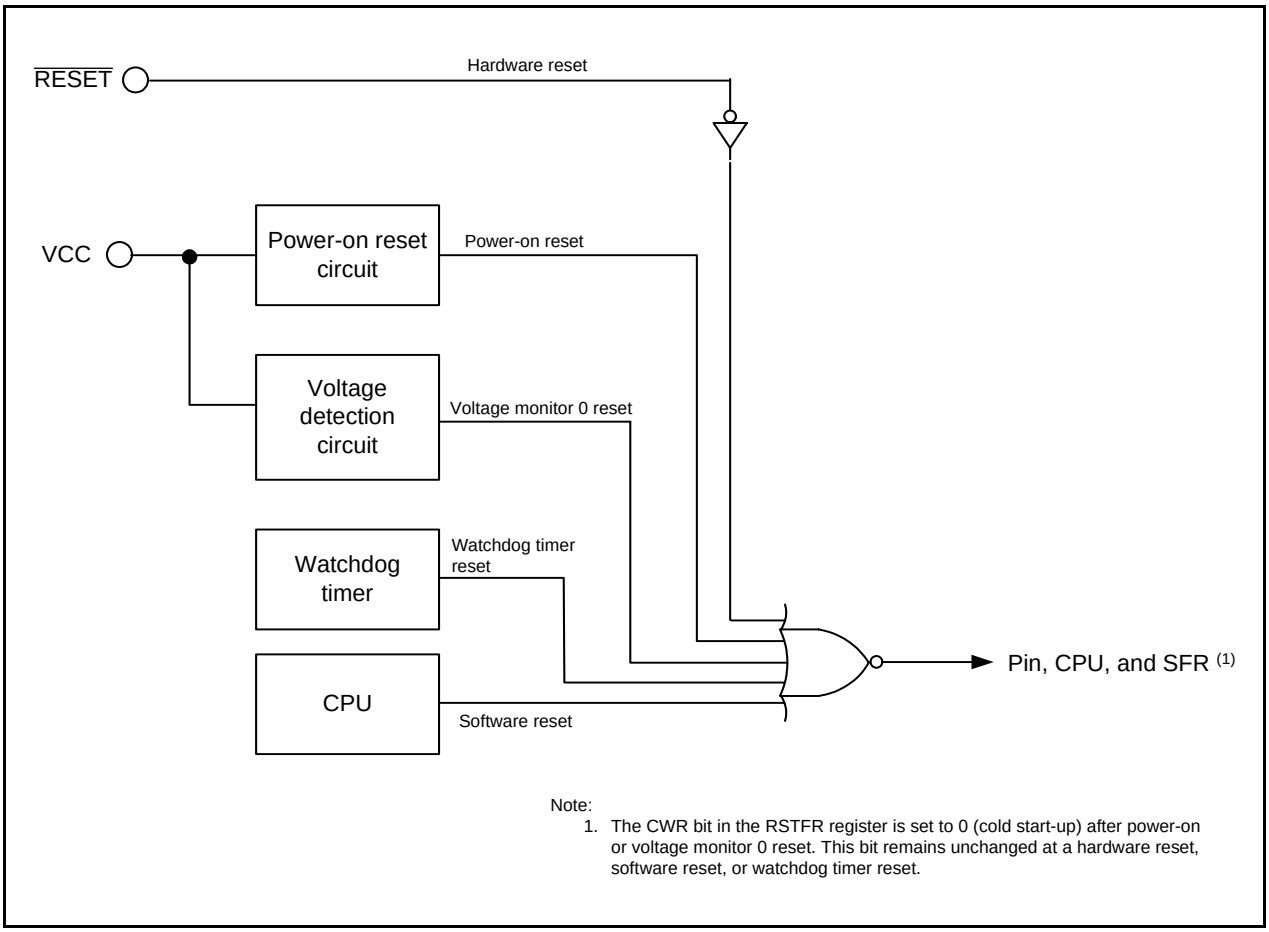


Figure 5.1 Block Diagram of Reset Circuit

Table 5.2 lists the Pin Functions while $\overline{\text{RESET}}$ Pin Level is “L”, Figure 5.2 shows the CPU Register Status after Reset, and Figure 5.3 shows the Reset Sequence.

Table 5.2 Pin Functions while $\overline{\text{RESET}}$ Pin Level is “L”

Pin Name	Pin Function
P0_0 to P0_4, P0_7, P1_0 to P1_7, P3_0, P3_3 to P3_5, P3_7, P4_5 to P4_7, P6_5 to P6_7, P7_6, P7_7, P8_1 to P8_3	Input port

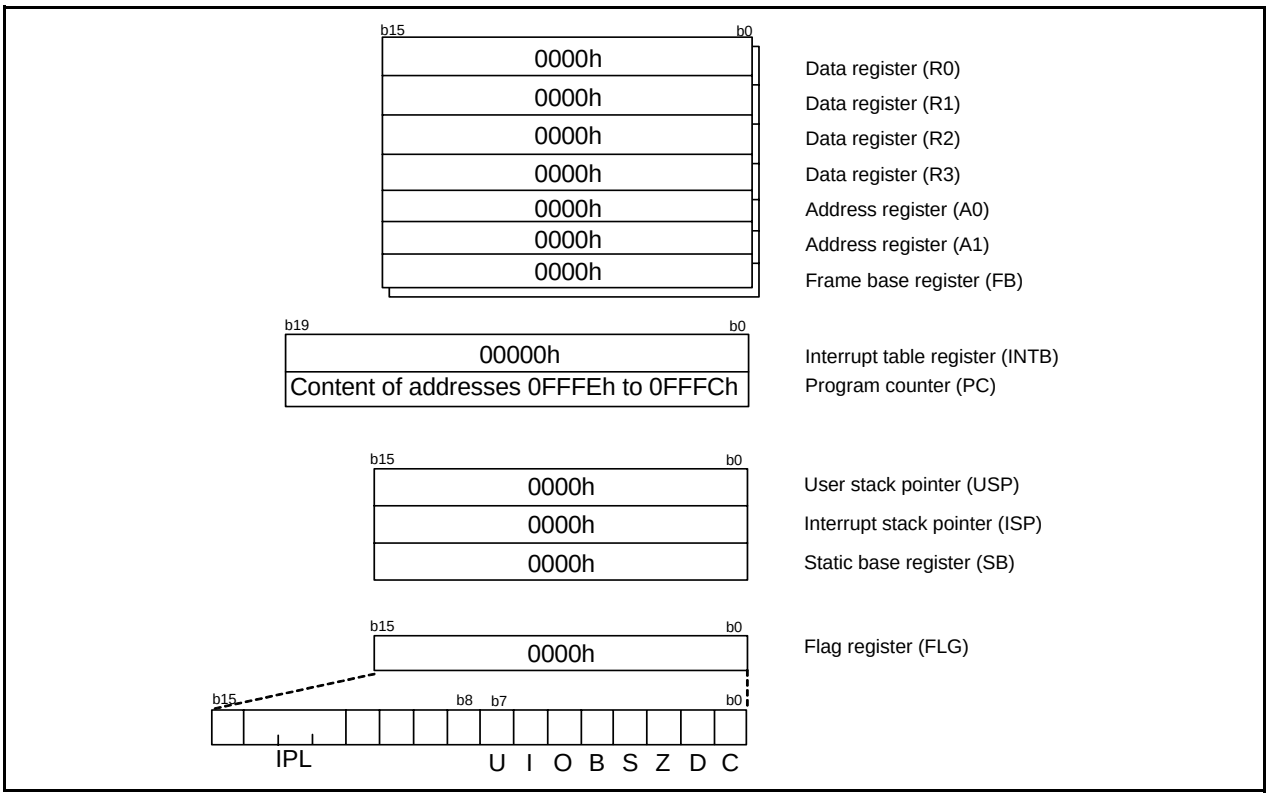
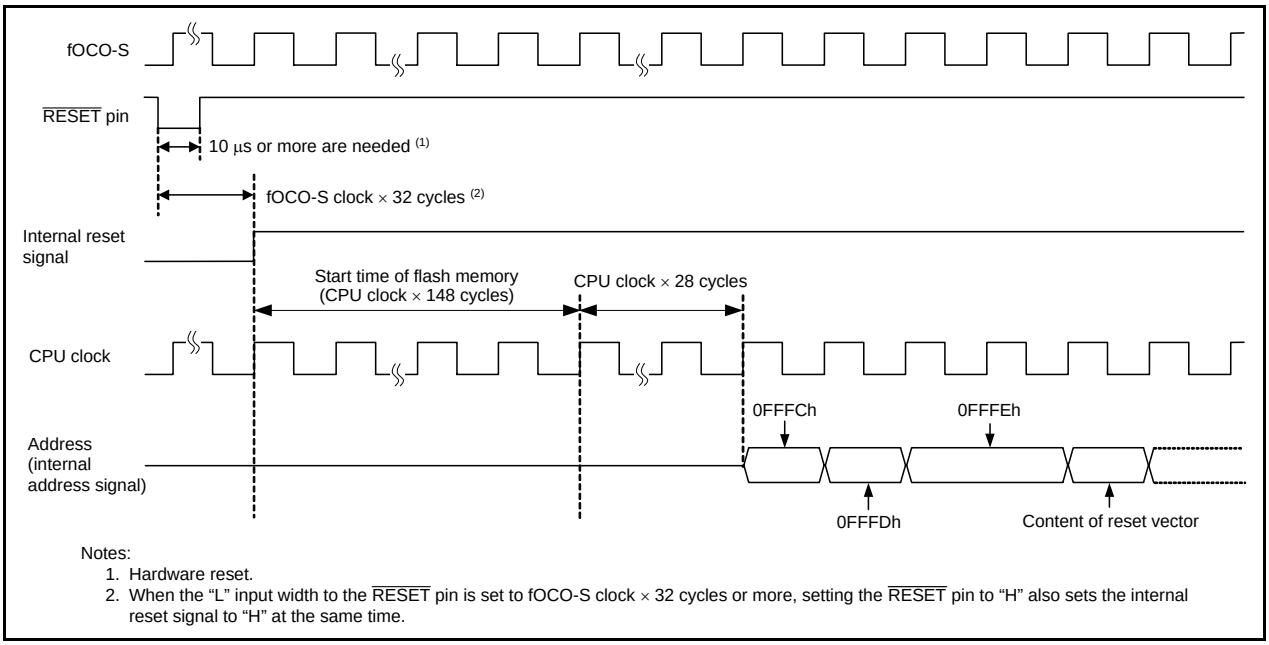


Figure 5.2 CPU Register Status after Reset



Notes:
1. Hardware reset.
2. When the “L” input width to the $\overline{\text{RESET}}$ pin is set to fOCO-S clock × 32 cycles or more, setting the $\overline{\text{RESET}}$ pin to “H” also sets the internal reset signal to “H” at the same time.

Figure 5.3 Reset Sequence

5.1 Registers

5.1.1 Processor Mode Register 0 (PM0)

Address 0004h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	PM03	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	—			
b3	PM03	Software reset bit	The MCU is reset when this bit is set to 1. When read, the content is 0.	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

Set the PRC1 bit in the PRCR register to 1 (write enabled) before rewriting the PM0 register.

5.1.2 Reset Source Determination Register (RSTFR)

Address 000Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0	
Symbol	—	—	—	—	WDR	SWR	HWR	CWR	
After Reset	0	X	X	X	X	X	X	X	(Note 1)

Bit	Symbol	Bit Name	Function	R/W
b0	CWR	Cold start-up/warm start-up determine flag (2, 3)	0: Cold start-up 1: Warm start-up	R/W
b1	HWR	Hardware reset detect flag	0: Not detected 1: Detected	R
b2	SWR	Software reset detect flag	0: Not detected 1: Detected	R
b3	WDR	Watchdog timer reset detect flag	0: Not detected 1: Detected	R
b4	—	Reserved bits	When read, the content is undefined.	R
b5	—			
b6	—			
b7	—	Reserved bit	Set to 0.	R/W

Notes:
1. The CWR bit is set to 0 (cold start-up) after power-on or voltage monitor 0 reset. This bit remains unchanged at a hardware reset, software reset, or watchdog timer reset.
2. If 1 is written to the CWR bit by a program, it is set to 1. (Writing 0 does not affect this bit.)
3. When the VW0C0 bit in the VW0C register is set to 0 (voltage monitor 0 reset disabled), the CWR bit value is undefined.

5.1.3 Option Function Select Register (OFS)

Address 0FFFFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CSPROINI	LVDAS	VDSEL1	VDSEL0	ROMCP1	ROMCR	—	WDTON
After Reset	User Setting Value (1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTON	Watchdog timer start select bit	0: Watchdog timer automatically starts after reset 1: Watchdog timer is stopped after reset	R/W
b1	—	Reserved bit	Set to 1.	R/W
b2	ROMCR	ROM code protect disable bit	0: ROM code protect disabled 1: ROMCP1 bit enabled	R/W
b3	ROMCP1	ROM code protect bit	0: ROM code protect enabled 1: ROM code protect disabled	R/W
b4	VDSEL0	Voltage detection 0 level select bit (2)	b5 b4 0 0: 3.80 V selected (Vdet0_3) 0 1: 2.85 V selected (Vdet0_2) 1 0: 2.35 V selected (Vdet0_1) 1 1: 1.90 V selected (Vdet0_0)	R/W
b5	VDSEL1			R/W
b6	LVDAS	Voltage detection 0 circuit start bit (3)	0: Voltage monitor 0 reset enabled after reset 1: Voltage monitor 0 reset disabled after reset	R/W
b7	CSPROINI	Count source protection mode after reset select bit	0: Count source protect mode enabled after reset 1: Count source protect mode disabled after reset	R/W

Notes:
1. The OFS register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the OFS register. If the block including the OFS register is erased, the OFS register is set to FFh.
   When blank products are shipped, the OFS register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS register is the value programmed by the user.
2. The same level of the voltage detection 0 level selected by bits VDSEL0 and VDESL1 is set in both functions of voltage monitor 0 reset and power-on reset.
3. To use power-on reset and voltage monitor 0 reset, set the LVDAS bit to 0 (voltage monitor 0 reset enabled after reset).

For a setting example of the OFS register, refer to **13.3.1 Setting Example of Option Function Select Area**.

LVDAS Bit (Voltage Detection 0 Circuit Start Bit)

The Vdet0 voltage to be monitored by the voltage detection 0 circuit is selected by bits VDSEL0 and VDSEL1.

5.1.4 Option Function Select Register 2 (OFS2)

Address 0FFDBh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	WDTRCS1	WDTRCS0	WDTUFS1	WDTUFS0
After Reset	User Settng Value (1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTUFS0	Watchdog timer underflow period set bit	b1 b0 0 0: 03FFh 0 1: 0FFFh 1 0: 1FFFh 1 1: 3FFFh	R/W
b1	WDTUFS1			R/W
b2	WDTRCS0	Watchdog timer refresh acknowledgement period set bit	b3 b2 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100%	R/W
b3	WDTRCS1			R/W
b4	—	Reserved bits	Set to 1.	R/W
b5	—			
b6	—			
b7	—			

Note:

1. The OFS2 register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the OFS2 register. If the block including the OFS2 register is erased, the OFS2 register is set to FFh.
   When blank products are shipped, the OFS2 register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS2 register is the value programmed by the user.

   For a setting example of the OFS2 register, refer to **13.3.1 Setting Example of Option Function Select Area**.

Bits WDTRCS0 and WDTRCS1 (Watchdog Timer Refresh Acknowledgement Period Set Bit)

Assuming that the period from when the watchdog timer starts counting until it underflows is 100%, the refresh acknowledgement period for the watchdog timer can be selected.
For details, refer to **14.3.1.1 Refresh Acknowledgment Period**.

5.2 Hardware Reset

A reset is applied using the $\overline{\text{RESET}}$ pin. When an “L” signal is applied to the $\overline{\text{RESET}}$ pin while the supply voltage meets the recommended operating conditions, pins, CPU, and SFRs are all reset (refer to **Table 5.2 Pin Functions while $\overline{\text{RESET}}$ Pin Level is “L”, Figure 5.2 CPU Register Status after Reset, and Table 4.1 to Table 4.15 SFR Information**).

When the input level applied to the $\overline{\text{RESET}}$ pin changes from “L” to “H”, a program is executed beginning with the address indicated by the reset vector. After reset, the low-speed on-chip oscillator clock with no division is automatically selected as the CPU clock.

Refer to **4. Special Function Registers (SFRs)** for the states of the SFRs after reset.

The internal RAM is not reset. If the $\overline{\text{RESET}}$ pin is pulled “L” while writing to the internal RAM is in progress, the contents of internal RAM will be undefined.

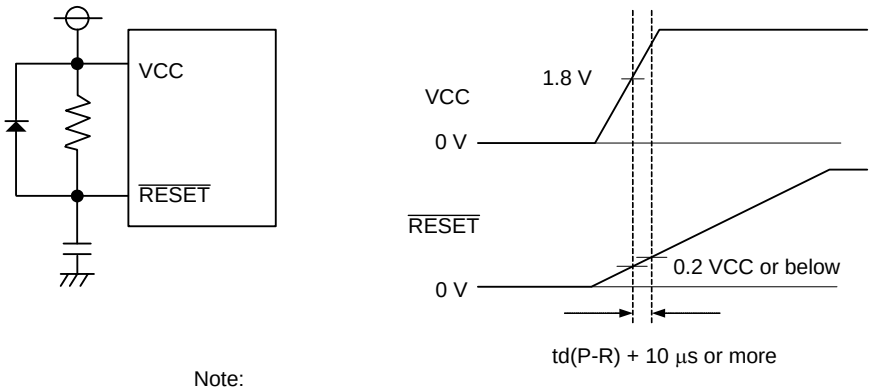
Figure 5.4 shows an Example of Hardware Reset Circuit and Operation and Figure 5.5 shows an Example of Hardware Reset Circuit (Usage Example of External Supply Voltage Detection Circuit) and Operation.

5.2.1 When Power Supply is Stable

(1) Apply “L” to the $\overline{\text{RESET}}$ pin.
(2) Wait for 10 μs.
(3) Apply “H” to the $\overline{\text{RESET}}$ pin.

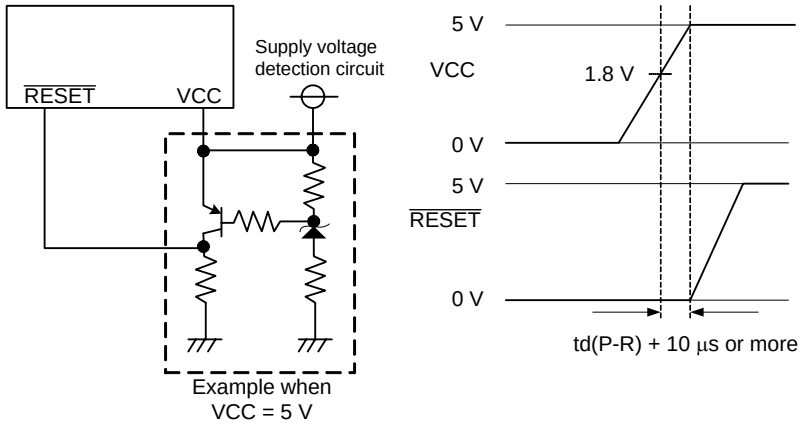
5.2.2 Power On

(1) Apply “L” to the $\overline{\text{RESET}}$ pin.
(2) Let the supply voltage increase until it meets the recommended operating conditions.
(3) Wait for td(P-R) or more to allow the internal power supply to stabilize (refer to **31. Electrical Characteristics**).
(4) Wait for 10 μs.
(5) Apply “H” to the $\overline{\text{RESET}}$ pin.



Note:
1. Refer to **31. Electrical Characteristics**.

Figure 5.4 Example of Hardware Reset Circuit and Operation



Note:
1. Refer to **31. Electrical Characteristics**.

Figure 5.5 Example of Hardware Reset Circuit (Usage Example of External Supply Voltage Detection Circuit) and Operation

5.3 Power-On Reset Function

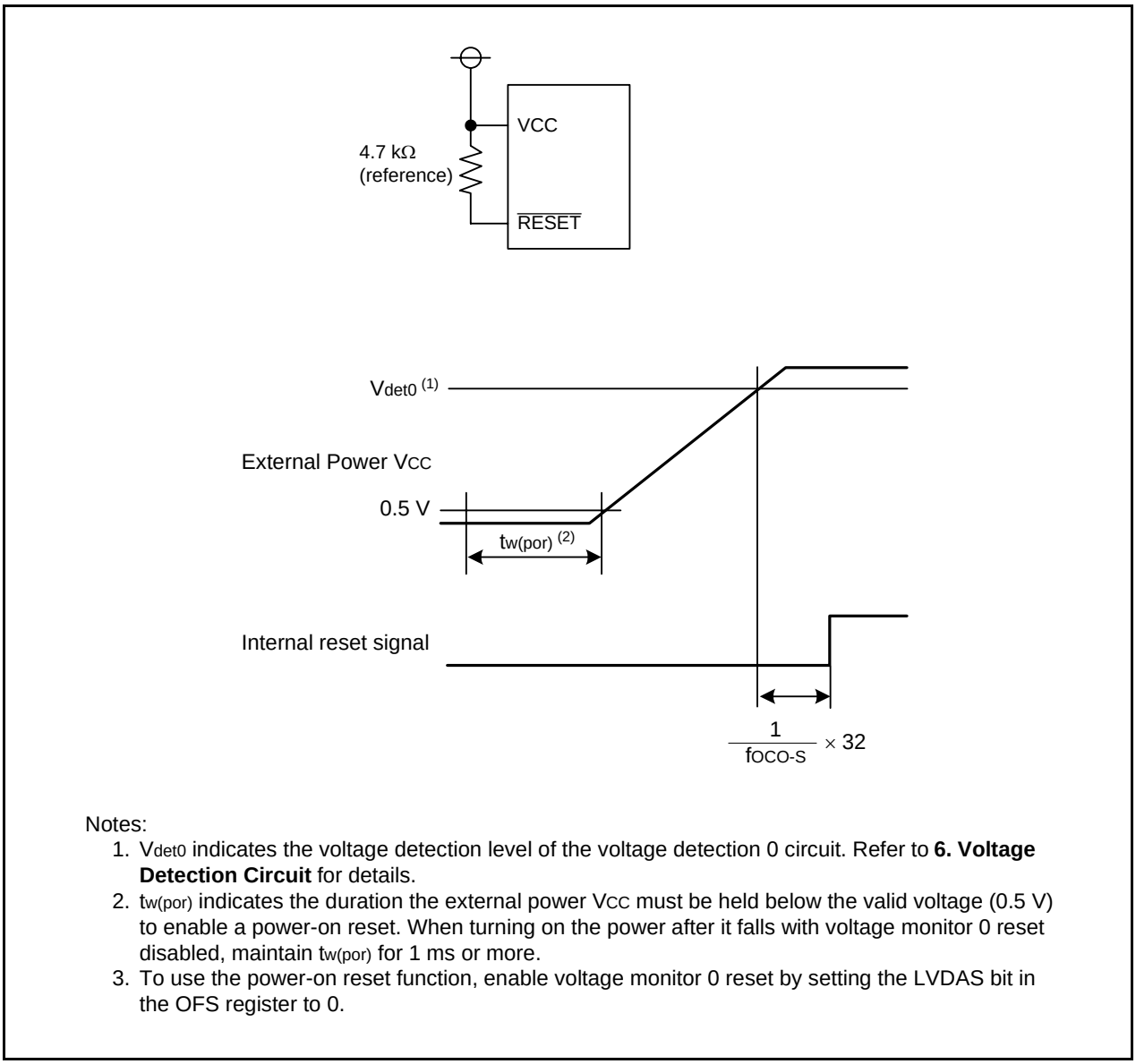
When the $\overline{\text{RESET}}$ pin is connected to the VCC pin via a pull-up resistor, and the VCC pin voltage level rises, the power-on reset function is enabled and the MCU resets its pins, CPU, and SFR. When a capacitor is connected to the $\overline{\text{RESET}}$ pin, too, always keep the voltage to the $\overline{\text{RESET}}$ pin 0.8 VCC or more.

When the input voltage to the VCC pin reaches the Vdet0 level or above, the low-speed on-chip oscillator clock starts counting. When the low-speed on-chip oscillator clock count reaches 32, the internal reset signal is held "H" and the MCU enters the reset sequence (refer to **Figure 5.3**). The low-speed on-chip oscillator clock with no division is automatically selected as the CPU clock after reset.

Refer to **4. Special Function Registers (SFRs)** for the states of the SFR after power-on reset.

To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.

Figure 5.6 shows an Example of Power-On Reset Circuit and Operation.



Notes:
1. V_{det0} indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** for details.
2. $t_{w(por)}$ indicates the duration the external power V_{CC} must be held below the valid voltage (0.5 V) to enable a power-on reset. When turning on the power after it falls with voltage monitor 0 reset disabled, maintain $t_{w(por)}$ for 1 ms or more.
3. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.

Figure 5.6 Example of Power-On Reset Circuit and Operation

5.4 Voltage Monitor 0 Reset

A reset is applied using the on-chip voltage detection 0 circuit. The voltage detection 0 circuit monitors the input voltage to the VCC pin. The voltage to monitor is Vdet0. To use voltage monitor 0 reset, set the LVDAS bit in the OFS register to 0 (voltage monitor 0 reset enabled after reset). The Vdet0 voltage detection level can be changed by the settings of bits VDSEL0 to VDSEL1 in the OFS register.

When the input voltage to the VCC pin reaches the Vdet0 level or below, the pins, CPU, and SFR are reset.

When the input voltage to the VCC pin reaches the Vdet0 level or above, the low-speed on-chip oscillator clock start counting. When the low-speed on-chip oscillator clock count reaches 32, the internal reset signal is held “H” and the MCU enters the reset sequence (refer to **Figure 5.3**). The low-speed on-chip oscillator clock with no division is automatically selected as the CPU clock after reset.

To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.

Bits VDSEL0 to VDSEL1 and LVDAS cannot be changed by a program. To set these bits, write values to b4 to b6 of address 0FFFFh using a flash programmer.

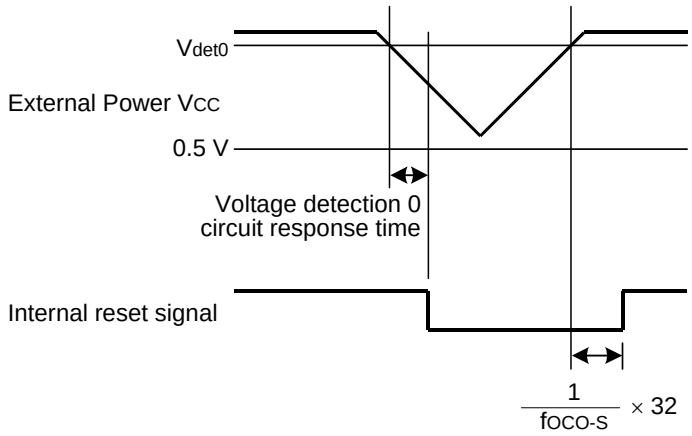
Refer to **5.1.3 Option Function Select Register (OFS)** for details of the OFS register.

Refer to **4. Special Function Registers (SFRs)** for the status of the SFR after voltage monitor 0 reset.

The internal RAM is not reset. When the input voltage to the VCC pin reaches the Vdet0 level or below while writing to the internal RAM is in progress, the contents of internal RAM are undefined.

Refer to **6. Voltage Detection Circuit** for details of voltage monitor 0 reset.

Figure 5.7 shows an Example of Voltage Monitor 0 Reset Circuit and Operation.



Notes:
1. Vdet0 indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** for details.
2. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.

Figure 5.7 Example of Voltage Monitor 0 Reset Circuit and Operation

5.5 Watchdog Timer Reset

When the PM12 bit in the PM1 register is set to 1 (reset when watchdog timer underflows), the MCU resets its pins, CPU, and SFR if the watchdog timer underflows. Then the program beginning with the address indicated by the reset vector is executed. After reset, the low-speed on-chip oscillator clock with no division is automatically selected as the CPU clock.
Refer to **4. Special Function Registers (SFRs)** for the states of the SFRs after watchdog timer reset.
The internal RAM is not reset. When the watchdog timer underflows while writing to the internal RAM is in progress, the contents of internal RAM are undefined.
The underflow period and refresh acknowledge period for the watchdog timer can be set by bits WDTUFS0 to WDTUFS1 and bits WDTRCS0 to WDTRCS1 in the OFS2 register, respectively.
Refer to **14. Watchdog Timer** for details of the watchdog timer.

5.6 Software Reset

When the PM03 bit in the PM0 register is set to 1 (MCU reset), the MCU resets its pins, CPU, and SFR. The program beginning with the address indicated by the reset vector is executed. After reset, the low-speed on-chip oscillator clock with no division is automatically selected for the CPU clock.
Refer to **4. Special Function Registers (SFRs)** for the states of the SFRs after software reset.
The internal RAM is not reset.

5.7 Cold Start-Up/Warm Start-Up Determination Function

The cold start-up/warm start-up determination function uses the CWR bit in the RSTFR register to determine cold start-up (reset process) at power-on and warm start-up (reset process) when a reset occurred during operation.
The CWR bit is set to 0 (cold start-up) at power-on and also set to 0 at a voltage monitor 0 reset. If 1 is written to the CWR bit by a program, it is set to 1. This bit remains unchanged at a hardware reset, software reset, or watchdog timer reset.
The cold start-up/warm start-up determination function uses voltage monitor 0 reset.
Figure 5.8 shows an Operating Example of Cold Start-Up/Warm Start-Up Function.

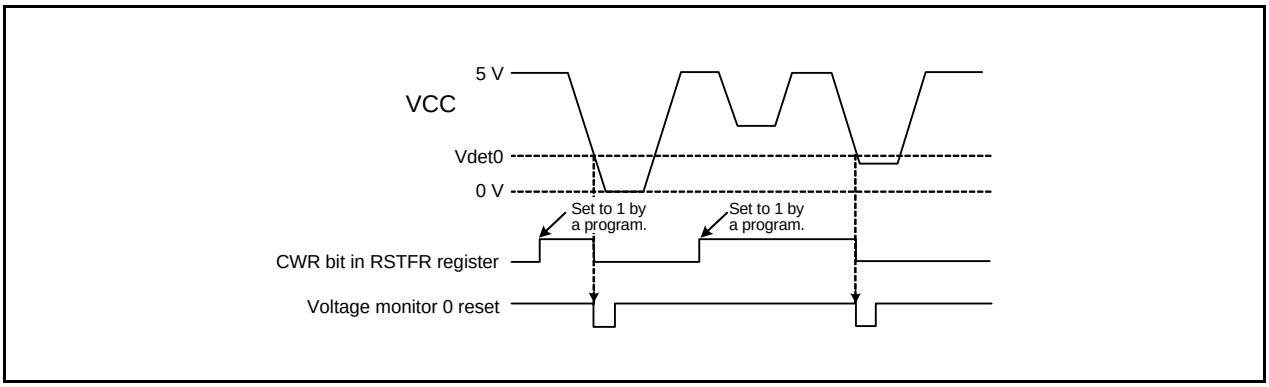


Figure 5.8 Operating Example of Cold Start-Up/Warm Start-Up Function

5.8 Reset Source Determination Function

The RSTFR register can be used to detect whether a hardware reset, software reset, or watchdog timer reset has occurred.
If a hardware reset occurs, the HWR bit is set to 1 (detected). If a software reset occurs, the SWR bit is set to 1 (detected). If a watchdog timer reset occurs, the WDR bit is set to 1 (detected).

6. Voltage Detection Circuit

The voltage detection circuit monitors the voltage input to the VCC pin. This circuit can be used to monitor the VCC input voltage by a program.

6.1 Overview

The detection voltage of voltage detection 0 can be selected among four levels using the OFS register.
The detection voltage of voltage detection 1 can be selected among 16 levels using the VD1LS register.
The voltage monitor 0 reset, and voltage monitor 1 interrupt and voltage monitor 2 interrupt can also be used.

Table 6.1 Voltage Detection Circuit Specifications

Item		Voltage Monitor 0	Voltage Monitor 1	Voltage Monitor 2
VCC monitor	Voltage to monitor	Vdet0	Vdet1	Vdet2
	Detection target	Whether passing through Vdet0 by rising or falling	Whether passing through Vdet1 by rising or falling	Whether passing through Vdet2 by rising or falling
	Detection voltage	Selectable among 4 levels using the OFS register.	Selectable among 16 levels using the VD1LS register.	The fixed level.
	Monitor	None	The VW1C3 bit in the VW1C register	The VCA13 bit in the VCA1 register
			Whether VCC is higher or lower than Vdet1	Whether VCC is higher or lower than Vdet2
Process at voltage detection	Reset	Voltage monitor 0 reset	None	None
		Reset at Vdet0 > VCC; CPU operation restarts at VCC > Vdet0		
	Interrupts	None	Voltage monitor 1 interrupt	Voltage monitor 2 interrupt
			Non-maskable or maskable selectable	Non-maskable or maskable selectable
			Interrupt request at: Vdet1 > VCC and/or VCC > Vdet1	Interrupt request at: Vdet2 > VCC and/or VCC > Vdet2
Digital filter	Switching enable/ disable	No digital filter function	Supported	Supported
	Sampling time	—	(fOCO-S divided by n) × 2 n: 1, 2, 4, and 8	(fOCO-S divided by n) × 2 n: 1, 2, 4, and 8

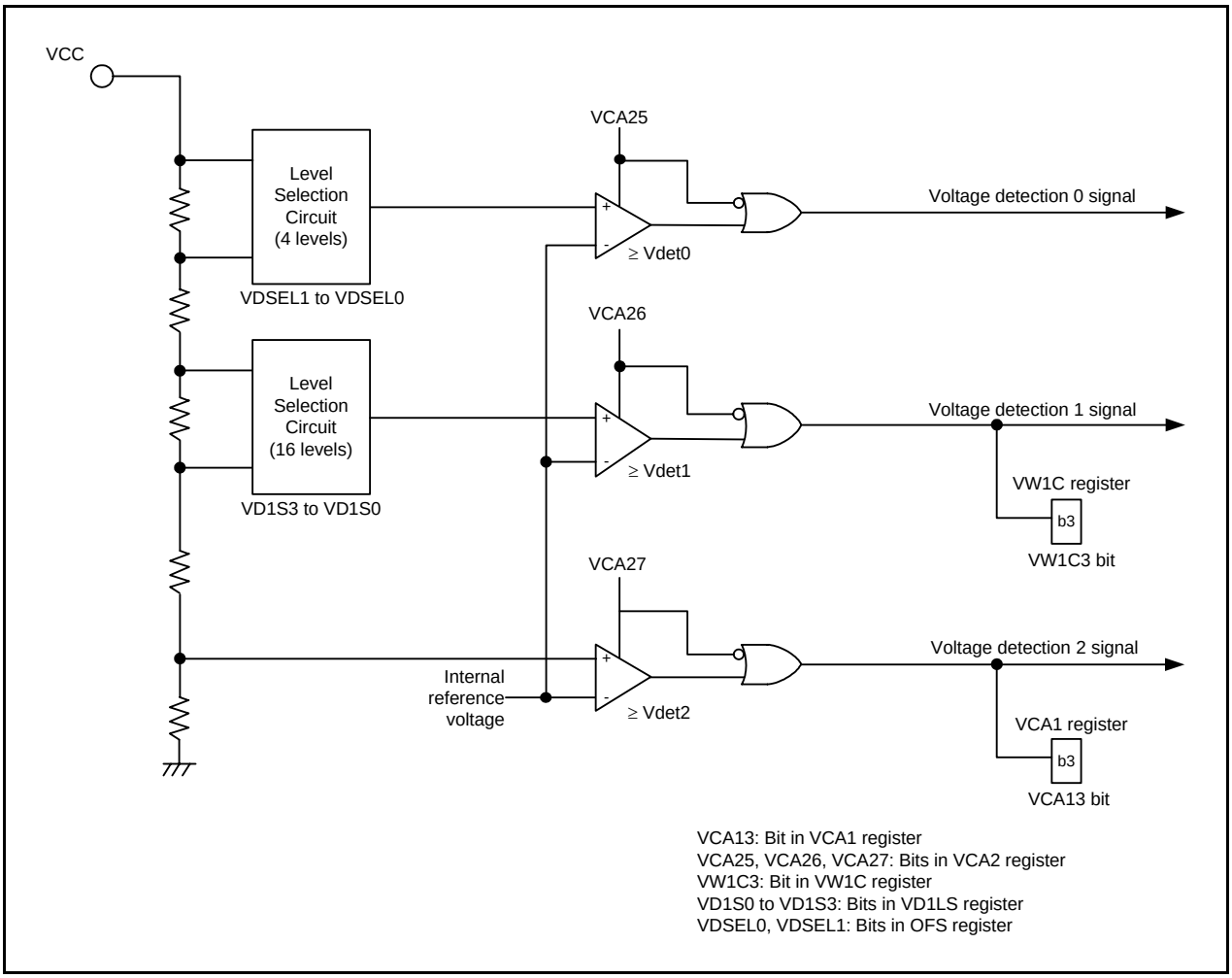


Figure 6.1 Voltage Detection Circuit Block Diagram

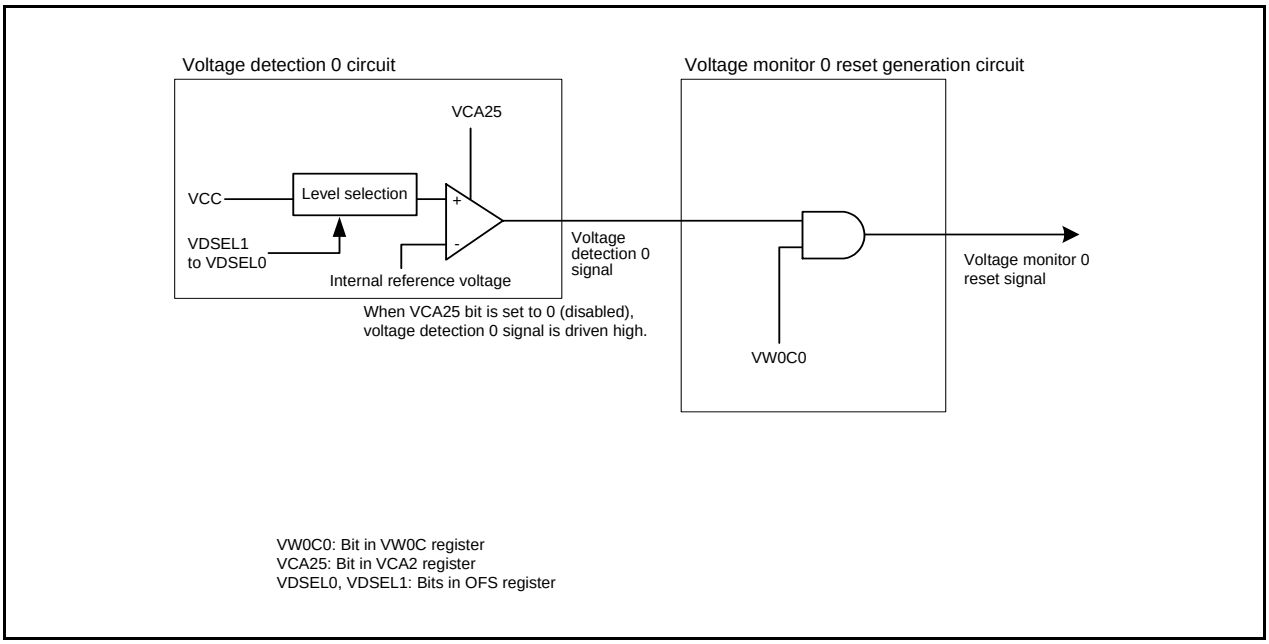


Figure 6.2 Block Diagram of Voltage Monitor 0 Reset Generation Circuit

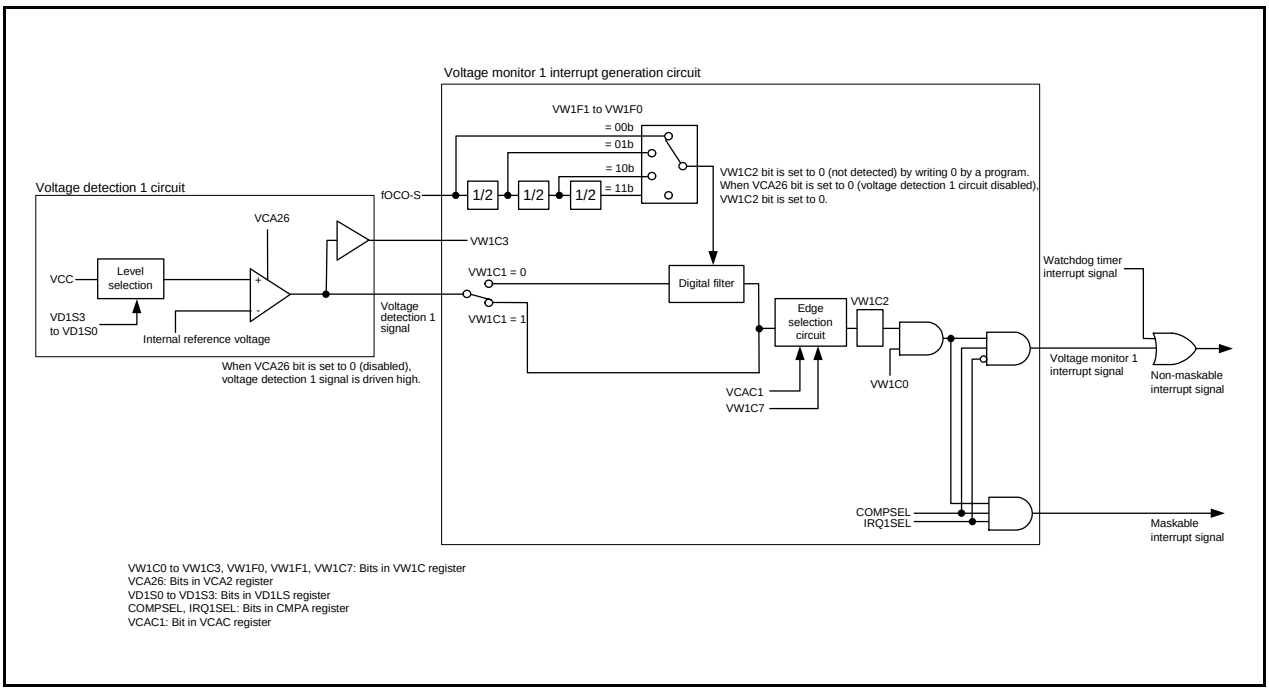


Figure 6.3 Block Diagram of Voltage Monitor 1 Interrupt Generation Circuit

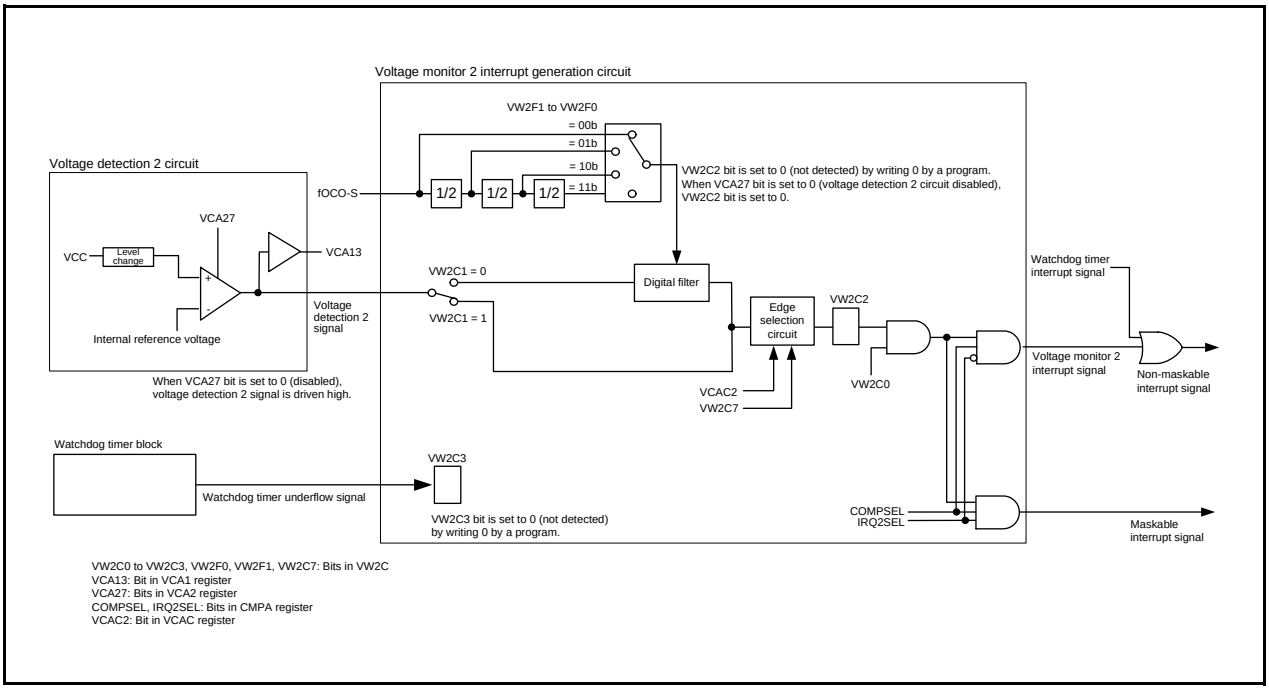


Figure 6.4 Block Diagram of Voltage Monitor 2 Interrupt Generation Circuit

6.2 Registers

6.2.1 Voltage Monitor Circuit Control Register (CMPA)

Address 0030h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	COMPSEL	—	IRQ2SEL	IRQ1SEL	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	—			
b3	—			
b4	IRQ1SEL	Voltage monitor 1 interrupt type select bit (1)	0: Non-maskable interrupt 1: Maskable interrupt	R/W
b5	IRQ2SEL	Voltage monitor 2 interrupt type select bit (2)	0: Non-maskable interrupt 1: Maskable interrupt	R/W
b6	—	Reserved bit	Set to 0.	R/W
b7	COMPSEL	Voltage monitor interrupt type selection enable bit (1, 2)	0: Bits IRQ1SEL and IRQ2SEL disabled 1: Bits IRQ1SEL and IRQ2SEL enabled	R/W

Notes:
1. When the VW1C0 bit in the VW1C register is set to 1 (enabled), do not set bits IRQ1SEL and COMPSEL simultaneously (with one instruction).
2. When the VW2C0 bit in the VW2C register is set to 1 (enabled), do not set bits IRQ2SEL and COMPSEL simultaneously (with one instruction).

6.2.2 Voltage Monitor Circuit Edge Select Register (VCAC)

Address 0031h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	VCAC2	VCAC1	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	VCAC1	Voltage monitor 1 circuit edge select bit (1)	0: One edge 1: Both edges	R/W
b2	VCAC2	Voltage monitor 2 circuit edge select bit (2)	0: One edge 1: Both edges	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—			
b5	—			
b6	—			
b7	—			

Notes:
1. When the VCAC1 bit is set tot 0 (one edge), the VW1C7 bit in the VW1C register is enabled. Set the VW1C7 bit after setting the VCAC1 bit to 0.
2. When the VCAC2 bit is set tot 0 (one edge), the VW2C7 bit in the VW2C register is enabled. Set the VW2C7 bit after setting the VCAC2 bit to 0.

6.2.3 Voltage Detect Register 1 (VCA1)

Address 0033h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	VCA13	—	—	—
After Reset	0	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	—			
b3	VCA13	Voltage detection 2 signal monitor flag (1)	0: VCC < Vdet2 1: VCC ≥ Vdet2 or voltage detection 2 circuit disabled	R
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—			
b7	—			

Note:
1. When the VCA27 bit in the VCA2 register is set to 1 (voltage detection 2 circuit enabled), the VCA13 bit is enabled.
   When the VCA27 bit in the VCA2 register is set to 0 (voltage detection 2 circuit disabled), the VCA13 bit is set to 1 (VCC ≥ Vdet2).

6.2.4 Voltage Detect Register 2 (VCA2)

Address 0034h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	VCA27	VCA26	VCA25	—	—	—	—	VCA20
After Reset	0	0	0	0	0	0	0	0

The above applies when the LVDAS bit in the OFS register is set to 1.

After Reset	0	0	1	0	0	0	0	0

The above applies when the LVDAS bit in the OFS register is set to 0.

Bit	Symbol	Bit Name	Function	R/W
b0	VCA20	Internal power low consumption enable bit (1)	0: Low consumption disabled 1: Low consumption enabled (2)	R/W
b1	—	Reserved bits	Set to 0.	R/W
b2	—			
b3	—			
b4	—			
b5	VCA25	Voltage detection 0 enable bit (3)	0: Voltage detection 0 circuit disabled 1: Voltage detection 0 circuit enabled	R/W
b6	VCA26	Voltage detection 1 enable bit (4)	0: Voltage detection 1 circuit disabled 1: Voltage detection 1 circuit enabled	R/W
b7	VCA27	Voltage detection 2 enable bit (5)	0: Voltage detection 2 circuit disabled 1: Voltage detection 2 circuit enabled	R/W

Notes:
1. Use the VCA20 bit only when the MCU enters wait mode. To set the VCA20 bit, follow the procedure shown in **Figure 9.3 Procedure for Reducing Internal Power Consumption Using VCA20 bit**.
2. When the VCA20 bit is set to 1 (low consumption enabled), do not set the CM10 bit in the CM1 register to 1 (stop mode).
3. When writing to the VCA25 bit, set a value after reset.
4. To use the voltage detection 1 interrupt or the VW1C3 bit in the VW1C register, set the VCA26 bit to 1. After the VCA26 bit is set to 1 from 0, allow td(E-A) to elapse before the voltage detection 1 circuit starts operation.
5. To use the voltage detection 2 interrupt or the VCA13 bit in the VCA1 register, set the VCA27 bit to 1. After the VCA27 bit is set to 1 from 0, allow td(E-A) to elapse before the voltage detection 2 circuit starts operation.

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VCA2 register.

6.2.5 Voltage Detection 1 Level Select Register (VD1LS)

Address 0036h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	VD1S3	VD1S2	VD1S1	VD1S0
After Reset	0	0	0	0	0	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	VD1S0	Voltage detection 1 level select bit (Reference voltage when the voltage falls)	b3 b2 b1 b0 0 0 0 0: 2.20 V (Vdet1_0) 0 0 0 1: 2.35 V (Vdet1_1) 0 0 1 0: 2.50 V (Vdet1_2) 0 0 1 1: 2.65 V (Vdet1_3) 0 1 0 0: 2.80 V (Vdet1_4) 0 1 0 1: 2.95 V (Vdet1_5) 0 1 1 0: 3.10 V (Vdet1_6) 0 1 1 1: 3.25 V (Vdet1_7) 1 0 0 0: 3.40 V (Vdet1_8) 1 0 0 1: 3.55 V (Vdet1_9) 1 0 1 0: 3.70 V (Vdet1_A) 1 0 1 1: 3.85 V (Vdet1_B) 1 1 0 0: 4.00 V (Vdet1_C) 1 1 0 1: 4.15 V (Vdet1_D) 1 1 1 0: 4.30 V (Vdet1_E) 1 1 1 1: 4.45 V (Vdet1_F)	R/W
b1	VD1S1			R/W
b2	VD1S2			R/W
b3	VD1S3			R/W
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—			
b7	—			

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VD1LS register.

6.2.6 Voltage Monitor 0 Circuit Control Register (VW0C)

Address 0038h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	VW0C0
After Reset	1	1	0	0	X	0	1	0

The above applies when the LVDAS bit in the OFS register is set to 1.

After Reset	1	1	0	0	X	0	1	1

The above applies when the LVDAS bit in the OFS register is set to 0.

Bit	Symbol	Bit Name	Function	R/W
b0	VW0C0	Voltage monitor 0 reset enable bit (1)	0: Disabled 1: Enabled	R/W
b1	—	Reserved bit	Set to 1.	R/W
b2	—	Reserved bit	Set to 0.	R/W
b3	—	Reserved bit	When read, the content is undefined.	R
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—	Reserved bits	Set to 1.	R/W
b7	—			

Note:

1. The VW0C0 bit is enabled when the VCA25 bit in the VCA2 register is set to 1 (voltage detection 0 circuit enabled).
   When writing to the VW0C0 bit, set a value after reset.

Set the PRC3 bit in the PRCR register to 1 (write enabled) before writing the VW0C register.

6.2.7 Voltage Monitor 1 Circuit Control Register (VW1C)

Address 0039h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	VW1C7	—	VW1F1	VW1F0	VW1C3	VW1C2	VW1C1	VW1C0
After Reset	1	0	0	0	1	0	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	VW1C0	Voltage monitor 1 interrupt enable bit (1)	0: Disabled 1: Enabled	R/W
b1	VW1C1	Voltage monitor 1 digital filter disable mode select bit (2, 6)	0: Digital filter enabled mode (digital filter circuit enabled) 1: Digital filter disable mode (digital filter circuit disabled)	R/W
b2	VW1C2	Voltage change detection flag (3, 4)	0: Not detected 1: Vdet1 passing detected	R/W
b3	VW1C3	Voltage detection 1 signal monitor flag (3)	0: VCC < Vdet1 1: VCC ≥ Vdet1 or voltage detection 1 circuit disabled	R
b4	VW1F0	Sampling clock select bit (6)	b5 b4 0 0: fOCO-S divided by 1 0 1: fOCO-S divided by 2 1 0: fOCO-S divided by 4 1 1: fOCO-S divided by 8	R/W
b5	VW1F1			R/W
b6	—	Reserved bit	Set to 0.	R/W
b7	VW1C7	Voltage monitor 1 interrupt generation condition select bit (5)	0: When VCC reaches Vdet1 or above 1: When VCC reaches Vdet1 or below	R/W

Notes:
1. The VW1C0 is enabled when the VCA26 bit in the VCA2 register is set to 1 (voltage detection 1 circuit enabled). Set the VW1C0 bit to 0 (disabled) when the VCA26 bit is set to 0 (voltage detection 1 circuit disabled).
   To set the VW0C0 bit to 1 (enabled), follow the procedure shown in **Table 6.2 Procedure for Setting Bits Associated with Voltage Monitor 1 Interrupt**.
2. When using the digital filter (while the VW1C1 bit is 0), set the CM14 bit in the CM1 register to 0 (low-speed on-chip oscillator on).
   To use the voltage monitor 1 interrupt to exit stop mode, set the VW1C1 bit in the VW1C register to 1 (digital filter disabled).
3. Bits VW1C2 and VW1C3 are enabled when the VCA26 bit in the VCA2 register is set to 1 (voltage detection 1 circuit enabled).
4. Set the VW1C2 bit to 0 by a program. When 0 is written by a program, this bit is set to 0 (and remains unchanged even if 1 is written to it).
5. The VW1C7 bit is enabled when the VCAC1 bit in the VCAC register is set to 0 (one edge). After setting the VCAC1 bit to 0, set the VW1C7 bit.
6. When the VW1C0 bit is set to 1 (enabled), do not set the VW1C1 bit and bits VW1F1 and VW1F0 simultaneously (with one instruction).

   Set the PRC3 bit in the PRCR register to 1 (write enabled) before writing the VW1C register.
   Rewriting the VW1C register may set the VW1C2 bit to 1. Set the VW1C2 bit to 0 after rewriting the VW1C register.

6.2.8 Voltage Monitor 2 Circuit Control Register (VW2C)

Address 003Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	VW2C7	—	VW2F1	VW2F0	VW2C3	VW2C2	VW2C1	VW2C0
After Reset	1	0	0	0	0	0	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	VW2C0	Voltage monitor 2 interrupt enable bit (1)	0: Disabled 1: Enabled	R/W
b1	VW2C1	Voltage monitor 2 digital filter disable mode select bit (2, 6)	0: Digital filter enable mode (digital filter circuit enabled) 1: Digital filter disable mode (digital filter circuit disabled)	R/W
b2	VW2C2	Voltage change detection flag (3, 4)	0: Not detected 1: Vdet2 passing detected	R/W
b3	VW2C3	WDT detection monitor flag (4)	0: Not detected 1: Detected	R/W
b4	VW2F0	Sampling clock select bit (6)	b5 b4 0 0: fOCO-S divided by 1 0 1: fOCO-S divided by 2 1 0: fOCO-S divided by 4 1 1: fOCO-S divided by 8	R/W
b5	VW2F1			R/W
b6	—	Reserved bit	Set to 0.	R/W
b7	VW2C7	Voltage monitor 2 interrupt generation condition select bit (5)	0: When VCC reaches Vdet2 or above 1: When VCC reaches Vdet2 or below	R/W

Notes:

1. The VW2C0 is enabled when the VCA27 bit in the VCA2 register is set to 1 (voltage detection 2 circuit enabled). Set the VW2C0 bit to 0 (disabled) when the VCA27 bit is set to 0 (voltage detection 2 circuit disabled).
   To set the VW2C0 bit to 1 (enabled), follow the procedure shown in **Table 6.3 Procedure for Setting Bits Associated with Voltage Monitor 2 Interrupt**.
2. When using the digital filter (while the VW2C1 bit is 0), set the CM14 bit in the CM1 register to 0 (low-speed on-chip oscillator on).
   To use the voltage monitor 2 interrupt to exit stop mode, set the VW2C1 bit in the VW2C register to 1 (digital filter disabled).
3. The VW2C2 bit is enabled when the VCA27 bit in the VCA2 register is set to 1 (voltage detection 2 circuit enabled).
4. Set this bit to 0 by a program. When 0 is written by a program, this bit is set to 0 (and remains unchanged even if 1 is written to it).
5. The VW2C7 bit is enabled when the VCAC2 bit in the VCAC register is set to 0 (one edge). After setting the VCAC2 bit to 0, set the VW2C7 bit.
6. When the VW2C0 bit is set to 1 (enabled), do not set the VW2C1 bit and bits VW2F1 and VW2F0 simultaneously (with one instruction).

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VW2C register.
Rewriting the VW2C register may set the VW2C2 bit to 1. After rewriting this register, set the VW2C2 bit to 0.

6.2.9 Option Function Select Register (OFS)

Address 0FFFFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CSPROINI	LVDAS	VDSEL1	VDSEL0	ROMCP1	ROMCR	—	WDTON
After Reset	User Setting Value (1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTON	Watchdog timer start select bit	0: Watchdog timer automatically starts after reset 1: Watchdog timer is stopped after reset	R/W
b1	—	Reserved bit	Set to 1.	R/W
b2	ROMCR	ROM code protect disable bit	0: ROM code protect disabled 1: ROMCP1 bit enabled	R/W
b3	ROMCP1	ROM code protect bit	0: ROM code protect enabled 1: ROM code protect disabled	R/W
b4	VDSEL0	Voltage detection 0 level select bit (2)	b5 b4 0 0: 3.80 V selected (Vdet0_3) 0 1: 2.85 V selected (Vdet0_2) 1 0: 2.35 V selected (Vdet0_1) 1 1: 1.90 V selected (Vdet0_0)	R/W
b5	VDSEL1			R/W
b6	LVDAS	Voltage detection 0 circuit start bit (3)	0: Voltage monitor 0 reset enabled after reset 1: Voltage monitor 0 reset disabled after reset	R/W
b7	CSPROINI	Count source protection mode after reset select bit	0: Count source protect mode enabled after reset 1: Count source protect mode disabled after reset	R/W

Notes:
1. The OFS register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the OFS register. If the block including the OFS register is erased, the OFS register is set to FFh.
   When blank products are shipped, the OFS register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS register is the value programmed by the user.
2. The same level of the voltage detection 0 level selected by bits VDSEL0 and VDESL1 is set in both functions of voltage monitor 0 reset and power-on reset.
3. To use power-on reset and voltage monitor 0 reset, set the LVDAS bit to 0 (voltage monitor 0 reset enabled after reset).

For a setting example of the OFS register, refer to **13.3.1 Setting Example of Option Function Select Area**.

LVDAS Bit (Voltage Detection 0 Circuit Start Bit)

The Vdet0 voltage to be monitored by the voltage detection 0 circuit is selected by bits VDSEL0 and VDSEL1.

6.3 VCC Input Voltage

6.3.1 Monitoring Vdet0

Vdet0 cannot be monitored.

6.3.2 Monitoring Vdet1

Once the following settings are made, the comparison result of voltage monitor 1 can be monitored by the VW1C3 bit in the VW1C register after td(E-A) has elapsed (refer to **31. Electrical Characteristics**).

(1) Set bits VD1S3 to VD1S0 in the VD1LS register (voltage detection 1 detection voltage).
(2) Set the VCA26 bit in the VCA2 register to 1 (voltage detection 1 circuit enabled).

6.3.3 Monitoring Vdet2

Once the following settings are made, the comparison result of voltage monitor 2 can be monitored by the VCA13 bit in the VCA1 register after td(E-A) has elapsed (refer to **31. Electrical Characteristics**).

- Set the VCA27 bit in the VCA2 register to 1 (voltage detection 2 circuit enabled).

6.4 Voltage Monitor 0 Reset

To use voltage monitor 0 reset, set the LVDAS bit in the OFS register to 0 (voltage monitor 0 reset enabled after reset).

Figure 6.5 shows an Operating Example of Voltage Monitor 0 Reset.

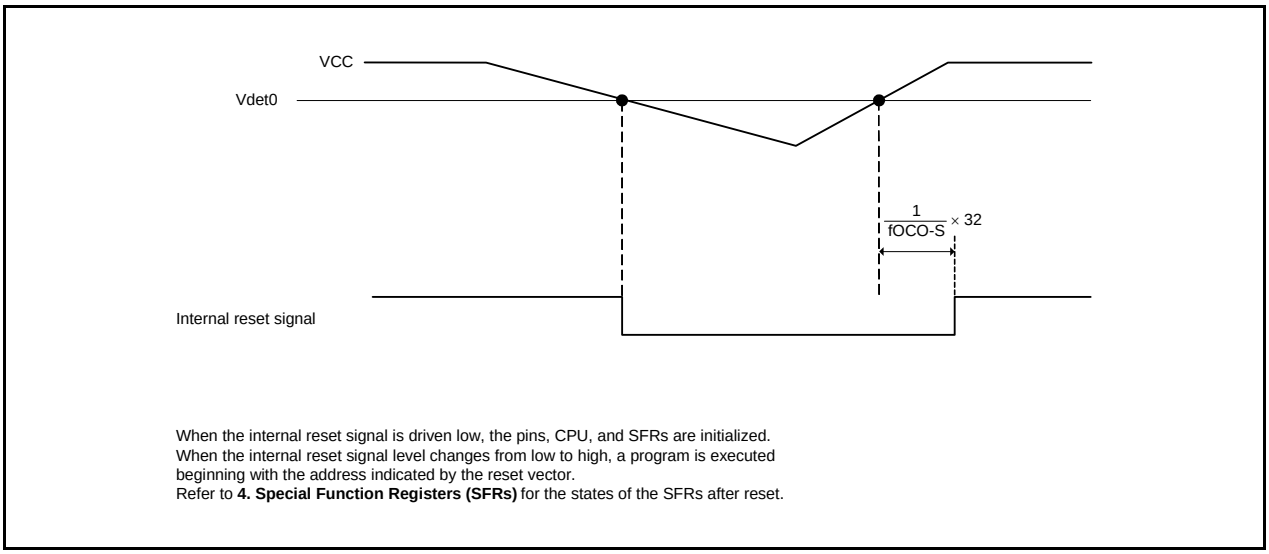


Figure 6.5 Operating Example of Voltage Monitor 0 Reset

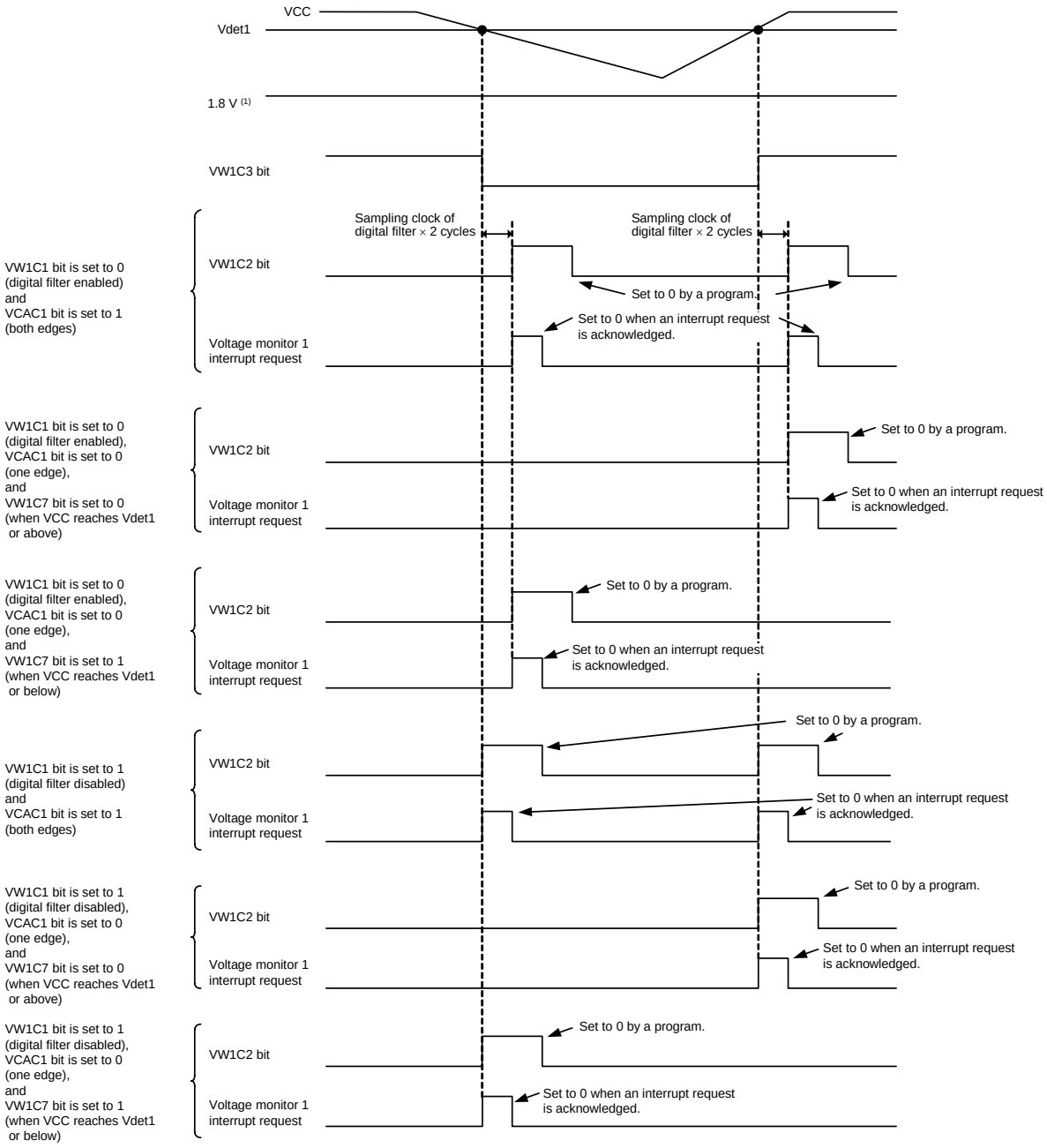
6.5 Voltage Monitor 1 Interrupt

Table 6.2 lists the Procedure for Setting Bits Associated with Voltage Monitor 1 Interrupt. Figure 6.6 shows an Operating Example of Voltage Monitor 1 Interrupt.
To use the voltage monitor 1 interrupt to exit stop mode, set the VW1C1 bit in the VW1C register to 1 (digital filter disabled).

Table 6.2 Procedure for Setting Bits Associated with Voltage Monitor 1 Interrupt

Step	When Using Digital Filter	When Using No Digital Filter
1	Select the voltage detection 1 detection voltage by bits VD1S3 to VD1S0 in the VD1LS register.	
2	Set the VCA26 bit in the VCA2 register to 1 (voltage detection 1 circuit enabled).	
3	Wait for td(E-A).	
4	Set the COMPSEL bit in the CMPA register to 1.	
5 (1)	Select the interrupt type by the IRQ1SEL in the CMPA register.	
6	Select the sampling clock of the digital filter by bits VW1F0 and VW1F1 in the VW1C register.	Set the VW1C1 bit in the VW1C register to 1 (digital filter disabled).
7 (2)	Set the VW1C1 bit in the VW1C register to 0 (digital filter enabled).	—
8	Select the interrupt request timing by the VCAC1 bit in the VCAC register and the VW1C7 bit in the VW1C register.	
9	Set the VW1C2 bit in the VW1C register to 0.	
10	Set the CM14 bit in the CM1 register to 0 (low-speed on-chip oscillator on)	—
11	Wait for 2 cycles of the sampling clock of the digital filter	— (No wait time required)
12 (3)	Set the VW1C0 bit in the VW1C register to 1 (voltage monitor 1 interrupt enabled)	

Notes:
1. When the VW1C0 bit is set to 0, steps 4 and 5 can be executed simultaneously (with one instruction).
2. When the VW1C0 bit is set to 0, steps 6 and 7 can be executed simultaneously (with one instruction).
3. When the voltage detection 1 circuit is enabled while the voltage monitor 1 interrupt is disabled, low voltage is detected and the VW1C2 bit becomes 1.
   When low voltage is detected after the voltage detection 1 circuit is enabled until an interrupt is enabled for the setting procedure of bits associated with voltage monitor 1 interrupt, an interrupt is not generated. After an interrupt is enabled, read the VW1C2 bit. When the bit is read as 1, perform the process that occurs when low voltage is detected.



VW1C1, VW1C2, VW1C3, VW1C7: Bits in VW1C register
VCAC1: Bit in VCAC register

The above applies when:
- VCA26 bit in VCA2 register = 1 (voltage detection 1 circuit enabled)
- VW1C0 bit in VW1C register = 1 (voltage monitor 1 interrupt enabled)

Note:
1. If voltage monitor 0 reset is not used, set the power supply to VCC ≥ 1.8 V.

Figure 6.6 Operating Example of Voltage Monitor 1 Interrupt

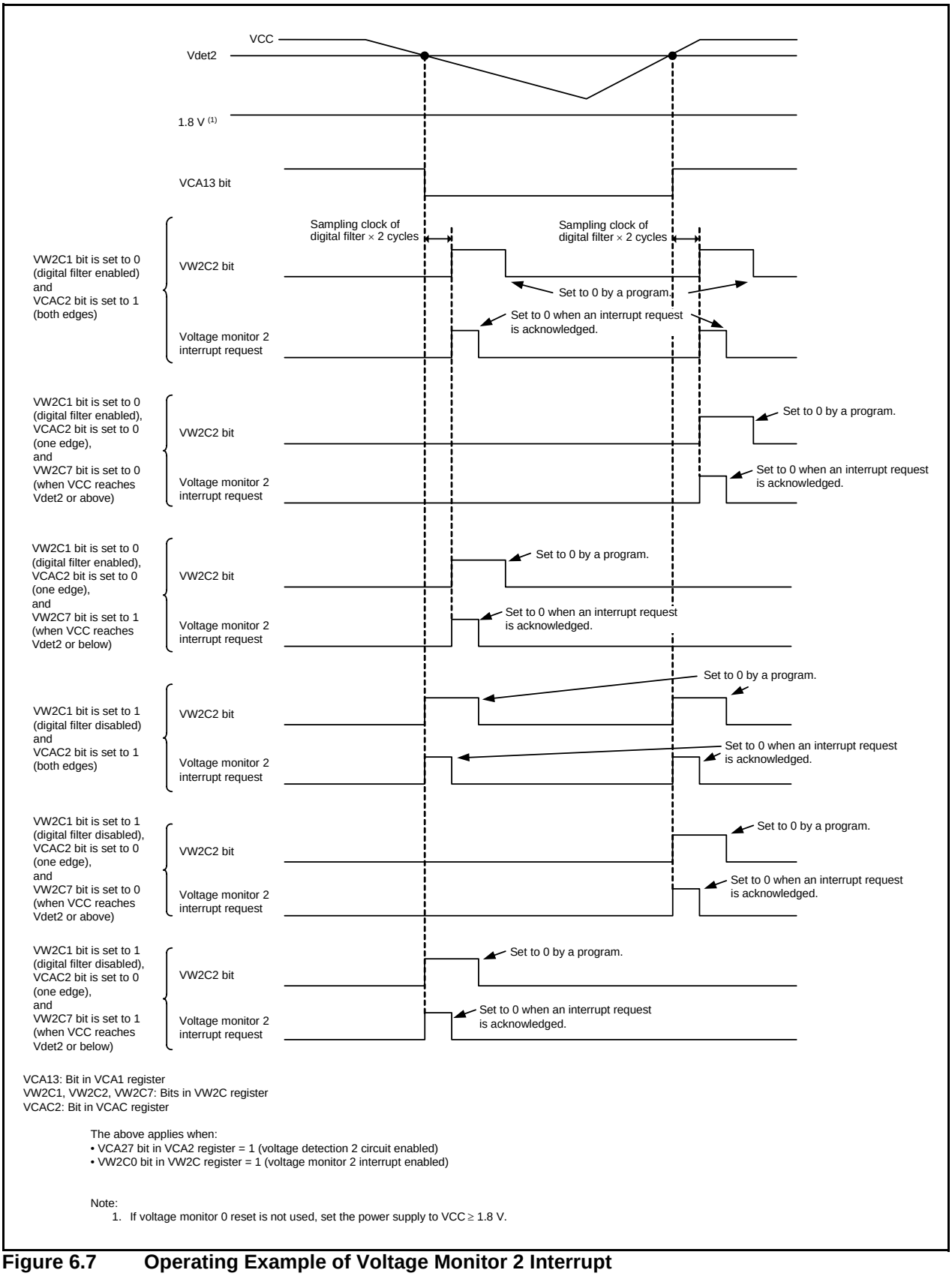
6.6 Voltage Monitor 2 Interrupt

Table 6.3 lists the Procedure for Setting Bits Associated with Voltage Monitor 2 Interrupt. Figure 6.7 shows an Operating Example of Voltage Monitor 2 Interrupt.
To use the voltage monitor 2 interrupt to exit stop mode, set the VW2C1 bit in the VW2C register to 1 (digital filter disabled).

Table 6.3 Procedure for Setting Bits Associated with Voltage Monitor 2 Interrupt

Step	When Using Digital Filter	When Using No Digital Filter
1	Set the VCA27 bit in the VCA2 register to 1 (voltage detection 2 circuit enabled).	
2	Wait for td(E-A).	
3	Set the COMPSEL bit in the CMPA register to 1.	
4 (1)	Select the interrupt type by the IRQ2SEL in the CMPA register.	
5	Select the sampling clock of the digital filter by bits VW2F0 and VW2F1 in the VW2C register.	Set the VW2C1 bit in the VW2C register to 1 (digital filter disabled).
6 (2)	Set the VW2C1 bit in the VW2C register to 0 (digital filter enabled).	—
7	Select the interrupt request timing by the VCAC2 bit in the VCAC register and the VW2C7 bit in the VW2C register.	
8	Set the VW2C2 bit in the VW2C register to 0.	
9	Set the CM14 bit in the CM1 register to 0 (low-speed on-chip oscillator on).	—
10	Wait for 2 cycles of the sampling clock of the digital filter.	— (No wait time required)
11 (3)	Set the VW2C0 bit in the VW2C register to 1 (voltage monitor 2 interrupt enabled).	

Notes:
1. When the VW2C0 bit is set to 0, steps 3 and 4 can be executed simultaneously (with one instruction).
2. When the VW2C0 bit is set to 0, steps 5 and 6 can be executed simultaneously (with one instruction).
3. When the voltage detection 2 circuit is enabled while the voltage monitor 2 interrupt is disabled, low voltage is detected and the VW2C2 bit becomes 1.
   When low voltage is detected after the voltage detection 2 circuit is enabled until an interrupt is enabled for the setting procedure of bits associated with voltage monitor 2 interrupt, an interrupt is not generated. After an interrupt is enabled, read the VW2C2 bit. When the bit is read as 1, perform the process that occurs when low voltage is detected.



VCA13: Bit in VCA1 register
VW2C1, VW2C2, VW2C7: Bits in VW2C register
VCAC2: Bit in VCAC register

The above applies when:
- VCA27 bit in VCA2 register = 1 (voltage detection 2 circuit enabled)
- VW2C0 bit in VW2C register = 1 (voltage monitor 2 interrupt enabled)

Note:
1. If voltage monitor 0 reset is not used, set the power supply to VCC ≥ 1.8 V.

Figure 6.7 Operating Example of Voltage Monitor 2 Interrupt

7. I/O Ports

Note

The description offered in this chapter is based on the R8C/3MK Group.
For R8C/3MU Group, refer to **1.1.2 Differences between Groups**.

There are 30 I/O ports: P0_0 to P0_4, P0_7, P1_0 to P1_7, P3_0, P3_3 to P3_5, P3_7, P4_5 to P4_7, P6_5 to P6_7, P7_6, P7_7, and P8_1 to P8_3. (P4_6 and P4_7 can be used as I/O ports if the XIN clock oscillation circuit is not used.)
Table 7.1 lists an Overview of I/O Ports.

Table 7.1 Overview of I/O Ports

Ports	I/O	Type of Output	I/O Setting	Internal Pull-Up Resister	Drive Capacity Switch	Input Level Switch
P0_0 to P0_3	I/O	CMOS3 state	Set in 1-bit units	Set in 4-bit units (1)	Set in 4-bit units (3)	Set in 6-bit units (4)
P0_4, P0_7	I/O	CMOS3 state	Set in 1-bit units	Set in 2-bit units (1)	Set in 2-bit units (3)	
P1	I/O	CMOS3 state	Set in 1-bit units	Set in 4-bit units (1)	Set in 1-bit units (2)	Set in 8-bit units (4)
P3_0, P3_3	I/O	CMOS3 state	Set in 1-bit units	Set in 2-bit units (1)	Set in 2-bit units (3)	Set in 5-bit units (4)
P3_4, P3_5, P3_7	I/O	CMOS3 state	Set in 1-bit units	Set in 3-bit units (1)	Set in 3-bit units (3)	
P4_5, P4_6 (5), P4_7 (5)	I/O	CMOS3 state	Set in 1-bit units	Set in 3-bit units (1)	Set in 3-bit units (3)	Set in 3-bit units (4)
P6_5 to P6_7	I/O	CMOS3 state	Set in 1-bit units	Set in 3-bit units (1)	Set in 3-bit units (3)	Set in 3-bit units (4)
P7_6, P7_7	I/O	CMOS3 state	Set in 1-bit units	Set in 2-bit units (1)	Set in 2-bit units (3)	Set in 2-bit units (4)
P8_1 to P8_3	I/O	CMOS3 state	Set in 1-bit units	Set in 3-bit units (1)	Set in 3-bit units (3)	Set in 3-bit units (4)

Notes:
1. In input mode, whether an internal pull-up resistor is connected or not can be selected by registers PUR0, PUR1, and PUR2.
2. Whether the drive capacity of the output transistor is set to low or high can be selected using register P1DRR.
3. Whether the drive capacity of the output transistor is set to low or high can be selected using registers DRR0, DRR1, and DRR2.
4. The input threshold value can be selected among three voltage levels (0.35 VCC, 0.50 VCC, and 0.70 VCC) using registers VLT0, VLT1, and VLT2.
5. When the XIN clock oscillation circuit is not used, these ports can be used as I/O ports.

7.1 Functions of I/O Ports

The PDi_j (j = 0 to 7) bit in the PDi (i = 0, 1, 3, 4, 6 to 8) register controls I/O of the ports P0_0 to P0_4, P0_7, P1_0 to P1_7, P3_0, P3_3 to P3_5, P3_7, P4_5 to P4_7, P6_5 to P6_7, P7_6, P7_7, and P8_1 to P8_3. The Pi register consists of a port latch to hold output data and a circuit to read pin states.
Figures 7.1 to 7.14 show the Configurations of I/O Ports. Table 7.2 lists the Functions of I/O Ports.

Table 7.2 Functions of I/O Ports

Operation When Accessing Pi Register	Value of PDi_j Bit in PDi Register	
	When PDi_j Bit is Set to 0 (Input Mode)	When PDi_j Bit is Set to 1 (Output Mode)
Read	Read the pin input level.	Read the port latch.
Write	Write to the port latch.	Write to the port latch. The value written to the port latch is output from the pin.

i = 0, 1, 3, 4, 6 to 8, j = 0 to 7

7.2 Effect on Peripheral Functions

I/O ports function as I/O ports for peripheral functions (refer to **Table 1.6 Pin Name Information by Pin Number**).
Table 7.3 lists the Setting of PDi_j Bit when Functioning as I/O Ports for Peripheral Functions (i = 0, 1, 3, 4, 6 to 8, j = 0 to 7).
Refer to the description of each function for information on how to set peripheral functions.

Table 7.3 Setting of PDi_j Bit when Functioning as I/O Ports for Peripheral Functions (i = 0, 1, 3, 4, 6 to 8, j = 0 to 7)

I/O of Peripheral Function	PDi_j Bit Settings for Shared Pin Function
Input	Set this bit to 0 (input mode).
Output	This bit can be set to either 0 or 1 (output regardless of the port setting).

7.3 Pins Other than I/O Ports

Figure 7.15 shows the Configuration of I/O Pins.

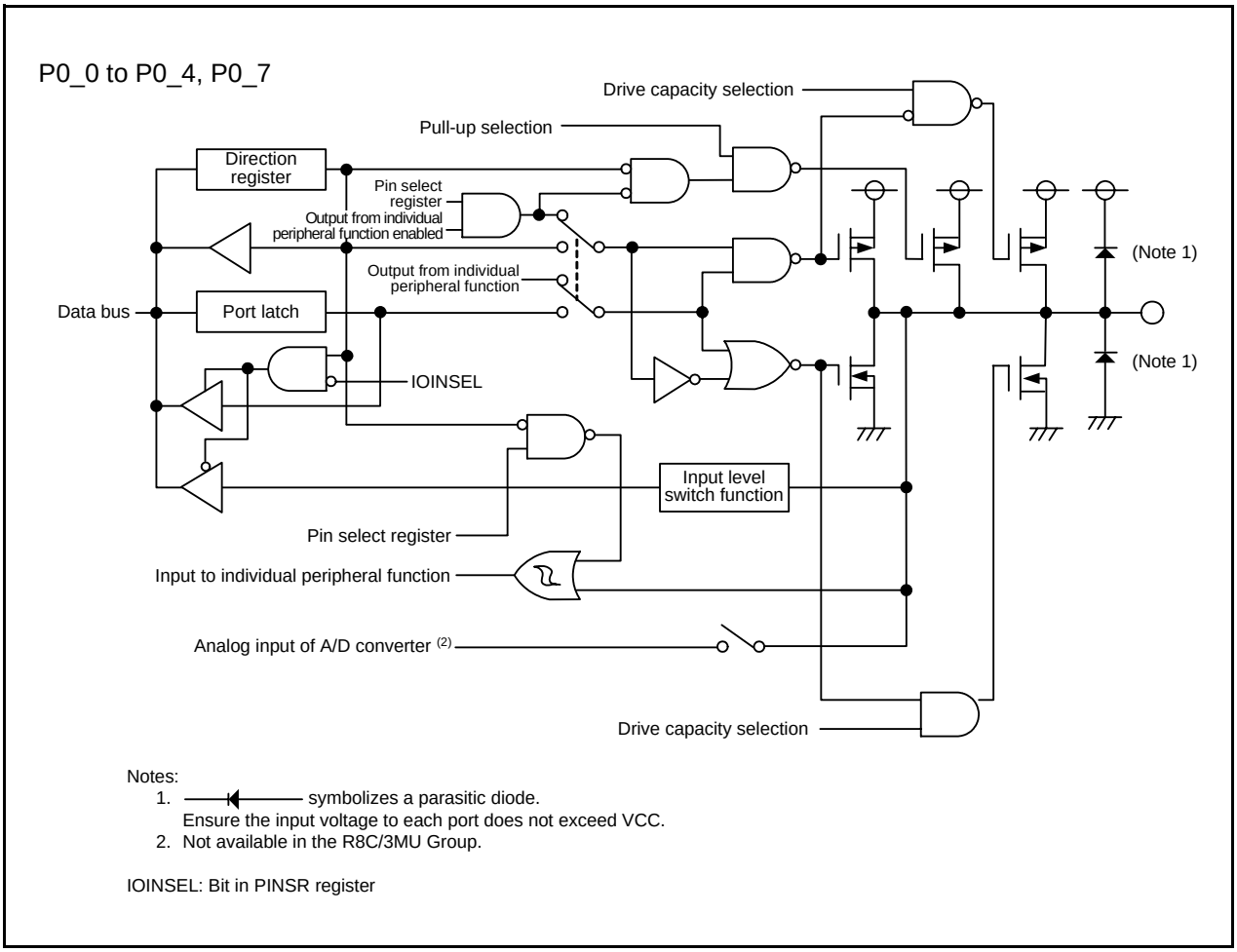


Figure 7.1 Configuration of I/O Ports (1)

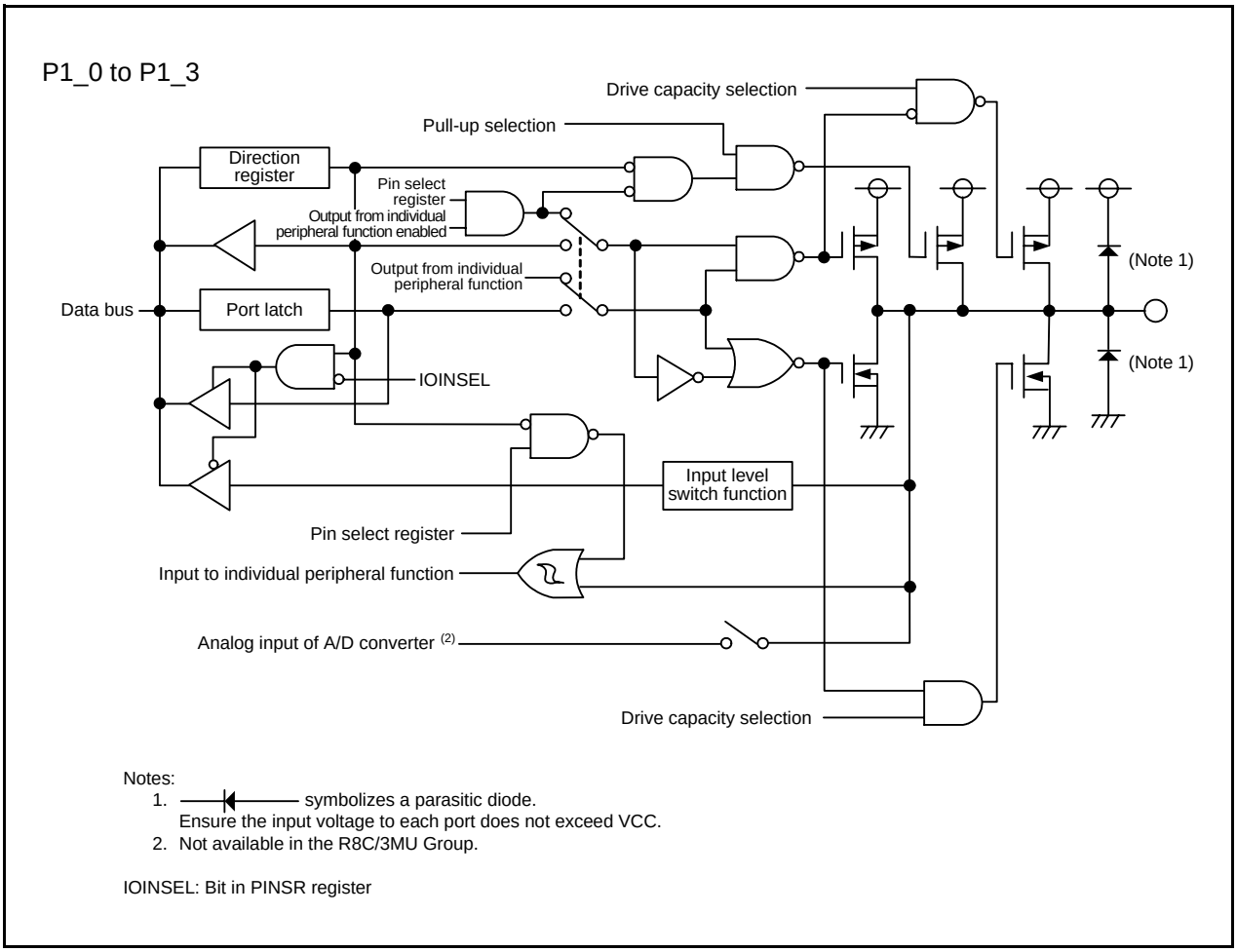


Figure 7.2 Configuration of I/O Ports (2)

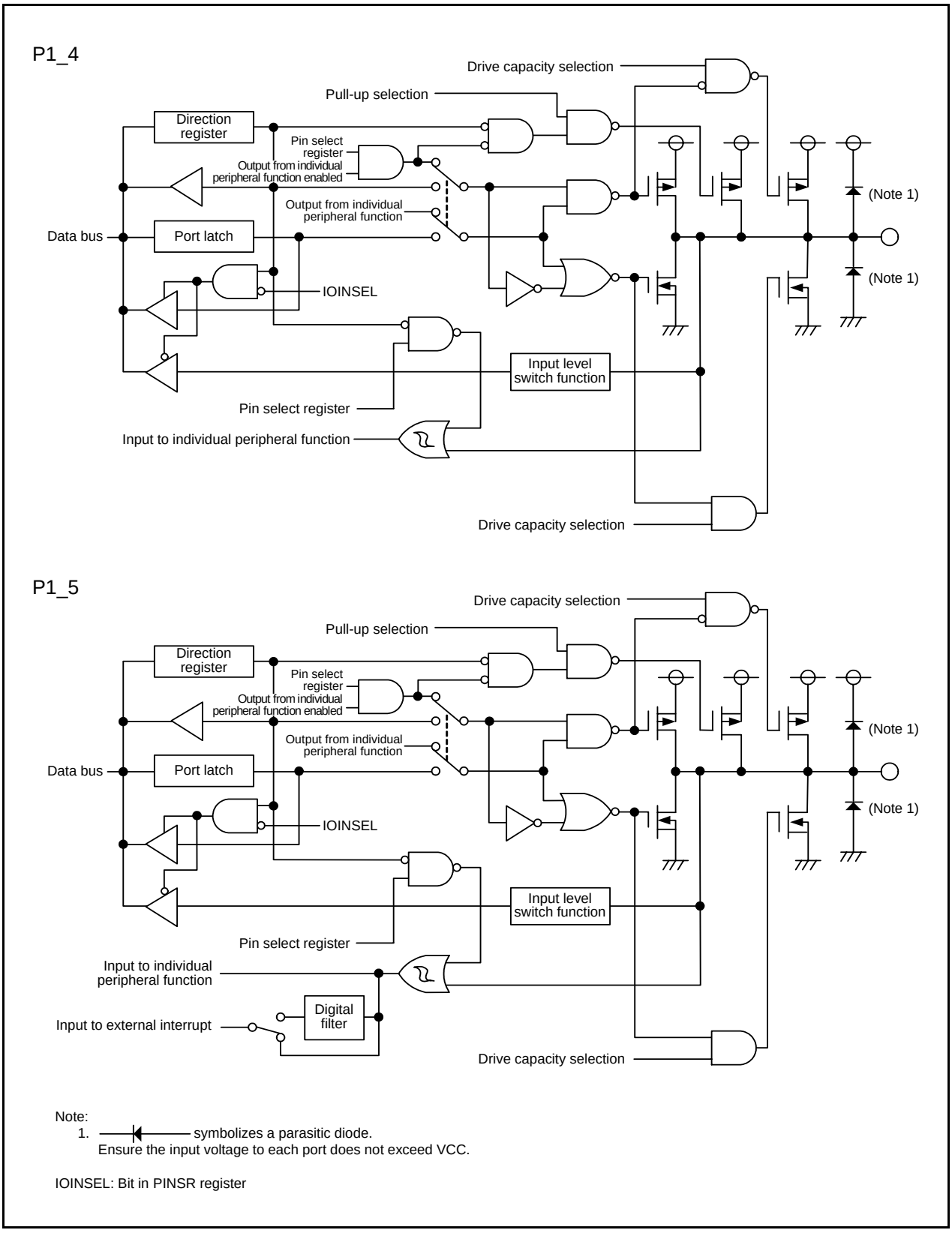
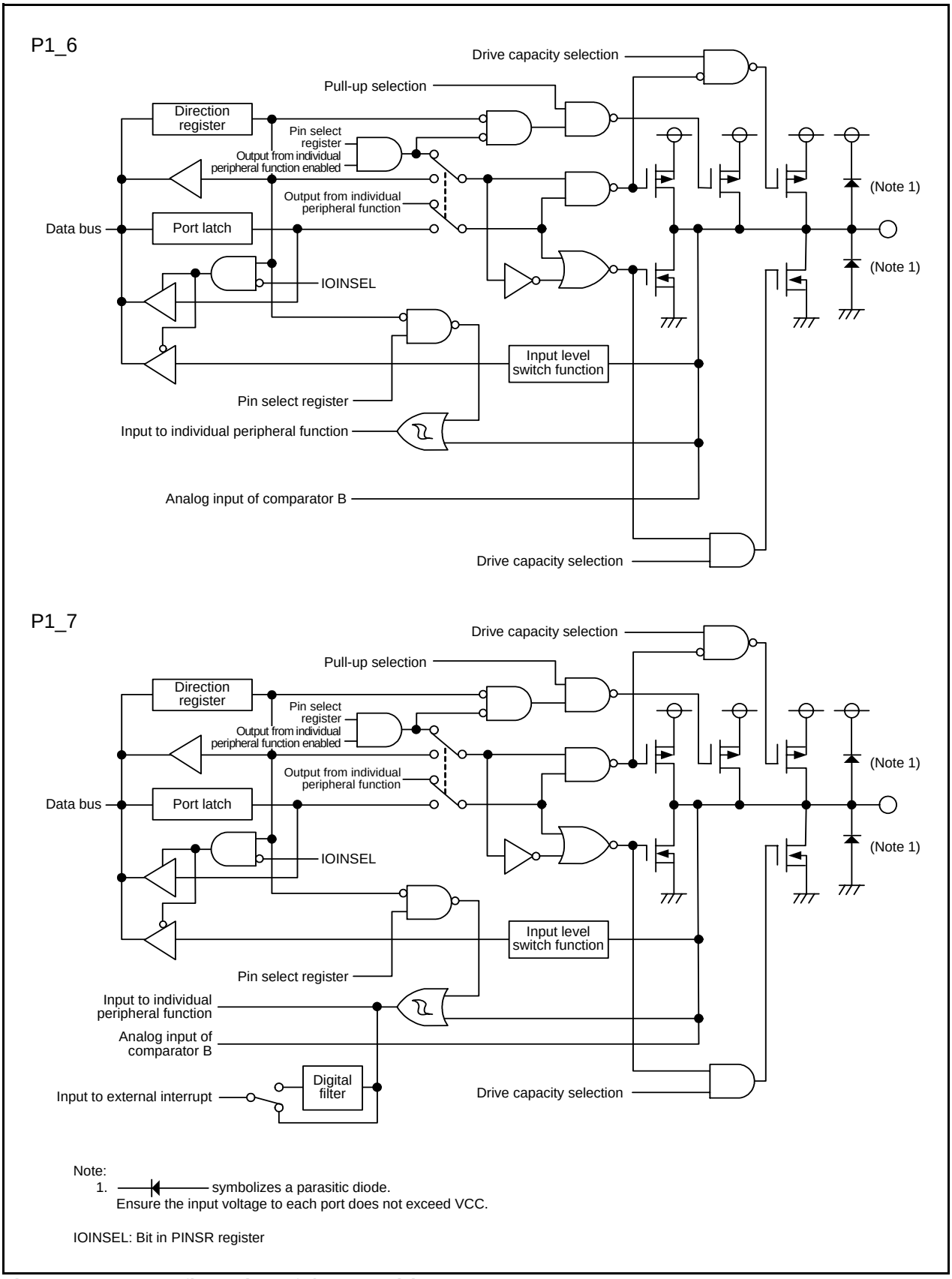


Figure 7.3 Configuration of I/O Ports (3)



Note:
1. ⟵ symbolizes a parasitic diode.
Ensure the input voltage to each port does not exceed VCC.

IOINSEL: Bit in PINSR register

Figure 7.4 Configuration of I/O Ports (4)

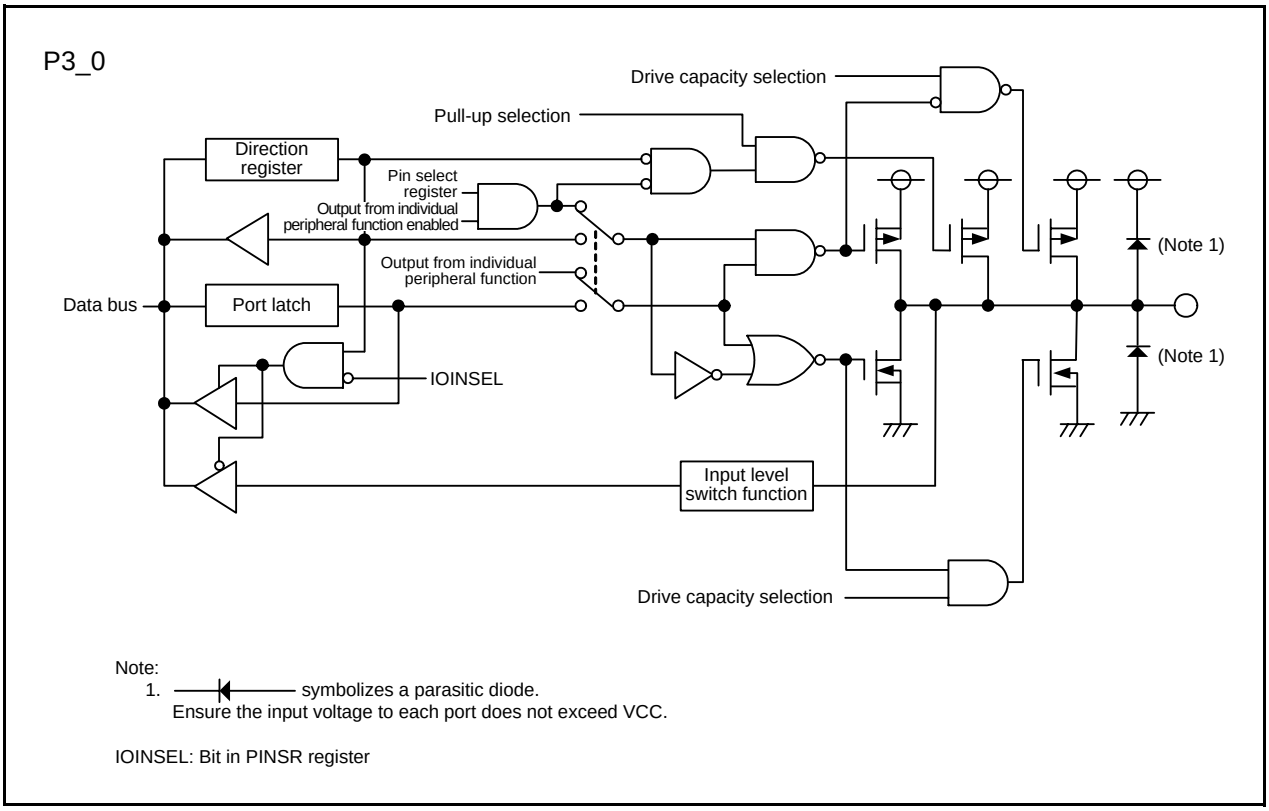


Figure 7.5 Configuration of I/O Ports (5)

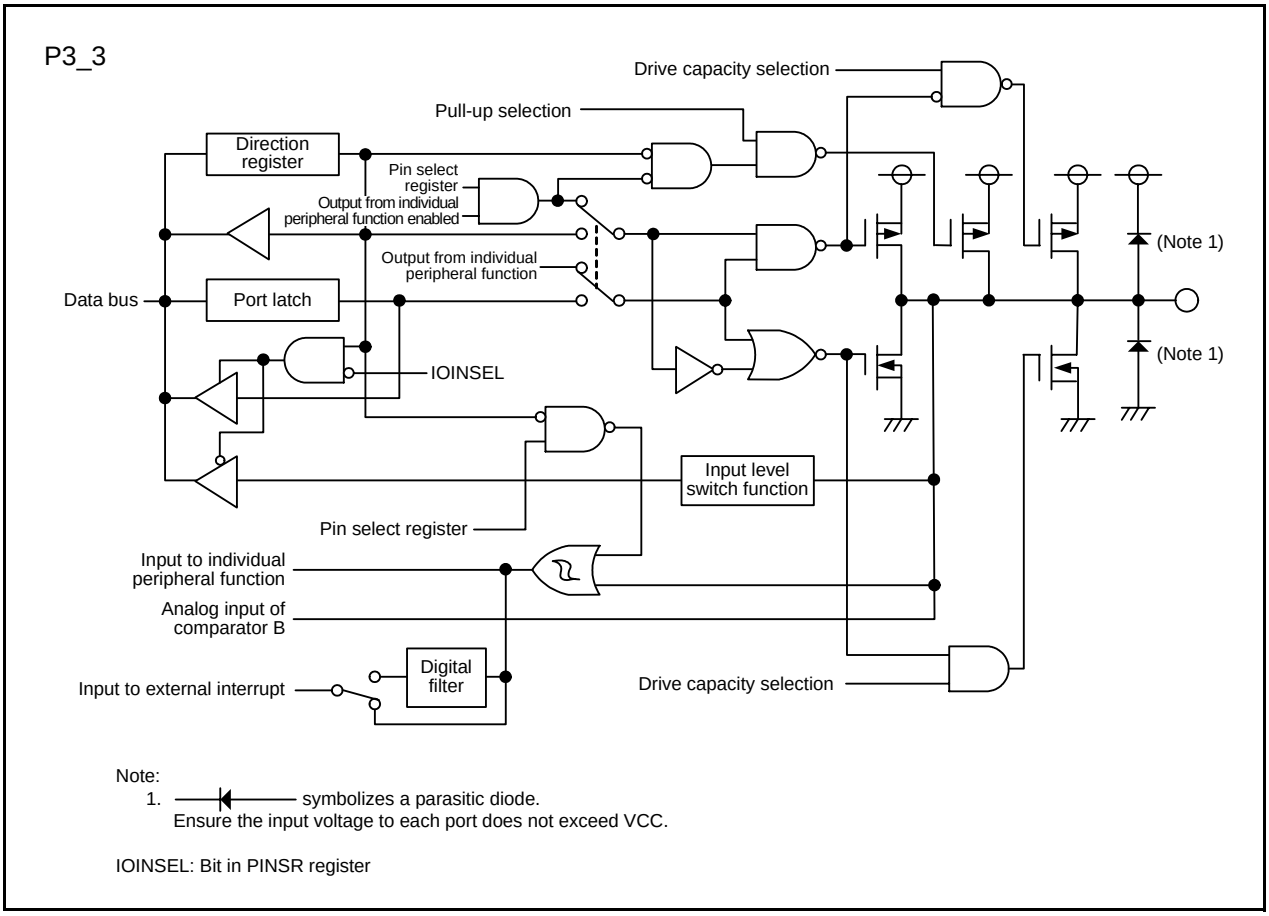


Figure 7.6 Configuration of I/O Ports (6)

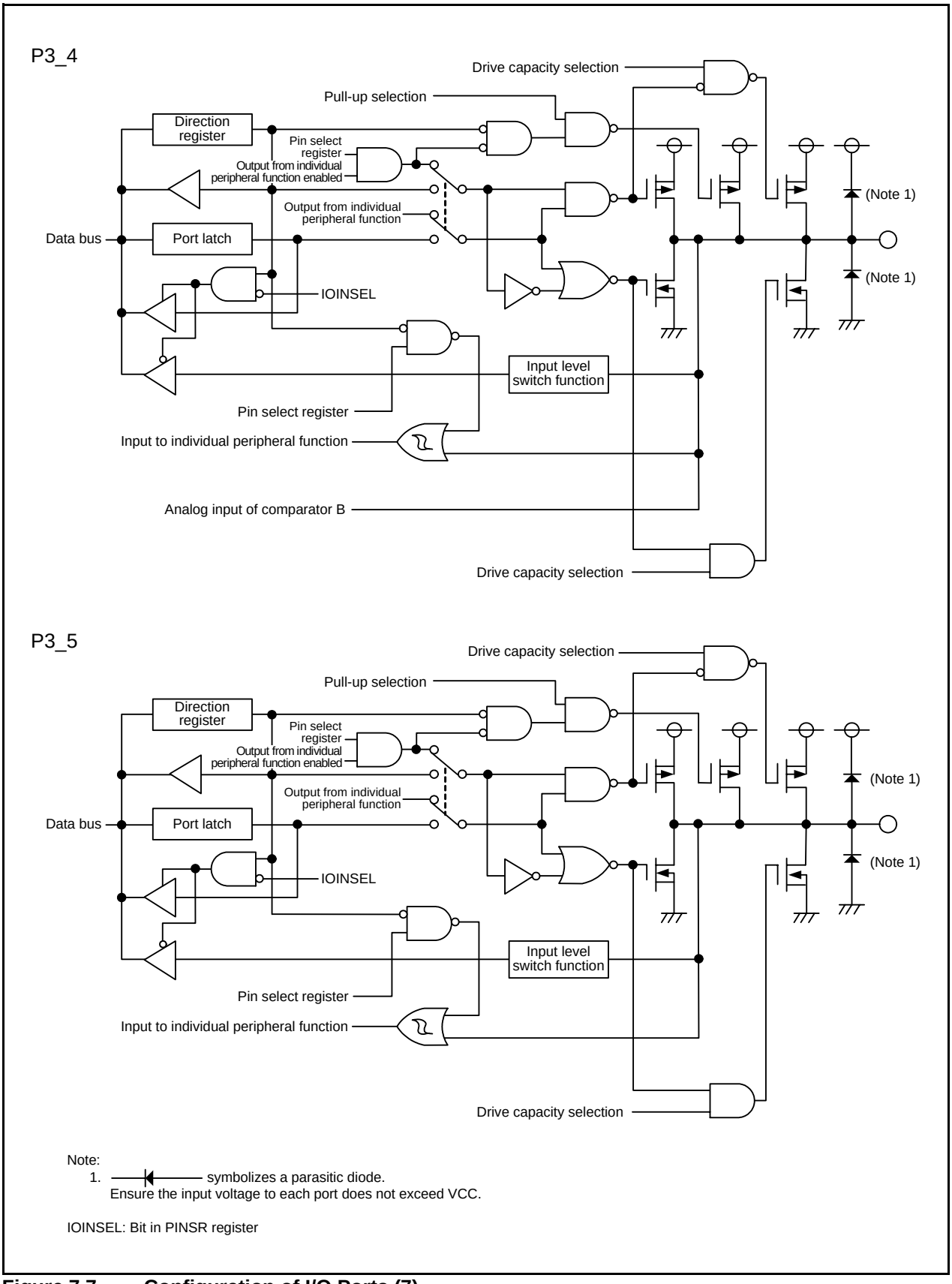


Figure 7.7 Configuration of I/O Ports (7)

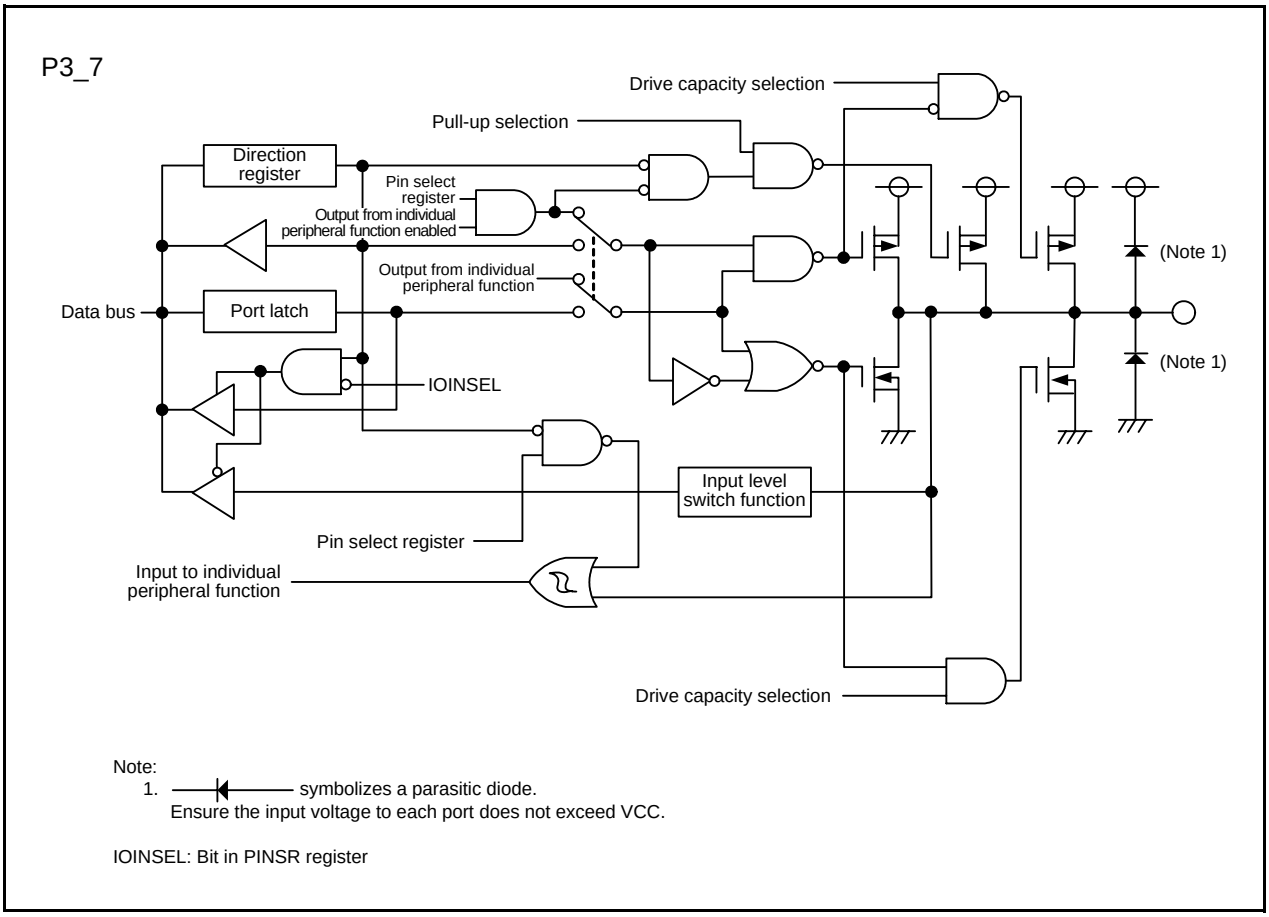


Figure 7.8 Configuration of I/O Ports (8)

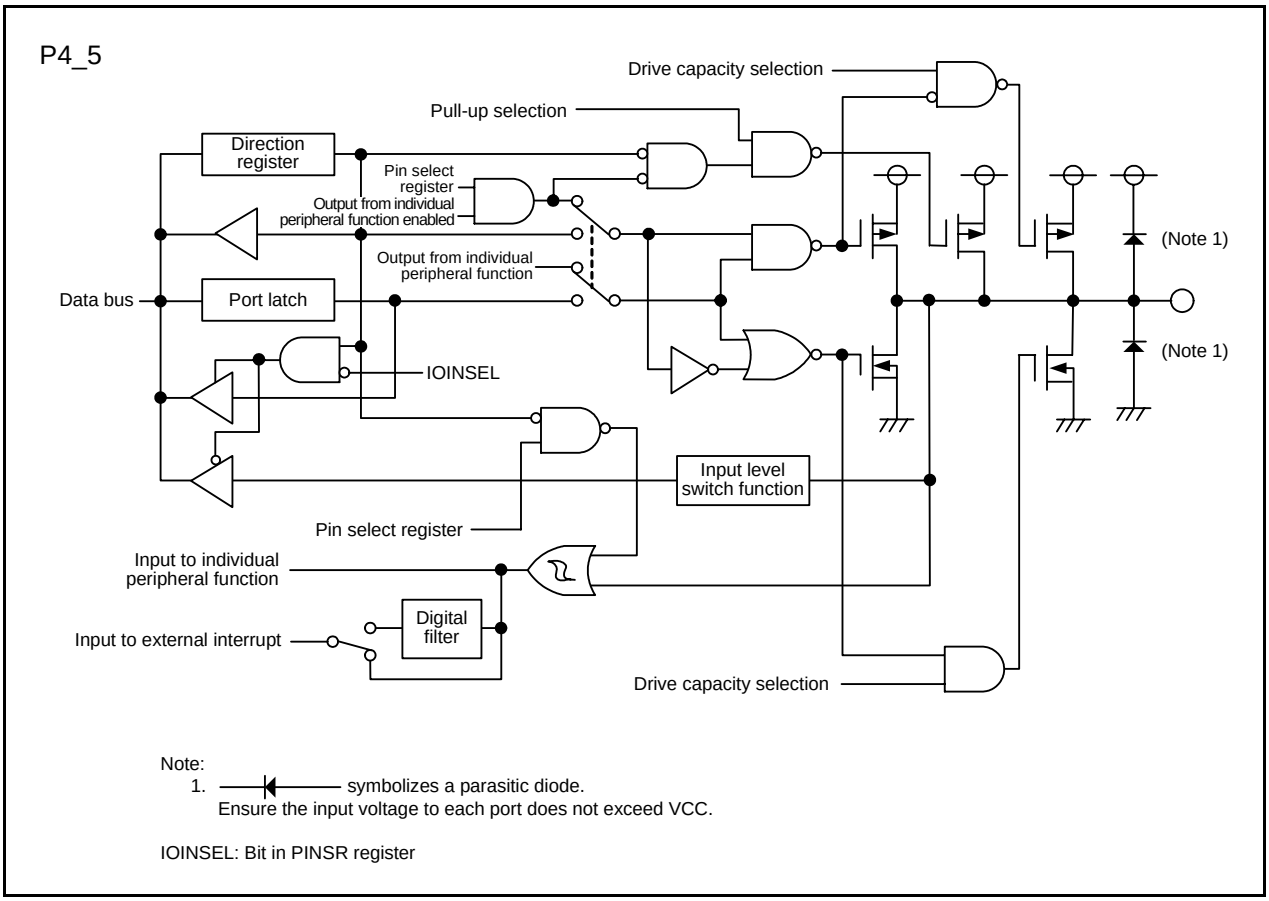
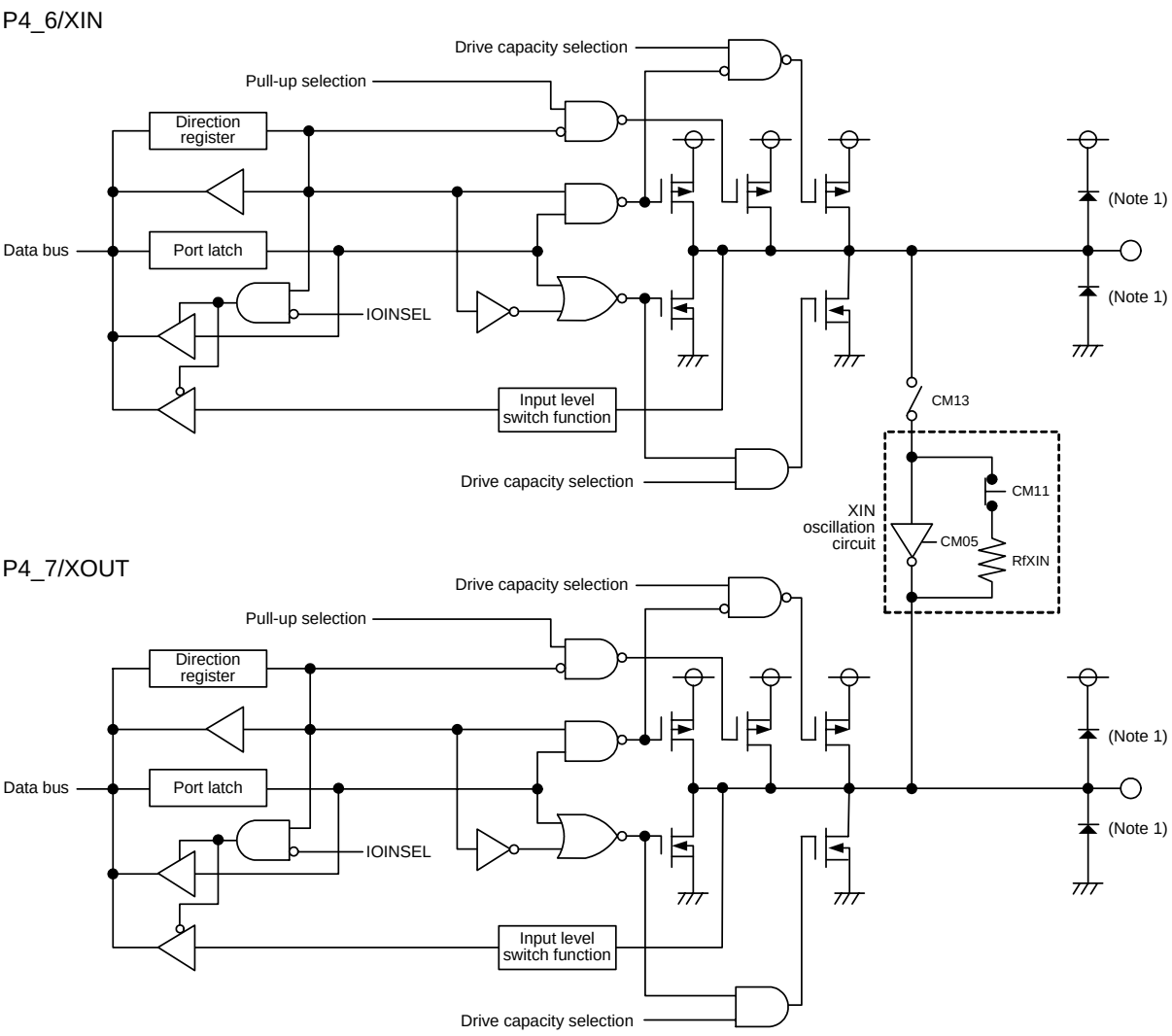


Figure 7.9 Configuration of I/O Ports (9)



Note:
1. ⊣◀— symbolizes a parasitic diode.
Ensure the input voltage to each port does not exceed VCC.

CM05: Bit in CM0 register
CM11, CM13: Bits in CM1 register
IOINSEL: Bit in PINSR register

Figure 7.10 Configuration of I/O Ports (10)

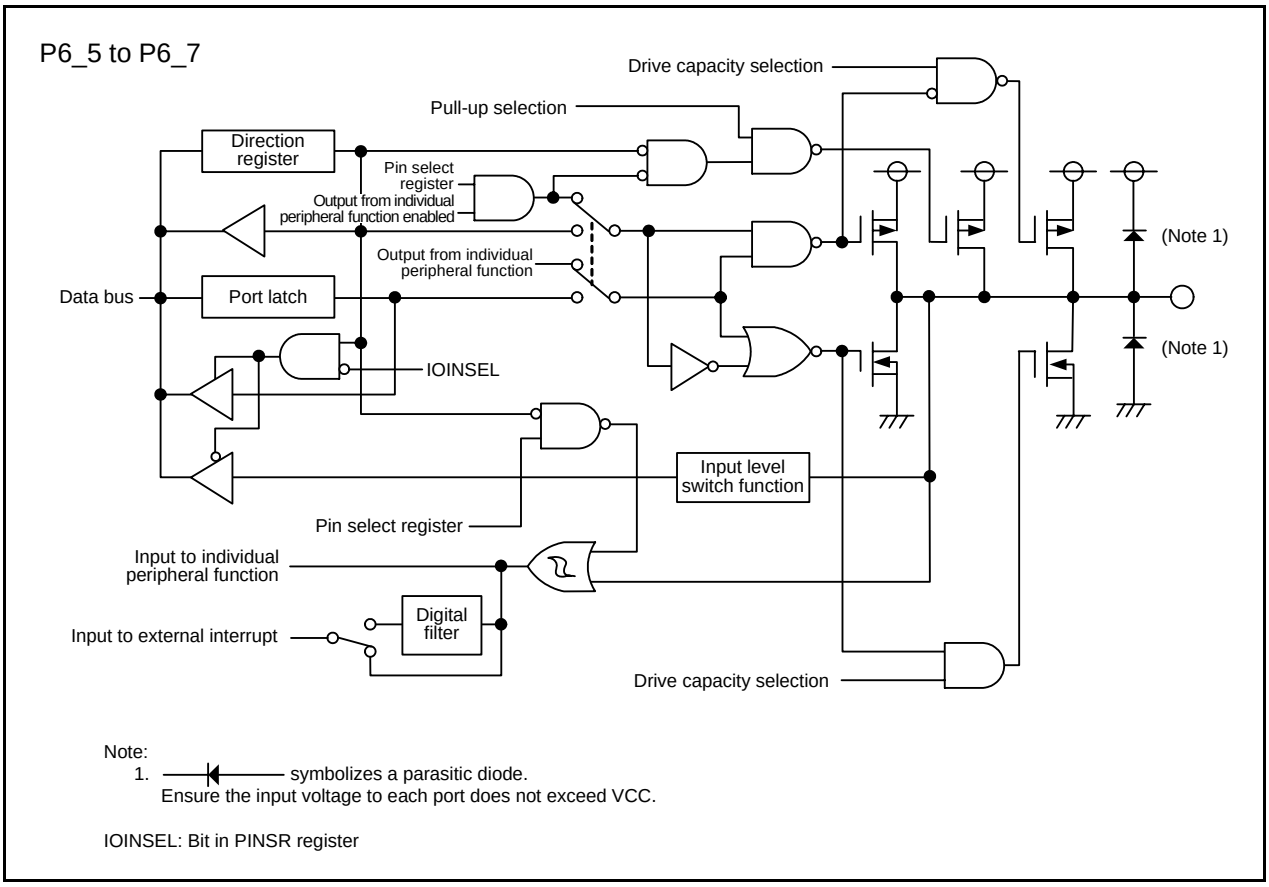


Figure 7.11 Configuration of I/O Ports (11)

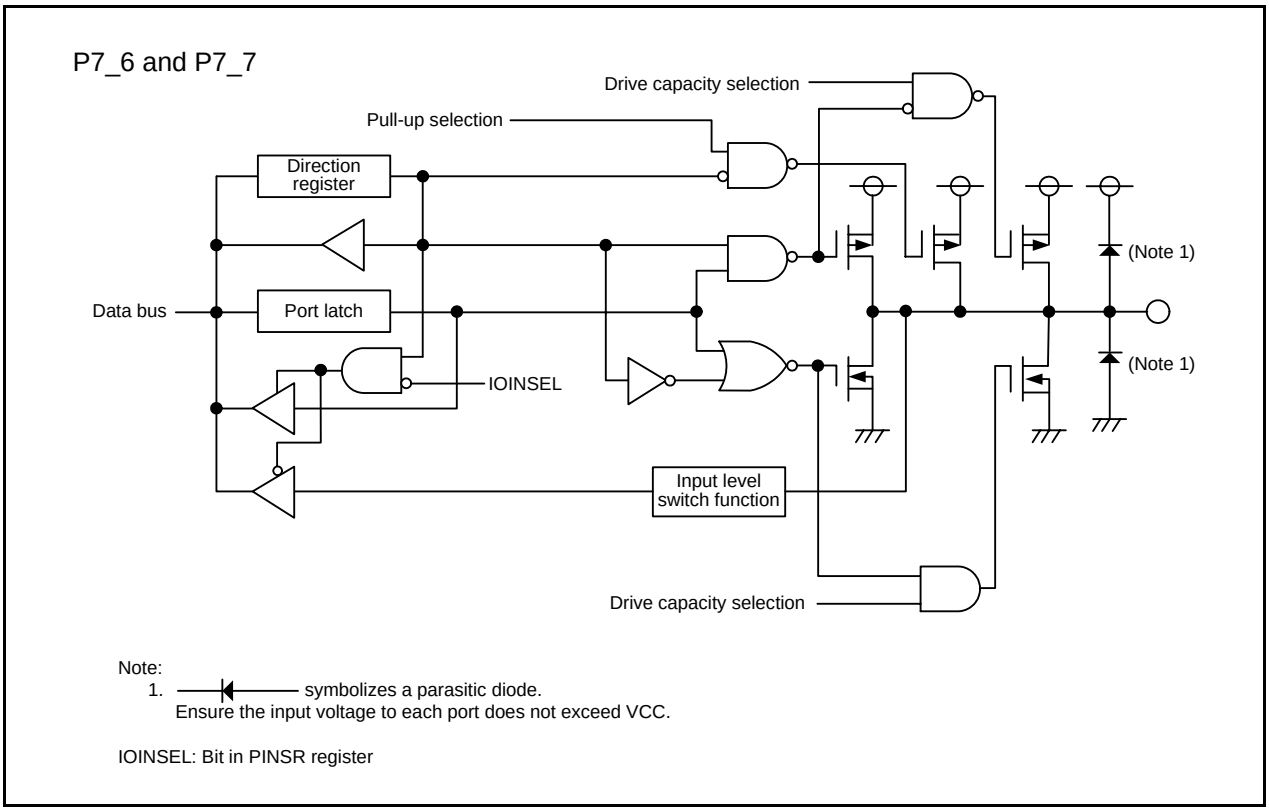
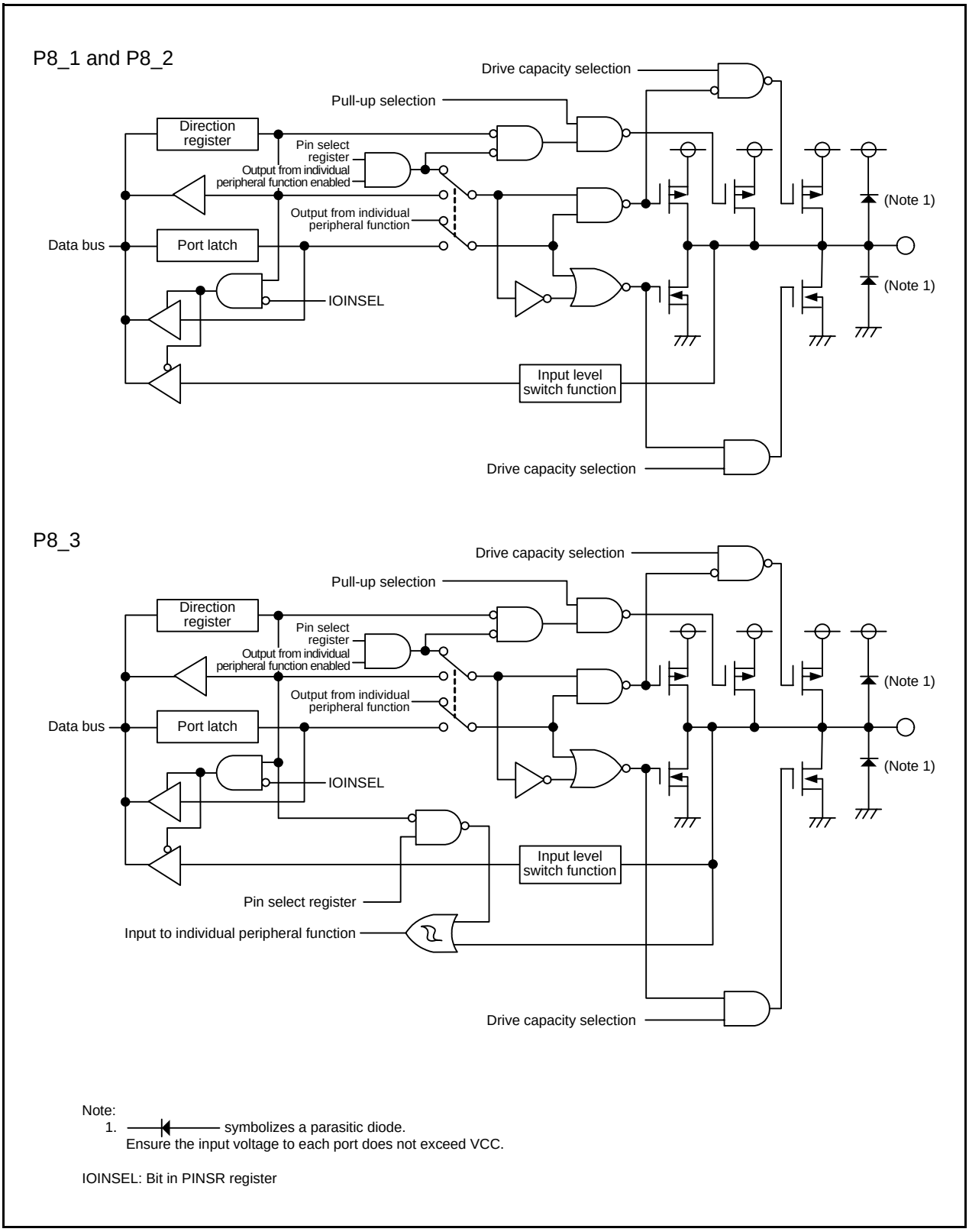


Figure 7.12 Configuration of I/O Ports (12)



Note:
1. ⊣◀ symbolizes a parasitic diode.
Ensure the input voltage to each port does not exceed VCC.

IOINSEL: Bit in PINSR register

Figure 7.13 Configuration of I/O Ports (13)

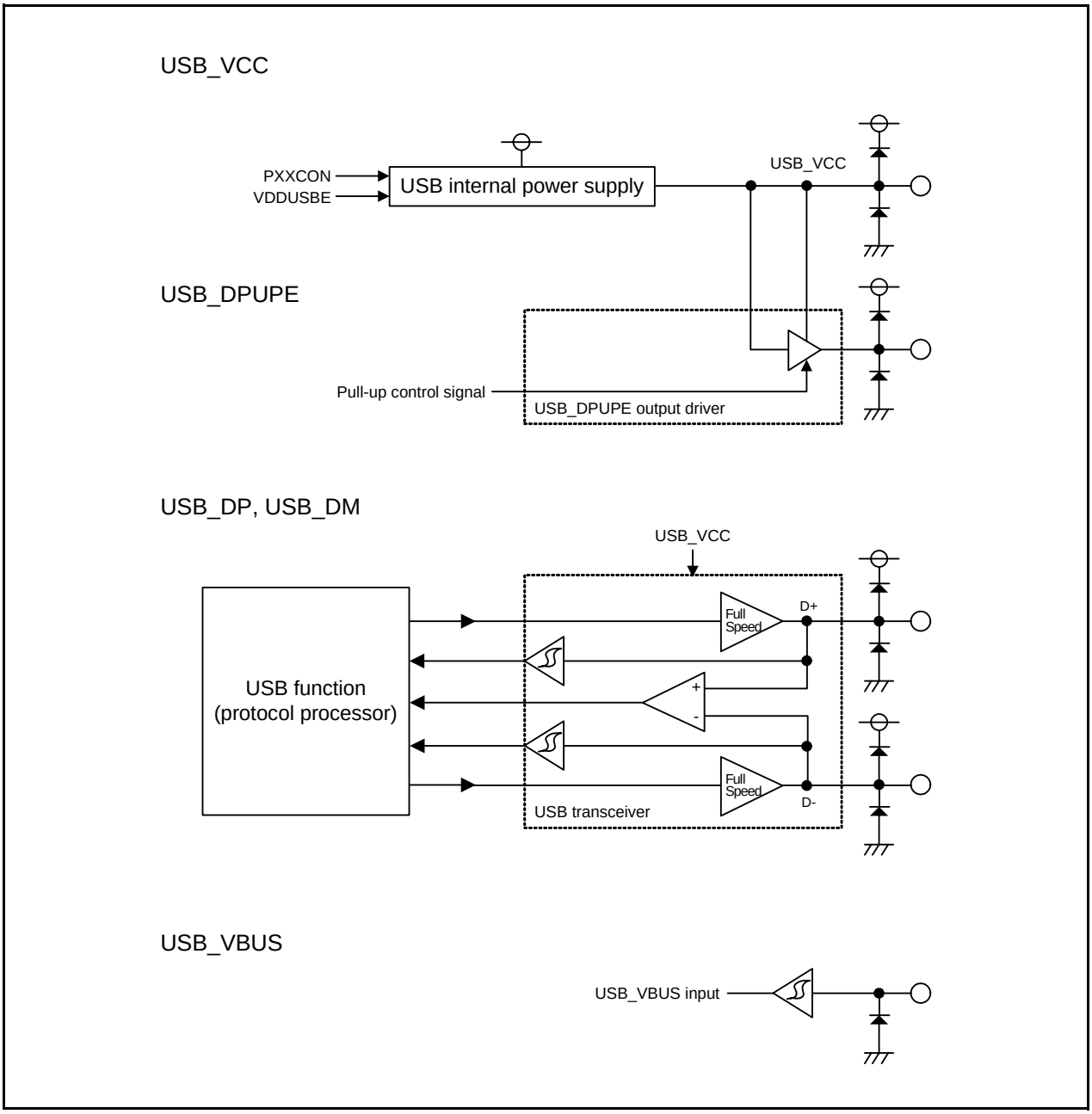


Figure 7.14 Configuration of I/O Ports (14)

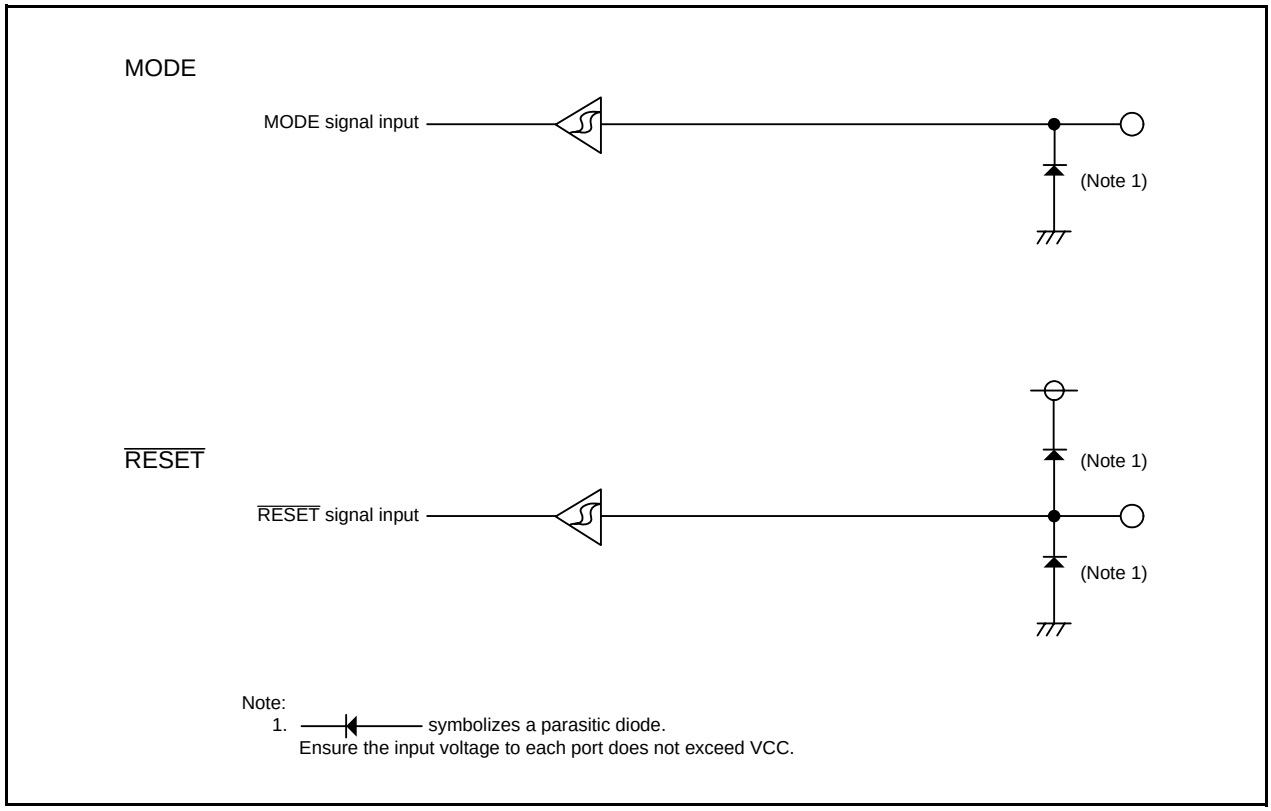


Figure 7.15 Configuration of I/O Pins

7.4 Registers

7.4.1 Port Pi Direction Register (PDi) (i = 0, 1, 3, 4, 6 to 8)

Address 00E2h (PD0 (1)), 00E3h (PD1), 00E7h (PD3), 00EAh (PD4 (2)), 00EEh (PD6), 00EFh (PD7), 00F2h (PD8)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PDi_7	PDi_6	PDi_5	PDi_4	PDi_3	PDi_2	PDi_1	PDi_0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PDi_0	Port Pi_0 direction bit	0: Input mode (functions as an input port) 1: Output mode (functions as an output port)	R/W
b1	PDi_1	Port Pi_1 direction bit		R/W
b2	PDi_2	Port Pi_2 direction bit		R/W
b3	PDi_3	Port Pi_3 direction bit		R/W
b4	PDi_4	Port Pi_4 direction bit		R/W
b5	PDi_5	Port Pi_5 direction bit		R/W
b6	PDi_6	Port Pi_6 direction bit		R/W
b7	PDi_7	Port Pi_7 direction bit		R/W

Notes:
1. Write to the PD0 register with the next instruction after that used to set the PRC2 bit in the PRCR register to 1 (write enabled).
2. Nothing is assigned to bits PD4_0 to PD4_2 in the PD4 register. If necessary, set these bits to 0. When read, the content is 0.

The PDi register selects whether I/O ports are used for input or output. Each bit in the PDi register corresponds to one port.

7.4.2 Port Pi Register (Pi) (i = 0, 1, 3, 4, 6 to 8)

Address 00E0h (P0), 00E1h (P1), 00E5h (P3), 00E8h (P4 (1)), 00ECh (P6), 00EDh (P7), 00F0h (P8)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	Pi_7	Pi_6	Pi_5	Pi_4	Pi_3	Pi_2	Pi_1	Pi_0
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Bit Name	Function	R/W
b0	Pi_0	Port Pi_0 bit	0: “L” level 1: “H” level	R/W
b1	Pi_1	Port Pi_1 bit		R/W
b2	Pi_2	Port Pi_2 bit		R/W
b3	Pi_3	Port Pi_3 bit		R/W
b4	Pi_4	Port Pi_4 bit		R/W
b5	Pi_5	Port Pi_5 bit		R/W
b6	Pi_6	Port Pi_6 bit		R/W
b7	Pi_7	Port Pi_7 bit		R/W

Note:

1. Nothing is assigned to bits P4_0 to P4_2 in the P4 register. If necessary, set these bits to 0. When read, the content is 0.

Data input and output to and from external devices are accomplished by reading and writing to the Pi register. The Pi register consists of a port latch to retain output data and a circuit to read the pin status. The value written in the port latch is output from the pin. Each bit in the Pi register corresponds to one port.

Pi_j Bit (i = 0, 1, 3, 4, 6 to 8, j = 0 to 7) (Port Pi_j Bit)

The pin level of any I/O port which is set to input mode can be read by reading the corresponding bit in this register. The pin level of any I/O port which is set to output mode can be controlled by writing to the corresponding bit in this register.

7.4.3 Timer RA Pin Select Register (TRASR)

Address 0180h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	TRAOSEL0	—	TRAIOSEL1	TRAIOSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRAIOSEL0	TRAIO pin select bit	b1 b0 0 0: TRAIO pin not used 0 1: P1_7 assigned 1 0: P1_5 assigned 1 1: Do not set.	R/W
b1	TRAIOSEL1			R/W
b2	—	Reserved bit	Set to 0.	R/W
b3	TRAOSEL0	TRAO pin select bit	0: P3_7 assigned 1: P3_0 assigned	R/W
b4	—	Reserved bit	Set to 0.	R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b6	—			
b7	—			

The TRASR register selects which pin is assigned to the timer RA I/O. To use the I/O pin for timer RA, set this register.
Set the TRASR register before setting the timer RA associated registers. Also, do not change the setting value in this register during timer RA operation.

7.4.4 Timer RC Pin Select Register (TRBRCSR)

Address 0181h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	TRCCLKSEL1	TRCCLKSEL0	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	—			
b4	TRCCLKSEL0	TRCCLK pin select bit	b5 b4 0 0: TRCCLK pin not used 0 1: P1_4 assigned 1 0: P3_3 assigned 1 1: Do not set.	R/W
b5	TRCCLKSEL1			R/W
b6	—	Reserved bit	Set to 0.	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

The TRBRCSR register selects which pin is assigned to the timer RC I/O. To use the I/O pin for timer RC, set this register.
Set bits TRCCLKSEL0 to TRCCLKSEL1 before setting the timer RC associated registers. Also, do not change the setting values. Do not change the setting values of bits TRCCLKSEL0 to TRCCLKSEL1 during timer RC operation.

7.4.5 Timer RC Pin Select Register 0 (TRCPSR0)

Address 0182h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	TRCIOBSEL1	TRCIOBSEL0	—	TRCIOASEL2	TRCIOASEL1	TRCIOASEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRCIOASEL0	TRCIOA/TRCTRG pin select bit	b2 b1 b0 0 0 0: TRCIOA/TRCTRG pin not used 0 0 1: P1_1 assigned 0 1 0: P0_0 assigned 0 1 1: P0_1 assigned 1 0 0: P0_2 assigned Other than above: Do not set.	R/W
b1	TRCIOASEL1			R/W
b2	TRCIOASEL2			R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	TRCIOBSEL0	TRCIOB pin select bit	b5 b4 0 0: TRCIOB pin not used 0 1: P1_2 assigned 1 0: P0_3 assigned 1 1: P0_4 assigned	R/W
b5	TRCIOBSEL1			R/W
b6	—	Reserved bit	Set to 0.	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

The TRCPSR0 register selects which pin is assigned to the timer RC I/O. To use the I/O pin for timer RC, set this register.
Set the TRCPSR0 register before setting the timer RC associated registers. Also, do not change the setting value in this register during timer RC operation.

7.4.6 Timer RC Pin Select Register 1 (TRCPSR1)

Address 0183h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	TRCIODSEL2	TRCIODSEL1	TRCIODSEL0	—	—	TRCIOCSEL1	TRCIOCSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRCIOCSEL0	TRCIOC pin select bit	b1 b0 0 0: TRCIOC pin not used 0 1: P1_3 assigned 1 0: P3_4 assigned 1 1: P0_7 assigned	R/W
b1	TRCIOCSEL1			R/W
b2	—	Reserved bit	Set to 0.	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	TRCIODSEL0	TRCIOD pin select bit	b6 b5 b4 0 0 0: TRCIOD pin not used 0 0 1: P1_0 assigned 0 1 0: P3_5 assigned 0 1 1: Do not set. 1 0 1: P6_7_assigned Other than above: Do not set.	R/W
b5	TRCIODSEL1			R/W
b6	TRCIODSEL2			R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

The TRCPSR1 register selects which pin is assigned to the timer RC I/O. To use the I/O pin for timer RC, set this register.
Set the TRCPSR1 register before setting the timer RC associated registers. Also, do not change the setting value in this register during timer RC operation.

7.4.7 UART0 Pin Select Register (U0SR)

Address 0188h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	CLK0SEL0	—	RXD0SEL0	—	TXD0SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TXD0SEL0	TXD0 pin select bit	0: TXD0 pin not used 1: P1_4 assigned	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	RXD0SEL0	RXD0 pin select bit	0: RXD0 pin not used 1: P1_5 assigned	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	CLK0SEL0	CLK0 pin select bit	0: CLK0 pin not used 1: P1_6 assigned	R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b6	—			
b7	—			

The U0SR register selects which pin is assigned to the UART0 I/O. To use the I/O pin for UART0, set this register.
Set the U0SR register before setting the UART0 associated registers. Also, do not change the setting value in this register during UART0 operation.

7.4.8 UART1 Pin Select Register (U1SR)

Address 0189h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	CLK1SEL1	CLK1SEL0	—	RXD1SEL0	—	TXD1SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TXD1SEL0	TXD1 pin select bit	0: TXD1 pin not used 1: P0_1 assigned	R/W
b1	—	Reserved bit	Set to 0.	R/W
b2	RXD1SEL0	RXD1 pin select bit	0: RXD1 pin not used 1: P0_2 assigned	R/W
b3	—	Reserved bit	Set to 0.	R/W
b4	CLK1SEL0	CLK1 pin select bit	b5 b4 0 0: CLK1 pin not used 0 1: P0_3 assigned 1 0: Do not set. 1 1: P6_5 assigned	R/W
b5	CLK1SEL1			
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	—			

The U1SR register selects which pin is assigned to the UART1 I/O. To use the I/O pin for UART1, set this register.
Set the U1SR register before setting the UART1 associated registers. Also, do not change the setting value in this register during UART1 operation.

7.4.9 UART3 Pin Select Register (U3SR)

Address 2F12h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	CLK3SEL0	—	RXD3SEL0	—	TXD3SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TXD3SEL0	TXD3 pin select bit	0: TXD3 pin not used 1: P8_2 assigned	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	RXD3SEL0	RXD3 pin select bit	0: RXD3 pin not used 1: P8_3 assigned	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	CLK3SEL0	CLK3 pin select bit	0: CLK3 pin not used 1: P8_1 assigned	R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b6	—			
b7	—			

The U3SR register selects which pin is assigned to the UART3 I/O. To use the I/O pin for UART3, set this register.
Set the U3SR register before setting the UART3 associated registers. Also, do not change the setting value in this register during UART3 operation.

7.4.10 UART2 Pin Select Register 0 (U2SR0)

Address 018Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	RXD2SEL1	RXD2SEL0	—	TXD2SEL2	TXD2SEL1	TXD2SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TXD2SEL0	TXD2 pin select bit	b2 b1 b0 0 0 0: TXD2 pin not used 1 0 1: P6_6 assigned Other than above: Do not set.	R/W
b1	TXD2SEL1			R/W
b2	TXD2SEL2			R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	RXD2SEL0	RXD2 pin select bit	b5 b4 0 0: RXD2 pin not used 1 1: P4_5 assigned Other than above: Do not set.	R/W
b5	RXD2SEL1			R/W
b6	—	Reserved bit	Set to 0.	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

The U2SR0 register selects which pin is assigned to the UART2 I/O. To use the I/O pin for UART2, set this register.
Set the U2SR0 register before setting the UART2 associated registers. Also, do not change the setting value in this register during UART2 operation.

7.4.11 UART2 Pin Select Register 1 (U2SR1)

Address 018Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	CTS2SEL0	—	—	CLK2SEL1	CLK2SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CLK2SEL0	CLK2 pin select bit	b1 b0 0 0: CLK2 pin not used 1 1: P6_5 assigned Other than above: Do not set.	R/W
b1	CLK2SEL1			R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	—			
b4	CTS2SEL0	$\overline{CTS2}$/$\overline{RTS2}$ pin select bit	0: $\overline{CTS2}$/$\overline{RTS2}$ pin not used 1: P3_3 assigned	R/W
b5	—	Reserved bit	Set to 0.	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	—			

The U2SR1 register selects which pin is assigned to the UART2 I/O. To use the I/O pin for UART2, set this register.
Set the U2SR1 register before setting the UART2 associated registers. Also, do not change the setting value in this register during UART2 operation.

7.4.12 SSU/IIC Pin Select Register (SSUIICSR)

Address 018Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	IICSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IICSEL	SSU/I^{2}C bus switch bit	0: SSU function selected 1: I^{2}C bus function selected	R/W
b1	—	Reserved bit	Set to 0.	R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	—			
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—			
b7	—			

7.4.13 INT Interrupt Input Pin Select Register (INTSR)

Address 018Eh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	INT1SEL0	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	INT1SEL0	$\overline{\text{INT1}}$ pin select bit	0: P1_7 assigned 1: P1_5 assigned	R/W
b2	—	Reserved bits	Set to 0.	R/W
b3	—			R/W
b4	—			R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b6	—	Reserved bit	Set to 0.	R/W
b7	—	Reserved bit	Set to 1.	R/W

The INTSR register selects which pin is assigned to the $\overline{\text{INT1}}$ input. To use $\overline{\text{INT1}}$, set this register.
Set the INTSR register before setting the $\overline{\text{INT1}}$ associated registers. Also, do not change the setting values in this register during $\overline{\text{INT1}}$ operation.

7.4.14 I/O Function Pin Select Register (PINSR)

Address 018Fh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	SDADLY1	SDADLY0	IICTCHALF	IICTCTWI	IOINSEL	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	IOINSEL	I/O port input function select bit	0: The I/O port input function depends on the PDi (i = 0, 1, 3, 4, 6 to 8) register. When the PDi_j (j = 0 to 7) bit in the PDi register is set to 0 (input mode), the pin input level is read. When the PDi_j bit in the PDi register is set to 1 (output mode), the port latch is read. 1: The I/O port input function reads the pin input level regardless of the PDi register	R/W
b4	IICTCTWI	I²C double transfer rate select bit	0: Transfer rate is the same as the value set with bits CKS0 to CKS3 in the ICCR1 register 1: Transfer rate is twice the value set with bits CKS0 to CKS3 in the ICCR1 register	R/W
b5	IICTCHALF	I²C half transfer rate select bit	0: Transfer rate is the same as the value set with bits CKS0 to CKS3 in the ICCR1 register 1: Transfer rate is half the value set with bits CKS0 to CKS3 in the ICCR1 register	R/W
b6	SDADLY0	SDA digital delay select bit	b7 b6 0 0: Digital delay of 3 × f1 cycles 0 1: Digital delay of 11 × f1 cycles 1 0: Digital delay of 19 × f1 cycles 1 1: Do not set.	R/W
b7	SDADLY1			R/W

IOINSEL Bit (I/O port input function select bit)

The IOINSEL bit is used to select the pin level of an I/O port when the PDi_j (j = 0 to 7) bit in the PDi (i = 0, 1, 3, 4, 6 to 8) register is set to 1 (output mode). When this bit is set to 1, the I/O port input function reads the pin input level regardless of the PDi register.

Table 7.4 lists I/O Port Values Read by Using IOINSEL Bit. The IOINSEL bit can be used to change the input function of all I/O ports.

Table 7.4 I/O Port Values Read by Using IOINSEL Bit

PDi_j bit in PDi register	0 (input mode)		1 (output mode)	
IOINSEL bit	0	1	0	1
I/O port values read	Pin input level		Port latch value	Pin input level

7.4.15 Pull-Up Control Register 0 (PUR0)

Address 01E0h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PU07	PU06	—	—	PU03	PU02	PU01	PU00
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PU00	P0_0 to P0_3 pull-up	0: Not pulled up	R/W
b1	PU01	P0_4, P0_7 pull-up	1: Pulled up (1)	R/W
b2	PU02	P1_0 to P1_3 pull-up		R/W
b3	PU03	P1_4 to P1_7 pull-up		R/W
b4	—	Reserved bits	Set to 0.	R/W
b5	—			R/W
b6	PU06	P3_0, P3_3 pull-up	0: Not pulled up	R/W
b7	PU07	P3_4, P3_5, P3_7 pull-up	1: Pulled up (1)	R/W

Note:
1. When this bit is set to 1 (pulled up), the pin whose port direction bit is set to 0 (input mode) is pulled up.

For pins used as input, the setting values in the PUR0 register are valid.

7.4.16 Pull-Up Control Register 1 (PUR1)

Address 01E1h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PU17	—	PU15	—	—	—	PU11	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bit	Set to 0.	R/W
b1	PU11	P4_5 to P4_7 pull-up	0: Not pulled up 1: Pulled up (1)	R/W
b2	—	Reserved bits	Set to 0.	R/W
b3	—			R/W
b4	—			R/W
b5	PU15	P6_5 to P6_7 pull-up	0: Not pulled up 1: Pulled up (1)	R/W
b6	—	Reserved bit	Set to 0.	R/W
b7	PU17	P7_6, P7_7 pull-up	0: Not pulled up 1: Pulled up (1)	R/W

Note:
1. When this bit is set to 1 (pulled up), the pin whose port direction bit is set to 0 (input mode) is pulled up.

For pins used as input, the setting values in the PUR1 register are valid.

7.4.17 Pull-Up Control Register 2 (PUR2)

Address 01E2h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	PU20
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PU20	P8_1 to P8_3 pull-up	0: Not pulled up 1: Pulled up (1)	R/W
b1	—	Reserved bits	Set to 0.	R/W
b2	—			R/W
b3	—			R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

Note:
1. When this bit is set to 1 (pulled up), the pin whose port direction bit is set to 0 (input mode) is pulled up.

   For pins used as input, the setting values in the PUR2 register are valid.

7.4.18 Port P1 Drive Capacity Control Register (P1DRR)

Address 01F0h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	P1DRR7	P1DRR6	P1DRR5	P1DRR4	P1DRR3	P1DRR2	P1DRR1	P1DRR0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	P1DRR0	P1_0 drive capacity	0: Low 1: High (1)	R/W
b1	P1DRR1	P1_1 drive capacity		R/W
b2	P1DRR2	P1_2 drive capacity		R/W
b3	P1DRR3	P1_3 drive capacity		R/W
b4	P1DRR4	P1_4 drive capacity		R/W
b5	P1DRR5	P1_5 drive capacity		R/W
b6	P1DRR6	P1_6 drive capacity		R/W
b7	P1DRR7	P1_7 drive capacity		R/W

Note:
1. Both “H” and “L” output are set to high drive capacity.

The P1DRR register selects whether the drive capacity of the P1 output transistor is set to low or high.
The P1DRRi bit (i = 0 to 7) is used to select whether the drive capacity of the output transistor is set to low or high for each pin.
For pins used as output, the setting values in the P1DRR register are valid.

7.4.19 Drive Capacity Control Register 0 (DRR0)

Address 01F2h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	DRR07	DRR06	—	—	—	—	DRR01	DRR00
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	DRR00	P0_0 to P0_3 drive capacity	0: Low	R/W
b1	DRR01	P0_4, P0_7 drive capacity	1: High (1)	R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	—			
b4	—			
b5	—			
b6	DRR06	P3_0, P3_3 drive capacity	0: Low	R/W
b7	DRR07	P3_4, P3_5 P3_7 drive capacity	1: High (1)	R/W

Note:
1. Both “H” and “L” output are set to high drive capacity.

For pins used as output, the setting values in the DRR0 register are valid.

DRR00 Bit (P0_0 to P0_3 drive capacity)

The DRR00 bit selects whether the drive capacity of the P0_0 to P0_3 output transistors is set to low or high. This bit is used to select whether the drive capacity of the output transistors is set to low or high for four pins.

DRR01 Bit (P0_4, P0_7 drive capacity)

The DRR01 bit selects whether the drive capacity of the P0_4, P0_7 output transistors is set to low or high. This bit is used to select whether the drive capacity of the output transistors is set to low or high for two pins.

DRR06 Bit (P3_0, P3_3 drive capacity)

The DRR06 bit selects whether the drive capacity of the P3_0, P3_3 output transistors is set to low or high. This bit is used to select whether the drive capacity of the output transistors is set to low or high for two pins.

DRR07 Bit (P3_4, P3_5, P3_7 drive capacity)

The DRR07 bit selects whether the drive capacity of the P3_4, P3_5, P3_7 output transistors is set to low or high. This bit is used to select whether the drive capacity of the output transistors is set to low or high for three pins.

7.4.20 Drive Capacity Control Register 1 (DRR1)

Address 01F3h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	DRR17	—	DRR15	—	—	—	DRR11	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bit	Set to 0.	R/W
b1	DRR11	P4_5 to P4_7 drive capacity	0: Low 1: High (1)	R/W
b2	—	Reserved bits	Set to 0.	R/W
b3	—			
b4	—			
b5	DRR15	P6_5 to P6_7 drive capacity	0: Low 1: High (1)	R/W
b6	—	Reserved bit	Set to 0.	R/W
b7	DRR17	P7_6, P7_7 drive capacity	0: Low 1: High (1)	R/W

Note:
1. Both “H” and “L” output are set to high drive capacity.

For pins used as output, the setting values in the DRR1 register are valid.

DRR11 Bit (P4_5 to P4_7 drive capacity)

The DRR11 bit selects whether the drive capacity of the P4_5 to P4_7 output transistors is set to low or high.This bit is used to select whether the drive capacity of the output transistors is set to low or high for three pins.

DRR15 Bit (P6_5 to P6_7 drive capacity)

The DRR15 bit selects whether the drive capacity of the P6_5 to P6_7 output transistors is set to low or high. This bit is used to select whether the drive capacity of the output transistors is set to low or high for three pins.

DRR17 Bit (P7_6, P7_7 drive capacity)

The DRR17 bit selects whether the drive capacity of the P7_6, P7_7 output transistors is set to low or high. This bit is used to select whether the drive capacity of the output transistors is set to low or high for two pins.

7.4.21 Drive Capacity Control Register 2 (DRR2)

Address 01F4h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	DRR20
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	DRR20	P8_1 to P8_3 drive capacity	0: Low 1: High (1)	R/W
b1	—	Reserved bits	Set to 0.	R/W
b2	—			R/W
b3	—			R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

Note:
1. Both “H” and “L” output are set to high drive capacity.

For pins used as output, the setting values in the DRR2 register are valid.

DRR20 Bit (P8_1 to P8_3 drive capacity)

The DRR20 bit selects whether the drive capacity of the P8_1 to P8_3 output transistors is set to low or high. This bit is used to select whether the drive capacity of the output transistors is set to low or high for three pins.

7.4.22 Input Threshold Control Register 0 (VLT0)

Address 01F5h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	VLT07	VLT06	—	—	VLT03	VLT02	VLT01	VLT00
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	VLT00	P0_0 to P0_4, P0_7 input level select bits	b1 b0 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b1	VLT01			R/W
b2	VLT02	P1 input level select bit	b3 b2 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b3	VLT03			R/W
b4	—	Reserved bits	Set to 0.	R/W
b5	—			R/W
b6	VLT06	P3_0, P3_3 to P3_5, P3_7 input level select bits	b7 b6 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b7	VLT07			R/W

The VLT0 register selects the voltage level of the input threshold values for ports P0_0 to P0_4, P0_7, P1, P3_0, P3_3 to P3_5, P3_7. Bits VLT00 to VLT03, VLT06, and VLT07 are used to select the input threshold value to be one of three voltage levels (0.35 VCC, 0.50 VCC, and 0.70 VCC) for each port.

7.4.23 Input Threshold Control Register 1 (VLT1)

Address 01F6h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	VLT17	VLT16	VLT15	VLT14	—	—	VLT11	VLT10
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	VLT10	P4_5 to P4_7 input level select bit	b1 b0 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b1	VLT11			R/W
b2	—	Reserved bits	Set to 0.	R/W
b3	—			R/W
b4	VLT14	P6_5 to P6_7 input level select bits	b5 b4 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b5	VLT15			R/W
b6	VLT16	P7_6, P7_7 input level select bits	b7 b6 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b7	VLT17			R/W

The VLT1 register selects the voltage level of the input threshold values for ports P4_5 to P4_7, P6_5 to P6_7, P7_6, and P7_7. Bits VLT10, VLT11, and VLT14 to VLT17 are used to select the input threshold values among three voltage levels (0.35 VCC, 0.50 VCC, and 0.70 VCC).

7.4.24 Input Threshold Control Register 2 (VLT2)

Address 01F7h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	VLT21	VLT20
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	VLT20	P8_1 to P8_3 input level select bits	b1 b0 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b1	VLT21			R/W
b2	—	Reserved bits	Set to 0.	R/W
b3	—			R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

The VLT2 register selects the voltage level of the input threshold values for ports P8_1 to P8_3. Bits VLT20 and VLT21 are used to select the input threshold values among three voltage levels (0.35 VCC, 0.50 VCC, and 0.70 VCC).

7.4.25 USB Pin Select Register 0 (USBSR0)

Address 2F10h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	USBVSENSEL	USBOVASEL	USBVBUSSEL	USBDMSEL	USBDPSEL	USBUPESEL	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	USBUPESEL	USB_DPUPE pin select bit	0: USB_DPUPE pin not used 1: USB_DPUPE pin used	R/W
b3	USBDPSEL	USB_DP pin select bit	0: USB_DP pin not used 1: USB_DP pin used	R/W
b4	USBDMSEL	USB_DM pin select bit	0: USB_DM pin not used 1: USB_DM pin used	R/W
b5	USBVBUSSEL	USB_VBUS pin select bit	0: USB_VBUS pin not used 1: USB_VBUS pin used	R/W
b6	USBOVASEL	USB_OVRCURA pin select bit (1)	0: USB_OVRCURA pin not used 1: P7_6 assigned	R/W
b7	USBVSENSEL	USB_VBUSEN pin select bit (1)	0: USB_VBUSEN pin not used 1: P7_7 assigned	R/W

Note:
1. This bit is reserved and must be set to 0 in the R8C/3MU Group.

The USBSR0 register is used to select the pins for the USB.

7.5 Port Settings

Tables 7.5 to 7.39 list the port settings.

Table 7.5 Port P0_0/AN7/TRCIOA/TRCTRG

Register	PD0	ADINSEL					TRCPSR0			Timer RC Setting	Function
Bit	PD0_0	CH			ADGSEL		TRCIOASEL			—	
		2	1	0	1	0	2	1	0		
Setting Value	0	X	X	X	X	X	Other than 010b			X	Input port (1)
	1	X	X	X	X	X	Other than 010b			X	Output port (2)
	0	1	1	1	0	0	Other than 010b			X	A/D converter input (AN7) (1, 3)
	0	X	X	X	X	X	0	1	0	Refer to **Table 7.36 TRCIOA Pin Setting**	TRCIOA input (1)
	X	X	X	X	X	X	0	1	0	Refer to **Table 7.36 TRCIOA Pin Setting**	TRCIOA output (2)

X: 0 or 1

Notes:
1. Pulled up by setting the PU00 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the DRR00 bit in the DRR0 register to 1.
3. Not available in the R8C/3MU Group.

Table 7.6 Port P0_1/AN6/TXD1/TRCIOA/TRCTRG

Register	PD0	ADINSEL					U1SR		U1MR			TRCPSR0			Timer RC Setting	Function
Bit	PD0_1	CH			ADGSEL		TXD1SEL		SMD			TRCIOASEL			—	
		2	1	0	1	0	1	0	2	1	0	2	1	0		
Setting Value	0	X	X	X	X	X	Other than 01b		X	X	X	Other than 011b			X	Input port (1)
	1	X	X	X	X	X	Other than 01b		X	X	X	Other than 011b			X	Output port (2)
	0	1	1	0	0	0	Other than 01b		X	X	X	Other than 011b			X	A/D converter input (AN6) (1, 4)
	X	X	X	X	X	X	0	1	0	0	1	X	X	X	X	TXD1 output (2, 3)
									1		0					
									0	1	0					
									1		1					
	0	X	X	X	X	X	Other than 01b		X	X	X	0	1	1	Refer to **Table 7.36 TRCIOA Pin Setting**	TRCIOA input (1)
	X	X	X	X	X	X	Other than 01b		X	X	X	0	1	1	Refer to **Table 7.36 TRCIOA Pin Setting**	TRCIOA output (2)

X: 0 or 1

Notes:
1. Pulled up by setting the PU00 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the DRR00 bit in the DRR0 register to 1.
3. N-channel open-drain output by setting the NCH bit in the U1C0 register to 1.
4. Not available in the R8C/3MU Group.

Table 7.7 Port 0_2/AN5/RXD1/TRCIOA/TRCTRG

Register	PD0	ADINSEL					U1SR		TRCPSR0			Timer RC Setting	Function
Bit	PD0_2	CH			ADGSEL		RXD1SEL		TRCIOASEL			—	
		2	1	0	1	0	1	0	2	1	0		
Setting Value	0	X	X	X	X	X	X	X	Other than 100b			X	Input port (1)
	1	X	X	X	X	X	X	X	Other than 100b			X	Output port (2)
	0	1	0	1	0	0	Other than 01b		Other than 100b			X	A/D converter input (AN5) (1, 3)
	0	X	X	X	X	X	0	1	Other than 100b			X	RXD1 input (1)
	0	X	X	X	X	X	X	X	1	0	0	Refer to **Table 7.36 TRCIOA Pin Setting**	TRCIOA input (1)
	X	X	X	X	X	X	X	X	1	0	0	Refer to **Table 7.36 TRCIOA Pin Setting**	TRCIOA output (2)

X: 0 or 1

Notes:
1. Pulled up by setting the PU00 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the DRR00 bit in the DRR0 register to 1.
3. Not available in the R8C/3MU Group.

Table 7.8 Port 0_3/AN4/CLK1/TRCIOB

Register	PD0	ADINSEL					U1SR		U1MR				TRCPSR0		Timer RC Setting	Function
Bit	PD0_3	CH			ADGSEL		CLK1SEL		SMD			CKDIR	TRCIOBSEL		—	
		2	1	0	1	0	1	0	2	1	0		1	0		
Setting Value	0	X	X	X	X	X	Other than 01b		X	X	X	X	Other than 10b		X	Input port (1)
	1	X	X	X	X	X	Other than 01b		X	X	X	X	Other than 10b		X	Output port (2)
	0	1	0	0	0	0	Other than 01b		X	X	X	X	Other than 10b		X	A/D converter input (AN4) (1, 3)
	0	X	X	X	X	X	0	1	X	X	X	1	X	X	X	CLK1 (external clock) input (1)
	X	X	X	X	X	X	0	1	0	0	1	0	X	X	X	CLK1 (internal clock) output (2)
	0	X	X	X	X	X	Other than 01b		X	X	X	X	1	0	Refer to **Table 7.37 TRCIOB Pin Setting**	TRCIOB input (1)
	X	X	X	X	X	X	Other than 01b		X	X	X	X	1	0	Refer to **Table 7.37 TRCIOB Pin Setting**	TRCIOB output (2)

X: 0 or 1

Notes:
1. Pulled up by setting the PU00 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the DRR00 bit in the DRR0 register to 1.
3. Not available in the R8C/3MU Group.

Table 7.9 Port 0_4/AN3/TRCIOB

Register	PD0	ADINSEL					TRCPSR0		Timer RC Setting	Function
Bit	PD0_4	CH			ADGSEL		TRCIOBSEL		—	
		2	1	0	1	0	1	0		
Setting Value	0	X	X	X	X	X	Other than 11b		X	Input port (1)
	1	X	X	X	X	X	Other than 11b		X	Output port (2)
	0	0	1	1	0	0	Other than 11b		X	A/D converter input (AN3) (1, 3)
	0	X	X	X	X	X	1	1	Refer to **Table 7.37 TRCIOB Pin Setting**	TRCIOB input (1)
	X	X	X	X	X	X	1	1	Refer to **Table 7.37 TRCIOB Pin Setting**	TRCIOB output (2)

X: 0 or 1

Notes:
1. Pulled up by setting the PU01 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the DRR01 bit in the DRR0 register to 1.
3. Not available in the R8C/3MU Group.

Table 7.10 Port 0_7/AN0/TRCIOC

Register	PD0	ADINSEL					TRCPSR1		Timer RC Setting	Function
Bit	PD0_7	CH			ADGSEL		TRCIOCSEL		—	
		2	1	0	1	0	1	0		
Setting Value	0	X	X	X	X	X	Other than 11b		X	Input port (1)
	1	X	X	X	X	X	Other than 11b		X	Output port (2)
	0	0	0	0	0	0	Other than 11b		X	A/D converter input (AN0) (1, 3)
	0	X	X	X	X	X	1	1	Refer to **Table 7.38 TRCIOC Pin Setting**	TRCIOC input (1)
	X	X	X	X	X	X	1	1	Refer to **Table 7.38 TRCIOC Pin Setting**	TRCIOC output (2)

X: 0 or 1

Notes:
1. Pulled up by setting the PU01 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the DRR01 bit in the DRR0 register to 1.
3. Not available in the R8C/3MU Group.

Table 7.11 Port 1_0/$\overline{\text{KI0}}$/AN8/TRCIOD

Register	PD1	KIEN	ADINSEL					TRCPSR1			Timer RC Setting	Function
Bit	PD1_0	KI0EN	CH			ADGSEL		TRCIODSEL			—	
			2	1	0	1	0	2	1	0		
Setting Value	0	X	X	X	X	X	X	Other than 001b			X	Input port (1)
	1	X	X	X	X	X	X	Other than 001b			X	Output port (2)
	0	1	X	X	X	X	X	Other than 001b			X	$\overline{\text{KI0}}$ input (1)
	0	0	0	0	0	0	1	Other than 001b			X	A/D converter input (AN8) (1, 3)
	0	X	X	X	X	X	X	0	0	1	Refer to **Table 7.39 TRCIOD Pin Setting**	TRCIOD input (1)
	X	X	X	X	X	X	X	0	0	1	Refer to **Table 7.39 TRCIOD Pin Setting**	TRCIOD output (2)

X: 0 or 1

Notes:
1. Pulled up by setting the PU02 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the P1DRR0 bit in the P1DRR register to 1.
3. Not available in the R8C/3MU Group.

Table 7.12 Port 1_1/$\overline{\text{KI1}}$/AN9/TRCIOA/TRCTRG

Register	PD1	KIEN	ADINSEL					TRCPSR0			Timer RC Setting	Function
Bit	PD1_1	KI1EN	CH			ADGSEL		TRCIOASEL			—	
			2	1	0	1	0	2	1	0		
Setting Value	0	X	X	X	X	X	X	Other than 001b			X	Input port (1)
	1	X	X	X	X	X	X	Other than 001b			X	Output port (2)
	0	1	X	X	X	X	X	Other than 001b			X	$\overline{\text{KI1}}$ input (1)
	0	0	0	0	1	0	1	Other than 001b			X	A/D converter input (AN9) (1, 3)
	0	X	X	X	X	X	X	0	0	1	Refer to **Table 7.36 TRCIOA Pin Setting**	TRCIOA input (1)
	X	X	X	X	X	X	X	0	0	1	Refer to **Table 7.36 TRCIOA Pin Setting**	TRCIOA output (2)

X: 0 or 1

Notes:
1. Pulled up by setting the PU02 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the P1DRR1 bit in the P1DRR register to 1.
3. Not available in the R8C/3MU Group.

Table 7.13 Port 1_2/$\overline{\text{KI2}}$/AN10/TRCIOB

Register	PD1	KIEN	ADINSEL					TRCPSR0		Timer RC Setting	Function
Bit	PD1_2	KI2EN	CH			ADGSEL		TRCIOBSEL		—	
			2	1	0	1	0	1	0		
Setting Value	0	X	X	X	X	X	X	Other than 01b		X	Input port (1)
	1	X	X	X	X	X	X	Other than 01b		X	Output port (2)
	0	1	X	X	X	X	X	Other than 01b		X	$\overline{\text{KI2}}$ input (1)
	0	0	0	1	0	0	1	Other than 01b		X	A/D converter input (AN10) (1, 3)
	0	X	X	X	X	X	X	0	1	Refer to **Table 7.37 TRCIOB Pin Setting**	TRCIOB input (1)
	X	X	X	X	X	X	X	0	1	Refer to **Table 7.37 TRCIOB Pin Setting**	TRCIOB output (2)

X: 0 or 1

Notes:
1. Pulled up by setting the PU02 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the P1DRR2 bit in the P1DRR register to 1.
3. Not available in the R8C/3MU Group.

Table 7.14 Port 1_3/$\overline{\text{KI3}}$/AN11/TRBO/TRCIOC

Register	PD1	KIEN	ADINSEL					TRBRCSR	TRCPSR1		Timer RB Setting	Timer RC Setting	Function
Bit	PD1_3	KI3EN	CH			ADGSEL		TRBOSEL0	TRCIOCSEL		—	—	
			2	1	0	1	0		1	0			
Setting Value	0	X	X	X	X	X	X	1	Other than 01b		X	X	Input port (1)
								X			Other than TRBO usage conditions		
	1	X	X	X	X	X	X	1	Other than 01b		X	X	Output port (2)
								X			Other than TRBO usage conditions		
	0	1	X	X	X	X	X	1	Other than 01b		X	X	$\overline{\text{KI3}}$ input (1)
								X			Other than TRBO usage conditions		
	0	0	0	1	1	0	1	1	Other than 01b		X	X	A/D converter input (AN11) (1, 3)
								X			Other than TRBO usage conditions		
	X	X	X	X	X	X	X	0	X	X	Refer to **Table 7.35 TRBO Pin Setting**	X	TRBO output (2)
	0	X	X	X	X	X	X	1	0	1	X	Refer to **Table 7.38 TRCIOC Pin Setting**	TRCIOC input (1)
								X			Other than TRBO usage conditions		
	X	X	X	X	X	X	X	1	0	1	X	Refer to **Table 7.38 TRCIOC Pin Setting**	TRCIOC output (2)
								X			Other than TRBO usage conditions		

X: 0 or 1

Notes:
1. Pulled up by setting the PU02 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the P1DRR3 bit in the P1DRR register to 1.
3. Not available in the R8C/3MU Group.

Table 7.15 Port 1_4/TXD0/TRCCLK

Register	PD1	U0SR	U0MR			TRBRCSR		TRCCR1			Function
Bit	PD1_4	TXD0SEL0	SMD			TRCCLKSEL		TCK			
			2	1	0	1	0	2	1	0	
Setting Value	0	0	X	X	X	X	X	X	X	X	Input port (1)
	1	0	X	X	X	X	X	X	X	X	Output port (2)
	X	1	0	0	1	X	X	X	X	X	TXD0 output (2, 3)
					0						
			1		1						
				1	0						
	0	0	X	X	X	0	1	1	0	1	TRCCLK input (1)

X: 0 or 1

Notes:
1. Pulled up by setting the PU03 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the P1DRR4 bit in the P1DRR register to 1.
3. N-channel open-drain output by setting the NCH bit in the U0C0 register to 1.

Table 7.16 Port 1_5/$\overline{\text{INT1}}$/RXD0/TRAIO

Register	PD1	U0SR	TRASR		TRAIOC	TRAMR			INTSR	INTEN	INTCMP	Function
Bit	PD1_5	RXD0SEL0	TRAIOSEL		TOPCR	TMOD			INT1SEL0	INT1EN	INT1CP0	
			1	0		2	1	0				
Setting Value	0	X	Other than 10b		X	X	X	X	X	X	X	Input port (1)
	1	X	Other than 10b		X	X	X	X	X	X	X	Output port (2)
	0	1	Other than 10b		X	X	X	X	X	X	X	RXD0 input (1)
	0	X	1	0	0	Other than 000b, 001b			X	X	X	TRAIO input (1)
	0	X	Other than 10b		X	X	X	X	1	1	0	$\overline{\text{INT1}}$ input (1)
	0	X	1	0	0	Other than 000b, 001b			1	1	0	TRAIO/$\overline{\text{INT1}}$ input (1)
	X	X	1	0	0	0	0	1	X	X	X	TRAIO pulse output (2)
	0	1	1	0	0	Master mode: 000b Slave mode: 011b			X	X	X	TRAIO/RXD0 input (Hardware LIN)
	0	1	1	0	0				1	1	0	TRAIO/RXD0/$\overline{\text{INT1}}$ input (Hardware LIN)

X: 0 or 1

Notes:
1. Pulled up by setting the PU03 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the P1DRR5 bit in the P1DRR register to 1.

Table 7.17 Port 1_6/CLK0/IVREF1

Register	PD1	U0SR	U0MR				INTCMP	Function
Bit	PD1_6	CLK0SEL 0	SMD			CKDIR	INT1CP0	
			2	1	0			
Setting Value	0	0	X	X	X	X	X	Input port (1)
	1	0	X	X	X	X	X	Output port (2)
	0	1	X	X	X	1	X	CLK0 (external clock) input (1)
	X	1	0	0	1	0	X	CLK0 (internal clock) output (2)
	0	0	X	X	X	X	1	Comparator B1 reference voltage input (IVREF1)

X: 0 or 1

Notes:
1. Pulled up by setting the PU03 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the P1DRR6 bit in the P1DRR register to 1.

Table 7.18 Port 1_7/$\overline{\text{INT1}}$/TRAIO/IVCMP1

Register	PD1	TRASR		TRAIOC	TRAMR			INTSR	INTEN	INTCMP	Function
Bit	PD1_7	TRAIOSEL		TOPCR	TMOD			INT1SEL0	INT1EN	INT1CP0	
		1	0		2	1	0				
Setting Value	0	Other than 01b		X	X	X	X	X	X	X	Input port (1)
	1	Other than 01b		X	X	X	X	X	X	X	Output port (2)
	0	0	1	0	Other than 000b, 001b			X	X	X	TRAIO input (1)
	0	Other than 01b		X	X	X	X	0	1	0	$\overline{\text{INT1}}$ input (1)
	0	0	1	0	Other than 000b, 001b			0	1	0	TRAIO/$\overline{\text{INT1}}$ input (1)
	X	0	1	0	0	0	1	X	X	X	TRAIO pulse output (2)
	0	Other than 01b		X	X	X	X	X	1	1	Comparator B1 input (IVCMP1)

X: 0 or 1

Notes:
1. Pulled up by setting the PU03 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the P1DRR7 bit in the P1DRR register to 1.

Table 7.19 Port 3_0/TRAO

Register	PD3	TRASR	TRAIOC	Function
Bit	PD3_0	TRAOSEL0	TOENA	
Setting Value	0	0	X	Input port (1)
	1	0	X	Output port (2)
	X	1	1	TRAO output (2)

X: 0 or 1

Notes:
1. Pulled up by setting the PU06 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the DRR06 bit in the DRR0 register to 1.

Table 7.20 Port 3_3/TRCCLK/$\overline{SCS}$/$\overline{CTS2}$/$\overline{RTS2}$/IVCMP3

Register	PD3	SSMR2		INTEN	TRBRCSR		TRCCR1			U2SR1	U2MR			U2CO		INTCMP	Function
Bit	PD3_3	CSS		INT3EN	TRCCLKSEL		TCK			CTS2SEL0	SMD			CRS	CRD	INT3CP0	
		1	0		1	0	2	1	0		2	1	0				
Setting Value	0	0	0	X	X	X	X	X	X	0	X	X	X	X	X	X	Input port (1)
	1	0	0	X	X	X	X	X	X	0	X	X	X	X	X	X	Output port (2)
	0	0	0	X	1	0	1	0	1	0	X	X	X	X	X	X	TRCCLK input (1)
	X	0	1	X	X	X	X	X	X	X	X			X	X	X	$\overline{SCS}$ input (1)
	X	1	0	X	X	X	X	X	X	X	X			X	X	X	$\overline{SCS}$ output (2, 3)
		1	1														
	0	0	0	X	X	X	X	X	X	1	Other than 000b			0	0	X	$\overline{CTS2}$ input (1)
	X	0	0	X	X	X	X	X	X	1	Other than 000b			1	0	X	$\overline{RTS2}$ output (2)
	0	0	0	1	Other than 10b		X	X	X	0	X	X	X	X	X	1	Comparator B3 input (IVCMP3)

X: 0 or 1

Notes:
1. Pulled up by setting the PU06 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the DRR06 bit in the DRR0 register to 1.
3. N-channel open-drain output by setting the CSOS bit in the SSMR2 register to 1 (N-channel open-drain output).

Table 7.21 Port 3_4/TRCIOC/SSI/IVREF3

Register	PD3	SSUIICSR	Synchronous Serial Communication Unit (refer to **Table 23.4 Association between Communication Modes and I/O Pins**)		TRCPSR1		INTCMP	Timer RC Setting	Function
Bit	PD3_4	IICSEL	SSI output control	SSI input control	TRCIOCSEL		INT3CP0	—	
					1	0			
Setting Value	0	X	0	0	Other than 10b		X	X	Input port (1)
	1	X	0	0	Other than 10b		X	X	Output port (2)
	0	X	0	0	1	0	X	Refer to **Table 7.38 TRCIOC Pin Setting**	TRCIOC input (1)
	X	X	0	0	1	0	X	Refer to **Table 7.38 TRCIOC Pin Setting**	TRCIOC output (2)
	X	0	0	1	X	X	X	X	SSI input (1)
	X	0	1	0	X	X	X	X	SSI output (2, 3)
	0	X	0	0	Other than 10b		1	X	Comparator B3 reference voltage input (IVREF3)

X: 0 or 1

Notes:
1. Pulled up by setting the PU07 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the DRR07 bit in the DRR0 register to 1.
3. N-channel open-drain output by setting the SOOS bit in the SSMR2 register to 1 (N-channel open-drain output) and setting the BIDE bit in the SSMR2 register to 0 (standard mode).
4. N-channel open-drain output by setting the NCH bit in the U2C0 register to 1.

Table 7.22 Port 3_5/TRCIOD/SCL/SSCK

Register	PD3	SSUIICSR	ICCR1	Synchronous Serial Communication Unit (refer to **Table 23.4 Association between Communication Modes and I/O Pins**)		TRCPSR1			U2SR1		Timer RC Setting	Function
Bit	PD3_5	IICSEL	ICE	SSCK output control	SSCK input control	TRCIODSEL			CLK2SEL		—	
						2	1	0	1	0		
Setting Value	0	0	X	0	0	Other than 010b			Other than 01b		X	Input port (1)
		1	0	X	X							
	1	0	X	0	0	Other than 010b			Other than 01b		X	Output port (2)
		1	0	X	X							
	X	1	1	X	X	X	X	X	X	X	X	SCL input/output (2)
	X	0	X	0	1	X	X	X	X	X	X	SSCK input (1)
	X	0	X	1	0	X	X	X	X	X	X	SSCK output (2, 3)
	0	0	X	0	0	0	1	0	Other than 01b		Refer to **Table 7.39 TRCIOD Pin Setting**	TRCIOD input (1)
		1	0	X	X							
	X	0	X	0	0	0	1	0	Other than 01b		Refer to **Table 7.39 TRCIOD Pin Setting**	TRCIOD output (2)
		1	0	X	X							

X: 0 or 1

Notes:

1. Pulled up by setting the PU07 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the DRR07 bit in the DRR0 register to 1.
3. N-channel open-drain output by setting the SCKOS bit in the SSMR2 register to 1 (N-channel open-drain output).

Table 7.23 Port 3_7/TRAO/SSO/SDA

Register	PD3	SSUIICSR	ICCR1	Synchronous Serial Communication Unit (refer to **Table 23.4 Association between Communication Modes and I/O Pins**)		TRASR	TRAIOC	Function
Bit	PD3_7	IICSEL	ICE	SSO output control	SSO input control	TRAOSEL0	TOENA	
Setting Value	0	1	0	X	X	Other than 01b		Input port (1)
		0	X	0	0			
	1	1	0	X	X	Other than 01b		Output port (2)
		0	X	0	0			
	X	1	1	X	X	X	X	SDA input/output (2)
	X	0	X	0	1	X	X	SSO input (1)
	X	0	X	1	0	X	X	SSO output (2, 3)
	X	1	0	X	X	0	1	TRAO output (2)
		0	X	0	0			

X: 0 or 1

Notes:

1. Pulled up by setting the PU07 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the DRR07 bit in the DRR0 register to 1.
3. N-channel open-drain output by setting the SOOS bit in the SSMR2 register to 1 (N-channel open-drain output).

Table 7.24 Port 4_5/$\overline{\text{INT0}}$/RXD2/$\overline{\text{ADTRG}}$

Register	PD4	INTEN	U2SR0		ADMOD (3)		Function
Bit	PD4_5	INT0EN	RXD2SEL		ADCAP		
			1	0	1	0	
Setting Value	0	X	Other than 11b		X	X	Input port (1)
	1	X	Other than 11b		X	X	Output port (2)
	0	1	Other than 11b		X	X	$\overline{\text{INT0}}$ input (1)
	0	X	1	1	X	X	RXD2 input (1)
	0	1	Other than 11b		1	X	$\overline{\text{ADTRG}}$ input (1, 3)

X: 0 or 1

Notes:
1. Pulled up by setting the PU11 bit in the PUR1 register to 1.
2. Output drive capacity high by setting the DRR11 bit in the DRR1 register to 1.
3. Not available in the R8C/3MU Group.

Table 7.25 Port 4_6/XIN

Register	PD4	PINSR	CM0			CM1				Circuit specifications		Function
Bit	PD4_6	XCSEL	CM03	CM04	CM05	CM10	CM11	CM12	CM13	Oscillation buffer	Feedback resistor	
Setting Value	0	0	X	0	X	0	X	X	0	OFF	OFF	Input port (1)
		1		X								
	1	0	X	0	X	0	X	X	0	OFF	OFF	Output port (2)
		1		X								
	X	X	X	X	0	0	0	X	1	ON	ON	XIN-XOUT oscillation (on-chip feedback resistor enabled)
							1			ON	OFF	XIN-XOUT oscillation (on-chip feedback resistor disabled)
					1		0			OFF	ON	XIN-XOUT oscillation stop (on-chip feedback resistor enabled)
							1			OFF	OFF	XIN-XOUT oscillation stop (on-chip feedback resistor disabled)
					X	1	X		X	OFF	OFF	oscillation stop (STOP mode)

X: 0 or 1

Notes:
1. Pulled up by setting the PU11 bit in the PUR1 register to 1.
2. Output drive capacity high by setting the DRR11 bit in the DRR1 register to 1.

Table 7.26 Port 4_7/XOUT

Register	PD4	PINSR	CM0			CM1				Circuit specifications		Function
Bit	PD4_7	XCSEL	CM03	CM04	CM05	CM10	CM11	CM12	CM13	Oscillation buffer	Feedback resistor	
Setting Value	0	0	X	0	X	0	X	X	0	OFF	OFF	Input port (1)
		1		X								
	1	0	X	0	X	0	X	X	0	OFF	OFF	Output port (2)
		1		X								
	X	X	X	X	0	0	0	X	1	ON	ON	XIN-XOUT oscillation (on-chip feedback resistor enabled)
							1			ON	OFF	XIN-XOUT oscillation (on-chip feedback resistor disabled)
					1		0			OFF	ON	XIN-XOUT oscillation stop (on-chip feedback resistor enabled)
							1			OFF	OFF	XIN-XOUT oscillation stop (on-chip feedback resistor disabled)
					X	1	X		X	OFF	OFF	oscillation stop (STOP mode)

X: 0 or 1

Notes:
1. Pulled up by setting the PU11 bit in the PUR1 register to 1.
2. Output drive capacity high by setting the DRR11 bit in the DRR1 register to 1.

Table 7.27 Port 6_5/$\overline{\text{INT4}}$/CLK1/CLK2

Register	PD6	INTEN1	U2SR1		U2MR				U1SR		U1MR				Function
Bit	PD6_5	INT4EN	CLK2SEL		SMD			CKDIR	CLK1SEL		SMD			CKDIR	
			1	0	2	1	0		1	0	2	1	0		
Setting Value	0	X	Other than 11b		X	X	X	X	Other than 11b		X	X	X	X	Input port (1)
	1	X	Other than 11b		X	X	X	X	Other than 11b		X	X	X	X	Output port (2)
	0	1	Other than 11b		X	X	X	X	Other than 11b		X	X	X	X	$\overline{\text{INT4}}$ input (1)
	0	X	1	1	X	X	X	1	Other than 11b		X	X	X	X	CLK2 (external clock) input (1)
	X	X	1	1	0	0	1	0	Other than 11b		X	X	X	X	CLK2 (internal clock) output (2, 3)
	0	X	X	X	X	X	X	X	1	1	X	X	X	1	CLK1 (external clock) input (1)
	X	X	X	X	X	X	X	X	1	1	0	0	1	0	CLK1 (internal clock) output (2)

X: 0 or 1

Notes:
1. Pulled up by setting the PU15 bit in the PUR1 register to 1.
2. Output drive capacity high by setting the DRR15 bit in the DRR1 register to 1.
3. N-channel open-drain output by setting the NODC bit in the U2SMR3 register to 1.

Table 7.28 Port 6_6/$\overline{\text{INT2}}$/TXD2

Register	PD6	INTSR	INTEN	U2SR0			U2MR			Function
Bit	PD6_6	INT2SEL0	INT2EN	TXD2SEL			SMD			
				2	1	0	2	1	0	
Setting Value	0	X	X	Other than 101b			X	X	X	Input port (1)
	1	X	X	Other than 101b			X	X	X	Output port (2)
	0	0	1	Other than 101b			X	X	X	$\overline{\text{INT2}}$ input (1)
	X	X	X	1	0	1	0	0	1	TXD2 output (2, 3)
									0	
							1	0	1	
									0	
								1	1	
									0	

X: 0 or 1

Notes:
1. Pulled up by setting the PU15 bit in the PUR1 register to 1.
2. Output drive capacity high by setting the DRR15 bit in the DRR1 register to 1.
3. N-channel open-drain output by setting the NCH bit in the U2C0 register to 1.

Table 7.29 Port 6_7/$\overline{\text{INT3}}$/TRCIOD

Register	PD6	INTEN	INTCMP	TRCPSR1			Timer RC Setting	Function
Bit	PD6_7	INT3EN	INT3CP0	TRCIODSEL			—	
				2	1	0		
Setting Value	0	X	X	Other than 101b			X	Input port (1)
	1	X	X	Other than 101b			X	Output port (2)
	0	1	0	Other than 101b			X	$\overline{\text{INT3}}$ input (1)
	0	X	X	1	0	1	Refer to **Table 7.39 TRCIOD Pin Setting**	TRCIOD input (1)
	X	X	X	1	0	1	Refer to **Table 7.39 TRCIOD Pin Setting**	TRCIOD output (2)

X: 0 or 1

Notes:
1. Pulled up by setting the PU15 bit in the PUR1 register to 1.
2. Output drive capacity high by setting the DRR15 bit in the DRR1 register to 1.

Table 7.30 Port 7_6

Register	PD7	Function
Bit	PD7_6	
Setting Value	0	Input port (1)
	1	Output port (2)

X: 0 or 1

Notes:
1. Pulled up by setting the PU17 bit in the PUR1 register to 1.
2. Output drive capacity high by setting the DRR17 bit in the DRR1 register to 1.

Table 7.31 Port 7_7

Register	PD7	Function
Bit	PD7_7	
Setting Value	0	Input port (1)
	1	Output port (2)

X: 0 or 1

Notes:
1. Pulled up by setting the PU17 bit in the PUR1 register to 1.
2. Output drive capacity high by setting the DRR17 bit in the DRR1 register to 1.

Table 7.32 Port 8_1/CLK3

Register	PD8	U3SR	U3MR				Function
Bit	PD8_1	CLK3SEL0	SMD2	SMD1	SMD0	CKDIR	
Setting Value	0	0	X	X	X	X	Input port (1)
	1	0	X	X	X	X	Output port (2)
	0	1	X	X	X	1	CLK3 (external clock) input (1)
	X	1	0	0	1	0	CLK3 (internal clock) output (2)

X: 0 or 1

Notes:
1. Pulled up by setting the PU20 bit in the PUR2 register to 1.
2. Output drive capacity high by setting the DRR20 bit in the DRR2 register to 1.

Table 7.33 Port 8_2/TXD3

Register	PD8	U3SR	U3MR			Function
Bit	PD8_2	TXD3SEL0	SMD2	SMD1	SMD0	
Setting Value	0	0	X	X	X	Input port (1)
	1	0	X	X	X	Output port (2)
	X	1	0	0	1	TXD3 output (2, 3)
			1	0	0	
			1	0	1	
			1	1	0	

X: 0 or 1

Notes:
1. Pulled up by setting the PU20 bit in the PUR2 register to 1.
2. Output drive capacity high by setting the DRR20 bit in the DRR2 register to 1.
3. N-channel open-drain output by setting the NCH bit in the U3C0 register to 1.

Table 7.34 Port 8_3/RXD3

Register	PD8	U3SR	Function
Bit	PD8_3	RXD3SEL0	
Setting Value	0	X	Input port (1)
	1	X	Output port (2)
	0	1	RXD3 output (1)

X: 0 or 1

Notes:
1. Pulled up by setting the PU20 bit in the PUR2 register to 1.
2. Output drive capacity high by setting the DRR20 bit in the DRR2 register to 1.

Table 7.35 TRBO Pin Setting

Register	TRBIOC	TRBMR		Function
Bit	TOCNT	TMOD1	TMOD0	
Setting Value	0	0	1	Programmable waveform generation mode (pulse output)
	1	0	1	Programmable waveform generation mode (programmable output)
	0	1	0	Programmable one-shot generation mode
	0	1	1	Programmable wait one-shot generation mode

Table 7.36 TRCIOA Pin Setting

Register	TRCOER	TRCMR	TRCIOR0			TRCCR2		Function
Bit	EA	PWM2	IOA2	IOA1	IOA0	TCEG1	TCEG0	
Setting Value	0	1	0	0	1	X	X	Timer waveform output (output compare function)
				1	X			
	0	1	1	X	X	X	X	Timer mode (input capture function)
	1							
	1	0	X	X	X	0	1	PWM2 mode TRCTRG input
						1	X	

X: 0 or 1

Table 7.37 TRCIOB Pin Setting

Register	TRCOER	TRCMR		TRCIOR0			Function
Bit	EB	PWM2	PWMB	IOB2	IOB1	IOB0	
Setting Value	0	0	X	X	X	X	PWM2 mode waveform output
	0	1	1	X	X	X	PWM mode waveform output
	0	1	0	0	0	1	Timer waveform output (output compare function)
					1	X	
	0	1	0	1	X	X	Timer mode (input capture function)
	1						

X: 0 or 1

Table 7.38 TRCIOC Pin Setting

Register	TRCOER	TRCMR		TRCIOR1			Function
Bit	EC	PWM2	PWMC	IOC2	IOC1	IOC0	
Setting Value	0	1	1	X	X	X	PWM mode waveform output
	0	1	0	0	0	1	Timer waveform output (output compare function)
					1	X	
	0	1	0	1	X	X	Timer mode (input capture function)
	1						

X: 0 or 1

Table 7.39 TRCIOD Pin Setting

Register	TRCOER	TRCMR		TRCIOR1			Function
Bit	ED	PWM2	PWMD	IOD2	IOD1	IOD0	
Setting Value	0	1	1	X	X	X	PWM mode waveform output
	0	1	0	0	0	1	Timer waveform output (output compare function)
					1	X	
	0	1	0	1	X	X	Timer mode (input capture function)
	1						

X: 0 or 1

7.6 Unassigned Pin Handling

Table 7.40 lists Unassigned Pin Handling.

Table 7.40 Unassigned Pin Handling

Pin Name	Connection
P0_0 to P0_4, P0_7, P1, P3_0, P3_3 to P3_5, P3_7, P4_5 to P4_7, P6_5 to P6_7, P7_6, P7_7, P8_1 to P8_3	• After setting to input mode, connect each pin to VSS via a resistor (pull-down) or connect each pin to VCC via a resistor (pull-up). (2) • After setting to output mode, leave these pins open. (1, 2)
USB_VCC	Set the PXXCON bit in the USBMC register to 0 and perform the following handling. • Leave the pin open.
VREF (4), NC (5)	Connect to VCC.
$\overline{\text{RESET}}$ (3)	Connect to VCC via a pull-up resistor (2)

Notes:
1. If these ports are set to output mode and left open, they remain in input mode until they are switched to output mode by a program. The voltage level of these pins may be undefined and the power current may increase while the ports remain in input mode.
   The content of the direction registers may change due to noise or program runaway caused by noise. In order to enhance program reliability, the program should periodically repeat the setting of the direction registers.
2. Connect these unassigned pins to the MCU using the shortest wire length (2 cm or less) possible.
3. When the power-on reset function is in use.
4. Available only in the R8C/3MK Group.
5. Available only in the R8C/3MU Group.

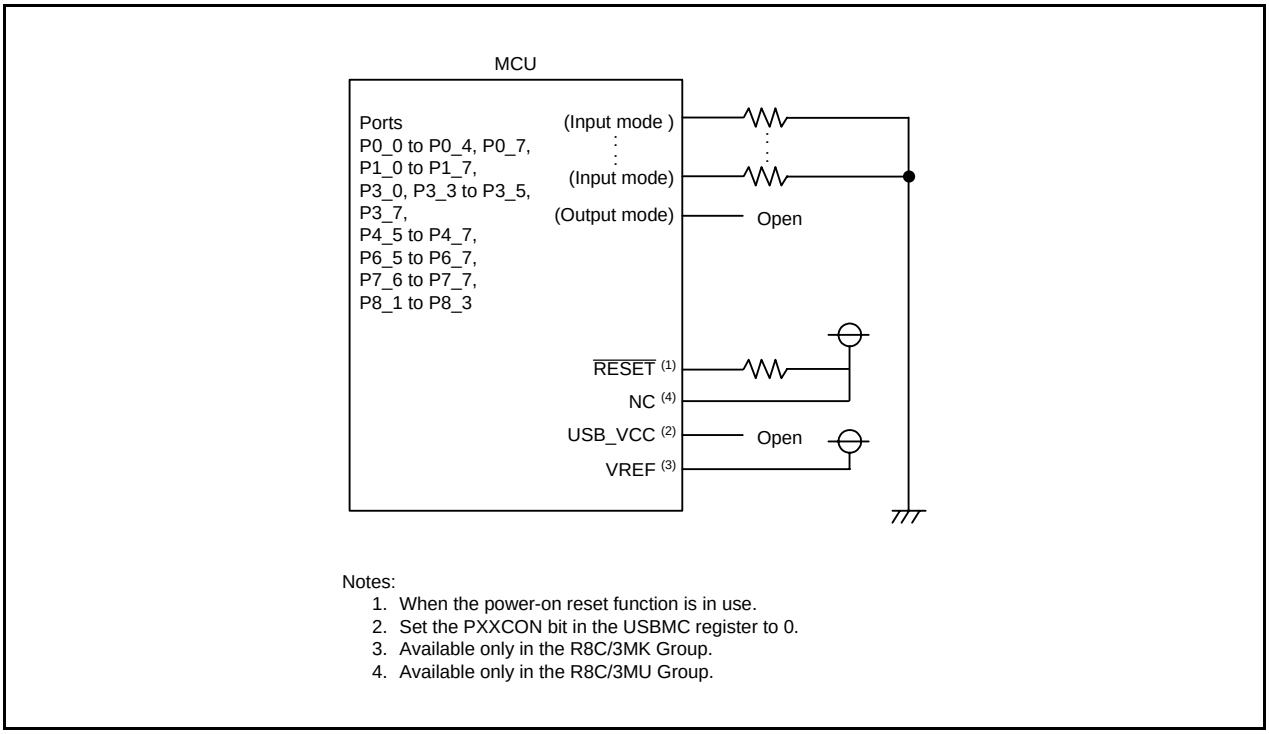


Figure 7.16 Unassigned Pin Handling

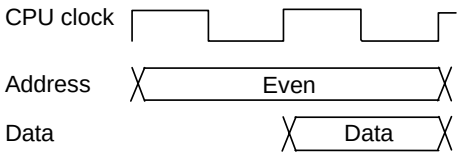
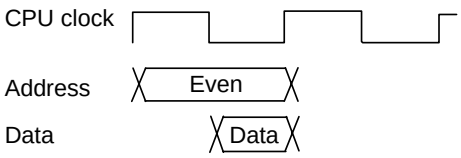
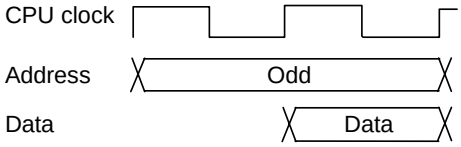
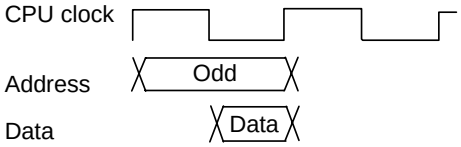
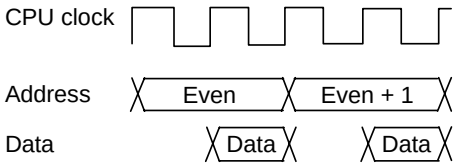
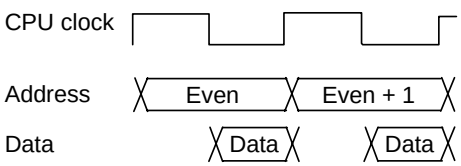
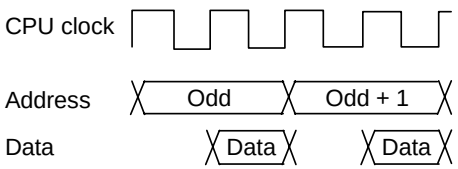
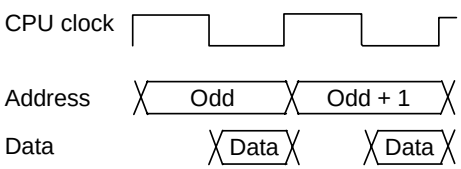
8. Bus

The bus cycles differ when accessing ROM, RAM, DTC vector area, DTC control data and when accessing SFR. Table 8.1 lists Bus Cycles by Access Area of R8C/3MU Group, R8C/3MK Group.
ROM, RAM, DTC vector area, DTC control data and SFR are connected to the CPU by an 8-bit bus. When accessing in word (16-bit) units, these areas are accessed twice in 8-bit units.
Table 8.2 shows Access Units and Bus Operations.

Table 8.1 Bus Cycles by Access Area of R8C/3MU Group, R8C/3MK Group

Access Area	Bus Cycle
SFR, Data flash	2 cycles of CPU clock
Program ROM, RAM	1 cycle of CPU clock

Table 8.2 Access Units and Bus Operations

Area	SFR, Data flash	ROM (program ROM), RAM, DTC vector area, DTC control data
Even address Byte access		
Odd address Byte access		
Even address Word access		
Odd address Word access		

However, only the following SFRs are connected with the 16-bit bus:

Interrupts: Each interrupt control register
Timer RC: Registers TRC, TRCGRA, TRCGRB, TRCGRC, and TRCGRD
SSU: Registers SSTDR, SSTDRH, SSRDR, and SSRDRH
UART2: Registers U2MR, U2BRG, U2TB, U2C0, U2C1, and U2RB
A/D converter (1): Registers AD0, AD1, AD2, AD3, AD4, AD5, AD6, AD7, ADMOD, ADINSEL, ADCON0, and ADCON1
Address match interrupt: Registers RMAD0, AIER0, RMAD1, and AIER1

Note:
1. Not available in the R8C/3MU Group.

Therefore, they are accessed once in 16-bit units. The bus operation is the same as “Area: SFR, Data flash, Even address Byte Access” in **Table 8.2 Access Units and Bus Operations**, and 16-bit data is accessed at a time.

9. Clock Generation Circuit

The following five circuits are incorporated in the clock generation circuit:
- XIN clock oscillation circuit
- PLL Frequency Synthesizer
- Low-speed on-chip oscillator
- High-speed on-chip oscillator
- Low-speed on-chip oscillator for watchdog timer

9.1 Overview

Table 9.1 lists the Specification Overview of Clock Generation Circuit. Figure 9.1 shows a Clock Generation Circuit, Figure 9.2 shows a Peripheral Function Clock, and Figure 9.3 shows a Procedure for Reducing Internal Power Consumption Using VCA20 bit.

Table 9.1 Specification Overview of Clock Generation Circuit

Item	XIN Clock Oscillation Circuit	PLL Frequency Synthesizer	On-Chip Oscillator		Low-Speed On-Chip Oscillator for Watchdog Timer
			High-Speed On-Chip Oscillator	Low-Speed On-Chip Oscillator	
Applications	• CPU clock source • Peripheral function clock source	• CPU clock source • Peripheral function clock source	• CPU clock source • Peripheral function clock source • CPU and peripheral function clock source when XIN clock stops oscillating	• CPU clock source • Peripheral function clock source • CPU and peripheral function clock source when XIN clock stops oscillating	• Watchdog timer clock source
Clock frequency	0 to 20 MHz	8/12/16 MHz (7)	Approx. 40 MHz (3)	Approx. 125 kHz	Approx. 125 kHz
Connectable oscillator	• Ceramic resonator • Crystal oscillator	— (6)	—	—	—
Oscillator connect pins	XIN, XOUT (1)	— (6)	— (1)	— (1)	—
Oscillation stop, restart function	Usable	Usable	Usable	Usable	Usable
Oscillator status after reset	Stop	Stop	Stop	Oscillate	Stop (4) Oscillate (5)
Others	Externally generated clock can be input (2)	— (6)	—	—	—

Notes:
1. When the on-chip oscillator clock is used as the CPU clock without using the XIN clock oscillation circuit, these pins can be used as P4_6 and P4_7.
   The P4_6 pin is multiplexed with the XIN pin and the P4_7 pin is multiplexed with the XOUT pin. When using the XIN clock, these pins cannot be used as I/O ports.
2. To input an external clock, set the CM05 bit in the CM0 register to 1 (XIN clock stops), the CM11 bit in the CM1 register to 1 (internal feedback resistor disabled), and the CM13 bit to 1 (XIN-XOUT pin).
3. The clock frequency is automatically set to up to 20 MHz by a divider when using the high-speed on-chip oscillator as the CPU clock source.
4. This applies when the CSPROINI bit in the OFS register is set to 1 (count source protection mode disabled after reset).
5. This applies when the CSPROINI bit in the OFS register is set to 0 (count source protection mode enabled after reset).
6. The XIN clock oscillation circuit is used as the base clock source in the PLL frequency synthesizer.
   These items vary depending on the XIN clock oscillation circuit.
7. The output is set to 48 MHz for the USB.

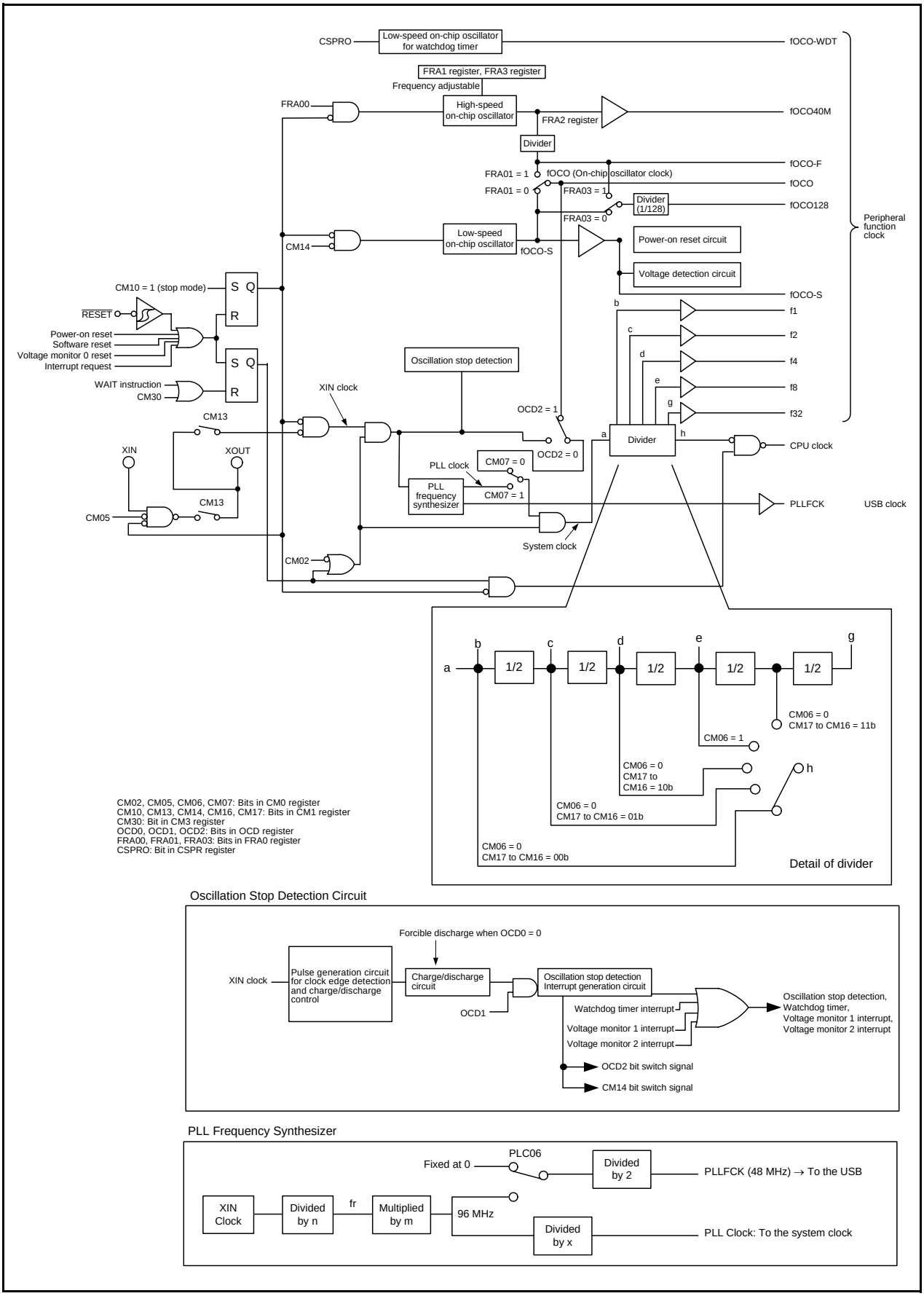


Figure 9.1 Clock Generation Circuit

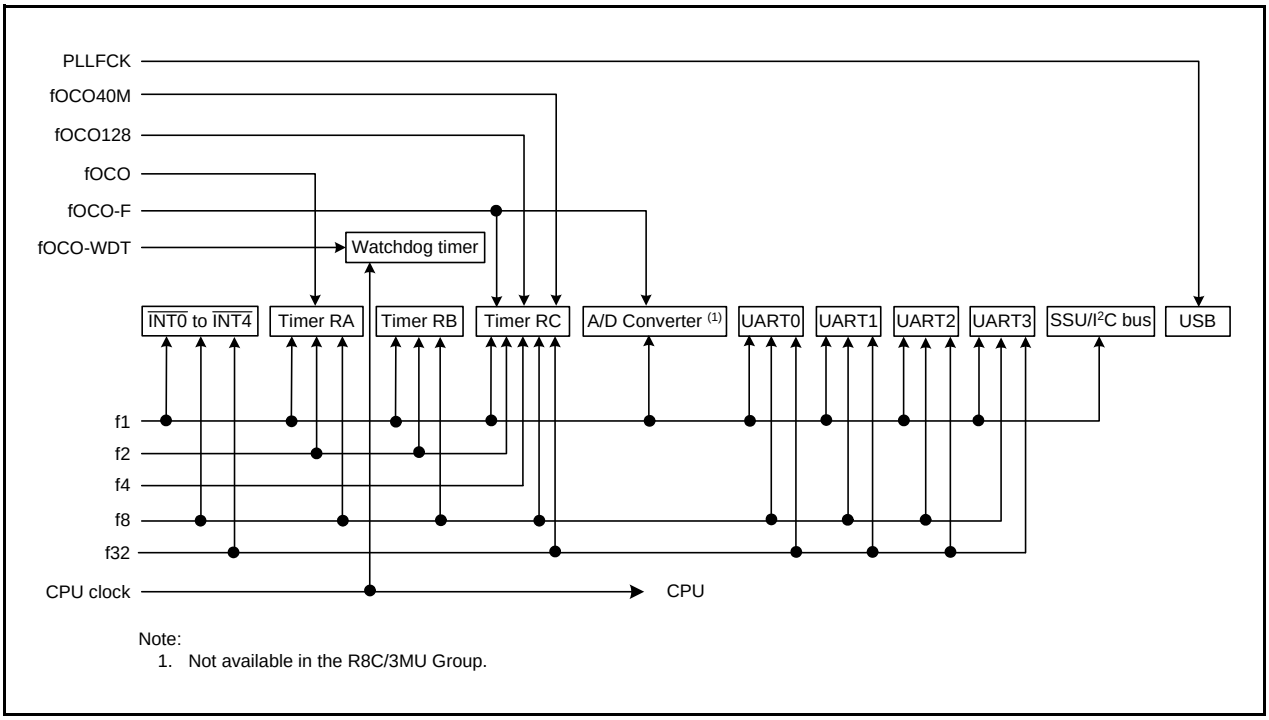


Figure 9.2 Peripheral Function Clock

9.2 Registers

9.2.1 System Clock Control Register 0 (CM0)

Address 0006h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CM07	CM06	CM05	—	—	CM02	—	—
After Reset	0	0	1	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			R/W
b2	CM02	Wait mode peripheral function clock stop bit	0: Peripheral function clock does not stop in wait mode 1: Peripheral function clock stops in wait mode	R/W
b3	—	Reserved bits	Set to 0.	R/W
b4	—			R/W
b5	CM05	XIN clock (XIN-XOUT) stop bit (1, 3)	0: XIN clock oscillates 1: XIN clock stops (2)	R/W
b6	CM06	CPU clock division select bit 0 (4)	0: Bits CM16 and CM17 in CM1 register enabled 1: Divide-by-8 mode	R/W
b7	CM07	CPU clock select bit (5)	0: XIN clock 1: PLL clock	R/W

Notes:

1. The CM05 bit stops the XIN clock when the high-speed on-chip oscillator mode or low-speed on-chip oscillator mode is selected. This bit cannot be used to detect whether the XIN clock has stopped. To stop the XIN clock, set the bits in the following order:
   (1) Set bits OCD1 to OCD0 in the OCD register to 00b.
   (2) Set the OCD2 bit to 1 (on-chip oscillator clock selected).
2. During external clock input, only the clock oscillation buffer stops and clock input is acknowledged.
3. Only when the CM05 bit is set to 1 (XIN clock stops) and the CM13 bit in the CM1 register is set to 0 (P4_6 and P4_7), P4_6 and P4_7 can be used as I/O ports.
   The P4_6 pin is multiplexed with the XIN pin and the P4_7 pin is multiplexed with the XOUT pin. When using the XIN clock, these pins cannot be used as I/O ports.
4. When the MCU enters stop mode, the CM06 bit is set to 1 (divide-by-8 mode).
5. After setting the PLC07 bit in PLL control register 0 to 1 (PLL operates) and the PLL clock oscillation stabilizes, change the CM07 bit from 0 to 1 (PLL clock).

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the CM0 register.

9.2.2 System Clock Control Register 1 (CM1)

Address 0007h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CM17	CM16	—	CM14	CM13	—	CM11	CM10
After Reset	0	0	1	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CM10	All clock stop control bit (2, 7)	0: Clock oscillates 1: All clocks stop (stop mode)	R/W
b1	CM11	XIN-XOUT on-chip feedback resistor select bit	0: On-chip feedback resistor enabled 1: On-chip feedback resistor disabled	R/W
b2	—	Reserved bit	Set to 0.	R/W
b3	CM13	Port/XIN-XOUT switch bit (5, 6)	0: I/O ports P4_6 and P4_7 1: XIN-XOUT pin	R/W
b4	CM14	Low-speed on-chip oscillator stop bit (3, 4)	0: Low-speed on-chip oscillator on 1: Low-speed on-chip oscillator off	R/W
b5	—	Reserved bit	Set to 1.	R/W
b6	CM16	CPU clock division select bit 1 (1)	b7 b6 0 0: No division mode 0 1: Divide-by-2 mode 1 0: Divide-by-4 mode 1 1: Divide-by-16 mode	R/W
b7	CM17			R/W

Notes:
1. When the CM06 bit is set to 0 (bits CM16 and CM17 enabled), bits CM16 and CM17 are enabled.
2. If the CM10 bit is set to 1 (stop mode), the on-chip feedback resistor is disabled.
3. When the OCD2 bit is set to 0 (XIN clock selected), the CM14 bit can be set to 1 (low-speed on-chip oscillator off). When the OCD2 bit is set to 1 (on-chip oscillator clock selected), the CM14 bit is set to 0 (low-speed on-chip oscillator on). It remains unchanged even if 1 is written to it.
4. To use the voltage monitor 1 interrupt or voltage monitor 2 interrupt (when the digital filter is used), set the CM14 bit to 0 (low-speed on-chip oscillator on).
5. When using these pins as I/O ports, set the CM13 bit to 0 (I/O ports) and the CM05 bit in the CM0 register to 1 (XIN clock stops).
   When using them as external clock input, set the CM13 bit to 1 (XIN-XOUT pin), the CM05 bit to 1 (XIN clock stops), and the CM11 bit to 1 (internal feedback resistor disabled). In addition, an external clock can be input if the PD4_7 bit in the PD4 register is set to 0 (input mode). Set XIN as the I/O port P4_6 at this time. When these pins are not used, treat them as unassigned pins and use the appropriate handling. The P4_6 pin is multiplexed with the XIN pin and the P4_7 pin is multiplexed with the XOUT pin. When using the on-chip oscillation circuit, these pins cannot be used as I/O ports.
6. Once the CM13 bit is set to 1 by a program, it cannot be set to 0.
7. Do not set the CM10 bit to 1 (stop mode) when the VCA20 bit in the VCA2 register to 1 (low consumption enabled).

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the CM1 register.

9.2.3 System Clock Control Register 3 (CM3)

Address 0009h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CM37	CM36	CM35	—	—	—	—	CM30
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CM30	Wait control bit (1)	0: Other than wait mode 1: MCU enters wait mode	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	—			
b3	—	Reserved bits	Set to 0.	R/W
b4	—			
b5	CM35	CPU clock division when exiting wait mode select bit (2)	0: Following settings are enabled: CM06 bit in CM0 register Bits CM16 and CM17 in CM1 register 1: No division	R/W
b6	CM36	System clock when exiting wait mode or stop mode select bit	b7 b6 0 0: MCU exits with the CPU clock immediately before entering wait or stop mode. 0 1: Do not set. 1 0: High-speed on-chip oscillator clock selected (3) 1 1: XIN clock selected (4)	R/W
b7	CM37			R/W

Notes:
1. When the MCU exits wait mode by a peripheral function interrupt, the CM30 bit is set to 0 (other than wait mode).
2. Set the CM35 bit to 0 in stop mode. When the MCU enters wait mode, if the CM35 bit is set to 1 (no division), the CM06 bit in the CM0 register is set to 0 (bits CM16 and CM17 enabled) and bits CM17 and CM16 in the CM1 register is set to 00b (no division mode).
3. When bits CM37 and CM36 are set to 10b (high-speed on-chip oscillator clock selected), the following will be set when the MCU exits wait mode or stop mode.
   • OCD2 bit in OCD register = 1 (on-chip oscillator selected)
   • FRA00 bit in FRA0 register = 1 (high-speed on-chip oscillator on)
   • FRA01 bit in FRA0 register = 1 (high-speed on-chip oscillator selected)
4. When bits CM37 and CM36 are set to 11b (XIN clock selected), the following will be set when the MCU exits wait mode or stop mode.
   • OM05 bit in OM0 register = 0 (XIN clock oscillates)
   • OM13 bit in OM1 register = 1 (XIN-XOUT pin)
   • OCD2 bit in OCD register = 0 (XIN clock selected)
   When the MCU enters wait mode while the CM05 bit in the CM0 register is 1 (XIN clock stops), if the XIN clock is selected as the CPU clock when exiting wait mode, set the CM06 bit to 1 (divide-by-8 mode) and the CM35 bit to 0.
   However, if an externally generated clock is used as the XIN clock, do not set bits CM37 to CM36 to 11b (XIN clock selected).

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the CM3 register.

CM30 bit (Wait Control Bit)

When the CM30 bit is set to 1 (MCU enters wait mode), the CPU clock stops (wait mode). Since the XIN clock, and the on-chip oscillator clock do not stop, the peripheral functions using these clocks continue operating. To set the CM30 bit to 1, set the I flag to 0 (maskable interrupt disabled).

The MCU exits wait mode by a reset or peripheral function interrupt. When the MCU exits wait mode by a peripheral function interrupt, it resumes executing the instruction immediately after the instruction to set the CM30 bit to 1.

When the MCU enters wait mode with the WAIT instruction, make sure to set the I flag to 1 (maskable interrupt enabled). With this setting, interrupt handling is performed by the CPU when the MCU exits wait mode.

9.2.4 Oscillation Stop Detection Register (OCD)

Address 000Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	OCD3	OCD2	OCD1	OCD0
After Reset	0	0	0	0	0	1	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	OCD0	Oscillation stop detection enable bit (6)	0: Oscillation stop detection function disabled (1) 1: Oscillation stop detection function enabled	R/W
b1	OCD1	Oscillation stop detection interrupt enable bit	0: Disabled (1) 1: Enabled	R/W
b2	OCD2	System clock select bit (3)	0: XIN clock selected (6) 1: On-chip oscillator clock selected (2)	R/W
b3	OCD3	Clock monitor bit (4, 5)	0: XIN clock oscillates 1: XIN clock stops	R
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—			
b7	—			

Notes:
1. Set bits OCD1 to OCD0 to 00b before the MCU enters stop mode, high-speed on-chip oscillator mode, or low-speed on-chip oscillator mode (XIN clock stops).
2. If the OCD2 bit is set to 1 (on-chip oscillator clock selected), the CM14 bit is set to 0 (low-speed on-chip oscillator on).
3. The OCD2 bit is automatically set to 1 (on-chip oscillator clock selected) if XIN clock oscillation stop is detected while bits OCD1 to OCD0 are set to 11b. If the OCD3 bit is set to 1 (XIN clock stops), the OCD2 bit remains unchanged even when set to 0 (XIN clock selected).
4. The OCD3 bit is enabled when the OCD0 bit is set to 1 (oscillation stop detection function enabled). In addition, the OCD3 bit cannot be used to confirm whether the XIN clock oscillation is stable.
5. The OCD3 bit remains 0 (XIN clock oscillates) if bits OCD1 to OCD0 are set to 00b.
6. Refer to **Figure 9.10 Procedure for Switching from Low-Speed On-Chip Oscillator to XIN Clock when Oscillation Stop is Detected** for the switching procedure when the XIN clock re-oscillates after detecting oscillation stop.

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the OCD register.

9.2.5 High-Speed On-Chip Oscillator Control Register 7 (FRA7)

Address 0015h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	When shipping							

Bit	Function	R/W
b7-b0	32 MHz frequency correction data is stored. The frequency can be adjusted by transferring this value to the FRA3 register and by transferring the correction value in the FRA6 register to the FRA1 register.	R

9.2.6 High-Speed On-Chip Oscillator Control Register 0 (FRA0)

Address 0023h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	FRA03	—	FRA01	FRA00
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	FRA00	High-speed on-chip oscillator enable bit	0: High-speed on-chip oscillator off 1: HIgh-speed on-chip oscillator on	R/W
b1	FRA01	High-speed on-chip oscillator select bit (1)	0: Low-speed on-chip oscillator selected (2) 1: High-speed on-chip oscillator selected (3)	R/W
b2	—	Reserved bit	Set to 0.	R/W
b3	FRA03	fOCO128 clock select bit	0: fOCO-S divided by 128 selected 1: fOCO-F divided by 128 selected	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

Notes:
1. Change the FRA01 bit in the following conditions.
   - FRA00 = 1 (high-speed on-chip oscillator on)
   - The CM14 bit in the CM1 register = 0 (low-speed on-chip oscillator on)
   - Bits FRA22 to FRA20 in the FRA2 register:
     All division mode can be set when VCC = 2.7 to 5.5 V 000b to 111b
     Divide ratio of 8 or more when VCC = 1.8 to 5.5 V 110b to 111b (divide-by-8 or more)
2. When setting the FRA01 bit to 0 (low-speed on-chip oscillator selected), do not set the FRA00 bit to 0 (high-speed on-chip oscillator off) at the same time. Set the FRA00 bit to 0 after setting the FRA01 bit to 0.
3. When setting the FRA01 bit to be 1 (high-speed on-chip oscillator selected) and stopping the low-speed on-chip oscillator, wait for one or more cycles of the low-speed on-chip oscillator and then set the CM14 bit in the CM1 register to 1 (low-speed on-chip oscillator off)

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the FRA0 register.

9.2.7 High-Speed On-Chip Oscillator Control Register 1 (FRA1)

Address 0024h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	When shipping							

Bit	Function	R/W
b7-b0	The frequency of the high-speed on-chip oscillator can be adjusted by setting as follows: 40 MHz: FRA1 = value after reset, FRA3 = value after reset 36.864 MHz: Transfer the value in the FRA4 register to the FRA1 register and the value in the FRA5 register to the FRA3 register. 32 MHz: Transfer the value in the FRA6 register to the FRA1 register and the value in the FRA7 register to the FRA3 register.	R/W

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the FRA1 register.
Also, rewrite the FRA1 register when the FRA00 bit in the FRA0 register is set 0 (high-speed on-chip oscillator off).

9.2.8 High-Speed On-Chip Oscillator Control Register 2 (FRA2)

Address 0025h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	FRA22	FRA21	FRA20
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	FRA20	High-speed on-chip oscillator frequency switching bit	Division selection These bits select the division ratio for the high-speed on-chip oscillator clock. b2 b1 b0 0 0 0: Divide-by-2 mode 0 0 1: Divide-by-3 mode 0 1 0: Divide-by-4 mode 0 1 1: Divide-by-5 mode 1 0 0: Divide-by-6 mode 1 0 1: Divide-by-7 mode 1 1 0: Divide-by-8 mode 1 1 1: Divide-by-9 mode	R/W
b1	FRA21			R/W
b2	FRA22			R/W
b3	—	Reserved bits	Set to 0.	R/W
b4	—			
b5	—			
b6	—			
b7	—			

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the FRA2 register.

9.2.9 Clock Prescaler Reset Flag (CPSRF)

Address 0028h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CPSR	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	CPSR	Clock prescaler reset flag	Setting this bit to 1 initializes the clock prescaler. (When read, the content is 0.)	R/W

9.2.10 High-Speed On-Chip Oscillator Control Register 4 (FRA4)

Address 0029h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	When shipping							

Bit	Function	R/W
b7-b0	36.864 MHz frequency correction data is stored. The frequency can be adjusted by transferring this value to the FRA1 register and by transferring the correction value in the FRA5 register to the FRA3 register.	R

9.2.11 High-Speed On-Chip Oscillator Control Register 5 (FRA5)

Address 002Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	When shipping							

Bit	Function	R/W
b7-b0	36.864 MHz frequency correction data is stored. The frequency can be adjusted by transferring this value to the FRA3 register and by transferring the correction value in the FRA4 register to the FRA1 register.	R

9.2.12 High-Speed On-Chip Oscillator Control Register 6 (FRA6)

Address 002Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	When shipping							

Bit	Function	R/W
b7-b0	32 MHz frequency correction data is stored. The frequency can be adjusted by transferring this value to the FRA1 register and by transferring the correction value in the FRA7 register to the FRA3 register.	R

9.2.13 High-Speed On-Chip Oscillator Control Register 3 (FRA3)

Address 002Fh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	When shipping							

Bit	Function	R/W
b7-b0	The frequency of the high-speed on-chip oscillator can be adjusted by setting as follows: 40 MHz: FRA1 = value after reset, FRA3 = value after reset 36.864 MHz: Transfer the value in the FRA4 register to the FRA1 register and the value in the FRA5 register to the FRA3 register. 32 MHz: Transfer the value in the FRA6 register to the FRA1 register and the value in the FRA7 register to the FRA3 register.	R/W

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the FRA3 register.
Also, rewrite the FRA3 register when the FRA00 bit in the FRA0 register is set 0 (high-speed on-chip oscillator off).

9.2.14 Voltage Detect Register 2 (VCA2)

Address 0034h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	VCA27	VCA26	VCA25	—	—	—	—	VCA20
After Reset	0	0	0	0	0	0	0	0
	The above applies when the LVDAS bit in the OFS register is set to 1.							
After Reset	0	0	1	0	0	0	0	0
	The above applies when the LVDAS bit in the OFS register is set to 0.							

Bit	Symbol	Bit Name	Function	R/W
b0	VCA20	Internal power low consumption enable bit (1)	0: Low consumption disabled 1: Low consumption enabled (2)	R/W
b1	—	Reserved bits	Set to 0.	R/W
b2	—			
b3	—			
b4	—			
b5	VCA25	Voltage detection 0 enable bit (3)	0: Voltage detection 0 circuit disabled 1: Voltage detection 0 circuit enabled	R/W
b6	VCA26	Voltage detection 1 enable bit (4)	0: Voltage detection 1 circuit disabled 1: Voltage detection 1 circuit enabled	R/W
b7	VCA27	Voltage detection 2 enable bit (5)	0: Voltage detection 2 circuit disabled 1: Voltage detection 2 circuit enabled	R/W

Notes:
1. Use the VCA20 bit only when the MCU enters wait mode. To set the VCA20 bit, follow the procedure shown in **Figure 9.3 Procedure for Reducing Internal Power Consumption Using VCA20 bit**.
2. When the VCA20 bit is set to 1 (low consumption enabled), do not set the CM10 bit in the CM1 register to 1 (stop mode).
3. When writing to the VCA25 bit, set a value after reset.
4. To use the voltage detection 1 interrupt or the VW1C3 bit in the VW1C register, set the VCA26 bit to 1. After the VCA26 bit is set to 1 from 0, allow td(E-A) to elapse before the voltage detection 1 circuit starts operation.
5. To use the voltage detection 2 interrupt or the VCA13 bit in the VCA1 register, set the VCA27 bit to 1. After the VCA27 bit is set to 1 from 0, allow td(E-A) to elapse before the voltage detection 2 circuit starts operation.

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VCA2 register.

9.2.15 I/O Function Pin Select Register (PINSR)

Address 018Fh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	SDADLY1	SDADLY0	IICTCHALF	IICTCTWI	IOINSEL	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	IOINSEL	I/O port input function select bit	0: The I/O port input function depends on the PDi (i = 0, 1, 3, 4, 6 to 8) register. When the PDi_j (j = 0 to 7) bit in the PDi register is set to 0 (input mode), the pin input level is read. When the PDi_j bit in the PDi register is set to 1 (output mode), the port latch is read. 1: The I/O port input function reads the pin input level regardless of the PDi register	R/W
b4	IICTCTWI	I²C double transfer rate select bit	0: Transfer rate is the same as the value set with bits CKS0 to CKS3 in the ICCR1 register 1: Transfer rate is twice the value set with bits CKS0 to CKS3 in the ICCR1 register	R/W
b5	IICTCHALF	I²C half transfer rate select bit	0: Transfer rate is the same as the value set with bits CKS0 to CKS3 in the ICCR1 register 1: Transfer rate is half the value set with bits CKS0 to CKS3 in the ICCR1 register	R/W
b6	SDADLY0	SDA digital delay select bit	b7 b6 0 0: Digital delay of 3 × f1 cycles 0 1: Digital delay of 11 × f1 cycles 1 0: Digital delay of 19 × f1 cycles 1 1: Do not set.	R/W
b7	SDADLY1			R/W

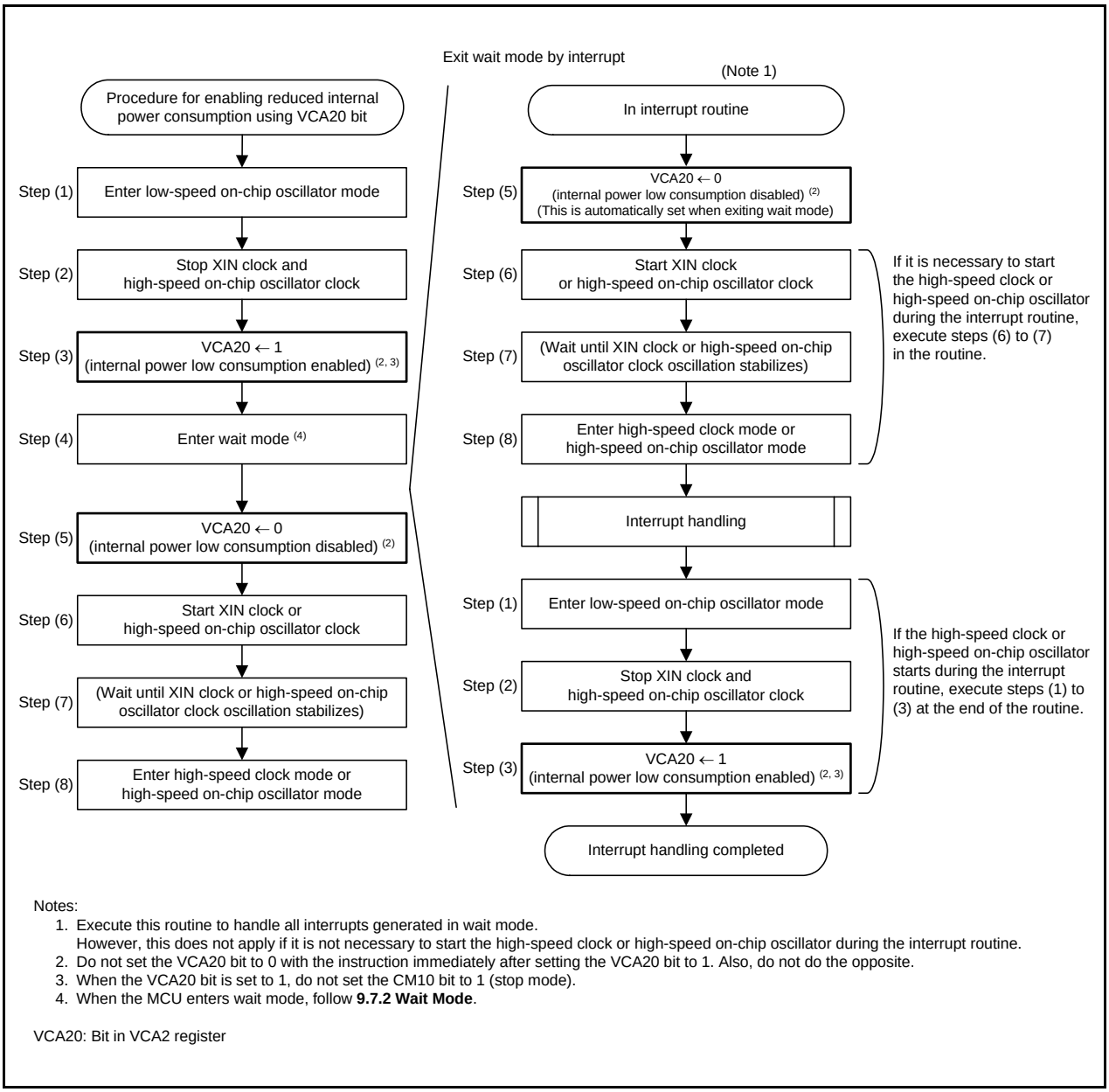
IOINSEL Bit (I/O port input function select bit)

The IOINSEL bit is used to select the pin level of an I/O port when the PDi_j (j = 0 to 7) bit in the PDi (i = 0, 1, 3, 4, 6 to 8) register is set to 1 (output mode). When this bit is set to 1, the I/O port input function reads the pin input level regardless of the PDi register.

Table 9.2 lists I/O Port Values Read by Using IOINSEL Bit. The IOINSEL bit can be used to change the input function of all I/O ports.

Table 9.2 I/O Port Values Read by Using IOINSEL Bit

PDi_j bit in PDi register	0 (input mode)		1 (output mode)	
IOINSEL bit	0	1	0	1
I/O port values read	Pin input level		Port latch value	Pin input level



Notes:
1. Execute this routine to handle all interrupts generated in wait mode.
   However, this does not apply if it is not necessary to start the high-speed clock or high-speed on-chip oscillator during the interrupt routine.
2. Do not set the VCA20 bit to 0 with the instruction immediately after setting the VCA20 bit to 1. Also, do not do the opposite.
3. When the VCA20 bit is set to 1, do not set the CM10 bit to 1 (stop mode).
4. When the MCU enters wait mode, follow **9.7.2 Wait Mode**.

VCA20: Bit in VCA2 register

Figure 9.3 Procedure for Reducing Internal Power Consumption Using VCA20 bit

9.2.16 PLL Control Register 0 (PLC0)

Address 2F01h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PLC07	PLC06	PLC05	PLC04	—	—	PLC01	PLC00
After Reset	0	0	1	0	X	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PLC00	PLL power supply control bit	0: PLL power supply off 1: PLL power supply on	R/W
b1	PLC01	PLL output control bit	0: PLL output stops 1: PLL output enabled	R/W
b2	—	Reserved bit	Set to 0.	R/W
b3	—	Reserved bit	When read, the content is undefined.	R
b4	PLC04	Reference frequency counter set bit	b5 b4 0 1: Divided by 2 1 0: Divided by 4 Other than above: Do not set.	R/W
b5	PLC05			
b6	PLC06	PLLFCK generation enable bit	0: PLLFCK generation disabled 1: PLLFCK generation enabled	R/W
b7	PLC07	Operation enable bit	0: PLL stops 1: PLL operates	R/W

9.2.17 PLL Control Register 1 (PLC1)

Address 2F02h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	PLC14	PLC13	PLC12	—	—
After Reset	0	0	0	0	1	1	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	PLC12	PLL multiplication select bit	b4 b3 b2 0 1 1: Multiplied by 24 1 0 0: Multiplied by 32 Other than above: Do not set.	R/W
b3	PLC13			
b4	PLC14			
b5	—	Reserved bits	Set to 0.	R/W
b6	—			
b7	—			

9.2.18 PLL Division Control Register (PLDIV)

Address 2F03h

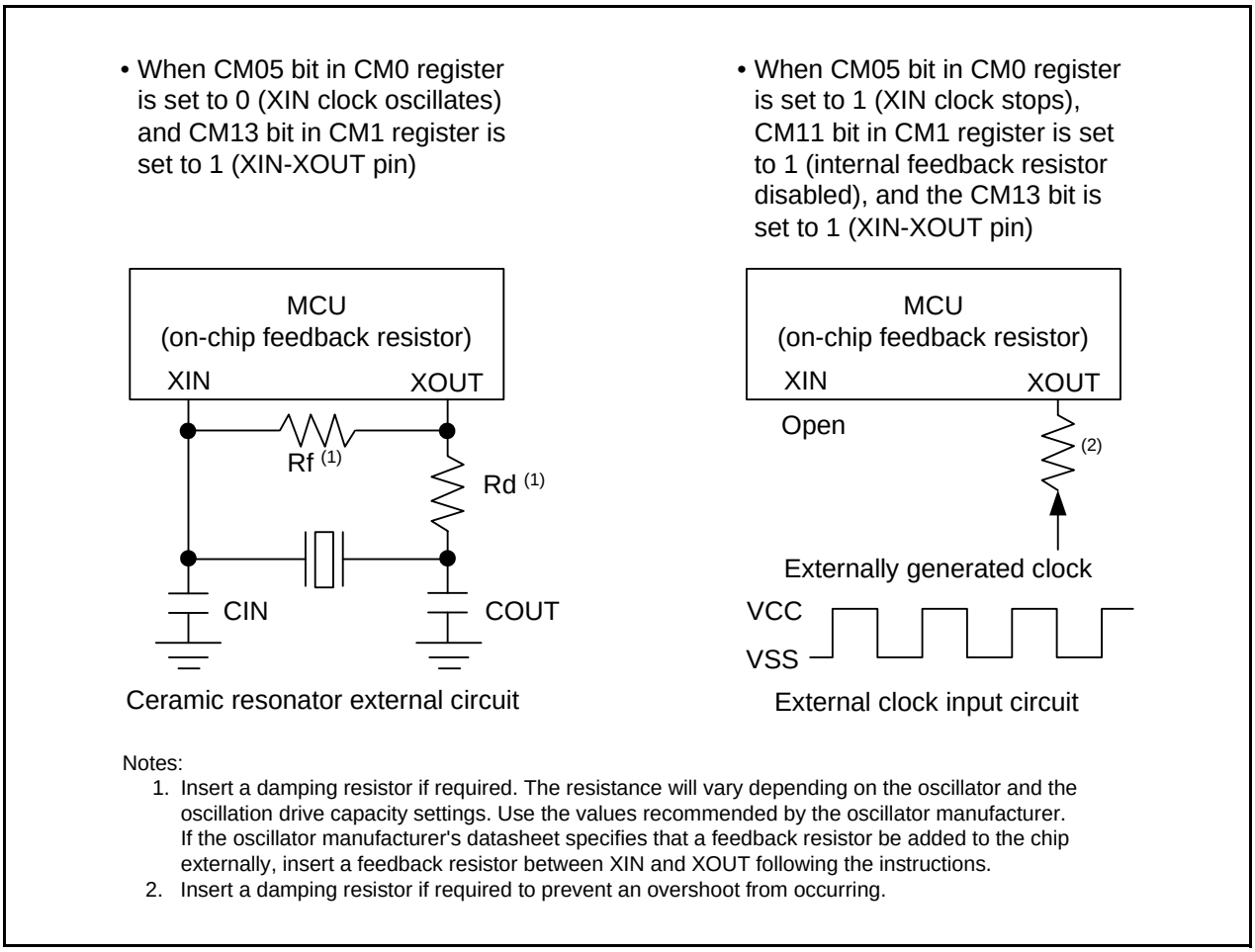
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	FCKDIV0	CPUDIV2	CPUDIV1	CPUDIV0
After Reset	0	0	0	0	1	0	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	CPUDIV0	CPU clock division select bit	b2 b1 b0 0 0 0: Fixed at high 0 1 0: Divided by 8 0 1 1: Divided by 6 1 0 0: Divided by 16 Other than above: Do not set.	R/W
b1	CPUDIV1			
b2	CPUDIV2			
b3	FCKDIV0	PLLFCK division select bit	0: Fixed at high 1: Divided by 2	R/W
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—			
b7	—			

The clocks generated by the clock generation circuits are described below.

9.3 XIN Clock

The XIN clock is supplied by the XIN clock oscillation circuit. This clock is used as the clock source for the CPU and peripheral function clocks. The XIN clock oscillation circuit is configured by connecting a resonator between pins XIN and XOUT. The XIN clock oscillation circuit includes an on-chip feedback resistor, which is disconnected from the oscillation circuit in stop mode in order to reduce the amount of power consumed by the chip. The XIN clock oscillation circuit may also be configured by feeding an externally generated clock to the XOUT pin.
Figure 9.4 shows Examples of XIN Clock Connection Circuit.
During and after a reset, the XIN clock stops.
After setting the CM13 bit in the CM1 register to 1 (XIN-XOUT pin), the XIN clock starts oscillating when the CM05 bit in the CM0 register is set to 0 (XIN clock oscillates). After the XIN clock oscillation stabilizes, the XIN clock is used as the CPU clock source when the OCD2 bit in the OCD register is set to 0 (XIN clock selected).
The power consumption can be reduced by setting the CM05 bit in the CM0 register to 1 (XIN clock stops) if the OCD2 bit is set to 1 (on-chip oscillator clock selected).
When an externally generated clock is input to the XOUT pin, the XIN clock does not stop even if the CM05 bit is set to 1. If necessary, use an external circuit to stop the clock.
In stop mode, all clocks including the XIN clock stop. Refer to **9.7 Power Control** for details.



Notes:
1. Insert a damping resistor if required. The resistance will vary depending on the oscillator and the oscillation drive capacity settings. Use the values recommended by the oscillator manufacturer. If the oscillator manufacturer's datasheet specifies that a feedback resistor be added to the chip externally, insert a feedback resistor between XIN and XOUT following the instructions.
2. Insert a damping resistor if required to prevent an overshoot from occurring.

Figure 9.4 Examples of XIN Clock Connection Circuit

9.4 On-Chip Oscillator Clock

The on-chip oscillator clock is supplied by the on-chip oscillator (high-speed on-chip oscillator or low-speed on-chip oscillator). This clock is selected by the FRA01 bit in the FRA0 register.

9.4.1 Low-Speed On-Chip Oscillator Clock

The clock generated by the low-speed on-chip oscillator is used as the clock source for the CPU clock, peripheral function clock, fOCO, fOCO-S, and fOCO128.
After a reset, the on-chip oscillator clock generated by the low-speed on-chip oscillator divided by 1 (no division) is selected as the CPU clock.
If the XIN clock stops oscillating when bits OCD1 to OCD0 in the OCD register are set to 11b, the low-speed on-chip oscillator automatically starts operating and supplies the necessary clock for the MCU.
The frequency of the low-speed on-chip oscillator varies depending on the supply voltage and the operating ambient temperature. Application products must be designed with sufficient margin to allow for frequency changes.

9.4.2 High-Speed On-Chip Oscillator Clock

The clock generated by the high-speed on-chip oscillator is used as the clock source for the CPU clock, peripheral function clock, fOCO, fOCO-F, fOCO40M, and fOCO128.
To use the high-speed on-chip oscillator clock as the clock source for the CPU clock, peripheral clock, fOCO, and fOCO-F, set bits FRA20 to FRA22 in the FRA2 register as follows:

- All division mode can be set when VCC = 2.7 to 5.5 V 000b to 111b
- Divide ratio of 8 or more when VCC = 1.8 to 5.5 V 110b to 111b (divide by 8 or more)

After a reset, the on-chip oscillator clock generated by the high-speed on-chip oscillator stops. Oscillation is started by setting the FRA00 bit in the FRA0 register to 1 (high-speed on-chip oscillator on).

Frequency correction data is stored in registers FRA4 to FRA7.
To adjust the frequency of the high-speed on-chip oscillator clock to 36.864 MHz, first transfer the correction value in the FRA4 register to the FRA1 register and the correction value in the FRA5 register to the FRA3 register before using the values. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode (refer to **Tables 20.8 and 21.8 Bit Rate Setting Example in UART Mode**).
To adjust the frequency of the high-speed on-chip oscillator clock to 32 MHz, first transfer the correction value in the FRA6 register to the FRA1 register and the correction value in the FRA7 register to the FRA3 register before using the values.

9.5 PLL Clock

The PLL clock is generated by the PLL frequency synthesizer. This clock is used as the clock source for the CPU clock and the peripheral function clock.
The PLL frequency synthesizer is stopped after a reset.
The PLL clock is obtained by dividing and multiplying the XIN clock.
Set bits PLC05 and PLC04 in the PLC0 register so that the clock frequency after division will be set to 3 MHz to 4 MHz.
To oscillate the PLL clock, follow the procedure below:

(1) Set the PLC00 bit in the PLC0 register to 1 (PLL power supply on).
(2) Set the PLC01 bit in the PLC0 register to 1 (PLL output enabled).
(3) Set the PLC06 bit in the PLC0 register to 1 (PLLFCK generation enabled).
(4) Set the PLC07 bit in the PLC0 register to 1 (PLL operates).
(5) Wait for ($t_{SU(PLL)}$) until the PLL clock stabilizes.
(6) Set the SCKE bit in the SYSCFG register to 1 (supplying the clock signal to the USB module enabled).

Figure 9.5 shows the Relation between XIN Clock and PLL Clock.

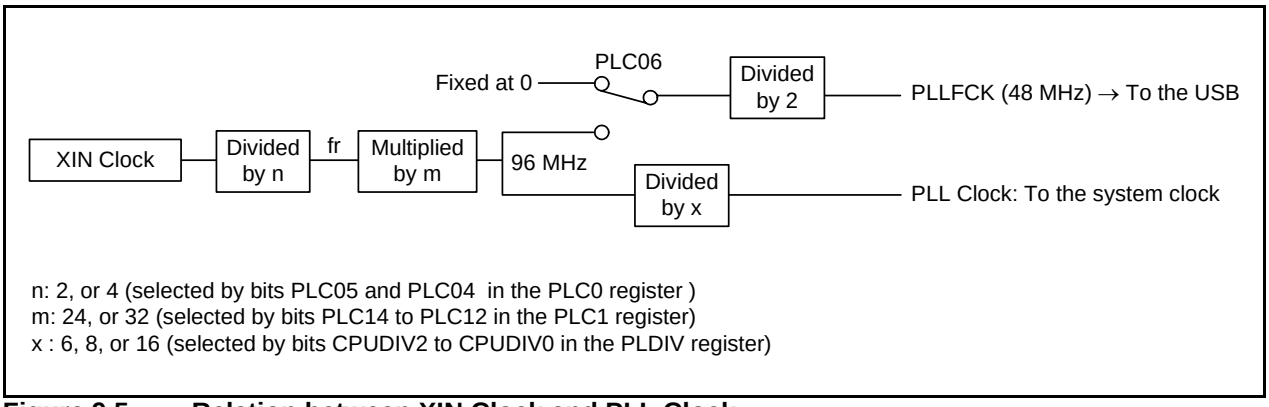


Figure 9.5 Relation between XIN Clock and PLL Clock

Table 9.3 lists an Example of USB Clock Frequency Settings, and Table 9.4 lists an Settings and Modes of Clock Associated Bits.

Table 9.3 Example of USB Clock Frequency Settings

XIN Clock	Divided by n		Frequency (fr) divided by n	Multiplied by m		USB Clock (PLLFCK)
	PLC05 and PLC04 bits			PLC14 to PLC12 bits		
16 MHz	10b	Divided by 4	4 MHz	011b	Multiplied by 24	48 MHz
12 MHz	10b	Divided by 4	3 MHz	100b	Multiplied by 32	48 MHz
8 MHz	01b	Divided by 2	4 MHz	011b	Multiplied by 24	48 MHz

Table 9.4 Example of PLL Clock Frequency Settings

Divided by x		PLL Clock
CPUDIV2 to CPUDIV0 bits		
100b	Divided by 16	6 MHz
011b	Divided by 6	16 MHz
010b	Divided by 8	12 MHz

9.6 CPU Clock and Peripheral Function Clock

There are a CPU clock to operate the CPU and a peripheral function clock to operate the peripheral functions (refer to **Figure 9.1 Clock Generation Circuit**).

9.6.1 System Clock

The system clock is the clock source for the CPU and peripheral function clocks. The XIN clock, or the on-chip oscillator clock can be selected.

9.6.2 CPU Clock

The CPU clock is an operating clock for the CPU and the watchdog timer.
The system clock divided by 1 (no division), 2, 4, 8, or 16 is used as the CPU clock. Use the CM06 bit in the CM0 register and bits CM16 and CM17 in the CM1 register to select the value of the division.
After a reset, the low-speed on-chip oscillator clock divided by 1 (no division) is used as the CPU clock.
When the MCU enters stop mode, the CM06 bit is set to 1 (divide-by-8 mode). To enter stop mode, set the CM35 bit in the CM3 register to 0 (settings of CM06 in CM0 register and bits CM16 and CM17 in CM1 register enabled).

9.6.3 Peripheral Function Clock (f1, f2, f4, f8, and f32)

The peripheral function clock is an operating clock for the peripheral functions.
The fi (i = 1, 2, 4, 8, and 32) clock is generated by the system clock divided by i. It is used for timers RA, RB, RC, the serial interface, and A/D converter.
If the MCU enters wait mode after the CM02 bit in the CM0 register is set to 1 (peripheral function clock stops in wait mode), the fi clock stops.

9.6.4 fOCO

fOCO is an operating clock for the peripheral functions.
The frequency of fOCO is the frequency of the on-chip oscillator clock selected by the FRA01 bit in the FRA0 register. For the high-speed on-chip oscillator, its frequency is the frequency divided by the divide ratio selected by bits FRA20 to FRA22 in the FRA2 register. fOCO can be used for timer RA.
In wait mode, the fOCO clock does not stop.

9.6.5 fOCO40M

fOCO40M is used as the count source for timers RC.
This clock is generated by the high-speed on-chip oscillator and supplied by setting the FRA00 bit to 1.
In wait mode, the fOCO40M clock does not stop.
This clock can be used with supply voltage VCC = 2.7 to 5.5 V.

9.6.6 fOCO-F

fOCO-F is used as the count source for timer RC, and the A/D converter.
fOCO-F is a clock generated by the high-speed on-chip oscillator and divided by i (i = 2, 3, 4, 5, 6, 7, 8, and 9; divide ratio selected by the FRA2 register). This clock is supplied by setting the FRA00 bit to 1.
In wait mode, the fOCO-F clock does not stop.

9.6.7 fOCO-S

fOCO-S is an operating clock for the voltage detection circuit.
This clock is generated by the low-speed on-chip oscillator and supplied by setting the CM14 bit to 0 (low-speed on-chip oscillator on).
In wait mode, the fOCO-S clock does not stop.

9.6.8 fOCO128

fOCO128 is a clock generated by dividing fOCO-S or fOCO-F by 128. When the FRA03 bit is set to 0, fOCO-S divided by 128 is selected. When this bit is set to 1, fOCO-F divided by 128 is selected.
fOCO128 is configured as the capture signal used in the TRCGRA register for timer RC.

9.6.9 fOCO-WDT

fOCO-WDT is an operating clock for the watchdog timer.
This clock is generated by the low-speed on-chip oscillator for the watchdog timer and supplied by setting the CSPRO bit in the CSPR register to 1 (count source protect mode enabled).
In count source protection mode for the watchdog timer, the fOCO-WDT clock does not stop.

9.6.10 PLLFCK

The PLLFCK is used for USB communications operation clock of the USB function. PLLFCK can be used when the PLC06 bit in the PLC0 register is set to 1 (PLLFCK generation enabled). Set registers PLC0, PLC1 and PLDIV at more than 48 MHz of PLLFCK.

9.7 Power Control

There are three power control modes. All modes other than wait mode and stop mode are referred to as standard operating mode.

9.7.1 Standard Operating Mode

Standard operating mode is further separated into four modes.
In standard operating mode, the CPU and peripheral function clocks are supplied to operate the CPU and the peripheral functions. Power consumption control is enabled by controlling the CPU clock frequency. The higher the CPU clock frequency, the more processing power increases. The lower the CPU clock frequency, the more power consumption decreases. If unnecessary oscillator circuits stop, power consumption is further reduced.
Before the clock sources for the CPU clock can be switched over, the new clock source needs to be oscillating and stable. Allow sufficient wait time in a program until oscillation stabilizes before switching the clock.

Table 9.5 Settings and Modes of Clock Associated Bits

Modes		OCD Register	CM1 Register			CM0 Register			FRA0 Register	
		OCD2	CM17, CM16	CM14	CM13	CM07	CM06	CM05	FRA01	FRA00
High-speed clock mode	No division	0	00b	—	1	0	0	0	—	—
	Divide-by-2	0	01b	—	1	0	0	0	—	—
	Divide-by-4	0	10b	—	1	0	0	0	—	—
	Divide-by-8	0	—	—	1	0	1	0	—	—
	Divide-by-16	0	11b	—	1	0	0	0	—	—
PLL operating mode	No division	0	00b	—	—	1	0	0	—	—
	Divide-by-2	0	01b	—	—	1	0	0	—	—
	Divide-by-4	0	10b	—	—	1	0	0	—	—
	Divide-by-8	0	—	—	—	1	1	0	—	—
	Divide-by-16	0	11b	—	—	1	0	0	—	—
High-speed on-chip oscillator mode	No division	1	00b	—	—	0	0	—	1	1
	Divide-by-2	1	01b	—	—	0	0	—	1	1
	Divide-by-4	1	10b	—	—	0	0	—	1	1
	Divide-by-8	1	—	—	—	0	1	—	1	1
	Divide-by-16	1	11b	—	—	0	0	—	1	1
Low-speed on-chip oscillator mode	No division	1	00b	0	—	0	0	—	0	—
	Divide-by-2	1	01b	0	—	0	0	—	0	—
	Divide-by-4	1	10b	0	—	0	0	—	0	—
	Divide-by-8	1	—	0	—	0	1	—	0	—
	Divide-by-16	1	11b	0	—	0	0	—	0	—

—: Indicates that either 0 or 1 can be set.

9.7.1.1 High-Speed Clock Mode

The XIN clock divided by 1 (no division), 2, 4, 8, or 16 is used as the CPU clock. If the CM14 bit is set to 0 (low-speed on-chip oscillator on) or the FRA00 bit in the FRA0 register is set to 1 (high-speed on-chip oscillator on), fOCO can be used for timer RA.
Also, if the FRA00 bit is set to 1, fOCO40M can be used for timer RC.
If the CM14 bit is set to 0 (low-speed on-chip oscillator on), fOCO-S can be used for the voltage detection circuit.

9.7.1.2 PLL Operating Mode

The CPU clock is obtained by dividing the PLL clock by 1 (no division), 2, 4, 8, or 16. Also, f1, which is the same frequency as that of the PLL clock divided by 1 (no division) is used as the peripheral function clock. The PLL operating mode can be entered from the high-speed clock mode.
If the FRA00 bit is set to 1, fOCO40M can be used for timer RC.
From the PLL operating mode, the high-speed clock mode can be entered. To enter any other modes including wait mode and stop mode, enter high-speed mode first and then enter to another mode (refer to **Figure 9.9 State Transitions in Power Control Mode**).

9.7.1.3 High-Speed On-Chip Oscillator Mode

The high-speed on-chip oscillator is used as the on-chip oscillator clock when the FRA00 bit in the FRA0 register is set to 1 (high-speed on-chip oscillator on) and the FRA01 bit in the FRA0 register is set to 1. The on-chip oscillator divided by 1 (no division), 2, 4, 8, or 16 is used as the CPU clock. If the FRA00 bit is set to 1, fOCO40M can be used for timer RC.
Also, if the CM14 bit is set to 0 (low-speed on-chip oscillator on), fOCO-S can be used for the voltage detection circuit.

9.7.1.4 Low-Speed On-Chip Oscillator Mode

If the CM14 bit in the CM1 register is set to 0 (low-speed on-chip oscillator on) and the FRA01 bit in the FRA0 register is set to 0, the low-speed on-chip oscillator is used as the on-chip oscillator clock. At this time, the on-chip oscillator clock divided by 1 (no division), 2, 4, 8 or 16 is used as the CPU clock. The on-chip oscillator clock is also the clock source for the peripheral function clocks. If the FRA00 bit is set to 1, fOCO40M can be used for timer RC.
Also, if the CM14 bit is set to 0 (low-speed on-chip oscillator on), fOCO-S can be used for the voltage detection circuit.
In this mode, low consumption operation is enabled by stopping the XIN clock and the high-speed on-chip oscillator, and by setting the FMR27 bit in the FMR2 register to 1 (low-current-consumption read mode enabled). When the CPU clock is set to the low-speed on-chip oscillator clock divided by 4, 8, or 16, low-current-consumption read mode can be used. After setting the divide ratio of the CPU clock, set the FMR27 bit to 1.
To enter wait mode from low-speed clock mode, lower consumption current in wait mode is enabled by setting the VCA20 bit in the VCA2 register to 1 (internal power low consumption enabled).
To reduce the power consumption, refer to **30. Reducing Power Consumption**.

9.7.2 Wait Mode

Since the CPU clock stops in wait mode, the CPU operating with the CPU clock and the watchdog timer when count source protection mode is disabled stop. Since the XIN clock, and on-chip oscillator clock do not stop, the peripheral functions using these clocks continue operating.

9.7.2.1 Peripheral Function Clock Stop Function

If the CM02 bit is set to 1 (peripheral function clock stops in wait mode), the f1, f2, f4, f8, and f32 clocks stop in wait mode. This reduces power consumption.

9.7.2.2 Entering Wait Mode

The MCU enters wait mode by executing the WAIT instruction or setting the CM30 bit in the CM3 register to 1 (MCU enters wait mode).
When the OCD2 bit in the OCD register is set to 1 (on-chip oscillator selected as system clock), set the OCD1 bit in the OCD register to 0 (oscillation stop detection interrupt disabled) before executing the WAIT instruction or setting the CM30 bit in the CM3 register to 1 (MCU enters wait mode).
If the MCU enters wait mode while the OCD1 bit is set to 1 (oscillation stop detection interrupt enabled), current consumption is not reduced because the CPU clock does not stop.
Enter wait mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled). Do not enter wait mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

9.7.2.3 Pin Status in Wait Mode

The I/O port retains the status immediately before the MCU enters wait mode.

9.7.2.4 Exiting Wait Mode

The MCU exits wait mode by a reset or peripheral function interrupt.
The peripheral function interrupts are affected by the CM02 bit. When the CM02 bit is set to 0 (peripheral function clock does not stop in wait mode), the peripheral function interrupts can be used to exit wait mode. When the CM02 bit is set to 1 (peripheral function clock stops in wait mode), the peripheral functions using the peripheral function clock stop and the peripheral functions operating with external signals or the on-chip oscillator clock can be used to exit wait mode.
Table 9.6 lists Interrupts to Exit Wait Mode and Usage Conditions.

Table 9.6 Interrupts to Exit Wait Mode and Usage Conditions

Interrupt	CM02 = 0	CM02 = 1
Serial interface interrupt	Usable when operating with internal or external clock	Usable when operating with external clock
Synchronous serial communication unit interrupt/ I^2C bus interface interrupt	Usable in all modes	(Do not use)
Key input interrupt	Usable	Usable
A/D conversion interrupt (1)	(Do not use)	(Do not use)
Timer RA interrupt	Usable in all modes	Usable if there is no filter in event counter mode. Usable by selecting fOCO as count source.
Timer RB interrupt	Usable in all modes	Usable by selecting fOCO as timer RA count source and timer RA underflow as timer RB count source
Timer RC interrupt	Usable in all modes	(Do not use)
USB functions	Usable only in USB RESUME Interrupt	Usable only in USB RESUME Interrupt
$\overline{\text{INT}}$ interrupt	Usable	Usable ($\overline{\text{INT0}}$ to $\overline{\text{INT4}}$ can be used if there is no filter.)
Voltage monitor 1 interrupt	Usable	Usable
Voltage monitor 2 interrupt	Usable	Usable
Oscillation stop detection interrupt	Usable	(Do not use)

Note:
1. Not available in the R8C/3MU Group.

Figure 9.6 shows the Time from Wait Mode to First Instruction Execution following Exit after CM30 Bit in CM3 Register is Set to 1 (MCU Enters Wait Mode).
To use a peripheral function interrupt to exit wait mode, set up the following before setting the CM30 bit to 1.
(1) Set the I flag to 0 (maskable interrupt disabled)
(2) Set the interrupt priority level in bits ILVL2 to ILVL0 in the interrupt control registers of the peripheral function interrupts to be used for exiting wait mode. Set bits ILVL2 to ILVL0 of the peripheral function interrupts that are not to be used for exiting wait mode to 000b (interrupt disabled).
(3) Operate the peripheral function to be used for exiting wait mode.

When the MCU exits by a peripheral function interrupt, the time (number of cycles) between interrupt request generation and interrupt routine execution is determined by the settings of the FMSTP bit in the FMR0 register and the VCA20 bit in the VCA2 register, as shown in Figure 9.6.
The clock set by bits CM35, CM36, and CM37 in the CM3 register is used as the CPU clock when the MCU exits wait mode by a peripheral function interrupt. At this time, the CM06 bit in the CM0 register and bits CM16 and CM17 in the CM1 register automatically change.

FMR0 Register / FMSTP Bit	VCA2 Register / VCA20 Bit	Internal Power Stabilization Time (T0)	Time until Flash Memory Activation (T1)	Time until CPU Clock Supply (T2)	Remarks
0 (flash memory operates)	0 (internal power low consumption disabled)	0 μs	Period of system clock × 1 cycle + 60 μs (max.)	Period of CPU clock × 2 cycles	The total of T0 to T2 is the time from wait mode to first instruction execution following exit.
	1 (internal power low consumption enabled)	100 μs (max.)			
1 (flash memory stops)	0 (internal power low consumption disabled	0 μs	Period of system clock × 1 cycle	Same as above	
	1 (internal power low consumption enabled)	100 μs (max.)			

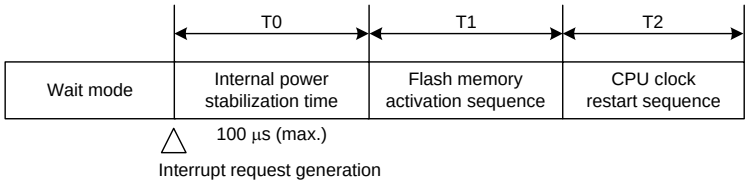


Figure 9.6 Time from Wait Mode to First Instruction Execution following Exit after CM30 Bit in CM3 Register is Set to 1 (MCU Enters Wait Mode)

Figure 9.7 shows the Time from Wait Mode to Interrupt Routine Execution after WAIT instruction is Executed. To use a peripheral function interrupt to exit wait mode, set up the following before executing the WAIT instruction.

(1) Set the interrupt priority level in bits ILVL2 to ILVL0 of the peripheral function interrupts to be used for exiting stop mode. Set bits ILVL2 to ILVL0 of the peripheral function interrupts that are not to be used for exiting stop mode to 000b (interrupt disabled).
(2) Set the I flag to 1.
(3) Operate the peripheral function to be used for exiting stop mode.

When the MCU exits by a peripheral function interrupt, the time (number of cycles) between interrupt request generation and interrupt routine execution is determined by the settings of the FMSTP bit in the FMR0 register and the VCA20 bit in the VCA2 register, as shown in Figure 9.7.
The clock set by bits CM35, CM36, and CM37 in the CM3 register is used as the CPU clock when the MCU exits wait mode by a peripheral function interrupt. At this time, the CM06 bit in the CM0 register and bits CM16 and CM17 in the CM1 register automatically change.

FMR0 Register / FMSTP Bit	VCA2 Register / VCA20 Bit	Internal Power Stabilization Time (T0)	Time until Flash Memory Activation (T1)	Time until CPU Clock Supply (T2)	Time for Interrupt Sequence (T3)	Remarks
0 (flash memory operates)	0 (internal power low consumption disabled)	0 μs	Period of system clock × 1 cycle + 60 μs (max.)	Period of CPU clock × 2 cycles	Period of CPU clock × 20 cycles	The total of T0 to T3 is the time from wait mode to interrupt routine execution.
	1 (internal power low consumption enabled)	100 μs (max.)				
1 (flash memory stops)	0 (internal power low consumption disabled	0 μs	Period of system clock × 1 cycle	Same as above	Same as above	
	1 (internal power low consumption enabled)	100 μs (max.)				

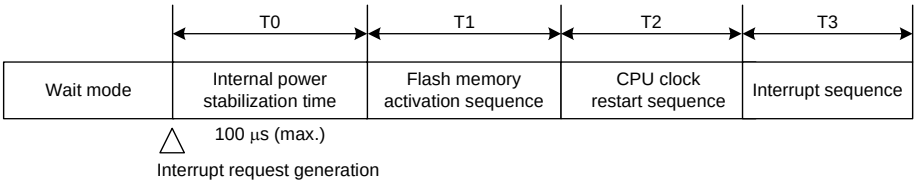


Figure 9.7 Time from Wait Mode to Interrupt Routine Execution after WAIT instruction is Executed

9.7.3 Stop Mode

Since all oscillator circuits except fOCO-WDT stop in stop mode, the CPU and peripheral function clocks stop and the CPU and the peripheral functions operating with these clocks also stop. The least power required to operate the MCU is in stop mode. If the voltage applied to the VCC pin is VRAM or more, the contents of internal RAM is retained.
The peripheral functions clocked by external signals continue operating.
Table 9.7 lists Interrupts to Exit Stop Mode and Usage Conditions.

Table 9.7 Interrupts to Exit Stop Mode and Usage Conditions

Interrupt	Usage Conditions
Key input interrupt	Usable
$\overline{\text{INT0}}$ to $\overline{\text{INT4}}$ interrupt	Usable if there is no filter
Timer RA interrupt	Usable if there is no filter when external pulse is counted in event counter mode
Serial interface interrupt	When external clock selected
USB functions	Usable only in USB RESUME Interrupt
Voltage monitor 1 interrupt	Usable in digital filter disabled mode (VW1C1 bit in VW1C register is set to 1)
Voltage monitor 2 interrupt	Usable in digital filter disabled mode (VW2C1 bit in VW2C register is set to 1)

9.7.3.1 Entering Stop Mode

The MCU enters stop mode when the CM10 bit in the CM1 register is set to 1 (all clocks stop). At the same time, the CM06 bit in the CM0 register is set to 1 (divide-by-8 mode).
To use stop mode, set the following before the MCU enters stop mode:

- Bits OCD1 to OCD0 in the OCD register = 00b
- CM35 bit in CM3 register = 0 (settings of CM06 bit in CM0 register and bits CM16 and CM17 in CM1 register enabled)

Enter stop mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled). Do not enter stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

9.7.3.2 Pin Status in Stop Mode

The I/O port retains the status before the MCU enters stop mode.
However, when the CM13 bit in the CM1 register is set to 1 (XIN-XOUT pin), the XOUT(P4_7) pin is held “H”. When the CM13 bit is set to 0 (input ports P4_6 and P4_7), the P4_7(XOUT pin) is held in an input status.

9.7.3.3 Exiting Stop Mode

The MCU exits stop mode by a reset or peripheral function interrupt.
Figure 9.8 shows the Time from Stop Mode to Interrupt Routine Execution.
To use a peripheral function interrupt to exit stop mode, set up the following before setting the CM10 bit to 1.

(1) Set the interrupt priority level in bits ILVL2 to ILVL0 of the peripheral function interrupts to be used for exiting stop mode. Set bits ILVL2 to ILVL0 of the peripheral function interrupts that are not to be used for exiting stop mode to 000b (interrupt disabled).
(2) Set the I flag to 1.
(3) Operate the peripheral function to be used for exiting stop mode.
When the MCU exits stop mode by a peripheral function interrupt, the interrupt sequence is executed when an interrupt request is generated and the CPU clock supply starts.

The clock used immediately before stop mode divided by 8 is used as the CPU clock when the MCU exits stop mode by a peripheral function interrupt. To enter stop mode, set the CM35 bit in the CM3 register to 0 (settings of CM06 bit in CM0 register and bits CM16 and CM17 in CM1 register enabled)

FMR0 Register / FMSTP Bit	Internal Power Stabilization Time (T0)	Time until Flash Memory Activation (T2)	Time until CPU Clock Supply (T3)	Time for Interrupt Sequence (T4)	Remarks
0 (flash memory operates)	100 µs (max.)	Period of system clock × 1 cycle + 60 µs (max.)	Period of CPU clock × 2 cycles	Period of CPU clock × 20 cycles	The total of T0 to T4 is the time from wait mode to interrupt routine execution.
1 (flash memory stops)	100 µs (max.)	Period of system clock × 1 cycle	Same as above	Same as above	

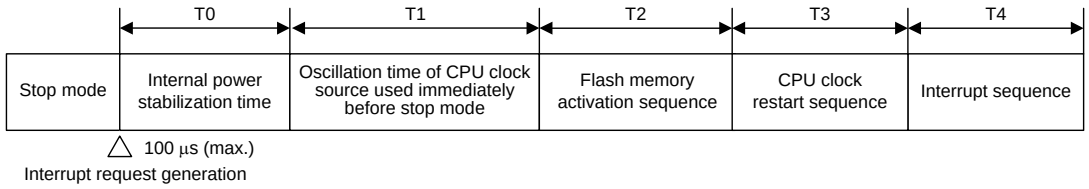


Figure 9.8 Time from Stop Mode to Interrupt Routine Execution

Figure 9.9 shows the State Transitions in Power Control Mode.

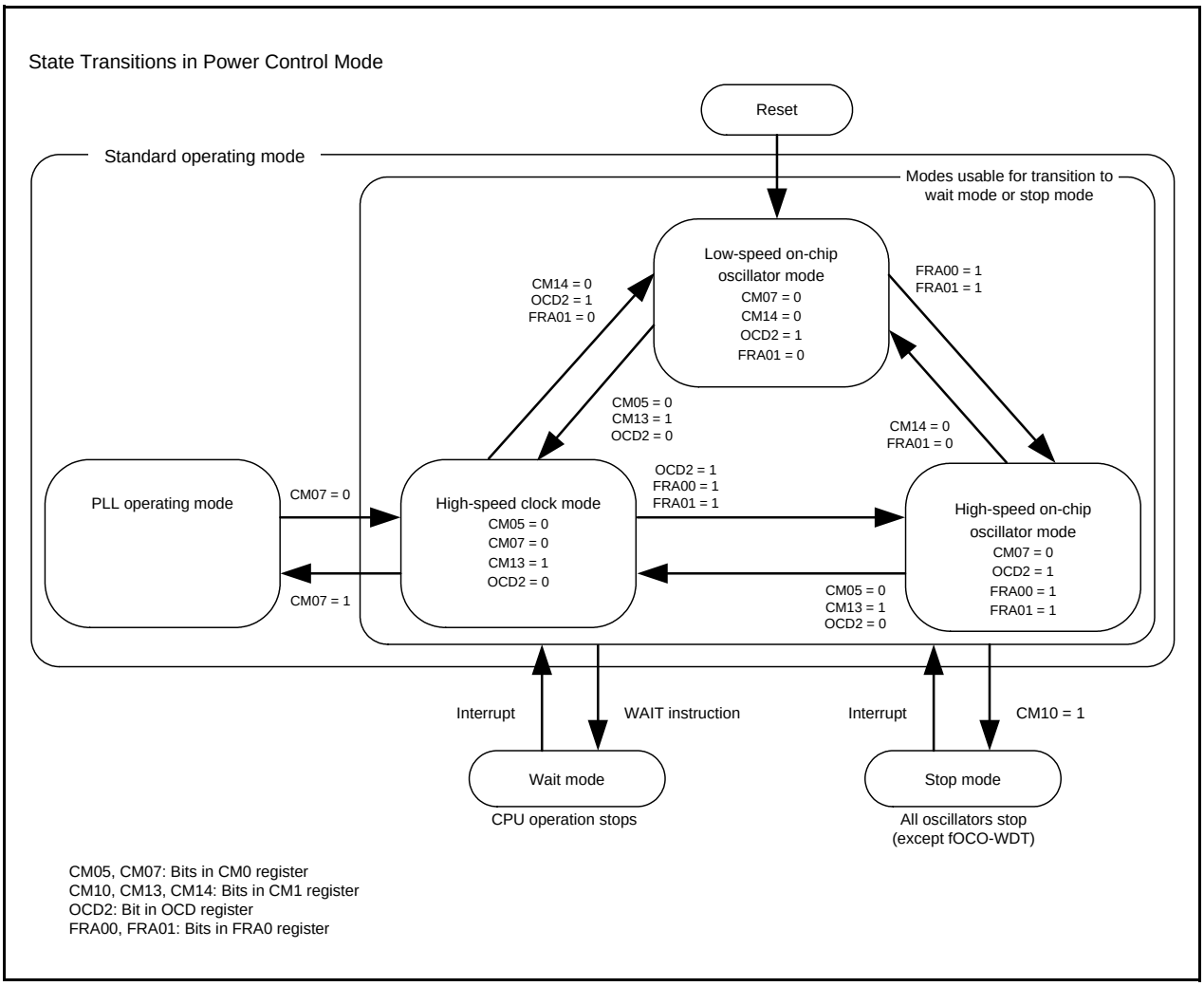


Figure 9.9 State Transitions in Power Control Mode

To start or stop clock oscillations, or to change modes in normal operating mode, follow the instructions below:

- Enter a new mode after the clock for that mode stabilizes completely.
- When stopping a clock, do it after mode transition is completed. Do not stop the clock at the same time as mode transition.
- When changing modes between PLL operating mode and high-speed clock mode, set the CPU clock to divided by 8 or divided by 16 before mode transition.

9.8 Oscillation Stop Detection Function

The oscillation stop detection function detects the stop of the XIN clock oscillating circuit.
The oscillation stop detection function can be enabled and disabled by the OCD0 bit in the OCD register.
Table 9.8 lists the Specifications of Oscillation Stop Detection Function.

When the XIN clock is the CPU clock source and bits OCD1 to OCD0 are set to 11b, the MCU is placed in the following state if the XIN clock stops.

- OCD2 bit in OCD register = 1 (on-chip oscillator clock selected)
- OCD3 bit in OCD register = 1 (XIN clock stops)
- CM14 bit in CM1 register = 0 (low-speed on-chip oscillator oscillates)
- Oscillation stop detection interrupt request is generated

Table 9.8 Specifications of Oscillation Stop Detection Function

Item	Specification
Oscillation stop detection clock and frequency bandwidth	f(XIN) ≥ 2 MHz
Enabled condition for oscillation stop detection function	Bits OCD1 to OCD0 set to 11b
Operation at oscillation stop detection	Oscillation stop detection interrupt generated

9.8.1 How to Use Oscillation Stop Detection Function

- The oscillation stop detection interrupt shares a vector with the voltage monitor 1 interrupt, the voltage monitor 2 interrupt, and the watchdog timer interrupt. To use the oscillation stop detection interrupt and watchdog timer interrupt, the interrupt source needs to be determined.
  Table 9.9 lists the Determination of Interrupt Sources for Oscillation Stop Detection, Watchdog Timer, Voltage Monitor 1, or Voltage Monitor 2 Interrupt. Figure 9.11 shows an Example of Determining Interrupt Sources for Oscillation Stop Detection, Watchdog Timer, Voltage Monitor 1, or Voltage Monitor 2 Interrupt.
- When the XIN clock restarts after oscillation stop, switch the XIN clock to the clock source for the CPU clock and the peripheral functions by a program.
  Figure 9.10 shows the Procedure for Switching from Low-Speed On-Chip Oscillator to XIN Clock when Oscillation Stop is Detected.
- To enter wait mode while the oscillation stop detection function is used, set the CM02 bit to 0 (peripheral function clock does not stop in wait mode).
- Since the oscillation stop detection function is a function for cases where the XIN clock is stopped by an external cause, set bits OCD1 to OCD0 to 00b to stop or start the XIN clock by a program (select stop mode or change the CM05 bit).
- This function cannot be used when the XIN clock frequency is below 2 MHz. In this case, set bits OCD1 to OCD0 to 00b.
- To use the low-speed on-chip oscillator clock as the clock source for the CPU clock and the peripheral functions after detecting the oscillation stop, set the FRA01 bit in the FRA0 register to 0 (low-speed on-chip oscillator selected) and bits OCD1 to OCD0 to 11b.
  To use the high-speed on-chip oscillator clock as the clock source for the CPU clock and the peripheral functions after detecting the oscillation stop, first set the FRA00 bit to 1 (high-speed on-chip oscillator oscillates) and the FRA01 bit to 1 (high-speed on-chip oscillator selected). Then set bits OCD1 to OCD0 to 11b.

Table 9.9 Determination of Interrupt Sources for Oscillation Stop Detection, Watchdog Timer, Voltage Monitor 1, or Voltage Monitor 2 Interrupt

Generated Interrupt Source	Bit Indicating Interrupt Source
Oscillation stop detection ((a) or (b))	(a) OCD3 bit in OCD register = 1
	(b) OCD1 to OCD0 bits in OCD register = 11b and OCD2 bit = 1
Watchdog timer	VW2C3 bit in VW2C register = 1
Voltage monitor 1	VW1C2 bit in VW1C register = 1
Voltage monitor 2	VW2C2 bit in VW2C register = 1

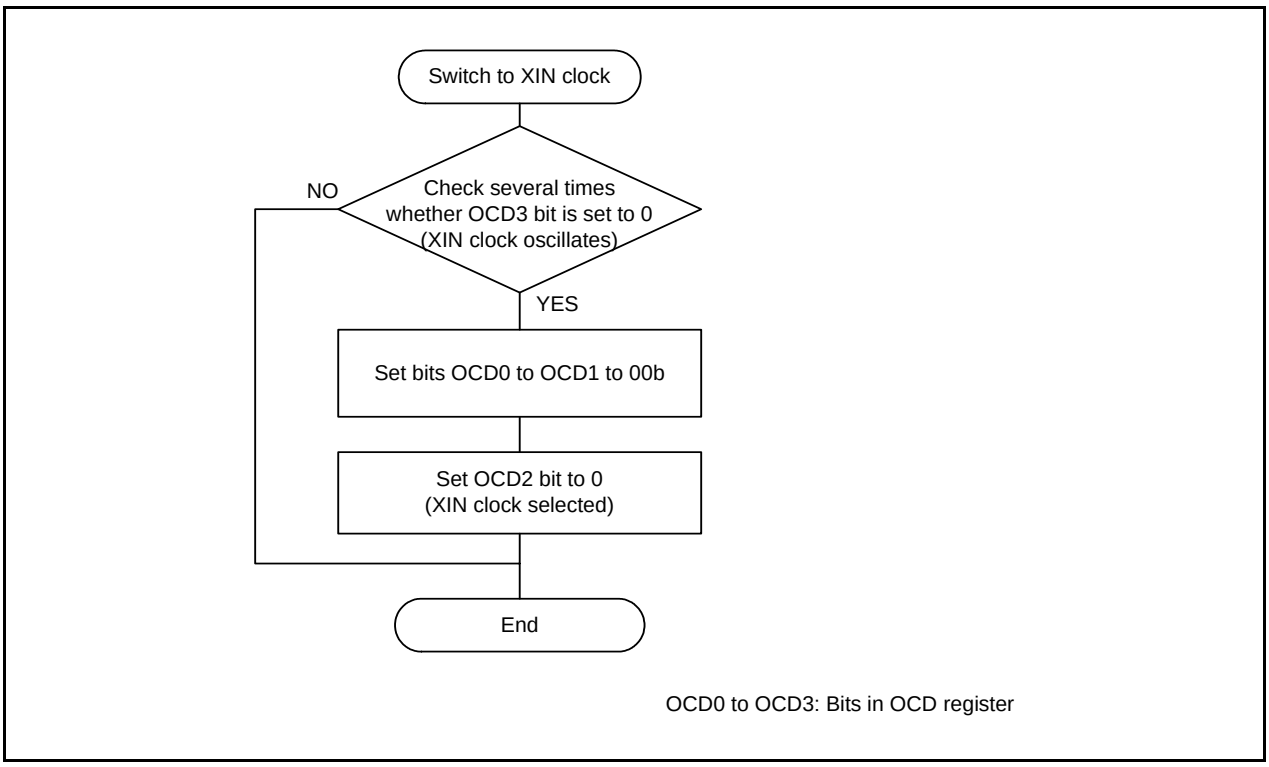


Figure 9.10 Procedure for Switching from Low-Speed On-Chip Oscillator to XIN Clock when Oscillation Stop is Detected

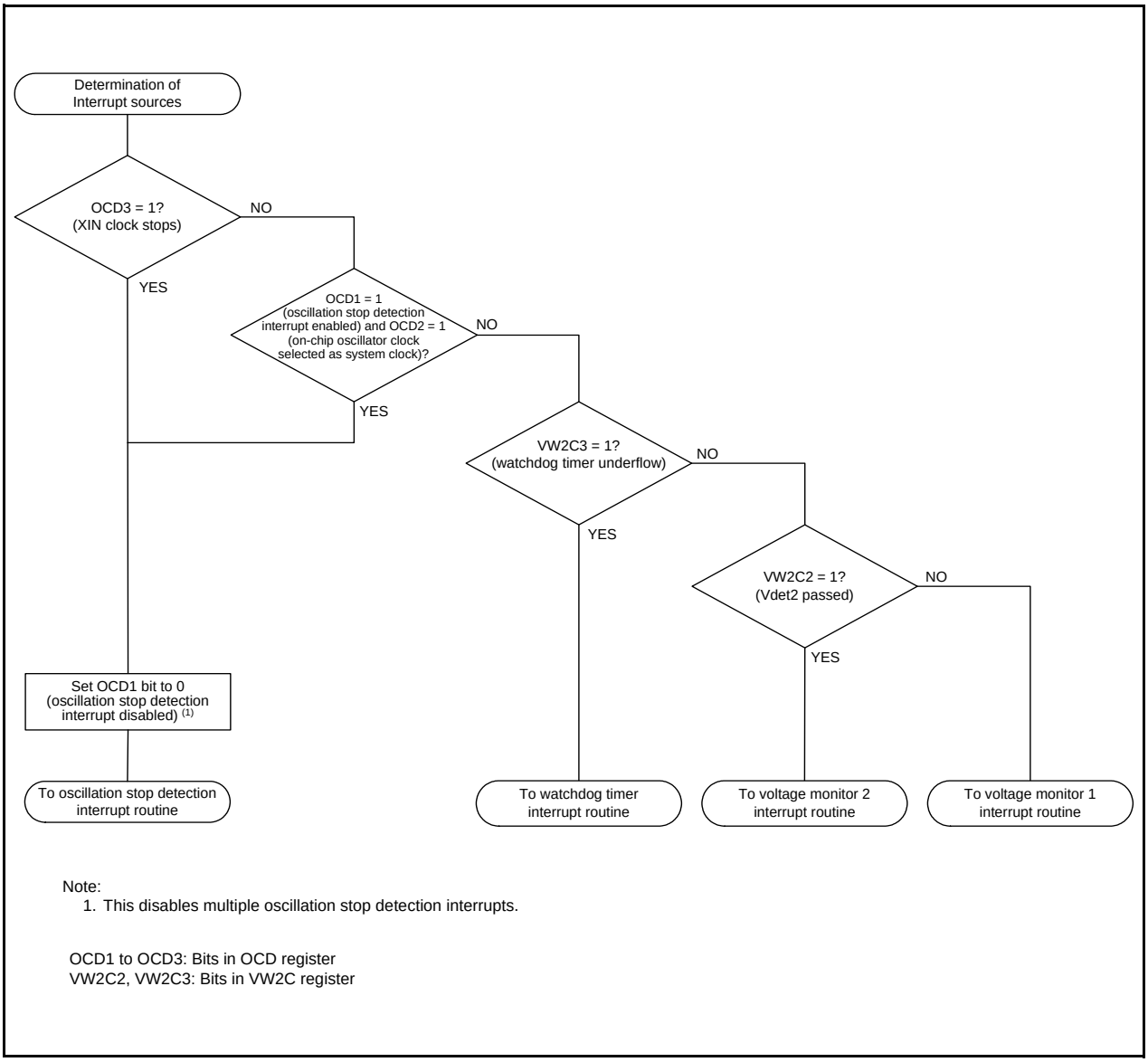


Figure 9.11 Example of Determining Interrupt Sources for Oscillation Stop Detection, Watchdog Timer, Voltage Monitor 1, or Voltage Monitor 2 Interrupt

9.9 Notes on Clock Generation Circuit

9.9.1 Stop Mode

To enter stop mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) and then the CM10 bit in the CM1 register to 1 (stop mode). An instruction queue pre-reads 4 bytes from the instruction which sets the CM10 bit to 1 (stop mode) and the program stops.
Insert at least four NOP instructions following the JMP.B instruction after the instruction which sets the CM10 bit to 1.

• Program example to enter stop mode

```
        BCLR    1, FMR0     ; CPU rewrite mode disabled
        BCLR    7, FMR2     ; Low-current-consumption read mode disabled
        BSET    0, PRCR     ; Writing to CM1 register enabled
        FSET    I           ; Enable interrupt
        BSET    0, CM1      ; Stop mode
        JMP.B   LABEL_001
LABEL_001:
        NOP
        NOP
        NOP
        NOP
```

9.9.2 Wait Mode

To enter wait mode by setting the CM30 bit to 1, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) before setting the CM30 bit to 1.
To enter wait mode with the WAIT instruction, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) and then execute the WAIT instruction. An instruction queue pre-reads 4 bytes from the instruction to set the CM30 bit to 1 (MCU enters wait mode) or the WAIT instruction, and then the program stops. Insert at least four NOP instructions after the instruction to set the CM30 bit to 1 (MCU enters wait mode) or the WAIT instruction.

• Program example to execute the WAIT instruction

```
        BCLR    1, FMR0     ; CPU rewrite mode disabled
        BCLR    7, FMR2     ; Low-current-consumption read mode disabled
        FSET    I           ; Enable interrupt
        WAIT                ; Wait mode
        NOP
        NOP
        NOP
        NOP
```

• Program example to execute the instruction to set the CM30 bit to 1

```
        BCLR    1, FMR0     ; CPU rewrite mode disabled
        BCLR    7, FMR2     ; Low-current-consumption read mode disabled
        BSET    0, PRCR     ; Writing to CM3 register enabled
        FCLR    I           ; Interrupt disabled
        BSET    0, CM3      ; Wait mode
        NOP
        NOP
        NOP
        NOP
        BCLR    0, PRCR     ; Writing to CM3 register disabled
        FSET    I           ; Interrupt enabled
```

9.9.3 Oscillation Stop Detection Function

Since the oscillation stop detection function cannot be used if the XIN clock frequency is below 2 MHz, set bits OCD1 to OCD0 to 00b. In addition, the OCD3 bit cannot be used to confirm whether the XIN clock oscillation is stable.

9.9.4 Oscillation Circuit Constants

Consult the oscillator manufacturer to determine the optimal oscillation circuit constants for the user system.

10. Protection

The protection function protects important registers from being easily overwritten if a program runs out of control. The registers protected by the PRCR register are as follows:

- Registers protected by PRC0 bit: Registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3
- Registers protected by PRC1 bit: Registers PM0 and PM1
- Registers protected by PRC2 bit: PD0 register
- Registers protected by PRC3 bit: Registers OCVREFCR (1), VCA2, VD1LS, VW0C, VW1C, and VW2C

Note:
1. Not available in the R8C/3MU Group.

10.1 Register

10.1.1 Protect Register (PRCR)

Address 000Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	PRC3	PRC2	PRC1	PRC0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3. 0: Write disabled 1: Write enabled (2)	R/W
b1	PRC1	Protect bit 1	Enables writing to registers PM0 and PM1. 0: Write disabled 1: Write enabled (2)	R/W
b2	PRC2	Protect bit 2	Enables writing to the PD0 register. 0: Write disabled 1: Write enabled (1)	R/W
b3	PRC3	Protect bit 3	Enables writing to registers OCVREFCR (3), VCA2, VD1LS, VW0C, VW1C, and VW2C. 0: Write disabled 1: Write enabled (2)	R/W
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—			
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

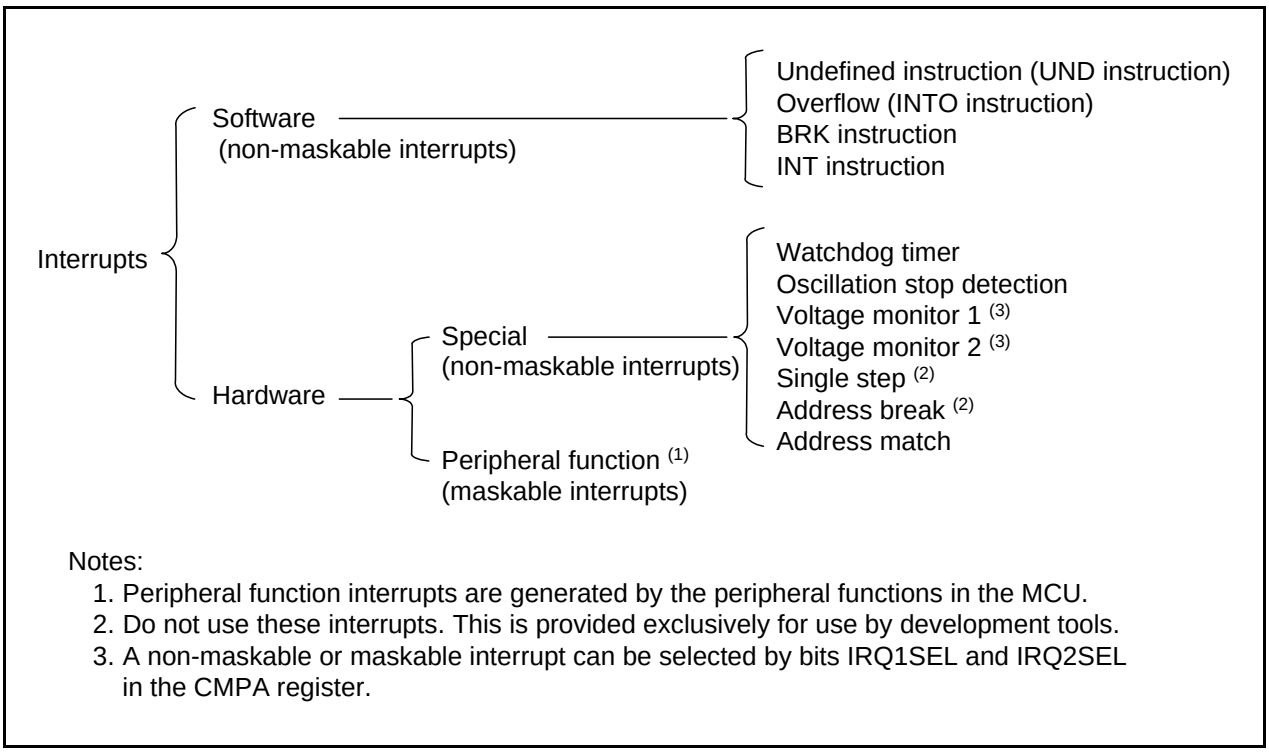
Notes:
1. The PRC2 bit is set to 0 after setting it to 1 (write enabled) and writing to the SFR area. Change the register protected by the PRC2 bit with the next instruction after that used to set the PRC2 bit to 1. Do not allow interrupts or DTC activation between the instruction to set to the PRC2 bit to 1 and the next instruction.
2. Bits PRC0, PRC1, and PRC3 are not set to 0 even after setting them to 1 (write enabled) and writing to the SFR areas. Set these bits to 0 by a program.
3. Not available in the R8C/3MU Group.

11. Interrupts

11.1 Overview

11.1.1 Types of Interrupts

Figure 11.1 shows the Types of Interrupts.



Notes:
1. Peripheral function interrupts are generated by the peripheral functions in the MCU.
2. Do not use these interrupts. This is provided exclusively for use by development tools.
3. A non-maskable or maskable interrupt can be selected by bits IRQ1SEL and IRQ2SEL in the CMPA register.

Figure 11.1 Types of Interrupts

- Maskable interrupts: These interrupts are enabled or disabled by the interrupt enable flag (I flag). The interrupt priority **can be changed** based on the interrupt priority level.
- Non-maskable interrupts: These interrupts are not enabled or disabled by the interrupt enable flag (I flag). The interrupt priority **cannot be changed** based on the interrupt priority level.

11.1.2 Software Interrupts

A software interrupt is generated when an instruction is executed. Software interrupts are non-maskable.

11.1.2.1 Undefined Instruction Interrupt

An undefined instruction interrupt is generated when the UND instruction is executed.

11.1.2.2 Overflow Interrupt

An overflow interrupt is generated when the O flag is set to 1 (arithmetic operation overflow) and the INTO instruction is executed. Instructions that set the O flag are as follows:
ABS, ADC, ADCF, ADD, CMP, DIV, DIVU, DIVX, NEG, RMPA, SBB, SHA, and SUB.

11.1.2.3 BRK Interrupt

A BRK interrupt is generated when the BRK instruction is executed.

11.1.2.4 INT Instruction Interrupt

An INT instruction interrupt is generated when the INT instruction is executed. Software interrupt numbers 0 to 63 can be specified with the INT instruction. Because some software interrupt numbers are assigned to peripheral function interrupts, the same interrupt routine as for peripheral function interrupts can be executed by executing the INT instruction.
For software interrupt numbers 0 to 31, the U flag is saved on the stack during instruction execution and the U flag is set to 0 (ISP selected) before the interrupt sequence is executed. The U flag is restored from the stack when returning from the interrupt routine. For software interrupt numbers 32 to 63, the U flag does not change state during instruction execution, and the selected SP is used.

11.1.3 Special Interrupts

Special interrupts are non-maskable.

11.1.3.1 Watchdog Timer Interrupt

A watchdog timer interrupt is generated by the watchdog timer. For details, refer to **14. Watchdog Timer**.

11.1.3.2 Oscillation Stop Detection Interrupt

An oscillation stop detection interrupt is generated by the oscillation stop detection function. For details of the oscillation stop detection function, refer to **9. Clock Generation Circuit**.

11.1.3.3 Voltage Monitor 1 Interrupt

A voltage monitor 1 interrupt is generated by the voltage detection circuit. A non-maskable or maskable interrupt can be selected by IRQ1SEL bit in the CMPA register. For details of the voltage detection circuit, refer to **6. Voltage Detection Circuit**.

11.1.3.4 Voltage Monitor 2 Interrupt

A voltage monitor 2 interrupt is generated by the voltage detection circuit. A non-maskable or maskable interrupt can be selected by IRQ2SEL bit in the CMPA register. For details of the voltage detection circuit, refer to **6. Voltage Detection Circuit**.

11.1.3.5 Single-Step Interrupt, and Address Break Interrupt

Do not use these interrupts. They are provided exclusively for use by development tools.

11.1.3.6 Address Match Interrupt

An address match interrupt is generated immediately before executing an instruction that is stored at an address indicated by registers RMAD0 to RMAD1 if the AIER00 bit in the AIER0 register or the AIER10 bit in the AIER1 register is set to 1 (address match interrupt enabled).
For details of the address match interrupt, refer to **11.6 Address Match Interrupt**.

11.1.4 Peripheral Function Interrupts

A peripheral function interrupt is generated by a peripheral function in the MCU. Peripheral function interrupts are maskable. Refer to **Tables 11.2 and 11.3 Relocatable Vector Tables** for sources of the corresponding peripheral function interrupt. For details of peripheral functions, refer to the descriptions of individual peripheral functions.

11.1.5 Interrupts and Interrupt Vectors

There are 4 bytes in each vector. Set the starting address of an interrupt routine in each interrupt vector. When an interrupt request is acknowledged, the CPU branches to the address set in the corresponding interrupt vector. Figure 11.2 shows an Interrupt Vector.

Figure 11.2 Interrupt Vector

11.1.5.1 Fixed Vector Tables

The fixed vector tables are allocated addresses 0FFDCh to 0FFFFh.
Table 11.1 lists the Fixed Vector Tables. The vector addresses (H) of fixed vectors are used by the ID code check function. For details, refer to **29.3 Functions to Prevent Flash Memory from being Rewritten**.

Table 11.1 Fixed Vector Tables

Interrupt Source	Vector Addresses Address (L) to (H)	Remarks	Reference
Undefined instruction	0FFDCh to 0FFDFh	Interrupt with UND instruction	R8C/Tiny Series Software Manual
Overflow	0FFE0h to 0FFE3h	Interrupt with INTO instruction	
BRK instruction	0FFE4h to 0FFE7h	If the content of address 0FFE6h is FFh, program execution starts from the address shown by the vector in the relocatable vector table.	
Address match	0FFE8h to 0FFEBh		11.6 Address Match Interrupt
Single step (1)	0FFECh to 0FFEFh		
Watchdog timer, Oscillation stop detection, Voltage monitor 1 (2), Voltage monitor 2 (3)	0FFF0h to 0FFF3h		14. Watchdog Timer 9. Clock Generation Circuit 6. Voltage Detection Circuit
Address break (1)	0FFF4h to 0FFF7h		
(Reserved)	0FFF8h to 0FFFBh		
Reset	0FFFCh to 0FFFFh		5. Resets

Notes:
1. Do not use these interrupts. They are provided exclusively for use by development tools.
2. Voltage monitor 1 interrupt is selected when the IRQ1SEL bit in the CMPA register is set to 0 (nonmaskable interrupt).
3. Voltage monitor 2 interrupt is selected when the IRQ2SEL bit in the CMPA register is set to 0 (nonmaskable interrupt).

11.1.5.2 Relocatable Vector Tables

The relocatable vector tables occupy 256 bytes beginning from the starting address set in the INTB register. Tables 11.2 and 11.3 list the Relocatable Vector Tables.

Table 11.2 Relocatable Vector Tables (1)

Interrupt Source	Vector Addresses (1) Address (L) to Address (H)	Software Interrupt Number	Interrupt Control Register	Reference
BRK instruction (3)	+0 to +3 (0000h to 0003h)	0	—	R8C/Tiny Series Software Manual
Flash memory ready	+4 to +7 (0004h to 0007h)	1	FMRDYIC	29. Flash Memory
(Reserved)		2 to 5	—	—
$\overline{\text{INT4}}$	+24 to +27 (0018h to 001Bh)	6	INT4IC	11.4 $\overline{\text{INT}}$ Interrupt
Timer RC	+28 to +31 (001Ch to 001Fh)	7	TRCIC	19. Timer RC
(Reserved)		8	—	—
USB RESUME	+36 to +39 (0024h to0027h)	9	USBRSMIC	26. USB 2.0 Host/Function Module (USB)
(Reserved)		10	—	—
UART2 transmit/NACK2	+44 to +47 (002Ch to 002Fh)	11	S2TIC	21. Serial Interface (UART2)
UART2 receive/ACK2	+48 to +51 (0030h to 0033h)	12	S2RIC	
Key input	+52 to +55 (0034h to 0037h)	13	KUPIC	11.5 Key Input Interrupt
A/D conversion (4)	+56 to +59 (0038h to 003Bh)	14	ADIC	27. A/D Converter
Synchronous serial communication unit/ I^2C bus interface (2)	+60 to +63 (003Ch to 003Fh)	15	SSUIC/IICIC	23. Synchronous Serial Communication Unit (SSU), 24. I^2C bus Interface
(Reserved)		16	—	—
UART0 transmit	+68 to +71 (0044h to 0047h)	17	S0TIC	20. Serial Interface (UARTi (i = 0, 1, 3))
UART0 receive	+72 to +75 (0048h to 004Bh)	18	S0RIC	
UART1 transmit	+76 to +79 (004Ch to 004Fh)	19	S1TIC	
UART1 receive	+80 to +83 (0050h to 0053h)	20	S1RIC	
$\overline{\text{INT2}}$	+84 to +87 (0054h to 0057h)	21	INT2IC	11.4 $\overline{\text{INT}}$ Interrupt
Timer RA	+88 to +91 (0058h to 005Bh)	22	TRAIC	17. Timer RA
(Reserved)		23	—	—
Timer RB	+96 to +99 (0060h to 0063h)	24	TRBIC	18. Timer RB
$\overline{\text{INT1}}$	+100 to +103 (0064h to 0067h)	25	INT1IC	11.4 $\overline{\text{INT}}$ Interrupt
$\overline{\text{INT3}}$	+104 to +107 (0068h to 006Bh)	26	INT3IC	
(Reserved)		27	—	—
(Reserved)		28	—	
$\overline{\text{INT0}}$	+116 to +119 (0074h to 0077h)	29	INT0IC	11.4 $\overline{\text{INT}}$ Interrupt
UART2 bus collision detection	+120 to +123 (0078h to 007Bh)	30	U2BCNIC	21. Serial Interface (UART2)
(Reserved)		31	—	—
Software (3)	+128 to +131 (0080h to 0083h) to +164 to +167 (00A4h to 00A7h)	32 to 41	—	R8C/Tiny Series Software Manual
(Reserved)		42	—	—
USB INT	+172 to +175 (00ACh to 00AFh)	43	USBINTIC	26. USB 2.0 Host/Function Module (USB)

Notes:
1. These addresses are relative to those in the INTB register.
2. Selectable by the IICSEL bit in the SSUIICSR register.
3. These interrupts are not disabled by the I flag.
4. Not available in the R8C/3MU Group.

Table 11.3 Relocatable Vector Tables (2)

Interrupt Source	Vector Addresses (1) Address (L) to Address (H)	Software Interrupt Number	Interrupt Control Register	Reference
UART3 receive	+176 to +179 (00B0h to 00B3h)	44	S3RIC	20. Serial Interface (UARTi (i = 0, 1, 3))
UART3 transmit	+180 to +183 (00B4h to 00B7h)	45	S3TIC	
(Reserved)		46 to 49	—	—
Voltage monitor 1 (2)	+200 to +203 (00C8h to 00CBh)	50	VCMP1IC	6. Voltage Detection Circuit
Voltage monitor 2 (3)	+204 to +207 (00CCh to 00CFh)	51	VCMP2IC	
(Reserved)		52 to 55	—	—
Software (1)	+224 to +227 (00E0h to 00E3h) to +252 to +255 (00FCh to 00FFh)	56 to 63	—	R8C/Tiny Series Software Manual

Note:
1. These interrupts are not disabled by the I flag.
2. Voltage monitor 1 interrupt is selected when the IRQ1SEL bit in the CMPA register is set to 1 (maskable interrupt).
3. Voltage monitor 2 interrupt is selected when the IRQ2SEL bit in the CMPA register is set to 1 (maskable interrupt).

11.2 Registers

11.2.1 Interrupt Control Register (USBRSMIC, S2TIC, S2RIC, KUPIC, ADIC (2) , S0TIC, S0RIC, S1TIC, S1RIC, TRAIC, TRBIC, U2BCNIC, USBINTIC, S3RIC, S3TIC, VCMP1IC, VCMP2IC)

Address 0049h (USBRSMIC), 004Bh (S2TIC), 004Ch (S2RIC), 004Dh (KUPIC), 004Eh (ADIC) (2), 0051h (S0TIC), 0052h (S0RIC), 0053h (S1TIC), 0054h (S1RIC), 0056h (TRAIC), 0058h (TRBIC), 005Eh (U2BCNIC), 006Bh (USBINTIC), 006Ch (S3RIC), 006Dh (S3TIC), 072h (VCMP1IC), 0073h (VCMP2IC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	IR	ILVL2	ILVL1	ILVL0
After Reset	X	X	X	X	X	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled) 0 0 1: Level 1 0 1 0: Level 2 0 1 1: Level 3 1 0 0: Level 4 1 0 1: Level 5 1 1 0: Level 6 1 1 1: Level 7	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested 1: Interrupt requested	R/W (1)
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b5	—			
b6	—			
b7	—			

Notes:
1. Only 0 can be written to the IR bit. (Do not write 1 to this bit.)
2. Not available in the R8C/3MU Group.

Rewrite the interrupt control register when an interrupt request corresponding to the register is not generated. Refer to **11.8.5 Rewriting Interrupt Control Register**.

11.2.2 Interrupt Control Register (FMRDYIC, TRCIC, SSUIC/IICIC)

Address 0041h (FMRDYIC), 0047h (TRCIC), 004Fh (SSUIC/IICIC (1))

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	IR	ILVL2	ILVL1	ILVL0
After Reset	X	X	X	X	X	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled) 0 0 1: Level 1 0 1 0: Level 2 0 1 1: Level 3 1 0 0: Level 4 1 0 1: Level 5 1 1 0: Level 6 1 1 1: Level 7	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested 1: Interrupt requested	R
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b5	—			
b6	—			
b7	—			

Note:
1. Selectable by the IICSEL bit in the SSUIICSR register.

Rewrite the interrupt control register when an interrupt request corresponding to the register is not generated. Refer to **11.8.5 Rewriting Interrupt Control Register**.

11.2.3 INTi Interrupt Control Register (INTiIC) (i = 0 to 4)

Address 0046h (INT4IC), 0055h (INT2IC), 0059h (INT1IC), 005Ah (INT3IC), 005Dh (INT0IC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	POL	IR	ILVL2	ILVL1	ILVL0
After Reset	X	X	0	0	X	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled) 0 0 1: Level 1 0 1 0: Level 2 0 1 1: Level 3 1 0 0: Level 4 1 0 1: Level 5 1 1 0: Level 6 1 1 1: Level 7	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested 1: Interrupt requested	R/W (1)
b4	POL	Polarity switch bit (3)	0: Falling edge selected 1: Rising edge selected (2)	R/W
b5	—	Reserved bit	Set to 0.	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b7	—			

Notes:
1. Only 0 can be written to the IR bit. (Do not write 1 to this bit.)
2. If the INTiPL bit in the INTEN register is set to 1 (both edges), set the POL bit to 0 (falling edge selected).
3. The IR bit may be set to 1 (interrupt requested) when the POL bit is rewritten.
   Refer to **11.8.4 Changing Interrupt Sources**.

Rewrite the interrupt control register when an interrupt request corresponding to the register is not generated.
Refer to **11.8.5 Rewriting Interrupt Control Register**.

11.3 Interrupt Control

The following describes enabling and disabling maskable interrupts and setting the acknowledgement priority. This description does not apply to non-maskable interrupts.
Use the I flag in the FLG register, IPL, and bits ILVL2 to ILVL0 in the corresponding interrupt control register to enable or disable a maskable interrupt. Whether an interrupt is requested or not is indicated by the IR bit in the corresponding interrupt control register.

11.3.1 I Flag

The I flag enables or disables maskable interrupts. Setting the I flag to 1 (enabled) enables maskable interrupts. Setting the I flag to 0 (disabled) disables all maskable interrupts.

11.3.2 IR Bit

The IR bit is set to 1 (interrupt requested) when an interrupt request is generated. After the interrupt request is acknowledged and the CPU branches to the corresponding interrupt vector, the IR bit is set to 0 (no interrupt requested).
The IR bit can be set to 0 by a program. Do not write 1 to this bit.
However, the IR bit operations of the timer RC interrupt, the synchronous serial communication unit interrupt the I^2C bus interface interrupt, and the flash memory interrupt are different. Refer to **11.7 Timer RC Interrupt, Synchronous Serial Communication Unit Interrupt, I^2C bus Interface Interrupt, and Flash Memory Interrupt (Interrupts with Multiple Interrupt Request Sources)**.

11.3.3 Bits ILVL2 to ILVL0, IPL

Interrupt priority levels can be set using bits ILVL2 to ILVL0.
Table 11.4 lists the Settings of Interrupt Priority Levels and Table 11.5 lists the Interrupt Priority Levels Enabled by IPL.
The following are the conditions when an interrupt is acknowledged:

- I flag = 1
- IR bit = 1
- Interrupt priority level > IPL

The I flag, IR bit, bits ILVL2 to ILVL0, and IPL are independent of each other. They do not affect one another.

Table 11.4 Settings of Interrupt Priority Levels

Bits ILVL2 to ILVL0	Interrupt Priority Level	Priority
000b	Level 0 (interrupt disabled)	—
001b	Level 1	Low
010b	Level 2	↓
011b	Level 3	↓
100b	Level 4	↓
101b	Level 5	↓
110b	Level 6	↓
111b	Level 7	High

Table 11.5 Interrupt Priority Levels Enabled by IPL

IPL	Enabled Interrupt Priority Level
000b	Interrupt level 1 and above
001b	Interrupt level 2 and above
010b	Interrupt level 3 and above
011b	Interrupt level 4 and above
100b	Interrupt level 5 and above
101b	Interrupt level 6 and above
110b	Interrupt level 7 and above
111b	All maskable interrupts are disabled

11.3.4 Interrupt Sequence

The following describes an interrupt sequence which is performed from when an interrupt request is acknowledged until the interrupt routine is executed.
When an interrupt request is generated while an instruction is being executed, the CPU determines its interrupt priority level after the instruction is completed. The CPU starts the interrupt sequence from the following cycle. However, for the SMOVB, SMOVF, SSTR, or RMPA instruction, if an interrupt request is generated while the instruction is being executed, the MCU suspends the instruction to start the interrupt sequence. The interrupt sequence is performed as indicated below.
Figure 11.3 shows the Time Required for Executing Interrupt Sequence.

(1) The CPU obtains interrupt information (interrupt number and interrupt request level) by reading address 00000h. The IR bit for the corresponding interrupt is set to 0 (no interrupt requested). (2)
(2) The FLG register is saved to a temporary register (1) in the CPU immediately before entering the interrupt sequence.
(3) The I, D and U flags in the FLG register are set as follows:
The I flag is set to 0 (interrupts disabled).
The D flag is set to 0 (single-step interrupt disabled).
The U flag is set to 0 (ISP selected).
However, the U flag does not change state if an INT instruction for software interrupt number 32 to 63 is executed.
(4) The CPU internal temporary register (1) is saved on the stack.
(5) The PC is saved on the stack.
(6) The interrupt priority level of the acknowledged interrupt is set in the IPL.
(7) The starting address of the interrupt routine set in the interrupt vector is stored in the PC.

After the interrupt sequence is completed, instructions are executed from the starting address of the interrupt routine.

Notes:
1. These registers cannot be accessed by the user.
2. Refer to **11.7 Timer RC Interrupt, Synchronous Serial Communication Unit Interrupt, I²C bus Interface Interrupt, and Flash Memory Interrupt (Interrupts with Multiple Interrupt Request Sources)** for the IR bit operations of the timer RC Interrupt, Synchronous Serial Communication unit Interrupt, and the I²C bus Interface Interrupt.

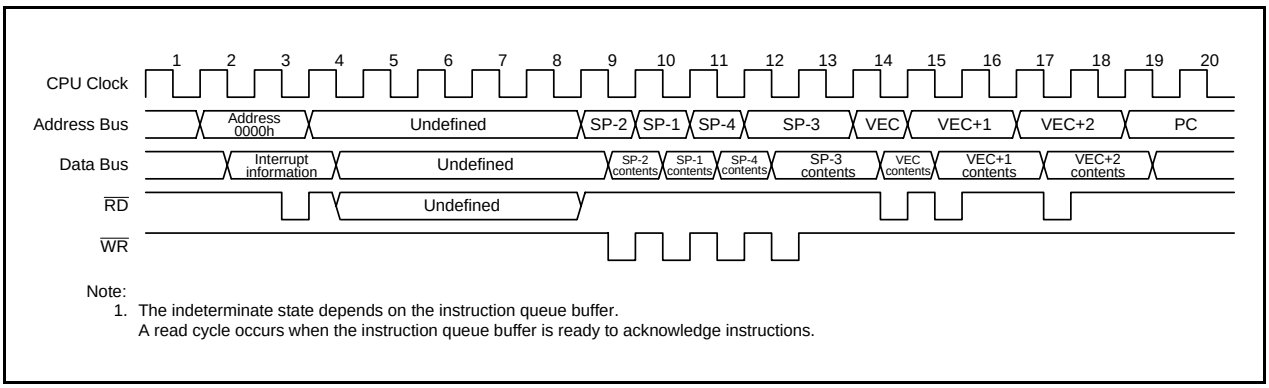
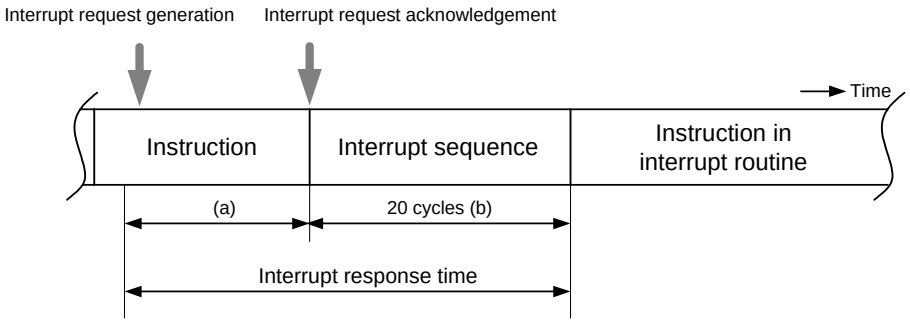


Figure 11.3 Time Required for Executing Interrupt Sequence

11.3.5 Interrupt Response Time

Figure 11.4 shows the Interrupt Response Time. The interrupt response time is the period from when an interrupt request is generated until the first instruction in the interrupt routine is executed. The interrupt response time includes the period from when an interrupt request is generated until the currently executing instruction is completed (refer to (a) in Figure 11.4) and the period required for executing the interrupt sequence (20 cycles, refer to (b) in Figure 11.4).



(a) The period from when an interrupt request is generated until the currently executing instruction is completed. The length of time varies depending on the instruction being executed. The DIVX instruction requires the longest time, 30 cycles (no wait states if the divisor is a register).
(b) 21 cycles for address match and single-step interrupts.

Figure 11.4 Interrupt Response Time

11.3.6 IPL Change when Interrupt Request is Acknowledged

When a maskable interrupt request is acknowledged, the interrupt priority level of the acknowledged interrupt is set in the IPL.
When a software interrupt or special interrupt request is acknowledged, the level listed in Table 11.6 is set in the IPL.
Table 11.6 lists the IPL Value When Software or Special Interrupt is Acknowledged.

Table 11.6 IPL Value When Software or Special Interrupt is Acknowledged

Interrupt Source without Interrupt Priority Level	Value Set in IPL
Watchdog timer, oscillation stop detection, voltage monitor 1, voltage monitor 2, address break	7
Software, address match, single-step	Not changed

11.3.7 Saving Registers

In the interrupt sequence, the FLG register and PC are saved on the stack.
After an extended 16 bits, 4 high-order bits in the PC and 4 high-order (IPL) and 8 low-order bits in the FLG register, are saved on the stack, the 16 low-order bits in the PC are saved.
Figure 11.5 shows the Stack State Before and After Acknowledgement of Interrupt Request.
The other necessary registers should be saved by a program at the beginning of the interrupt routine. The PUSHM instruction can save several registers in the register bank being currently used (1) with a single instruction.

Note:
1. Selectable from registers R0, R1, R2, R3, A0, A1, SB, and FB.

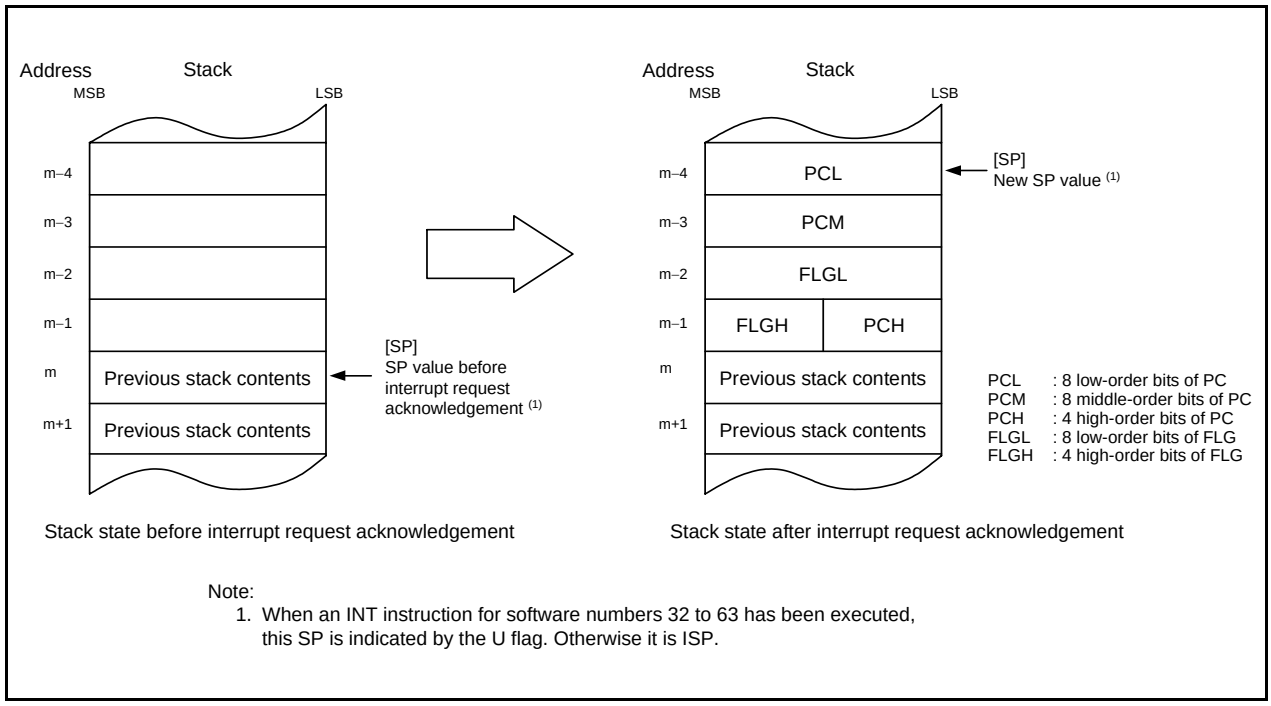
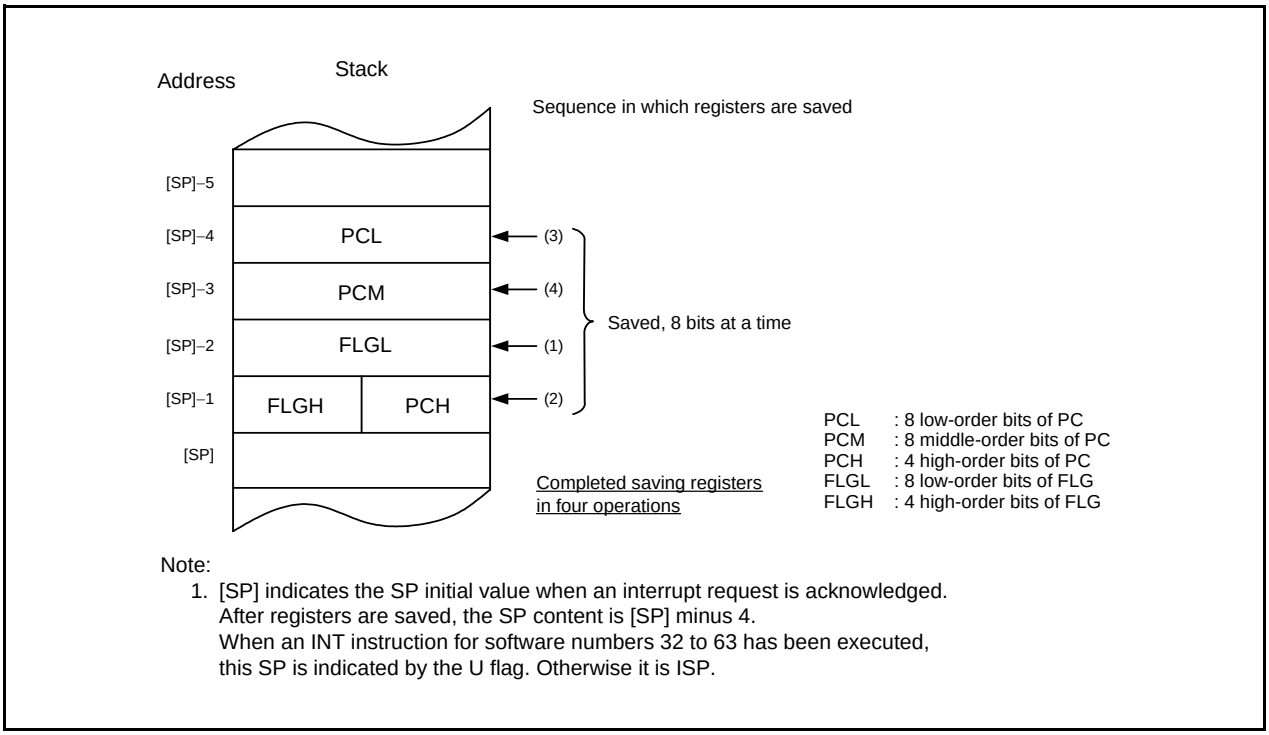


Figure 11.5 Stack State Before and After Acknowledgement of Interrupt Request

The register saving operation, which is performed as part of the interrupt sequence, saved in 8 bits at a time in four steps.
Figure 11.6 shows the Register Saving Operation.



Note:
1. [SP] indicates the SP initial value when an interrupt request is acknowledged.
After registers are saved, the SP content is [SP] minus 4.
When an INT instruction for software numbers 32 to 63 has been executed,
this SP is indicated by the U flag. Otherwise it is ISP.

Figure 11.6 Register Saving Operation

11.3.8 Returning from Interrupt Routine

When the REIT instruction is executed at the end of an interrupt routine, the FLG register and PC, which have been saved on the stack, are automatically restored. The program, that was running before the interrupt request was acknowledged, starts running again.

Registers saved by a program in an interrupt routine should be saved using the POPM instruction or a similar instruction before executing the REIT instruction.

11.3.9 Interrupt Priority

If two or more interrupt requests are generated while a single instruction is being executed, the interrupt with the higher priority is acknowledged.

Set bits ILVL2 to ILVL0 to select any priority level for maskable interrupts (peripheral function). However, if two or more maskable interrupts have the same priority level, their interrupt priority is resolved by hardware, with the higher priority interrupts acknowledged.

The priority of watchdog timer and other special interrupts is set by hardware.

Figure 11.7 shows the Hardware Interrupt Priority.

Software interrupts are not affected by the interrupt priority. If an instruction is executed, the MCU executes the interrupt routine.

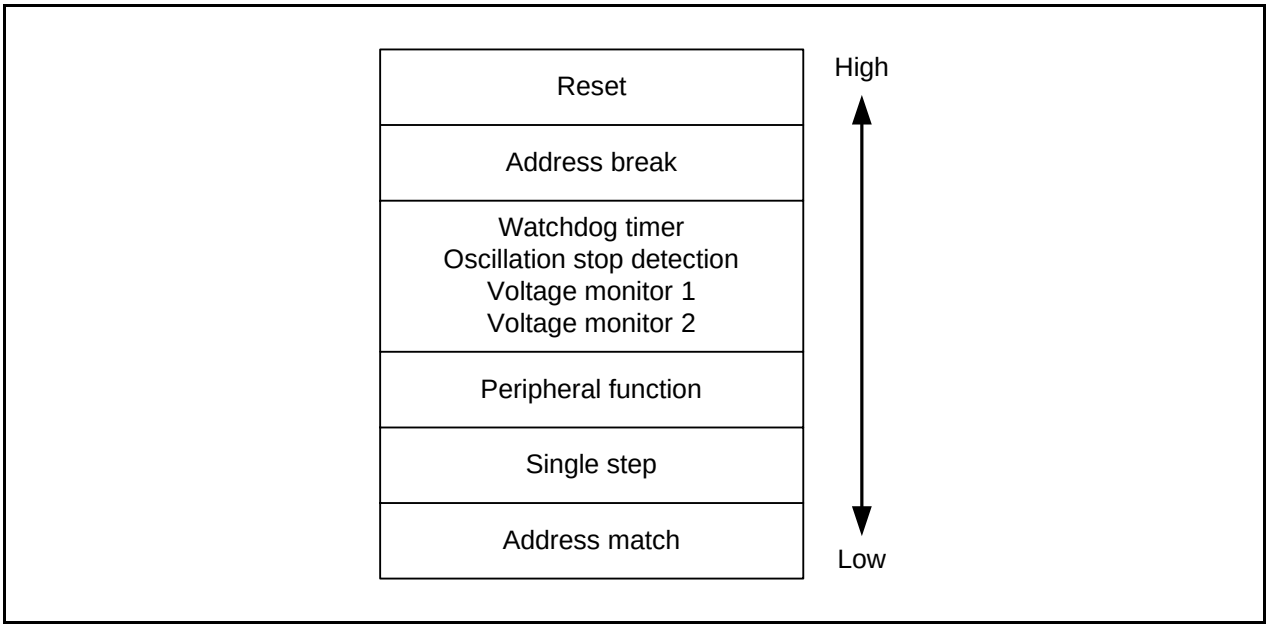


Figure 11.7 Hardware Interrupt Priority

11.3.10 Interrupt Priority Level Selection Circuit

The interrupt priority level selection circuit is used to select the highest priority interrupt.
Figure 11.8 shows the Interrupt Priority Level Selection Circuit.

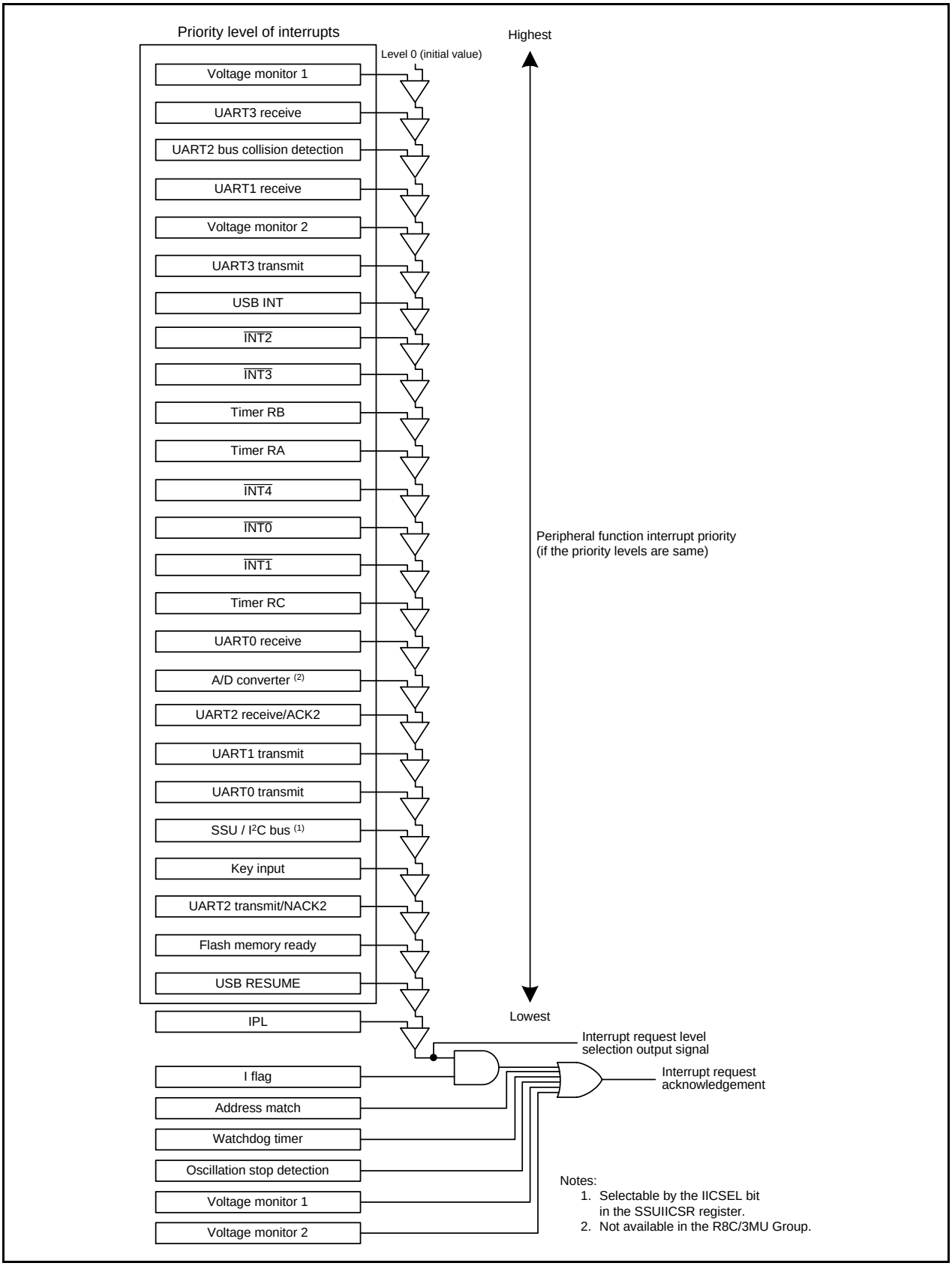


Figure 11.8 Interrupt Priority Level Selection Circuit

11.4 $\overline{\text{INT}}$ Interrupt

11.4.1 $\overline{\text{INTi}}$ Interrupt (i = 0 to 4)

The $\overline{\text{INTi}}$ interrupt is generated by an $\overline{\text{INTi}}$ input. To use the $\overline{\text{INTi}}$ interrupt, set the INTiEN bit in the INTEN register is to 1 (enabled). The edge polarity is selected using the INTiPL bit in the INTEN register and the POL bit in the INTiIC register. The input pins used as the $\overline{\text{INT1}}$ input can be selected.
Also, inputs can be passed through a digital filter with three different sampling clocks.
The $\overline{\text{INT0}}$ pin is shared with the pulse output forced cutoff input of timer RC, and the external trigger input of timer RB. The $\overline{\text{INT2}}$ pin is shared with the event input enabled of timer RA.
Table 11.7 lists the Pin Configuration of $\overline{\text{INT}}$ Interrupt.

Table 11.7 Pin Configuration of $\overline{\text{INT}}$ Interrupt

Pin Name	Assigned Pin	I/O	Function
$\overline{\text{INT0}}$	P4_5	Input	$\overline{\text{INT0}}$ interrupt input, timer RB external trigger input, timer RC pulse output forced cutoff input
$\overline{\text{INT1}}$	P1_5, or P1_7	Input	$\overline{\text{INT1}}$ interrupt input
$\overline{\text{INT2}}$	P6_6	Input	$\overline{\text{INT2}}$ interrupt input, timer RA event input enabled
$\overline{\text{INT3}}$	P6_7	Input	$\overline{\text{INT3}}$ interrupt input
$\overline{\text{INT4}}$	P6_5	Input	$\overline{\text{INT4}}$ interrupt input

11.4.2 INT Interrupt Input Pin Select Register (INTSR)

Address 018Eh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	INT1SEL0	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	INT1SEL0	$\overline{\text{INT1}}$ pin select bit	0: P1_7 assigned 1: P1_5 assigned	R/W
b2	—	Reserved bits	Set to 0.	R/W
b3	—			R/W
b4	—			R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b6	—	Reserved bit	Set to 0.	R/W
b7	—	Reserved bit	Set to 1.	R/W

The INTSR register selects which pin is assigned to the $\overline{\text{INT1}}$ input. To use $\overline{\text{INT1}}$, set this register.
Set the INTSR register before setting the $\overline{\text{INT1}}$ associated registers. Also, do not change the setting values in this register during $\overline{\text{INT1}}$ operation.

11.4.3 External Input Enable Register 0 (INTEN)

Address 01FAh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	INT3PL	INT3EN	INT2PL	INT2EN	INT1PL	INT1EN	INT0PL	INT0EN
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	INT0EN	$\overline{\text{INT0}}$ input enable bit	0: Disabled 1: Enabled	R/W
b1	INT0PL	$\overline{\text{INT0}}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W
b2	INT1EN	$\overline{\text{INT1}}$ input enable bit	0: Disabled 1: Enabled	R/W
b3	INT1PL	$\overline{\text{INT1}}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W
b4	INT2EN	$\overline{\text{INT2}}$ input enable bit	0: Disabled 1: Enabled	R/W
b5	INT2PL	$\overline{\text{INT2}}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W
b6	INT3EN	$\overline{\text{INT3}}$ input enable bit	0: Disabled 1: Enabled	R/W
b7	INT3PL	$\overline{\text{INT3}}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W

Notes:
1. To set the INTiPL bit (i = 0 to 3) to 1 (both edges), set the POL bit in the INTiIC register to 0 (falling edge selected).
2. The IR bit in the INTiIC register may be set to 1 (interrupt requested) if the INTEN register is rewritten. Refer to **11.8.4 Changing Interrupt Sources**.

11.4.4 External Input Enable Register 1 (INTEN1)

Address 01FBh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	INT4PL	INT4EN
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	INT4EN	$\overline{\text{INT4}}$ input enable bit	0: Disabled 1: Enabled	R/W
b1	INT4PL	$\overline{\text{INT4}}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

Notes:
1. To set the INT4PL bit to 1 (both edges), set the POL bit in the INT4IC register to 0 (falling edge selected).
2. The IR bit in the INT4IC register may be set to 1 (interrupt requested) if the INTEN1 register is rewritten. Refer to **11.8.4 Changing Interrupt Sources**.

11.4.5 INT Input Filter Select Register 0 (INTF)

Address 01FCh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	INT3F1	INT3F0	INT2F0	INT2F0	INT1F1	INT1F0	INT0F1	INT01F0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	INT01F0	$\overline{\text{INT0}}$ input filter select bit	b1 b0 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b1	INT0F1			
b2	INT1F0	$\overline{\text{INT1}}$ input filter select bit	b3 b2 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b3	INT1F1			R/W
b4	INT2F0	$\overline{\text{INT2}}$ input filter select bit	b5 b4 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b5	INT2F0			
b6	INT3F0	$\overline{\text{INT3}}$ input filter select bit	b7 b6 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b7	INT3F1			R/W

11.4.6 INT Input Filter Select Register 1 (INTF1)

Address 01FDh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	INT4F1	INT4F0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	INT4F0	$\overline{\text{INT4}}$ input filter select bit	b1 b0 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b1	INT4F1			R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

11.4.7 $\overline{\text{INTi}}$ Input Filter (i = 0 to 4)

The $\overline{\text{INTi}}$ input contains a digital filter. The sampling clock is selected using bits INTiF1 and INTiF0 in registers INTF and INTF1. The $\overline{\text{INTi}}$ level is sampled every sampling clock cycle and if the sampled input level matches three times, the IR bit in the INTiIC register is set to 1 (interrupt requested).
Figure 11.9 shows the $\overline{\text{INTi}}$ Input Filter Configuration. Figure 11.10 shows an Operating Example of $\overline{\text{INTi}}$ Input Filter.

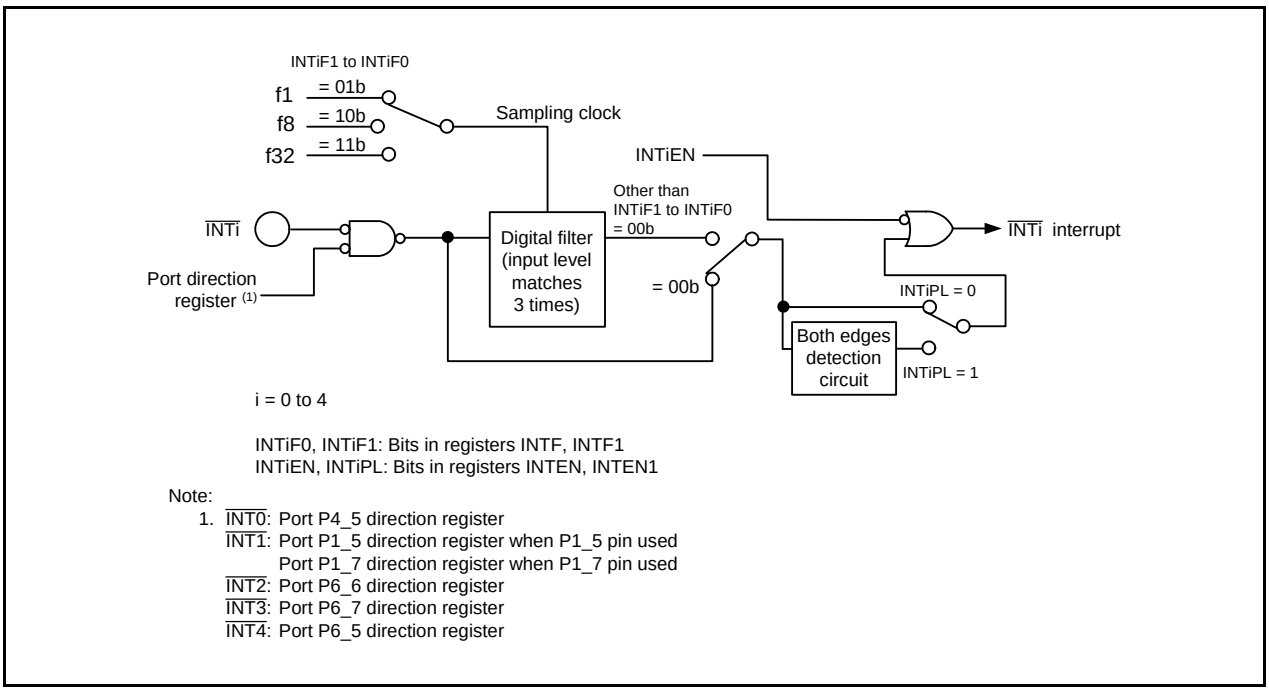


Figure 11.9 $\overline{\text{INTi}}$ Input Filter Configuration

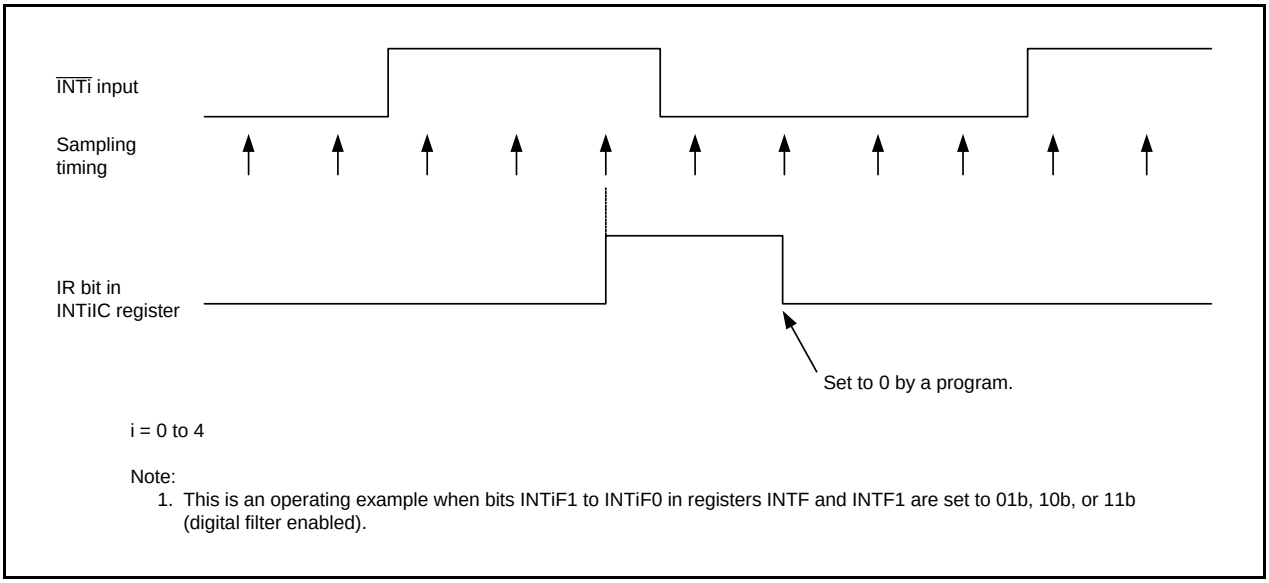


Figure 11.10 Operating Example of $\overline{\text{INTi}}$ Input Filter

11.5 Key Input Interrupt

A key input interrupt request is generated by one of the input edges of pins $\overline{K10}$ to $\overline{K13}$. The key input interrupt can be used as a key-on wake-up function to exit wait or stop mode.

The KIiEN (i = 0 to 3) bit in the KIEN register is be used to select whether or not the pins are used as the $\overline{KIi}$ input. The KIiPL bit in the KIEN register is also be used to select the input polarity.

When inputting "L" to the $\overline{KIi}$ pin, which sets the KIiPL bit to 0 (falling edge), the input to the other pins $\overline{K10}$ to $\overline{K13}$ is not detected as interrupts. When inputting "H" to the $\overline{KIi}$ pin, which sets the KIiPL bit to 1 (rising edge), the input to the other pins $\overline{K10}$ to $\overline{K13}$ is not also detected as interrupts.

Figure 11.11 shows a Block Diagram of Key Input Interrupt. Table 11.8 lists the Pin Configuration of Key Input Interrupt.

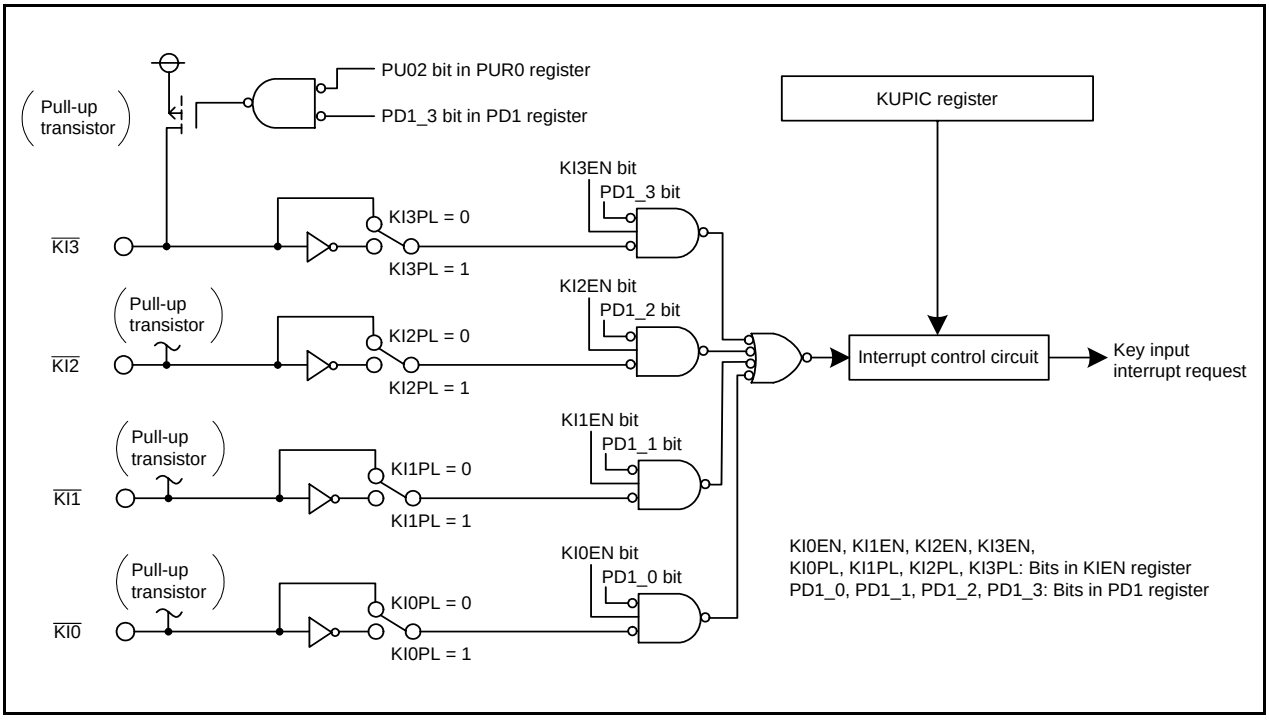


Figure 11.11 Block Diagram of Key Input Interrupt

Table 11.8 Pin Configuration of Key Input Interrupt

Pin Name	I/O	Function
$\overline{KI0}$	Input	$\overline{KI0}$ interrupt input
$\overline{KI1}$	Input	$\overline{KI1}$ interrupt input
$\overline{KI2}$	Input	$\overline{KI2}$ interrupt input
$\overline{KI3}$	Input	$\overline{KI3}$ interrupt input

11.5.1 Key Input Enable Register 0 (KIEN)

Address 01FEh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	KI3PL	KI3EN	KI2PL	KI2EN	KI1PL	KI1EN	KI0PL	KI0EN
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	KI0EN	KI0 input enable bit	0: Disabled 1: Enabled	R/W
b1	KI0PL	KI0 input polarity select bit	0: Falling edge 1: Rising edge	R/W
b2	KI1EN	KI1 input enable bit	0: Disabled 1: Enabled	R/W
b3	KI1PL	KI1 input polarity select bit	0: Falling edge 1: Rising edge	R/W
b4	KI2EN	KI2 input enable bit	0: Disabled 1: Enabled	R/W
b5	KI2PL	KI2 input polarity select bit	0: Falling edge 1: Rising edge	R/W
b6	KI3EN	KI3 input enable bit	0: Disabled 1: Enabled	R/W
b7	KI3PL	KI3 input polarity select bit	0: Falling edge 1: Rising edge	R/W

The IR bit in the KUPIC register may be set to 1 (interrupt requested) when the KIEN register is rewritten. Refer to **11.8.4 Changing Interrupt Sources**.

11.6 Address Match Interrupt

An address match interrupt request is generated immediately before execution of the instruction at the address indicated by the RMADi register (i = 0 or 1). This interrupt is used as a break function by the debugger. When the on-chip debugger is used, do not set an address match interrupt (registers AIER0, AIER1, RMAD0, and RMAD1, and fixed vector tables) in the user system.

Set the starting address of any instruction in the RMADi register (i = 0 or 1). The AIERi0 bit in the AIERi register can be used to select enable or disable the interrupt. The address match interrupt is not affected by the I flag and IPL.

The PC value (refer to **11.3.7 Saving Registers**) which is saved on the stack when an address match interrupt request is acknowledged varies depending on the instruction at the address indicated by the RMADi register. (The appropriate return address is not saved on the stack.) When returning from the address match interrupt, follow one of the following means:

- Rewrite the contents of the stack and use the REIT instruction to return.
- Use an instruction such as POP to restore the stack to its previous state before the interrupt request was acknowledged. Then use a jump instruction to return.

Table 11.9 lists the PC Value Saved on Stack When Address Match Interrupt Request is Acknowledged. Table 11.10 lists the Correspondence Between Address Match Interrupt Sources and Associated Registers.

Table 11.9 PC Value Saved on Stack When Address Match Interrupt Request is Acknowledged

Address Indicated by RMADi Register (i = 0 or 1)	PC Value Saved (1)
• Instruction with 2-byte operation code (2) • Instruction with 1-byte operation code (2) ADD.B:S #IMM8,dest SUB.B:S #IMM8,dest AND.B:S #IMM8,dest OR.B:S #IMM8,dest MOV.B:S #IMM8,dest STZ #IMM8,dest STNZ #IMM8,dest STZX #IMM81,#IMM82,dest CMP.B:S #IMM8,dest PUSHM src POPM dest JMPS #IMM8 JSRS #IMM8 MOV.B:S #IMM,dest (however, dest = A0 or A1)	Address indicated by RMADi register + 2
Instructions other than above	Address indicated by RMADi register + 1

Notes:
1. Refer to **11.3.7 Saving Registers**.
2. Operation code: Refer to the **R8C/Tiny Series Software Manual** (REJ09B0001). **Chapter 4. Instruction Code/Number of Cycles** contains diagrams showing operation code below each syntax. Operation code is shown in the bold frame in the diagrams.

Table 11.10 Correspondence Between Address Match Interrupt Sources and Associated Registers

Address Match Interrupt Source	Address Match Interrupt Enable Bit	Address Match Interrupt Register
Address match interrupt 0	AIER00	RMAD0
Address match interrupt 1	AIER10	RMAD1

11.6.1 Address Match Interrupt Enable Register i (AIERi) (i = 0 or 1)

Address 01C3h (AIER0), 01C7h (AIER1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0	
Symbol	—	—	—	—	—	—	—	AIER00	AIER0 register
After Reset	0	0	0	0	0	0	0	0	

Symbol	—	—	—	—	—	—	—	AIER10	AIER1 register
After Reset	0	0	0	0	0	0	0	0	

Bit	Symbol	Bit Name	Function	R/W
b0	AIERi0	Address match interrupt i enable bit	0: Disabled 1: Enabled	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

11.6.2 Address Match Interrupt Register i (RMADi) (i = 0 or 1)

Address 01C2h to 01C0h (RMAD0), 01C6h to 01C4h (RMAD1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b23	b22	b21	b20	b19	b18	b17	b16
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	X	X	X	X

Bit	Symbol	Function	Setting Range	R/W
b19 to b0	—	Address setting register for address match interrupt	00000h to FFFFFh	R/W
b20	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b21	—			
b22	—			
b23	—			

11.7 Timer RC Interrupt, Synchronous Serial Communication Unit Interrupt, I²C bus Interface Interrupt, and Flash Memory Interrupt (Interrupts with Multiple Interrupt Request Sources)

The timer RC interrupt, synchronous serial communication unit interrupt, I²C bus interface interrupt, and flash memory interrupt each have multiple interrupt request sources. An interrupt request is generated by the logical OR of several interrupt request sources and is reflected in the IR bit in the corresponding interrupt control register. Therefore, each of these peripheral functions has its own interrupt request source status register (status register) and interrupt request source enable register (enable register) to control the generation of interrupt requests (change of the IR bit in the interrupt control register). Table 11.11 lists the Registers Associated with Timer RC Interrupt, Synchronous Serial Communication Unit Interrupt, I²C bus Interface Interrupt, and Flash Memory Interrupt.

Table 11.11 Registers Associated with Timer RC Interrupt, Synchronous Serial Communication Unit Interrupt, I²C bus Interface Interrupt, and Flash Memory Interrupt

Peripheral Function Name	Status Register of Interrupt Request Source	Enable Register of Interrupt Request Source	Interrupt Control Register
Timer RC	TRCSR	TRCIER	TRCIC
Synchronous serial communication unit	SSSR	SSER	SSUIC
I²C bus interface	ICSR	ICIER	IICIC
Flash memory	RDYSTI	RDYSTIE	FMRDYIC
	BSYAEI	BSYAEIE	
		CMDERIE	

As with other maskable interrupts, the timer RC interrupt, synchronous serial communication unit interrupt, I^2C bus interface interrupt, and flash memory interrupt are controlled by the combination of the I flag, IR bit, bits ILVL0 to ILVL2, and IPL. However, since each interrupt source is generated by a combination of multiple interrupt request sources, the following differences from other maskable interrupts apply:

- When bits in the enable register are set to 1 and the corresponding bits in the status register are set to 1 (interrupt enabled), the IR bit in the interrupt control register is set to 1 (interrupt requested).
- When either bits in the status register or the corresponding bits in the enable register, or both are set to 0, the IR bit is set to 0 (no interrupt requested).
  That is, even if the interrupt is not acknowledged after the IR bit is set to 1, the interrupt request will not be retained.
  Also, the IR bit is not set to 0 even if 0 is written to this bit.
- Individual bits in the status register are not automatically set to 0 even if the interrupt is acknowledged.
  The IR bit is also not automatically set to 0 when the interrupt is acknowledged.
  Set individual bits in the status register to 0 in the interrupt routine. Refer to the status register figure for how to set individual bits in the status register to 0.
- When multiple bits in the enable register are set to 1 and other request sources are generated after the IR bit is set to 1, the IR bit remains 1.
- When multiple bits in the enable register are set to 1, use the status register to determine which request source causes an interrupt.

Refer to chapters of the individual peripheral functions (**19. Timer RC**, **23. Synchronous Serial Communication Unit (SSU)**, **24. I^2C bus Interface**, and **29. Flash Memory**) for the status register and enable register.
For the interrupt control register, refer to **11.3 Interrupt Control**.

11.8 Notes on Interrupts

11.8.1 Reading Address 00000h

Do not read address 00000h by a program. When a maskable interrupt request is acknowledged, the CPU reads interrupt information (interrupt number and interrupt request level) from 00000h in the interrupt sequence. At this time, the IR bit for the acknowledged interrupt is set to 0.
If address 00000h is read by a program, the IR bit for the interrupt which has the highest priority among the enabled interrupts is set to 0. This may cause the interrupt to be canceled, or an unexpected interrupt to be generated.

11.8.2 SP Setting

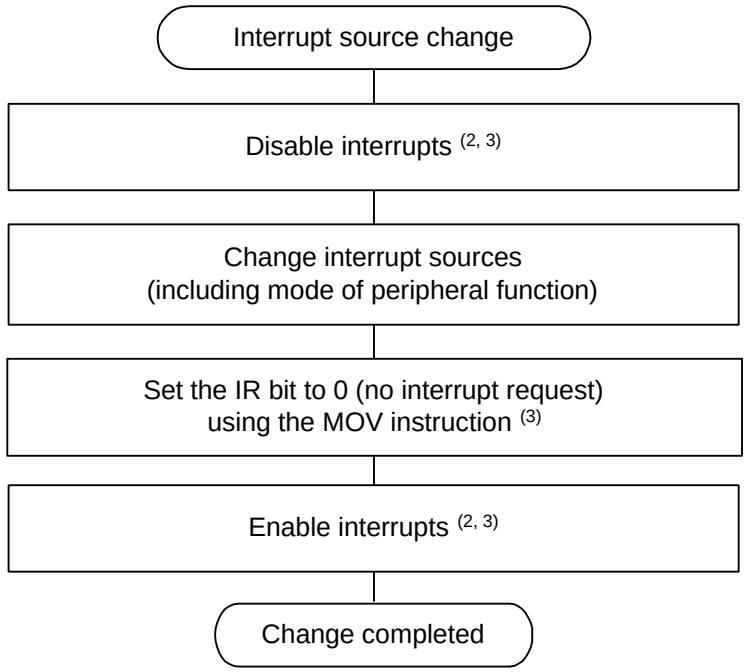
Set a value in the SP before an interrupt is acknowledged. The SP is set to 0000h after a reset. If an interrupt is acknowledged before setting a value in the SP, the program may run out of control.

11.8.3 External Interrupt and Key Input Interrupt

Either the “L” level width or “H” level width shown in the Electrical Characteristics is required for the signal input to pins $\overline{\text{INT0}}$ to $\overline{\text{INT4}}$ and pins $\overline{\text{KI0}}$ to $\overline{\text{KI3}}$, regardless of the CPU clock.
For details, refer to **Table 31.55** (VCC = 5 V), **Table 31.61** (VCC = 3 V), **Table 31.67** (VCC = 2.2 V) **External Interrupt $\overline{\text{INT}}$i (i = 0 to 4) Input, Key Input Interrupt $\overline{\text{KI}}$i (i = 0 to 3)**.

11.8.4 Changing Interrupt Sources

The IR bit in the interrupt control register may be set to 1 (interrupt requested) when the interrupt source changes. To use an interrupt, set the IR bit to 0 (no interrupt requested) after changing interrupt sources.
Changing interrupt sources as referred to here includes all factors that change the source, polarity, or timing of the interrupt assigned to a software interrupt number. Therefore, if a mode change of a peripheral function involves the source, polarity, or timing of an interrupt, set the IR bit to 0 (no interrupt requested) after making these changes. Refer to the descriptions of the individual peripheral functions for related interrupts.
Figure 11.12 shows a Procedure Example for Changing Interrupt Sources.



IR bit: The interrupt control register bit for the interrupt whose source is to be changed

Notes:
1. The above settings must be executed individually. Do not execute two or more settings simultaneously (using one instruction).
2. To prevent interrupt requests from being generated, disable the peripheral function before changing the interrupt source. In this case, use the I flag if all maskable interrupts can be disabled.
   If all maskable interrupts cannot be disabled, use bits ILVL0 to ILVL2 for the interrupt whose source is to be changed.
3. To change the interrupt source to the input with the digital filter used, wait for three or more cycles of the sampling clock of the digital filter before setting the IR bit to 0 (no interrupt request). Refer to **11.8.5 Rewriting Interrupt Control Register** for the instructions to use and related notes.

Figure 11.12 Procedure Example for Changing Interrupt Sources

11.8.5 Rewriting Interrupt Control Register

(a) The contents of the interrupt control register can be rewritten only while no interrupt requests corresponding to that register are generated. If an interrupt request may be generated, disable the interrupt before rewriting the contents of the interrupt control register.

(b) When rewriting the contents of the interrupt control register after disabling the interrupt, be careful to choose appropriate instructions.
Changing any bit other than the IR bit
If an interrupt request corresponding to the register is generated while executing the instruction, the IR bit may not be set to 1 (interrupt requested), and the interrupt may be ignored. If this causes a problem, use one of the following instructions to rewrite the contents of the register: AND, OR, BCLR, and BSET.

Changing the IR bit
Depending on the instruction used, the IR bit may not be set to 0 (no interrupt requested). Use the MOV instruction to set the IR bit to 0.

(c) When using the I flag to disable an interrupt, set the I flag as shown in the sample programs below. Refer to (b) regarding rewriting the contents of interrupt control registers using the sample programs.

Examples 1 to 3 shows how to prevent the I flag from being set to 1 (interrupts enabled) before the contents of the interrupt control register are rewritten for the effects of the internal bus and the instruction queue buffer.

Example 1: Use the NOP instructions to pause program until the interrupt control register is rewritten

```
INT_SWITCH1:
    FCLR    I               ; Disable interrupts
    AND.B   #00H, 0056H     ; Set the TRAIC register to 00h
    NOP                     ;
    NOP
    FSET    I               ; Enable interrupts
```

Example 2: Use a dummy read to delay the FSET instruction

```
INT_SWITCH2:
    FCLR    I               ; Disable interrupts
    AND.B   #00H, 0056H     ; Set the TRAIC register to 00h
    MOV.W   MEM, R0         ; Dummy read
    FSET    I               ; Enable interrupts
```

Example 3: Use the POPC instruction to change the I flag

```
INT_SWITCH3:
    PUSHC   FLG
    FCLR    I               ; Disable interrupts
    AND.B   #00H, 0056H     ; Set the TRAIC register to 00h
    POPC    FLG             ; Enable interrupts
```

12. ID Code Areas

The ID code areas are used to implement a function that prevents the flash memory from being rewritten in standard serial I/O mode. This function prevents the flash memory from being read, rewritten, or erased.

12.1 Overview

The ID code areas are assigned to 0FFDFh, 0FFE3h, 0FFEBh, 0FFEFh, 0FFF3h, 0FFF7h, and 0FFFBh of the respective vector highest-order addresses of the fixed vector table. Figure 12.1 shows the ID Code Areas.

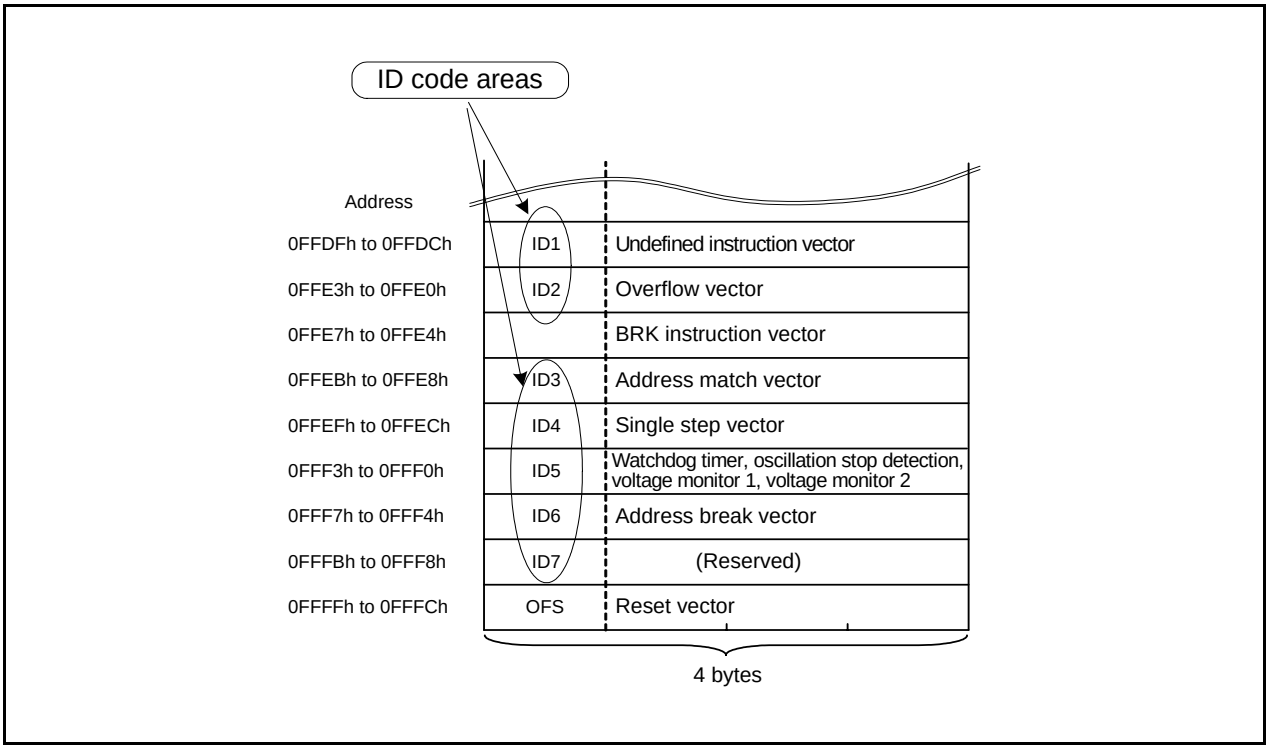


Figure 12.1 ID Code Areas

12.2 Functions

The ID code areas are used in standard serial I/O mode. Unless 3 bytes (addresses 0FFFCh to 0FFFEh) of the reset vector are set to FFFFFFh, the ID codes stored in the ID code areas and the ID codes sent from the serial programmer or the on-chip debugging emulator are checked to see if they match. If the ID codes match, the commands sent from the serial programmer or the on-chip debugging emulator are acknowledged. If the ID codes do not match, the commands are not acknowledged. To use the serial programmer or the on-chip debugging emulator, first write predetermined ID codes to the ID code areas.
If 3 bytes (addresses 0FFFCh to 0FFFEh) of the reset vector are set to FFFFFFh, the ID codes are not checked and all commands are accepted.

The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.

The character sequence of the ASCII codes “ALeRASE” is the reserved word used for the forced erase function. The character sequence of the ASCII codes “Protect” is the reserved word used for the standard serial I/O mode disabled function. Table 12.1 shows the ID Code Reserved Word. The reserved word is a set of reserved characters when all the addresses and data in the ID code storage addresses sequentially match Table 12.1. When the forced erase function or standard serial I/O mode disabled function is not used, use another character sequence of the ASCII codes.

Table 12.1 ID Code Reserved Word

ID Code Storage Address		ID Code Reserved Word (ASCII) (1)	
		ALeRASE	Protect
0FFDFh	ID1	41h (upper-case “A”)	50h (upper-case “P”)
0FFE3h	ID2	4Ch (upper-case “L”)	72h (lower-case “r”)
0FFEBh	ID3	65h (lower-case “e”)	6Fh (lower-case “o”)
0FFEFh	ID4	52h (upper-case “R”)	74h (lower-case “t”)
0FFF3h	ID5	41h (upper-case “A”)	65h (lower-case “e”)
0FFF7h	ID6	53h (upper-case “S”)	63h (lower-case “c”)
0FFFBh	ID7	45h (upper-case “E”)	74h (lower-case “t”)

Note:
1. Reserve word: A set of characters when all the addresses and data in the ID code storage addresses sequentially match Table 12.1.

12.3 Forced Erase Function

This function is used in standard serial I/O mode. When the ID codes sent from the serial programmer or the on-chip debugging emulator are “ALeRASE” in ASCII code, the content of the user ROM area will be erased at once. However, if the contents of the ID code addresses are set to other than “ALeRASE” (other than **Table 12.1 ID Code Reserved Word**) when the ROMCR bit in the OFS register is set to 1 and the ROMCP1 bit is set to 0 (ROM code protect enabled), forced erasure is not executed and the ID codes are checked with the ID code check function. Table 12.2 lists the Conditions and Operations of Forced Erase Function.
Also, when the contents of the ID code addresses are set to “ALeRASE” in ASCII code, if the ID codes sent from the serial programmer or the on-chip debugging emulator are “ALeRASE”, the content of the user ROM area will be erased. If the ID codes sent from the serial programmer are other than “ALeRASE”, the ID codes do not match and no command is acknowledged, thus the user ROM area remains protected.

Table 12.2 Conditions and Operations of Forced Erase Function

Condition			Operation
ID code from serial programmer or the on-chip debugging emulator	ID code in ID code storage address	Bits ROMCP1 and ROMCR in OFS register	
ALeRASE	ALeRASE	—	All erasure of user ROM area (forced erase function)
	Other than ALeRASE (1)	Other than 01b (ROM code protect disabled)	
		01b (ROM code protect enabled)	ID code check (ID code check function)
Other than ALeRASE	ALeRASE	—	ID code check (ID code check function. No ID code match.)
	Other than ALeRASE (1)	—	ID code check (ID code check function)

Note:
1. For “Protect”, refer to **12.4 Standard Serial I/O Mode Disabled Function**.

12.4 Standard Serial I/O Mode Disabled Function

This function is used in standard serial I/O mode. When the I/D codes in the ID code storage addresses are set to the reserved character sequence of the ASCII codes “Protect” (refer to **Table 12.1 ID Code Reserved Word**), communication with the serial programmer or the on-chip debugging emulator is not performed. This does not allow the flash memory to be read, rewritten, or erased using the serial programmer or the on-chip debugging emulator.
Also, if the ID codes are also set to the reserved character sequence of the ASCII codes “Protect” when the ROMCR bit in the OFS register is set to 1 and the ROMCP1 bit is set to 0 (ROM code protect enabled), ROM code protection cannot be disabled using the serial programmer or the on-chip debugging emulator. This prevents the flash memory from being read, rewritten, or erased using the serial programmer, the on-chip debugging emulator, or parallel programmer.

12.5 Notes on ID Code Areas

12.5.1 Setting Example of ID Code Areas

The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. The following shows a setting example.

- To set 55h in all of the ID code areas

```
.org 00FFDCH
.lword dummy | (55000000h)   ; UND
.lword dummy | (55000000h)   ; INTO
.lword dummy                 ; BREAK
.lword dummy | (55000000h)   ; ADDRESS MATCH
.lword dummy | (55000000h)   ; SET SINGLE STEP
.lword dummy | (55000000h)   ; WDT
.lword dummy | (55000000h)   ; ADDRESS BREAK
.lword dummy | (55000000h)   ; RESERVE
```

(Programming formats vary depending on the compiler. Check the compiler manual.)

13. Option Function Select Area

13.1 Overview

The option function select area is used to select the MCU state after a reset, the function to prevent rewriting in parallel I/O mode, or the watchdog timer operation. The reset vector highest-order-address, 0FFFFh and 0FFDBh, are assigned as the option function select area. Figure 13.1 shows the Option Function Select Area.

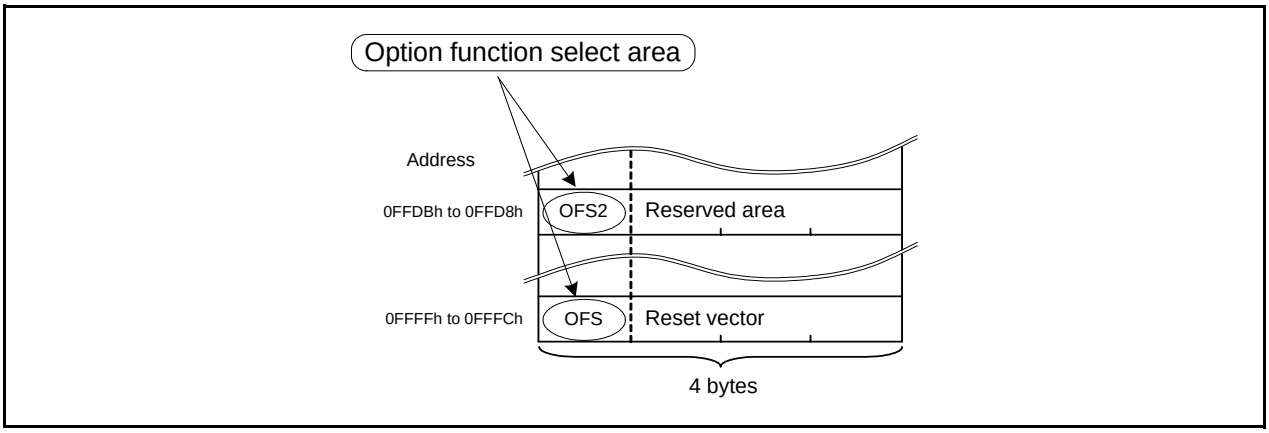


Figure 13.1 Option Function Select Area

13.2 Registers

Registers OFS and OFS2 are used to select the MCU state after a reset, the function to prevent rewriting in parallel I/O mode, or the watchdog timer operation.

13.2.1 Option Function Select Register (OFS)

Address 0FFFFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CSPROINI	LVDAS	VDSEL1	VDSEL0	ROMCP1	ROMCR	—	WDTON
After Reset	User Setting Value (1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTON	Watchdog timer start select bit	0: Watchdog timer automatically starts after reset 1: Watchdog timer is stopped after reset	R/W
b1	—	Reserved bit	Set to 1.	R/W
b2	ROMCR	ROM code protect disable bit	0: ROM code protect disabled 1: ROMCP1 bit enabled	R/W
b3	ROMCP1	ROM code protect bit	0: ROM code protect enabled 1: ROM code protect disabled	R/W
b4	VDSEL0	Voltage detection 0 level select bit (2)	b5 b4 0 0: 3.80 V selected (Vdet0_3) 0 1: 2.85 V selected (Vdet0_2) 1 0: 2.35 V selected (Vdet0_1) 1 1: 1.90 V selected (Vdet0_0)	R/W
b5	VDSEL1			R/W
b6	LVDAS	Voltage detection 0 circuit start bit (3)	0: Voltage monitor 0 reset enabled after reset 1: Voltage monitor 0 reset disabled after reset	R/W
b7	CSPROINI	Count source protection mode after reset select bit	0: Count source protect mode enabled after reset 1: Count source protect mode disabled after reset	R/W

Notes:

1. The OFS register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the OFS register. If the block including the OFS register is erased, the OFS register is set to FFh.
   When blank products are shipped, the OFS register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS register is the value programmed by the user.
2. The same level of the voltage detection 0 level selected by bits VDSEL0 and VDESL1 is set in both functions of voltage monitor 0 reset and power-on reset.
3. To use power-on reset and voltage monitor 0 reset, set the LVDAS bit to 0 (voltage monitor 0 reset enabled after reset).

For a setting example of the OFS register, refer to **13.3.1 Setting Example of Option Function Select Area**.

LVDAS Bit (Voltage Detection 0 Circuit Start Bit)

The Vdet0 voltage to be monitored by the voltage detection 0 circuit is selected by bits VDSEL0 and VDSEL1.

13.2.2 Option Function Select Register 2 (OFS2)

Address 0FFDBh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	WDTRCS1	WDTRCS0	WDTUFS1	WDTUFS0
After Reset	User Settng Value (1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTUFS0	Watchdog timer underflow period set bit	b1 b0 0 0: 03FFh 0 1: 0FFFh 1 0: 1FFFh 1 1: 3FFFh	R/W
b1	WDTUFS1			R/W
b2	WDTRCS0	Watchdog timer refresh acknowledgement period set bit	b3 b2 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100%	R/W
b3	WDTRCS1			R/W
b4	—	Reserved bits	Set to 1.	R/W
b5	—			
b6	—			
b7	—			

Note:

1. The OFS2 register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the OFS2 register. If the block including the OFS2 register is erased, the OFS2 register is set to FFh.
   When blank products are shipped, the OFS2 register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS2 register is the value programmed by the user.

   For a setting example of the OFS2 register, refer to **13.3.1 Setting Example of Option Function Select Area**.

Bits WDTRCS0 and WDTRCS1 (Watchdog Timer Refresh Acknowledgement Period Set Bit)

Assuming that the period from when the watchdog timer starts counting until it underflows is 100%, the refresh acknowledgement period for the watchdog timer can be selected.
For details, refer to **14.3.1.1 Refresh Acknowledgment Period**.

13.3 Notes on Option Function Select Area

13.3.1 Setting Example of Option Function Select Area

The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. The following shows a setting example.

- To set FFh in the OFS register

```
.org 00FFFCH
.lword reset | (0FF000000h)     ; RESET
```

(Programming formats vary depending on the compiler. Check the compiler manual.)

- To set FFh in the OFS2 register

```
.org 00FFDBH
.byte 0FFh
```

(Programming formats vary depending on the compiler. Check the compiler manual.)

14. Watchdog Timer

The watchdog timer is a function that detects when a program is out of control. Use of the watchdog timer is recommended to improve the reliability of the system.

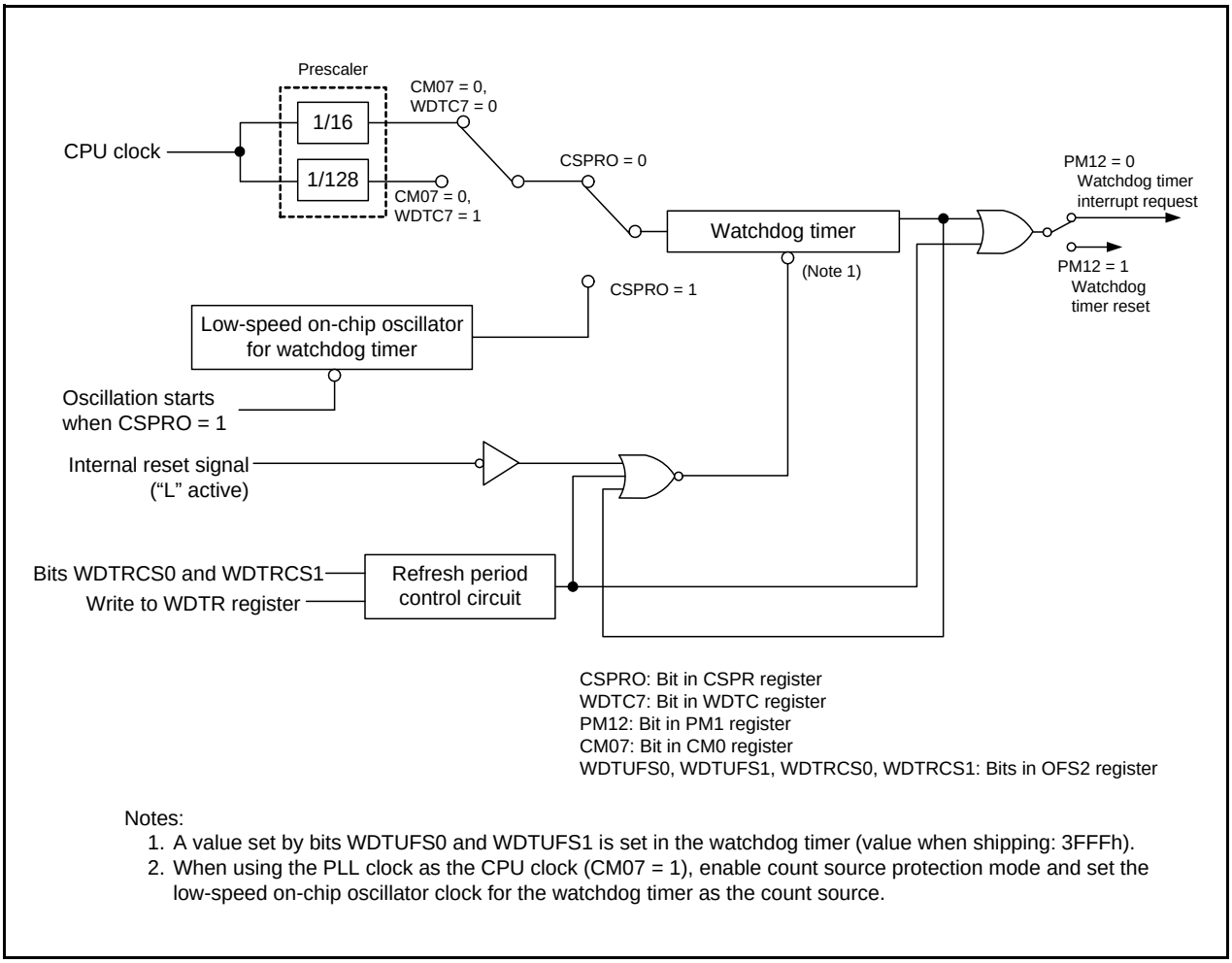
14.1 Overview

The watchdog timer contains a 14-bit counter and allows selection of count source protection mode enable or disable.
Table 14.1 lists the Watchdog Timer Specifications.
Refer to **5.5 Watchdog Timer Reset** for details of the watchdog timer reset.
Figure 14.1 shows a Watchdog Timer Block Diagram.

Table 14.1 Watchdog Timer Specifications

Item	Count Source Protection Mode Disabled	Count Source Protection Mode Enabled (2)
Count source	CPU clock	Low-speed on-chip oscillator clock for the watchdog timer
Count operation	Decrement	
Count start condition	Either of the following can be selected: • After a reset, count starts automatically • Count starts by writing to the WDTS register	
Count stop condition	Stop mode, wait mode	None
Watchdog timer initialization conditions	• Reset • Write 00h and then FFh to the WDTR register (with acknowledgement period setting) (1) • Underflow	
Operations at underflow	Watchdog timer interrupt or watchdog timer reset	Watchdog timer reset
Selectable functions	• Division ratio of the prescaler Selected by the WDTC7 bit in the WDTC register or the CM07 bit in the CM0 register. • Count source protection mode Whether count source protection mode is enabled or disabled after a reset can be selected by the CSPROINI bit in the OFS register (flash memory). If count source protection mode is disabled after a reset, it can be enabled or disabled by the CSPRO bit in the CSPR register (program). • Start or stop of the watchdog timer after a reset Selected by the WDTON bit in the OFS register (flash memory). • Initial value of the watchdog timer Selectable by bits WDTUFS0 and WDTUFS1 in the OFS2 register. • Refresh acknowledgement period for the watchdog timer Selectable by bits WDTRCS0 and WDTRCS1 in the OFS2 register.	

Notes:
1. Write the WDTR register during the count operation of the watchdog timer.
2. When using the PLL clock as the CPU clock (CM07 = 1), enable count source protection mode.



Notes:
1. A value set by bits WDTUFS0 and WDTUFS1 is set in the watchdog timer (value when shipping: 3FFFh).
2. When using the PLL clock as the CPU clock (CM07 = 1), enable count source protection mode and set the low-speed on-chip oscillator clock for the watchdog timer as the count source.

Figure 14.1 Watchdog Timer Block Diagram

14.2 Registers

14.2.1 Processor Mode Register 1 (PM1)

Address 0005h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	PM12	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	PM12	WDT interrupt/reset switch bit	0: Watchdog timer interrupt 1: Watchdog timer reset (1)	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—			
b5	—			
b6	—			
b7	—	Reserved bit	Set to 0.	R/W

Note:
1. The PM12 bit is set to 1 when 1 is written by a program (and remains unchanged even if 0 is written to it). This bit is automatically set to 1 when the CSPRO bit in the CSPR register is set to 1 (count source protection mode enabled).

Set the PRC1 bit in the PRCR register to 1 (write enabled) before rewriting the PM1 register.

14.2.2 Watchdog Timer Reset Register (WDTR)

Address 000Dh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	R/W
b7 to b0	Writing 00h and then FFh to this register initializes the watchdog timer. The initial value of the watchdog timer is specified by bits WDTUFS0 and WDTUF1 in the OFS2 register. (1)	W

Note:
1. Write the WDTR register during the count operation of the watchdog timer.

14.2.3 Watchdog Timer Start Register (WDTS)

Address 000Eh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	R/W
b7 to b0	A write instruction to this register starts the watchdog timer.	W

14.2.4 Watchdog Timer Control Register (WDTC)

Address 000Fh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	WDTC7	—	—	—	—	—	—	—
After Reset	0	0	1	1	1	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	—	The following bits of the watchdog timer can be read. When bits WDTUFS1 to WDTUFS0 in the OFS2 register are 00b (03FFh): b5 to b0 01b (0FFFh): b7 to b2 10b (1FFFh): b8 to b3 11b (3FFFh): b9 to b4		R
b1	—			R
b2	—			R
b3	—			R
b4	—			R
b5	—			R
b6	—	Reserved bit	When read, the content is 0.	R
b7	WDTC7	Prescaler select bit	0: Divided-by-16 1: Divided-by-128	R/W

14.2.5 Count Source Protection Mode Register (CSPR)

Address 001Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CSPRO	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

The above applies when the CSPROINI bit in the OFS register is set to 1.

After Reset	1	0	0	0	0	0	0	0

The above applies when the CSPROINI bit in the OFS register is set to 0.

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	CSPRO	Count source protection mode select bit (1)	0: Count source protection mode disabled 1: Count source protection mode enabled	R/W

Note:
1. To set the CSPRO bit to 1, write 0 and then 1 to it. This bit cannot be set to 0 by a program. Disable interrupts and DTC activation between writing 0 and writing 1.

14.2.6 Option Function Select Register (OFS)

Address 0FFFFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CSPROINI	LVDAS	VDSEL1	VDSEL0	ROMCP1	ROMCR	—	WDTON
After Reset	User Setting Value (1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTON	Watchdog timer start select bit	0: Watchdog timer automatically starts after reset 1: Watchdog timer is stopped after reset	R/W
b1	—	Reserved bit	Set to 1.	R/W
b2	ROMCR	ROM code protect disable bit	0: ROM code protect disabled 1: ROMCP1 bit enabled	R/W
b3	ROMCP1	ROM code protect bit	0: ROM code protect enabled 1: ROM code protect disabled	R/W
b4	VDSEL0	Voltage detection 0 level select bit (2)	b5 b4 0 0: 3.80 V selected (Vdet0_3) 0 1: 2.85 V selected (Vdet0_2) 1 0: 2.35 V selected (Vdet0_1) 1 1: 1.90 V selected (Vdet0_0)	R/W
b5	VDSEL1			R/W
b6	LVDAS	Voltage detection 0 circuit start bit (3)	0: Voltage monitor 0 reset enabled after reset 1: Voltage monitor 0 reset disabled after reset	R/W
b7	CSPROINI	Count source protection mode after reset select bit	0: Count source protect mode enabled after reset 1: Count source protect mode disabled after reset	R/W

Notes:
1. The OFS register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the OFS register. If the block including the OFS register is erased, the OFS register is set to FFh.
   When blank products are shipped, the OFS register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS register is the value programmed by the user.
2. The same level of the voltage detection 0 level selected by bits VDSEL0 and VDESL1 is set in both functions of voltage monitor 0 reset and power-on reset.
3. To use power-on reset and voltage monitor 0 reset, set the LVDAS bit to 0 (voltage monitor 0 reset enabled after reset).

For a setting example of the OFS register, refer to **13.3.1 Setting Example of Option Function Select Area**.

LVDAS Bit (Voltage Detection 0 Circuit Start Bit)

The Vdet0 voltage to be monitored by the voltage detection 0 circuit is selected by bits VDSEL0 and VDSEL1.

14.2.7 Option Function Select Register 2 (OFS2)

Address 0FFDBh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	WDTRCS1	WDTRCS0	WDTUFS1	WDTUFS0
After Reset	User Settng Value (1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTUFS0	Watchdog timer underflow period set bit	b1 b0 0 0: 03FFh 0 1: 0FFFh 1 0: 1FFFh 1 1: 3FFFh	R/W
b1	WDTUFS1			R/W
b2	WDTRCS0	Watchdog timer refresh acknowledgement period set bit	b3 b2 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100%	R/W
b3	WDTRCS1			R/W
b4	—	Reserved bits	Set to 1.	R/W
b5	—			
b6	—			
b7	—			

Note:

1. The OFS2 register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the OFS2 register. If the block including the OFS2 register is erased, the OFS2 register is set to FFh.
   When blank products are shipped, the OFS2 register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS2 register is the value programmed by the user.

   For a setting example of the OFS2 register, refer to **13.3.1 Setting Example of Option Function Select Area**.

Bits WDTRCS0 and WDTRCS1 (Watchdog Timer Refresh Acknowledgement Period Set Bit)

Assuming that the period from when the watchdog timer starts counting until it underflows is 100%, the refresh acknowledgement period for the watchdog timer can be selected.
For details, refer to **14.3.1.1 Refresh Acknowledgment Period**.

14.3 Functional Description

14.3.1 Common Items for Multiple Modes

14.3.1.1 Refresh Acknowledgment Period

The period for acknowledging refreshment operation to the watchdog timer (write to the WDTR register) can be selected by bits WDTRCS0 and WDTRCS1 in the OFS2 register. Figure 14.2 shows the Refresh Acknowledgement Period for Watchdog Timer.

Assuming that the period from when the watchdog timer starts counting until it underflows is 100%, a refresh operation executed during the refresh acknowledgement period is acknowledged. Any refresh operation executed during the period other than the above is processed as an incorrect write, and a watchdog timer interrupt or watchdog timer reset (selectable by the PM12 bit in the PM1 register) is generated.

Do not execute any refresh operation while the count operation of the watchdog timer is stopped.

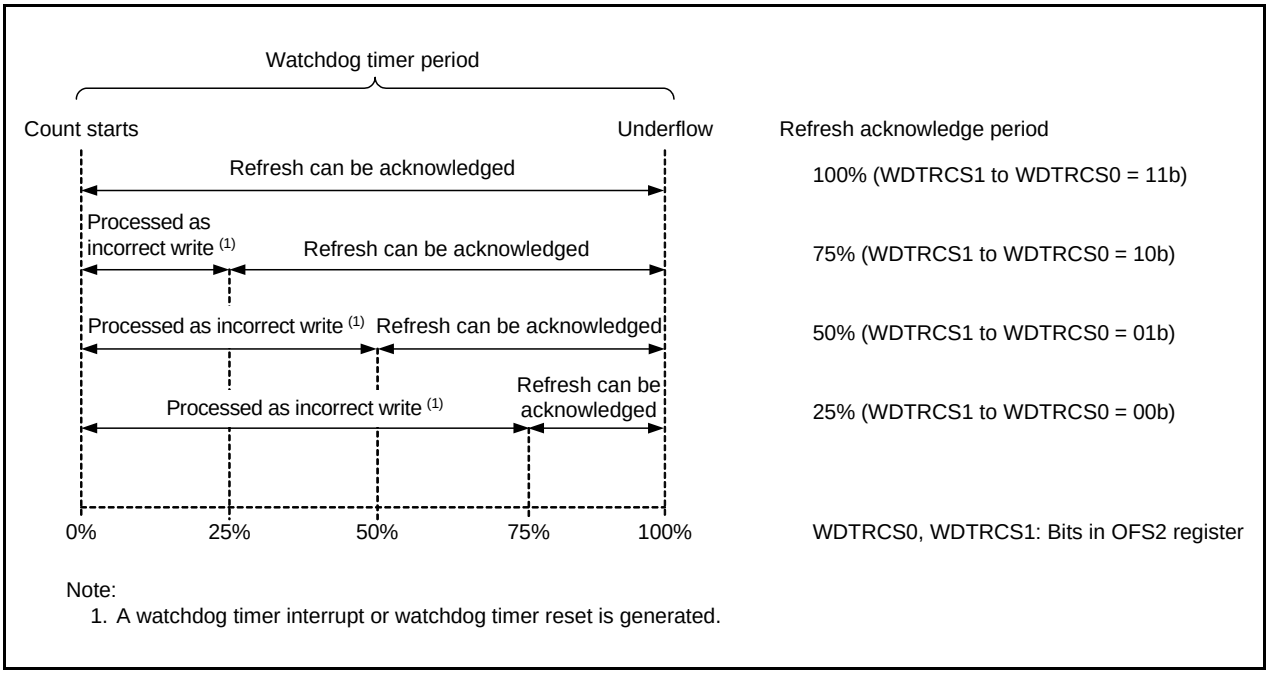


Figure 14.2 Refresh Acknowledgement Period for Watchdog Timer

14.3.2 Count Source Protection Mode Disabled

The count source for the watchdog timer is the CPU clock when count source protection mode is disabled. Table 14.2 lists the Watchdog Timer Specifications (Count Source Protection Mode Disabled).

Table 14.2 Watchdog Timer Specifications (Count Source Protection Mode Disabled)

Item	Specification
Count source	CPU clock
Count operation	Decrement
Period	$\frac{\text{Division ratio of prescaler (n)} \times \text{count value of watchdog timer (m)}}{\text{CPU clock}}$ (1) n: 16 or 128 (selected by the WDTC7 bit in the WDTC register) m: Value set by bits WDTUFS0 and WDTUFS1 in the OFS2 register Example: The period is approximately 13.1 ms when: - The CPU clock frequency is set to 20 MHz. - The prescaler is divided by 16. - Bits WDTUFS1 to WDTUFS0 are set to 11b (3FFFh).
Watchdog timer initialization conditions	• Reset • Write 00h and then FFh to the WDTR register. (3) • Underflow
Count start conditions	The operation of the watchdog timer after a reset is selected by the WDTON bit (2) in the OFS register (address 0FFFFh). • When the WDTON bit is set to 1 (watchdog timer is stopped after reset) The watchdog timer and prescaler are stopped after a reset and start counting when the WDTS register is written to. • When the WDTON bit is set to 0 (watchdog timer starts automatically after reset) The watchdog timer and prescaler start counting automatically after a reset.
Count stop condition	Stop mode, wait mode (Count resumes from the retained value after exiting.)
Operations at underflow	• When the PM12 bit in the PM1 register is set to 0 Watchdog timer interrupt • When the PM12 bit in the PM1 register is set to 1 Watchdog timer reset (refer to **5.5 Watchdog Timer Reset**)

Notes:
1. The watchdog timer is initialized when 00h and then FFh is written to the WDTR register. The prescaler is initialized after a reset. This may cause some errors due to the prescaler during the watchdog timer period.
2. The WDTON bit cannot be changed by a program. To set this bit, write 0 to bit 0 of address 0FFFFh with a flash programmer.
3. Write the WDTR register during the count operation of the watchdog timer.

14.3.3 Count Source Protection Mode Enabled

The count source for the watchdog timer is the low-speed on-chip oscillator clock for the watchdog timer when count source protection mode is enabled. If the CPU clock stops when a program is out of control, the clock can still be supplied to the watchdog timer.
Table 14.3 lists the Watchdog Timer Specifications (Count Source Protection Mode Enabled).

Table 14.3 Watchdog Timer Specifications (Count Source Protection Mode Enabled)

Item	Specification
Count source	Low-speed on-chip oscillator clock
Count operation	Decrement
Period	$\frac{\text{Count value of watchdog timer (m)}}{\text{Low-speed on-chip oscillator clock for the watchdog timer}}$ m: Value set by bits WDTUFS0 and WDTUFS1 in the OFS2 register Example: The period is approximately 8.2 ms when: - The on-chip oscillator clock for the watchdog timer is set to 125 kHz. - Bits WDTUFS1 to WDTUFS0 are set to 00b (03FFh).
Watchdog timer initialization conditions	• Reset • Write 00h and then FFh to the WDTR register (3) • Underflow
Count start conditions	The operation of the watchdog timer after a reset is selected by the WDTON bit (1) in the OFS register (address 0FFFFh). • When the WDTON bit is set to 1 (watchdog timer is stopped after reset) The watchdog timer and prescaler are stopped after a reset and start counting when the WDTS register is written to. • When the WDTON bit is set to 0 (watchdog timer starts automatically after reset) The watchdog timer and prescaler start counting automatically after a reset.
Count stop condition	None (Count does not stop even in wait mode and stop mode once it starts)
Operation at underflow	Watchdog timer reset (refer to **5.5 Watchdog Timer Reset**)
Registers, bits	• When the CSPPRO bit in the CSPR register is set to 1 (count source protection mode enabled) (2), the following are set automatically: - The low-speed on-chip oscillator for the watchdog timer is on. - The PM12 bit in the PM1 register is set to 1 (watchdog timer reset when the watchdog timer underflows).

Notes:
1. The WDTON bit cannot be changed by a program. To set this bit, write 0 to bit 0 of address 0FFFFh with a flash programmer.
2. Even if 0 is written to the CSPROINI bit in the OFS register, the CSPRO bit is set to 1. The CSPROINI bit cannot be changed by a program. To set this bit, write 0 to bit 7 of address 0FFFFh with a flash programmer.
3. Write the WDTR register during the count operation of the watchdog timer.

15. DTC

Note

The description offered in this chapter is based on the R8C/3MK Group.
For R8C/3MU Group, refer to **1.1.2 Differences between Groups**.

The DTC (data transfer controller) is a function that transfers data between the SFR and on-chip memory without using the CPU. This chip incorporates one DTC channel. The DTC is activated by a peripheral function interrupt to perform data transfers. The DTC and CPU use the same bus, and the DTC takes priority over the CPU in using the bus.
To control DTC data transfers, control data comprised of a transfer source address, a transfer destination address, and operating modes are allocated in the DTC control data area. Each time the DTC is activated, the DTC reads control data to perform data transfers.

15.1 Overview

Table 15.1 shows the DTC Specifications.

Table 15.1 DTC Specifications

Item		Specification
Activation sources		26 sources
Allocatable control data		24 sets
Address space which can be transferred		64 Kbytes (00000h to 0FFFFh)
Maximum number of transfer times	Normal mode	256 times
	Repeat mode	255 times
Maximum size of block to be transferred	Normal mode	256 bytes
	Repeat mode	255 bytes
Unit of transfers		Byte
Transfer mode	Normal mode	Transfers end on completion of the transfer causing the DTCCTj register value to change from 1 to 0.
	Repeat mode	On completion of the transfer causing the DTCCTj register value to change from 1 to 0, the repeat area address is initialized and the DTRLDj register value is reloaded to the DTCCTj register to continue transfers.
Address control	Normal mode	Fixed or incremented
	Repeat mode	Addresses of the area not selected as the repeat area are fixed or incremented.
Priority of activation sources		Refer to **Table 15.5 DTC Activation Sources and DTC Vector Addresses**.
Interrupt request	Normal mode	When the data transfer causing the DTCCTj register value to change from 1 to 0 is performed, the activation source interrupt request is generated for the CPU, and interrupt handling is performed on completion of the data transfer.
	Repeat mode	When the data transfer causing the DTCCTj register value to change from 1 to 0 is performed while the RPTINT bit in the DTCCRj register is 1 (interrupt generation enabled), the activation source interrupt request is generated for the CPU, and interrupt handling is performed on completion of the transfer.
Transfer start		When bits DTCENi0 to DTCENi7 in the DTCENi registers are 1 (activation enabled), data transfer is started each time the corresponding DTC activation sources are generated.
Transfer stop	Normal mode	• When bits DTCENi0 to DTCENi7 are set to 0 (activation disabled). • When the data transfer causing the DTCCTj register value to change from 1 to 0 is completed.
	Repeat mode	• When bits DTCENi0 to DTCENi7 are set to 0 (activation disabled). • When the data transfer causing the DTCCTj register value to change from 1 to 0 is completed while the RPTINT bit is 1 (interrupt generation enabled).

i = 0 to 3, 6, j = 0 to 23

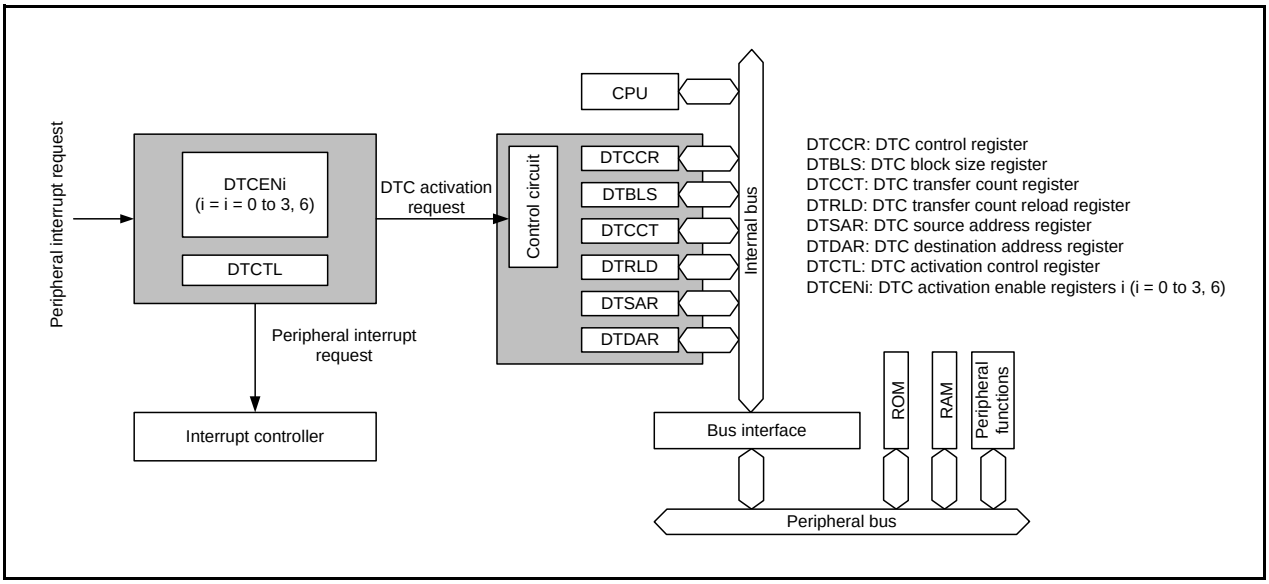


Figure 15.1 DTC Block Diagram

15.2 Registers

When the DTC is activated, control data (DTCCRj, DTBLSj, DTCCTj, DTRLDj, DTSARj, and DTDARj, j = 0 to 23) allocated in the control data area is read, and then transferred to the control registers (DTCCR, DTBLS, DTCCT, DTRLD, DTSAR, and DTDAR) in the DTC. On completion of the DTC data transfer, the contents of the DTC control registers are written back to the control data area.

Each DTCCR, DTBLS, DTCCT, DTRLD, DTSAR, and DTDAR register cannot be directly read or written to. DTCCRj, DTBLSj, DTCCTj, DTRLDj, DTSARj, and DTDARj are allocated as control data at addresses from 2C40h to 2CFFh in the DTC control data area, and can be directly accessed.
Also, registers DTCTL and DTCENi (i = 0 to 3, 6) can be directly accessed.

15.2.1 DTC Control Register j (DTCCRj) (j = 0 to 23)

Address Refer to **Table 15.4 Control Data Allocation Addresses**.

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	RPTINT	CHNE	DAMOD	SAMOD	RPTSEL	MODE
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Bit Name	Function	R/W
b0	MODE	Transfer mode select bit	0: Normal mode 1: Repeat mode	R/W
b1	RPTSEL	Repeat area select bit (1)	0: Transfer destination is the repeat area 1: Transfer source is the repeat area	R/W
b2	SAMOD	Source address control bit (2)	0: Fixed 1: Incremented	R/W
b3	DAMOD	Destination address control bit (2)	0: Fixed 1: Incremented	R/W
b4	CHNE	Chain transfer enable bit (3)	0: Chain transfers disabled 1: Chain transfers enabled	R/W
b5	RPTINT	Repeat mode interrupt enable bit (1)	0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b6	—	Reserved bits	Set to 0.	R/W
b7	—			

Notes:
1. This bit is valid when the MODE bit is 1 (repeat mode).
2. Settings of bits SAMOD and DAMOD are invalid for the repeat area.
3. Set the CHNE bit in the DTCCR23 register to 0 (chain transfers disabled).

15.2.2 DTC Block Size Register j (DTBLSj) (j = 0 to 23)

Address Refer to **Table 15.4 Control Data Allocation Addresses**.

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	Setting Range	R/W
b7 to b0	These bits specify the size of the data block to be transferred by one activation.	00h to FFh (1)	R/W

Note:
1. When the DTBLS register is set to 00h, the block size is 256 bytes.

15.2.3 DTC Transfer Count Register j (DTCCTj) (j = 0 to 23)

Address Refer to **Table 15.4 Control Data Allocation Addresses**.

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	Setting Range	R/W
b7 to b0	These bits specify the number of times of DTC data transfers.	00h to FFh (1)	R/W

Note:
1. When the DTCCT register is set to 00h, the number of transfer times is 256. Each time the DTC is activated, the DTCCT register is decremented by 1.

15.2.4 DTC Transfer Count Reload Register j (DTRLDj) (j = 0 to 23)

Address Refer to **Table 15.4 Control Data Allocation Addresses**.

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	Setting Range	R/W
b7 to b0	This register value is reloaded to the DTCCT register in repeat mode.	00h to FFh (1)	R/W

Note:
1. Set the initial value for the DTCCT register.

15.2.5 DTC Source Address Register j (DTSARj) (j = 0 to 23)

Address Refer to **Table 15.4 Control Data Allocation Addresses**.

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	Setting Range	R/W
b15 to b0	These bits specify a transfer source address for data transfer.	0000h to FFFFh	R/W

15.2.6 DTC Destination Address Register j (DTDARj) (j = 0 to 23)

Address Refer to **Table 15.4 Control Data Allocation Addresses**.

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	Setting Range	R/W
b15 to b0	These bits specify a transfer destination address for data transfer.	0000h to FFFFh	R/W

15.2.7 DTC Activation Enable Register i (DTCENi) (i = 0 to 3, 6)

Address 0088h (DTCEN0), 0089h (DTCEN1), 008Ah (DTCEN2), 008Bh (DTCEN3), 008Eh (DTCEN6)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	DTCENi7	DTCENi6	DTCENi5	DTCENi4	DTCENi3	DTCENi2	DTCENi1	DTCENi0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	DTCENi0	DTC activation enable bit (1)	0: Activation disabled 1: Activation enabled	R/W
b1	DTCENi1			R/W
b2	DTCENi2			R/W
b3	DTCENi3			R/W
b4	DTCENi4			R/W
b5	DTCENi5			R/W
b6	DTCENi6			R/W
b7	DTCENi7			R/W

i = 0 to 3, 6

Note:

1. For the operation of this bit, refer to **15.3.7 Interrupt Sources**.

The DTCENi registers enable/disable DTC activation by interrupt sources. Table 15.2 shows Correspondences between Bits DTCENi0 to DTCENi7 (i = 0 to 3, 6) and Interrupt Sources.

Table 15.2 Correspondences between Bits DTCENi0 to DTCENi7 (i = 0 to 3, 6) and Interrupt Sources

Register	DTCENi7 Bit	DTCENi6 Bit	DTCENi 5Bit	DTCENi4 Bit	DTCENi3 Bit	DTCENi2 Bit	DTCENi1 Bit	DTCENi0 Bit
DTCEN0	$\overline{\text{INT0}}$	$\overline{\text{INT1}}$	$\overline{\text{INT2}}$	$\overline{\text{INT3}}$	$\overline{\text{INT4}}$	—	—	—
DTCEN1	Key input	A/D converter (1)	UART0 reception	UART0 transmission	UART1 reception	UART1 transmission	UART2 reception	UART2 transmission
DTCEN2	SSU/I²C bus receive data full	SSU/I²C bus transmit data empty	Voltage Monitor 2	Voltage Monitor 1	—	—	Timer RC input-capture/ compare-match A	Timer RC input-capture/ compare-match B
DTCEN3	Timer RC input-capture/ compare-match C	Timer RC input-capture/ compare-match D	UART3 reception	—	—	—	UART3 transmission	—
DTCEN6	—	Timer RA	—	Timer RB	Flash ready status	—	A/D converter (1)	—

Note:

1. Not available in the R8C/3MU Group.

15.2.8 DTC Activation Control Register (DTCTL)

Address 0080h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	NMIF	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bit	Set to 0.	R/W
b1	NMIF	Non-maskable interrupt generation bit (1)	0: Non-maskable interrupts not generated 1: Non-maskable interrupts generated	R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

Note:
1. This bit is set to 0 when the read result is 1 and 0 is written to the same bit. This bit remains unchanged even if the read result is 0 and 0 is written to the same bit. This bit remains unchanged if 1 is written to it.

The DTCTL register controls DTC activation when a non-maskable interrupt (an interrupt by the watchdog timer, oscillation stop detection, voltage monitor 1, or voltage monitor 2) is generated.

NMIF Bit (Non-Maskable Interrupt Generation Bit)

The NMIF bit is set to 1 when a watchdog timer interrupt, an oscillation stop detection interrupt, a voltage monitor 1 interrupt, or a voltage monitor 2 interrupt is generated.
When the NMIF bit is 1, the DTC is not activated even if the interrupt which enables DTC activation is generated. If the NMIF bit is changed to 1 during DTC transfer, the transfer is continued until it is completed.

When an interrupt source is the watchdog timer, wait for the following cycles before writing 0 to the NMIF bit:
If the WDTC7 bit in the WDTC register is set to 0 (divide-by-16 using the prescaler), wait for 16 cycles of the CPU clock after the interrupt source is generated.
If the WDTC7 bit is set to 1 (divide-by-128 using the prescaler), wait for 128 cycles of the CPU clock after the interrupt source is generated.
When an interrupt source is oscillation stop detection, set to the OCD1 bit in the OCD register to 0 (oscillation stop detection interrupt disabled) before writing 0 to the NMIF bit.

15.3 Function Description

15.3.1 Overview

When the DTC is activated, control data is read from the DTC control data area to perform data transfers and control data after data transfer is written back to the DTC control data area. Twenty-four sets of control data can be stored in the DTC control data area, which allows 24 types of data transfers to be performed.
There are two transfer modes: normal mode and repeat mode. When the CHNE bit in the DTCCRj (j = 0 to 23) register is set to 1 (chain transfers enabled), multiple control data is read and data transfers are continuously performed by one activation source (chain transfers).
A transfer source address is specified by the 16-bit register DTSARj, and a transfer destination address is specified by the 16-bit register DTDARj. The values in the registers DTSARj and DTDARj are separately fixed or incremented according to the control data on completion of the data transfer.

15.3.2 Activation Sources

The DTC is activated by an interrupt source. Figure 15.2 is a Block Diagram Showing Control of DTC Activation Sources.
The interrupt sources to activate the DTC are selected with the DTCENi (i = 0 to 3, 6) registers.
The DTC sets 0 (activation disabled) to the corresponding bit among bits DTCENi0 to DTCENi7 in the DTCENi register during operation when the setting of data transfer (the first transfer in chain transfers) is either of the following:

- Transfer causing the DTCCTj (j = 0 to 23) register value to change to 0 in normal mode
- Transfer causing the DTCCTj register value to change to 0 while the RPTINT bit in the DTCCRj register is 1 (interrupt generation enabled) in repeat mode

If the data transfer setting is not either of the above and the activation source is an interrupt source for timer RC, or the flash memory, the DTC sets 0 to the interrupt source flag corresponding to the activation source during operation.
Table 15.3 shows the DTC Activation Sources and Interrupt Source Flags for Setting to 0 during DTC Operation.
If multiple activation sources are simultaneously generated, the DTC activation will be performed according to the DTC activation source priority.
If multiple activation sources are simultaneously generated on completion of DTC operation, the next transfer will be performed according to the priority.
DTC activation is not affected by the I flag or interrupt control register, unlike with interrupt request operation. Therefore, even if interrupt requests cannot be acknowledged because interrupts are disabled, DTC activation requests can be acknowledged. The IR bit in the interrupt control register does not change even when an interrupt source to enable DTC activation is generated.

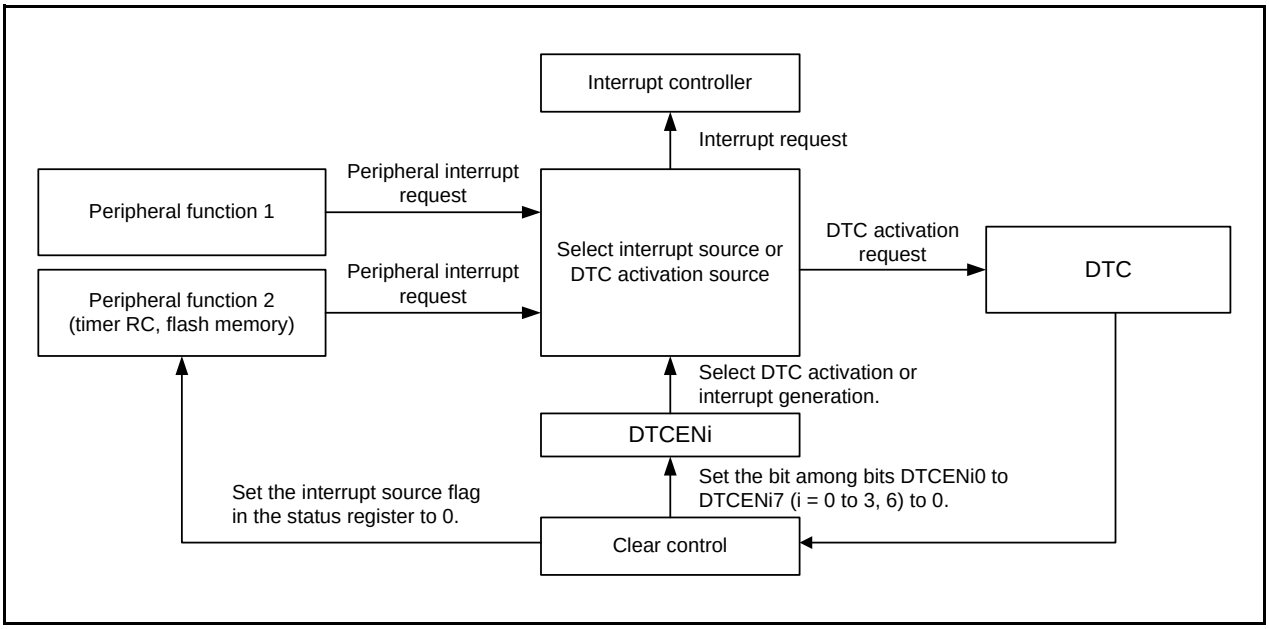


Figure 15.2 Block Diagram Showing Control of DTC Activation Sources

Table 15.3 DTC Activation Sources and Interrupt Source Flags for Setting to 0 during DTC Operation

DTC activation source generation	Interrupt Source Flag for Setting to 0
Timer RC input-capture/compare-match A	IMFA bit in TRCSR register
Timer RC input-capture/compare-match B	IMFB bit in TRCSR register
Timer RC input-capture/compare-match C	IMFC bit in TRCSR register
Timer RC input-capture/compare-match D	IMFD bit in TRCSR register
Flash ready status	RDYSTI bit in FST register

15.3.3 Control Data Allocation and DTC Vector Table

Control data is allocated in the order: Registers DTCCRj, DTBLSj, DTCCTj, DTRLDj, DTSARj, and DTDARj (j = 0 to 23). Table 15.4 shows the Control Data Allocation Addresses.

Table 15.4 Control Data Allocation Addresses

Register Symbol	Control Data No.	Address	DTCCRj Register	DTBLSj Register	DTCCTj Register	DTRLDj Register	DTSARj Register (Lower 8 Bits)	DTSARj Register (Higher 8 Bits)	DTDARj Register (Lower 8 Bits)	DTDARj Register (Higher 8 Bits)
DTCD0	Control Data 0	2C40h to 2C47h	2C40h	2C41h	2C42h	2C43h	2C44h	2C45h	2C46h	2C47h
DTCD1	Control Data 1	2C48h to 2C4Fh	2C48h	2C49h	2C4Ah	2C4Bh	2C4Ch	2C4Dh	2C4Eh	2C4Fh
DTCD2	Control Data 2	2C50h to 2C57h	2C50h	2C51h	2C52h	2C53h	2C54h	2C55h	2C56h	2C57h
DTCD3	Control Data 3	2C58h to 2C5Fh	2C58h	2C59h	2C5Ah	2C5Bh	2C5Ch	2C5Dh	2C5Eh	2C5Fh
DTCD4	Control Data 4	2C60h to 2C67h	2C60h	2C61h	2C62h	2C63h	2C64h	2C65h	2C66h	2C67h
DTCD5	Control Data 5	2C68h to 2C6Fh	2C68h	2C69h	2C6Ah	2C6Bh	2C6Ch	2C6Dh	2C6Eh	2C6Fh
DTCD6	Control Data 6	2C70h to 2C77h	2C70h	2C71h	2C72h	2C73h	2C74h	2C75h	2C76h	2C77h
DTCD7	Control Data 7	2C78h to 2C7Fh	2C78h	2C79h	2C7Ah	2C7Bh	2C7Ch	2C7Dh	2C7Eh	2C7Fh
DTCD8	Control Data 8	2C80h to 2C87h	2C80h	2C81h	2C82h	2C83h	2C84h	2C85h	2C86h	2C87h
DTCD9	Control Data 9	2C88h to 2C8Fh	2C88h	2C89h	2C8Ah	2C8Bh	2C8Ch	2C8Dh	2C8Eh	2C8Fh
DTCD10	Control Data 10	2C90h to 2C97h	2C90h	2C91h	2C92h	2C93h	2C94h	2C95h	2C96h	2C97h
DTCD11	Control Data 11	2C98h to 2C9Fh	2C98h	2C99h	2C9Ah	2C9Bh	2C9Ch	2C9Dh	2C9Eh	2C9Fh
DTCD12	Control Data 12	2CA0h to 2CA7h	2CA0h	2CA1h	2CA2h	2CA3h	2CA4h	2CA5h	2CA6h	2CA7h
DTCD13	Control Data 13	2CA8h to 2CAFh	2CA8h	2CA9h	2CAAh	2CABh	2CACh	2CADh	2CAEh	2CAFh
DTCD14	Control Data 14	2CB0h to 2CB7h	2CB0h	2CB1h	2CB2h	2CB3h	2CB4h	2CB5h	2CB6h	2CB7h
DTCD15	Control Data 15	2CB8h to 2CBFh	2CB8h	2CB9h	2CBAh	2CBBh	2CBCh	2CBDh	2CBEh	2CBFh
DTCD16	Control Data 16	2CC0h to 2CC7h	2CC0h	2CC1h	2CC2h	2CC3h	2CC4h	2CC5h	2CC6h	2CC7h
DTCD17	Control Data 17	2CC8h to 2CCFh	2CC8h	2CC9h	2CCAh	2CCBh	2CCCh	2CCDh	2CCEh	2CCFh
DTCD18	Control Data 18	2CD0h to 2CD7h	2CD0h	2CD1h	2CD2h	2CD3h	2CD4h	2CD5h	2CD6h	2CD7h
DTCD19	Control Data 19	2CD8h to 2CDFh	2CD8h	2CD9h	2CDAh	2CDBh	2CDCh	2CDDh	2CDEh	2CDFh
DTCD20	Control Data 20	2CE0h to 2CE7h	2CE0h	2CE1h	2CE2h	2CE3h	2CE4h	2CE5h	2CE6h	2CE7h
DTCD21	Control Data 21	2CE8h to 2CEFh	2CE8h	2CE9h	2CEAh	2CEBh	2CECh	2CEDh	2CEEh	2CEFh
DTCD22	Control Data 22	2CF0h to 2CF7h	2CF0h	2CF1h	2CF2h	2CF3h	2CF4h	2CF5h	2CF6h	2CF7h
DTCD23	Control Data 23	2CF8h to 2CFFh	2CF8h	2CF9h	2CFAh	2CFBh	2CFCh	2CFDh	2CFEh	2CFFh

j = 0 to 23

When the DTC is activated, one control data is selected according to the data read from the vector table which has been assigned to each activation source, and the selected control data is read from the DTC control data area.
Table 15.5 shows the DTC Activation Sources and DTC Vector Addresses. A one-byte vector table area is assigned to each activation source and one value from 00000000b to 00010111b (control data numbers in Table 15.4) is stored in each area to select one of the 24 control data sets.
Figures 15.3 to 15.7 show the DTC Internal Operation Flowchart.

Table 15.5 DTC Activation Sources and DTC Vector Addresses

Interrupt Request Source	Interrupt Name	Source No.	DTC Vector Address	Priority
External input	$\overline{\text{INT0}}$	0	2C00h	High
	$\overline{\text{INT1}}$	1	2C01h	
	$\overline{\text{INT2}}$	2	2C02h	
	$\overline{\text{INT3}}$	3	2C03h	
	$\overline{\text{INT4}}$	4	2C04h	
Key input	Key input	8	2C08h	
A/D (1)	A/D converter	9	2C09h	
UART0	UART0 reception	10	2C0Ah	
	UART0 transmission	11	2C0Bh	
UART1	UART1 reception	12	2C0Ch	
	UART1 transmission	13	2C0Dh	
UART2	UART2 reception	14	2C0Eh	
	UART2 transmission	15	2C0Fh	
SSU/I^{2}C bus	Receive data full	16	2C10h	
	Transmit data empty	17	2C11h	
Voltage detection circuit	Voltage monitor 2	18	2C12h	
	Voltage monitor 1	19	2C13h	
Timer RC	Input-capture/compare-match A	22	2C16h	
	Input-capture/compare-match B	23	2C17h	
	Input-capture/compare-match C	24	2C18h	
	Input-capture/compare-match D	25	2C19h	
UART3	UART3 receive	26	2C1Ah	
	UART3 transmission	30	2C1Eh	
Timer RA	Timer RA	49	2C31h	
Timer RB	Timer RB	51	2C33h	
Flash memory	Flash ready status	52	2C34h	Low

Notes:
1. Not available in the R8C/3MU Group.

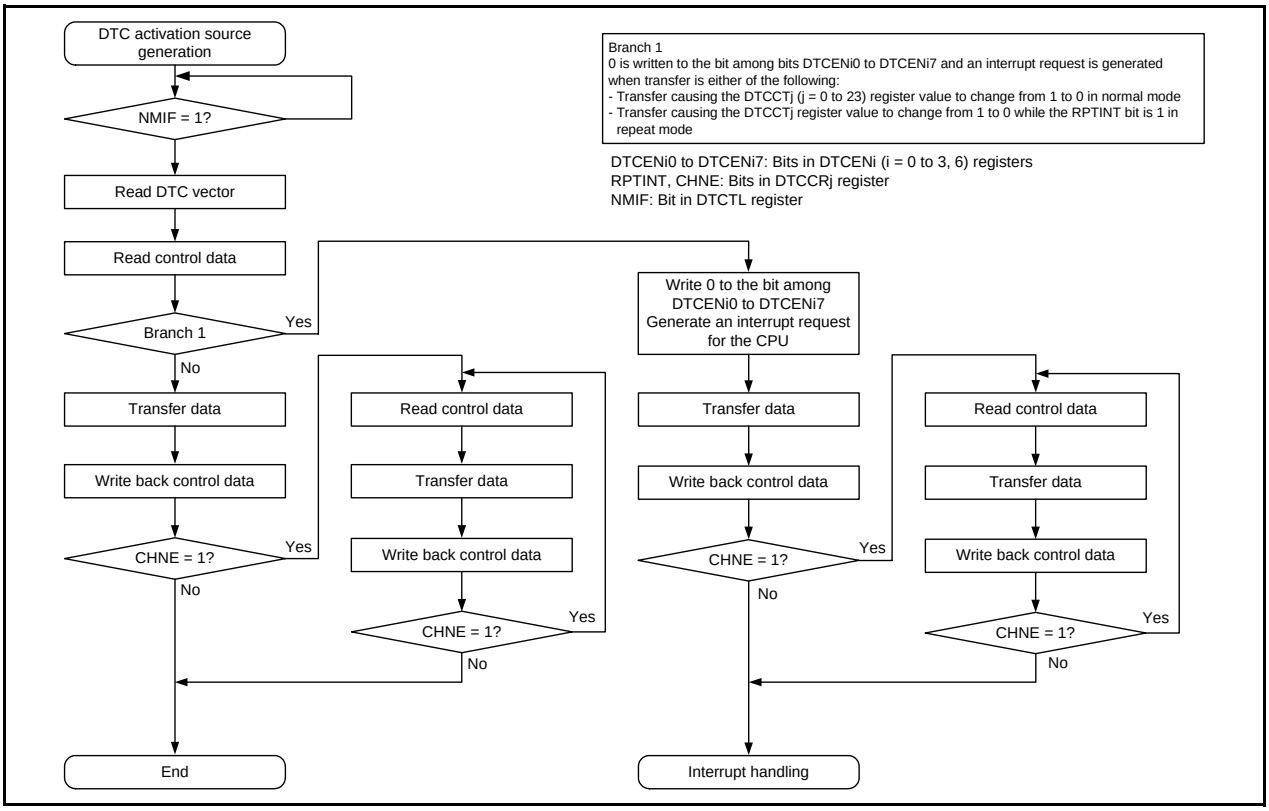


Figure 15.3 DTC Internal Operation Flowchart When DTC Activation Source is not SSU/I²C bus, Timer RC, or Flash Memory Interrupt Source

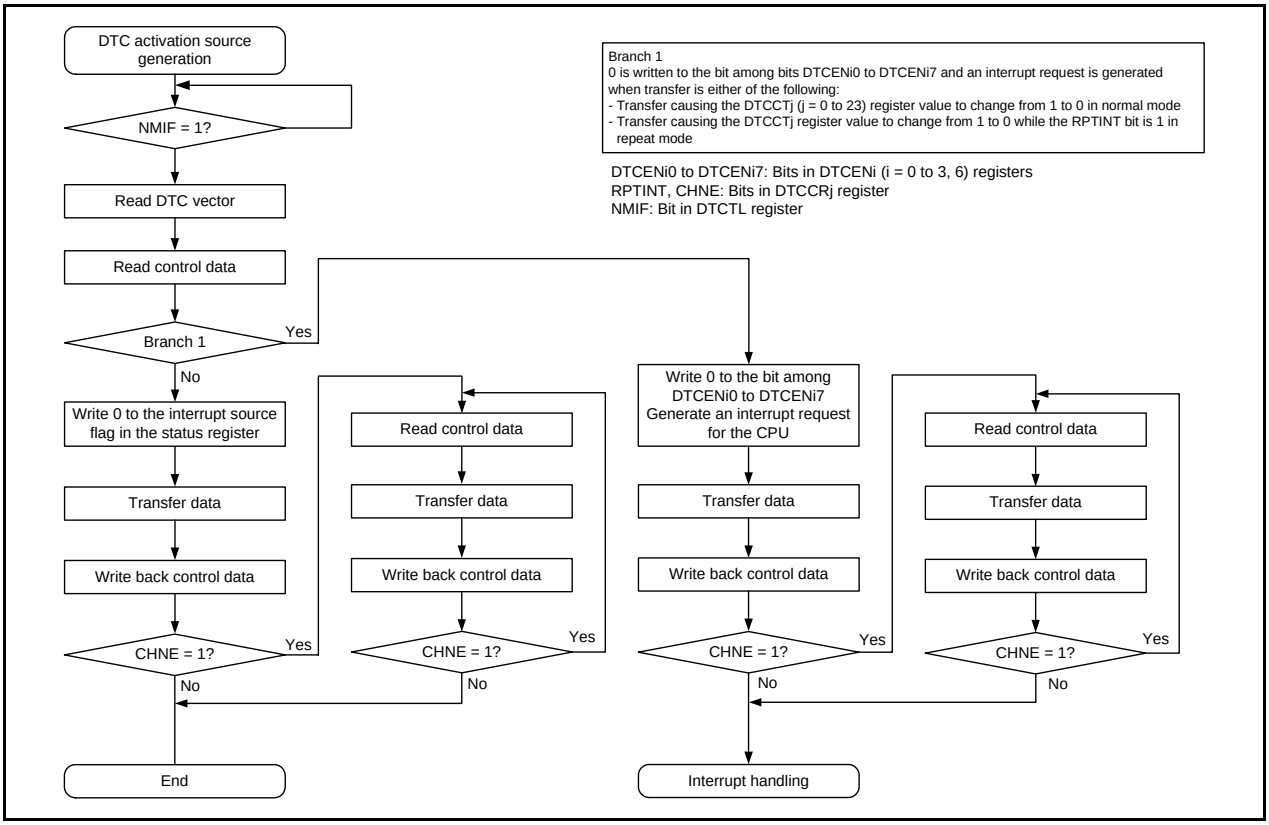
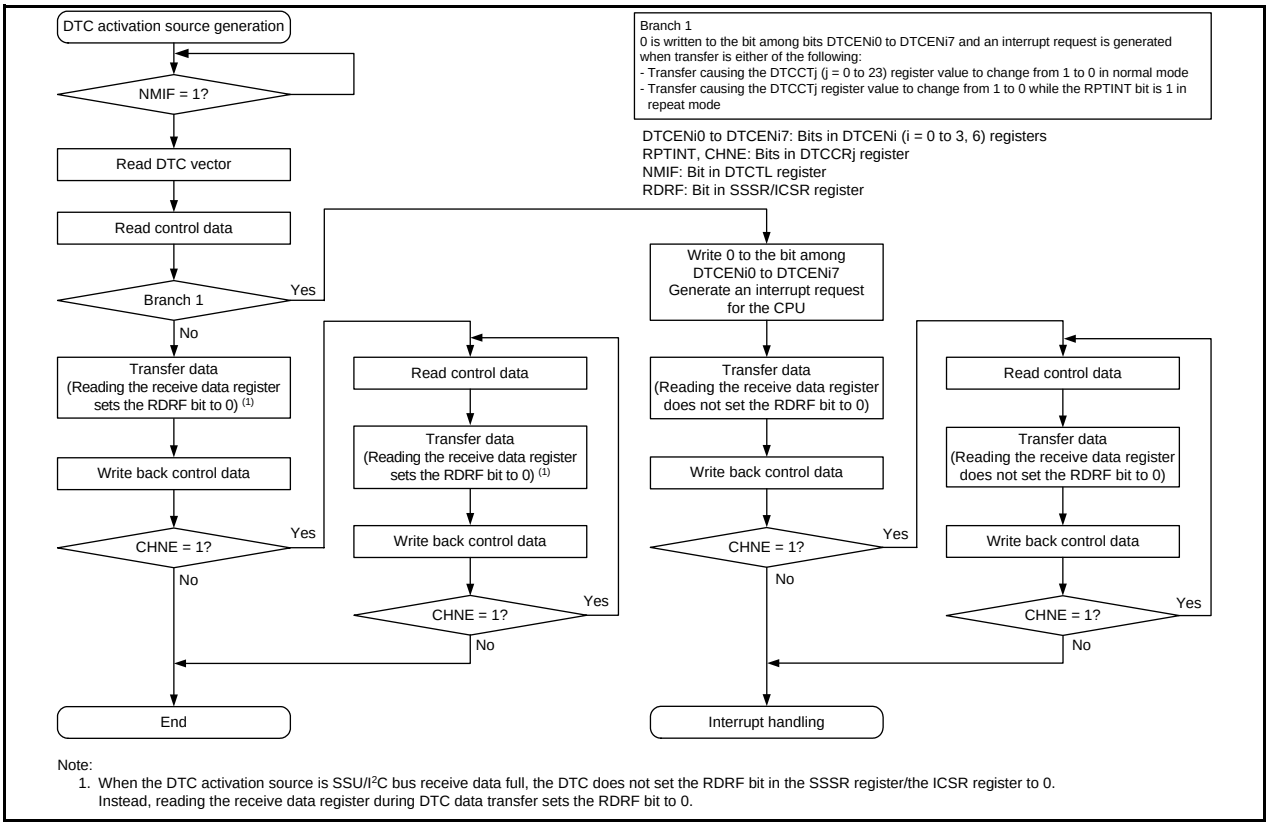
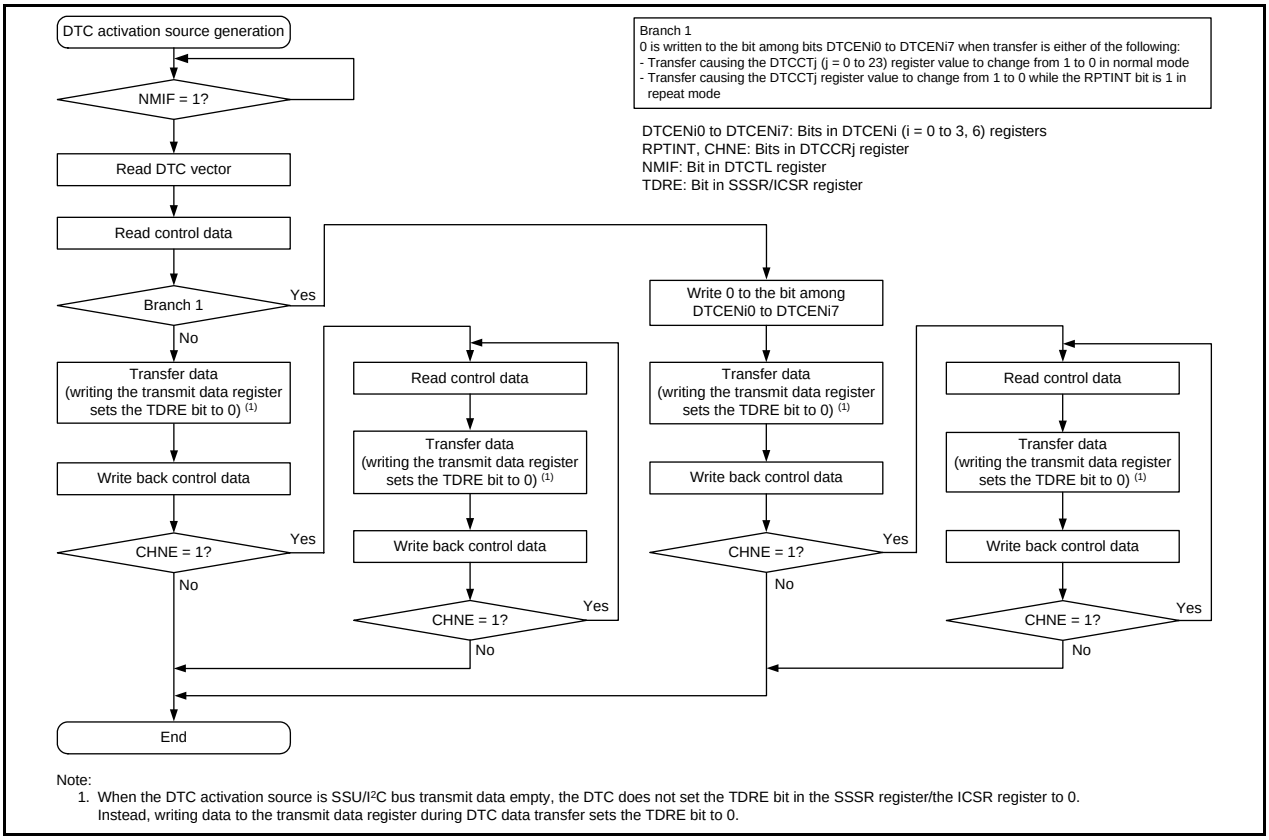


Figure 15.4 DTC Internal Operation Flowchart When DTC Activation Source is Timer RC Interrupt Source



Note:
1. When the DTC activation source is SSU/I²C bus receive data full, the DTC does not set the RDRF bit in the SSSR register/the ICSR register to 0. Instead, reading the receive data register during DTC data transfer sets the RDRF bit to 0.

Figure 15.5 DTC Internal Operation Flowchart When DTC Activation Source is SSU/I²C bus Receive Data Full



Note:
1. When the DTC activation source is SSU/I²C bus transmit data empty, the DTC does not set the TDRE bit in the SSSR register/the ICSR register to 0. Instead, writing data to the transmit data register during DTC data transfer sets the TDRE bit to 0.

Figure 15.6 DTC Internal Operation Flowchart When DTC Activation Source is SSU/I²C bus Transmit Data Empty

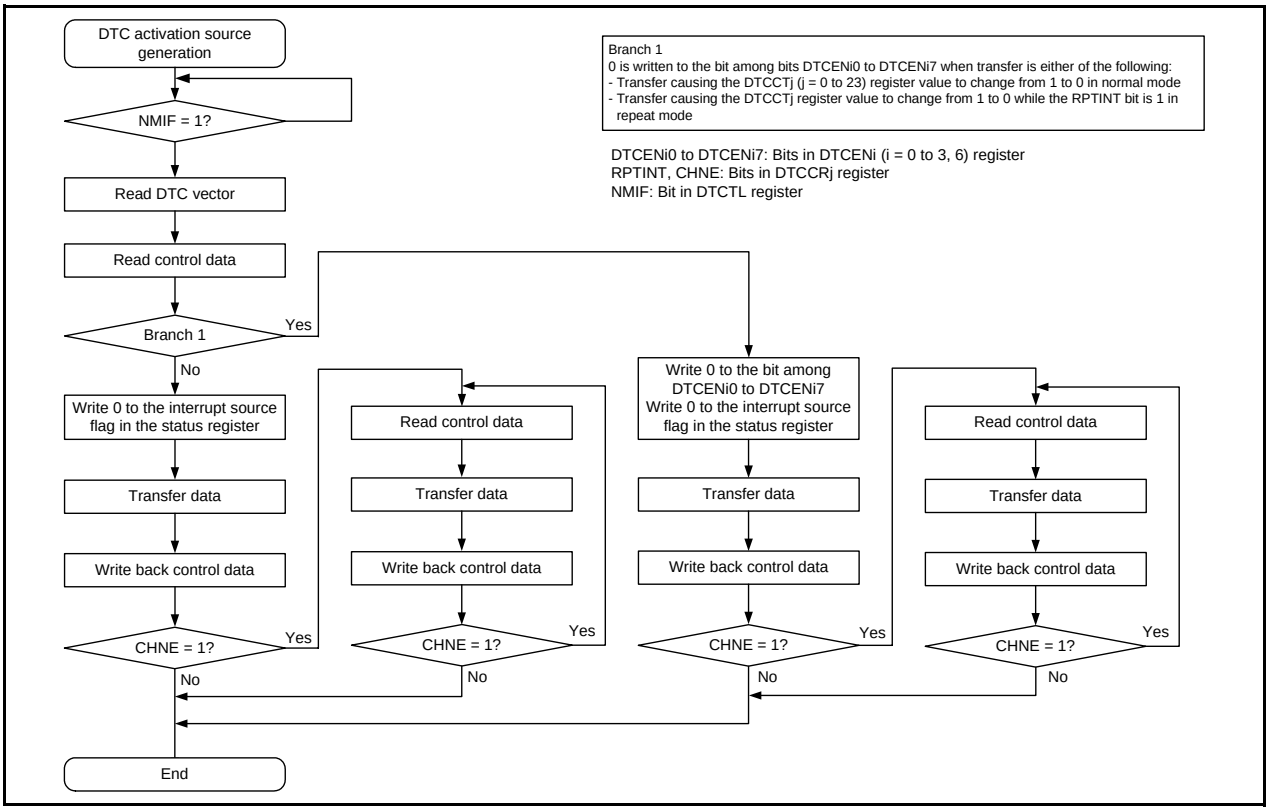


Figure 15.7 DTC Internal Operation Flowchart When DTC Activation Source is Flash ready status

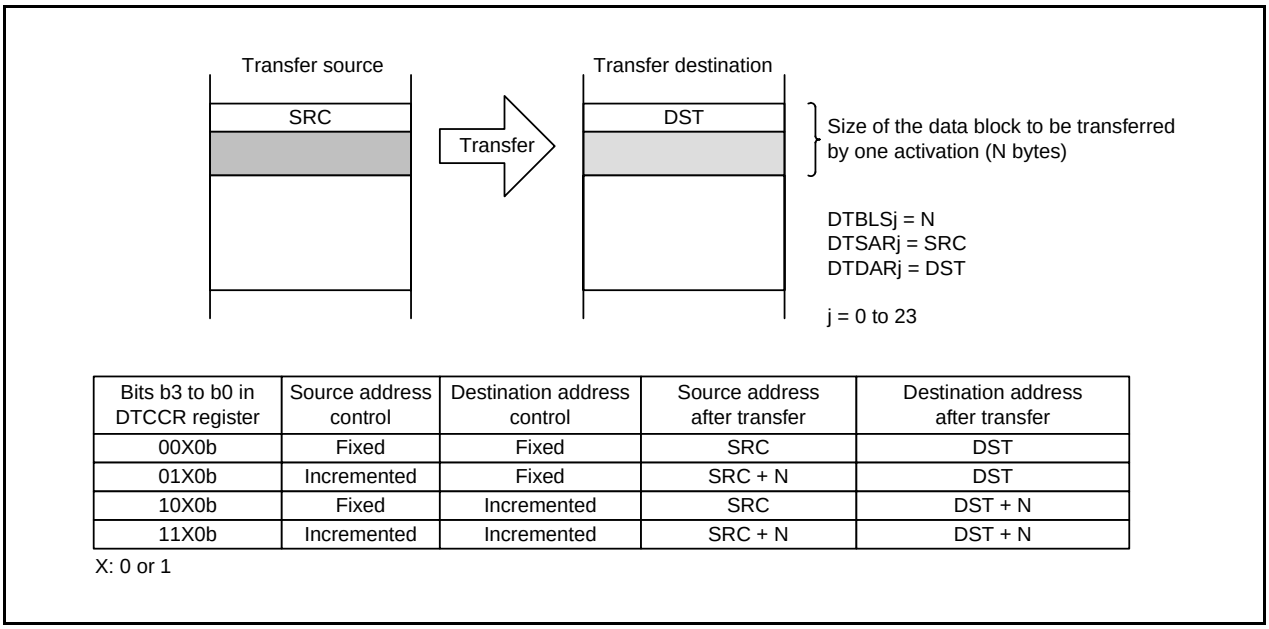
15.3.4 Normal Mode

One to 256 bytes of data are transferred by one activation. The number of transfer times can be 1 to 256. When the data transfer causing the DTCCTj (j = 0 to 23) register value to change to 0 is performed, an interrupt request for the CPU is generated during DTC operation.
Table 15.6 shows Register Functions in Normal Mode.
Figure 15.8 shows Data Transfers in Normal Mode.

Table 15.6 Register Functions in Normal Mode

Register	Symbol	Function
DTC block size register j	DTBLSj	Size of the data block to be transferred by one activation
DTC transfer count register j	DTCCTj	Number of times of data transfers
DTC transfer count reload register j	DTRLDj	Not used
DTC source address register j	DTSARj	Data transfer source address
DTC destination address register j	DTDARj	Data transfer destination address

j =0 to 23



Bits b3 to b0 in DTCCR register	Source address control	Destination address control	Source address after transfer	Destination address after transfer
00X0b	Fixed	Fixed	SRC	DST
01X0b	Incremented	Fixed	SRC + N	DST
10X0b	Fixed	Incremented	SRC	DST + N
11X0b	Incremented	Incremented	SRC + N	DST + N

X: 0 or 1

Figure 15.8 Data Transfers in Normal Mode

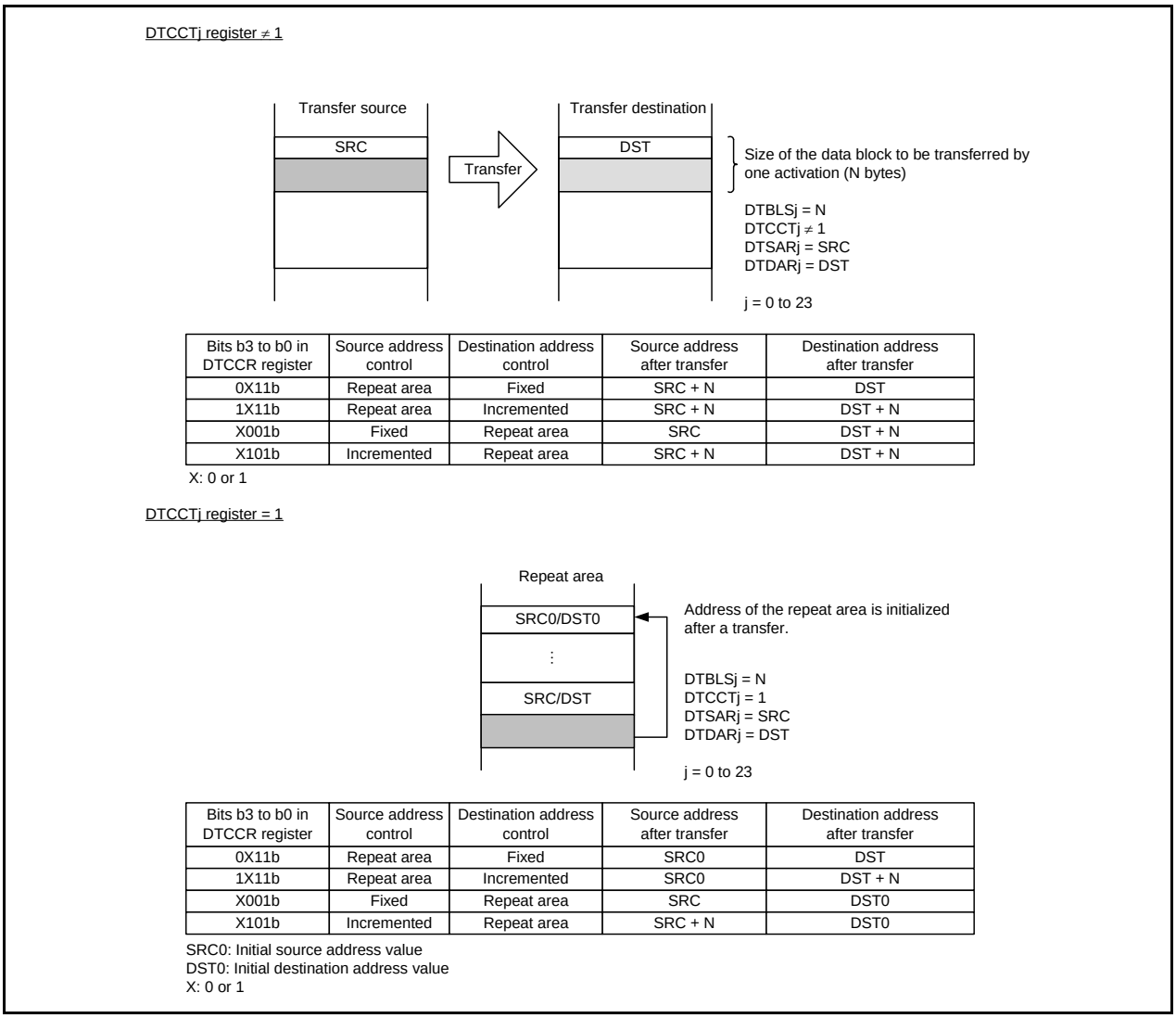
15.3.5 Repeat Mode

One to 255 bytes of data are transferred by one activation. Either of the transfer source or destination should be specified as the repeat area. The number of transfer times can be 1 to 255. On completion of the specified number of transfer times, the DTCCTj (i =0 to 23) register and the address specified for the repeat area are initialized to continue transfers. When the data transfer causing the DTCCTj register value to change to 0 is performed while the RPTINT bit in the DTCCRj register is 1 (interrupt generation enabled), an interrupt request for the CPU is generated during DTC operation.
The lower 8 bits of the initial value for the repeat area address must be 00h. The size of data to be transferred must be set to 255 bytes or less before the specified number of transfer times is completed.
Table 15.7 shows Register Functions in Repeat Mode. Figure 15.9 shows Data Transfers in Repeat Mode.

Table 15.7 Register Functions in Repeat Mode

Register	Symbol	Function
DTC block size register j	DTBLSj	Size of the data block to be transferred by one activation
DTC transfer count register j	DTCCTj	Number of times of data transfers
DTC transfer count reload register j	DTRLDj	This register value is reloaded to the DTCCT register (Data transfer count is initialized)
DTC source address register j	DTSARj	Data transfer source address
DTC destination address register j	DTDARj	Data transfer destination address

j =0 to 23



Bits b3 to b0 in DTCCR register	Source address control	Destination address control	Source address after transfer	Destination address after transfer
0X11b	Repeat area	Fixed	SRC + N	DST
1X11b	Repeat area	Incremented	SRC + N	DST + N
X001b	Fixed	Repeat area	SRC	DST + N
X101b	Incremented	Repeat area	SRC + N	DST + N

X: 0 or 1

Bits b3 to b0 in DTCCR register	Source address control	Destination address control	Source address after transfer	Destination address after transfer
0X11b	Repeat area	Fixed	SRC0	DST
1X11b	Repeat area	Incremented	SRC0	DST + N
X001b	Fixed	Repeat area	SRC	DST0
X101b	Incremented	Repeat area	SRC + N	DST0

SRC0: Initial source address value
DST0: Initial destination address value
X: 0 or 1

Figure 15.9 Data Transfers in Repeat Mode

15.3.6 Chain Transfers

When the CHNE bit in the DTCCRj (j = 0 to 22) register is 1 (chain transfers enabled), multiple data transfers can be continuously performed by one activation source. Figure 15.10 shows a Flow of Chain Transfers.
When the DTC is activated, one control data is selected according to the data read from the DTC vector address corresponding to the activation source, and the selected control data is read from the DTC control data area. When the CHNE bit for the control data is 1 (chain transfers enabled), the next control data immediately following the current control data is read and transferred after the current transfer is completed. This operation is repeated until the data transfer with the control data for which the CHNE bit is 0 (chain transfers disabled) is completed.
Set the CHNE bit in the DTCCR23 register to 0 (chain transfers disabled).

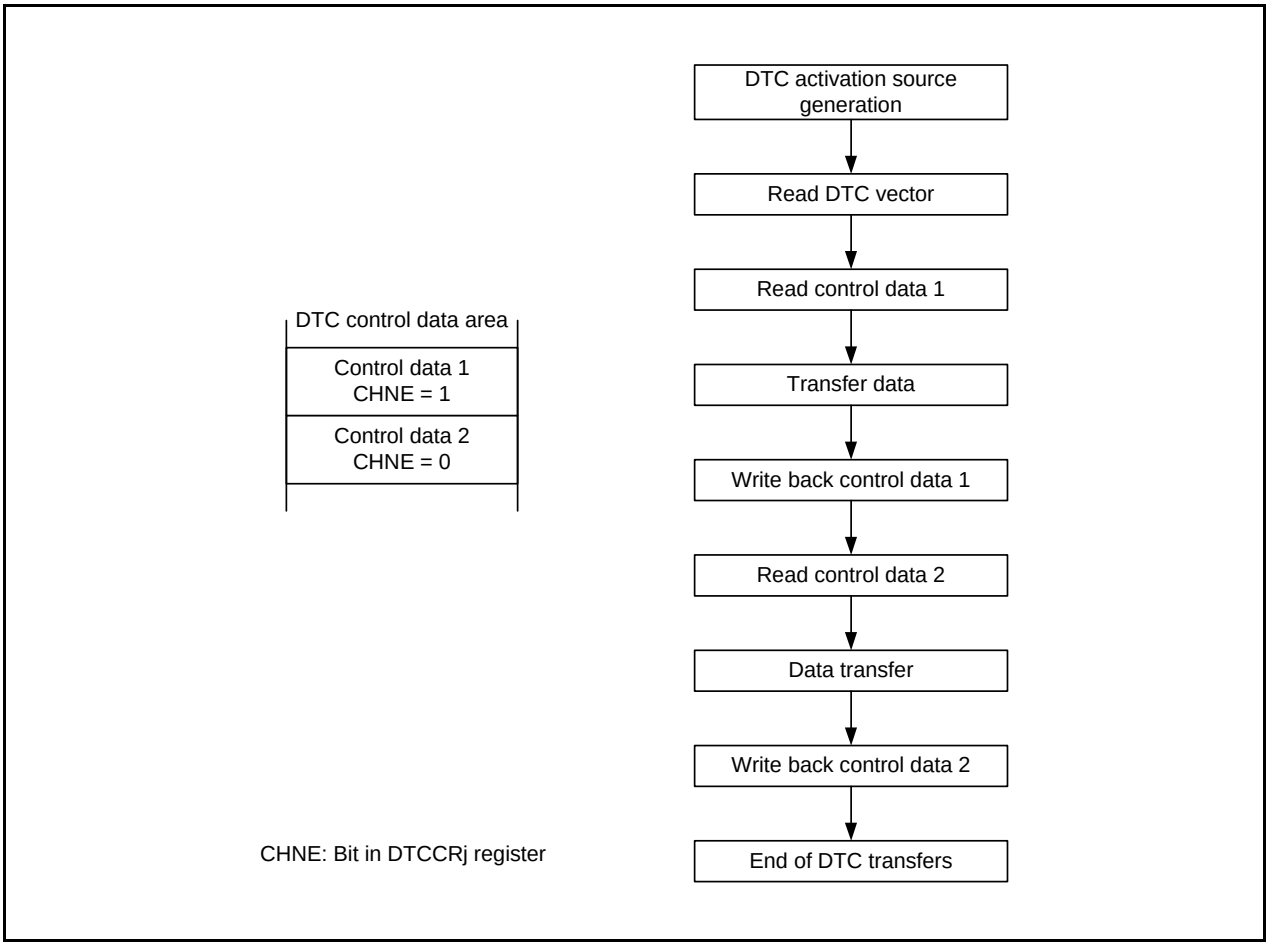


Figure 15.10 Flow of Chain Transfers

15.3.7 Interrupt Sources

When the data transfer causing the DTCCTj (j = 0 to 23) register value to change to 0 is performed in normal mode, and when the data transfer causing the DTCCTj register value to change to 0 is performed while the RPTINT bit in the DTCCRj register is 1 (interrupt generation enabled) in repeat mode, the interrupt request corresponding to the activation source is generated for the CPU during DTC operation. However, no interrupt request is generated for the CPU when the activation source is SSU/I^2C bus transmit data empty or flash ready status.
Interrupt requests for the CPU are affected by the I flag or interrupt control register. In chain transfers, whether the interrupt request is generated or not is determined either by the number of transfer times specified for the first type of the transfer or the RPTINT bit. When an interrupt request is generated for the CPU, the bit among bits DTCENi0 to DTCENi7 in the DTCENi (i = 0 to 3, 6) registers corresponding to the activation source are set to 0 (activation disabled).

15.3.8 Operation Timings

The DTC requires five clock cycles to read control data allocated in the DTC control data area. The number of clock cycles required to write back control data differs depending on the control data settings.
Figure 15.11 shows an Example of DTC Operation Timings and Figure 15.12 shows an Example of DTC Operation Timings in Chain Transfers.
Table 15.8 shows the Specifications of Control Data Write-Back Operation.

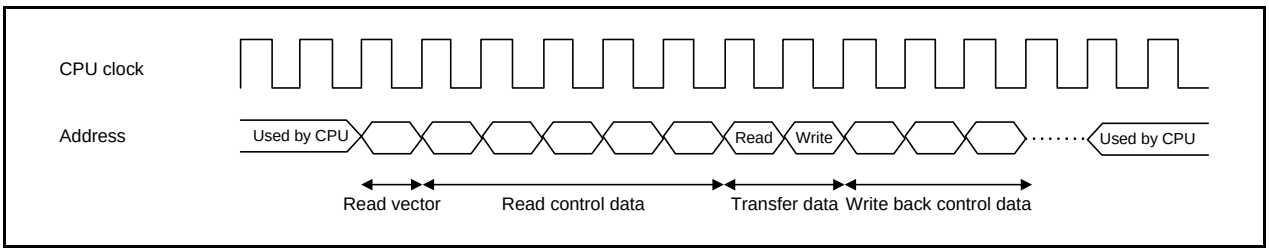


Figure 15.11 Example of DTC Operation Timings

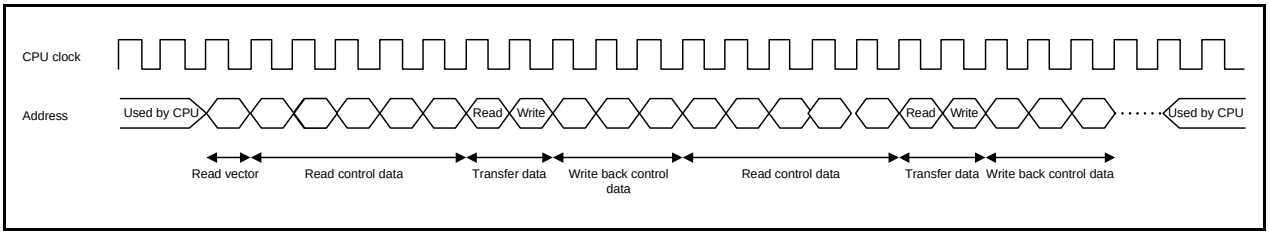


Figure 15.12 Example of DTC Operation Timings in Chain Transfers

Table 15.8 Specifications of Control Data Write-Back Operation

Bits b3 to b0 in DTCCR Register	Operating Mode	Address Control		Control Data to be Written Back				Number of Clock Cycles
		Source	Destination	DTCCTj Register	DTRLDj Register	DTSARj Register	DTDARj Register	
00X0b	Normal mode	Fixed	Fixed	Written back	Written back	Not written back	Not written back	1
01X0b		Incremented	Fixed	Written back	Written back	Written back	Not written back	2
10X0b		Fixed	Incremented	Written back	Written back	Not written back	Written back	2
11X0b		Incremented	Incremented	Written back	Written back	Written back	Written back	3
0X11b	Repeat mode	Repeat area	Fixed	Written back	Written back	Written back	Not written back	2
1X11b			Incremented	Written back	Written back	Written back	Written back	3
X001b		Fixed	Repeat area	Written back	Written back	Not written back	Written back	2
X101b		Incremented		Written back	Written back	Written back	Written back	3

j = 0 to 23
X: 0 or 1

15.3.9 Number of DTC Execution Cycles

Table 15.9 shows the Operations Following DTC Activation and Required Number of Cycles for each operation.
Table 15.10 shows the Number of Clock Cycles Required for Data Transfers.

Table 15.9 Operations Following DTC Activation and Required Number of Cycles

Vector Read	Control Data		Data Read	Data Write	Internal Operation
	Read	Write-back			
1	5	(Note 2)	(Note 1)	(Note 1)	1

Notes:
1. For the number of clock cycles required for data read/write, refer to **Table 15.10 Number of Clock Cycles Required for Data Transfers**.
2. For the number of clock cycles required for control data write-back, refer to **Table 15.8 Specifications of Control Data Write-Back Operation**.

Data is transferred as described below, when the DTBLSj (j = 0 to 23) register = N,
(1) When N = 2n (even), two-byte transfers are performed n times.
(2) When N = 2n + 1 (odd), two-byte transfers are performed n times followed by one time of one-byte transfer.

Table 15.10 Number of Clock Cycles Required for Data Transfers

Operation	Unit of Transfers	Internal RAM (During DTC Transfers)		Internal ROM (Program ROM)	Internal ROM (Data flash)	SFR (Word Access)		SFR (Byte Access)	SFR (DTC control data area)	
		Even Address	Odd Address			Even Address	Odd Address		Even Address	Odd Address
Data read	1-byte SK1	1		1	2	2		2	1	
	2-byte SK2	1	2	2	4	2	4	4	1	2
Data write	1-byte SL1	1		—	—	2		2	1	
	2-byte SL2	1	2	—	—	2	4	4	1	2

From Tables 15.9 and 15.10, the total number of required execution cycles can be obtained by the following formula:

Number of required execution cycles = 1 + Σ[formula A] + 2
Σ: Sum of the cycles for the number of transfer times performed by one activation source ([the number of transfer times for which CHNE is set to 1] + 1)

(1) For N = 2n (even)
Formula A = J + n • SK2 + n • SL2
(2) For N = 2n+1 (odd)
Formula A = J + n • SK2 + 1 • SK1 + n • SL2 + 1 • SL1
J: Number of cycles required to read control data (5 cycles) + number of cycles required to write back control data

To read data from or write data to the register that to be accessed in 16-bit units, set an even value of 2 or greater to the DTBLSj (j = 0 to 23) register.
The DTC performs accesses in 16-bit units.

15.3.10 DTC Activation Source Acknowledgement and Interrupt Source Flags

15.3.10.1 Interrupt Sources Except for Flash Memory, Timer RC, and Synchronous Serial Communication Unit (SSU)/I²C bus

When the DTC activation source is an interrupt source except for the flash memory, timer RC, or the synchronous serial communication unit/I²C bus, the same DTC activation source cannot be acknowledged for 8 to 12 cycles of the CPU clock after the interrupt source is generated. If an interrupt source is generated when a software command is executed, the same DTC activation source cannot be acknowledged for 9 to 16 cycles of the CPU clock. If a DTC activation source is generated during DTC operation and acknowledged, the same DTC activation source cannot be acknowledged for 8 to 12 cycles of the CPU clock on completion of the DTC transfer immediately before the DTC is activated by the source. When a software command is executed on completion of the DTC transfer immediately before the DTC is activated, the same DTC activation source cannot be acknowledged for 16 cycles of the CPU clock.

15.3.10.2 Flash Memory

When the DTC activation source is flash ready status, even if a flash ready status interrupt request is generated, it is not acknowledged as the DTC activation source after the RDYSTI bit in the FST register is set to 1 (flash ready status interrupt request) and before the DTC sets the RDYSTI bit to 0 (no flash ready status interrupt request). If a flash ready status interrupt request is generated after the DTC sets the RDYSTI bit to 0, the DTC acknowledges it as the activation source. 8 to 12 cycles of the CPU clock are required after the RDYSTI bit is set to 1 and before the DTC sets the interrupt request flag to 0. If a flash ready status interrupt is generated when a software command is executed, 9 to 16 cycles of the CPU clock are required before the DTC sets the interrupt source flag to 0. If a flash ready status interrupt request is generated during DTC operation and acknowledged as the DTC activation source, the RDYSTI bit is set to 0 after 8 to 12 cycles of the CPU clock on completion of the DTC transfer immediately before the DTC is activated by the source. When a software command is executed on completion of the DTC transfer immediately before the DTC is activated, the RDYSTI bit is set to 0 after 16 cycles of the CPU clock.

15.3.10.3 Timer RC

When the DTC activation source is an interrupt source for timer RC, even if an input capture/compare match in individual timers occurs, it is not acknowledged as the DTC activation source after the interrupt source flag is set to 1 and before the DTC sets the flag to 0. If an input capture/compare match occurs after the DTC sets the interrupt source flag to 0, the DTC acknowledges it as the activation source. 8 to 12 cycles of the CPU clock plus 0.5 to 1.5 cycles of the timer operating clock are required after the interrupt source flag is set to 1 and before the DTC sets the flag to 0. If the interrupt request flag is set to 1 when a software command is executed, 9 to 16 cycles of the CPU clock plus 0.5 to 1.5 cycles of the timer operating clock are required before the DTC sets the interrupt source flag to 0. If individual DTC activation sources are generated for timer RC during DTC operation and acknowledged, the interrupt source flag is set to 0 after 8 to 12 cycles of the CPU clock plus 0.5 to 1.5 cycles of the timer operating clock on completion of the DTC transfer immediately before the DTC is activated by the source. When a software command is executed on completion of the DTC transfer immediately before the DTC is activated, the interrupt source flag is set to 0 after 16 cycles of the CPU clock plus 0.5 to 1.5 cycles of the timer operating clock.

15.3.10.4 SSU/I²C bus Receive Data Full

When the DTC activation source is SSU/I²C bus receive data full, read the SSRDR register/the ICDRR register using a data transfer. The RDRF bit in the SSSR register/the ICSR register is set to 0 (no data in SSRDR/ICDRR register) by reading the SSRDR register/ the ICDRR register. If an interrupt source for receive data full is subsequently generated, the DTC acknowledges it as the activation source.

15.3.10.5 SSU/I²C bus Transmit Data Empty

When the DTC activation source is SSU/I²C bus transmit data empty, write to the SSTDR register/the ICDRT register using a data transfer. The TDRE bit in the SSSR register/the ICSR register is set to 0 (data is not transferred from registers SSTDR/ICDRT to SSTRSR/ICDRS) by writing to the SSTDR register/the ICDRT register. If an interrupt source for transmit data empty is subsequently generated, the DTC acknowledges it as the activation source.

15.4 Notes on DTC

15.4.1 DTC activation source

- Do not generate any DTC activation sources before entering wait mode or during wait mode.
- Do not generate any DTC activation sources before entering stop mode or during stop mode.

15.4.2 DTCENi (i = 0 to 3, 6) Registers

- Modify bits DTCENi0 to DTCENi7 only while an interrupt request corresponding to the bit is not generated.
- When the interrupt source flag in the status register for the peripheral function is 1, do not modify the corresponding activation source bit among bits DTCENi0 to DTCENi7.
- Do not access the DTCENi registers using DTC transfers.

15.4.3 Peripheral Modules

- Do not set the status register bit for the peripheral function to 0 using a DTC transfer.
- When the DTC activation source is SSU/I^{2}C bus receive data full, read the SSRDR register/the ICDRR register using a DTC transfer.
  The RDRF bit in the SSSR register/the ICSR register is set to 0 (no data in SSRDR/ICDRR register) by reading the SSRDR register/the ICDRR register.
  However, the RDRF bit is not set to 0 by reading the SSRDR register/the ICDRR register when the DTC data transfer setting is either of the following:
  - Transfer causing the DTCCTj (j = 0 to 23) register value to change from 1 to 0 in normal mode
  - Transfer causing the DTCCRj register value to change from 1 to 0 while the RPTINT bit in the DTCCRj register is 1 (interrupt generation enabled) in repeat mode.
- When the DTC activation source is SSU/I^{2}C bus transmit data empty, write to the SSTDR register/the ICDRT register using a DTC transfer. The TDRE bit in the SSSR register/the ICSR register is set to 0 (data is not transferred from registers SSTDR/ICDRT to SSTRSR/ICDRS) by writing to the SSTDR register/the ICDRT register.

15.4.4 Interrupt Request

No interrupt is generated for the CPU during DTC operation in any of the following cases:

- When the DTC activation source is SSU/I^{2}C transmit data empty or flash ready status
- When performing the data transfer causing the DTCCTj (j = 0 to 23) register value to change to 0 in normal mode
- When performing the data transfer causing the DTCCRj register value to change to 0 while the RPTINT bit in the DTCCRj register is 1 (interrupt generation enabled) in repeat mode

16. General Overview of Timers

The MCU has two 8-bit timers with 8-bit prescalers and one 16-bit timer. The two 8-bit timers with 8-bit prescalers are timer RA and timer RB. These timers contain a reload register to store the default value of the counter. These three 16-bit timer is timer RC that have input capture and output compare functions. All the timers operate independently. Table 16.1 lists Functional Comparison of Timers.

Table 16.1 Functional Comparison of Timers

Item		Timer RA	Timer RB	Timer RC
Configuration		8-bit timer with 8-bit prescaler (with reload register)	8-bit timer with 8-bit prescaler (with reload register)	16-bit timer (with input capture and output compare)
Count		Decrement	Decrement	Increment
Count sources		• f1 • f2 • f8 • fOCO	• f1 • f2 • f8 • Timer RA underflow	• f1 • f2 • f4 • f8 • f32 • fOCO40M • fOCO-F • TRCCLK
Function	Count of the internal count source	Timer mode	Timer mode	Timer mode (output compare function)
	Count of the external count source	Event counter mode	—	Timer mode (output compare function)
	External pulse width/ period measurement	Pulse width measurement mode, pulse period measurement mode	—	Timer mode (input capture function; 4 pins)
	PWM output	Pulse output mode (1), Event counter mode (1)	Programmable waveform generation mode	Timer mode (output compare function; 4 pins) (1), PWM mode (3 pins), PWM2 mode (1 pin)
	One-shot waveform output	—	Programmable one-shot generation mode, Programmable wait one-shot generation mode	PWM mode (3 pins)
	Three-phase waveforms output	—	—	—
	Timer	—	—	—
Input pin		TRAIO, $\overline{\text{INT2}}$	$\overline{\text{INT0}}$	$\overline{\text{INT0}}$, TRCCLK, TRCTRG, TRCIOA, TRCIOB, TRCIOC, TRCIOD
Output pin		TRAO, TRAIO	TRBO	TRCIOA, TRCIOB, TRCIOC, TRCIOD
Related interrupt		Timer RA interrupt, $\overline{\text{INT2}}$ interrupt	Timer RB interrupt, $\overline{\text{INT0}}$ interrupt	Compare match/input capture A to D interrupt, Overflow interrupt, $\overline{\text{INT0}}$ interrupt
Timer stop		Provided	Provided	Provided

Note:
1. Rectangular waves are output in these modes. Since the waves are inverted at each overflow, the “H” and “L” level widths of the pulses are the same.

17. Timer RA

Timer RA is an 8-bit timer with an 8-bit prescaler.

17.1 Overview

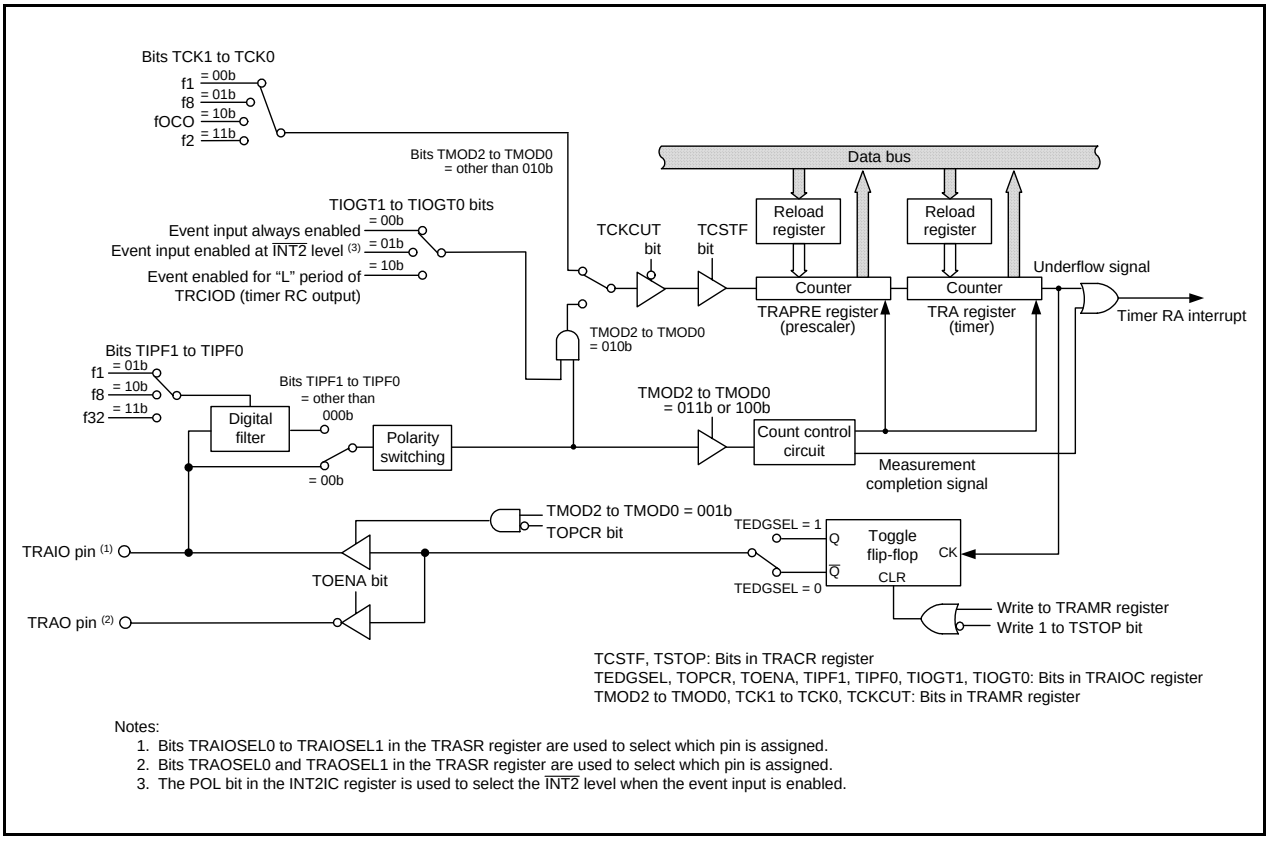
The prescaler and timer each consist of a reload register and counter. The reload register and counter are allocated at the same address, and can be accessed when accessing registers TRAPRE and TRA (refer to **Tables 17.2 to 17.6 the Specifications of Each Mode**).

The count source for timer RA is the operating clock that regulates the timing of timer operations such as counting and reloading.

Figure 17.1 shows a Timer RA Block Diagram. Table 17.1 lists the Pin Configuration of Timer RA.

Timer RA contains the following five operating modes:

- Timer mode — The timer counts the internal count source.
- Pulse output mode — The timer counts the internal count source and outputs pulses which invert the polarity by underflow of the timer.
- Event counter mode — The timer counts external pulses.
- Pulse width measurement mode — The timer measures the pulse width of an external pulse.
- Pulse period measurement mode — The timer measures the pulse period of an external pulse.



Notes:
1. Bits TRAIOSEL0 to TRAIOSEL1 in the TRASR register are used to select which pin is assigned.
2. Bits TRAOSEL0 and TRAOSEL1 in the TRASR register are used to select which pin is assigned.
3. The POL bit in the INT2IC register is used to select the $\overline{INT2}$ level when the event input is enabled.

Figure 17.1 Timer RA Block Diagram

Table 17.1 Pin Configuration of Timer RA

Pin Name	Assigned Pin	I/O	Function
TRAIO	P1_5, or P1_7	I/O	Function differs according to the mode. Refer to descriptions of individual modes for details
TRAO	P3_0, or P3_7	Output	

17.2 Registers

17.2.1 Timer RA Control Register (TRACR)

Address 0100h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	TUNDF	TEDGF	—	TSTOP	TCSTF	TSTART
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART	Timer RA count start bit (1)	0: Count stops 1: Count starts	R/W
b1	TCSTF	Timer RA count status flag (1)	0: Count stops 1: During count	R
b2	TSTOP	Timer RA count forcible stop bit (2)	When this bit is set to 1, the count is forcibly stopped. When read, its content is 0.	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	TEDGF	Active edge judgment flag (3, 4)	0: Active edge not received 1: Active edge received (end of measurement period)	R/W
b5	TUNDF	Timer RA underflow flag (3, 4)	0: No underflow 1: Underflow	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	—			

Notes:
1. Refer to **17.8 Notes on Timer RA** for precautions regarding bits TSTART and TCSTF.
2. When the TSTOP bit is set to 1, bits TSTART and TCSTF and registers TRAPRE and TRA are set to the values after a reset.
3. Bits TEDGF and TUNDF can be set to 0 by writing 0 to these bits by a program. However, their value remains unchanged when 1 is written.
4. Set to 0 in timer mode, pulse output mode, and event counter mode.

In pulse width measurement mode and pulse period measurement mode, use the MOV instruction to set the TRACR register. If it is necessary to avoid changing the values of bits TEDGF and TUNDF, write 1 to them.

17.2.2 Timer RA I/O Control Register (TRAIOC)

Address 0101h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIOGT1	TIOGT0	TIPF1	TIPF0	TIOSEL	TOENA	TOPCR	TEDGSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TEDGSEL	TRAIO polarity switch bit	Function varies according to the operating mode.	R/W
b1	TOPCR	TRAIO output control bit		R/W
b2	TOENA	TRAO output enable bit		R/W
b3	TIOSEL	Hardware LIN function select bit		R/W
b4	TIPF0	TRAIO input filter select bit		R/W
b5	TIPF1			R/W
b6	TIOGT0	TRAIO event input control bit		R/W
b7	TIOGT1			R/W

17.2.3 Timer RA Mode Register (TRAMR)

Address 0102h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TCKCUT	—	TCK1	TCK0	—	TMOD2	TMOD1	TMOD0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TMOD0	Timer RA operating mode select bit	b2 b1 b0 0 0 0: Timer mode 0 0 1: Pulse output mode 0 1 0: Event counter mode 0 1 1: Pulse width measurement mode 1 0 0: Pulse period measurement mode 1 0 1: Do not set. 1 1 0: Do not set. 1 1 1: Do not set.	R/W
b1	TMOD1			R/W
b2	TMOD2			R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	TCK0	Timer RA count source select bit	b5 b4 0 0: f1 0 1: f8 1 0: fOCO 1 1: f2	R/W
b5	TCK1			R/W
b6	—	Reserved bit	Set to 0.	R/W
b7	TCKCUT	Timer RA count source cutoff bit	0: Provides count source 1: Cuts off count source	R/W

When both the TSTART and TCSTF bits in the TRACR register are set to 0 (count stops), rewrite this register.

17.2.4 Timer RA Prescaler Register (TRAPRE)

Address 0103h

Bit	b7	b6	b5	b4	b3	b2	b1	b0	
Symbol	—	—	—	—	—	—	—	—	
After Reset	1	1	1	1	1	1	1	1	(Note 1)

Bit	Mode	Function	Setting Range	R/W
b7 to b0	Timer mode	Counts an internal count source	00h to FFh	R/W
	Pulse output mode		00h to FFh	R/W
	Event counter mode	Counts an external count source	00h to FFh	R/W
	Pulse width measurement mode	Measure pulse width of input pulses from external (counts internal count source)	00h to FFh	R/W
	Pulse period measurement mode	Measure pulse period of input pulses from external (counts internal count source)	00h to FFh	R/W

Note:
1. When the TSTOP bit in the TRACR register is set to 1, the TRAPRE register is set to FFh.

17.2.5 Timer RA Register (TRA)

Address 0104h

Bit	b7	b6	b5	b4	b3	b2	b1	b0	
Symbol	—	—	—	—	—	—	—	—	
After Reset	1	1	1	1	1	1	1	1	(Note 1)

Bit	Mode	Function	Setting Range	R/W
b7 to b0	All modes	Counts on underflow of TRAPRE register	00h to FFh (2)	R/W

Notes:
1. When the TSTOP bit in the TRACR register is set to 1, the TRAPRE register is set to FFh.
2. Do not set 00h to the TRA register in pulse width measurement mode and pulse period measurement mode.

17.2.6 Timer RA Pin Select Register (TRASR)

Address 0180h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	TRAOSEL0	—	TRAIOSEL1	TRAIOSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRAIOSEL0	TRAIO pin select bit	b1 b0 0 0: TRAIO pin not used 0 1: P1_7 assigned 1 0: P1_5 assigned 1 1: Do not set.	R/W
b1	TRAIOSEL1			R/W
b2	—	Reserved bit	Set to 0.	R/W
b3	TRAOSEL0	TRAO pin select bit	0: P3_7 assigned 1: P3_0 assigned	R/W
b4	—	Reserved bit	Set to 0.	R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b6	—			
b7	—			

The TRASR register selects which pin is assigned to the timer RA I/O. To use the I/O pin for timer RA, set this register.
Set the TRASR register before setting the timer RA associated registers. Also, do not change the setting value in this register during timer RA operation.

17.3 Timer Mode

In this mode, the timer counts an internally generated count source (refer to **Table 17.2**).

Table 17.2 Timer Mode Specifications

Item	Specification
Count sources	f1, f2, f8, fOCO
Count operations	• Decrement • When the timer underflows, the contents of the reload register are reloaded and the count is continued.
Divide ratio	1/(n+1)(m+1) n: Value set in TRAPRE register, m: Value set in TRA register
Count start condition	1 (count starts) is written to the TSTART bit in the TRACR register.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRACR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRACR register.
Interrupt request generation timing	When timer RA underflows [timer RA interrupt].
TRAIO pin function	Programmable I/O port
TRAO pin function	Programmable I/O port
Read from timer	The count value can be read by reading registers TRA and TRAPRE.
Write to timer	• When registers TRAPRE and TRA are written while the count is stopped, values are written to both the reload register and counter. • When registers TRAPRE and TRA are written during the count, values are written to the reload register and counter (refer to **17.3.2 Timer Write Control during Count Operation**).

17.3.1 Timer RA I/O Control Register (TRAIOC) in Timer Mode

Address 0101h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIOGT1	TIOGT0	TIPF1	TIPF0	TIOSEL	TOENA	TOPCR	TEDGSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TEDGSEL	TRAIO polarity switch bit	Set to 0 in timer mode.	R/W
b1	TOPCR	TRAIO output control bit		R/W
b2	TOENA	TRAO output enable bit		R/W
b3	TIOSEL	Hardware LIN function select bit	Set to 0. However, set to 1 when the hardware LIN function is used.	R/W
b4	TIPF0	TRAIO input filter select bit	Set to 0 in timer mode.	R/W
b5	TIPF1			R/W
b6	TIOGT0	TRAIO event input control bit		R/W
b7	TIOGT1			R/W

17.3.2 Timer Write Control during Count Operation

Timer RA has a prescaler and a timer (which counts the prescaler underflows). The prescaler and timer each consist of a reload register and a counter. When writing to the prescaler or timer, values are written to both the reload register and counter.

However, values are transferred from the reload register to the counter of the prescaler in synchronization with the count source. In addition, values are transferred from the reload register to the counter of the timer in synchronization with prescaler underflows. Therefore, if the prescaler or timer is written to when count operation is in progress, the counter value is not updated immediately after the WRITE instruction is executed. Figure 17.2 shows an Operating Example of Timer RA when Counter Value is Rewritten during Count Operation.

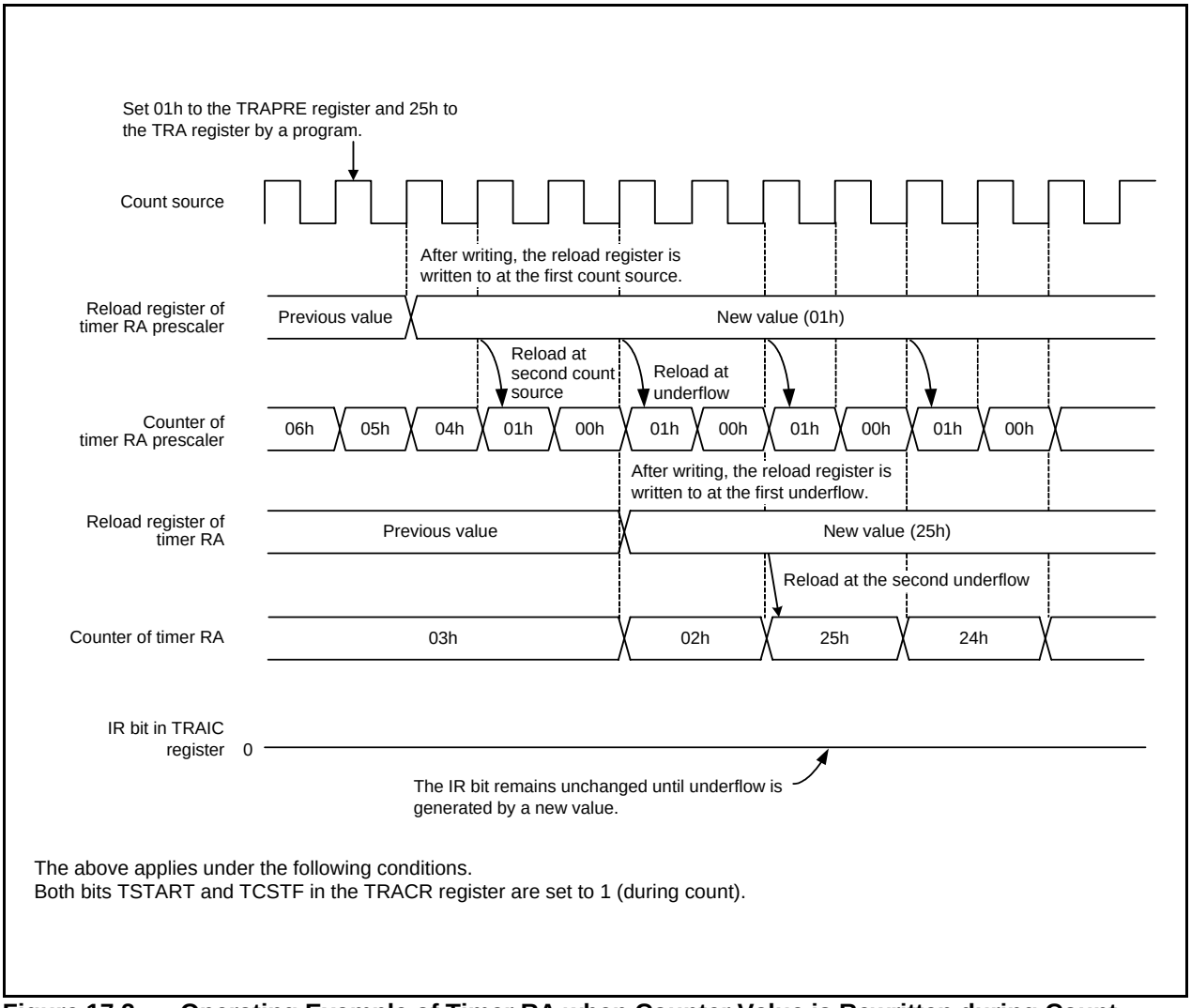


Figure 17.2 Operating Example of Timer RA when Counter Value is Rewritten during Count Operation

17.4 Pulse Output Mode

In pulse output mode, the internally generated count source is counted, and a pulse with inverted polarity is output from the TRAIO pin each time the timer underflows (refer to **Table 17.3**).

Table 17.3 Pulse Output Mode Specifications

Item	Specification
Count sources	f1, f2, f8, fOCO
Count operations	• Decrement • When the timer underflows, the contents in the reload register is reloaded and the count is continued.
Divide ratio	1/(n+1)(m+1) n: Value set in TRAPRE register, m: Value set in TRA register
Count start condition	1 (count starts) is written to the TSTART bit in the TRACR register.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRACR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRACR register.
Interrupt request generation timing	When timer RA underflows [timer RA interrupt].
TRAIO pin function	Pulse output or programmable output port
TRAO pin function	Programmable I/O port or inverted output of TRAIO
Read from timer	The count value can be read by reading registers TRA and TRAPRE.
Write to timer	• When registers TRAPRE and TRA are written while the count is stopped, values are written to both the reload register and counter. • When registers TRAPRE and TRA are written during the count, values are written to the reload register and counter (refer to **17.3.2 Timer Write Control during Count Operation**).
Selectable functions	• TRAIO signal polarity switch function The level when the pulse output starts is selected by the TEDGSEL bit in the TRAIOC register. (1) • TRAO output function Pulses inverted from the TRAIO output polarity can be output from the TRAO pin (selectable by the TOENA bit in the TRAIOC register). • Pulse output stop function Output from the TRAIO pin is stopped by the TOPCR bit in the TRAIOC register. • TRAIO pin select function P1_5, or P1_7 is selected by bits TRAIOSEL0 to TRAIOSEL1 in the TRASR register. • TRAO pin select function P3_0, or P3_7 is selected by TRAOSEL0 bit in the TRASR register.

Note:
1. The level of the output pulse becomes the level when the pulse output starts when the TRAMR register is written to.

17.4.1 Timer RA I/O Control Register (TRAIOC) in Pulse Output Mode

Address 0101h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIOGT1	TIOGT0	TIPF1	TIPF0	TIOSEL	TOENA	TOPCR	TEDGSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TEDGSEL	TRAIO polarity switch bit	0: TRAIO output starts at “H” 1: TRAIO output starts at “L”	R/W
b1	TOPCR	TRAIO output control bit	0: TRAIO output 1: TRAIO output disabled	R/W
b2	TOENA	TRAO output enable bit	0: TRAO output disabled 1: TRAO output (inverted TRAIO output from the port)	R/W
b3	TIOSEL	Hardware LIN function select bit	Set to 0.	R/W
b4	TIPF0	TRAIO input filter select bit	Set to 0 in pulse output mode.	R/W
b5	TIPF1			R/W
b6	TIOGT0	TRAIO event input control bit		R/W
b7	TIOGT1			R/W

17.5 Event Counter Mode

In event counter mode, external signal inputs to the TRAIO pin are counted (refer to **Table 17.4**).

Table 17.4 Event Counter Mode Specifications

Item	Specification
Count source	External signal which is input to TRAIO pin (active edge selectable by a program)
Count operations	• Decrement • When the timer underflows, the contents of the reload register are reloaded and the count is continued.
Divide ratio	1/(n+1)(m+1) n: setting value of TRAPRE register, m: setting value of TRA register
Count start condition	1 (count starts) is written to the TSTART bit in the TRACR register.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRACR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRACR register.
Interrupt request generation timing	When timer RA underflows [timer RA interrupt].
TRAIO pin function	Count source input
TRAO pin function	Programmable I/O port or pulse output (1)
Read from timer	The count value can be read by reading registers TRA and TRAPRE.
Write to timer	• When registers TRAPRE and TRA are written while the count is stopped, values are written to both the reload register and counter. • When registers TRAPRE and TRA are written during the count, values are written to the reload register and counter (refer to **17.3.2 Timer Write Control during Count Operation**).
Selectable functions	• TRAIO input polarity switch function The active edge of the count source is selected by the TEDGSEL bit in the TRAIOC register. • Count source input pin select function P1_5, or P1_7 is selected by bits TRAIOSEL0 to TRAIOSEL1 in the TRASR register. • Pulse output function Pulses of inverted polarity can be output from the TRAO pin each time the timer underflows (selectable by the TOENA bit in the TRAIOC register). (1) • TRAO pin select function P3_0, or P3_7 is selected by TRAOSEL0 bit in the TRASR register. • Digital filter function Whether enabling or disabling the digital filter and the sampling frequency is selected by bits TIPF0 and TIPF1 in the TRAIOC register. • Event input control function The enabled period for the event input to the TRAIO pin is selected by bits TIOGT0 and TIOGT1 in the TRAIOC register.

Note:
1. The level of the output pulse becomes the level when the pulse output starts when the TRAMR register is written to.

17.5.1 Timer RA I/O Control Register (TRAIOC) in Event Counter Mode

Address 0101h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIOGT1	TIOGT0	TIPF1	TIPF0	TIOSEL	TOENA	TOPCR	TEDGSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TEDGSEL	TRAIO polarity switch bit	0: Starts counting at rising edge of the TRAIO input and TRAO starts output at “L” 1: Starts counting at falling edge of the TRAIO input and TRAO starts output at “H”	R/W
b1	TOPCR	TRAIO output control bit	Set to 0 in event counter mode.	R/W
b2	TOENA	TRAO output enable bit	0: TRAO output disabled 1: TRAO output	R/W
b3	TIOSEL	Hardware LIN function select bit	Set to 0.	R/W
b4	TIPF0	TRAIO input filter select bit (1)	b5 b4 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b5	TIPF1			R/W
b6	TIOGT0	TRAIO event input control bit	b7 b6 0 0: Event input always enabled 0 1: Event input enabled at INT2 level (2) 1 0: Event input enabled for “L” period of TRCIOD (timer RC output) 1 1: Do not set.	R/W
b7	TIOGT1			R/W

Notes:
1. When the same value from the TRAIO pin is sampled three times continuously, the input is determined.
2. Make the following settings to use event input enabled at INT2 level:
   - Set the INT2EN bit in the INTEN register to 1 (INT2 input enabled) and the INT2PL bit to 0 (one edge).
   - Set the INT2 polarity by the POL bit in the INT2IC register.
     When the POL bit is set 0 (falling edge selected), the event input for the INT2 high-level period is enabled.
     When the POL bit is set 1 (rising edge selected), the event input for the INT2 low-level period is enabled.
   - Set the PD6_6 bit in the PD6 register for the port assigned as the INT2 pin to 0 (input mode).
   - Select the INT2 digital filter by bits INT2F1 to INT2F0 in the INTF register.

   The IR bit in the INT2IC register is set to 1 (interrupt requested) in accordance with the setting of the POL bit in the INT2IC register and the INT2PL bit in the INTEN register, and a change in the INT2 pin input (refer to **11.8 Notes on Interrupts**).
   For details on interrupts, refer to **11. Interrupts**.

17.6 Pulse Width Measurement Mode

In pulse width measurement mode, the pulse width of an external signal input to the TRAIO pin is measured (refer to **Table 17.5**).
Figure 17.3 shows an Operating Example of Pulse Width Measurement Mode.

Table 17.5 Pulse Width Measurement Mode Specifications

Item	Specification
Count sources	f1, f2, f8, fOCO
Count operations	• Decrement • Continuously counts the selected signal only when measurement pulse is “H” level, or conversely only “L” level. • When the timer underflows, the contents of the reload register are reloaded and the count is continued.
Count start condition	1 (count starts) is written to the TSTART bit in the TRACR register.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRACR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRACR register.
Interrupt request generation timing	• When timer RA underflows [timer RA interrupt]. • Rising or falling of the TRAIO input (end of measurement period) [timer RA interrupt]
TRAIO pin function	Measured pulse input
TRAO pin function	Programmable I/O port
Read from timer	The count value can be read by reading registers TRA and TRAPRE.
Write to timer	• When registers TRAPRE and TRA are written while the count is stopped, values are written to both the reload register and counter. • When registers TRAPRE and TRA are written during the count, values are written to the reload register and counter (refer to **17.3.2 Timer Write Control during Count Operation**).
Selectable functions	• Measurement level setting The “H” level or “L” level period is selected by the TEDGSEL bit in the TRAIOC register. • Measured pulse input pin select function P1_5, or P1_7 is selected by bits TRAIOSEL0 to TRAIOSEL1 in the TRASR register. • Digital filter function Whether enabling or disabling the digital filter and the sampling frequency is selected by bits TIPF0 and TIPF1 in the TRAIOC register.

17.6.1 Timer RA I/O Control Register (TRAIOC) in Pulse Width Measurement Mode

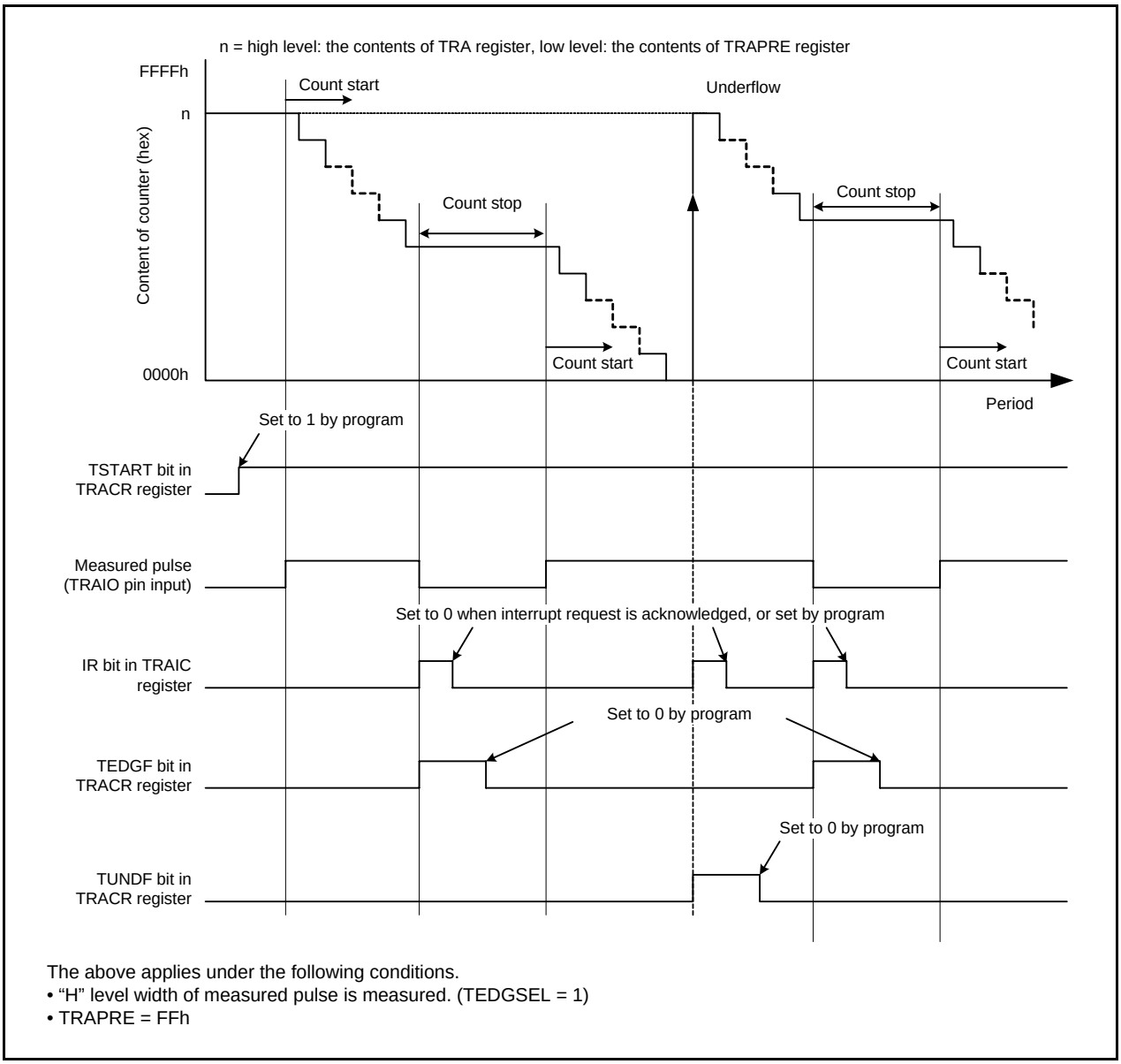
Address 0101h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIOGT1	TIOGT0	TIPF1	TIPF0	TIOSEL	TOENA	TOPCR	TEDGSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TEDGSEL	TRAIO polarity switch bit	0: TRAIO input starts at “L” 1: TRAIO input starts at “H”	R/W
b1	TOPCR	TRAIO output control bit	Set to 0 in pulse width measurement mode.	R/W
b2	TOENA	TRAO output enable bit		R/W
b3	TIOSEL	Hardware LIN function select bit	Set to 0. However, set to 1 when the hardware LIN function is used.	R/W
b4	TIPF0	TRAIO input filter select bit (1)	b5 b4 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b5	TIPF1			R/W
b6	TIOGT0	TRAIO event input control bit	Set to 0 in pulse width measurement mode.	R/W
b7	TIOGT1			R/W

Note:
1. When the same value from the TRAIO pin is sampled three times continuously, the input is determined.

17.6.2 Operating Example



The above applies under the following conditions.
- "H" level width of measured pulse is measured. (TEDGSEL = 1)
- TRAPRE = FFh

Figure 17.3 Operating Example of Pulse Width Measurement Mode

17.7 Pulse Period Measurement Mode

In pulse period measurement mode, the pulse period of an external signal input to the TRAIO pin is measured (refer to **Table 17.6 Pulse Period Measurement Mode Specifications**).
Figure 17.4 shows an Operating Example of Pulse Period Measurement Mode.

Table 17.6 Pulse Period Measurement Mode Specifications

Item	Specification
Count sources	f1, f2, f8, fOCO
Count operations	• Decrement • After the active edge of the measured pulse is input, the contents of the read-out buffer are retained at the first underflow of timer RA prescaler. Then timer RA reloads the contents in the reload register at the second underflow of timer RA prescaler and continues counting.
Count start condition	1 (count starts) is written to the TSTART bit in the TRACR register.
Count stop conditions	• 0 (count stops) is written to TSTART bit in the TRACR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRACR register.
Interrupt request generation timing	• When timer RA underflows or reloads [timer RA interrupt]. • Rising or falling of the TRAIO input (end of measurement period) [timer RA interrupt]
TRAIO pin function	Measured pulse input (1)
TRAO pin function	Programmable I/O port
Read from timer	The count value can be read by reading registers TRA and TRAPRE.
Write to timer	• When registers TRAPRE and TRA are written while the count is stopped, values are written to both the reload register and counter. • When registers TRAPRE and TRA are written during the count, values are written to the reload register and counter (refer to **17.3.2 Timer Write Control during Count Operation**).
Selectable functions	• Measurement period selection The measurement period of the input pulse is selected by the TEDGSEL in the TRAIOC register. • Measured pulse input pin select function P1_5, or P1_7 is selected by bits TRAIOSEL0 to TRAIOSEL1 in the TRASR register. • Digital filter function Whether enabling or disabling the digital filter and the sampling frequency is selected by bits TIPF0 and TIPF1 in the TRAIOC register.

Note:
1. Input a pulse with a period longer than twice the timer RA prescaler period. Input a pulse with a longer “H” and “L” width than the timer RA prescaler period. If a pulse with a shorter period is input to the TRAIO pin, the input may be ignored.

17.7.1 Timer RA I/O Control Register (TRAIOC) in Pulse Period Measurement Mode

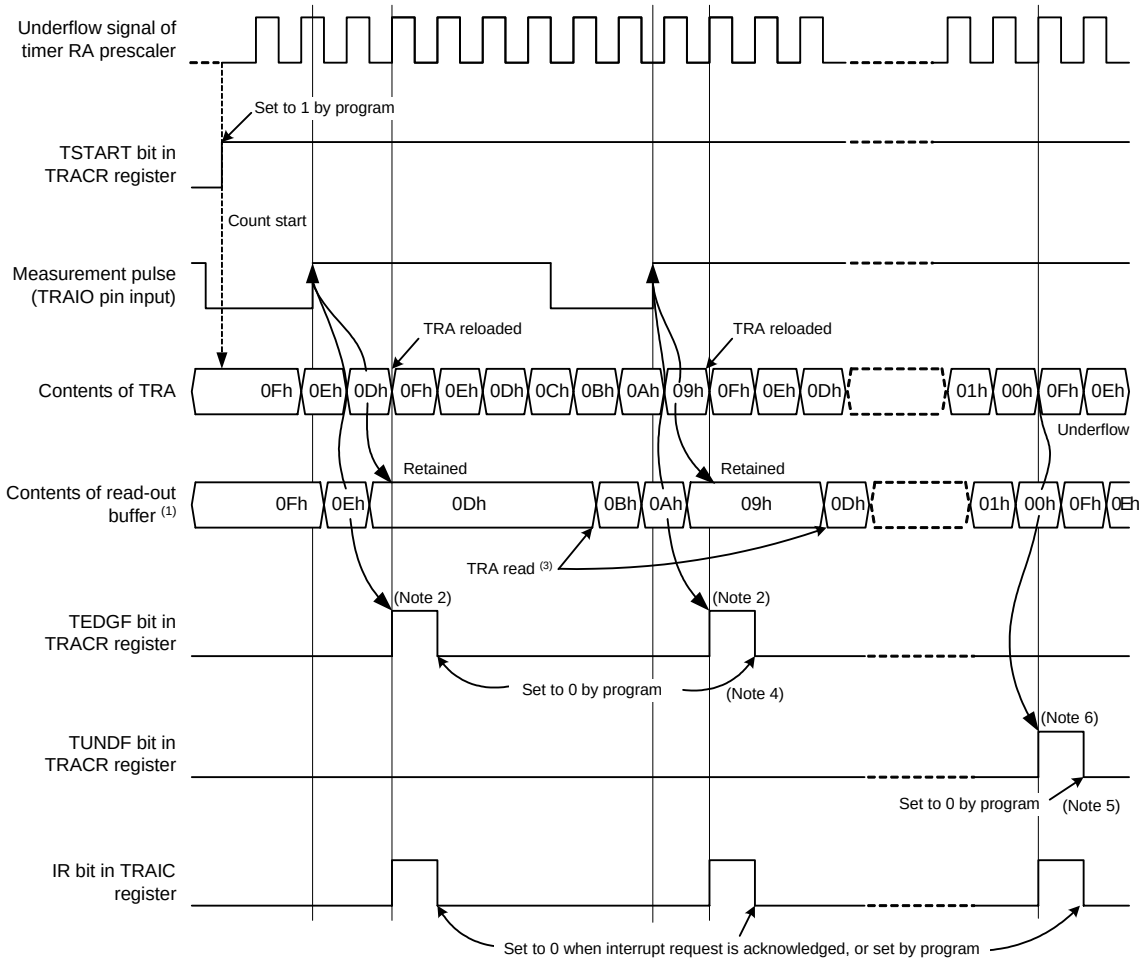
Address 0101h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIOGT1	TIOGT0	TIPF1	TIPF0	TIOSEL	TOENA	TOPCR	TEDGSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TEDGSEL	TRAIO polarity switch bit	0: Measures measurement pulse from one rising edge to next rising edge 1: Measures measurement pulse from one falling edge to next falling edge	R/W
b1	TOPCR	TRAIO output control bit	Set to 0 in pulse period measurement mode.	R/W
b2	TOENA	TRAO output enable bit		R/W
b3	TIOSEL	Hardware LIN function select bit	Set to 0.	R/W
b4	TIPF0	TRAIO input filter select bit (1)	b5 b4 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b5	TIPF1			R/W
b6	TIOGT0	TRAIO event input control bit	Set to 0 in pulse period measurement mode.	R/W
b7	TIOGT1			R/W

Note:
1. When the same value from the TRAIO pin is sampled three times continuously, the input is determined.

17.7.2 Operating Example



Conditions: The period from one rising edge to the next rising edge of the measured pulse is measured (TEDGSEL = 0) with the default value of the TRA register as 0Fh.

Notes:
1. The contents of the read-out buffer can be read by reading the TRA register in pulse period measurement mode.
2. After an active edge of the measured pulse is input, the TEDGF bit in the TRACR register is set to 1 (active edge received) when the timer RA prescaler underflows for the second time.
3. The TRA register should be read before the next active edge is input after the TEDGF bit is set to 1 (active edge received). The contents in the read-out buffer are retained until the TRA register is read. If the TRA register is not read before the next active edge is input, the measured result of the previous period is retained.
4. To set to 0 by a program, use a MOV instruction to write 0 to the TEDGF bit in the TRACR register. At the same time, write 1 to the TUNDF bit in the TRACR register.
5. To set to 0 by a program, use a MOV instruction to write 0 to the TUNDF bit. At the same time, write 1 to the TEDGF bit.
6. Bits TUNDF and TEDGF are both set to 1 if timer RA underflows and reloads on an active edge simultaneously.

Figure 17.4 Operating Example of Pulse Period Measurement Mode

17.8 Notes on Timer RA

- Timer RA stops counting after a reset. Set the values in the timer RA and timer RA prescalers before the count starts.
- Even if the prescaler and timer RA are read out in 16-bit units, these registers are read 1 byte at a time by the MCU. Consequently, the timer value may be updated during the period when these two registers are being read.
- In pulse width measurement mode and pulse period measurement mode, bits TEDGF and TUNDF in the TRACR register can be set to 0 by writing 0 to these bits by a program. However, these bits remain unchanged if 1 is written. When using the READ-MODIFY-WRITE instruction for the TRACR register, the TEDGF or TUNDF bit may be set to 0 although these bits are set to 1 while the instruction is being executed. In this case, write 1 to the TEDGF or TUNDF bit which is not supposed to be set to 0 with the MOV instruction.
- When changing to pulse period measurement mode from another mode, the contents of bits TEDGF and TUNDF are undefined. Write 0 to bits TEDGF and TUNDF before the count starts.
- The TEDGF bit may be set to 1 by the first timer RA prescaler underflow generated after the count starts.
- When using the pulse period measurement mode, leave two or more periods of the timer RA prescaler immediately after the count starts, then set the TEDGF bit to 0.
- The TCSTF bit retains 0 (count stops) for 0 to 1 cycle of the count source after setting the TSTART bit to 1 (count starts) while the count is stopped.

  During this time, do not access registers associated with timer RA (1) other than the TCSTF bit. Timer RA starts counting at the first valid edge of the count source after the TCSTF bit is set to 1 (during count).

  The TCSTF bit remains 1 for 0 to 1 cycle of the count source after setting the TSTART bit to 0 (count stops) while the count is in progress. Timer RA counting is stopped when the TCSTF bit is set to 0.

  During this time, do not access registers associated with timer RA (1) other than the TCSTF bit.

  Note:
  1. Registers associated with timer RA: TRACR, TRAIOC, TRAMR, TRAPRE, and TRA.

- When the TRAPRE register is continuously written during count operation (TCSTF bit is set to 1), allow three or more cycles of the count source clock for each write interval.
- When the TRA register is continuously written during count operation (TCSTF bit is set to 1), allow three or more cycles of the prescaler underflow for each write interval.
- Do not set 00h to the TRA register in pulse width measurement mode and pulse period measurement mode.

18. Timer RB

Timer RB is an 8-bit timer with an 8-bit prescaler.

18.1 Overview

The prescaler and timer each consist of a reload register and counter (refer to **Tables 18.2 to 18.5 the Specifications of Each Mode**). Timer RB has timer RB primary and timer RB secondary as reload registers.
The count source for timer RB is the operating clock that regulates the timing of timer operations such as counting and reloading.
Figure 18.1 shows a Timer RB Block Diagram. Table 18.1 lists the Pin Configuration of Timer RB.

Timer RB has four operation modes listed as follows:

- Timer mode — The timer counts an internal count source (peripheral function clock or timer RA underflows).
- Programmable waveform generation mode — The timer outputs pulses of a given width successively.
- Programmable one-shot generation mode — The timer outputs a one-shot pulse.
- Programmable wait one-shot generation mode — The timer outputs a delayed one-shot pulse.

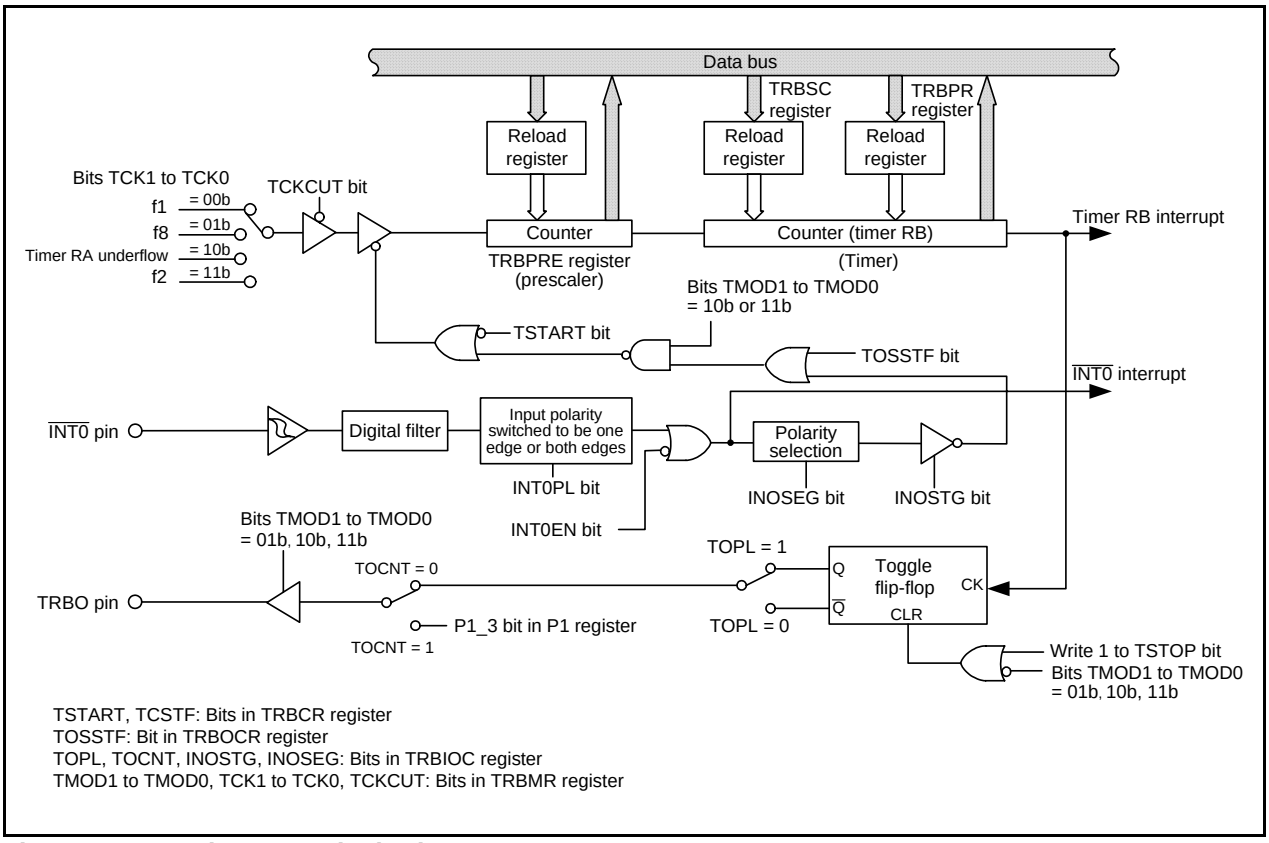


Figure 18.1 Timer RB Block Diagram

Table 18.1 Pin Configuration of Timer RB

Pin Name	Assigned Pin	I/O	Function
TRBO	P1_3	Output	Pulse output (programmable waveform generation mode, programmable one-shot generation mode, programmable wait one-shot generation mode)

18.2 Registers

18.2.1 Timer RB Control Register (TRBCR)

Address 0108h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	TSTOP	TCSTF	TSTART
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART	Timer RB count start bit (1)	0: Count stops 1: Count starts	R/W
b1	TCSTF	Timer RB count status flag (1)	0: Count stops 1: During count (3)	R
b2	TSTOP	Timer RB count forcible stop bit (1, 2)	When this bit is set to 1, the count is forcibly stopped. When read, the content is 0.	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—			
b5	—			
b6	—			
b7	—			

Notes:
1. Refer to **18.7 Notes on Timer RB** for precautions regarding bits TSTART, TCSTF and TSTOP.
2. When the TSTOP bit is set to 1, registers TRBPRE, TRBSC, TRBPR, and bits TSTART and TCSTF, and the TOSSTF bit in the TRBOCR register are set to values after a reset.
3. Indicates that count operation is in progress in timer mode or programmable waveform mode. In programmable one-shot generation mode or programmable wait one-shot generation mode, indicates that a one-shot pulse trigger has been acknowledged.

18.2.2 Timer RB One-Shot Control Register (TRBOCR)

Address 0109h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	TOSSTF	TOSSP	TOSST
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOSST	Timer RB one-shot start bit	When this bit is set to 1, one-shot trigger generated. When read, its content is 0.	R/W
b1	TOSSP	Timer RB one-shot stop bit	When this bit is set to 1, counting of one-shot pulses (including programmable wait one-shot pulses) stops. When read, the content is 0.	R/W
b2	TOSSTF	Timer RB one-shot status flag (1)	0: One-shot stopped 1: One-shot operating (Including wait period)	R
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—			
b5	—			
b6	—			
b7	—			

Note:
1. When 1 is set to the TSTOP bit in the TRBCR register, the TOSSTF bit is set to 0.

This register is enabled when bits TMOD1 to TMOD0 in the TRBMR register is set to 10b (programmable one-shot generation mode) or 11b (programmable wait one-shot generation mode).

18.2.3 Timer RB I/O Control Register (TRBIOC)

Address 010Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	INOSEG	INOSTG	TOCNT	TOPL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOPL	Timer RB output level select bit	Function varies according to the operating mode.	R/W
b1	TOCNT	Timer RB output switch bit		R/W
b2	INOSTG	One-shot trigger control bit		R/W
b3	INOSEG	One-shot trigger polarity select bit		R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

18.2.4 Timer RB Mode Register (TRBMR)

Address 010Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TCKCUT	—	TCK1	TCK0	TWRC	—	TMOD1	TMOD0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TMOD0	Timer RB operating mode select bit (1)	b1 b0 0 0: Timer mode 0 1: Programmable waveform generation mode 1 0: Programmable one-shot generation mode 1 1: Programmable wait one-shot generation mode	R/W
b1	TMOD1			R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	TWRC	Timer RB write control bit (2)	0: Write to reload register and counter 1: Write to reload register only	R/W
b4	TCK0	Timer RB count source select bit (1)	b5 b4 0 0: f1 0 1: f8 1 0: Timer RA underflow (3) 1 1: f2	R/W
b5	TCK1			R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	TCKCUT	Timer RB count source cutoff bit (1)	0: Provides count source 1: Cuts off count source	R/W

Notes:
1. Change bits TMOD1 and TMOD0; TCK1 and TCK0; and TCKCUT when both the TSTART and TCSTF bits in the TRBCR register set to 0 (count stops).
2. The TWRC bit can be set to either 0 or 1 in timer mode. In programmable waveform generation mode, programmable one-shot generation mode, or programmable wait one-shot generation mode, the TWRC bit must be set to 1 (write to reload register only).
3. To use the underflow signal of timer RA as the count source for timer RB, set timer RA in timer mode, pulse output mode, or event count mode.

18.2.5 Timer RB Prescaler Register (TRBPRE)

Address 010Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Mode	Function	Setting Range	R/W
b7 to b0	Timer mode	Counts an internal count source or timer RA underflows	00h to FFh	R/W
	Programmable waveform generation mode		00h to FFh	R/W
	Programmable one-shot generation mode		00h to FFh	R/W
	Programmable wait one-shot generation mode		00h to FFh	R/W

When the TSTOP bit in the TRBCR register is set to 1, the TRBPRE register is set to FFh.

18.2.6 Timer RB Secondary Register (TRBSC)

Address 010Dh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Mode	Function	Setting Range	R/W
b7 to b0	Timer mode	Disabled	00h to FFh	—
	Programmable waveform generation mode	Counts timer RB prescaler underflows (1)	00h to FFh	W (2)
	Programmable one-shot generation mode	Disabled	00h to FFh	—
	Programmable wait one-shot generation mode	Counts timer RB prescaler underflows (one-shot width is counted)	00h to FFh	W (2)

Notes:
1. The values of registers TRBPR and TRBSC are reloaded to the counter alternately and counted.
2. The count value can be read out by reading the TRBPR register even when the secondary period is being counted.

When the TSTOP bit in the TRBCR register is set to 1, the TRBSC register is set to FFh.
To write to the TRBSC register, perform the following steps.
(1) Write the value to the TRBSC register.
(2) Write the value to the TRBPR register. (If the value does not change, write the same value second time.)

18.2.7 Timer RB Primary Register (TRBPR)

Address 010Eh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Mode	Function	Setting Range	R/W
b7 to b0	Timer mode	Counts timer RB prescaler underflows	00h to FFh	R/W
	Programmable waveform generation mode	Counts timer RB prescaler underflows (1)	00h to FFh	R/W
	Programmable one-shot generation mode	Counts timer RB prescaler underflows (one-shot width is counted)	00h to FFh	R/W
	Programmable wait one-shot generation mode	Counts timer RB prescaler underflows (wait period width is counted)	00h to FFh	R/W

Note:
1. The values of registers TRBPR and TRBSC are reloaded to the counter alternately and counted.

When the TSTOP bit in the TRBCR register is set to 1, the TRBPR register is set to FFh.

18.3 Timer Mode

In timer mode, a count source which is internally generated or timer RA underflows are counted (refer to **Table 18.2 Timer Mode Specifications**). Registers TRBOCR and TRBSC are not used in timer mode.

Table 18.2 Timer Mode Specifications

Item	Specification
Count sources	f1, f2, f8, timer RA underflow
Count operations	• Decrement • When the timer underflows, it reloads the reload register contents before the count continues (when timer RB underflows, the contents of timer RB primary reload register is reloaded).
Divide ratio	1/(n+1)(m+1) n: setting value in TRBPRE register, m: setting value in TRBPR register
Count start condition	1 (count starts) is written to the TSTART bit in the TRBCR register.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRBCR register. • 1 (count forcibly stop) is written to the TSTOP bit in the TRBCR register.
Interrupt request generation timing	When timer RB underflows [timer RB interrupt].
TRBO pin function	Programmable I/O port
$\overline{\text{INT0}}$ pin function	Programmable I/O port or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read out by reading registers TRBPR and TRBPRE.
Write to timer	• When registers TRBPRE and TRBPR are written while the count is stopped, values are written to both the reload register and counter. • When registers TRBPRE and TRBPR are written to while count operation is in progress: If the TWRC bit in the TRBMR register is set to 0, the value is written to both the reload register and the counter. If the TWRC bit is set to 1, the value is written to the reload register only (refer to **18.3.2 Timer Write Control during Count Operation**).

18.3.1 Timer RB I/O Control Register (TRBIOC) in Timer Mode

Address 010Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	INOSEG	INOSTG	TOCNT	TOPL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOPL	Timer RB output level select bit	Set to 0 in timer mode.	R/W
b1	TOCNT	Timer RB output switch bit		R/W
b2	INOSTG	One-shot trigger control bit		R/W
b3	INOSEG	One-shot trigger polarity select bit		R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

18.3.2 Timer Write Control during Count Operation

Timer RB has a prescaler and a timer (which counts the prescaler underflows). The prescaler and timer each consist of a reload register and a counter. In timer mode, the TWRC bit in the TRBMR register can be used to select whether writing to the prescaler or timer during count operation is performed to both the reload register and counter or only to the reload register.

However, values are transferred from the reload register to the counter of the prescaler in synchronization with the count source. In addition, values are transferred from the reload register to the counter of the timer in synchronization with prescaler underflows. Therefore, even if the TWRC bit is set for writing to both the reload register and counter, the counter value is not updated immediately after the WRITE instruction is executed. In addition, if the TWRC bit is set for writing to the reload register only, the synchronization of the writing will be shifted if the prescaler value changes. Figure 18.2 shows an Operating Example of Timer RB when Counter Value is Rewritten during Count Operation.

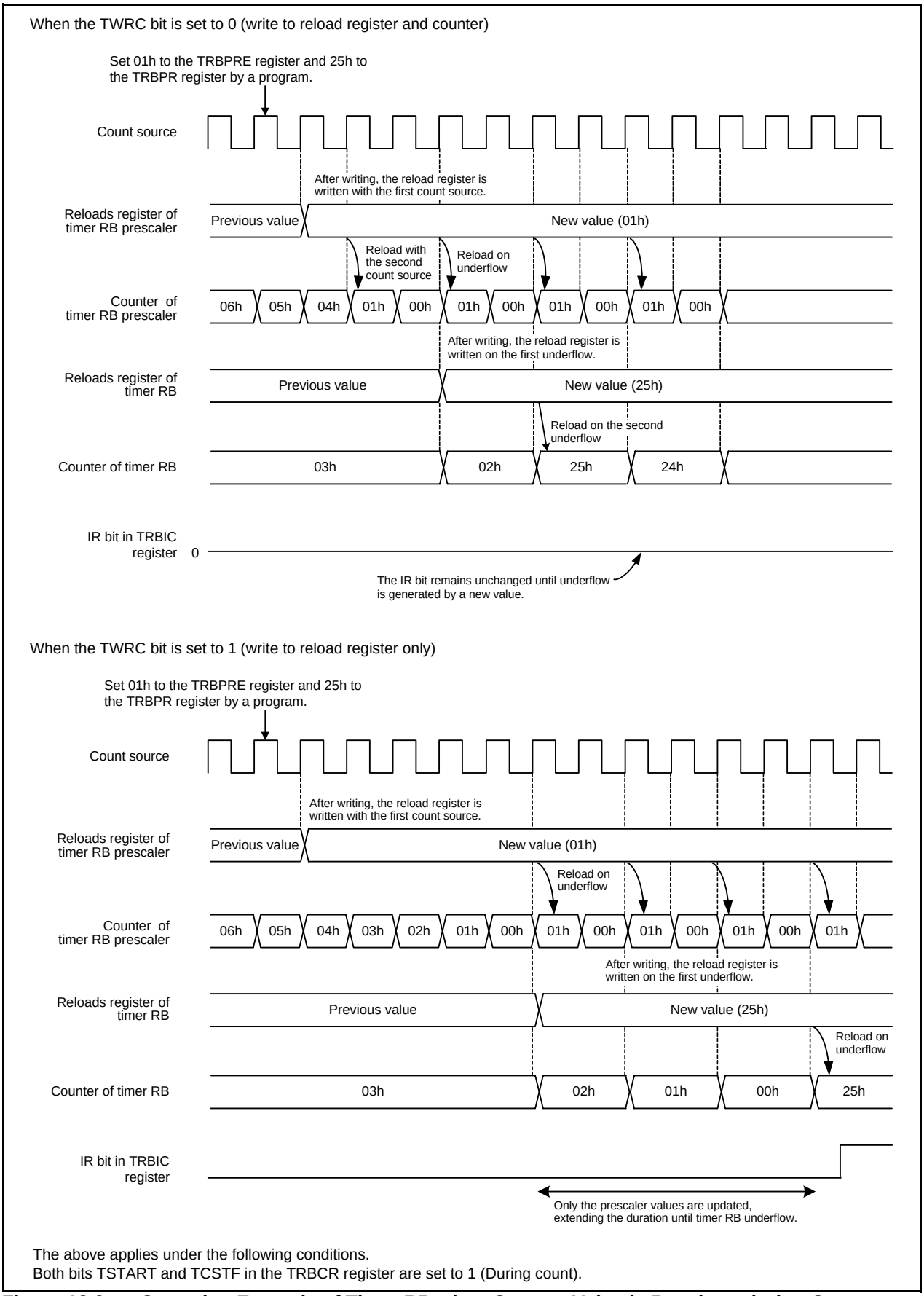


Figure 18.2 Operating Example of Timer RB when Counter Value is Rewritten during Count Operation

18.4 Programmable Waveform Generation Mode

In programmable waveform generation mode, the signal output from the TRBO pin is inverted each time the counter underflows, while the values in registers TRBPR and TRBSC are counted alternately (refer to **Table 18.3 Programmable Waveform Generation Mode Specifications**). Counting starts by counting the setting value in the TRBPR register. The TRBOCR register is unused in this mode.
Figure 18.3 shows an Operating Example of Timer RB in Programmable Waveform Generation Mode.

Table 18.3 Programmable Waveform Generation Mode Specifications

Item	Specification
Count sources	f1, f2, f8, timer RA underflow
Count operations	• Decrement • When the timer underflows, it reloads the contents of the primary reload and secondary reload registers alternately before the count continues.
Width and period of output waveform	Primary period: (n+1)(m+1)/fi Secondary period: (n+1)(p+1)/fi Period: (n+1){(m+1)+(p+1)}/fi fi: Count source frequency n: Value set in TRBPRE register, m: Value set in TRBPR register p: Value set in TRBSC register
Count start condition	1 (count start) is written to the TSTART bit in the TRBCR register.
Count stop conditions	• 0 (count stop) is written to the TSTART bit in the TRBCR register. • 1 (count forcibly stop) is written to the TSTOP bit in the TRBCR register.
Interrupt request generation timing	In half a cycle of the count source, after timer RB underflows during the secondary period (at the same time as the TRBO output change) [timer RB interrupt]
TRBO pin function	Programmable output port or pulse output
$\overline{\text{INT0}}$ pin function	Programmable I/O port or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read out by reading registers TRBPR and TRBPRE. (1)
Write to timer	• When registers TRBPRE, TRBSC, and TRBPR are written while the count is stopped, values are written to both the reload register and counter. • When registers TRBPRE, TRBSC, and TRBPR are written to during count operation, values are written to the reload registers only. (2)
Selectable functions	• Output level select function The output level during primary and secondary periods is selected by the TOPL bit in the TRBIOC register. • TRBO pin output switch function Timer RB pulse output or P1_3 latch output is selected by the TOCNT bit in the TRBIOC register. (3)

Notes:
1. Even when counting the secondary period, the TRBPR register may be read.
2. The set values are reflected in the waveform output beginning with the following primary period after writing to the TRBPR register.
3. The value written to the TOCNT bit is enabled by the following.
   • When counting starts.
   • When a timer RB interrupt request is generated.
   The contents after the TOCNT bit is changed are reflected from the output of the following primary period.

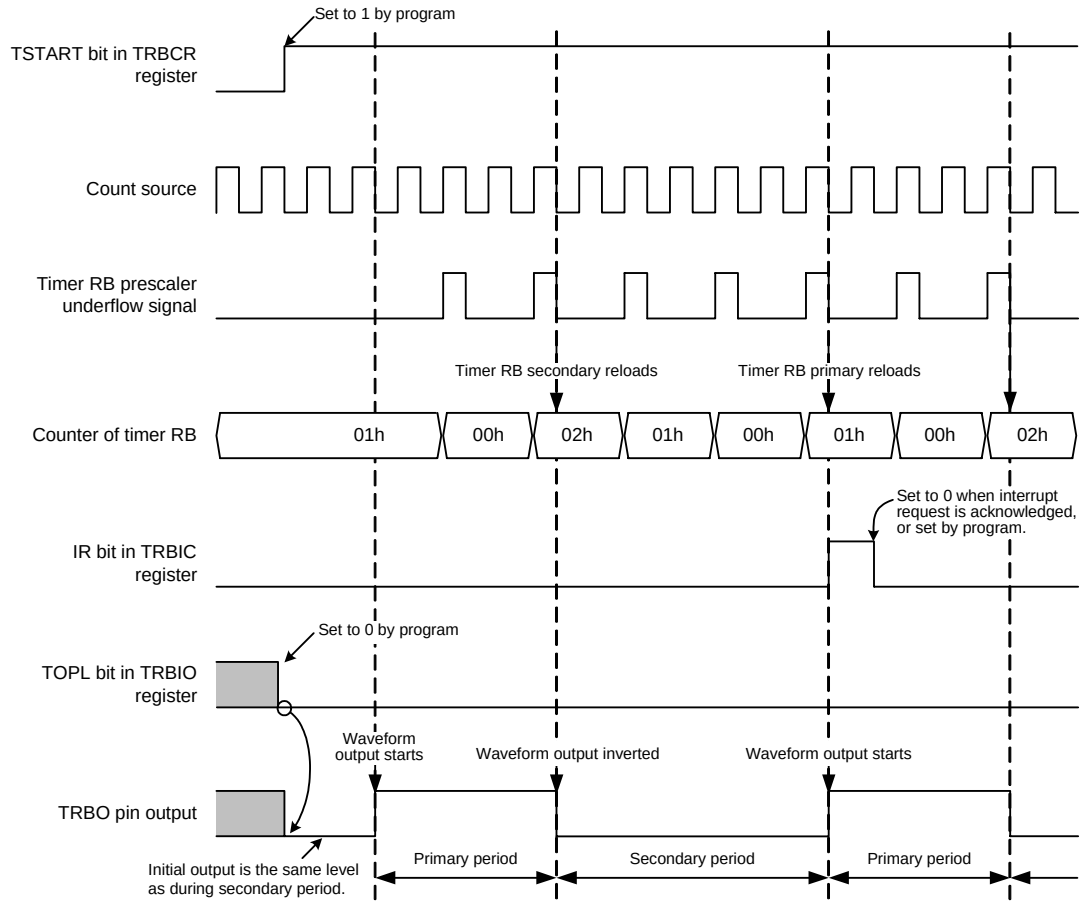
18.4.1 Timer RB I/O Control Register (TRBIOC) in Programmable Waveform Generation Mode

Address 010Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	INOSEG	INOSTG	TOCNT	TOPL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOPL	Timer RB output level select bit	0: Outputs “H” for primary period Outputs “L” for secondary period Outputs “L” when the timer is stopped 1: Outputs “L” for primary period Outputs “H” for secondary period Outputs “H” when the timer is stopped	R/W
b1	TOCNT	Timer RB output switch bit	0: Outputs timer RB waveform 1: Outputs value in P1_3 port register	R/W
b2	INOSTG	One-shot trigger control bit	Set to 0 in programmable waveform generation mode.	R/W
b3	INOSEG	One-shot trigger polarity select bit		R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

18.4.2 Operating Example



The above applies under the following conditions.

TRBPRE = 01h, TRBPR = 01h, TRBSC = 02h
TRBIOC register TOCNT = 0 (timer RB waveform is output from the TRBO pin)

Figure 18.3 Operating Example of Timer RB in Programmable Waveform Generation Mode

18.5 Programmable One-shot Generation Mode

In programmable one-shot generation mode, a one-shot pulse is output from the TRBO pin by a program or an external trigger input (input to the $\overline{\text{INT0}}$ pin) (refer to **Table 18.4 Programmable One-Shot Generation Mode Specifications**). When a trigger is generated, the timer starts operating from the point only once for a given period equal to the set value in the TRBPR register. The TRBSC register is not used in this mode.
Figure 18.4 shows an Operating Example of Programmable One-Shot Generation Mode.

Table 18.4 Programmable One-Shot Generation Mode Specifications

Item	Specification
Count sources	f1, f2, f8, timer RA underflow
Count operations	• Decrement the setting value in the TRBPR register • When the timer underflows, it reloads the contents of the reload register before the count completes and the TOSSTF bit is set to 0 (one-shot stops). • When the count stops, the timer reloads the contents of the reload register before it stops.
One-shot pulse output time	(n+1)(m+1)/fi fi: Count source frequency, n: Setting value in TRBPRE register, m: Setting value in TRBPR register
Count start conditions	• The TSTART bit in the TRBCR register is set to 1 (count starts) and the next trigger is generated • Set the TOSST bit in the TRBOCR register to 1 (one-shot starts) • Input trigger to the $\overline{\text{INT0}}$ pin
Count stop conditions	• When reloading completes after timer RB underflows during primary period • When the TOSSP bit in the TRBOCR register is set to 1 (one-shot stops) • When the TSTART bit in the TRBCR register is set to 0 (stops counting) • When the TSTOP bit in the TRBCR register is set to 1 (forcibly stops counting)
Interrupt request generation timing	In half a cycle of the count source, after the timer underflows (at the same time as the TRBO output ends) [timer RB interrupt]
TRBO pin function	Pulse output
$\overline{\text{INT0}}$ pin functions	• When the INOSTG bit in the TRBIOC register is set to 0 ($\overline{\text{INT0}}$ one-shot trigger disabled): programmable I/O port or $\overline{\text{INT0}}$ interrupt input • When the INOSTG bit in the TRBIOC register is set to 1 ($\overline{\text{INT0}}$ one-shot trigger enabled): external trigger ($\overline{\text{INT0}}$ interrupt input)
Read from timer	The count value can be read out by reading registers TRBPR and TRBPRE.
Write to timer	• When registers TRBPRE and TRBPR are written while the count is stopped, values are written to both the reload register and counter. • When registers TRBPRE and TRBPR are written during the count, values are written to the reload register only (the data is transferred to the counter at the following reload). (1)
Selectable functions	• Output level select function The output level of the one-shot pulse waveform is selected by the TOPL bit in the TRBIOC register. • One-shot trigger select function Refer to **18.5.3 One-Shot Trigger Selection**.

Note:
1. The set value is reflected at the following one-shot pulse after writing to the TRBPR register.

18.5.1 Timer RB I/O Control Register (TRBIOC) in Programmable One-Shot Generation Mode

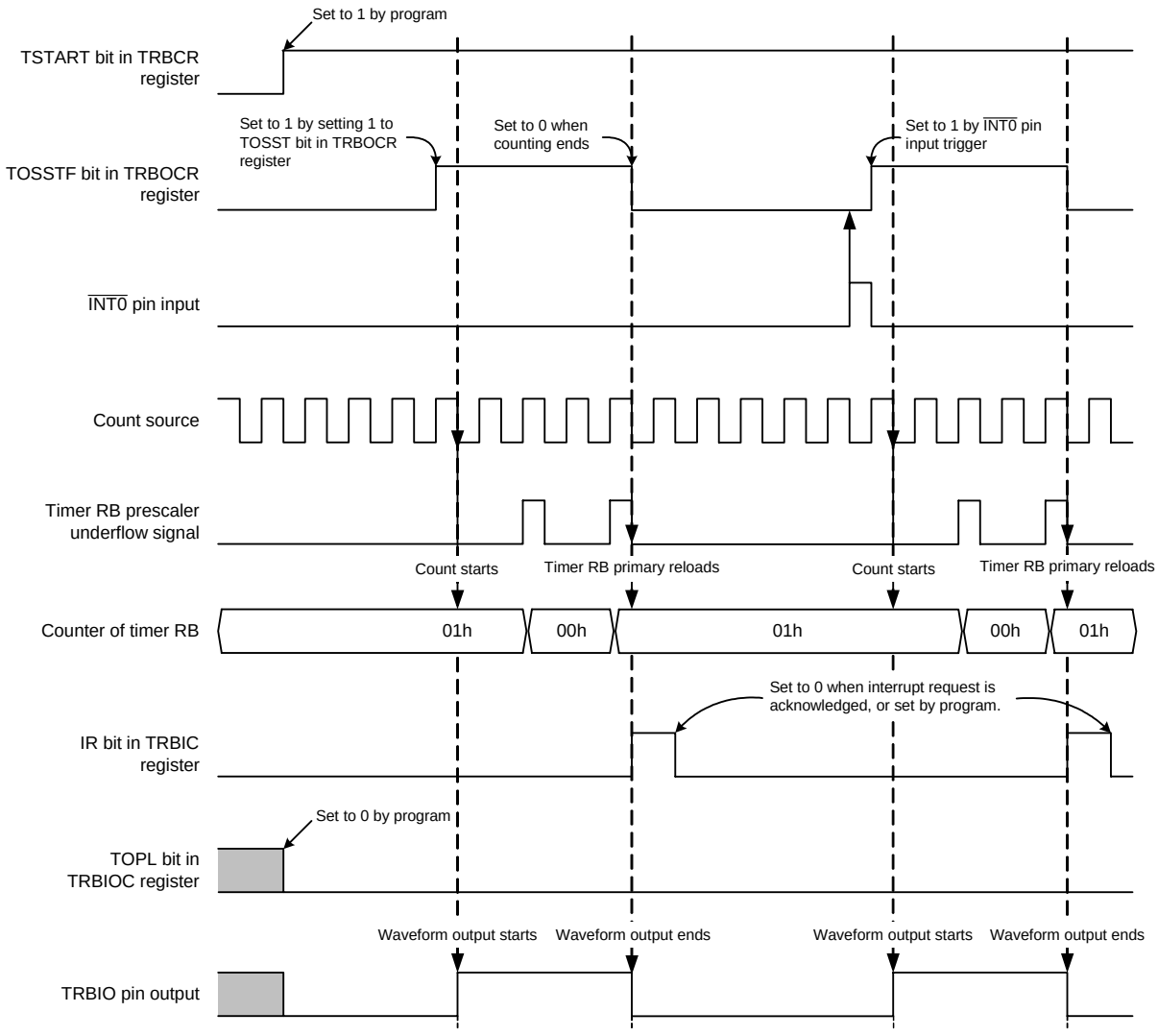
Address 010Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	INOSEG	INOSTG	TOCNT	TOPL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOPL	Timer RB output level select bit	0: Outputs one-shot pulse “H” Outputs “L” when the timer is stopped 1: Outputs one-shot pulse “L” Outputs “H” when the timer is stopped	R/W
b1	TOCNT	Timer RB output switch bit	Set to 0 in programmable one-shot generation mode.	R/W
b2	INOSTG	One-shot trigger control bit (1)	0: $\overline{\text{INT0}}$ pin one-shot trigger disabled 1: $\overline{\text{INT0}}$ pin one-shot trigger enabled	R/W
b3	INOSEG	One-shot trigger polarity select bit (1)	0: Falling edge trigger 1: Rising edge trigger	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

Note:
1. Refer to **18.5.3 One-Shot Trigger Selection**.

18.5.2 Operating Example



The above applies under the following conditions.

TRBPRE = 01h, TRBPR = 01h
TRBIOC register TOPL = 0, TOCNT = 0
INOSTG = 1 (INT0 one-shot trigger enabled)
INOSEG = 1 (edge trigger at rising edge)

Figure 18.4 Operating Example of Programmable One-Shot Generation Mode

18.5.3 One-Shot Trigger Selection

In programmable one-shot generation mode and programmable wait one-shot generation mode, operation starts when a one-shot trigger is generated while the TCSTF bit in the TRBCR register is set to 1 (count starts).
A one-shot trigger can be generated by either of the following causes:

- 1 is written to the TOSST bit in the TRBOCR register by a program.
- Trigger input from the $\overline{\text{INT0}}$ pin.

When a one-shot trigger occurs, the TOSSTF bit in the TRBOCR register is set to 1 (one-shot operation in progress) after one or two cycles of the count source have elapsed. Then, in programmable one-shot generation mode, count operation begins and one-shot waveform output starts. (In programmable wait one-shot generation mode, count operation starts for the wait period.) If a one-shot trigger occurs while the TOSSTF bit is set to 1, no retriggering occurs.

To use trigger input from the $\overline{\text{INT0}}$ pin, input the trigger after making the following settings:

- Set the PD4_5 bit in the PD4 register to 0 (input port).
- Select the $\overline{\text{INT0}}$ digital filter with bits INT0F1 and INT0F0 in the INTF register.
- Select both edges or one edge with the INT0PL bit in INTEN register. If one edge is selected, further select falling or rising edge with the INOSEG bit in TRBIOC register.
- Set the INT0EN bit in the INTEN register to 1 (enabled).
- After completing the above, set the INOSTG bit in the TRBIOC register to 1 ($\overline{\text{INT0}}$ pin one-shot trigger enabled).

Note the following points with regard to generating interrupt requests by trigger input from the $\overline{\text{INT0}}$ pin.

- Processing to handle the interrupts is required. Refer to **11. Interrupts**, for details.
- If one edge is selected, use the POL bit in the INT0IC register to select falling or rising edge. (The INOSEG bit in the TRBIOC register does not affect $\overline{\text{INT0}}$ interrupts).
- If a one-shot trigger occurs while the TOSSTF bit is set to 1, timer RB operation is not affected, but the value of the IR bit in the INT0IC register changes.

18.6 Programmable Wait One-Shot Generation Mode

In programmable wait one-shot generation mode, a one-shot pulse is output from the TRBO pin by a program or an external trigger input (input to the $\overline{\text{INT0}}$ pin) (refer to **Table 18.5 Programmable Wait One-Shot Generation Mode Specifications**). When a trigger is generated from that point, the timer outputs a pulse only once for a given length of time equal to the setting value in the TRBSC register after waiting for a given length of time equal to the setting value in the TRBPR register.
Figure 18.5 shows an Operating Example of Programmable Wait One-Shot Generation Mode.

Table 18.5 Programmable Wait One-Shot Generation Mode Specifications

Item	Specification
Count sources	f1, f2, f8, timer RA underflow
Count operations	• Decrement the timer RB primary setting value. • When a count of the timer RB primary underflows, the timer reloads the contents of timer RB secondary before the count continues. • When a count of the timer RB secondary underflows, the timer reloads the contents of timer RB primary before the count completes and the TOSSTF bit is set to 0 (one-shot stops). • When the count stops, the timer reloads the contents of the reload register before it stops.
Wait time	(n+1)(m+1)/fi fi: Count source frequency n: Value set in the TRBPRE register, m Value set in the TRBPR register
One-shot pulse output time	(n+1)(p+1)/fi fi: Count source frequency n: Value set in the TRBPRE register, p: Value set in the TRBSC register
Count start conditions	• The TSTART bit in the TRBCR register is set to 1 (count starts) and the next trigger is generated. • Set the TOSST bit in the TRBOCR register to 1 (one-shot starts). • Input trigger to the $\overline{\text{INT0}}$ pin
Count stop conditions	• When reloading completes after timer RB underflows during secondary period. • When the TOSSP bit in the TRBOCR register is set to 1 (one-shot stops). • When the TSTART bit in the TRBCR register is set to 0 (starts counting). • When the TSTOP bit in the TRBCR register is set to 1 (forcibly stops counting).
Interrupt request generation timing	In half a cycle of the count source after timer RB underflows during secondary period (complete at the same time as waveform output from the TRBO pin) [timer RB interrupt].
TRBO pin function	Pulse output
$\overline{\text{INT0}}$ pin functions	• When the INOSTG bit in the TRBIOC register is set to 0 ($\overline{\text{INT0}}$ one-shot trigger disabled): programmable I/O port or $\overline{\text{INT0}}$ interrupt input • When the INOSTG bit in the TRBIOC register is set to 1 ($\overline{\text{INT0}}$ one-shot trigger enabled): external trigger ($\overline{\text{INT0}}$ interrupt input)
Read from timer	The count value can be read out by reading registers TRBPR and TRBPRE.
Write to timer	• When registers TRBPRE, TRBSC, and TRBPR are written while the count stops, values are written to both the reload register and counter. • When registers TRBPRE, TRBSC, and TRBPR are written to during count operation, values are written to the reload registers only. (1)
Selectable functions	• Output level select function The output level of the one-shot pulse waveform is selected by the TOPL bit in the TRBIOC register. • One-shot trigger select function Refer to **18.5.3 One-Shot Trigger Selection**.

Note:
1. The set value is reflected at the following one-shot pulse after writing to registers TRBSC and TRBPR.

18.6.1 Timer RB I/O Control Register (TRBIOC) in Programmable Wait One-Shot Generation Mode

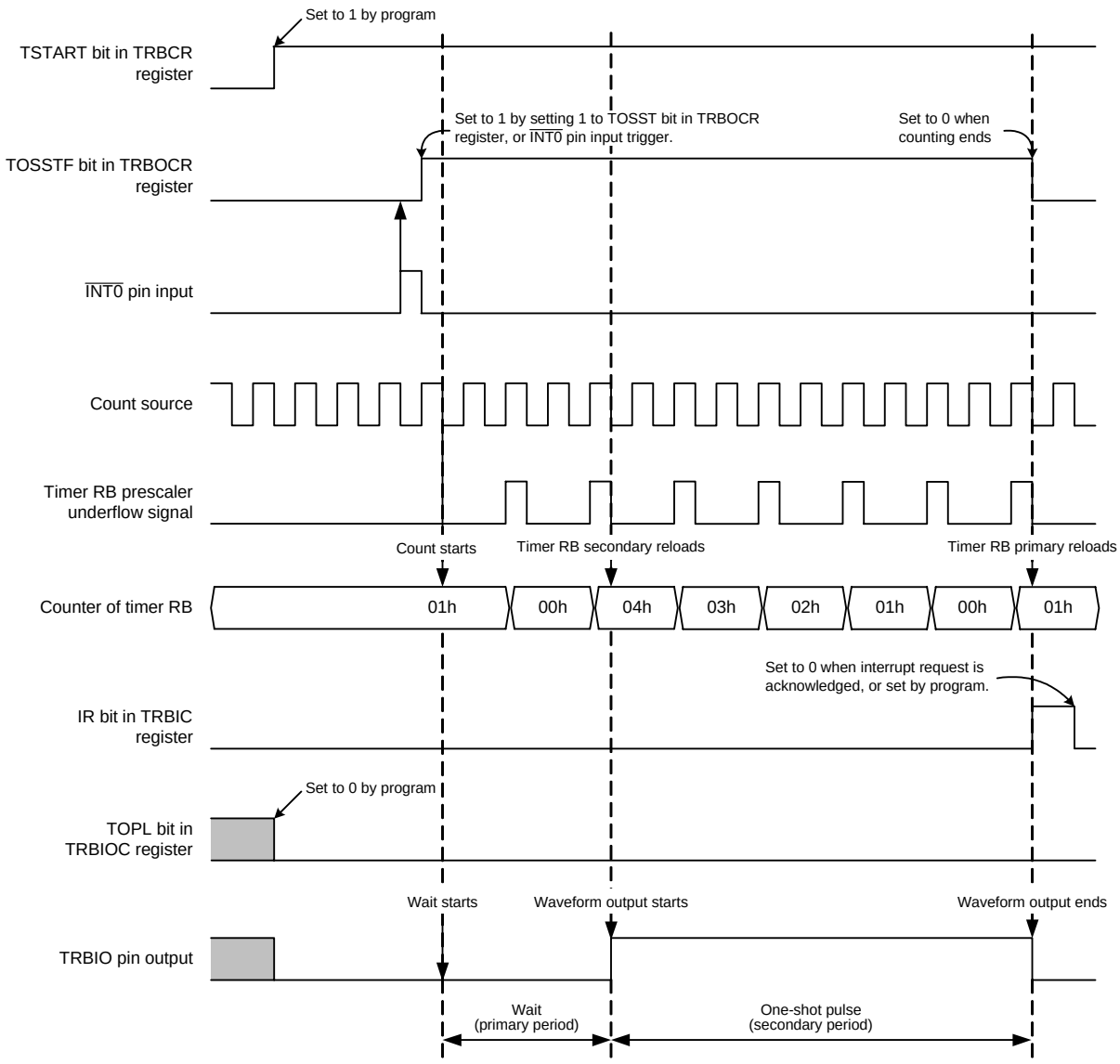
Address 010Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	INOSEG	INOSTG	TOCNT	TOPL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOPL	Timer RB output level select bit	0: Outputs one-shot pulse “H” Outputs “L” when the timer stops or during wait 1: Outputs one-shot pulse “L” Outputs “H” when the timer stops or during wait	R/W
b1	TOCNT	Timer RB output switch bit	Set to 0 in programmable wait one-shot generation mode.	R/W
b2	INOSTG	One-shot trigger control bit (1)	0: $\overline{\text{INT0}}$ pin one-shot trigger disabled 1: $\overline{\text{INT0}}$ pin one-shot trigger enabled	R/W
b3	INOSEG	One-shot trigger polarity select bit (1)	0: Falling edge trigger 1: Rising edge trigger	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

Note:
1. Refer to **18.5.3 One-Shot Trigger Selection**.

18.6.2 Operating Example



The above applies under the following conditions.

TRBPRE = 01h, TRBPR = 01h, TRBSC = 04h
INOSTG = 1 (INT0 one-shot trigger enabled)
INOSEG = 1 (edge trigger at rising edge)

Figure 18.5 Operating Example of Programmable Wait One-Shot Generation Mode

18.7 Notes on Timer RB

- Timer RB stops counting after a reset. Set the values in the timer RB and timer RB prescalers before the count starts.
- Even if the prescaler and timer RB is read out in 16-bit units, these registers are read 1 byte at a time by the MCU. Consequently, the timer value may be updated during the period when these two registers are being read.
- In programmable one-shot generation mode and programmable wait one-shot generation mode, when setting the TSTART bit in the TRBCR register to 0 (stops counting) or setting the TOSSP bit in the TRBOCR register to 1 (stops one-shot), the timer reloads the value of reload register and stops. Therefore, in programmable one-shot generation mode and programmable wait one-shot generation mode, read the timer count value before the timer stops.
- The TCSTF bit remains 0 (count stops) for 1 to 2 cycles of the count source after setting the TSTART bit to 1 (count starts) while the count is stopped.
  During this time, do not access registers associated with timer RB (1) other than the TCSTF bit. Timer RB starts counting at the first valid edge of the count source after the TCSTF bit is set to 1 (during count).
  The TCSTF bit remains 1 for 1 to 2 cycles of the count source after setting the TSTART bit to 0 (count stops) while the count is in progress. Timer RB counting is stopped when the TCSTF bit is set to 0.
  During this time, do not access registers associated with timer RB (1) other than the TCSTF bit.

  Note:
  1. Registers associated with timer RB: TRBCR, TRBOCR, TRBIOC, TRBMR, TRBPRE, TRBSC, and TRBPR.

- If the TSTOP bit in the TRBCR register is set to 1 during timer operation, timer RB stops immediately.
- If 1 is written to the TOSST or TOSSP bit in the TRBOCR register, the value of the TOSSTF bit changes after one or two cycles of the count source have elapsed. If the TOSSP bit is written to 1 during the period between when the TOSST bit is written to 1 and when the TOSSTF bit is set to 1, the TOSSTF bit may be set to either 0 or 1 depending on the content state. Likewise, if the TOSST bit is written to 1 during the period between when the TOSSP bit is written to 1 and when the TOSSTF bit is set to 0, the TOSSTF bit may be set to either 0 or 1.
- To use the underflow signal of timer RA as the count source for timer RB, set timer RA in timer mode, pulse output mode, or event count mode.

18.7.1 Timer Mode

To write to registers TRBPRE and TRBPR during count operation (TCSTF bit in the TRBCR register is set to 1), note the following points:

- When the TRBPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

18.7.2 Programmable Waveform Generation Mode

To write to registers TRBPRE and TRBPR during count operation (TCSTF bit in the TRBCR register is set to 1), note the following points:

- When the TRBPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

18.7.3 Programmable One-shot Generation Mode

To write to registers TRBPRE and TRBPR during count operation (TCSTF bit in the TRBCR register is set to 1), note the following points:

- When the TRBPRE register is written continuously during count operation (TCSTF bit is set to 1), allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously during count operation (TCSTF bit is set to 1), allow three or more cycles of the prescaler underflow for each write interval.

18.7.4 Programmable Wait One-shot Generation Mode

To write to registers TRBPRE and TRBPR during count operation (TCSTF bit in the TRBCR register is set to 1), note the following points:

- When the TRBPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

19. Timer RC

Timer RC is a 16-bit timer with four I/O pins.

19.1 Overview

Timer RC uses either f1, fOCO40M or fOCO-F as its operation clock. Table 19.1 lists the Timer RC Operation Clocks.

Table 19.1 Timer RC Operation Clocks

Condition	Timer RC Operation Clock
Count source is f1, f2, f4, f8, f32, or TRCCLK input (bits TCK2 to TCK0 in TRCCR1 register are set to a value from 000b to 101b)	f1
Count source is fOCO40M (bits TCK2 to TCK0 in TRCCR1 register are set to 110b)	fOCO40M
Count source is fOCO-F (bits TCK2 to TCK0 in TRCCR1 register are set to 111b)	fOCO-F

Table 19.2 lists the Pin Configuration of Timer RC and Figure 19.1 shows a Timer RC Block Diagram.
Timer RC has three modes.

- Timer mode
  - Input capture function — The counter value is captured to a register, using an external signal as the trigger.
  - Output compare function — Matches between the counter and register values are detected. (Pin output state changes when a match is detected.)

The following two modes use the output compare function.

- PWM mode — Pulses of a given width are output continuously.
- PWM2 mode — A one-shot waveform or PWM waveform is output following the trigger after the wait time has elapsed.

Input capture function, output compare function, and PWM mode settings may be specified independently for each pin.
In PWM2 mode waveforms are output based on a combination of the counter or the register.

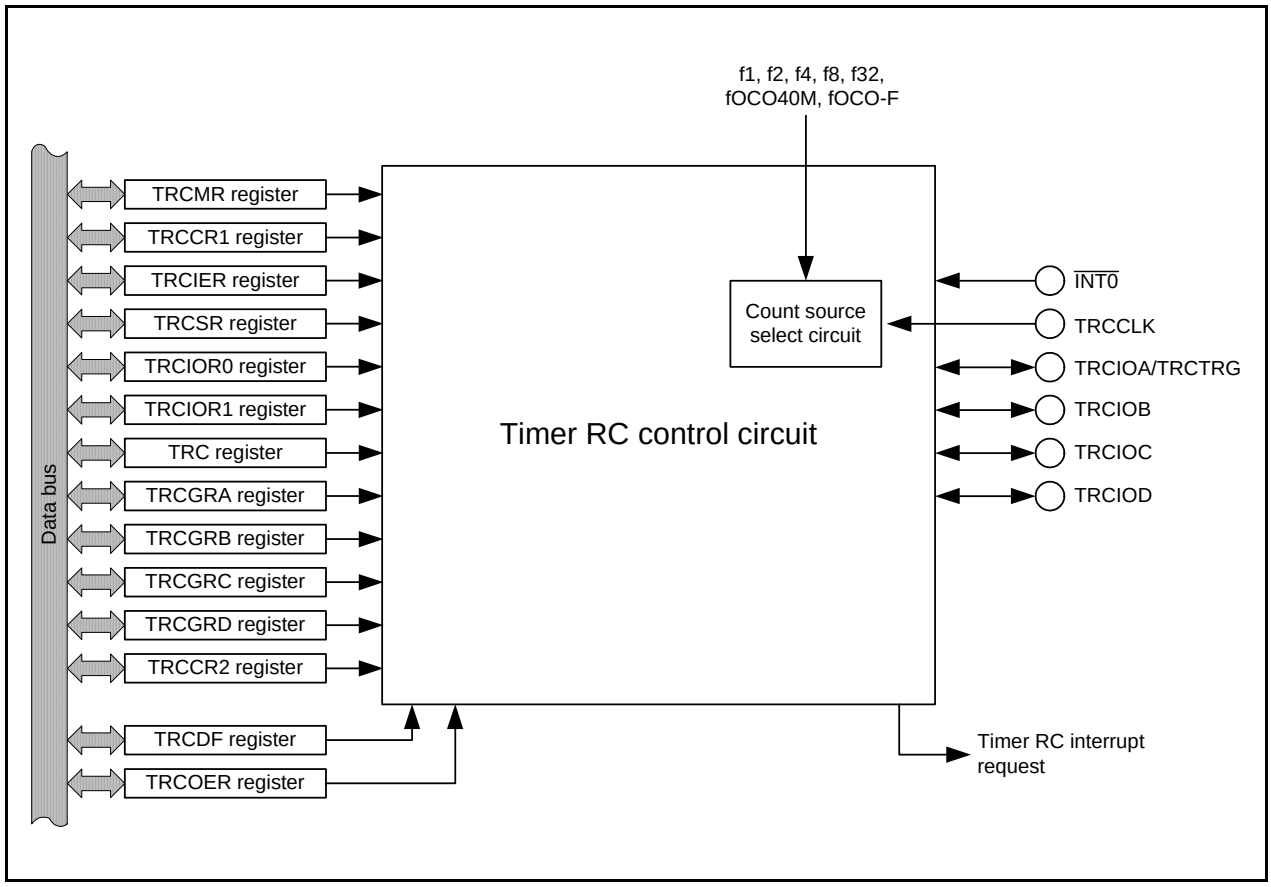


Figure 19.1 Timer RC Block Diagram

Table 19.2 Pin Configuration of Timer RC

Pin Name	Assigned Pin	I/O	Function
TRCIOA	P0_0, P0_1, P0_2, or P1_1	I/O	Function differs according to the mode. Refer to descriptions of individual modes for details.
TRCIOB	P0_3, P0_4, or P1_2		
TRCIOC	P0_7, P1_3, or P3_4		
TRCIOD	P1_0, P3_5, or P6_7		
TRCCLK	P1_4 or P3_3	Input	External clock input
TRCTRG	P0_0, P0_1, P0_2, or P1_1	Input	PWM2 mode external trigger input

19.2 Registers

Table 19.3 lists the Registers Associated with Timer RC.

Table 19.3 Registers Associated with Timer RC

Address	Symbol	Mode				Related Information
		Timer		PWM	PWM2	
		Input Capture Function	Output Compare Function			
0008h	MSTCR	Valid	Valid	Valid	Valid	19.2.1 Module Standby Control Register (MSTCR)
0120h	TRCMR	Valid	Valid	Valid	Valid	19.2.2 Timer RC Mode Register (TRCMR)
0121h	TRCCR1	Valid	Valid	Valid	Valid	Timer RC control register 1 19.2.3 Timer RC Control Register 1 (TRCCR1) 19.5.1 Timer RC Control Register 1 (TRCCR1) for Output Compare Function 19.6.1 Timer RC Control Register 1 (TRCCR1) in PWM Mode 19.7.1 Timer RC Control Register 1 (TRCCR1) in PWM2 Mode
0122h	TRCIER	Valid	Valid	Valid	Valid	19.2.4 Timer RC Interrupt Enable Register (TRCIER)
0123h	TRCSR	Valid	Valid	Valid	Valid	19.2.5 Timer RC Status Register (TRCSR)
0124h	TRCIOR0	Valid	Valid	—	—	Timer RC I/O control register 0, timer RC I/O control register 1 19.2.6 Timer RC I/O Control Register 0 (TRCIOR0) 19.2.7 Timer RC I/O Control Register 1 (TRCIOR1) 19.4.1 Timer RC I/O Control Register 0 (TRCIOR0) for Input Capture Function 19.4.2 Timer RC I/O Control Register 1 (TRCIOR1) for Input Capture Function 19.5.2 Timer RC I/O Control Register 0 (TRCIOR0) for Output Compare Function 19.5.3 Timer RC I/O Control Register 1 (TRCIOR1) for Output Compare Function
0125h	TRCIOR1					
0126h 0127h	TRC	Valid	Valid	Valid	Valid	19.2.8 Timer RC Counter (TRC)
0128h 0129h	TRCGRA	Valid	Valid	Valid	Valid	19.2.9 Timer RC General Registers A, B, C, and D (TRCGRA, TRCGRB, TRCGRC, TRCGRD)
012Ah 012Bh	TRCGRB					
012Ch 012Dh	TRCGRC					
012Eh 012Fh	TRCGRD					
0130h	TRCCR2	—	Valid	Valid	Valid	19.2.10 Timer RC Control Register 2 (TRCCR2)
0131h	TRCDF	Valid	—	—	Valid	19.2.11 Timer RC Digital Filter Function Select Register (TRCDF)
0132h	TRCOER	—	Valid	Valid	Valid	19.2.12 Timer RC Output Master Enable Register (TRCOER)
0133h	TRCADCR (1)	—	Valid	Valid	Valid	19.2.13 Timer RC Trigger Control Register (TRCADCR)
0181h	TRBRCSR	Valid	Valid	Valid	Valid	19.2.14 Timer RC Pin Select Register (TRBRCSR)
0182h	TRCPSR0	Valid	Valid	Valid	Valid	19.2.15 Timer RC Pin Select Register 0 (TRCPSR0)
0183h	TRCPSR1	Valid	Valid	Valid	Valid	19.2.16 Timer RC Pin Select Register 1 (TRCPSR1)

—: Invalid

Note:
1. Not available in the R8C/3MU Group.

19.2.1 Module Standby Control Register (MSTCR)

Address 0008h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	MSTTRC	—	MSTIIC	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	—			
b2	—			
b3	MSTIIC	SSU, I2C bus standby bit	0: Active 1: Standby (1)	R/W
b4	—	Reserved bit	Set to 0.	R/W
b5	MSTTRC	Timer RC standby bit	0: Active 1: Standby (2)	R/W
b6	—	Reserved bit	Set to 0.	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Notes:
1. Stop the SSU and the I2C bus functions before setting to standby. When the MSTIIC bit is set to 1 (standby), any access to the SSU or the I2C bus associated registers (addresses 0193h to 019Dh) is disabled.
2. Stop the timer RC function before setting to standby. When the MSTTRC bit is set to 1 (standby), any access to the timer RC associated registers (addresses 0120h to 0133h (0133h is not available in the R8C/3MU Group)) is disabled.

19.2.2 Timer RC Mode Register (TRCMR)

Address 0120h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TSTART	—	BFD	BFC	PWM2	PWMD	PWMC	PWMB
After Reset	0	1	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PWMB	PWM mode of TRCIOB select bit (1)	0: Timer mode 1: PWM mode	R/W
b1	PWMC	PWM mode of TRCIOC select bit (1)	0: Timer mode 1: PWM mode	R/W
b2	PWMD	PWM mode of TRCIOD select bit (1)	0: Timer mode 1: PWM mode	R/W
b3	PWM2	PWM2 mode select bit	0: PWM 2 mode 1: Timer mode or PWM mode	R/W
b4	BFC	TRCGRC register function select bit (2)	0: General register 1: Buffer register of TRCGRA register	R/W
b5	BFD	TRCGRD register function select bit	0: General register 1: Buffer register of TRCGRB register	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b7	TSTART	TRC count start bit	0: Count stops 1: Count starts	R/W

Notes:
1. These bits are enabled when the PWM2 bit is set to 1 (timer mode or PWM mode).
2. Set the BFC bit to 0 (general register) in PWM2 mode.

For notes on PWM2 mode, refer to **19.9.6 TRCMR Register in PWM2 Mode**.

19.2.3 Timer RC Control Register 1 (TRCCR1)

Address 0121h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CCLR	TCK2	TCK1	TCK0	TOD	TOC	TOB	TOA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOA	TRCIOA output level select bit (1)	Function varies according to the operating mode (function).	R/W
b1	TOB	TRCIOB output level select bit (1)		R/W
b2	TOC	TRCIOC output level select bit (1)		R/W
b3	TOD	TRCIOD output level select bit (1)		R/W
b4	TCK0	Count source select bit (1)	b6 b5 b4 0 0 0: f1 0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: TRCCLK input rising edge 1 1 0: fOCO40M 1 1 1: fOCO-F (2)	R/W
b5	TCK1			R/W
b6	TCK2			R/W
b7	CCLR	TRC counter clear select bit	0: Disable clear (free-running operation) 1: Clear TRC counter by input capture or by compare match in TRCGRA	R/W

Notes:
1. Set to these bits when the TSTART bit in the TRCMR register is set to 0 (count stops).
2. To select fOCO-F, set it to the clock frequency higher than the CPU clock frequency.

19.2.4 Timer RC Interrupt Enable Register (TRCIER)

Address 0122h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	OVIE	—	—	—	IMIED	IMIEC	IMIEB	IMIEA
After Reset	0	1	1	1	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMIEA	Input capture/compare match interrupt enable bit A	0: Disable interrupt (IMIA) by the IMFA bit 1: Enable interrupt (IMIA) by the IMFA bit	R/W
b1	IMIEB	Input capture/compare match interrupt enable bit B	0: Disable interrupt (IMIB) by the IMFB bit 1: Enable interrupt (IMIB) by the IMFB bit	R/W
b2	IMIEC	Input capture/compare match interrupt enable bit C	0: Disable interrupt (IMIC) by the IMFC bit 1: Enable interrupt (IMIC) by the IMFC bit	R/W
b3	IMIED	Input capture/compare match interrupt enable bit D	0: Disable interrupt (IMID) by the IMFD bit 1: Enable interrupt (IMID) by the IMFD bit	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b5	—			
b6	—			
b7	OVIE	Overflow interrupt enable bit	0: Disable interrupt (OVI) by the OVF bit 1: Enable interrupt (OVI) by the OVF bit	R/W

19.2.5 Timer RC Status Register (TRCSR)

Address 0123h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	OVF	—	—	—	IMFD	IMFC	IMFB	IMFA
After Reset	0	1	1	1	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMFA	Input capture/compare match flag A	[Source for setting this bit to 0] Write 0 after read. (1) [Source for setting this bit to 1] Refer to **Table 19.4 Source for Setting Bit of Each Flag to 1**.	R/W
b1	IMFB	Input capture/compare match flag B		R/W
b2	IMFC	Input capture/compare match flag C		R/W
b3	IMFD	Input capture/compare match flag D		R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b5	—			
b6	—			
b7	OVF	Overflow flag	[Source for setting this bit to 0] Write 0 after read. (1) [Source for setting this bit to 1] Refer to **Table 19.4 Source for Setting Bit of Each Flag to 1**.	R/W

Note:
1. The writing results are as follows:
   - This bit is set to 0 when the read result is 1 and 0 is written to the same bit.
   - This bit remains unchanged even if the read result is 0 and 0 is written to the same bit. (This bit remains 1 even if it is set to 1 from 0 after reading, and writing 0.)
   - This bit remains unchanged if 1 is written to it.

Table 19.4 Source for Setting Bit of Each Flag to 1

Bit Symbol	Timer Mode		PWM Mode	PWM2 Mode
	Input capture Function	Output Compare Function		
IMFA	TRCIOA pin input edge (1)	When the values of the registers TRC and TRCGRA match.		
IMFB	TRCIOB pin input edge (1)	When the values of the registers TRC and TRCGRB match.		
IMFC	TRCIOC pin input edge (1)	When the values of the registers TRC and TRCGRC match. (2)		
IMFD	TRCIOD pin input edge (1)	When the values of the registers TRC and TRCGRD match. (2)		
OVF	When the TRC register overflows.			

Notes:
1. Edge selected by bits IOj1 to IOj0 (j = A, B, C, or D).
2. Includes the condition that bits BFC and BFD are set to 1 (buffer registers of registers TRCGRA and TRCGRB).

19.2.6 Timer RC I/O Control Register 0 (TRCIOR0)

Address 0124h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOA0	TRCGRA control bit	Function varies according to the operating mode (function).	R/W
b1	IOA1			R/W
b2	IOA2	TRCGRA mode select bit (1)	0: Output compare function 1: Input capture function	R/W
b3	IOA3	TRCGRA input capture input switch bit (3)	0: fOCO128 signal 1: TRCIOA pin input	R/W
b4	IOB0	TRCGRB control bit	Function varies according to the operating mode (function).	R/W
b5	IOB1			R/W
b6	IOB2	TRCGRB mode select bit (2)	0: Output compare function 1: Input capture function	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

Notes:
1. When the BFC bit in the TRCMR register is set to 1 (buffer register of TRCGRA register), set the IOC2 bit in the TRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
2. When the BFD bit in the TRCMR register is set to 1 (buffer register of TRCGRB register), set the IOD2 bit in the TRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.
3. The IOA3 bit is enabled when the IOA2 bit is set to 1 (input capture function).

The TRCIOR0 register is enabled in timer mode. It is disabled in modes PWM and PWM2.

19.2.7 Timer RC I/O Control Register 1 (TRCIOR1)

Address 0125h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	IOD3	IOD2	IOD1	IOD0	IOC3	IOC2	IOC1	IOC0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOC0	TRCGRC control bit	Function varies according to the operating mode (function).	R/W
b1	IOC1			R/W
b2	IOC2	TRCGRC mode select bit (1)	0: Output compare function 1: Input capture function	R/W
b3	IOC3	TRCGRC register function select bit	0: TRCIOA output register 1: General register or buffer register	R/W
b4	IOD0	TRCGRD control bit	Function varies according to the operating mode (function).	R/W
b5	IOD1			R/W
b6	IOD2	TRCGRD mode select bit (2)	0: Output compare function 1: Input capture function	R/W
b7	IOD3	TRCGRD register function select bit	0: TRCIOB output register 1: General register or buffer register	R/W

Notes:
1. When the BFC bit in the TRCMR register is set to 1 (buffer register of TRCGRA register), set the IOC2 bit in the TRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
2. When the BFD bit in the TRCMR register is set to 1 (buffer register of TRCGRB register), set the IOD2 bit in the TRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.

The TRCIOR1 register is enabled in timer mode. It is disabled in modes PWM and PWM2.

19.2.8 Timer RC Counter (TRC)

Address 0127h to 0126h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Function	Setting Range	R/W
b15 to b0	Count a count source. Count operation is incremented. When an overflow occurs, the OVF bit in the TRCSR register is set to 1.	0000h to FFFFh	R/W

Access the TRC register in 16-bit units. Do not access it in 8-bit units.

19.2.9 Timer RC General Registers A, B, C, and D (TRCGRA, TRCGRB, TRCGRC, TRCGRD)

Address 0129h to 0128h (TRCGRA), 012Bh to 012Ah (TRCGRB), 012Dh to 012Ch (TRCGRC), 012Fh to 012Eh (TRCGRD)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Function	R/W
b15 to b0	Function varies according to the operating mode.	R/W

Access registers TRCGRA to TRCGRD in 16-bit units. Do not access them in 8-bit units.

19.2.10 Timer RC Control Register 2 (TRCCR2)

Address 0130h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TCEG1	TCEG0	CSEL	—	—	POLD	POLC	POLB
After Reset	0	0	0	1	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	POLB	PWM mode output level control bit B (1)	0: TRCIOB output level selected as “L” active 1: TRCIOB output level selected as “H” active	R/W
b1	POLC	PWM mode output level control bit C (1)	0: TRCIOC output level selected as “L” active 1: TRCIOC output level selected as “H” active	R/W
b2	POLD	PWM mode output level control bit D (1)	0: TRCIOD output level selected as “L” active 1: TRCIOD output level selected as “H” active	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b4	—			
b5	CSEL	TRC count operation select bit (2)	0: Count continues at compare match with the TRCGRA register 1: Count stops at compare match with the TRCGRA register	R/W
b6	TCEG0	TRCTRG input edge select bit (3)	b7 b6 0 0: Disable the trigger input from the TRCTRG pin 0 1: Rising edge selected 1 0: Falling edge selected 1 1: Both edges selected	R/W
b7	TCEG1			R/W

Notes:
1. Enabled when in PWM mode.
2. Enabled when in the output compare function, PWM mode, or PWM2 mode. For notes on PWM2 mode, refer to **19.9.6 TRCMR Register in PWM2 Mode**.
3. Enabled when in PWM2 mode.

19.2.11 Timer RC Digital Filter Function Select Register (TRCDF)

Address 0131h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	DFCK1	DFCK0	—	DFTRG	DFD	DFC	DFB	DFA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	DFA	TRCIOA pin digital filter function select bit (1)	0: Function is not used 1: Function is used	R/W
b1	DFB	TRCIOB pin digital filter function select bit (1)		R/W
b2	DFC	TRCIOC pin digital filter function select bit (1)		R/W
b3	DFD	TRCIOD pin digital filter function select bit (1)		R/W
b4	DFTRG	TRCTRG pin digital filter function select bit (2)		R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b6	DFCK0	Clock select bits for digital filter function (1, 2)	b7 b6 0 0: f32 0 1: f8 1 0: f1 1 1: Count source (clock selected by bits TCK2 to TCK0 in the TRCCR1 register)	R/W
b7	DFCK1			R/W

Notes:
1. These bits are enabled for the input capture function.
2. These bits are enabled when in PWM2 mode and bits TCEG1 to TCEG0 in the TRCCR2 register are set to 01b, 10b, or 11b (TRCTRG trigger input enabled).

19.2.12 Timer RC Output Master Enable Register (TRCOER)

Address 0132h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PTO	—	—	—	ED	EC	EB	EA
After Reset	0	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	EA	TRCIOA output disable bit (1)	0: Enable output 1: Disable output (The TRCIOA pin is used as a programmable I/O port.)	R/W
b1	EB	TRCIOB output disable bit (1)	0: Enable output 1: Disable output (The TRCIOB pin is used as a programmable I/O port.)	R/W
b2	EC	TRCIOC output disable bit (1)	0: Enable output 1: Disable output (The TRCIOC pin is used as a programmable I/O port.)	R/W
b3	ED	TRCIOD output disable bit (1)	0: Enable output 1: Disable output (The TRCIOD pin is used as a programmable I/O port.)	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b5	—			
b6	—			
b7	PTO	$\overline{\text{INT0}}$ of pulse output forced cutoff signal input enabled bit	0: Pulse output forced cutoff input disabled 1: Pulse output forced cutoff input enabled (Bits EA, EB, EC, and ED are set to 1 (disable output) when “L” is applied to the $\overline{\text{INT0}}$ pin)	R/W

Note:
1. These bits are disabled for input pins set to the input capture function.

19.2.13 Timer RC Trigger Control Register (TRCADCR)(1)

Address 0133h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	ADTRGDE	ADTRGCE	ADTRGBE	ADTRGAE
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ADTRGAE	A/D trigger A enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRC and TRCGRA	R/W
b1	ADTRGBE	A/D trigger B enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRC and TRCGRB	R/W
b2	ADTRGCE	A/D trigger C enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRC and TRCGRC	R/W
b3	ADTRGDE	A/D trigger D enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRC and TRCGRD	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

Note:
1. Not available in the R8C/3MU Group.

19.2.14 Timer RC Pin Select Register (TRBRCSR)

Address 0181h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	TRCCLKSEL1	TRCCLKSEL0	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	—			
b4	TRCCLKSEL0	TRCCLK pin select bit	b5 b4 0 0: TRCCLK pin not used 0 1: P1_4 assigned 1 0: P3_3 assigned 1 1: Do not set.	R/W
b5	TRCCLKSEL1			R/W
b6	—	Reserved bit	Set to 0.	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

The TRBRCSR register selects which pin is assigned to the timer RC I/O. To use the I/O pin for timer RC, set this register.
Set bits TRCCLKSEL0 to TRCCLKSEL1 before setting the timer RC associated registers. Also, do not change the setting values. Do not change the setting values of bits TRCCLKSEL0 to TRCCLKSEL1 during timer RC operation.

19.2.15 Timer RC Pin Select Register 0 (TRCPSR0)

Address 0182h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	TRCIOBSEL1	TRCIOBSEL0	—	TRCIOASEL2	TRCIOASEL1	TRCIOASEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRCIOASEL0	TRCIOA/TRCTRG pin select bit	b2 b1 b0 0 0 0: TRCIOA/TRCTRG pin not used 0 0 1: P1_1 assigned 0 1 0: P0_0 assigned 0 1 1: P0_1 assigned 1 0 0: P0_2 assigned Other than above: Do not set.	R/W
b1	TRCIOASEL1			R/W
b2	TRCIOASEL2			R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	TRCIOBSEL0	TRCIOB pin select bit	b5 b4 0 0: TRCIOB pin not used 0 1: P1_2 assigned 1 0: P0_3 assigned 1 1: P0_4 assigned	R/W
b5	TRCIOBSEL1			R/W
b6	—	Reserved bit	Set to 0.	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

The TRCPSR0 register selects which pin is assigned to the timer RC I/O. To use the I/O pin for timer RC, set this register.
Set the TRCPSR0 register before setting the timer RC associated registers. Also, do not change the setting value in this register during timer RC operation.

19.2.16 Timer RC Pin Select Register 1 (TRCPSR1)

Address 0183h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	TRCIODSEL2	TRCIODSEL1	TRCIODSEL0	—	—	TRCIOCSEL1	TRCIOCSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRCIOCSEL0	TRCIOC pin select bit	b1 b0 0 0: TRCIOC pin not used 0 1: P1_3 assigned 1 0: P3_4 assigned 1 1: P0_7 assigned	R/W
b1	TRCIOCSEL1			R/W
b2	—	Reserved bit	Set to 0.	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	TRCIODSEL0	TRCIOD pin select bit	b6 b5 b4 0 0 0: TRCIOD pin not used 0 0 1: P1_0 assigned 0 1 0: P3_5 assigned 0 1 1: Do not set. 1 0 1: P6_7_assigned Other than above: Do not set.	R/W
b5	TRCIODSEL1			R/W
b6	TRCIODSEL2			R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

The TRCPSR1 register selects which pin is assigned to the timer RC I/O. To use the I/O pin for timer RC, set this register.
Set the TRCPSR1 register before setting the timer RC associated registers. Also, do not change the setting value in this register during timer RC operation.

19.3 Common Items for Multiple Modes

19.3.1 Count Source

The method of selecting the count source is common to all modes.
Table 19.5 lists the Count Source Selection and Figure 19.2 shows a Count Source Block Diagram.

Table 19.5 Count Source Selection

Count Source	Selection Method
f1, f2, f4, f8, f32	Count source selected using bits TCK2 to TCK0 in TRCCR1 register
fOCO40M fOCO-F	FRA00 bit in FRA0 register set to 1 (high-speed on-chip oscillator on) Bits TCK2 to TCK0 in TRCCR1 register are set to 110b (fOCO40M) Bits TCK2 to TCK0 in TRCCR1 register are set to 111b (fOCO-F)
External signal input to TRCCLK pin	Bits TCK2 to TCK0 in TRCCR1 register are set to 101b (count source is rising edge of external clock) and the corresponding direction bit in the corresponding direction register is set is set to 0 (input mode)

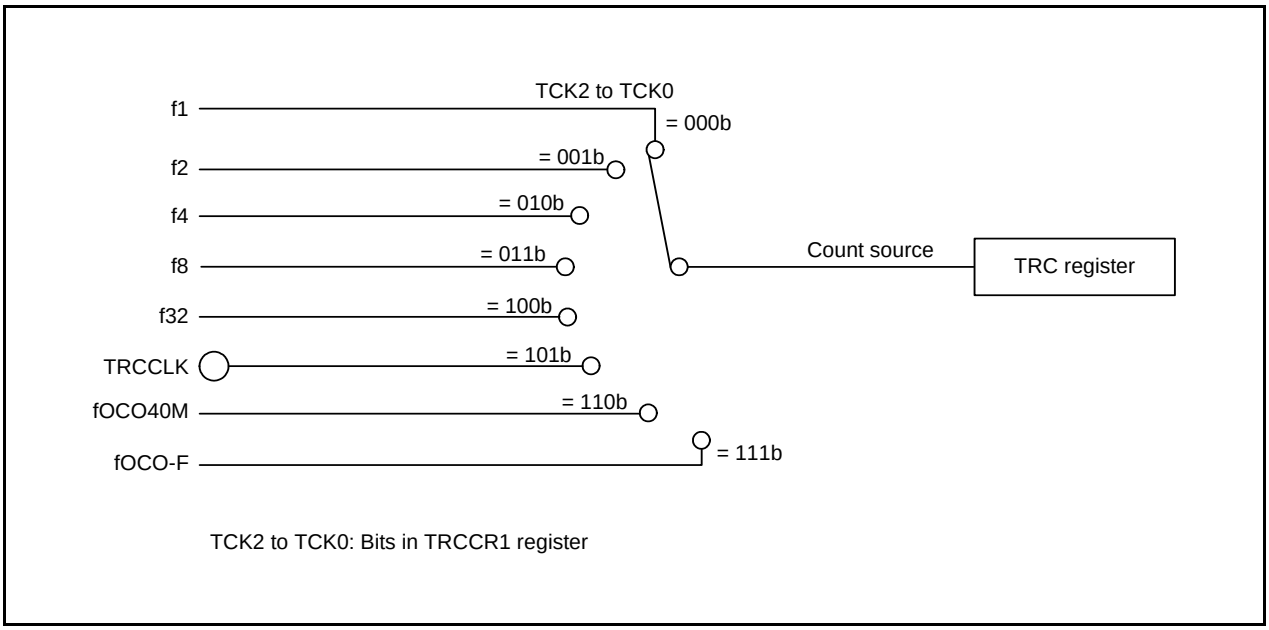


Figure 19.2 Count Source Block Diagram

The pulse width of the external clock input to the TRCCLK pin should be three cycles or more of the timer RC operation clock (refer to **Table 19.1 Timer RC Operation Clocks**).
To select fOCO40M or fOCO-F as the count source, set the FRA00 bit in the FRA0 register set to 1 (high-speed on-chip oscillator on), and then set bits TCK2 to TCK0 in the TRCCR1 register to 110b (fOCO40M) or 111b (fOCO-F).

19.3.2 Buffer Operation

Bits BFC and BFD in the TRCMR register are used to select the TRCGRC or TRCGRD register as the buffer register for the TRCGRA or TRCGRB register.

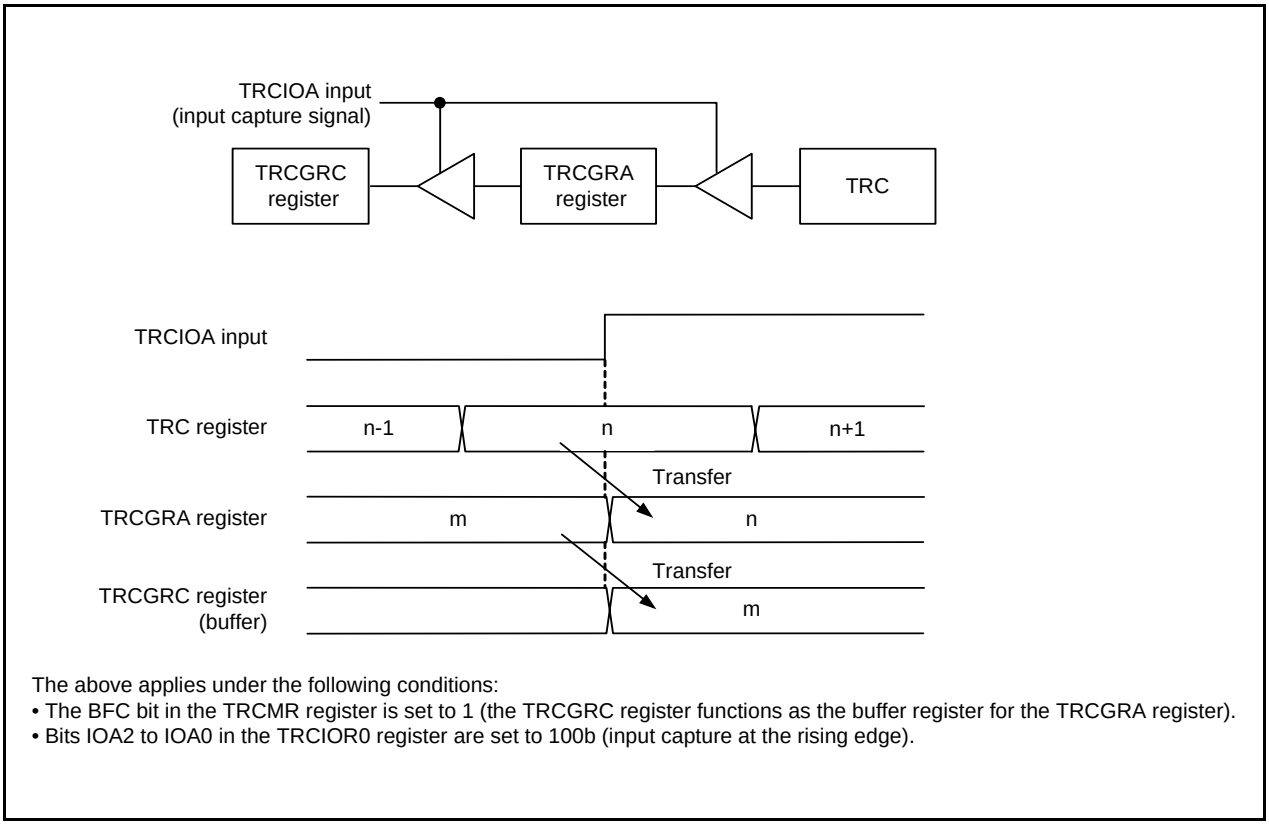
- Buffer register for TRCGRA register: TRCGRC register
- Buffer register for TRCGRB register: TRCGRD register

Buffer operation differs depending on the mode.

Table 19.6 lists the Buffer Operation in Each Mode, Figure 19.3 shows the Buffer Operation for Input Capture Function, and Figure 19.4 shows the Buffer Operation for Output Compare Function.

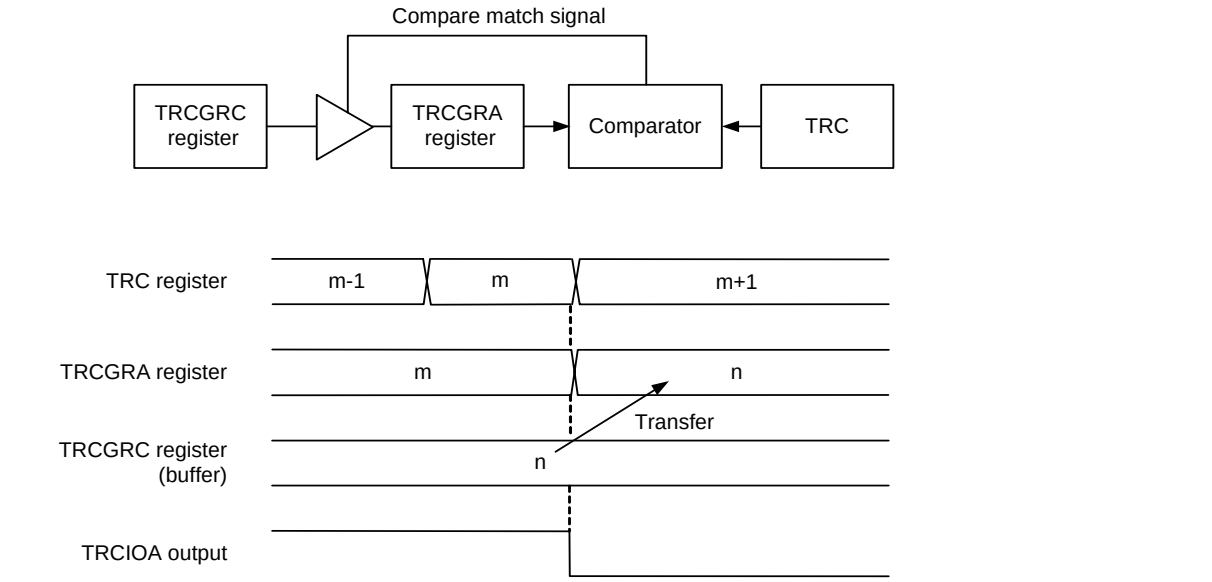
Table 19.6 Buffer Operation in Each Mode

Function, Mode	Transfer Timing	Transfer Destination Register
Input capture function	Input capture signal input	Contents of TRCGRA (TRCGRB) register are transferred to buffer register
Output compare function PWM mode	Compare match between TRC register and TRCGRA (TRCGRB) register	Contents of buffer register are transferred to TRCGRA (TRCGRB) register
PWM2 mode	• Compare match between TRC register and TRCGRA register • TRCTRG pin trigger input	Contents of buffer register (TRCGRD) are transferred to TRCGRB register



The above applies under the following conditions:
- The BFC bit in the TRCMR register is set to 1 (the TRCGRC register functions as the buffer register for the TRCGRA register).
- Bits IOA2 to IOA0 in the TRCIOR0 register are set to 100b (input capture at the rising edge).

Figure 19.3 Buffer Operation for Input Capture Function



The above applies under the following conditions:
- The BFC bit in the TRCMR register is set to 1 (the TRCGRC register functions as the buffer register for the TRCGRA register).
- Bits IOA2 to IOA0 in the TRCIOR0 register are set to 001b (“L” output by compare match).

Figure 19.4 Buffer Operation for Output Compare Function

Make the following settings in timer mode.
- To use the TRCGRC register as the buffer register for the TRCGRA register:
  Set the IOC2 bit in the TRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
- To use the TRCGRD register as the buffer register for the TRCGRB register:
  Set the IOD2 bit in the TRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.

The output compare function, PWM mode, or PWM2 mode, and the TRCGRC or TRCGRD register is functioning as a buffer register, the IMFC bit or IMFD bit in the TRCSR register is set to 1 when a compare match with the TRC register occurs.
The input capture function and the TRCGRC register or TRCGRD register is functioning as a buffer register, the IMFC bit or IMFD bit in the TRCSR register is set to 1 at the input edge of a signal input to the TRCIOC pin or TRCIOD pin.

19.3.3 Digital Filter

The input to TRCTRG or TRCIOj (j = A, B, C, or D) is sampled, and the level is considered to be determined when three matches occur. The digital filter function and sampling clock are selected using the TRCDF register. Figure 19.5 shows a Digital Filter Block Diagram.

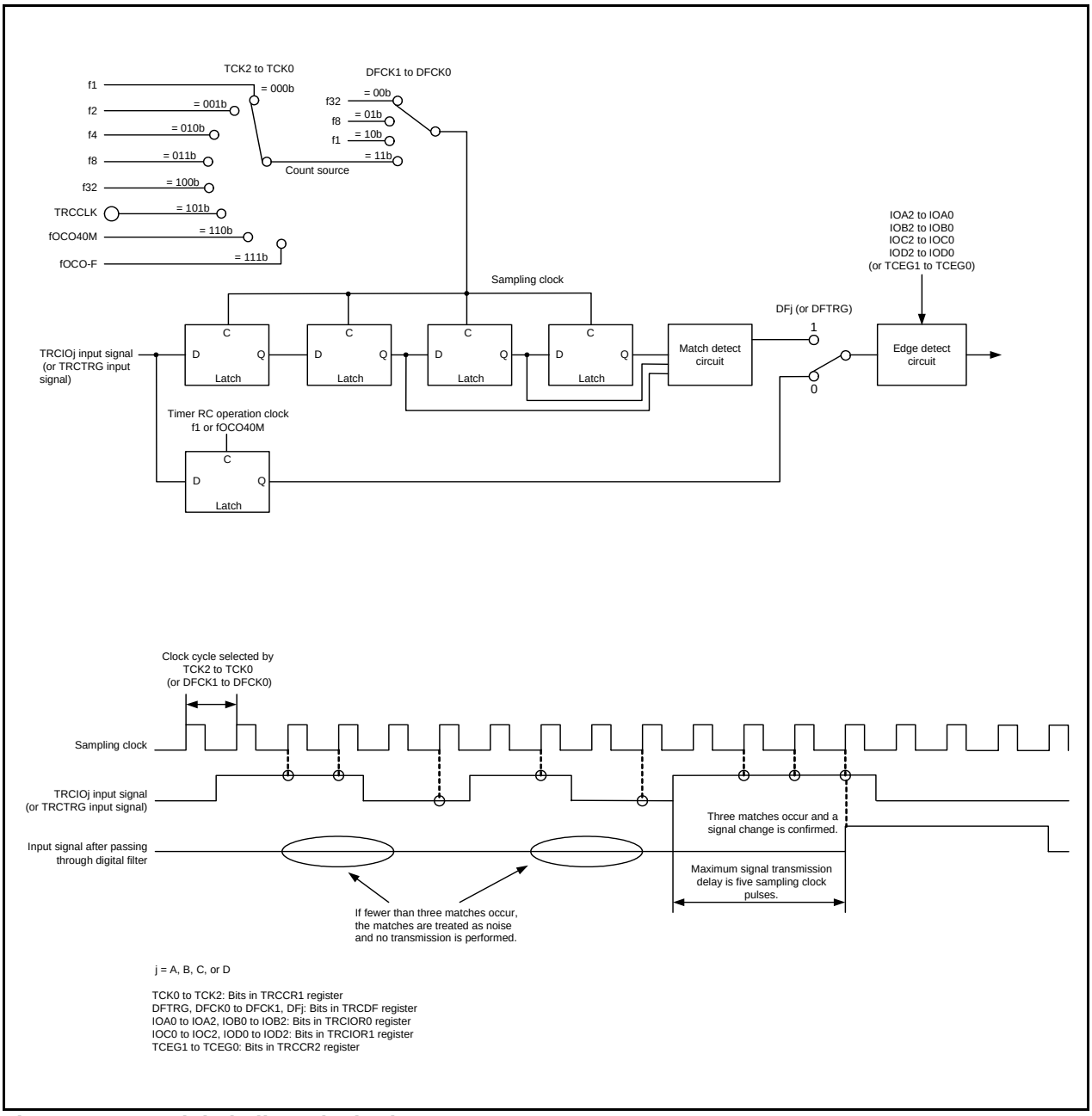


Figure 19.5 Digital Filter Block Diagram

19.3.4 Forced Cutoff of Pulse Output

When using the timer mode's output compare function, the PWM mode, or the PWM2 mode, pulse output from the TRCIOj (j = A, B, C, or D) output pin can be forcibly cut off and the TRCIOj pin set to function as a programmable I/O port by means of input to the $\overline{\text{INT0}}$ pin.
A pin used for output by the timer mode's output compare function, the PWM mode, or the PWM2 mode can be set to function as the timer RC output pin by setting the Ej bit in the TRCOER register to 0 (timer RC output enabled). If "L" is input to the $\overline{\text{INT0}}$ pin while the PTO bit in the TRCOER register is set to 1 (pulse output forced cutoff signal input $\overline{\text{INT0}}$ enabled), bits EA, EB, EC, and ED in the TRCOER register are all set to 1 (timer RC output disabled, TRCIOj output pin functions as the programmable I/O port). When one or two cycles of the timer RC operation clock after "L" input to the $\overline{\text{INT0}}$ pin (refer to **Table 19.1 Timer RC Operation Clocks**) has elapsed, the TRCIOj output pin becomes a programmable I/O port.

Make the following settings to use this function:
- Set the pin state following forced cutoff of pulse output (high impedance (input), "L" output, or "H" output) (refer to **7. I/O Ports**).
- Set the INT0EN bit in the INTEN register to 1 ($\overline{\text{INT0}}$ input enabled) and the INT0PL bit to 0 (one edge), and set the POL bit in the INT0IC register to 0 (falling edge selected).
- Set the PD4_5 bit in the PD4 register to 0 (input mode).
- Select the $\overline{\text{INT0}}$ digital filter by bits INT0F1 to INT0F0 in the INTF register.
- Set the PTO bit in the TRCOER register to 1 (pulse output forced cutoff signal input $\overline{\text{INT0}}$ enabled).

The IR bit in the INT0IC register is set to 1 (interrupt requested) in accordance with the setting of the POL bit in the INT0IC register and the INT0PL bit in the INTEN register, and a change in the $\overline{\text{INT0}}$ pin input (refer to **11.8 Notes on Interrupts**).
For details on interrupts, refer to **11. Interrupts**.

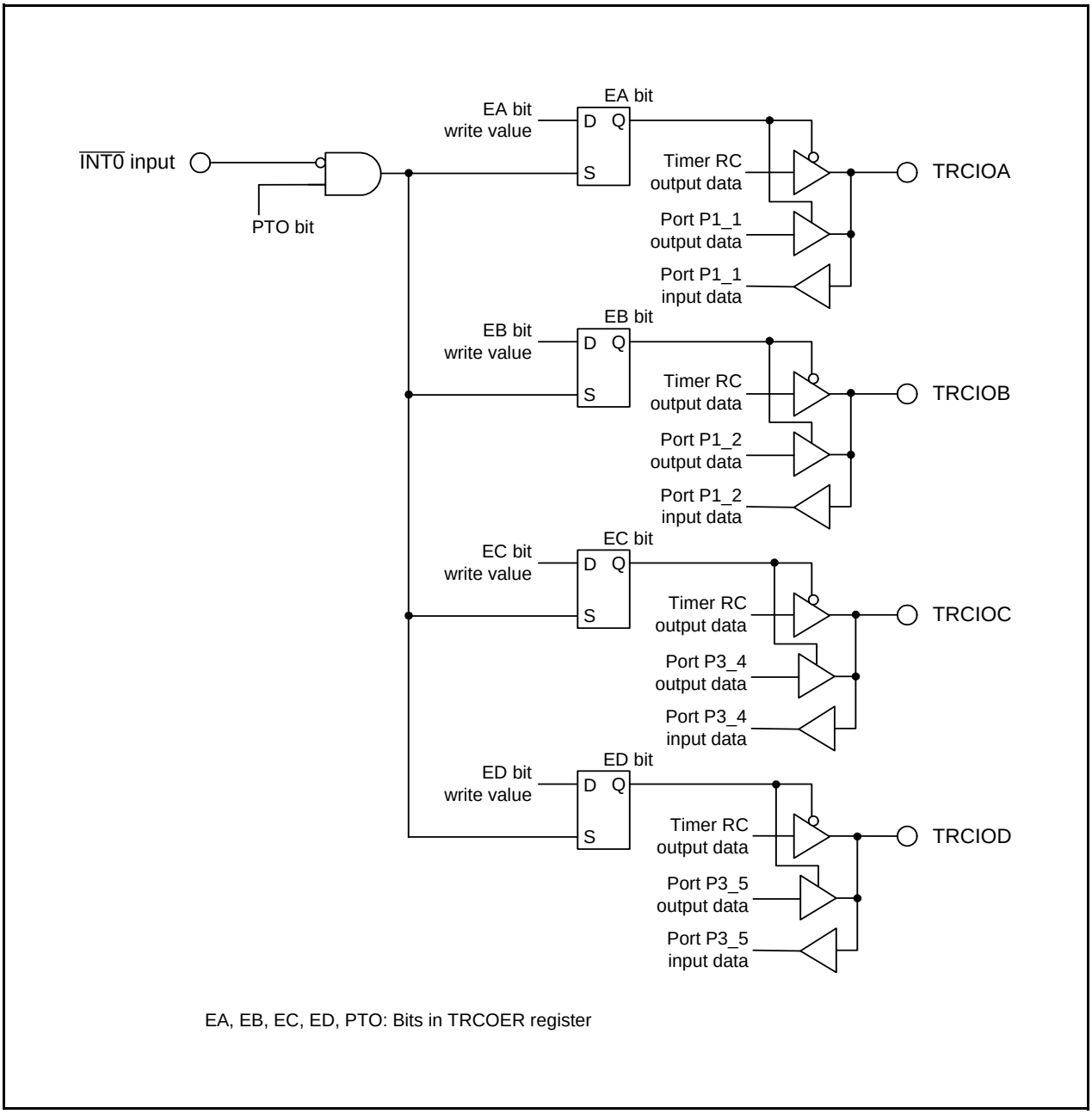


Figure 19.6 Forced Cutoff of Pulse Output

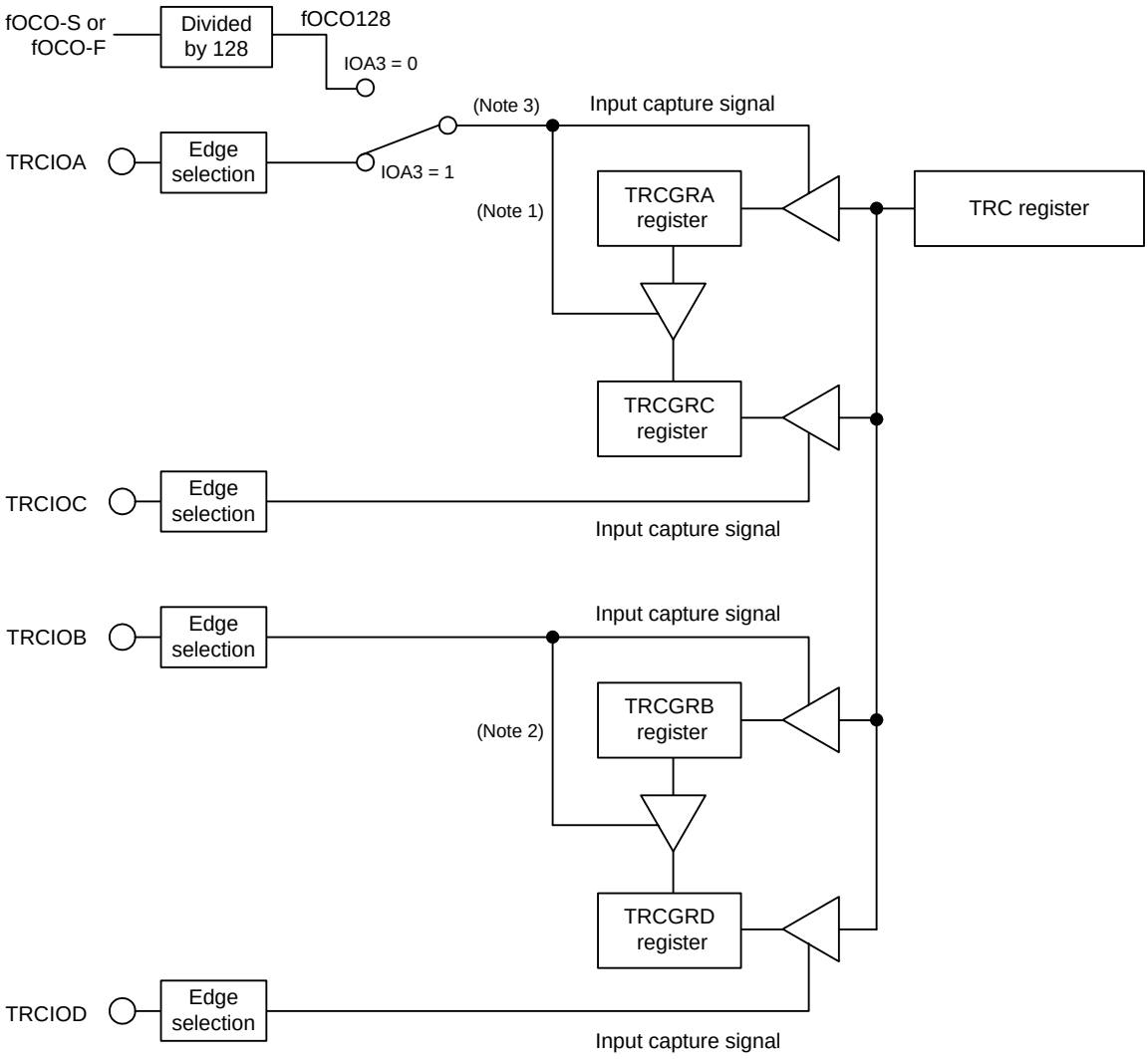
19.4 Timer Mode (Input Capture Function)

This function measures the width or period of an external signal. An external signal input to the TRCIOj (j = A, B, C, or D) pin acts as a trigger for transferring the contents of the TRC register (counter) to the TRCGRj register (input capture). The input capture function, or any other mode or function, can be selected for each individual pin. The TRCGRA register can also select fOCO128 signal as input-capture trigger input.
Table 19.7 lists the Input Capture Function Specifications, Figure 19.7 shows a Block Diagram of Input Capture Function, Table 19.8 lists the Functions of TRCGRj Register when Using Input Capture Function, and Figure 19.8 shows an Operating Example of Input Capture Function.

Table 19.7 Input Capture Function Specifications

Item	Specification
Count source	f1, f2, f4, f8, f32, fOCO40M, fOCO-F External signal input to TRCCLK pin (rising edge)
Count operation	Increment
Count period	• The CCLR bit in the TRCCR1 register is set to 0 (free running operation): 1/fk × 65,536 fk: Count source frequency • The CCLR bit in the TRCCR1 register is set to 1 (TRC register set to 0000h at TRCGRA compare match): 1/fk × (n+1) n: TRCGRA register setting value
Count start condition	1 (count starts) is written to the TSTART bit in the TRCMR register.
Count stop condition	0 (count stops) is written to the TSTART bit in the TRCMR register. The TRC register retains a value before count stops.
Interrupt request generation timing	• Input capture (valid edge of TRCIOj input or fOCO128 signal edge) • The TRC register overflows.
TRCIOA, TRCIOB, TRCIOC, and TRCIOD pin functions	Programmable I/O port or input capture input (selectable individually for each pin)
$\overline{\text{INT0}}$ pin function	Programmable I/O port or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read by reading TRC register.
Write to timer	The TRC register can be written to.
Selectable functions	• Input capture input pin selection One or more of pins TRCIOA, TRCIOB, TRCIOC, and TRCIOD • Input capture input valid edge selection Rising edge, falling edge, or both rising and falling edges • Buffer operation (refer to **19.3.2 Buffer Operation**) • Digital filter (refer to **19.3.3 Digital Filter**) • Timing for setting the TRC register to 0000h Overflow or input capture • Input-capture trigger selected fOCO128 can be selected for input-capture trigger input of the TRCGRA register.

j = A, B, C, or D



IOA3: Bit in TRCIOR0 register

Notes:
1. The BFC bit in the TRCMR register is set to 1 (TRCGRC register functions as the buffer register for the TRCGRA register)
2. The BFD bit in the TRCMR register is set to 1 (TRCGRD register functions as the buffer register for the TRCGRB register)
3. The trigger input of the TRCGRA register can select the TRCIOA pin input or fOCO128 signal.

Figure 19.7 Block Diagram of Input Capture Function

19.4.1 Timer RC I/O Control Register 0 (TRCIOR0) for Input Capture Function

Address 0124h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOA0	TRCGRA control bit	b1 b0 0 0: Input capture to the TRCGRA register at the rising edge 0 1: Input capture to the TRCGRA register at the falling edge 1 0: Input capture to the TRCGRA register at both edges 1 1: Do not set.	R/W
b1	IOA1			R/W
b2	IOA2	TRCGRA mode select bit (1)	Set to 1 (input capture) in the input capture function.	R/W
b3	IOA3	TRCGRA input capture input switch bit (3)	0: fOCO128 signal 1: TRCIOA pin input	R/W
b4	IOB0	TRCGRB control bit	b5 b4 0 0: Input capture to the TRCGRB register at the rising edge 0 1: Input capture to the TRCGRB register at the falling edge 1 0: Input capture to the TRCGRB register at both edges 1 1: Do not set.	R/W
b5	IOB1			R/W
b6	IOB2	TRCGRB mode select bit (2)	Set to 1 (input capture) in the input capture function.	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

Notes:
1. When the BFC bit in the TRCMR register is set to 1 (buffer register of TRCGRA register), set the IOC2 bit in the TRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
2. When the BFD bit in the TRCMR register is set to 1 (buffer register of TRCGRB register), set the IOD2 bit in the TRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.
3. The IOA3 bit is enabled when the IOA2 bit is set to 1 (input capture function).

19.4.2 Timer RC I/O Control Register 1 (TRCIOR1) for Input Capture Function

Address 0125h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	IOD3	IOD2	IOD1	IOD0	IOC3	IOC2	IOC1	IOC0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOC0	TRCGRC control bit	b1 b0 0 0: Input capture to the TRCGRC register at the rising edge 0 1: Input capture to the TRCGRC register at the falling edge 1 0: Input capture to the TRCGRC register at both edges 1 1: Do not set.	R/W
b1	IOC1			R/W
b2	IOC2	TRCGRC mode select bit (1)	Set to 1 (input capture) in the input capture function.	R/W
b3	IOC3	TRCGRC register function select bit	Set to 1.	R/W
b4	IOD0	TRCGRD control bit	b5 b4 0 0: Input capture to the TRCGRD register at the rising edge 0 1: Input capture to the TRCGRD register at the falling edge 1 0: Input capture to the TRCGRD register at both edges 1 1: Do not set.	R/W
b5	IOD1			R/W
b6	IOD2	TRCGRD mode select bit (2)	Set to 1 (input capture) in the input capture function.	R/W
b7	IOD3	TRCGRD register function select bit	Set to 1.	R/W

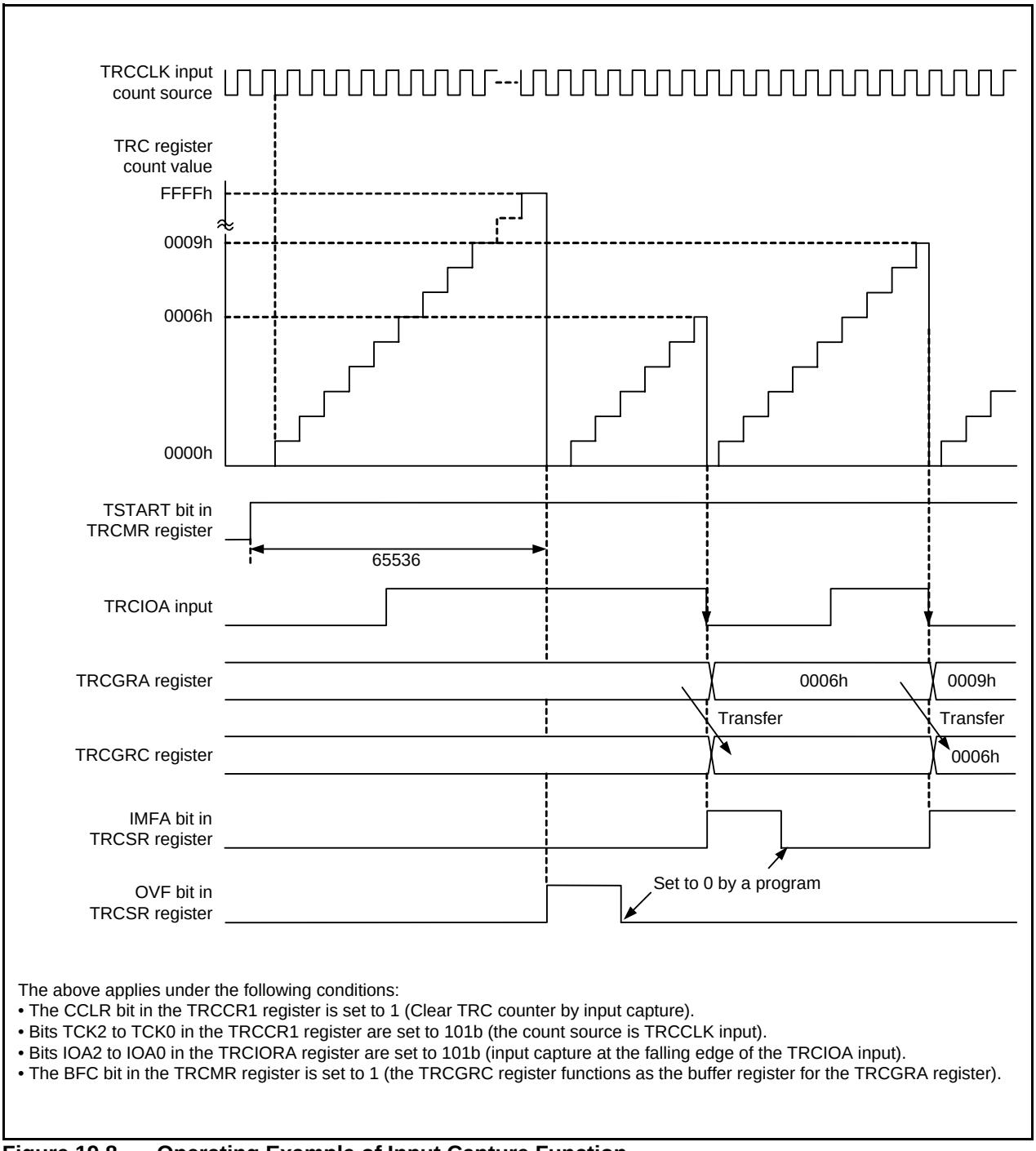
Notes:
1. When the BFC bit in the TRCMR register is set to 1 (buffer register of TRCGRA register), set the IOC2 bit in the TRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
2. When the BFD bit in the TRCMR register is set to 1 (buffer register of TRCGRB register), set the IOD2 bit in the TRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.

Table 19.8 Functions of TRCGRj Register when Using Input Capture Function

Register	Setting	Register Function	Input Capture Input Pin
TRCGRA	—	General register. Can be used to read the TRC register value at input capture.	TRCIOA
TRCGRB			TRCIOB
TRCGRC	BFC = 0	General register. Can be used to read the TRC register value at input capture.	TRCIOC
TRCGRD	BFD = 0		TRCIOD
TRCGRC	BFC = 1	Buffer registers. Can be used to hold transferred value from the general register (refer to **19.3.2 Buffer Operation**).	TRCIOA
TRCGRD	BFD = 1		TRCIOB

j = A, B, C, or D
BFC, BFD: Bits in TRCMR register

19.4.3 Operating Example



The above applies under the following conditions:
- The CCLR bit in the TRCCR1 register is set to 1 (Clear TRC counter by input capture).
- Bits TCK2 to TCK0 in the TRCCR1 register are set to 101b (the count source is TRCCLK input).
- Bits IOA2 to IOA0 in the TRCIORA register are set to 101b (input capture at the falling edge of the TRCIOA input).
- The BFC bit in the TRCMR register is set to 1 (the TRCGRC register functions as the buffer register for the TRCGRA register).

Figure 19.8 Operating Example of Input Capture Function

19.5 Timer Mode (Output Compare Function)

This function detects when the contents of the TRC register (counter) and the TRCGRj register (j = A, B, C, or D) match (compare match). When a match occurs a signal is output from the TRCIOj pin at a given level. The output compare function, or other mode or function, can be selected for each individual pin.
Table 19.9 lists the Output Compare Function Specifications, Figure 19.9 shows a Block Diagram of Output Compare Function, Table 19.10 lists the Functions of TRCGRj Register when Using Output Compare Function, and Figure 19.10 shows an Operating Example of Output Compare Function.

Table 19.9 Output Compare Function Specifications

Item	Specification
Count source	f1, f2, f4, f8, f32, fOCO40M, fOCO-F External signal input to TRCCLK pin (rising edge)
Count operation	Increment
Count period	• The CCLR bit in the TRCCR1 register is set to 0 (free running operation): 1/fk × 65,536 fk: Count source frequency • The CCLR bit in the TRCCR1 register is set to 1 (TRC register set to 0000h at TRCGRA compare match): 1/fk × (n+1) n: TRCGRA register setting value
Waveform output timing	Compare match
Count start condition	1 (count starts) is written to the TSTART bit in the TRCMR register.
Count stop condition	• When the CSEL bit in the TRCCR2 register is set to 0 (count continues after compare match with TRCGRA). 0 (count stops) is written to the TSTART bit in the TRCMR register. The output compare output pin retains output level before count stops, the TRC register retains a value before count stops. • When the CSEL bit in the TRCCR2 register is set to 1 (count stops at compare match with TRCGRA register). The count stops at the compare match with the TRCGRA register. The output compare output pin retains the level after the output is changed by the compare match.
Interrupt request generation timing	• Compare match (contents of registers TRC and TRCGRj match) • The TRC register overflows.
TRCIOA, TRCIOB, TRCIOC, and TRCIOD pin functions	Programmable I/O port or output compare output (selectable individually for each pin)
$\overline{\text{INT0}}$ pin function	Programmable I/O port, pulse output forced cutoff signal input, or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read by reading the TRC register.
Write to timer	The TRC register can be written to.
Selectable functions	• Output compare output pin selection One or more of pins TRCIOA, TRCIOB, TRCIOC, and TRCIOD • Compare match output level selection “L” output, “H” output, or toggle output • Initial output level selection Sets output level for period from count start to compare match • Timing for setting the TRC register to 0000h Overflow or compare match with the TRCGRA register • Buffer operation (refer to **19.3.2 Buffer Operation**) • Pulse output forced cutoff signal input (refer to **19.3.4 Forced Cutoff of Pulse Output**) • Can be used as an internal timer by disabling timer RC output • Changing output pins for registers TRCGRC and TRCGRD TRCGRC can be used for output control of the TRCIOA pin and TRCGRD can be used for output control of the TRCIOB pin. • A/D trigger generation (1)

j = A, B, C, or D

Note:
1. Not available in the R8C/3MU Group.

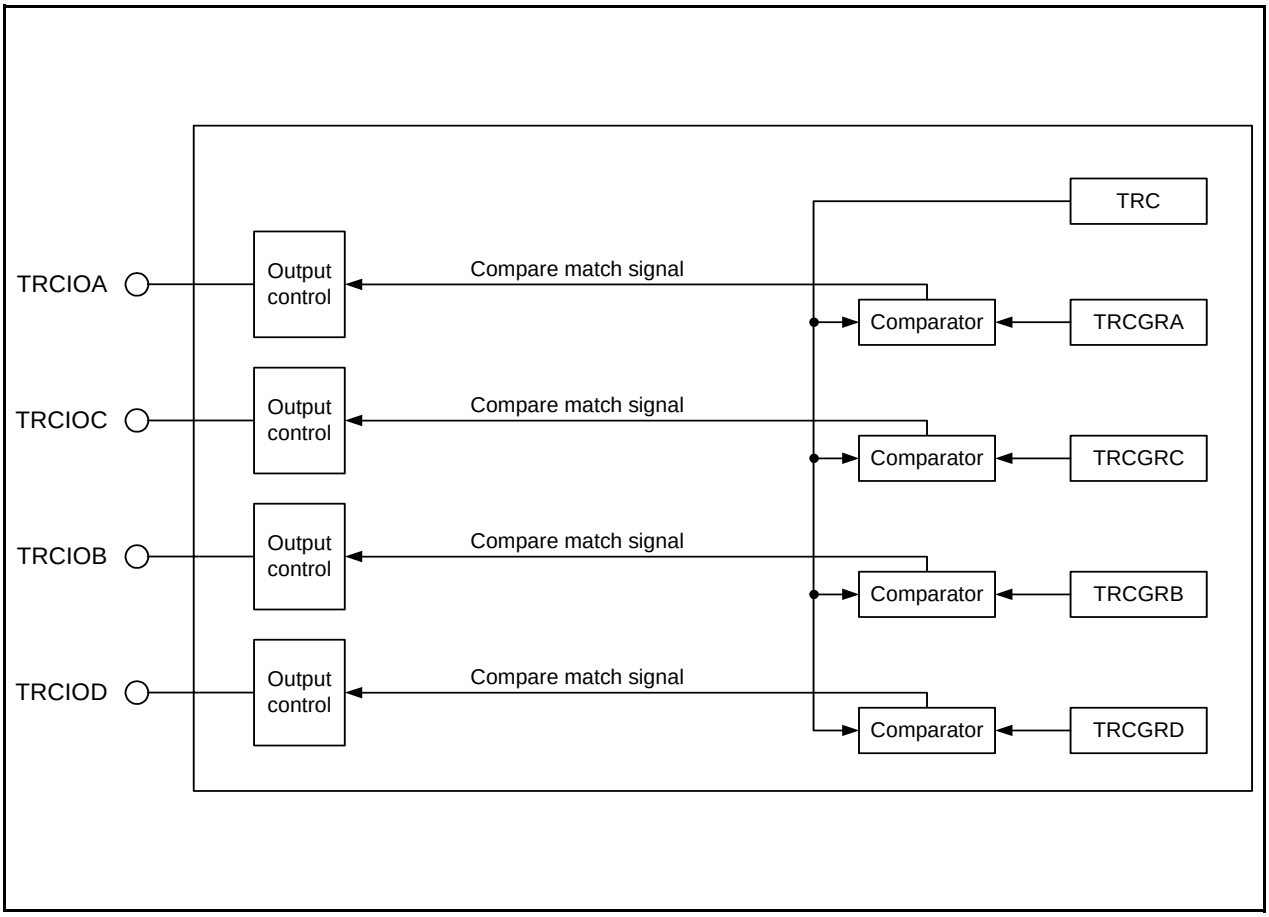


Figure 19.9 Block Diagram of Output Compare Function

19.5.1 Timer RC Control Register 1 (TRCCR1) for Output Compare Function

Address 0121h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CCLR	TCK2	TCK1	TCK0	TOD	TOC	TOB	TOA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOA	TRCIOA output level select bit (1, 2)	0: Initial output “L” 1: Initial output “H”	R/W
b1	TOB	TRCIOB output level select bit (1, 2)		R/W
b2	TOC	TRCIOC output level select bit (1, 2)		R/W
b3	TOD	TRCIOD output level select bit (1, 2)		R/W
b4	TCK0	Count source select bit (1)	b6 b5 b4 0 0 0: f1 0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: TRCCLK input rising edge 1 1 0: fOCO40M 1 1 1: fOCO-F (3)	R/W
b5	TCK1			R/W
b6	TCK2			R/W
b7	CCLR	TRC counter clear select bit	0: Disable clear (free-running operation) 1: Clear by compare match in the TRCGRA register	R/W

Notes:
1. Set to these bits when the TSTART bit in the TRCMR register is set to 0 (count stops).
2. If the pin function is set for waveform output (refer to **7.5 Port Settings**), the initial output level is output when the TRCCR1 register is set.
3. To select fOCO-F, set it to the clock frequency higher than the CPU clock frequency.

Table 19.10 Functions of TRCGRj Register when Using Output Compare Function

Register	Setting	Register Function	Output Compare Output Pin
TRCGRA	—	General register. Write a compare value to one of these registers.	TRCIOA
TRCGRB			TRCIOB
TRCGRC	BFC = 0	General register. Write a compare value to one of these registers.	TRCIOC
TRCGRD	BFD = 0		TRCIOD
TRCGRC	BFC = 1	Buffer register. Write the next compare value to one of these registers (refer to **19.3.2 Buffer Operation**).	TRCIOA
TRCGRD	BFD = 1		TRCIOB

j = A, B, C, or D
BFC, BFD: Bits in TRCMR register

19.5.2 Timer RC I/O Control Register 0 (TRCIOR0) for Output Compare Function

Address 0124h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOA0	TRCGRA control bit	b1 b0 0 0: Disable pin output by compare match (TRCIOA pin functions as the programmable I/O port) 0 1: “L” output by compare match in the TRCGRA register 1 0: “H” output by compare match in the TRCGRA register 1 1: Toggle output by compare match in the TRCGRA register	R/W
b1	IOA1			R/W
b2	IOA2	TRCGRA mode select bit (1)	Set to 0 (output compare) in the output compare function.	R/W
b3	IOA3	TRCGRA input capture input switch bit	Set to 1.	R/W
b4	IOB0	TRCGRB control bit	b5 b4 0 0: Disable pin output by compare match (TRCIOB pin functions as the programmable I/O port) 0 1: “L” output by compare match in the TRCGRB register 1 0: “H” output by compare match in the TRCGRB register 1 1: Toggle output by compare match in the TRCGRB register	R/W
b5	IOB1			R/W
b6	IOB2	TRCGRB mode select bit (2)	Set to 0 (output compare) in the output compare function.	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

Notes:
1. When the BFC bit in the TRCMR register is set to 1 (buffer register of TRCGRA register), set the IOC2 bit in theTRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
2. When the BFD bit in the TRCMR register is set to 1 (buffer register of TRCGRB register), set the IOD2 bit in the TRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.

19.5.3 Timer RC I/O Control Register 1 (TRCIOR1) for Output Compare Function

Address 0125h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	IOD3	IOD2	IOD1	IOD0	IOC3	IOC2	IOC1	IOC0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOC0	TRCGRC control bit	b1 b0 0 0: Disable pin output by compare match 0 1: “L” output by compare match in the TRCGRC register 1 0: “H” output by compare match in the TRCGRC register 1 1: Toggle output by compare match in the TRCGRC register	R/W
b1	IOC1			R/W
b2	IOC2	TRCGRC mode select bit (1)	Set to 0 (output compare) in the output compare function.	R/W
b3	IOC3	TRCGRC register function select bit	0: TRCIOA output register 1: General register or buffer register	R/W
b4	IOD0	TRCGRD control bit	b5 b4 0 0: Disable pin output by compare match 0 1: “L” output by compare match in the TRCGRD register 1 0: “H” output by compare match in the TRCGRD register 1 1: Toggle output by compare match in the TRCGRD register	R/W
b5	IOD1			R/W
b6	IOD2	TRCGRD mode select bit (2)	Set to 0 (output compare) in the output compare function.	R/W
b7	IOD3	TRCGRD register function select bit	0: TRCIOB output register 1: General register or buffer register	R/W

Notes:
1. When the BFC bit in the TRCMR register is set to 1 (buffer register of TRCGRA register), set the IOC2 bit in theTRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
2. When the BFD bit in the TRCMR register is set to 1 (buffer register of TRCGRB register), set the IOD2 bit in theTRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.

19.5.4 Timer RC Control Register 2 (TRCCR2) for Output Compare Function

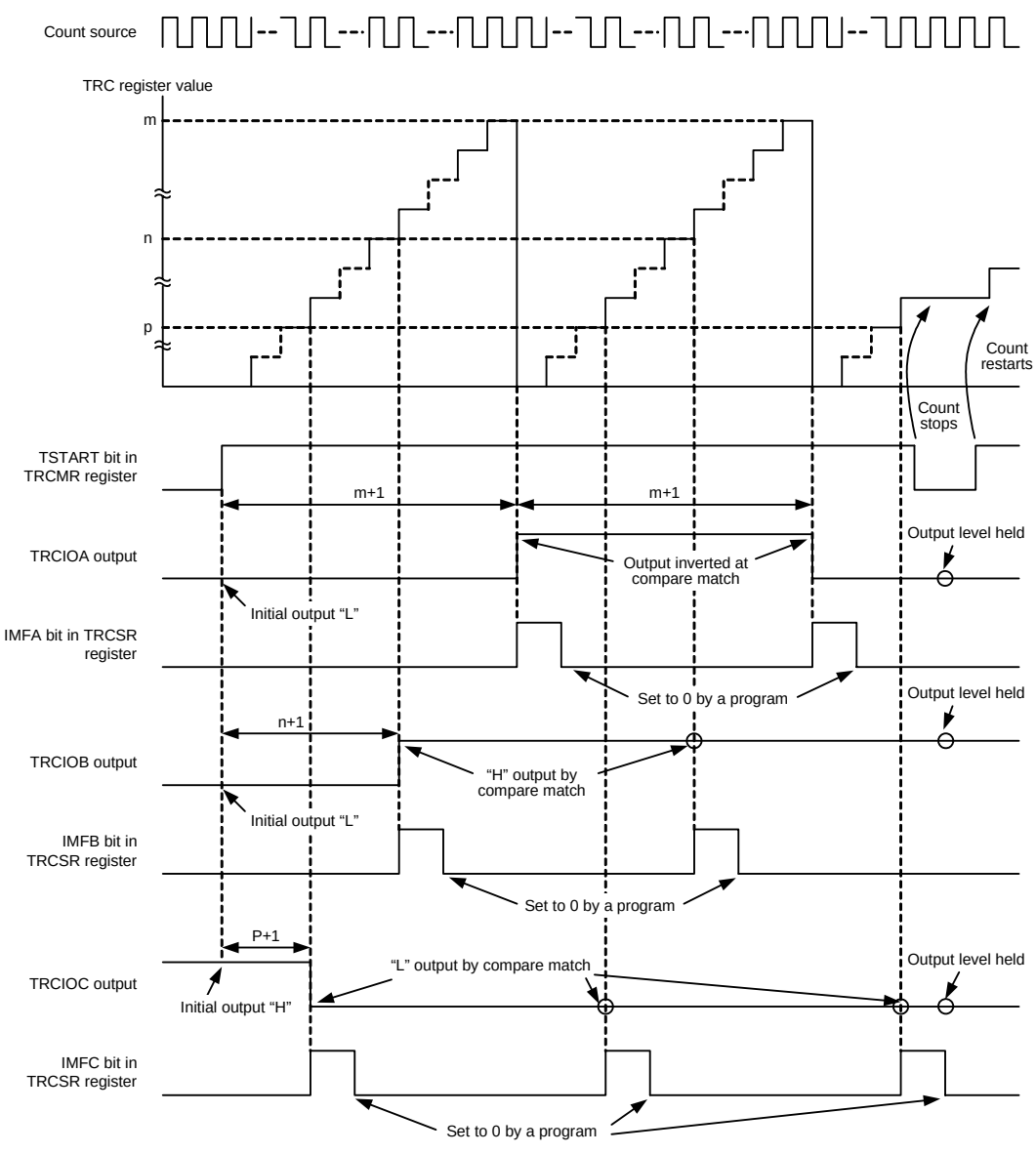
Address 0130h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TCEG1	TCEG0	CSEL	—	—	POLD	POLC	POLB
After Reset	0	0	0	1	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	POLB	PWM mode output level control bit B (1)	0: TRCIOB output level selected as “L” active 1: TRCIOB output level selected as “H” active	R/W
b1	POLC	PWM mode output level control bit C (1)	0: TRCIOC output level selected as “L” active 1: TRCIOC output level selected as “H” active	R/W
b2	POLD	PWM mode output level control bit D (1)	0: TRCIOD output level selected as “L” active 1: TRCIOD output level selected as “H” active	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b4	—			
b5	CSEL	TRC count operation select bit (2)	0: Count continues at compare match with the TRCGRA register 1: Count stops at compare match with the TRCGRA register	R/W
b6	TCEG0	TRCTRG input edge select bit (3)	b7 b6 0 0: Disable the trigger input from the TRCTRG pin 0 1: Rising edge selected 1 0: Falling edge selected 1 1: Both edges selected	R/W
b7	TCEG1			R/W

Notes:
1. Enabled when in PWM mode.
2. Enabled when in the output compare function, PWM mode, or PWM2 mode. For notes on PWM2 mode, refer to **19.9.6 TRCMR Register in PWM2 Mode**.
3. Enabled when in PWM2 mode.

19.5.5 Operating Example



m: TRCGRA register setting value
n: TRCGRB register setting value
p: TRCGRC register setting value

The above applies under the following conditions:
- Bits BFC and BFD in the TRCMR register are set to 0 (TRCGRC and TRCGRD do not operate as buffers).
- Bits EA, EB, and EC in the TRCOER register are set to 0 (output from TRCIOA, TRCIOB, and TRCIOC enabled).
- The CCLR bit in the TRCCR1 register is set to 1 (set the TRC register to 0000h by TRCGRA compare match).
- In the TRCCR1 register, bits TOA and TOB are set to 0 ("L" initial output until compare match) and the TOC bit is set to 1 ("H" initial output until compare match).
- Bits IOA2 to IOA0 in the TRCIOR0 register are set to 011b (TRCIOA output inverted at TRCGRA compare match).
- Bits IOB2 to IOB0 in the TRCIOR0 register are set to 010b ("H" TRCIOB output at TRCGRB compare match).
- Bits IOC2 to IOC2 in the TRCIOR1 register are set to 001b ("L" TRCIOC output at TRCGRC compare match).
- The CSEL bit in the TRCCR2 register is set to 0 (TRC count continues after TRCGRA compare match).

Figure 19.10 Operating Example of Output Compare Function

19.5.6 Changing Output Pins in Registers TRCGRC and TRCGRD

The TRCGRC register can be used for output control of the TRCIOA pin, and the TRCGRD register can be used for output control of the TRCIOB pin. Therefore, each pin output can be controlled as follows:

- TRCIOA output is controlled by the values in registers TRCGRA and TRCGRC.
- TRCIOB output is controlled by the values in registers TRCGRB and TRCGRD.

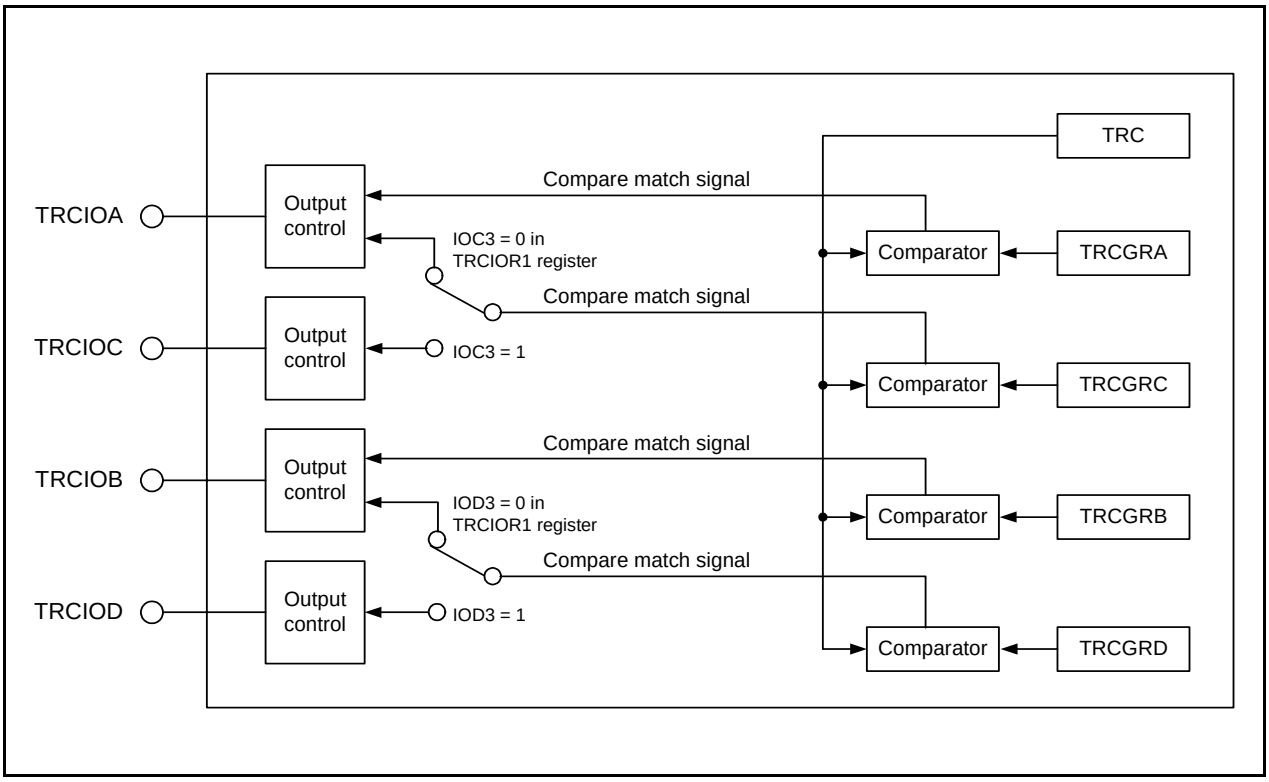
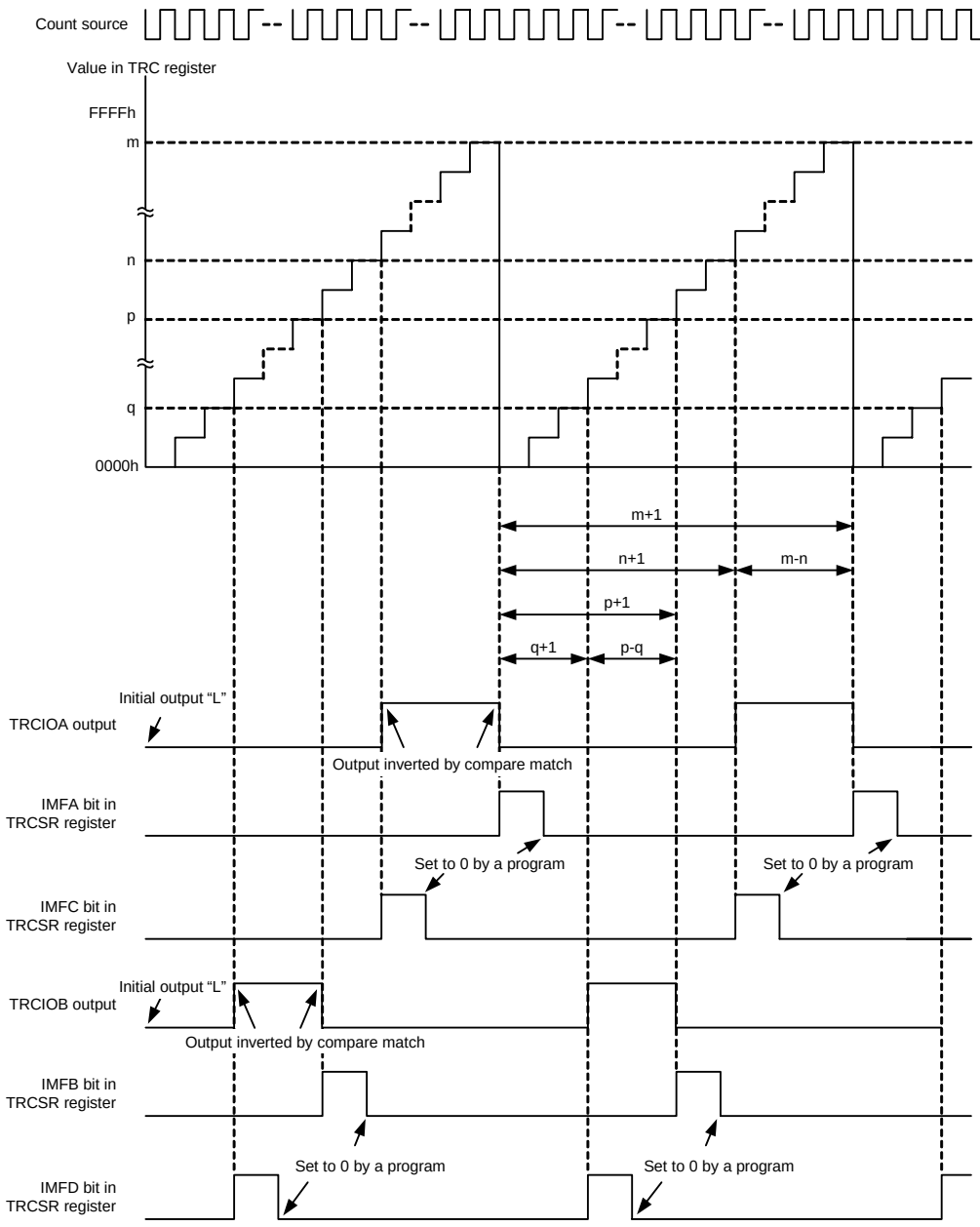


Figure 19.11 Changing Output Pins in Registers TRCGRC and TRCGRD

Change output pins in registers TRCGRC and TRCGRD as follows:

- Set the IOC3 bit in the TRCIOR1 register to 0 (TRCIOA output register) and set the IOD3 bit to 0 (TRCIOB output register).
- Set bits BFC and BFD in the TRCMR register to 0 (general register).
- Set different values in registers TRCGRC and TRCGRA. Also, set different values in registers TRCGRD and TRCGRB.

Figure 19.12 shows an Operating Example When TRCGRC Register is Used for Output Control of TRCIOA Pin and TRCGRD Register is Used for Output Control of TRCIOB Pin.



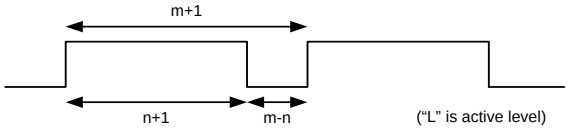
The above applies under the following conditions:
- Bits BFC and BFD in the TRCMR register are set to 0 (registers TRCGRC and TRCGRD are not used as buffer register).
- Bits EA and EB in the TRCOER register are set to 0 (enable TRCIOA and TRCIOB pin outputs).
- The CCLR bit in the TRCCR1 register are set to 1 (set the TRC register to 0000h by compare match in the TRCGRA register).
- Bits TOA and TOB in the TRCCR1 register are set to 0 (initial output "L" to compare match).
- Bits IOA2 to IOA0 in the TRCIOR0 register are set to 011b (TRCIOA output inverted at TRCGRA register compare match).
- Bits IOB2 to IOB0 in the TRCIOR0 register are set to 011b (TRCIOB output inverted at TRCGRB register compare match).
- Bits IOC2 to IOC0 in the TRCIOR1 register are set to 011b (TRCIOA output inverted at TRCGRC register compare match).
- The IOC3 bit in the TRCIOR1 register are set to 0 (TRCIOA output register).
- Bits IOD2 to IOD0 in the TRCIOR1 register are set to 011b (TRCIOB output inverted at TRCGRD register compare match).
- The IOD3 bit in the TRCIOR1 register are set to 0 (TRCIOB output register).
- The CSEL bit in the TRCCR2 register are set to 0 (TRC continues counting after compare match).

Figure 19.12 Operating Example When TRCGRC Register is Used for Output Control of TRCIOA Pin and TRCGRD Register is Used for Output Control of TRCIOB Pin

19.6 PWM Mode

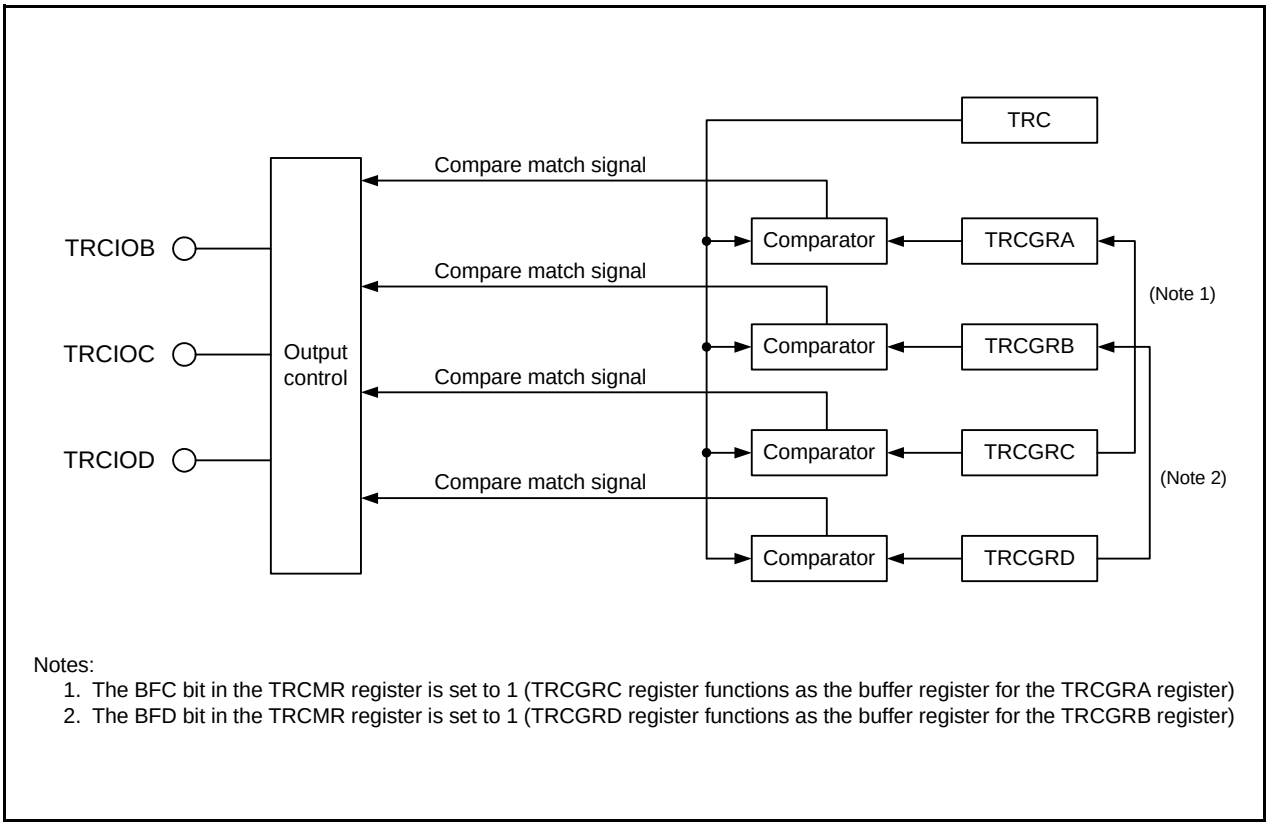
This mode outputs PWM waveforms. A maximum of three PWM waveforms with the same period are output. The PWM mode, or the timer mode, can be selected for each individual pin. (However, since the TRCGRA register is used when using any pin for the PWM mode, the TRCGRA register cannot be used for the timer mode.)
Table 19.11 lists the PWM Mode Specifications, Figure 19.13 shows a PWM Mode Block Diagram, Table 19.12 lists the Functions of TRCGRh Register in PWM Mode, and Figures 19.14 and 19.15 show Operating Examples of PWM Mode.

Table 19.11 PWM Mode Specifications

Item	Specification
Count source	f1, f2, f4, f8, f32, fOCO40M, fOCO-F External signal input to TRCCLK pin (rising edge)
Count operation	Increment
PWM waveform	PWM period: 1/fk × (m+1) Active level width: 1/fk × (m-n) Inactive width: 1/fk × (n+1) fk: Count source frequency m: TRCGRA register setting value n: TRCGRj register setting value 
Count start condition	1 (count starts) is written to the TSTART bit in the TRCMR register.
Count stop condition	• When the CSEL bit in the TRCCR2 register is set to 0 (count continues after compare match with TRCGRA). 0 (count stops) is written to the TSTART bit in the TRCMR register. PWM output pin retains output level before count stops, TRC register retains value before count stops. • When the CSEL bit in the TRCCR2 register is set to 1 (count stops at compare match with TRCGRA register). The count stops at the compare match with the TRCGRA register. The PWM output pin retains the level after the output is changed by the compare match.
Interrupt request generation timing	• Compare match (contents of registers TRC and TRCGRh match) • The TRC register overflows.
TRCIOA pin function	Programmable I/O port
TRCIOB, TRCIOC, and TRCIOD pin functions	Programmable I/O port or PWM output (selectable individually for each pin)
$\overline{\text{INT0}}$ pin function	Programmable I/O port, pulse output forced cutoff signal input, or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read by reading the TRC register.
Write to timer	The TRC register can be written to.
Selectable functions	• One to three pins selectable as PWM output pins One or more of pins TRCIOB, TRCIOC, and TRCIOD • Active level selectable for each pin • Initial level selectable for each pin • Buffer operation (refer to **19.3.2 Buffer Operation**) • Pulse output forced cutoff signal input (refer to **19.3.4 Forced Cutoff of Pulse Output**) • A/D trigger generation (1)

j = B, C, or D
h = A, B, C, or D

Note:
1. Not available in the R8C/3MU Group.



Notes:
1. The BFC bit in the TRCMR register is set to 1 (TRCGRC register functions as the buffer register for the TRCGRA register)
2. The BFD bit in the TRCMR register is set to 1 (TRCGRD register functions as the buffer register for the TRCGRB register)

Figure 19.13 PWM Mode Block Diagram

19.6.1 Timer RC Control Register 1 (TRCCR1) in PWM Mode

Address 0121h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CCLR	TCK2	TCK1	TCK0	TOD	TOC	TOB	TOA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOA	TRCIOA output level select bit (1)	Disabled in PWM mode	R/W
b1	TOB	TRCIOB output level select bit (1, 2)	0: Initial output selected as non-active level 1: Initial output selected as active level	R/W
b2	TOC	TRCIOC output level select bit (1, 2)		R/W
b3	TOD	TRCIOD output level select bit (1, 2)		R/W
b4	TCK0	Count source select bit (1)	b6 b5 b4 0 0 0: f1 0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: TRCCLK input rising edge 1 1 0: fOCO40M 1 1 1: fOCO-F (3)	R/W
b5	TCK1			R/W
b6	TCK2			R/W
b7	CCLR	TRC counter clear select bit	0: Disable clear (free-running operation) 1: Clear by compare match in the TRCGRA register	R/W

Notes:
1. Set to these bits when the TSTART bit in the TRCMR register is set to 0 (count stops).
2. If the pin function is set for waveform output (refer to **7.5 Port Settings**), the initial output level is output when the TRCCR1 register is set.
3. To select fOCO-F, set it to the clock frequency higher than the CPU clock frequency.

19.6.2 Timer RC Control Register 2 (TRCCR2) in PWM Mode

Address 0130h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TCEG1	TCEG0	CSEL	—	—	POLD	POLC	POLB
After Reset	0	0	0	1	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	POLB	PWM mode output level control bit B (1)	0: TRCIOB output level selected as “L” active 1: TRCIOB output level selected as “H” active	R/W
b1	POLC	PWM mode output level control bit C (1)	0: TRCIOC output level selected as “L” active 1: TRCIOC output level selected as “H” active	R/W
b2	POLD	PWM mode output level control bit D (1)	0: TRCIOD output level selected as “L” active 1: TRCIOD output level selected as “H” active	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b4	—			
b5	CSEL	TRC count operation select bit (2)	0: Count continues at compare match with the TRCGRA register 1: Count stops at compare match with the TRCGRA register	R/W
b6	TCEG0	TRCTRG input edge select bit (3)	b7 b6 0 0: Disable the trigger input from the TRCTRG pin 0 1: Rising edge selected 1 0: Falling edge selected 1 1: Both edges selected	R/W
b7	TCEG1			R/W

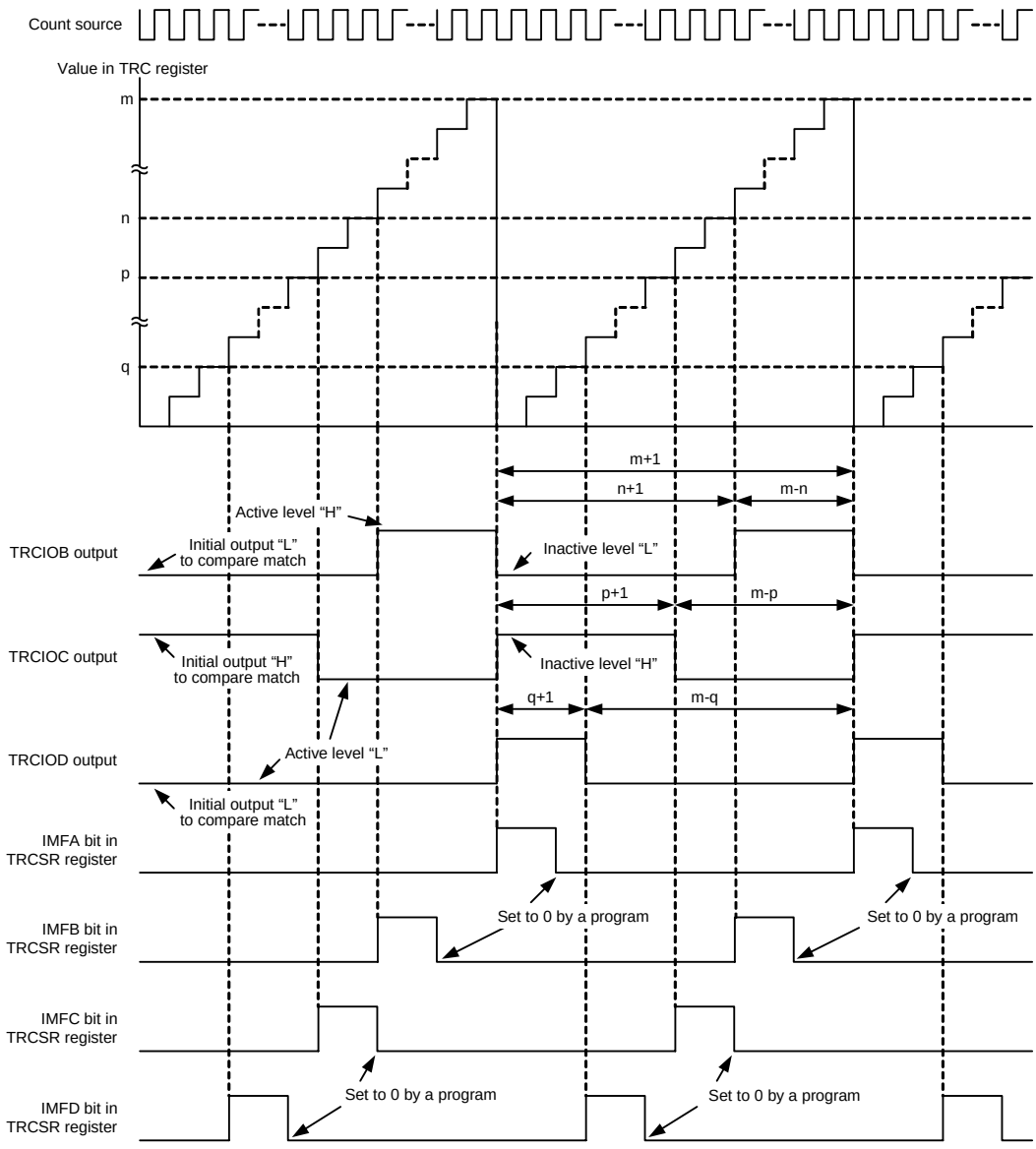
Notes:
1. Enabled when in PWM mode.
2. Enabled when in the output compare function, PWM mode, or PWM2 mode. For notes on PWM2 mode, refer to **19.9.6 TRCMR Register in PWM2 Mode**.
3. Enabled when in PWM2 mode.

Table 19.12 Functions of TRCGRh Register in PWM Mode

Register	Setting	Register Function	PWM Output Pin
TRCGRA	—	General register. Set the PWM period.	—
TRCGRB	—	General register. Set the PWM output change point.	TRCIOB
TRCGRC	BFC = 0	General register. Set the PWM output change point.	TRCIOC
TRCGRD	BFD = 0		TRCIOD
TRCGRC	BFC = 1	Buffer register. Set the next PWM period (refer to **19.3.2 Buffer Operation**).	—
TRCGRD	BFD = 1	Buffer register. Set the next PWM output change point (refer to **19.3.2 Buffer Operation**).	TRCIOB

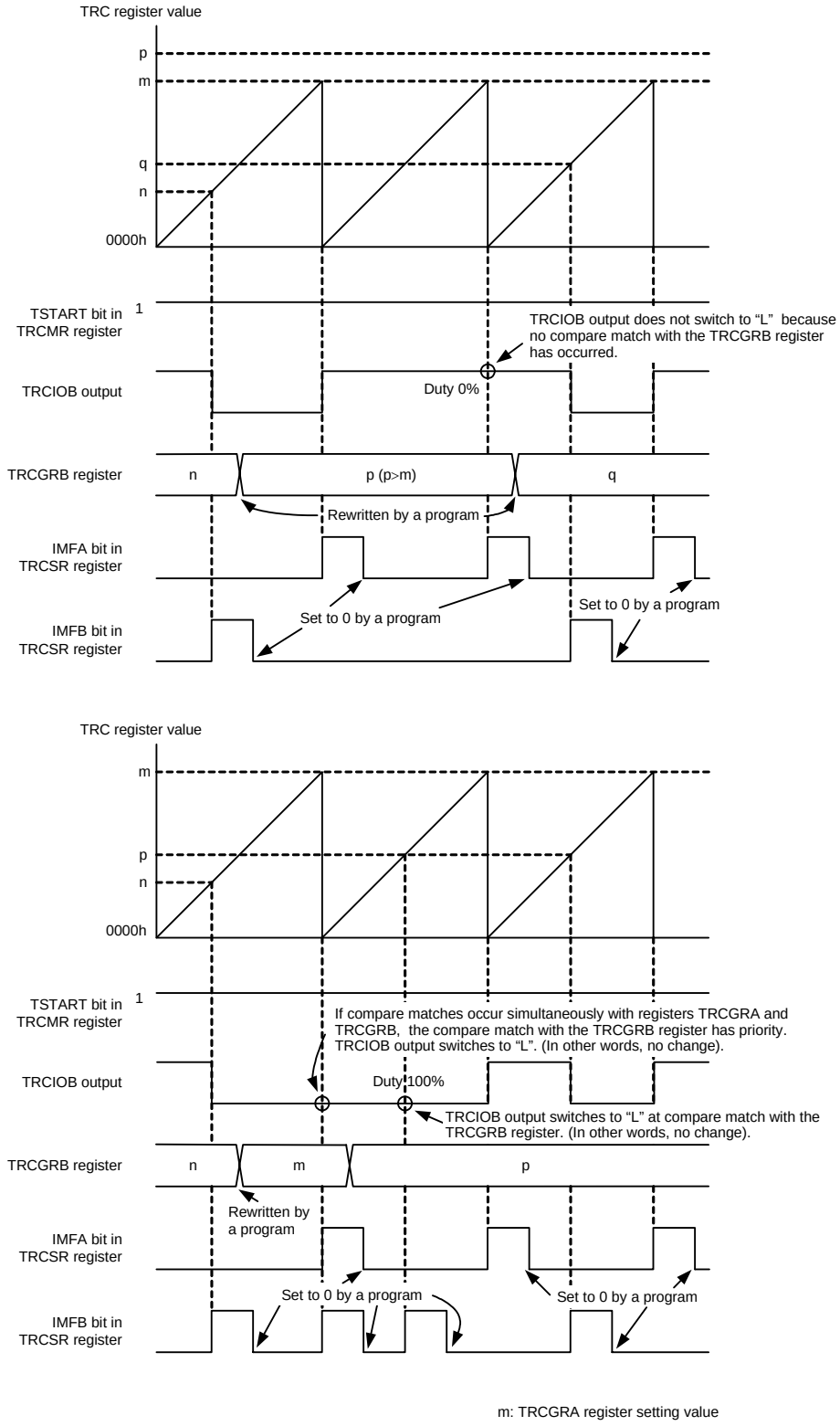
h = A, B, C, or D
BFC, BFD: Bits in TRCMR register
Note:
1. The output level does not change even when a compare match occurs if the TRCGRA register value (PWM period) is the same as the TRCGRB, TRCGRC, or TRCGRD register value.

19.6.3 Operating Example



The above applies under the following conditions:
- Bits BFC and BFD in the TRCMR register are set to 0 (registers TRCGRC and TRCGRD do not operate as buffers).
- Bits EB, EC, and ED in the TRCOER register are set to 0 (output from TRCIOB, TRCIOC, and TRCIOD enabled).
- Bits TOB and TOC in the TRCCR1 register are set to 0 (inactive level), the TOD bit is set to 1 (active level).
- The POLB bit in the TRCCR2 register is set to 1 ("H" active), bits POLC and POLD are set to 0 ("L" active).

Figure 19.14 Operating Example of PWM Mode

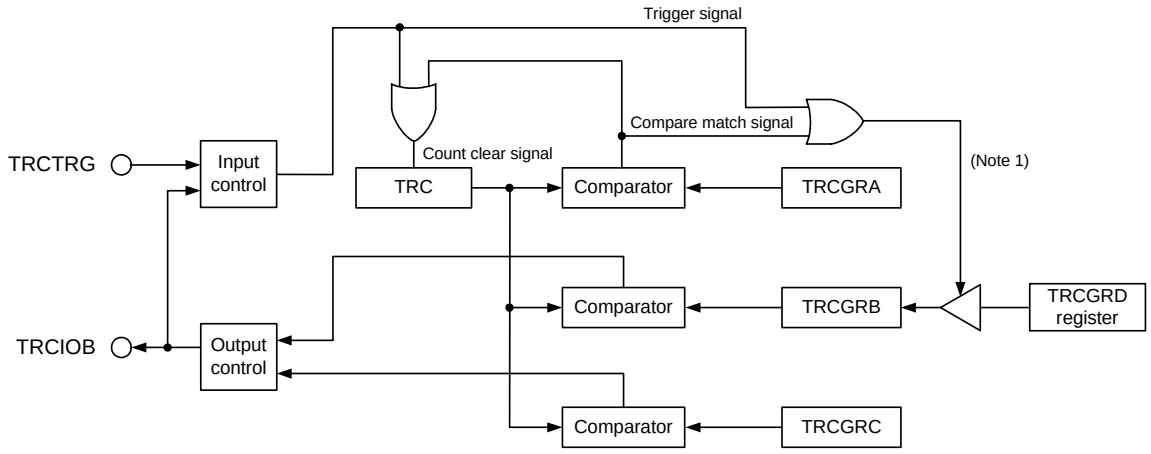


The above applies under the following conditions:
- The EB bit in the TRCOER register is set to 0 (output from TRCIOB enabled).
- The POLB bit in the TRCCR2 register is set to 0 ("L" active).

Figure 19.15 Operating Example of PWM Mode (Duty 0% and Duty 100%)

19.7 PWM2 Mode

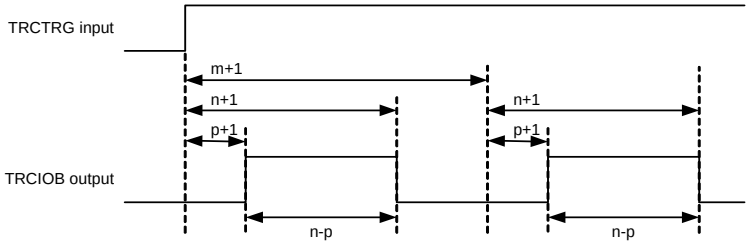
This mode outputs a single PWM waveform. After a given wait duration has elapsed following the trigger, the pin output switches to active level. Then, after a given duration, the output switches back to inactive level. Furthermore, the counter stops at the same time the output returns to inactive level, making it possible to use PWM2 mode to output a programmable wait one-shot waveform.
Since timer RC uses multiple general registers in PWM2 mode, other modes cannot be used in conjunction with it. Figure 19.16 shows a PWM2 Mode Block Diagram, Table 19.13 lists the PWM2 Mode Specifications, Table 19.14 lists the Functions of TRCGRj Register in PWM2 Mode, and Figures 19.17 to 19.19 show Operating Examples of PWM2 Mode.



Note:
1. The BFD bit in the TRCMR register is set to 1 (the TRCGRD register functions as the buffer register for the TRCGRB register).

Figure 19.16 PWM2 Mode Block Diagram

Table 19.13 PWM2 Mode Specifications

Item	Specification
Count source	f1, f2, f4, f8, f32, fOCO40M, fOCO-F External signal input to TRCCLK pin (rising edge)
Count operation	Increment TRC register
PWM waveform	PWM period: 1/fk × (m+1) (no TRCTRG input) Active level width: 1/fk × (n-p) Wait time from count start or trigger: 1/fk × (p+1) fk: Count source frequency m: TRCGRA register setting value n: TRCGRB register setting value p: TRCGRC register setting value  (TRCTRG: Rising edge, active level is "H")
Count start conditions	• Bits TCEG1 to TCEG0 in the TRCCR2 register are set to 00b (TRCTRG trigger disabled) or the CSEL bit in the TRCCR2 register is set to 0 (count continues). 1 (count starts) is written to the TSTART bit in the TRCMR register. • Bits TCEG1 to TCEG0 in the TRCCR2 register are set to 01b, 10b, or 11b (TRCTRG trigger enabled) and the TSTART bit in the TRCMR register is set to 1 (count starts). A trigger is input to the TRCTRG pin
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRCMR register while the CSEL bit in the TRCCR2 register is set to 0 or 1. The TRCIOB pin outputs the initial level in accordance with the value of the TOB bit in the TRCCR1 register. The TRC register retains the value before count stops. • The count stops due to a compare match with TRCGRA while the CSEL bit in the TRCCR2 register is set to 1 The TRCIOB pin outputs the initial level. The TRC register retains the value before count stops if the CCLR bit in the TRCCR1 register is set to 0. The TRC register is set to 0000h if the CCLR bit in the TRCCR1 register is set to 1.
Interrupt request generation timing	• Compare match (contents of TRC and TRCGRj registers match) • The TRC register overflows
TRCIOA/TRCTRG pin function	Programmable I/O port or TRCTRG input
TRCIOB pin function	PWM output
TRCIOC and TRCIOD pin functions	Programmable I/O port
$\overline{\text{INT0}}$ pin function	Programmable I/O port, pulse output forced cutoff signal input, or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read by reading the TRC register.
Write to timer	The TRC register can be written to.
Selectable functions	• External trigger and valid edge selection The edge or edges of the signal input to the TRCTRG pin can be used as the PWM output trigger: rising edge, falling edge, or both rising and falling edges • Buffer operation (refer to **19.3.2 Buffer Operation**) • Pulse output forced cutoff signal input (refer to **19.3.4 Forced Cutoff of Pulse Output**) • Digital filter (refer to **19.3.3 Digital Filter**) • A/D trigger generation (1)

j = A, B, or C

Note:
1. Not available in the R8C/3MU Group.

19.7.1 Timer RC Control Register 1 (TRCCR1) in PWM2 Mode

Address 0121h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CCLR	TCK2	TCK1	TCK0	TOD	TOC	TOB	TOA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOA	TRCIOA output level select bit (1)	Disabled in PWM2 mode	R/W
b1	TOB	TRCIOB output level select bit (1, 2)	0: Active level “H” (Initial output “L” “H” output by compare match in the TRCGRC register “L” output by compare match in the TRCGRB register) 1: Active level “L” (Initial output “H” “L” output by compare match in the TRCGRC register “H” output by compare match in the TRCGRB register)	R/W
b2	TOC	TRCIOC output level select bit (1)	Disabled in PWM2 mode	R/W
b3	TOD	TRCIOD output level select bit (1)		R/W
b4	TCK0	Count source select bit (1)	b6 b5 b4 0 0 0: f1 0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: TRCCLK input rising edge 1 1 0: fOCO40M 1 1 1: fOCO-F (3)	R/W
b5	TCK1			R/W
b6	TCK2			R/W
b7	CCLR	TRC counter clear select bit	0: Disable clear (free-running operation) 1: Clear by compare match in the TRCGRA register	R/W

Notes:
1. Set to these bits when the TSTART bit in the TRCMR register is set to 0 (count stops).
2. If the pin function is set for waveform output (refer to **7.5 Port Settings**), the initial output level is output when the TRCCR1 register is set.
3. To select fOCO-F, set it to the clock frequency higher than the CPU clock frequency.

19.7.2 Timer RC Control Register 2 (TRCCR2) in PWM2 Mode

Address 0130h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TCEG1	TCEG0	CSEL	—	—	POLD	POLC	POLB
After Reset	0	0	0	1	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	POLB	PWM mode output level control bit B (1)	0: TRCIOB output level selected as “L” active 1: TRCIOB output level selected as “H” active	R/W
b1	POLC	PWM mode output level control bit C (1)	0: TRCIOC output level selected as “L” active 1: TRCIOC output level selected as “H” active	R/W
b2	POLD	PWM mode output level control bit D (1)	0: TRCIOD output level selected as “L” active 1: TRCIOD output level selected as “H” active	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b4	—			
b5	CSEL	TRC count operation select bit (2)	0: Count continues at compare match with the TRCGRA register 1: Count stops at compare match with the TRCGRA register	R/W
b6	TCEG0	TRCTRG input edge select bit (3)	b7 b6 0 0: Disable the trigger input from the TRCTRG pin 0 1: Rising edge selected 1 0: Falling edge selected 1 1: Both edges selected	R/W
b7	TCEG1			R/W

Notes:
1. Enabled when in PWM mode.
2. Enabled when in the output compare function, PWM mode, or PWM2 mode. For notes on PWM2 mode, refer to **19.9.6 TRCMR Register in PWM2 Mode**.
3. Enabled when in PWM2 mode.

19.7.3 Timer RC Digital Filter Function Select Register (TRCDF) in PWM2 Mode

Address 0131h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	DFCK1	DFCK0	—	DFTRG	DFD	DFC	DFB	DFA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	DFA	TRCIOA pin digital filter function select bit (1)	0: Function is not used 1: Function is used	R/W
b1	DFB	TRCIOB pin digital filter function select bit (1)		R/W
b2	DFC	TRCIOC pin digital filter function select bit (1)		R/W
b3	DFD	TRCIOD pin digital filter function select bit (1)		R/W
b4	DFTRG	TRCTRG pin digital filter function select bit (2)		R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b6	DFCK0	Clock select bits for digital filter function (1, 2)	b7 b6 0 0: f32 0 1: f8 1 0: f1 1 1: Count source (clock selected by bits TCK2 to TCK0 in the TRCCR1 register)	R/W
b7	DFCK1			R/W

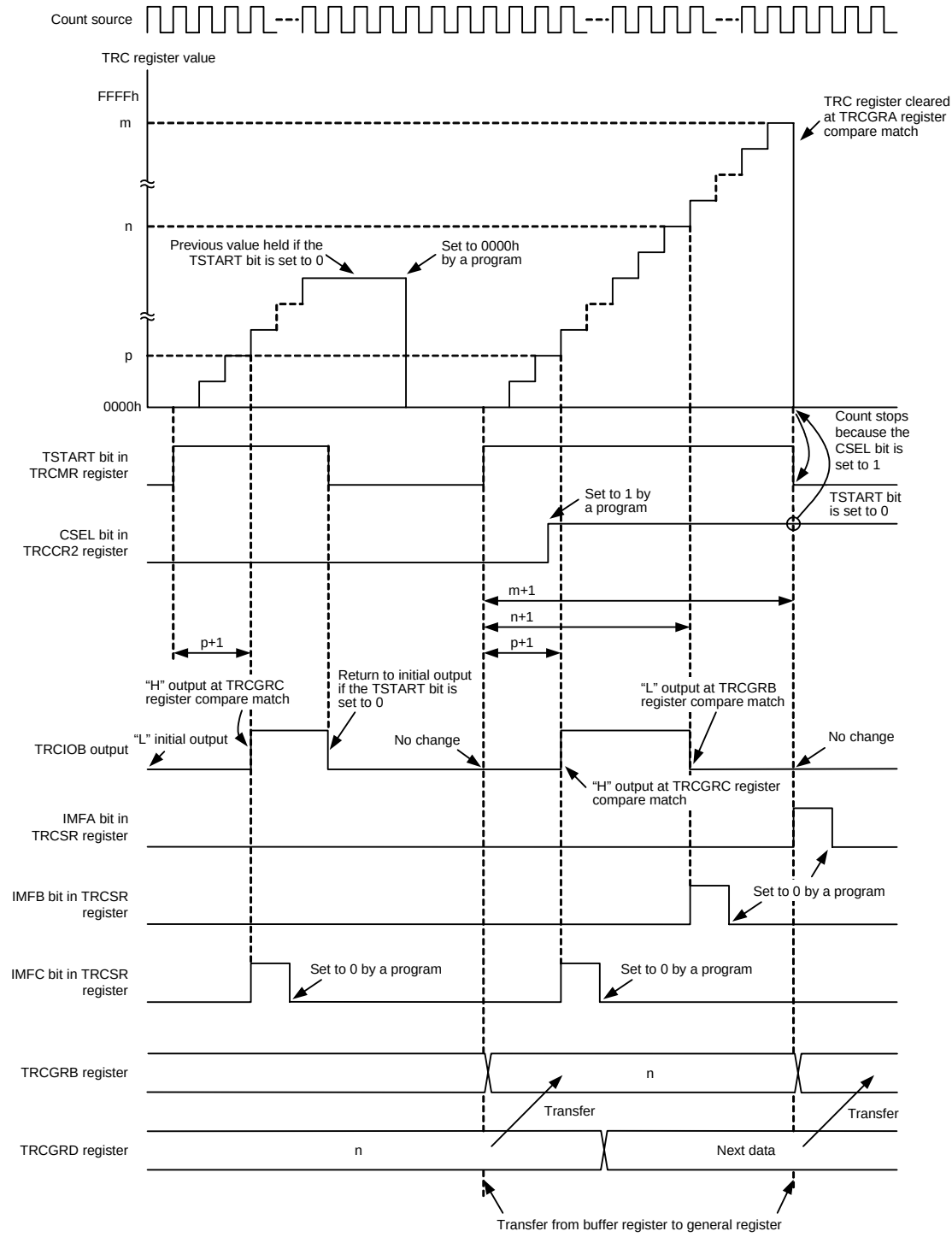
Notes:
1. These bits are enabled for the input capture function.
2. These bits are enabled when in PWM2 mode and bits TCEG1 to TCEG0 in the TRCCR2 register are set to 01b, 10b, or 11b (TRCTRG trigger input enabled).

Table 19.14 Functions of TRCGRj Register in PWM2 Mode

Register	Setting	Register Function	PWM2 Output Pin
TRCGRA	—	General register. Set the PWM period.	TRCIOB pin
TRCGRB (1)	—	General register. Set the PWM output change point.	
TRCGRC (1)	BFC = 0	General register. Set the PWM output change point (wait time after trigger).	
TRCGRD	BFD = 0	(Not used in PWM2 mode)	—
TRCGRD	BFD = 1	Buffer register. Set the next PWM output change point (refer to **19.3.2 Buffer Operation**).	TRCIOB pin

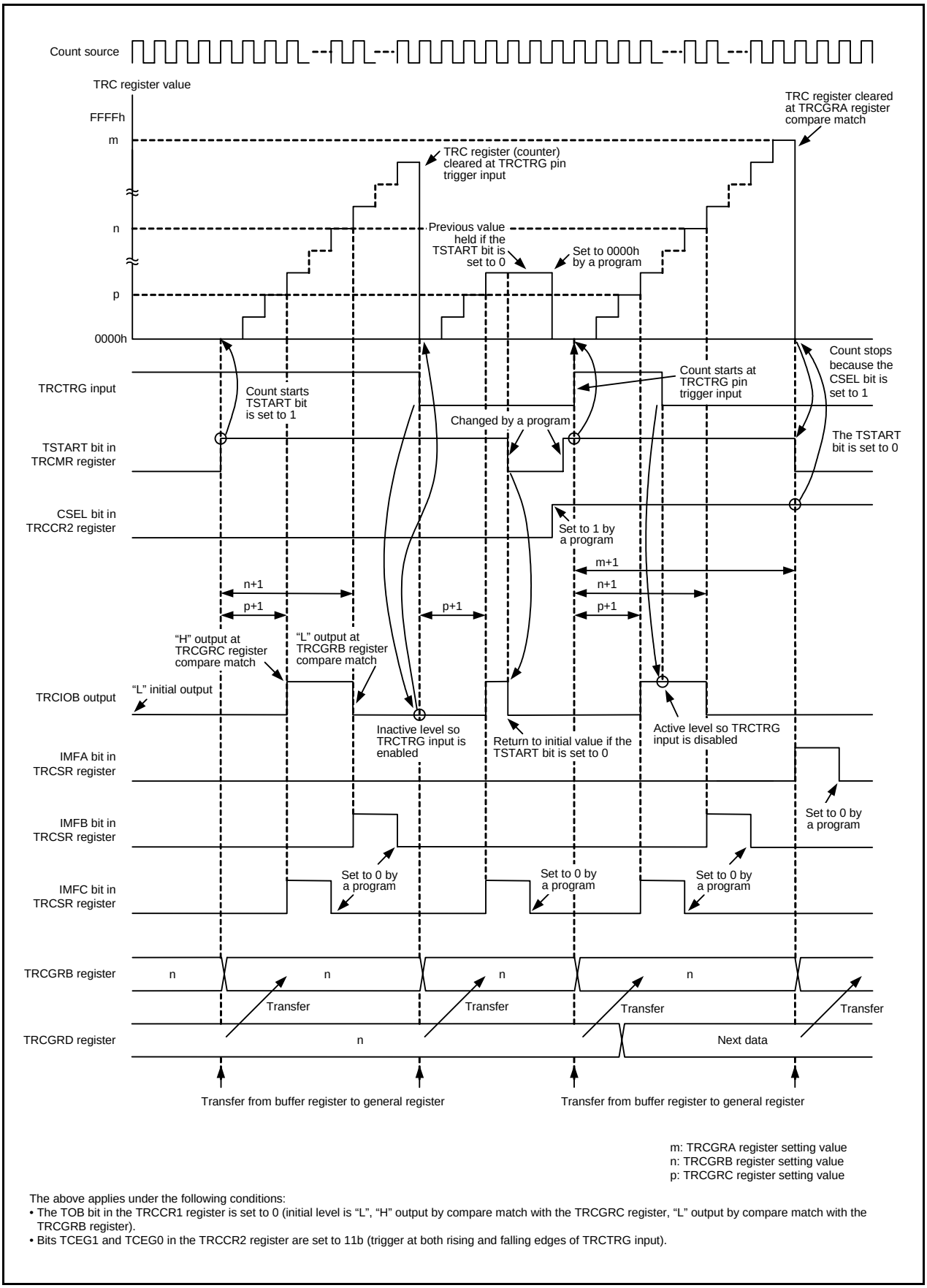
j = A, B, C, or D
BFC, BFD: Bits in TRCMR register
Note:
1. Do not set the TRCGRB and TRCGRC registers to the same value.

19.7.4 Operating Example



The above applies under the following conditions:
- The TOB bit in the TRCCR1 register is set to 0 (initial level is "L", "H" output by compare match with the TRCGRC register, "L" output by compare match with the TRCGRB register).
- Bits TCEG1 and TCEG0 in the TRCCR2 register are set to 00b (TRCTRG trigger input disabled).

Figure 19.17 Operating Example of PWM2 Mode (TRCTRG Trigger Input Disabled)



The above applies under the following conditions:
- The TOB bit in the TRCCR1 register is set to 0 (initial level is "L", "H" output by compare match with the TRCGRC register, "L" output by compare match with the TRCGRB register).
- Bits TCEG1 and TCEG0 in the TRCCR2 register are set to 11b (trigger at both rising and falling edges of TRCTRG input).

Figure 19.18 Operating Example of PWM2 Mode (TRCTRG Trigger Input Enabled)

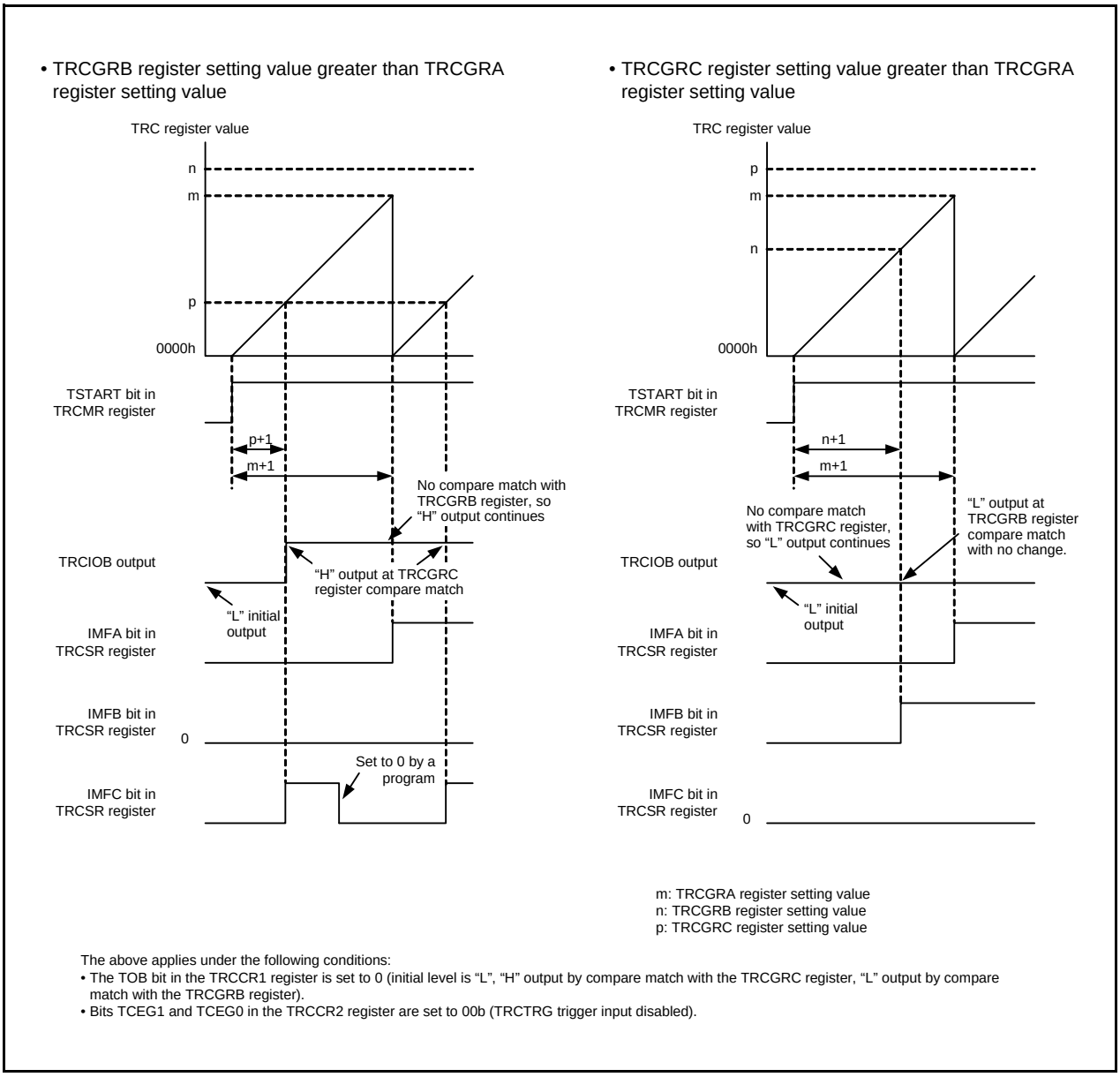


Figure 19.19 Operating Example of PWM2 Mode (Duty 0% and Duty 100%)

19.8 Timer RC Interrupt

Timer RC generates a timer RC interrupt request from five sources. The timer RC interrupt uses the single TRCIC register (bits IR and ILVL0 to ILVL2) and a single vector.
Table 19.15 lists the Registers Associated with Timer RC Interrupt and Figure 19.20 is a Timer RC Interrupt Block Diagram.

Table 19.15 Registers Associated with Timer RC Interrupt

Timer RC Status Register	Timer RC Interrupt Enable Register	Timer RC Interrupt Control Register
TRCSR	TRCIER	TRCIC

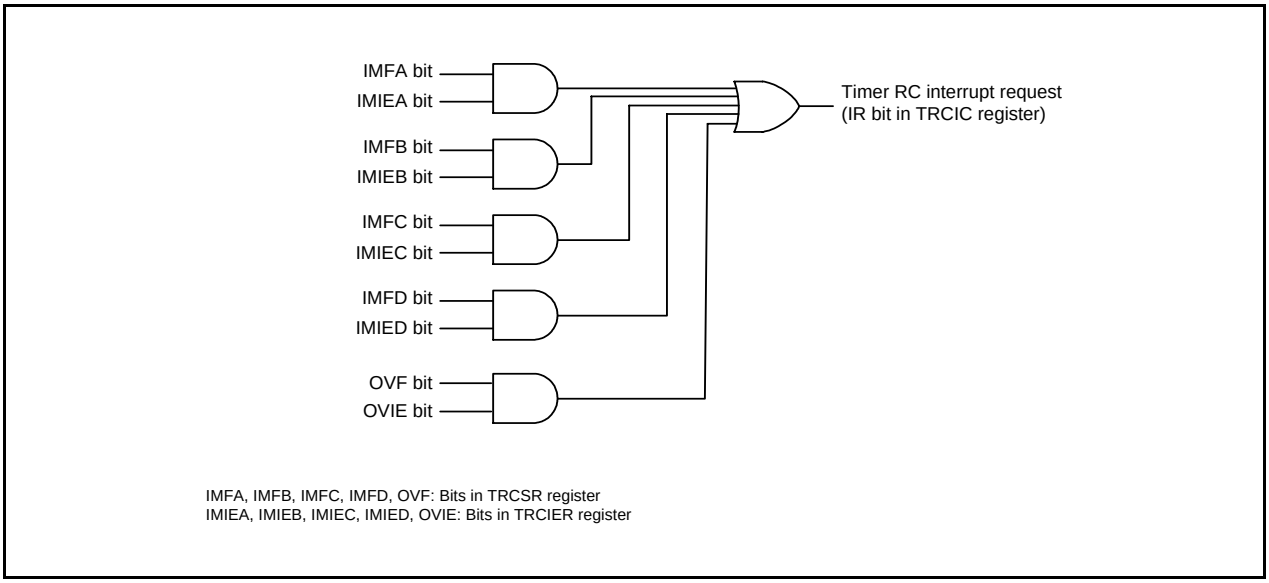


Figure 19.20 Timer RC Interrupt Block Diagram

Like other maskable interrupts, the timer RC interrupt is controlled by the combination of the I flag, IR bit, bits ILVL0 to ILVL2, and IPL. However, it differs from other maskable interrupts in the following respects because a single interrupt source (timer RC interrupt) is generated from multiple interrupt request sources.

- The IR bit in the TRCIC register is set to 1 (interrupt requested) when a bit in the TRCSR register is set to 1 and the corresponding bit in the TRCIER register is also set to 1 (interrupt enabled).
- The IR bit is set to 0 (no interrupt requested) when the bit in the TRCSR register or the corresponding bit in the TRCIER register is set to 0, or both are set to 0. In other words, the interrupt request is not maintained if the IR bit is once set to 1 but the interrupt is not acknowledged.
- If another interrupt source is triggered after the IR bit is set to 1, the IR bit remains set to 1 and does not change.
- If multiple bits in the TRCIER register are set to 1, use the TRCSR register to determine the source of the interrupt request.
- The bits in the TRCSR register are not automatically set to 0 when an interrupt is acknowledged. Set them to 0 within the interrupt routine. Refer to **19.2.5 Timer RC Status Register (TRCSR)**, for the procedure for setting these bits to 0.

Refer to **19.2.4 Timer RC Interrupt Enable Register (TRCIER)**, for details of the TRCIER register.
Refer to **11.3 Interrupt Control**, for details of the TRCIC register and **11.1.5.2 Relocatable Vector Tables**, for information on interrupt vectors.

19.9 Notes on Timer RC

19.9.1 TRC Register

- The following note applies when the CCLR bit in the TRCCR1 register is set to 1 (clear TRC register at compare match with TRCGRA register).
  When using a program to write a value to the TRC register while the TSTART bit in the TRCMR register is set to 1 (count starts), ensure that the write does not overlap with the timing with which the TRC register is set to 0000h.
  If the timing of the write to the TRC register and the setting of the TRC register to 0000h coincide, the write value will not be written to the TRC register and the TRC register will be set to 0000h.

- Reading from the TRC register immediately after writing to it can result in the value previous to the write being read out. To prevent this, execute the JMP.B instruction between the read and the write instructions.

```
Program Example     MOV.W   #XXXXh, TRC    ; Write
                    JMP.B   L1             ; JMP.B instruction
                L1: MOV.W   TRC, DATA      ; Read
```

19.9.2 TRCSR Register

Reading from the TRCSR register immediately after writing to it can result in the value previous to the write being read out. To prevent this, execute the JMP.B instruction between the read and the write instructions.

```
Program Example     MOV.B   #XXh, TRCSR    ; Write
                    JMP.B   L1             ; JMP.B instruction
                L1: MOV.B   TRCSR, DATA    ; Read
```

19.9.3 TRCCR1 Register

To set bits TCK2 to TCK0 in the TRCCR1 register to 111b (fOCO-F), set fOCO-F to the clock frequency higher than the CPU clock frequency.

19.9.4 Count Source Switching

- Stop the count before switching the count source.

Switching procedure
(1) Set the TSTART bit in the TRCMR register to 0 (count stops).
(2) Change the settings of bits TCK2 to TCK0 in the TRCCR1 register.

- After switching the count source from fOCO40M to another clock, allow a minimum of two cycles of f1 to elapse after changing the clock setting before stopping fOCO40M.

Switching procedure
(1) Set the TSTART bit in the TRCMR register to 0 (count stops).
(2) Change the settings of bits TCK2 to TCK0 in the TRCCR1 register.
(3) Wait for a minimum of two cycles of f1.
(4) Set the FRA00 bit in the FRA0 register to 0 (high-speed on-chip oscillator off).

- After switching the count source from fOCO-F to fOCO40M, allow a minimum of two cycles of fOCO-F to elapse after changing the clock setting before stopping fOCO-F.

Switching procedure
(1) Set the TSTART bit in the TRCMR register to 0 (count stops).
(2) Change the settings of bits TCK2 to TCK0 in the TRCCR1 register.
(3) Wait for a minimum of two cycles of fOCO-F.
(4) Set the FRA00 bit in the FRA0 register to 0 (high-speed on-chip oscillator off).

- After switching the count source from fOCO-F to a clock other than fOCO40M, allow a minimum of one cycle of fOCO-F + fOCO40M to elapse after changing the clock setting before stopping fOCO-F.

Switching procedure
(1) Set the TSTART bit in the TRCMR register to 0 (count stops).
(2) Change the settings of bits TCK2 to TCK0 in the TRCCR1 register.
(3) Wait for a minimum of one cycle of fOCO-F + fOCO40M.
(4) Set the FRA00 bit in the FRA0 register to 0 (high-speed on-chip oscillator off).

19.9.5 Input Capture Function

- Set the pulse width of the input capture signal as follows:
  [When the digital filter is not used]
  Three or more cycles of the timer RC operation clock (refer to **Table 19.1 Timer RC Operation Clocks**)
  [When the digital filter is used]
  Five cycles of the digital filter sampling clock + three cycles of the timer RC operating clock, minimum (refer to **Figure 19.5 Digital Filter Block Diagram**)
- The value of the TRC register is transferred to the TRCGRj register one or two cycles of the timer RC operation clock after the input capture signal is input to the TRCIOj (j = A, B, C, or D) pin (when the digital filter function is not used).

19.9.6 TRCMR Register in PWM2 Mode

When the CSEL bit in the TRCCR2 register is set to 1 (count stops at compare match with the TRCGRA register), do not set the TRCMR register at compare match timing of registers TRC and TRCGRA.

19.9.7 Count Source fOCO40M

The count source fOCO40M can be used with supply voltage VCC = 2.7 to 5.5 V. For supply voltage other than that, do not set bits TCK2 to TCK0 in the TRCCR1 register to 110b (select fOCO40M as the count source).

20. Serial Interface (UARTi (i = 0, 1, 3))

The serial interface consists of four channels, UART0 to UART3. This chapter describes the UARTi (i = 0, 1, 3).

20.1 Overview

UART0, UART1, and UART3 have a dedicated timer to generate a transfer clock and operate independently. UART0, UART1, and UART3 support clock synchronous serial I/O mode and clock asynchronous serial I/O mode (UART mode).

Figure 20.1 shows a UARTi (i = 0, 1, 3) Block Diagram. Figure 20.2 shows a Block Diagram of UARTi Transmit/Receive Unit. Table 20.1 lists the Pin Configuration of UARTi (i = 0, 1, 3).

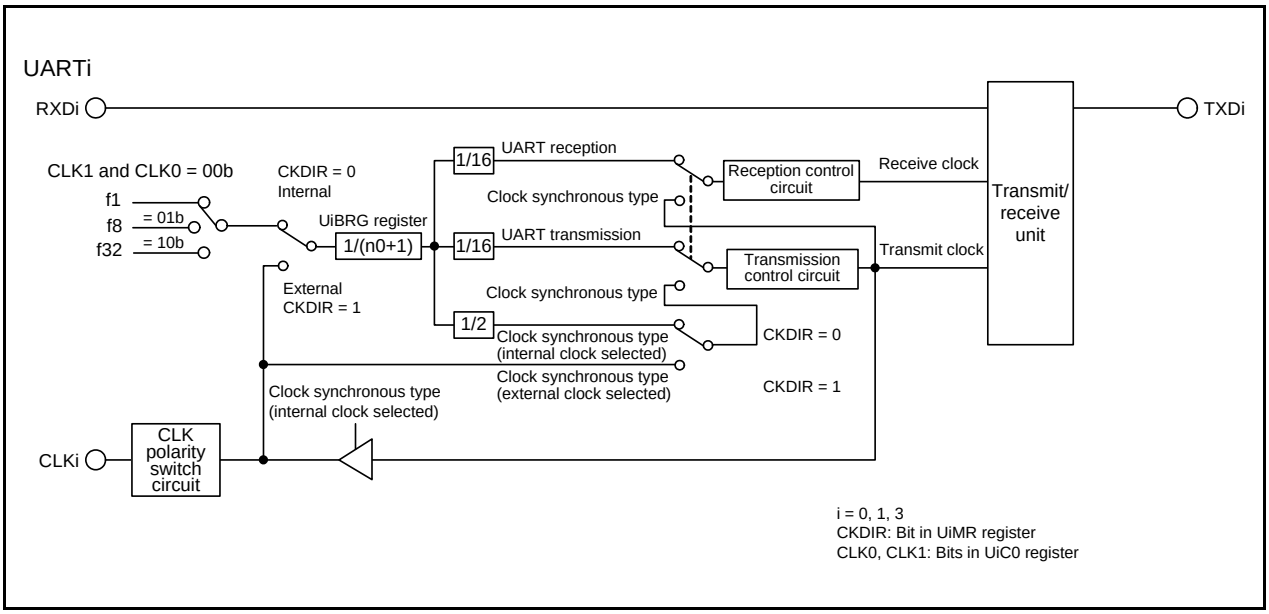


Figure 20.1 UARTi (i = 0, 1, 3) Block Diagram

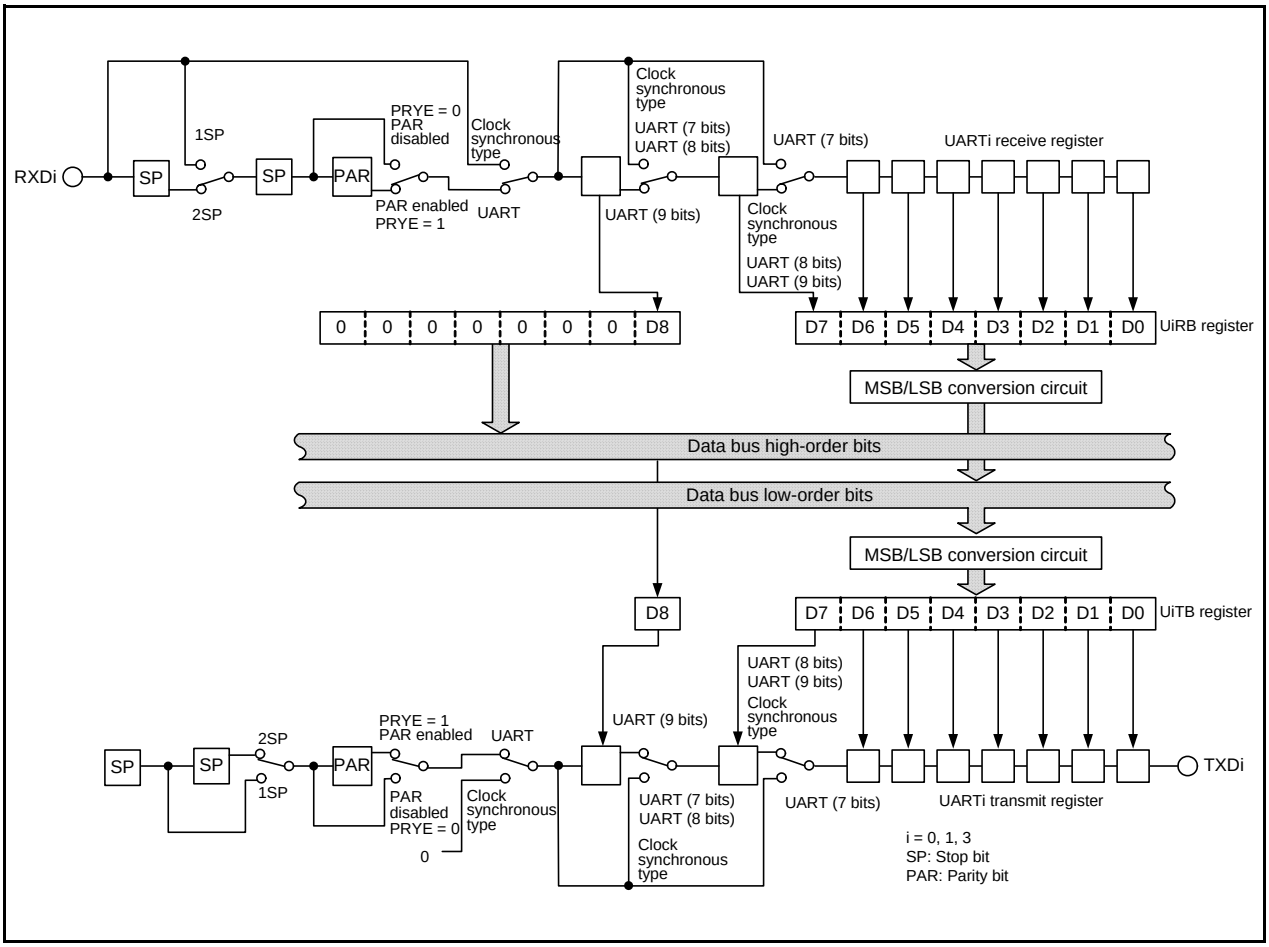


Figure 20.2 Block Diagram of UARTi Transmit/Receive Unit

Table 20.1 Pin Configuration of UARTi (i = 0, 1, 3)

Pin Name	Assigned Pin	I/O	Function
TXD0	P1_4	Output	Serial data output
RXD0	P1_5	Input	Serial data input
CLK0	P1_6	I/O	Transfer clock I/O
TXD1	P0_1	Output	Serial data output
RXD1	P0_2	Input	Serial data input
CLK1	P0_3, or P6_5	I/O	Transfer clock I/O
TXD3	P8_2	Output	Serial data output
RXD3	P8_3	Input	Serial data input
CLK3	P8_1	I/O	Transfer clock I/O

20.2 Registers

20.2.1 UARTi Transmit/Receive Mode Register (UiMR) (i = 0, 1, 3)

Address 00A0h (U0MR), 0160h (U1MR), 168h (U3MR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	PRYE	PRY	STPS	CKDIR	SMD2	SMD1	SMD0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	SMD0	Serial I/O mode select bit	b2 b1 b0 0 0 0: Serial interface disabled 0 0 1: Clock synchronous serial I/O mode 1 0 0: UART mode, transfer data 7 bits long 1 0 1: UART mode, transfer data 8 bits long 1 1 0: UART mode, transfer data 9 bits long Other than above: Do not set.	R/W
b1	SMD1			R/W
b2	SMD2			R/W
b3	CKDIR	Internal/external clock select bit	0: Internal clock 1: External clock	R/W
b4	STPS	Stop bit length select bit	0: One stop bit 1: Two stop bits	R/W
b5	PRY	Odd/even parity select bit	Enabled when PRYE = 1 0: Odd parity 1: Even parity	R/W
b6	PRYE	Parity enable bit	0: Parity disabled 1: Parity enabled	R/W
b7	—	Reserved bit	Set to 0.	R/W

20.2.2 UARTi Bit Rate Register (UiBRG) (i = 0, 1, 3)

Address 00A1h (U0BRG), 0161h (U1BRG), 169h (U3BRG)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	Setting Range	R/W
b7 to b0	If the setting value is n, UiBRG divides the count source by n+1.	00h to FFh	W

Write to the UiBRG register while transmission and reception stop.
Use the MOV instruction to write to this register.
Set bits CLK0 and CLK1 in the UiC0 register before writing to the UiBRG register.

20.2.3 UARTi Transmit Buffer Register (UiTB) (i = 0, 1, 3)

Address 00A3h to 00A2h (U0TB), 0163h to 0162h (U1TB), 016Bh to 016Ah (U3TB)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Function	R/W
b0	—	Transmit data	W
b1	—		
b2	—		
b3	—		
b4	—		
b5	—		
b6	—		
b7	—		
b8	—		
b9	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.	—
b10	—		
b11	—		
b12	—		
b13	—		
b14	—		
b15	—		

If the transfer data is 9 bits long, write data to the high-order byte first, then low-order byte of the UiTB register. Use the MOV instruction to write to this register.

20.2.4 UARTi Transmit/Receive Control Register 0 (UiC0) (i = 0, 1, 3)

Address 00A4h (U0C0), 0164h (U1C0), 016Ch (U3C0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	UFORM	CKPOL	NCH	—	TXEPT	—	CLK1	CLK0
After Reset	0	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CLK0	BRG count source select bit (1)	b1 b0 0 0: f1 selected 0 1: f8 selected 1 0: f32 selected 1 1: Do not set.	R/W
b1	CLK1			R/W
b2	—	Reserved bit	Set to 0.	R/W
b3	TXEPT	Transmit register empty flag	0: Data present in the transmit register (transmission in progress) 1: No data in the transmit register (transmission completed)	R
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	NCH	Data output select bit	0: TXDi pin set to CMOS output 1: TXDi pin set to N-channel open-drain output	R/W
b6	CKPOL	CLK polarity select bit	0: Transmit data output at the falling edge and receive data input at the rising edge of the transfer clock 1: Transmit data output at the rising edge and receive data input at the falling edge of the transfer clock	R/W
b7	UFORM	Transfer format select bit	0: LSB first 1: MSB first	R/W

Note:
1. If the BRG count source is switched, set the UiBRG register again.

20.2.5 UARTi Transmit/Receive Control Register 1 (UiC1) (i = 0, 1, 3)

Address 00A5h (U0C1), 0165h (U1C1), 016Dh (U3C1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	UiRRM	UiIRS	RI	RE	TI	TE
After Reset	0	0	0	0	0	0	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	TE	Transmit enable bit	0: Transmission disabled 1: Transmission enabled	R/W
b1	TI	Transmit buffer empty flag	0: Data present in the UiTB register 1: No data in the UiTB register	R
b2	RE	Receive enable bit	0: Reception disabled 1: Reception enabled	R/W
b3	RI	Receive complete flag (1)	0: No data in the UiRB register 1: Data present in the UiRB register	R
b4	UiIRS	UARTi transmit interrupt source select bit	0: Transmission buffer empty (TI = 1) 1: Transmission completed (TXEPT = 1)	R/W
b5	UiRRM	UARTi continuous receive mode enable bit (2)	0: Continuous receive mode disabled 1: Continuous receive mode enabled	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	—			

Notes:
1. The RI bit is set to 0 when the higher byte of the UiRB register is read.
2. In UART mode, set the UiRRM bit to 0 (continuous receive mode disabled).

20.2.6 UARTi Receive Buffer Register (UiRB) (i = 0, 1, 3)

Address 00A7h to 00A6h (U0RB), 0167h to 0166h (U1RB), 016Fh to 016Eh (U3RB)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	SUM	PER	FER	OER	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Bit Name	Function	R/W
b0	—	—	Receive data (D7 to D0)	R
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			
b8	—	—	Receive data (D8)	R
b9	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b10	—			
b11	—			
b12	OER	Overrun error flag (1)	0: No overrun error 1: Overrun error	R
b13	FER	Framing error flag (1, 2)	0: No framing error 1: Framing error	R
b14	PER	Parity error flag (1, 2)	0: No parity error 1: Parity error	R
b15	SUM	Error sum flag (1, 2)	0: No error 1: Error	R

Notes:
1. Bits SUM, PER, FER, and OER are set to 0 (no error) when either of the following is set:
   - Bits SMD2 to SMD0 in the UiMR register are set to 000b (serial interface disabled), or
   - The RE bit in the UiC1 register is set to 0 (reception disabled)

   The SUM bit is set to 0 (no error) when all of bits PER, FER, and OER are set to 0 (no error).
   Bits PER and FER are also set to 0 when the high-order byte of the UiRB register is read.
   When setting bits SMD2 to SMD0 in the UiMR register to 000b, set the TE bit in the UiC1 register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
2. These error flags are invalid when bits SMD2 to SMD0 in the UiMR register are set to 001b (clock synchronous serial I/O mode). When read, the content is undefined.

Always read the UiRB register in 16-bit units.

20.2.7 UART0 Pin Select Register (U0SR)

Address 0188h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	CLK0SEL0	—	RXD0SEL0	—	TXD0SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TXD0SEL0	TXD0 pin select bit	0: TXD0 pin not used 1: P1_4 assigned	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	RXD0SEL0	RXD0 pin select bit	0: RXD0 pin not used 1: P1_5 assigned	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	CLK0SEL0	CLK0 pin select bit	0: CLK0 pin not used 1: P1_6 assigned	R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b6	—			
b7	—			

The U0SR register selects which pin is assigned to the UART0 I/O. To use the I/O pin for UART0, set this register.
Set the U0SR register before setting the UART0 associated registers. Also, do not change the setting value in this register during UART0 operation.

20.2.8 UART1 Pin Select Register (U1SR)

Address 0189h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	CLK1SEL1	CLK1SEL0	—	RXD1SEL0	—	TXD1SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TXD1SEL0	TXD1 pin select bit	0: TXD1 pin not used 1: P0_1 assigned	R/W
b1	—	Reserved bit	Set to 0.	R/W
b2	RXD1SEL0	RXD1 pin select bit	0: RXD1 pin not used 1: P0_2 assigned	R/W
b3	—	Reserved bit	Set to 0.	R/W
b4	CLK1SEL0	CLK1 pin select bit	b5 b4 0 0: CLK1 pin not used 0 1: P0_3 assigned 1 0: Do not set. 1 1: P6_5 assigned	R/W
b5	CLK1SEL1			
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	—			

The U1SR register selects which pin is assigned to the UART1 I/O. To use the I/O pin for UART1, set this register.
Set the U1SR register before setting the UART1 associated registers. Also, do not change the setting value in this register during UART1 operation.

20.2.9 UART3 Pin Select Register (U3SR)

Address 2F12h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	CLK3SEL0	—	RXD3SEL0	—	TXD3SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TXD3SEL0	TXD3 pin select bit	0: TXD3 pin not used 1: P8_2 assigned	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	RXD3SEL0	RXD3 pin select bit	0: RXD3 pin not used 1: P8_3 assigned	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	CLK3SEL0	CLK3 pin select bit	0: CLK3 pin not used 1: P8_1 assigned	R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b6	—			
b7	—			

The U3SR register selects which pin is assigned to the UART3 I/O. To use the I/O pin for UART3, set this register.
Set the U3SR register before setting the UART3 associated registers. Also, do not change the setting value in this register during UART3 operation.

20.3 Clock Synchronous Serial I/O Mode

In clock synchronous serial I/O mode, data is transmitted and received using a transfer clock.
Table 20.2 lists the Clock Synchronous Serial I/O Mode Specifications. Table 20.3 lists the Registers Used and Settings in Clock Synchronous Serial I/O Mode.

Table 20.2 Clock Synchronous Serial I/O Mode Specifications

Item	Specification
Transfer data format	Transfer data length: 8 bits
Transfer clocks	• The CKDIR bit in the UiMR register is set to 0 (internal clock): fi/(2(n+1)) fi = f1, f8, f32 n = setting value in the UiBRG register: 00h to FFh • The CKDIR bit is set to 1 (external clock): Input from the CLKi pin
Transmit start conditions	To start transmission, the following requirements must be met: (1) • The TE bit in the UiC1 register is set to 1 (transmission enabled). • The TI bit in the UiC1 register is set to 0 (data present in the UiTB register).
Receive start conditions	To start reception, the following requirements must be met: (1) • The RE bit in the UiC1 register is set to 1 (reception enabled). • The TE bit in the UiC1 register is set to 1 (transmission enabled). • The TI bit in the UiC1 register is set to 0 (data present in the UiTB register).
Interrupt request generation timing	For transmission: One of the following can be selected. • The UiIRS bit is set to 0 (transmit buffer empty): When data is transferred from the UiTB register to the UARTi transmit register (at start of transmission). • The UiIRS bit is set to 1 (transmission completed): When data transmission from the UARTi transmit register is completed. • For reception: When data is transferred from the UARTi receive register to the UiRB register (at completion of reception).
Error detection	Overrun error (2) This error occurs if the serial interface starts receiving the next unit of data before reading the UiRB register and receives the 7th bit of the next unit of data.
Selectable functions	• CLK polarity selection Transfer data input/output can be selected to occur synchronously with the rising or the falling edge of the transfer clock. • LSB first, MSB first selection Whether transmitting or receiving data begins with bit 0 or begins with bit 7 can be selected. • Continuous receive mode selection Reception is enabled immediately by reading the UiRB register.

i = 0, 1, 3
Notes:
1. When an external clock is selected, the requirements must be met in either of the following states:
   - The external clock is held high when the CKPOL bit in the UiC0 register is set to 0 (transmit data output at the falling edge and receive data input at the rising edge of the transfer clock)
   - The external clock is held low when the CKPOL bit in the UiC0 register is set to 1 (transmit data output at the rising edge and receive data input at the falling edge of the transfer clock)
2. If an overrun error occurs, the receive data (b0 to b8) in the UiRB register will be undefined. The IR bit in the SiRIC register remains unchanged.

Table 20.3 Registers Used and Settings in Clock Synchronous Serial I/O Mode (1)

Register	Bit	Function
UiTB	b0 to b7	Set data transmission.
UiRB	b0 to b7	Receive data can be read.
	OER	Overrun error flag
UiBRG	b0 to b7	Set a bit rate.
UiMR	SMD2 to SMD0	Set to 001b.
	CKDIR	Select the internal clock or external clock.
UiC0	CLK1, CLK0	Select the count source for the UiBRG register.
	TXEPT	Transmit register empty flag
	NCH	Select TXDi pin output mode.
	CKPOL	Select the transfer clock polarity.
	UFORM	Select LSB first or MSB first.
UiC1	TE	Set to 1 to enable transmission/reception
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Receive complete flag
	UiIRS	Select the UARTi transmit interrupt source.
	UiRRM	Set to 1 to use continuous receive mode.

i = 0, 1, 3

Note:

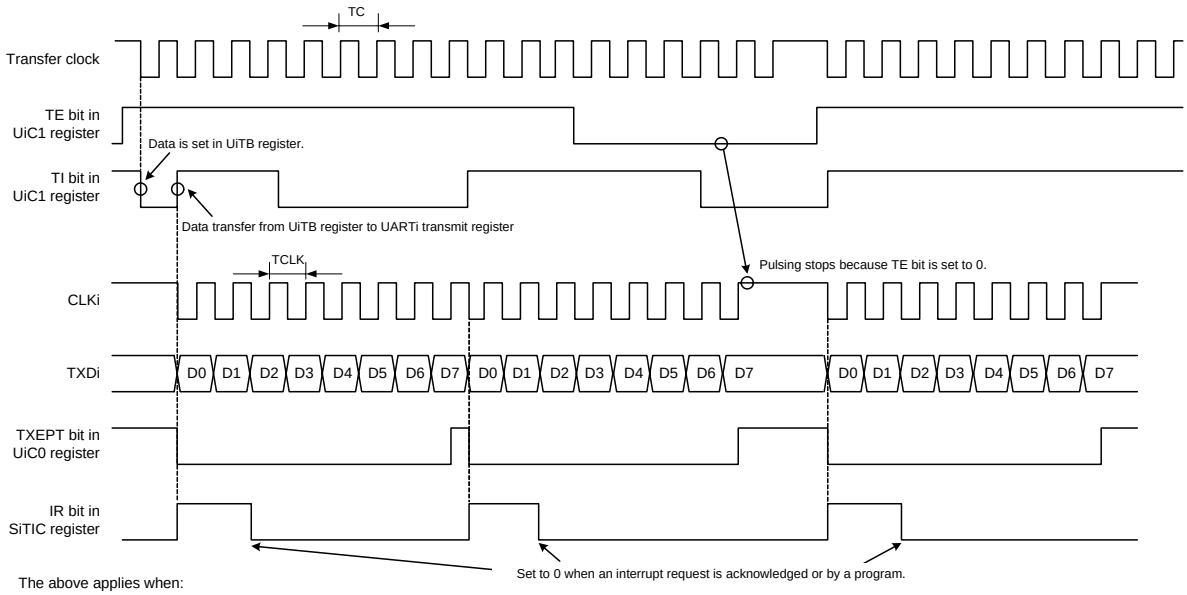
1. Set the bits not listed in this table to 0 when writing to the above registers in clock synchronous serial I/O mode.

Table 20.4 lists the I/O Pin Functions in Clock Synchronous Serial I/O Mode.
After UARTi (i = 0, 1, 3) operating mode is selected, the TXDi pin outputs a “H” level until transfer starts. (If the NCH bit is set to 1 (N-channel open-drain output), this pin is in the high-impedance state.)

Table 20.4 I/O Pin Functions in Clock Synchronous Serial I/O Mode

Pin Name	Function	Selection Method
TXD0 (P1_4)	Serial data output	TXD0SEL0 bit in U0SR register = 1 (For reception only: P1_4 can be used as a port by setting TXD0SEL0 bit = 0.)
RXD0 (P1_5)	Serial data input	RXD0SEL0 bit in U0SR register = 1 PD1_5 bit in PD1 register = 0 (For transmission only: P1_5 can be used as a port by setting RXD0SEL0 bit = 0.)
CLK0 (P1_6)	Transfer clock output	CLK0SEL0 bit in U0SR register = 1 CKDIR bit in U0MR register = 0
	Transfer clock input	CLK0SEL0 bit in U0SR register = 1 CKDIR bit in U0MR register = 1 PD1_6 bit in PD1 register = 0
TXD1 (P0_1)	Serial data output	TXD1SEL0 bit in U1SR register = 1 (For reception only: P0_1 can be used as a port by setting bit TXD1SEL0 = 0)
RXD1 (P0_2)	Serial data input	RXD1SEL1 bit in U1SR register = 1 PD0_2 bit in PD0 register = 0 (For transmission only: P0_2 can be used as a port by setting bit RXD1SEL0 = 0)
CLK1 (P0_3, or P6_5)	Transfer clock output	• CLK1 (P0_3) Bits CLK1SEL1 to CLK1SEL0 in U1SR register = 01b (P0_3) CKDIR bit in U1MR register = 0 • CLK1 (P6_5) Bits CLK1SEL1 to CLK1SEL0 in U1SR register = 11b (P6_5) CKDIR bit in U1MR register = 0
	Transfer clock input	• CLK1 (P0_3) Bits CLK1SEL1 to CLK1SEL0 in U1SR register = 01b (P0_3) CKDIR bit in U1MR register = 1 PD0_3 bit in PD0 register = 0 • CLK1 (P6_5) Bits CLK1SEL1 to CLK1SEL0 in U1SR register = 11b (P6_5) CKDIR bit in U1MR register = 1 PD6_5 bit in PD6 register = 0
CLK3 (P8_1)	Transfer clock output	CLK3SEL0 bit in U3SR register = 1 CKDIR bit in U3MR register = 0
	Transfer clock input	CLK3SEL0 bit in U3SR register = 1 CKDIR bit in U3MR register = 1 PD8_1 bit in PD8 register = 0
TXD3 (P8_2)	Serial data output	TXD3SEL0 bit in U3SR register = 1 (For reception only: P8_2 can be used as a port by setting bit TXD3SEL0 = 0)
RXD3 (P8_3)	Serial data input	RXD3SEL0 bit in U3SR register = 1 PD8_3 bit in PD8 register = 0 (For transmission only: P8_3 can be used as a port by setting bit RXD3SEL0 = 0)

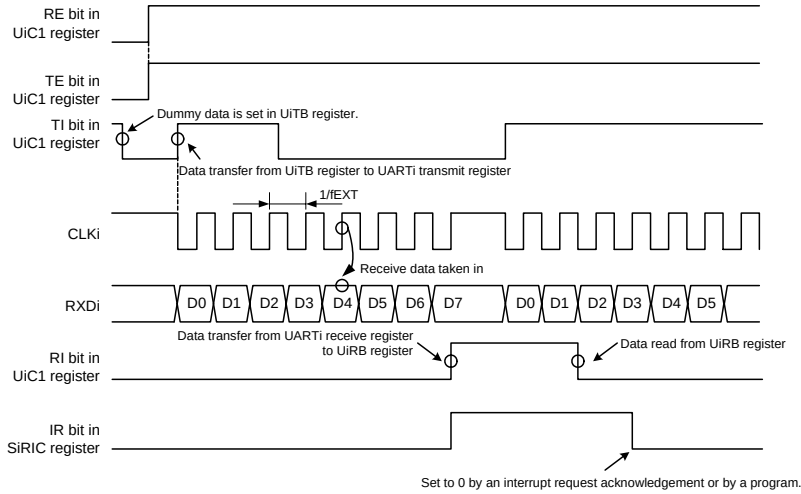
• Transmit Timing Example (Internal Clock Selected)



The above applies when:
- CKDIR bit in UiMR register = 0 (internal clock)
- CKPOL bit in UiC0 register = 0 (transmit data output at the falling edge and receive data input at the rising edge of the transfer clock)
- UiIRS bit in UiC1 register = 0 (interrupt request generation when the transmit buffer is empty)

TC = TCLK = 2(n+1)/fi
fi: Frequency of UiBRG count source (f1, f8, f32)
n: Setting value in UiBRG register

• Receive Timing Example (External Clock Selected)



The above applies when:
- CKDIR bit in UiMR register = 1 (external clock)
- CKPOL bit in UiC0 register = 0 (transmit data output at the falling edge and receive data input at the rising edge of the transfer clock)

The following should be met when “H” is applied to the CLKi pin before receiving data:
- TE bit in UiC1 register = 1 (transmission enabled)
- RE bit in UiC1 register = 1 (reception enabled)
- Dummy data is written to UiTB register

fEXT: Frequency of external clock

i = 0, 1, 3

Figure 20.3 Transmit and Receive Timing in Clock Synchronous Serial I/O Mode

20.3.1 Measure for Dealing with Communication Errors

If communication is aborted or a communication error occurs while transmitting or receiving in clock synchronous serial I/O mode, follow the procedures below:

(1) Set the TE bit in the UiC1 (i = 0, 1, 3) register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
(2) Set bits SMD2 to SMD0 in the UiMR register to 000b (serial interface disabled).
(3) Set bits SMD2 to SMD0 in the UiMR register to 001b (clock synchronous serial I/O mode).
(4) Set the TE bit in the UiC1 register to 1 (transmission enabled) and the RE bit to 1 (reception enabled).

20.3.2 Polarity Select Function

Figure 20.4 shows the Transfer Clock Polarity. Use the CKPOL bit in the UiC0 (i = 0, 1, 3) register to select the transfer clock polarity.

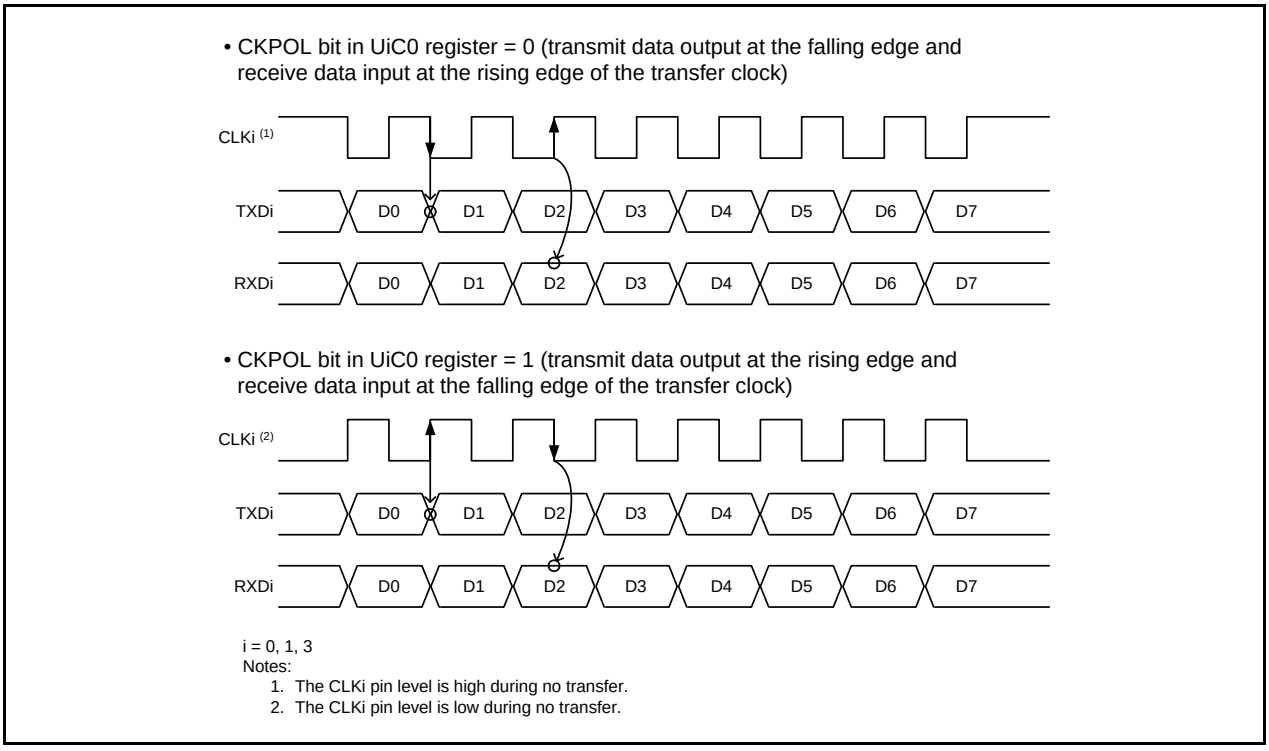


Figure 20.4 Transfer Clock Polarity

20.3.3 LSB First/MSB First Select Function

Figure 20.5 shows the Transfer Format. Use the UFORM bit in the UiC0 (i = 0, 1, 3) register to select the transfer format.

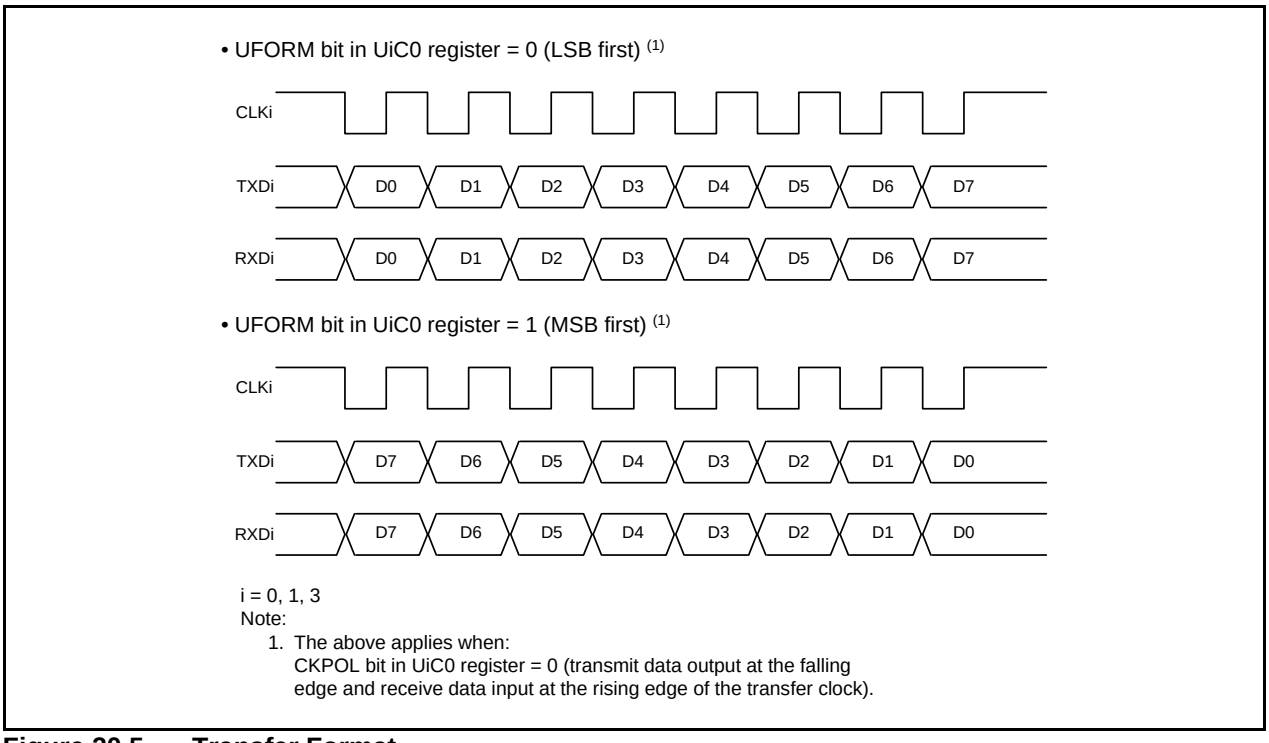


Figure 20.5 Transfer Format

20.3.4 Continuous Receive Mode

Continuous receive mode is selected by setting the UiRRM bit in the UiC1 register (i = 0, 1, 3) to 1 (continuous receive mode enabled). In this mode, reading the UiRB register sets the TI bit in the UiC1 register to 0 (data present in the UiTB register). If the UiRRM bit is set to 1, do not write dummy data to the UiTB register by a program.

20.4 Clock Asynchronous Serial I/O (UART) Mode

The UART mode allows data transmission and reception after setting the desired bit rate and transfer data format. Table 20.5 lists the UART Mode Specifications. Table 20.6 lists the Registers Used and Settings in UART Mode.

Table 20.5 UART Mode Specifications

Item	Specification
Transfer data formats	• Character bits (transfer data): Selectable among 7, 8 or 9 bits • Start bit: 1 bit • Parity bit: Selectable among odd, even, or none • Stop bits: Selectable among 1 or 2 bits
Transfer clocks	• The CKDIR bit in the UiMR register is set to 0 (internal clock): fj/(16(n+1)) fj = f1, f8, f32 n = setting value in the UiBRG register: 00h to FFh • The CKDIR bit is set to 1 (external clock): fEXT/(16(n+1)) fEXT: Input from the CLKi pin n = setting value in the UiBRG register: 00h to FFh
Transmit start conditions	• To start transmission, the following requirements must be met: - The TE bit in the UiC1 register is set to 1 (transmission enabled). - The TI bit in the UiC1 register is set to 0 (data present in the UiTB register).
Receive start conditions	• To start reception, the following requirements must be met: - The RE bit in the UiC1 register is set to 1 (reception enabled). - Start bit detection
Interrupt request generation timing	• For transmission: One of the following can be selected. - The UiIRS bit is set to 0 (transmit buffer empty): When data is transferred from the UiTB register to the UARTi transmit register (at start of transmission). - The UiIRS bit is set to 1 (transfer completed): When data transmission from the UARTi transmit register is completed. • For reception: When data is transferred from the UARTi receive register to the UiRB register (at completion of reception).
Error detection	• Overrun error (1) This error occurs if the serial interface starts receiving the next unit of data before reading the UiRB register and receive the bit one before the last stop bit of the next unit of data. • Framing error This error occurs when the set number of stop bits is not detected. (2) • Parity error This error occurs when parity is enabled, and the number of 1's in the parity and character bits do not match the set number of 1's. (2) • Error sum flag This flag is set to 1 if an overrun, framing, or parity error occurs.

i = 0, 1, 3

Notes:

1. If an overrun error occurs, the receive data (b0 to b8) in the UiRB register will be undefined.
2. The framing error flag and the parity error flag are set to 1 when data is transferred from the UARTi receive register to the UiRB register.

Table 20.6 Registers Used and Settings in UART Mode

Register	Bit	Function
UiTB	b0 to b8	Set transmit data. (1)
UiRB	b0 to b8	Receive data can be read. (2)
	OER, FER, PER, SUM	Error flag
UiBRG	b0 to b7	Set a bit rate.
UiMR	SMD2 to SMD0	Set to 100b when transfer data is 7 bits long. Set to 101b when transfer data is 8 bits long. Set to 110b when transfer data is 9 bits long.
	CKDIR	Select the internal clock or external clock.
	STPS	Select the stop bit.
	PRY, PRYE	Select whether parity is included and whether odd or even.
UiC0	CLK0, CLK1	Select the count source for the UiBRG register.
	TXEPT	Transmit register empty flag
	NCH	Select TXDi pin output mode.
	CKPOL	Set to 0.
	UFORM	Select LSB first or MSB first when transfer data is 8 bits long. Set to 0 when transfer data is 7 bits or 9 bits long.
UiC1	TE	Set to 1 to enable transmission.
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Receive complete flag
	UiIRS	Select the UARTi transmit interrupt source.
	UiRRM	Set to 0.

i = 0, 1, 3

Notes:

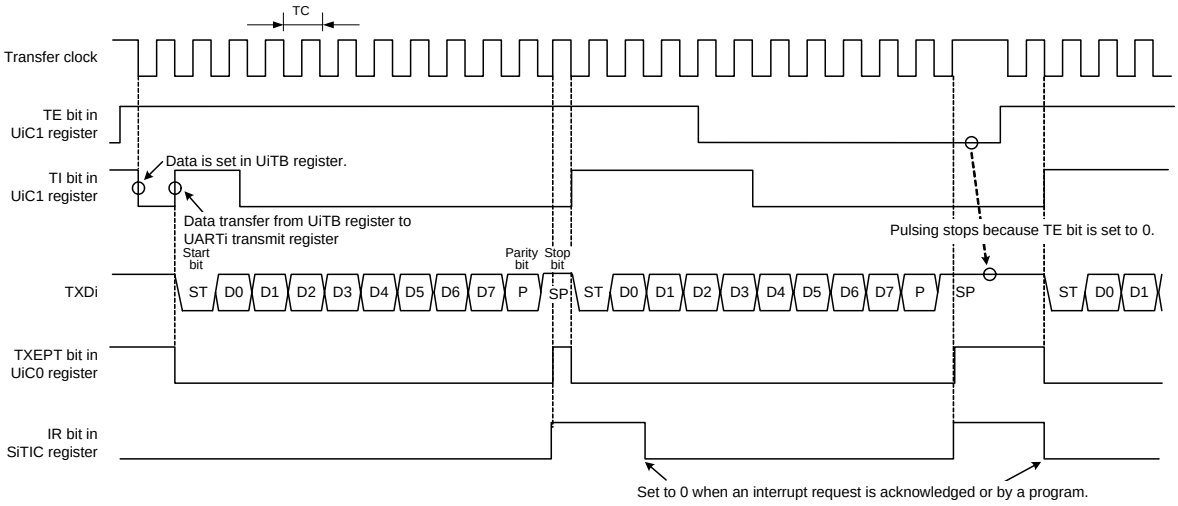
1. The bits used for transmission/receive data are as follows:
   - Bits b0 to b6 when transfer data is 7 bits long
   - Bits b0 to b7 when transfer data is 8 bits long
   - Bits b0 to b8 when transfer data is 9 bits long
2. The contents of the following are undefined:
   - Bits 7 and 8 when the transfer data is 7 bits long
   - Bit 8 when the transfer data is 8 bits long

Table 20.7 lists the I/O Pin Functions in UART Mode.
After the UARTi (i = 0, 1, 3) operating mode is selected, the TXDi pin outputs a “H” level until transfer starts. (If the NCH bit is set to 1 (N-channel open-drain output), this pin is in the high-impedance state.)

Table 20.7 I/O Pin Functions in UART Mode

Pin name	Function	Selection Method
TXD0 (P1_4)	Serial data output	TXD0SEL0 bit in U0SR register = 1 For reception only: P1_4 can be used as a port by setting TXD0SEL0 bit = 0.
RXD0 (P1_5)	Serial data input	RXD0SEL0 bit in U0SR register = 1 PD1_5 bit in PD1 register = 0 For transmission only: P1_5 can be used as a port by setting RXD0SEL0 bit = 0.
CLK0 (P1_6)	Programmable I/O port	CLK0SEL0 bit in U0SR register = 0 (CLK0 pin not used)
	Transfer clock input	CLK0SEL0 bit in U0SR register = 1 CKDIR bit in U0MR register = 1 PD1_6 bit in PD1 register = 0
TXD1 (P0_1)	Serial data output	TXD1SEL0 bit in U1SR register = 1 (For reception only: P0_1 can be used as a port by setting bit TXD1SEL0 = 0)
RXD1 (P0_2)	Serial data input	RXD1SEL0 bit in U1SR register = 1 PD0_2 bit in PD0 register = 0 (For transmission only: P0_2 can be used as a port by setting bit RXD1SEL0 = 0)
CLK1 (P0_3, or P6_5)	Programmable I/O port	Bits CLK1SEL1 to CLK1SEL0 in U1SR register = 00b (CLK1 pin not used)
	Transfer clock input	• CLK1 (P0_3) Bits CLK1SEL1 to CLK1SEL0 in U1SR register = 01b (P0_3) CKDIR bit in U1MR register = 1 PD0_3 bit in PD0 register = 0 • CLK1 (P6_5) Bits CLK1SEL1 to CLK1SEL0 in U1SR register = 11b (P6_5) CKDIR bit in U1MR register = 1 PD6_5 bit in PD6 register = 0
TXD3 (P8_2)	Serial data output	TXD3SEL0 bit in U3SR register = 1 (For reception only: P8_2 can be used as a port by setting bit TXD3SEL0 = 0)
RXD3 (P8_3)	Serial data input	RXD3SEL0 bit in U3SR register = 1 PD8_3 bit in PD8 register = 0 (For transmission only: P8_3 can be used as a port by setting bit RXD3SEL0 = 0)
CLK3 (P8_1)	Programmable I/O port	CLK3SEL0 in U3SR register = 0 (CLK3 pin not used)
	Transfer clock input	CLK3SEL0 bit in U3SR register = 1 CKDIR bit in U3MR register = 1 PD8_1 bit in PD8 register = 0

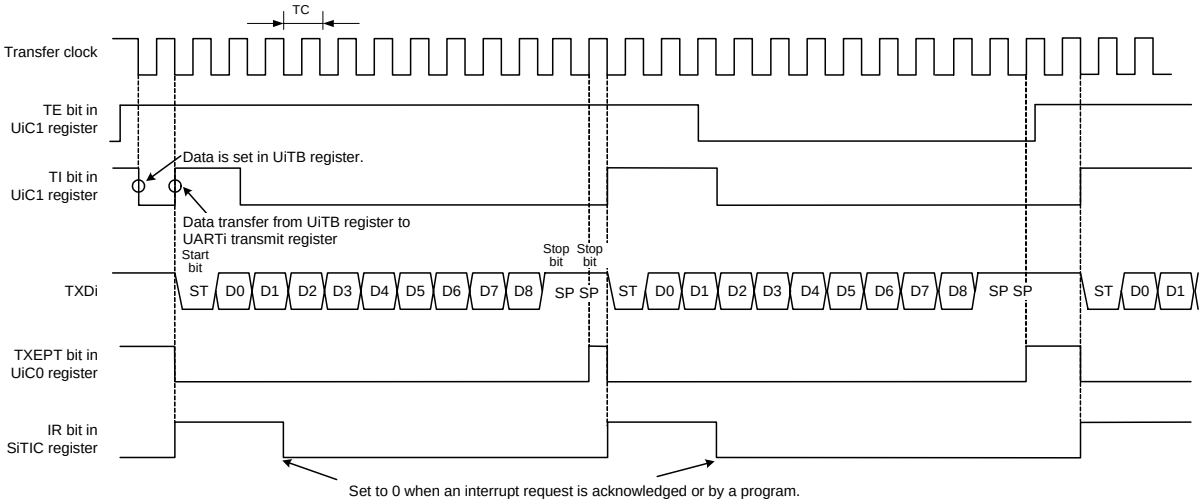
• Transmit Timing Example When Transfer Data 8 Bits is Long (Parity Enabled, One Stop Bit)



The above applies when:
- PRYE bit in UiMR register = 1 (parity enabled)
- STPS bit in UiMR register = 0 (one stop bit)
- UiIRS bit in UiC1 register = 1
  (interrupt request generation when transmission is completed)

TC = 16(n+1)/fj or 16(n+1)/fEXT
fj: Frequency of UiBRG count source (f1, f8, f32)
fEXT: Frequency of UiBRG count source (external clock)
n: Setting value in UiBRG register
i = 0, 1, 3

• Transmit Timing Example When Transfer Data is 9 Bits Long (Parity Disabled, Two Stop Bits)



The above applies when:
- PRYE bit in UiMR register = 0 (parity disabled)
- STPS bit in UiMR register = 1 (two stop bits)
- UiIRS bit in UiC1 register = 0
  (interrupt request generation when the transmit buffer is empty)

TC = 16(n+1)/fj or 16(n+1)/fEXT
fj: Frequency of UiBRG count source (f1, f8, f32)
fEXT: Frequency of UiBRG count source (external clock)
n: Setting value in UiBRG register
i = 0, 1, 3

Figure 20.6 Transmit Timing in UART Mode

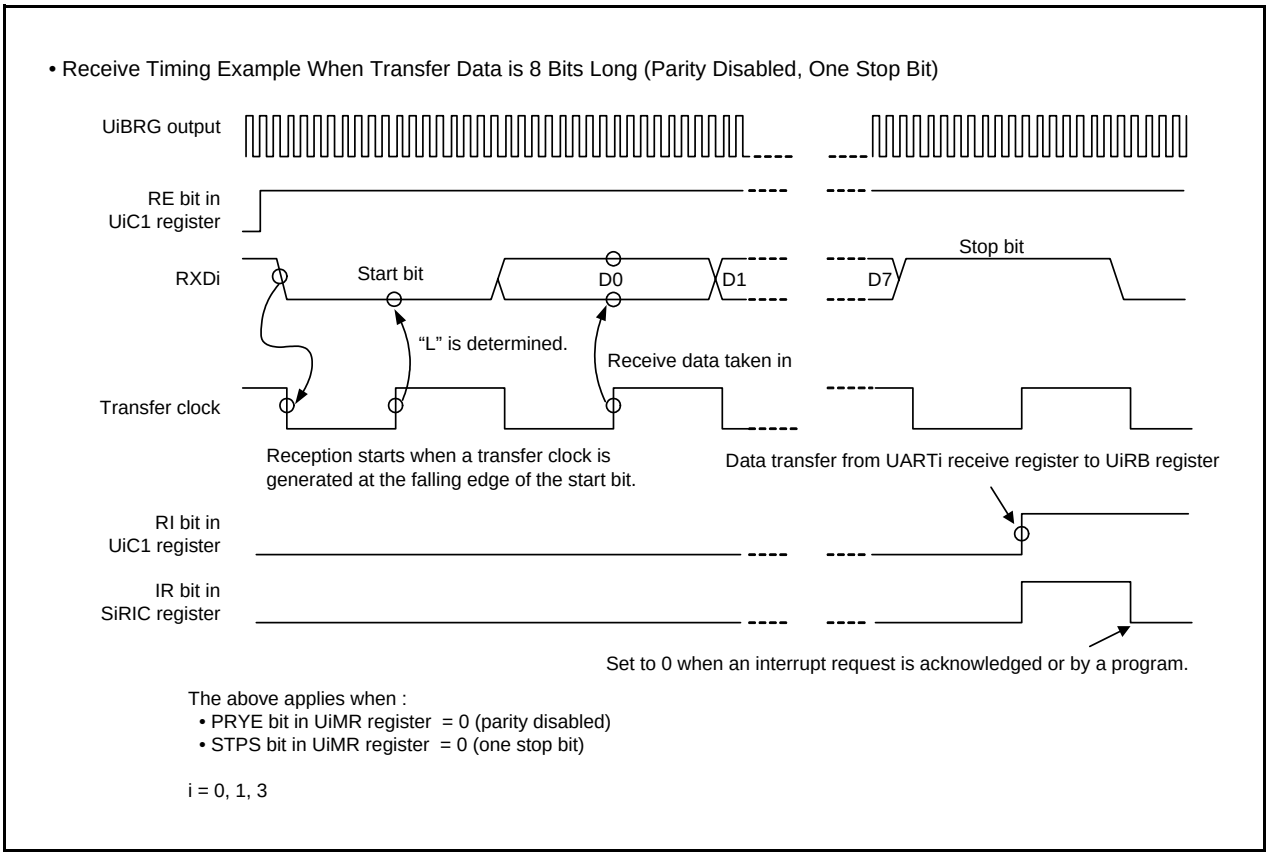


Figure 20.7 Receive Timing in UART Mode

20.4.1 Bit Rate

In UART mode, the bit rate is the frequency divided by the UiBRG (i = 0, 1, 3) register and divided by 16.

UART mode

• Internal clock selected

$$\text{Setting value in UiBRG register} = \frac{fj}{\text{Bit Rate} \times 16} - 1$$

fj: Count source frequency of UiBRG register (f1, f8, or f32)

• External clock selected

$$\text{Setting value in UiBRG register} = \frac{fEXT}{\text{Bit Rate} \times 16} - 1$$

fEXT: Count source frequency of UiBRG register (external clock)

i = 0, 1, 3

Figure 20.8 Formula for Calculating Setting Value in UiBRG (i = 0, 1, 3) Register

Table 20.8 Bit Rate Setting Example in UART Mode (Internal Clock Selected)

Bit Rate (bps)	UiBRG Count Source	System Clock = 20 MHz			System Clock = 18.432 MHz (1)			System Clock = 8 MHz		
		UiBRG Setting Value	Actual Time (bps)	Setting Error (%)	UiBRG Setting Value	Actual Time (bps)	Setting Error (%)	UiBRG Setting Value	Actual Time (bps)	Setting Error (%)
1200	f8	129 (81h)	1201.92	0.16	119 (77h)	1200.00	0.00	51 (33h)	1201.92	0.16
2400	f8	64 (40h)	2403.85	0.16	59 (3Bh)	2400.00	0.00	25 (19h)	2403.85	0.16
4800	f8	32 (20h)	4734.85	–1.36	29 (1Dh)	4800.00	0.00	12 (0Ch)	4807.69	0.16
9600	f1	129 (81h)	9615.38	0.16	119 (77h)	9600.00	0.00	51 (33h)	9615.38	0.16
14400	f1	86 (56h)	14367.82	–0.22	79 (4Fh)	14400.00	0.00	34 (22h)	14285.71	–0.79
19200	f1	64 (40h)	19230.77	0.16	59 (3Bh)	19200.00	0.00	25 (19h)	19230.77	0.16
28800	f1	42 (2Ah)	29069.77	0.94	39 (27h)	28800.00	0.00	16 (10h)	29411.76	2.12
38400	f1	32 (20h)	37878.79	–1.36	29 (1Dh)	38400.00	0.00	12 (0Ch)	38461.54	0.16
57600	f1	21 (15h)	56818.18	–1.36	19 (13h)	57600.00	0.00	8 (08h)	55555.56	–3.55
115200	f1	10 (0Ah)	113636.36	–1.36	9 (09h)	115200.00	0.00	—	—	—

i = 0, 1, 3

Note:

1. For the high-speed on-chip oscillator, the correction value in the FRA4 register should be written into the FRA1 register and the correction value in the FRA5 register should be written into the FRA3 register.
   This applies when the high-speed on-chip oscillator is selected as the system clock and bits FRA22 to FRA20 in the FRA2 register are set to 000b (divide-by-2 mode). For the precision of the high-speed on-chip oscillator, refer to **31. Electrical Characteristics**.

20.4.2 Measure for Dealing with Communication Errors

If communication is aborted or a communication error occurs while transmitting or receiving in UART mode, follow the procedures below:

(1) Set the TE bit in the UiC1 (i = 0, 1, 3) register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
(2) Set bits SMD2 to SMD0 in the UiMR register to 000b (serial interface disabled).
(3) Set bits SMD2 to SMD0 in the UiMR register to 100b (UART mode, transfer data 7 bits long), 101b (UART mode, transfer data 8 bits long), or 110b (UART mode, transfer data 9 bits long).
(4) Set the TE bit in the UiC1 register to 1 (transmission enabled) and the RE bit to 1 (reception enabled).

20.5 Notes on Serial Interface (UARTi (i = 0, 1, 3))

- When reading data from the UiRB (i = 0, 1, 3) register either in clock synchronous serial I/O mode or in clock asynchronous serial I/O mode, always read data in 16-bit units.
  When the high-order byte of the UiRB register is read, bits PER and FER in the UiRB register and the RI bit in the UiC1 register are set to 0.
  To check receive errors, read the UiRB register and then use the read data.

  Program example to read the receive buffer register:

```
MOV.W    00A6H, R0    ; Read the U0RB register
```

- When writing data to the UiTB register in clock asynchronous serial I/O mode with 9-bit transfer data length, write data to the high-order byte first and then the low-order byte, in 8-bit units.

  Program example to write to the transmit buffer register:

```
MOV.B    #XXH, 00A3H  ; Write to the high-order byte of the U0TB register
MOV.B    #XXH, 00A2H  ; Write to the low-order byte of the U0TB register
```

21. Serial Interface (UART2)

The serial interface consists of four channels, UART0 to UART3. This chapter describes the UART2.

21.1 Overview

UART2 has a dedicated timer to generate a transfer clock.
Figure 21.1 shows a UART2 Block Diagram. Figure 21.2 shows a Block Diagram of UART2 Transmit/Receive Unit. Table 21.1 lists the Pin Configuration of UART2.

UART2 has the following modes:
- Clock synchronous serial I/O mode
- Clock asynchronous serial I/O mode (UART mode)
- Multiprocessor communication function

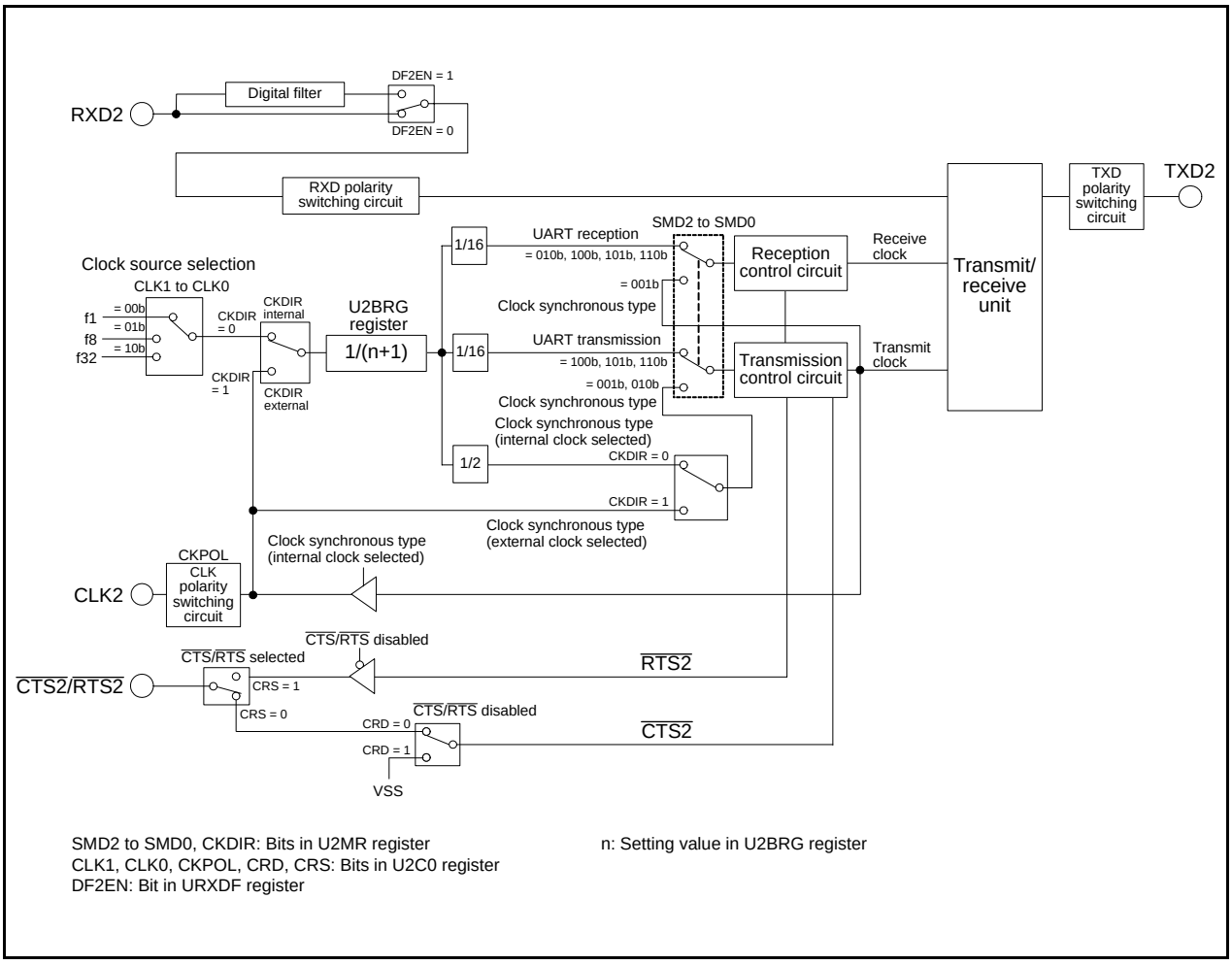


Figure 21.1 UART2 Block Diagram

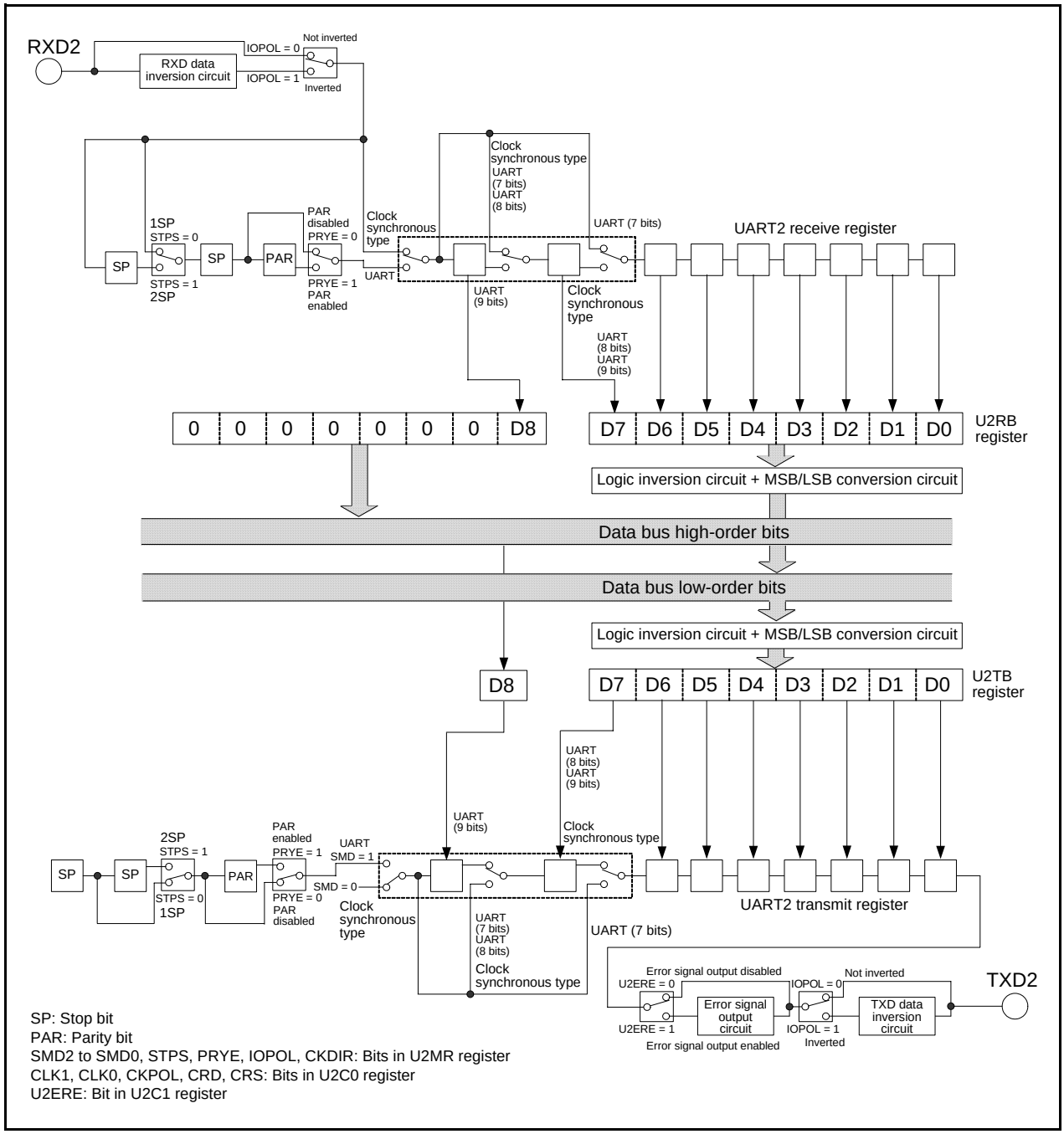


Figure 21.2 Block Diagram of UART2 Transmit/Receive Unit

Table 21.1 Pin Configuration of UART2

Pin Name	Assigned Pin	I/O	Function
TXD2	P6_6	Output	Serial data output
RXD2	P4_5	Input	Serial data input
CLK2	P6_5	I/O	Transfer clock I/O
$\overline{\text{CTS2}}$	P3_3	Input	Transmit control input
$\overline{\text{RTS2}}$	P3_3	Output	Receive control output

21.2 Registers

21.2.1 UART2 Transmit/Receive Mode Register (U2MR)

Address 00A8h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	IOPOL	PRYE	PRY	STPS	CKDIR	SMD2	SMD1	SMD0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	SMD0	Serial I/O mode select bit	b2 b1 b0 0 0 0: Serial interface disabled 0 0 1: Clock synchronous serial I/O mode 1 0 0: UART mode, transfer data 7 bits long 1 0 1: UART mode, transfer data 8 bits long 1 1 0: UART mode, transfer data 9 bits long Other than above: Do not set.	R/W
b1	SMD1			R/W
b2	SMD2			R/W
b3	CKDIR	Internal/external clock select bit	0: Internal clock 1: External clock	R/W
b4	STPS	Stop bit length select bit	0: One stop bit 1: Two stop bits	R/W
b5	PRY	Odd/even parity select bit	Enabled when PRYE = 1 0: Odd parity 1: Even parity	R/W
b6	PRYE	Parity enable bit	0: Parity disabled 1: Parity enabled	R/W
b7	IOPOL	TXD, RXD I/O polarity switch bit	0: Not inverted 1: Inverted	R/W

21.2.2 UART2 Bit Rate Register (U2BRG)

Address 00A9h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	Setting Range	R/W
b7 to b0	If the setting value is n, U2BRG divides the count source by n+1.	00h to FFh	W

Write to the U2BRG register while transmission and reception stop.
Use the MOV instruction to write to this register.
Set bits CLK1 to CLK0 in the U2C0 register before writing to the U2BRG register.

21.2.3 UART2 Transmit Buffer Register (U2TB)

Address 00ABh to 00AAh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	MPTB
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Function	R/W
b0	—	Transmit data (D7 to D0)	W
b1	—		
b2	—		
b3	—		
b4	—		
b5	—		
b6	—		
b7	—		
b8	MPTB	Transmit data (D8) (1) [When the multiprocessor communication function is not used] Transmit data (D8) [When the multiprocessor communication function is used] • To transfer an ID, set the MPTB bit to 1. • To transfer data, set the MPTB bit to 0.	W
b9	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.	—
b10	—		
b11	—		
b12	—		
b13	—		
b14	—		
b15	—		

Note:
1. Set bits b0 to b7 after setting the MPTB bit.

21.2.4 UART2 Transmit/Receive Control Register 0 (U2C0)

Address 00ACh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	UFORM	CKPOL	NCH	CRD	TXEPT	CRS	CLK1	CLK0
After Reset	0	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CLK0	U2BRG count source select bit (1)	b1 b0 0 0: f1 selected 0 1: f8 selected 1 0: f32 selected 1 1: Do not set.	R/W
b1	CLK1			R/W
b2	CRS	$\overline{CTS}$/$\overline{RTS}$ function select bit	Enabled when CRD = 0 0: $\overline{CTS}$ function selected 1: $\overline{RTS}$ function selected	R/W
b3	TXEPT	Transmit register empty flag	0: Data present in the transmit register (transmission in progress) 1: No data in the transmit register (transmission completed)	R
b4	CRD	$\overline{CTS}$/$\overline{RTS}$ disable bit	0: $\overline{CTS}$/$\overline{RTS}$ function enabled 1: $\overline{CTS}$/$\overline{RTS}$ function disabled	R/W
b5	NCH	Data output select bit	0: Pin TXD2 set to CMOS output 1: Pin TXD2 set to N-channel open-drain output	R/W
b6	CKPOL	CLK polarity select bit	0: Transmit data output at the falling edge and receive data input at the rising edge of the transfer clock 1: Transmit data output at the rising edge and receive data input at the falling edge of the transfer clock	R/W
b7	UFORM	Transfer format select bit (2)	0: LSB first 1: MSB first	R/W

Notes:
1. If bits CLK1 to CLK0 are switched, set the U2BRG register again.
2. The UFORM bit is enabled when bits SMD2 to SMD0 in the U2MR register are set to 001b (clock synchronous serial I/O mode), or 101b (UART mode, transfer data 8 bits long).
   Set the UFORM bit to 0 when bits SMD2 to SMD0 are set to 100b (UART mode, transfer data 7 bits long) or 110b (UART mode, transfer data 9 bits long).

21.2.5 UART2 Transmit/Receive Control Register 1 (U2C1)

Address 00ADh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	U2ERE	U2LCH	U2RRM	U2IRS	RI	RE	TI	TE
After Reset	0	0	0	0	0	0	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	TE	Transmit enable bit	0: Transmission disabled 1: Transmission enabled	R/W
b1	TI	Transmit buffer empty flag	0: Data present in the U2TB register 1: No data in the U2TB register	R
b2	RE	Receive enable bit	0: Reception disabled 1: Reception enabled	R/W
b3	RI	Receive complete flag	0: No data in the U2RB register 1: Data present in the U2RB register	R
b4	U2IRS	UART2 transmit interrupt source select bit	0: Transmit buffer empty (TI = 1) 1: Transmission completed (TXEPT = 1)	R/W
b5	U2RRM	UART2 continuous receive mode enable bit	0: Continuous receive mode disabled 1: Continuous receive mode enabled	R/W
b6	U2LCH	Data logic select bit (1)	0: Not inverted 1: Inverted	R/W
b7	U2ERE	Error signal output enable bit	0: Output disabled 1: Output enabled	R/W

Note:
1. The U2LCH bit is enabled when bits SMD2 to SMD0 in the U2MR register are set to 001b (clock synchronous serial I/O mode), 100b (UART mode, transfer data 7 bits long), or 101b (UART mode, transfer data 8 bits long). Set the U2LCH bit to 0 when bits SMD2 to SMD0 are set to 110b (UART mode, transfer data 9 bits long).

21.2.6 UART2 Receive Buffer Register (U2RB)

Address 00AFh to 00AEh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	SUM	PER	FER	OER	—	—	—	MPRB
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Bit Name	Function	R/W
b0	—	—	Receive data (D7 to D0)	R
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			
b8	MPRB	—	Receive data (D8) (1) [When the multiprocessor communication function is not used] Receive data (D8) [When the multiprocessor communication function is used] • When the MPRB bit is set to 0, received D0 to D7 are data fields. • When the MPRB bit is set to 1, received D0 to D7 are ID fields.	R
b9	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b10	—			
b11	—	Reserved bit	Set to 0.	R/W
b12	OER	Overrun error flag (1)	0: No overrun error 1: Overrun error	R
b13	FER	Framing error flag (1, 2)	0: No framing error 1: Framing error	R
b14	PER	Parity error flag (1, 2)	0: No parity error 1: Parity error	R
b15	SUM	Error sum flag (1, 2)	0: No error 1: Error	R

Notes:
1. When bits SMD2 to SMD0 in the U2MR register are set to 000b (serial interface disabled) or the RE bit in the U2C1 register is set to 0 (reception disabled), all of bits SUM, PER, FER, and OER are set to 0 (no error). The SUM bit is set to 0 (no error) when all of bits PER, FER, and OER are set to 0 (no error). Bits PER and FER are set to 0 by reading the lower byte of the U2RB register.
   When setting bits SMD2 to SMD0 in the U2MR register to 000b, set the TE bit in the U2C1 register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
2. These error flags are disabled when bits SMD2 to SMD0 in the U2MR register are set to 001b (clock synchronous serial I/O mode). When read, the content is undefined.

Always read the U2RB register in 16-bit units.

21.2.7 UART2 Digital Filter Function Select Register (URXDF)

Address 00B0h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	DF2EN	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	—			
b2	DF2EN	RXD2 digital filter enable bit (1)	0: RXD2 digital filter disabled 1: RXD2 digital filter enabled	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—			
b5	—			
b6	—			
b7	—			

Note:
1. The RXD2 digital filter can be used only in clock asynchronous serial I/O (UART) mode. When bits SMD2 to SMD0 in the U2MR register are set to 001b (clock synchronous serial I/O mode), set the DF2EN bit to 0 (RXD2 digital filter disabled).

21.2.8 UART2 Special Mode Register 5 (U2SMR5)

Address 00BBh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	MPIE	—	—	—	MP
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	MP	Multiprocessor communication enable bit	0: Multiprocessor communication disabled 1: Multiprocessor communication enabled (1)	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	—			
b3	—			
b4	MPIE	Multiprocessor communication control bit	This bit is enabled when the MP bit is set to 1 (multiprocessor communication enabled). When the MPIE bit is set to 1, the following will result: • Receive data in which the multiprocessor bit is 0 is ignored. Setting of the RI bit in the U2C1 register and bits OER and FER in the U2RB register to 1 is disabled. • On receiving receive data in which the multiprocessor bit is 1, the MPIE bit is set to 0 and receive operation other than multiprocessor communication is performed.	R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b6	—			
b7	—	Reserved bit	Set to 0.	R/W

Note:
1. When the MP bit is set to 1 (multiprocessor communication enabled), the settings of bits PRY and PRYE in the U2MR register are disabled. If bits SMD2 to SMD0 in the U2MR register are set to 001b (clock synchronous serial I/O mode), set the MP bit to 0 (multiprocessor communication disabled).

21.2.9 UART2 Special Mode Register 3 (U2SMR3)

Address 00BDh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	NODC	—	—	—
After Reset	0	0	0	X	0	X	0	X

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b1	—	Reserved bit	Set to 0.	R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b3	NODC	Clock output select bit	0: CLK2 set to CMOS output 1: CLK2 set to N-channel open-drain output	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b5	—	Reserved bits	Set to 0.	R/W
b6	—			
b7	—			

Notes:
1. Bits DL2 to DL0 are used to generate a delay in SDA2 output digitally in I^2C mode. In other than I^2C mode, set these bits to 000b (no delay).
2. The amount of delay varies with the load on pins SCL2 and SDA2. When an external clock is used, the amount of delay increases by about 100 ns.

21.2.10 UART2 Pin Select Register 0 (U2SR0)

Address 018Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	RXD2SEL1	RXD2SEL0	—	TXD2SEL2	TXD2SEL1	TXD2SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TXD2SEL0	TXD2 pin select bit	b2 b1 b0 0 0 0: TXD2 pin not used 1 0 1: P6_6 assigned Other than above: Do not set.	R/W
b1	TXD2SEL1			R/W
b2	TXD2SEL2			R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	RXD2SEL0	RXD2 pin select bit	b5 b4 0 0: RXD2 pin not used 1 1: P4_5 assigned Other than above: Do not set.	R/W
b5	RXD2SEL1			R/W
b6	—	Reserved bit	Set to 0.	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

The U2SR0 register selects which pin is assigned to the UART2 I/O. To use the I/O pin for UART2, set this register.
Set the U2SR0 register before setting the UART2 associated registers. Also, do not change the setting value in this register during UART2 operation.

21.2.11 UART2 Pin Select Register 1 (U2SR1)

Address 018Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	CTS2SEL0	—	—	CLK2SEL1	CLK2SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CLK2SEL0	CLK2 pin select bit	b1 b0 0 0: CLK2 pin not used 1 1: P6_5 assigned Other than above: Do not set.	R/W
b1	CLK2SEL1			R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	—			
b4	CTS2SEL0	$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$ pin select bit	0: $\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$ pin not used 1: P3_3 assigned	R/W
b5	—	Reserved bit	Set to 0.	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	—			

The U2SR1 register selects which pin is assigned to the UART2 I/O. To use the I/O pin for UART2, set this register.
Set the U2SR1 register before setting the UART2 associated registers. Also, do not change the setting value in this register during UART2 operation.

21.3 Clock Synchronous Serial I/O Mode

In clock synchronous serial I/O mode, data is transmitted and received using a transfer clock.
Table 21.2 lists the Clock Synchronous Serial I/O Mode Specifications. Table 21.3 lists the Registers Used and Settings in Clock Synchronous Serial I/O Mode.

Table 21.2 Clock Synchronous Serial I/O Mode Specifications

Item	Specification
Transfer data format	Transfer data length: 8 bits
Transfer clock	• The CKDIR bit in the U2MR register is set to 0 (internal clock): fj/(2(n+1)) fj = f1, f8, f32 n = setting value in the U2BRG register: 00h to FFh • The CKDIR bit is set to 1 (external clock): Input from the CLK2 pin
Transmit/receive control	Selectable from the $\overline{\text{CTS}}$ function, $\overline{\text{RTS}}$ function, or $\overline{\text{CTS}}$/$\overline{\text{RTS}}$ function disabled.
Transmit start conditions	To start transmission, the following requirements must be met: (1) • The TE bit in the U2C1 register is set to 1 (transmission enabled) • The $\overline{\text{TI}}$ bit in the U2C1 register is set to 0 (data present in the U2TB register) • If the $\overline{\text{CTS}}$ function is selected, input to the $\overline{\text{CTS2}}$ pin = “L”.
Receive start conditions	To start reception, the following requirements must be met: (1) • The RE bit in the U2C1 register is set to 1 (reception enabled). • The TE bit in the U2C1 register is set to 1 (transmission enabled). • The TI bit in the U2C1 register is set to 0 (data present in the U2TB register).
Interrupt request generation timing	• For transmission, one of the following conditions can be selected. - The U2IRS bit in the U2C1 register is set to 0 (transmit buffer empty): When data is transferred from the U2TB register to the UART2 transmit register (at start of transmission). - The U2IRS bit is set to 1 (transmission completed): When data transmission from the UART2 transmit register is completed. • For reception When data is transferred from the UART2 receive register to the U2RB register (at completion of reception).
Error detection	Overrun error (2) This error occurs if the serial interface starts receiving the next unit of data before reading the U2RB register and receives the 7th bit of the next unit of data.
Selectable functions	• CLK polarity selection Transfer data I/O can be selected to occur synchronously with the rising or falling edge of the transfer clock. • LSB first, MSB first selection Whether transmitting or receiving data begins with bit 0 or begins with bit 7 can be selected. • Continuous receive mode selection Reception is enabled immediately by reading the U2RB register. • Serial data logic switching This function inverts the logic value of the transmit/receive data.

Notes:
1. When an external clock is selected, the requirements must be met in either of the following states:
   - The external clock is held high when the CKPOL bit in the U2C0 register is set to 0 (transmit data output at the falling edge and receive data input at the rising edge of the transfer clock)
   - The external clock is held low when the CKPOL bit in the U2C0 register is set to 1 (transmit data output at the rising edge and receive data input at the falling edge of the transfer clock)
2. If an overrun error occurs, the receive data in the U2RB register will be undefined. The IR bit in the S2RIC register does not change to 1 (interrupt requested).

Table 21.3 Registers Used and Settings in Clock Synchronous Serial I/O Mode

Register	Bit	Function
U2TB (1)	b0 to b7	Set transmit data.
U2RB (1)	b0 to b7	Receive data can be read.
	OER	Overrun error flag
U2BRG	b0 to b7	Set a bit rate.
U2MR (1)	SMD2 to SMD0	Set to 001b.
	CKDIR	Select the internal clock or external clock.
	IOPOL	Set to 0.
U2C0	CLK1, CLK0	Select the count source for the U2BRG register.
	CRS	Select either $\overline{\text{CTS}}$ or $\overline{\text{RTS}}$ to use functions.
	TXEPT	Transmit register empty flag
	CRD	Enable or disable the $\overline{\text{CTS}}$ or $\overline{\text{RTS}}$ function.
	NCH	Select TXD2 pin output mode.
	CKPOL	Select the transfer clock polarity.
	UFORM	Select LSB first or MSB first.
U2C1	TE	Set to 1 to enable transmission/reception.
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Receive complete flag
	U2IRS	Select the source of UART2 transmit interrupt.
	U2RRM	Set to 1 to use continuous receive mode.
	U2LCH	Set to 1 to use inverted data logic.
	U2ERE	Set to 0.
U2SMR	b0 to b7	Set to 0.
U2SMR2	b0 to b7	Set to 0.
U2SMR3	b0 to b2	Set to 0.
	NODC	Select clock output mode.
	b4 to b7	Set to 0.
U2SMR4	b0 to b7	Set to 0.
URXDF	DF2EN	Set to 0.
U2SMR5	MP	Set to 0.

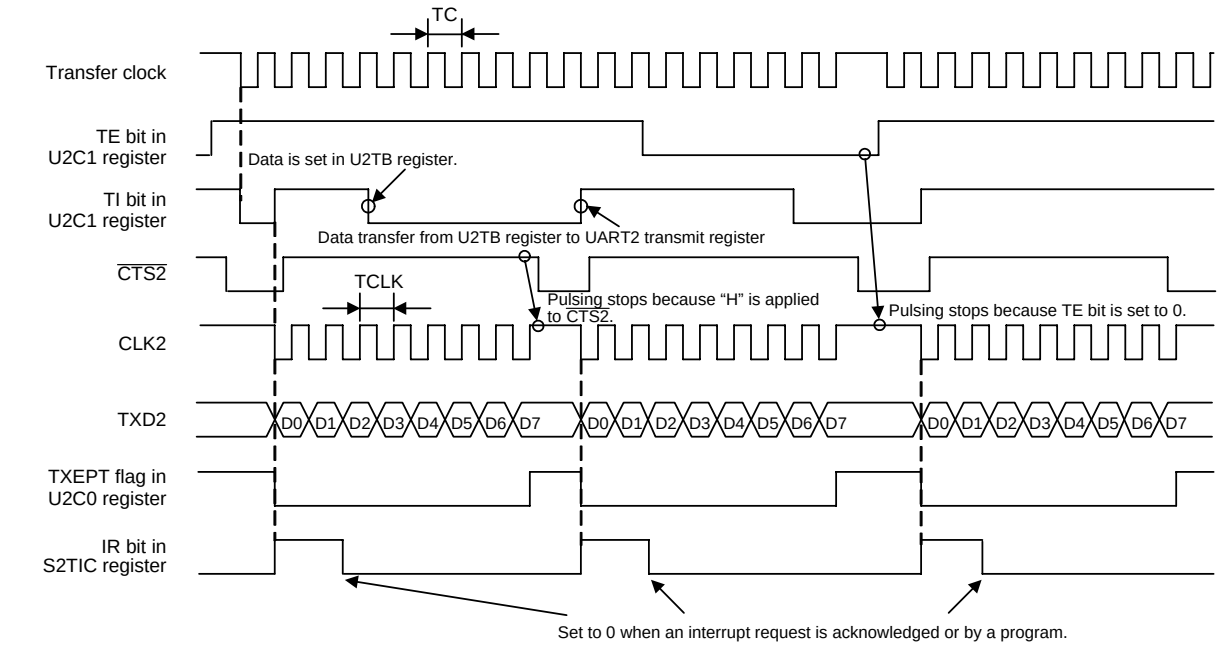
Note:
1. Set the bits not listed in this table to 0 when writing to the above registers in clock synchronous serial I/O mode.

Table 21.4 lists the Pin Functions in Clock Synchronous Serial I/O Mode (Multiple Transfer Clock Output Pin Function Not Selected).
Note that for a period from when UART2 operating mode is selected to when transfer starts, the TXD2 pin outputs a “H” level. (When N-channel open-drain output is selected, this pin is in the high-impedance state.)
Figure 21.3 shows the Transmit and Receive Timing in Clock Synchronous Serial I/O Mode.

Table 21.4 Pin Functions in Clock Synchronous Serial I/O Mode (Multiple Transfer Clock Output Pin Function Not Selected)

Pin Name	Function	Selection Method
TXD2 (P6_6)	Serial data output	Bits TXD2SEL2 to TXD2SEL0 in U2SR0 register = 101b (P6_6) (For reception only: P3_4, P3_7 and P6_6 can be used as ports by setting TXD2SEL2 to TXD2SEL0 to 000b)
RXD2 (P4_5)	Serial data input	Bits RXD2SEL1 to RXD2SEL0 in U2SR0 register = 11b (P4_5) PD4_5 bit in PD4 register = 0 (For transmission only: P4_5 can be used as ports by setting RXD2SEL1 to RXD2SEL0 to 00b.)
CLK2 (P6_5)	Transfer clock output	Bits CLK2SEL1 to CLK2SEL0 in U2SR1 register = 11b (P6_5) CKDIR bit in U2MR register = 0
	Transfer clock input	Bits CLK2SEL1 to CLK2SEL0 in U2SR1 register = 11b (P6_5) CKDIR bit in U2MR register = 1 PD6_5 bit in PD6 register = 0
$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$ (P3_3)	$\overline{\text{CTS}}$ input	CTS2SEL0 bit in U2SR1 register = 1 CRD bit in U2C0 register = 0 CRS bit in U2C0 register = 0 PD3_3 bit in PD3 register = 0
	$\overline{\text{RTS}}$ output	CTS2SEL0 bit in U2SR1 register = 1 CRD bit in U2C0 register = 0 CRS bit in U2C0 register = 1
	I/O port	CTS2SEL0 bit in U2SR1 register = 0

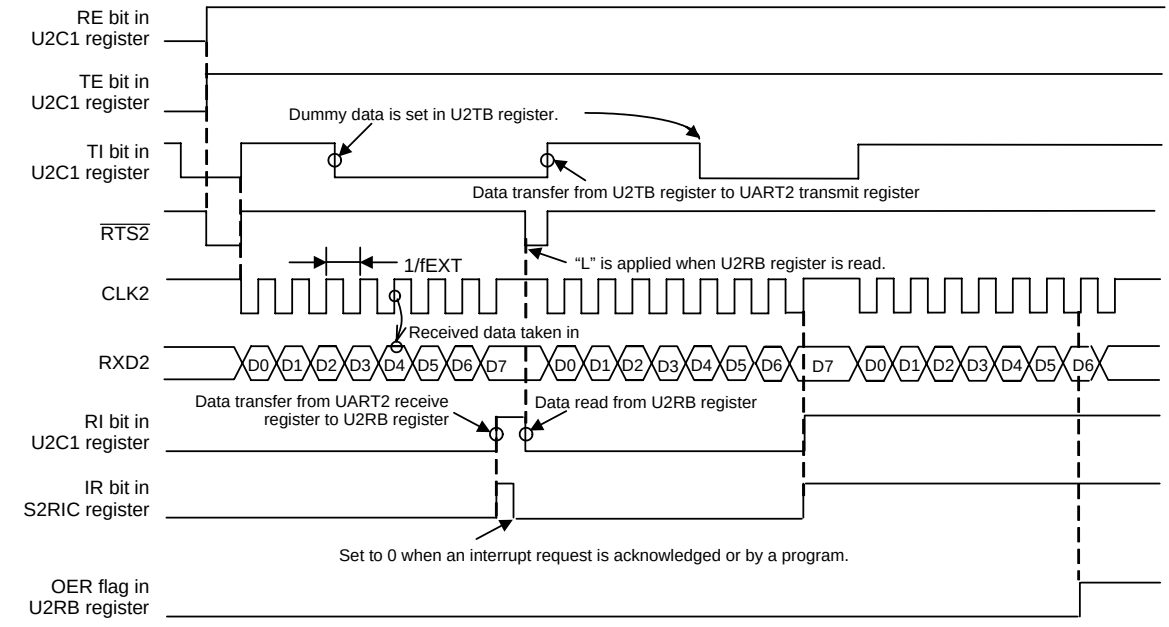
(1) Transmit Timing Example (Internal Clock Selected)



The above applies when:
- CKDIR bit in U2MR register = 0 (internal clock)
- CRD bit in U2C0 register = 0 (CTS/RTS function enabled), CRS bit = 0 (CTS function selected)
- CKPOL bit in U2C0 register = 0 (transmit data output at the falling edge and receive data input at the rising edge of the transfer clock)
- U2IRS bit in U2C1 register = 0 (interrupt request generation when the U2TB register is empty)

TC = TCLK = 2(n+1)/fj
fj: Frequency of U2BRG count source (f1, f8, f32)
n: Setting value in U2BRG register

(2) Receive Timing Example (External Clock Selected)



The above applies when:
- CKDIR bit in U2MR register = 1 (external clock)
- CRD bit in U2C0 register = 0 (CTS/RTS function enabled), CRS bit = 1 (RTS function selected)
- CKPOL bit in U2C0 register = 0 (transmit data output at the falling edge and receive data input at the rising edge of the transfer clock)

Make sure the following conditions are met when the CLK2 pin input before receiving data is high:
- TE bit in U2C0 register = 1 (transmission enabled)
- RE bit in U2C1 register = 1 (reception enabled)
- Dummy data is written to U2TB register

fEXT: Frequency of external clock

Figure 21.3 Transmit and Receive Timing in Clock Synchronous Serial I/O Mode

21.3.1 Measure for Dealing with Communication Errors

If communication is aborted or a communication error occurs while transmitting or receiving in clock synchronous serial I/O mode, follow the procedures below:

(1) Set the TE bit in the U2C1 register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
(2) Set bits SMD2 to SMD0 in the U2MR register to 000b (serial interface disabled).
(3) Set bits SMD2 to SMD0 in the U2MR register to 001b (clock synchronous serial I/O mode).
(4) Set the TE bit in the U2C1 register to 1 (transmission enabled) and the RE bit to 1 (reception enabled).

21.3.2 CLK Polarity Select Function

Use the CKPOL bit in the U2C0 register to select the transfer clock polarity. Figure 21.4 shows the Transfer Clock Polarity.

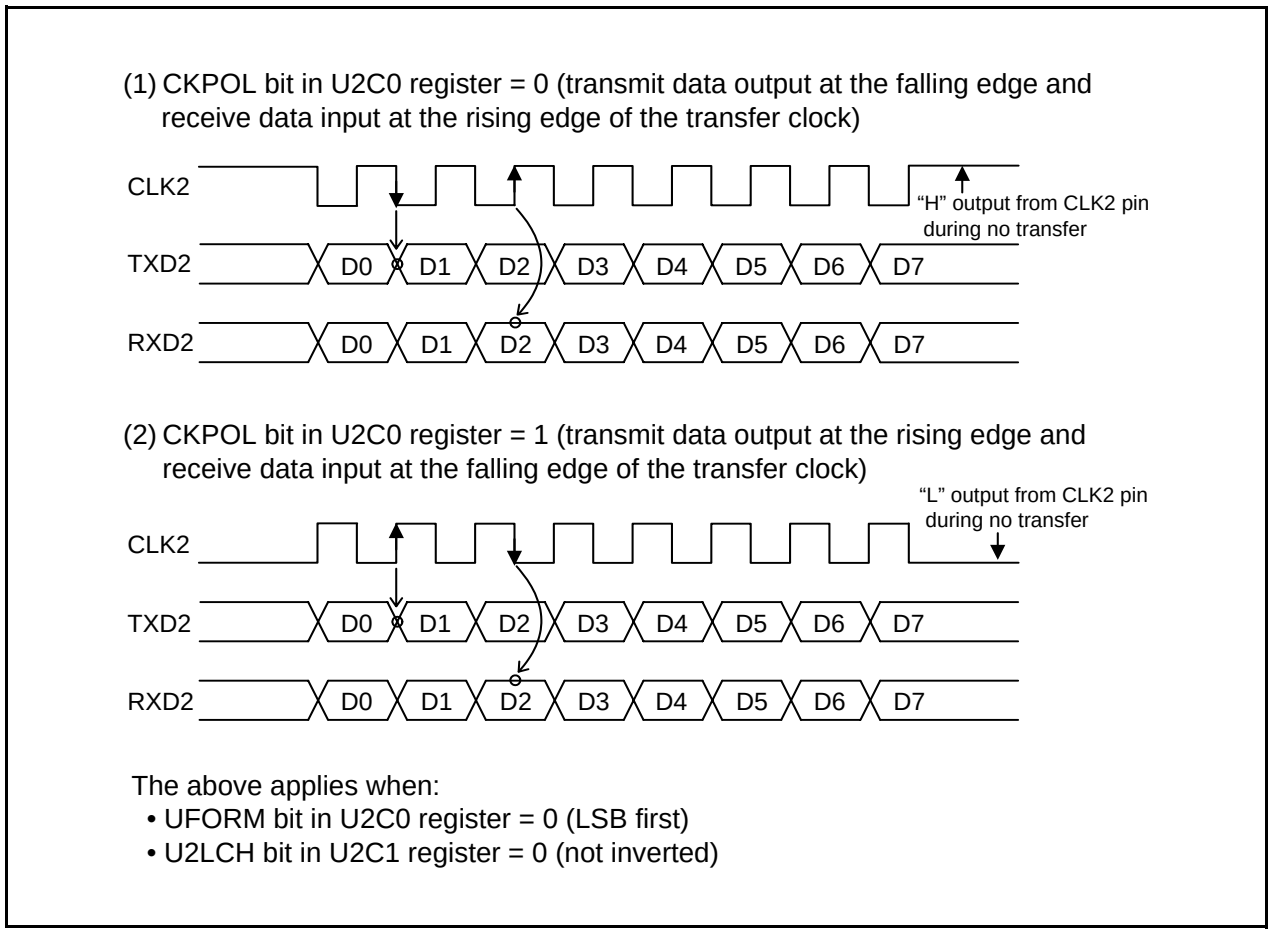


Figure 21.4 Transfer Clock Polarity

21.3.3 LSB First/MSB First Select Function

Use the UFORM bit in the U2C0 register to select the transfer format. Figure 21.5 shows the Transfer Format.

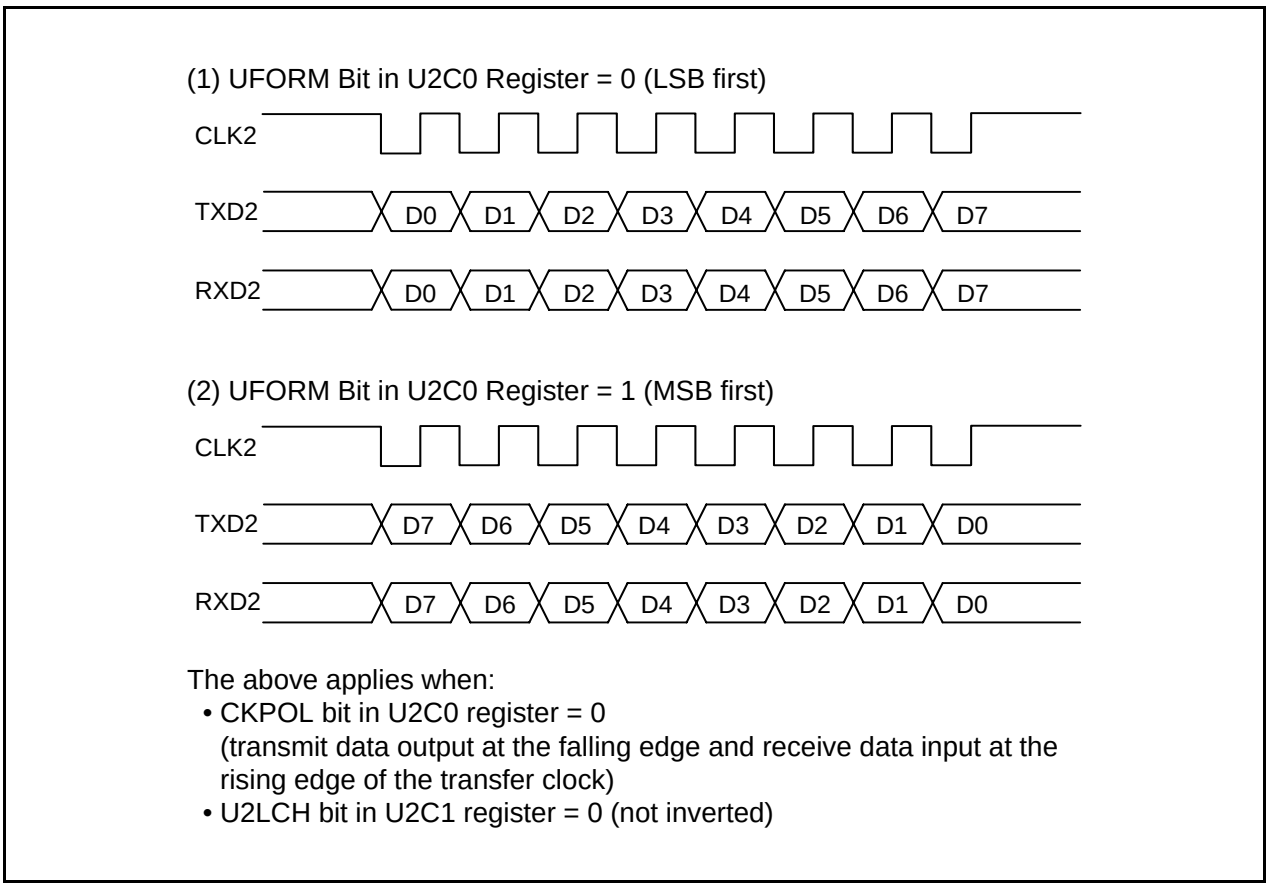


Figure 21.5 Transfer Format

21.3.4 Continuous Receive Mode

In continuous receive mode, receive operation is enabled when the receive buffer register is read. It is not necessary to write dummy data to the transmit buffer register to enable receive operation in this mode. However, a dummy read of the receive buffer register is required when starting the operating mode.

When the U2RRM bit in the U2C1 register is set to 1 (continuous receive mode), the TI bit in the U2C1 register is set to 0 (data present in the U2TB register) by reading the U2RB register. If the U2RRM bit is set to 1, do not write dummy data to the U2TB register by a program.

21.3.5 Serial Data Logic Switching Function

If the U2LCH bit in the U2C1 register is set to 1 (inverted), the data written to the U2TB register has its logic inverted before being transmitted. Similarly, the received data has its logic inverted when read from the U2RB register. Figure 21.6 shows the Serial Data Logic Switching.

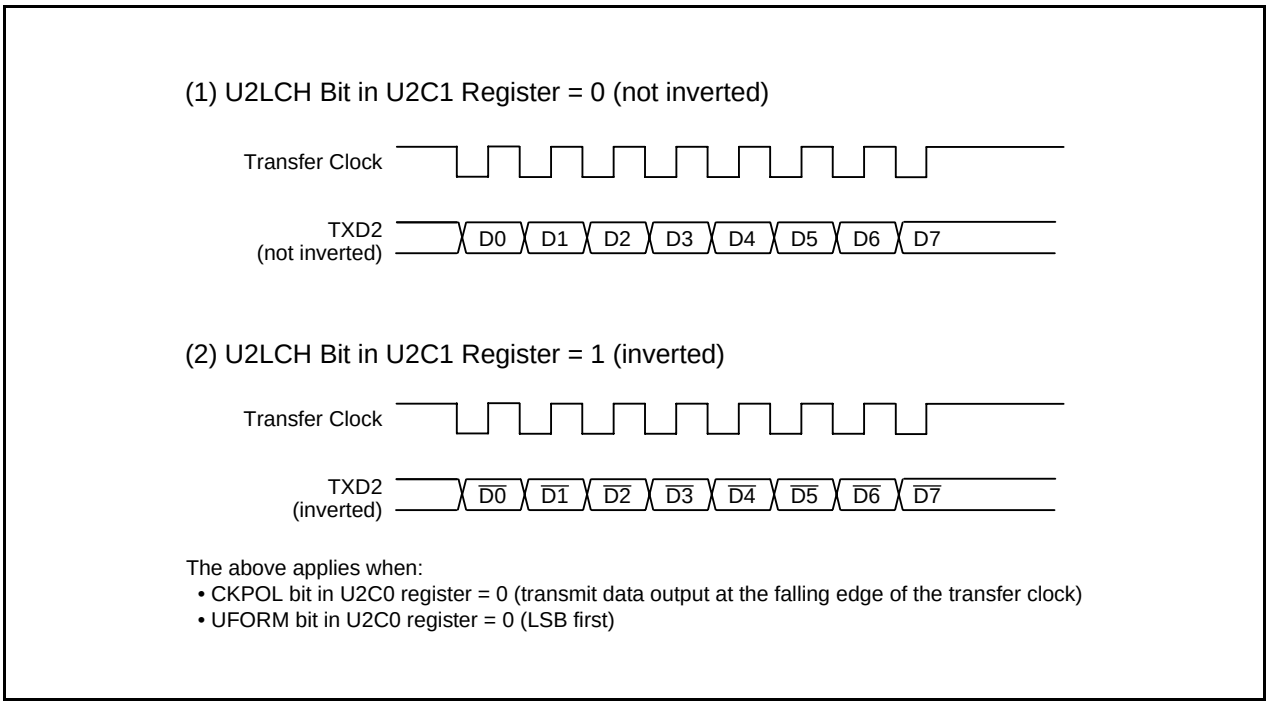


Figure 21.6 Serial Data Logic Switching

21.3.6 $\overline{\text{CTS}}/\overline{\text{RTS}}$ Function

The $\overline{\text{CTS}}$ function is used to start transmit and receive operation when "L" is applied to the $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ pin. Transmit and receive operation begins when the $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ pin is held low. If the "L" signal is switched to "H" during a transmit or receive operation, the operation stops before the next data.

For the $\overline{\text{RTS}}$ function, the $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ pin outputs "L" when the MCU is ready for a receive operation. The output level goes high at the first falling edge of the CLK2 pin.

- The CRD bit in the U2C0 register = 1 ($\overline{\text{CTS}}/\overline{\text{RTS}}$ function disabled)
  The $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ pin operates as the programmable I/O function.
- The CRD bit = 0, CRS bit = 0 ($\overline{\text{CTS}}$ function selected)
  The $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ pin operates as the $\overline{\text{CTS}}$ function.
- The CRD bit = 0, CRS bit = 1 ($\overline{\text{RTS}}$ function selected)
  The $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ pin operates as the $\overline{\text{RTS}}$ function.

21.4 Clock Asynchronous Serial I/O (UART) Mode

In UART mode, data is transmitted and received after setting the desired bit rate and transfer data format. Table 21.5 lists the UART Mode Specifications. Table 21.6 lists the Registers Used and Settings in UART Mode.

Table 21.5 UART Mode Specifications

Item	Specification
Transfer data format	• Character bits (transfer data): Selectable from 7, 8, or 9 bits • Start bit: 1 bit • Parity bit: Selectable from odd, even, or none • Stop bits: Selectable from 1 or 2 bits
Transfer clock	• The CKDIR bit in the U2MR register is set to 0 (internal clock): fj/(16(n+1)) fj = f1, f8, f32 n = setting value in the U2BRG register: 00h to FFh • The CKDIR bit is set to 1 (external clock): fEXT/(16(n + 1)) fEXT: Input from CLK2 pin n: Setting value in the U2BRG register: 00h to FFh
Transmit/receive control	Selectable from the $\overline{\text{CTS}}$ function, $\overline{\text{RTS}}$ function, or $\overline{\text{CTS}}$/$\overline{\text{RTS}}$ function disabled.
Transmit start conditions	To start transmission, the following requirements must be met: • The TE bit in the U2C1 register is set to 1 (transmission enabled). • The TI bit in the U2C1 register is set to 0 (data present in the U2TB register). • If the $\overline{\text{CTS}}$ function is selected, input to the $\overline{\text{CTS2}}$ pin = “L”.
Receive start conditions	To start reception, the following requirements must be met: • The RE bit in the U2C1 register is set to 1 (reception enabled). • Start bit detection
Interrupt request generation timing	• For transmission, one of the following conditions can be selected. - The U2IRS bit in the U2C1 register is set to 0 (transmit buffer empty): When data is transferred from the U2TB register to the UART2 transmit register (at start of transmission). - The U2IRS bit is set to 1 (transmission completed): When data transmission from the UART2 transmit register is completed. • For reception When data is transferred from the UART2 receive register to the U2RB register (at completion of reception).
Error detection	• Overrun error (1) This error occurs if the serial interface starts receiving the next unit of data before reading the U2RB register and receives the bit one before the last stop bit of the next unit of data. • Framing error (2) This error occurs when the set number of stop bits is not detected. • Parity error (2) This error occurs when if parity is enabled, the number of 1’s in the parity and character bits does not match the set number of 1’s. • Error sum flag This flag is set to 1 if an overrun, framing, or parity error occurs.
Selectable functions	• LSB first, MSB first selection Whether transmitting or receiving data begins with bit 0 or begins with bit 7 can be selected. • Serial data logic switching This function inverts the logic of the transmit/receive data. The start and stop bits are not inverted. • TXD, RXD I/O polarity switching This function inverts the polarities of the TXD pin output and RXD pin input. The logic levels of all I/O data are inverted. • RXD2 digital filter selection The RXD2 input signal can be enabled or disabled.

Notes:
1. If an overrun error occurs, the receive data in the U2RB register will be undefined. The IR bit in the S2RIC register remains unchanged.
2. The framing error flag and the parity error flag are set to 1 when data is transferred from the UART2 receive register to the U2RB register.

Table 21.6 Registers Used and Settings in UART Mode

Register	Bit	Function
U2TB	b0 to b8	Set transmit data. (1)
U2RB	b0 to b8	Receive data can be read. (1, 2)
	OER, FER, PER, SUM	Error flag
U2BRG	b0 to b7	Set a bit rate.
U2MR	SMD2 to SMD0	Set to 100b when transfer data is 7 bits long. Set to 101b when transfer data is 8 bits long. Set to 110b when transfer data is 9 bits long.
	CKDIR	Select the internal clock or external clock.
	STPS	Select the stop bit.
	PRY, PRYE	Select whether parity is included and whether odd or even.
	IOPOL	Select the TXD/RXD I/O polarity.
U2C0	CLK0, CLK1	Select the count source for the U2BRG register.
	CRS	Select $\overline{\text{CTS}}$ or $\overline{\text{RTS}}$ to use functions.
	TXEPT	Transmit register empty flag
	CRD	Enable or disable the $\overline{\text{CTS}}$ or $\overline{\text{RTS}}$ function.
	NCH	Select TXD2 pin output mode.
	CKPOL	Set to 0.
	UFORM	Select LSB first or MSB first when transfer data is 8 bits long. Set to 0 when transfer data is 7 or 9 bits long.
U2C1	TE	Set to 1 to enable transmission.
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Receive complete flag
	U2IRS	Select the UART2 transmit interrupt source.
	U2RRM	Set to 0.
	U2LCH	Set to 1 to use inverted data logic.
	U2ERE	Set to 0.
U2SMR	b0 to b7	Set to 0.
U2SMR2	b0 to b7	Set to 0.
U2SMR3	b0 to b7	Set to 0.
U2SMR4	b0 to b7	Set to 0.
URXDF	DF2EN	Select the digital filter disabled or enabled.
U2SMR5	MP	Set to 0.

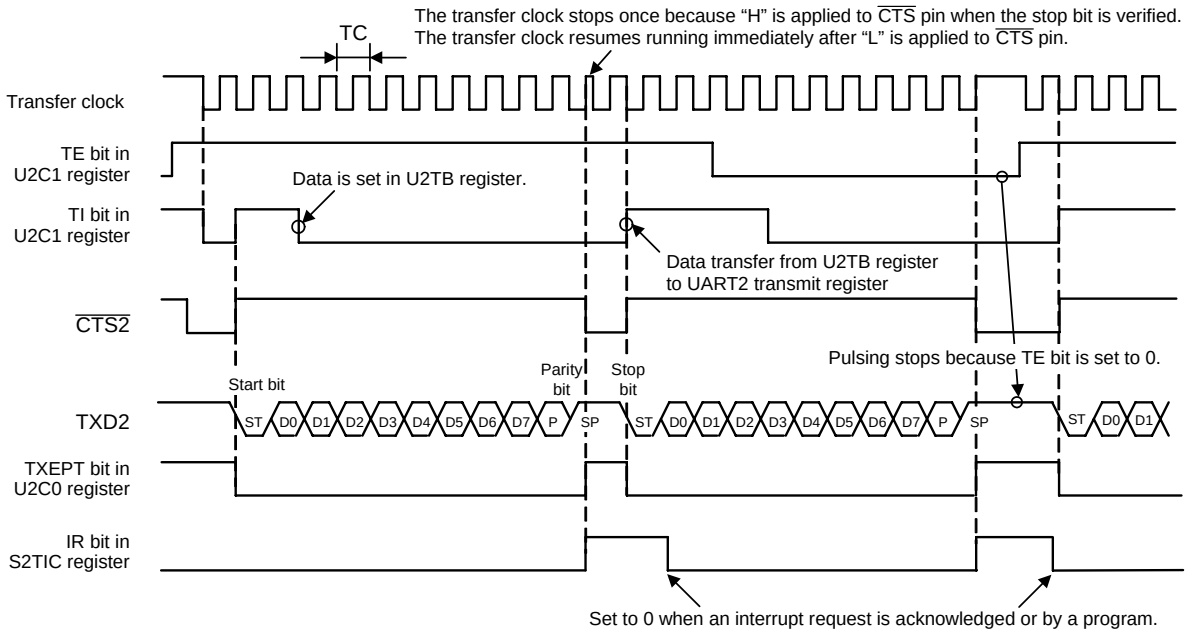
Notes:
1. The bits used for transmit/receive data are as follows:
   - Bits b0 to b6 when transfer data is 7 bits long
   - Bits b0 to b7 when transfer data is 8 bits long
   - Bits b0 to b8 when transfer data is 9 bits long
2. The contents of the following are undefined:
   - Bits b7 and b8 when transfer data is 7 bits long
   - Bit b8 when transfer data is 8 bits long

Table 21.7 lists the I/O Pin Functions in UART Mode.
Note that for a period from when the UART2 operating mode is selected to when transfer starts, the TXD2 pin outputs “H”. (When N-channel open-drain output is selected, this pin is in the high-impedance state.)
Figure 21.7 shows the Transmit Timing in UART Mode. Figure 21.8 shows the Receive Timing in UART Mode.

Table 21.7 I/O Pin Functions in UART Mode

Pin Name	Function	Selection Method
TXD2 (P6_6)	Serial data output	Bits TXD2SEL2 to TXD2SEL0 in U2SR0 register = 101b (P6_6) (For reception only: P6_6 can be used as ports by setting TXD2SEL2 to TXD2SEL0 to 000b.)
RXD2 (P4_5)	Serial data input	Bits RXD2SEL1 to RXD2SEL0 in U2SR0 register = 11b (P4_5) PD4_5 bit in PD4 register = 0 For transmission only: P4_5 can be used as ports by setting RXD2SEL1 to RXD2SEL0 to 00b.
CLK2 (P6_5)	I/O port	Bits CLK2SEL1 to CLK2SEL0 in U2SR1 register = 00b (P6_5)
	Transfer clock input	Bits CLK2SEL1 to CLK2SEL0 in U2SR1 register = 11b (P6_5) CKDIR bit in U2MR register = 1 PD6_5 bit in PD6 register = 0
$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$ (P3_3)	$\overline{\text{CTS}}$ input	CTS2SEL0 bit in U2SR1 register = 1 CRD bit in U2C0 register = 0 CRS bit in U2C0 register = 0 PD3_3 bit in PD3 register = 0
	$\overline{\text{RTS}}$ output	CTS2SEL0 bit in U2SR1 register = 1 CRD bit in U2C0 register = 0 CRS bit in U2C0 register = 1
	I/O port	CTS2SEL0 bit in U2SR1 register = 0

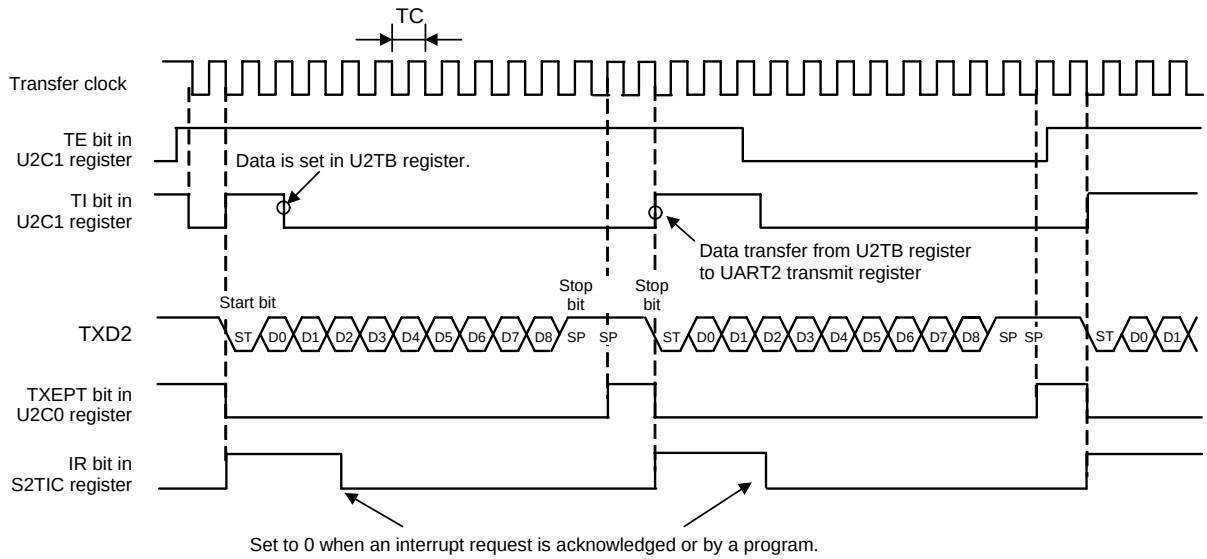
(1) Transmit Timing Example When Transfer Data 8 Bits is Long (Parity Enabled, One Stop Bit)



The above applies when:
- PRYE bit in U2MR register = 1 (parity enabled)
- STPS bit in U2MR register = 0 (one stop bit)
- CRD bit in U2C0 register = 0 (CTS/RTS function enabled), CRS bit = 0 (CTS function selected)
- U2IRS bit in U2C1 register = 1 (interrupt request generation when transmission is completed)

TC = 16(n+1)/fj or 16(n+1)/fEXT
fj: Frequency of U2BRG count source (f1, f8, f32)
fEXT: Frequency of U2BRG count source (external clock)
n: Setting value in U2BRG

(2) Transmit Timing Example When Transfer Data 9 Bits is Long (Parity Disabled, Two Stop Bits)



The above applies when:
- PRYE bit in U2MR register = 0 (parity disabled)
- STPS bit in U2MR register = 1 (two stop bits)
- CRD bit in U2C0 register = 1 (CTS/RTS function disabled)
- U2IRS bit in U2C1 register = 0 (interrupt request generation when the transmit buffer is empty)

TC = 16(n+1)/fj or 16(n+1)/fEXT
fj: Frequency of U2BRG count source (f1, f8, f32)
fEXT: Frequency of U2BRG count source (external clock)
n: Setting value in U2BRG

Figure 21.7 Transmit Timing in UART Mode

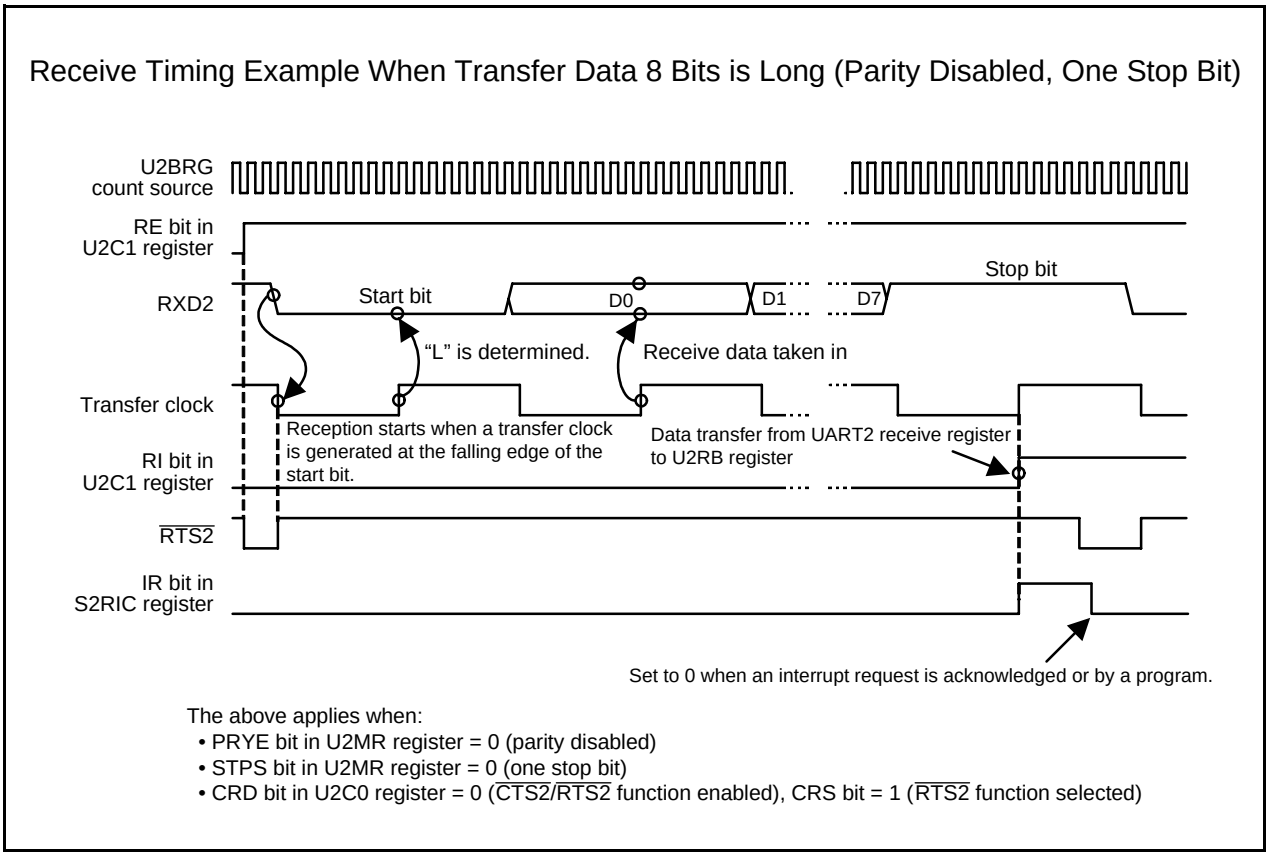


Figure 21.8 Receive Timing in UART Mode

21.4.1 Bit Rate

In UART mode, the bit rate is the frequency divided by the U2BRG register divided by 16. Table 21.8 lists the Bit Rate Setting Example in UART Mode (Internal Clock Selected).

Table 21.8 Bit Rate Setting Example in UART Mode (Internal Clock Selected)

Bit Rate (bps)	U2BRG Count Source	System Clock = 20 MHz			System Clock = 18.432 MHz (1)			System Clock = 8 MHz		
		U2BRG Setting Value	Actual Time (bps)	Setting Error (%)	U2BRG Setting Value	Actual Time (bps)	Setting Error (%)	U2BRG Setting Value	Actual Time (bps)	Setting Error (%)
1200	f8	129 (81h)	1201.92	0.16	119 (77h)	1200.00	0.00	51 (33h)	1201.92	0.16
2400	f8	64 (40h)	2403.85	0.16	59 (3Bh)	2400.00	0.00	25 (19h)	2403.85	0.16
4800	f8	32 (20h)	4734.85	–1.36	29 (1Dh)	4800.00	0.00	12 (0Ch)	4807.69	0.16
9600	f1	129 (81h)	9615.38	0.16	119 (77h)	9600.00	0.00	51 (33h)	9615.38	0.16
14400	f1	86 (56h)	14367.82	–0.22	79 (4Fh)	14400.00	0.00	34 (22h)	14285.71	–0.79
19200	f1	64 (40h)	19230.77	0.16	59 (3Bh)	19200.00	0.00	25 (19h)	19230.77	0.16
28800	f1	42 (2Ah)	29069.77	0.94	39 (27h)	28800.00	0.00	16 (10h)	29411.76	2.12
38400	f1	32 (20h)	37878.79	–1.36	29 (1Dh)	38400.00	0.00	12 (0Ch)	38461.54	0.16
57600	f1	21 (15h)	56818.18	–1.36	19 (13h)	57600.00	0.00	8 (08h)	55555.56	–3.55
115200	f1	10 (0Ah)	113636.36	–1.36	9 (09h)	115200.00	0.00	—	—	—

Note:
1. For the high-speed on-chip oscillator, the correction value in the FRA4 register should be written into the FRA1 register and the correction value in the FRA5 register should be written into the FRA3 register.
This applies when the high-speed on-chip oscillator is selected as the system clock and bits FRA22 to FRA20 in the FRA2 register are set to 000b (divide-by-2 mode). For the precision of the high-speed on-chip oscillator, refer to **31. Electrical Characteristics**.

21.4.2 Measure for Dealing with Communication Errors

If communication is aborted or a communication error occurs while transmitting or receiving in UART mode, follow the procedures below:

(1) Set the TE bit in the U2C1 register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
(2) Set bits SMD2 to SMD0 in the U2MR register to 000b (serial interface disabled).
(3) Set bits SMD2 to SMD0 in the U2MR register to 100b (UART mode, transfer data 7 bits long), 101b (UART mode, transfer data 8 bits long), or 110b (UART mode, transfer data 9 bits long).
(4) Set the TE bit in the U2C1 register to 1 (transmission enabled) and the RE bit to 1 (reception enabled).

21.4.3 LSB First/MSB First Select Function

As shown in Figure 21.9, use the UFORM bit in the U2C0 register to select the transfer format. This function is enabled when transfer data is 8 bits long. Figure 21.9 shows the Transfer Format.

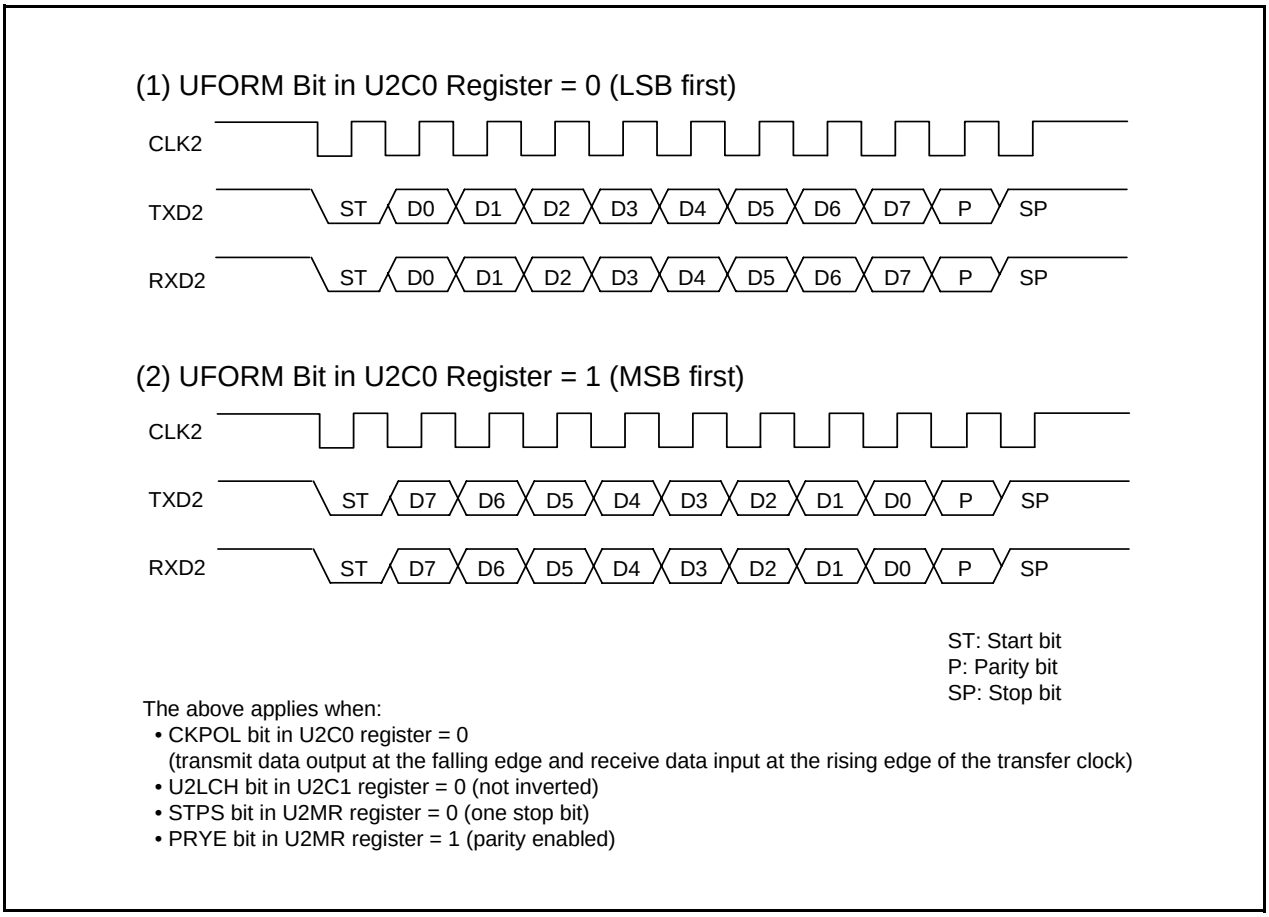


Figure 21.9 Transfer Format

21.4.4 Serial Data Logic Switching Function

The data written to the U2TB register has its logic inverted before being transmitted. Similarly, the received data has its logic inverted when read from the U2RB register. Figure 21.10 shows the Serial Data Logic Switching.

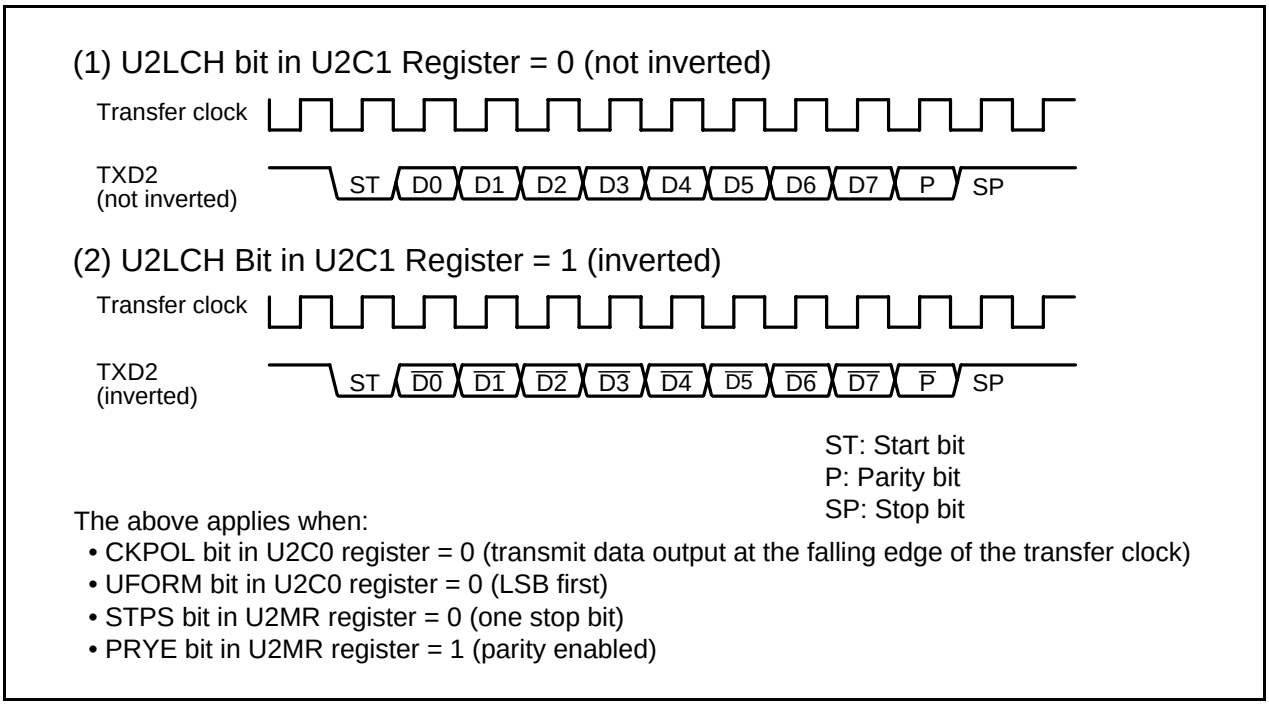


Figure 21.10 Serial Data Logic Switching

21.4.5 TXD and RXD I/O Polarity Inverse Function

This function inverts the polarities of the TXD2 pin output and RXD2 pin input. The logic levels of all I/O data (including bits for start, stop, and parity) are inverted. Figure 21.11 shows the TXD and RXD I/O Inversion.

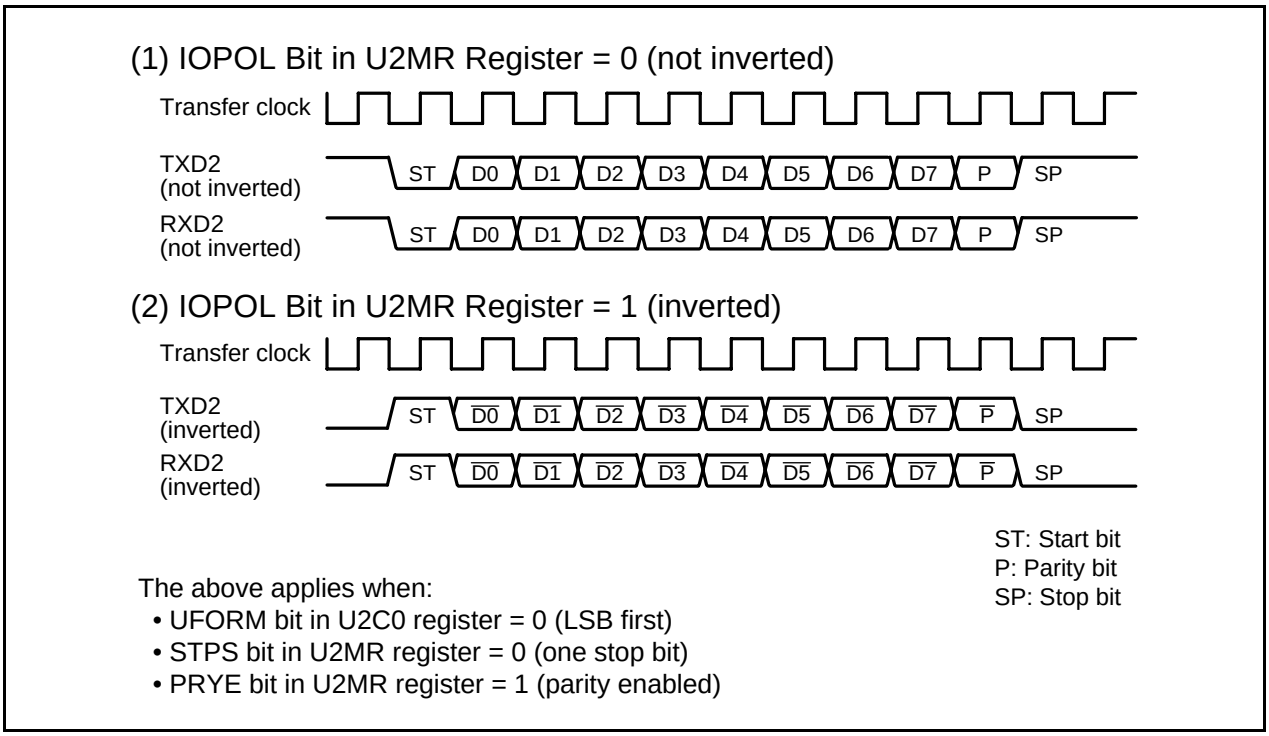


Figure 21.11 TXD and RXD I/O Inversion

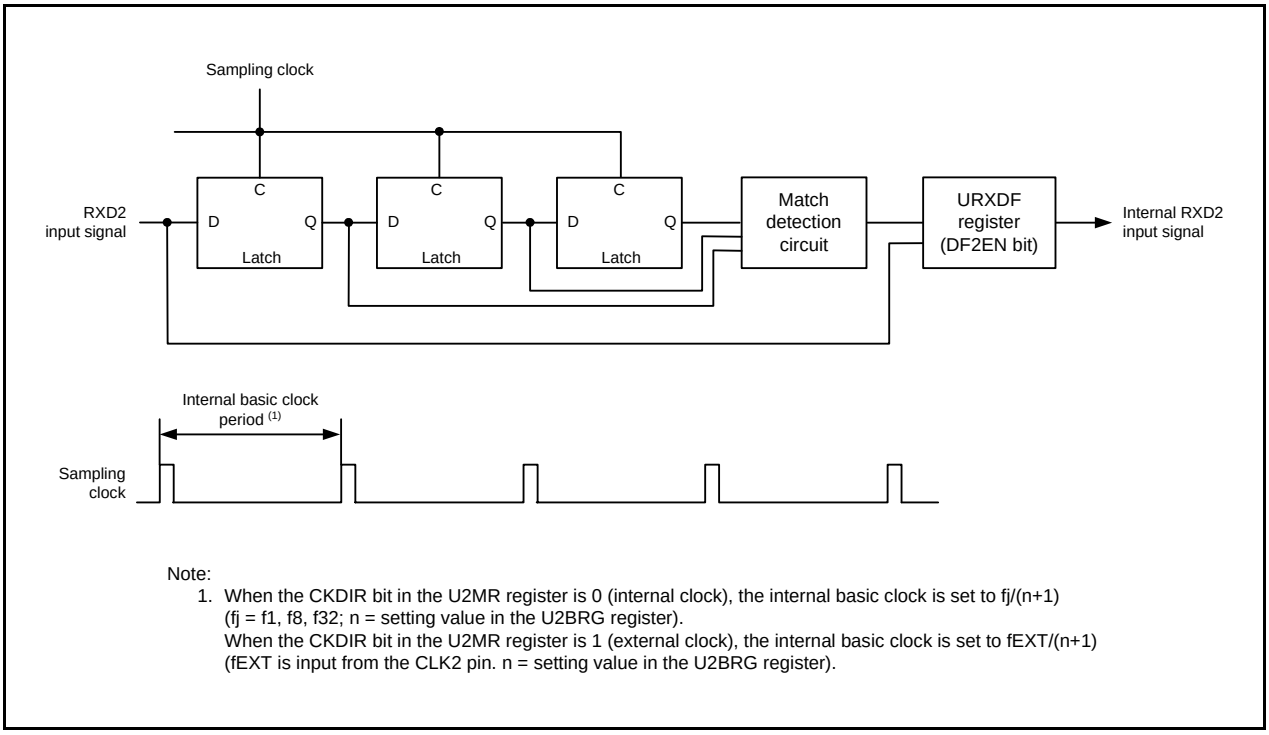
21.4.6 $\overline{\text{CTS}}/\overline{\text{RTS}}$ Function

The $\overline{\text{CTS}}$ function is used to start transmit operation when "L" is applied to the $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ pin. Transmit operation begins when the $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ pin is held low. If the "L" signal is switched to "H" during transmit operation, the operation stops after the ongoing transmit/receive operation is completed.
When the $\overline{\text{RTS}}$ function is used, the $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ pin outputs "L" when the MCU is ready for a receive operation.

- The CRD bit in the U2C0 register = 1 ($\overline{\text{CTS}}/\overline{\text{RTS}}$ function disabled)
  The $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ pin operates as the programmable I/O function.
- The CRD bit = 0, CRS bit = 0 ($\overline{\text{CTS}}$ function selected)
  The $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ pin operates as the $\overline{\text{CTS}}$ function.
- The CRD bit = 0, CRS bit = 1 ($\overline{\text{RTS}}$ function selected)
  The $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ pin operates as the $\overline{\text{RTS}}$ function.

21.4.7 RXD2 Digital Filter Select Function

When the DF2EN bit in the URXDF register is set to 1 (RXD2 digital filer enabled), the RXD2 input signal is loaded internally via the digital filter circuit for noise reduction. The noise canceller consists of three cascaded latch circuits and a match detection circuit. The RXD2 input signal is sampled on the internal basic clock with a frequency 16 times the bit rate. It is recognized as a signal and the level is passed forward to the next circuit when three latch outputs match. When the outputs do not match, the previous value is retained.
In other words, when the level is changed within three clocks, the change is recognized as not a signal but noise.
Figure 21.12 shows a Block Diagram of RXD2 Digital Filter Circuit.



Note:
1. When the CKDIR bit in the U2MR register is 0 (internal clock), the internal basic clock is set to fj/(n+1)
   (fj = f1, f8, f32; n = setting value in the U2BRG register).
   When the CKDIR bit in the U2MR register is 1 (external clock), the internal basic clock is set to fEXT/(n+1)
   (fEXT is input from the CLK2 pin. n = setting value in the U2BRG register).

Figure 21.12 Block Diagram of RXD2 Digital Filter Circuit

21.5 Multiprocessor Communication Function

When the multiprocessor communication function is used, data transmission/reception can be performed between a number of processors sharing communication lines by asynchronous serial communication, in which a multiprocessor bit is added to the data. For multiprocessor communication, each receiving station is addressed by a unique ID code. The serial communication cycle consists of two component cycles; an ID transmission cycle for specifying the receiving station, and a data transmission cycle for the specified receiving station. The multiprocessor bit is used to differentiate between the ID transmission cycle and the data transmission cycle. When the multiprocessor bit is set to 1, the cycle is an ID transmission cycle; when the multiprocessor bit is set to 0, the cycle is a data transmission cycle. Figure 21.13 shows an Inter-Processor Communication Example Using Multiprocessor Format (Data AAh Transmission to Receiving Station A).

The transmitting station first sends the ID code of the receiving station to perform communication as communication data with a 1 multiprocessor bit added. It then sends transmit data as communication data with a 0 multiprocessor bit added.

When communication data in which the multiprocessor bit is 1 is received, the receiving station compares that data with its own ID. If they match, the data to be sent next is received. If they do not match, the receive station continues to skip communication data until data in which the multiprocessor bit is 1 is again received.

UART2 uses the MPIE bit in the U2SMR5 register to implement this function. When the MPIE bit is set to 1, data transfer from the UART2 receive register to the U2RB register, receive error detection, and the settings of the status flags, the RI bit in the U2C1 register, bits FER and OER in the U2RB register, are disabled until data in which the multiprocessor bit is 1 is received. On receiving a receive character in which the multiprocessor bit is 1, the MPRB bit in the U2RB register is set to 1 and the MPIE in the U2SMR5 register bit is set to 0, thus normal reception is resumed.

When the multiprocessor format is specified, the parity bit specification is invalid. All other bit settings are the same as those in normal asynchronous mode (UART mode). The clock used for multiprocessor communication is the same as that in normal asynchronous mode (UART mode).

Figure 21.14 shows a Block Diagram of Multiprocessor Communication Function. Table 21.9 lists the Registers and Settings in Multiprocessor Communication Function.

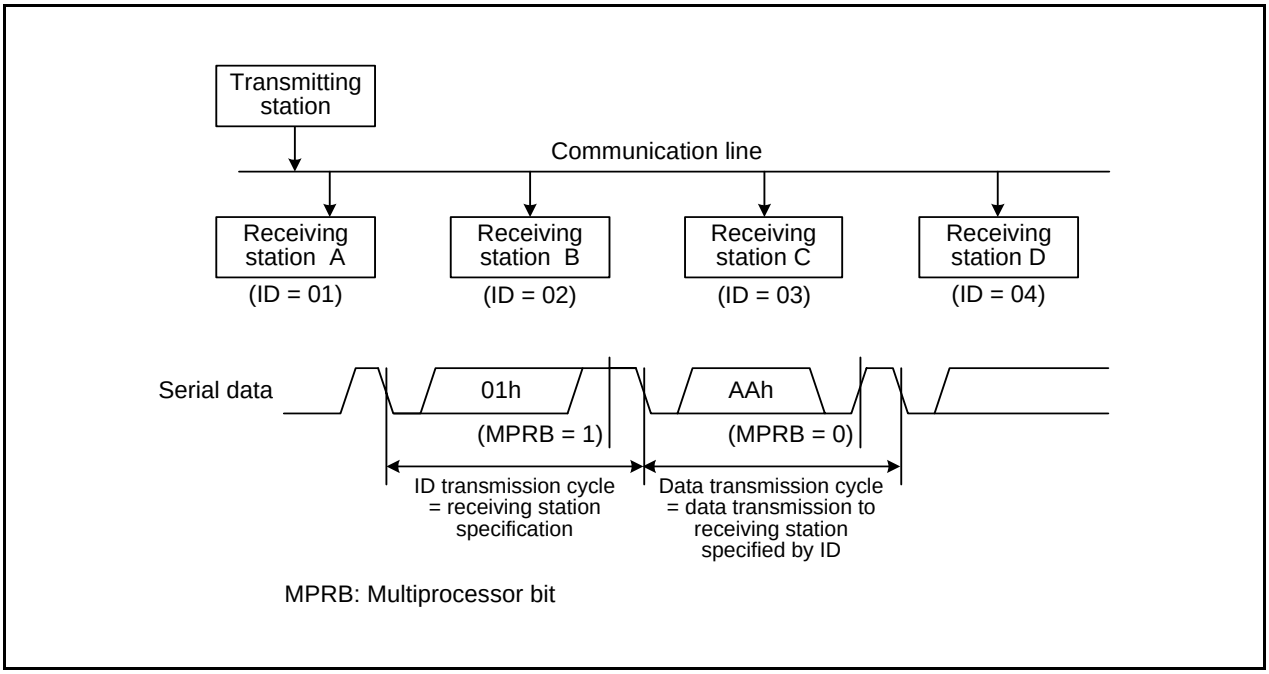


Figure 21.13 Inter-Processor Communication Example Using Multiprocessor Format (Data AAh Transmission to Receiving Station A)

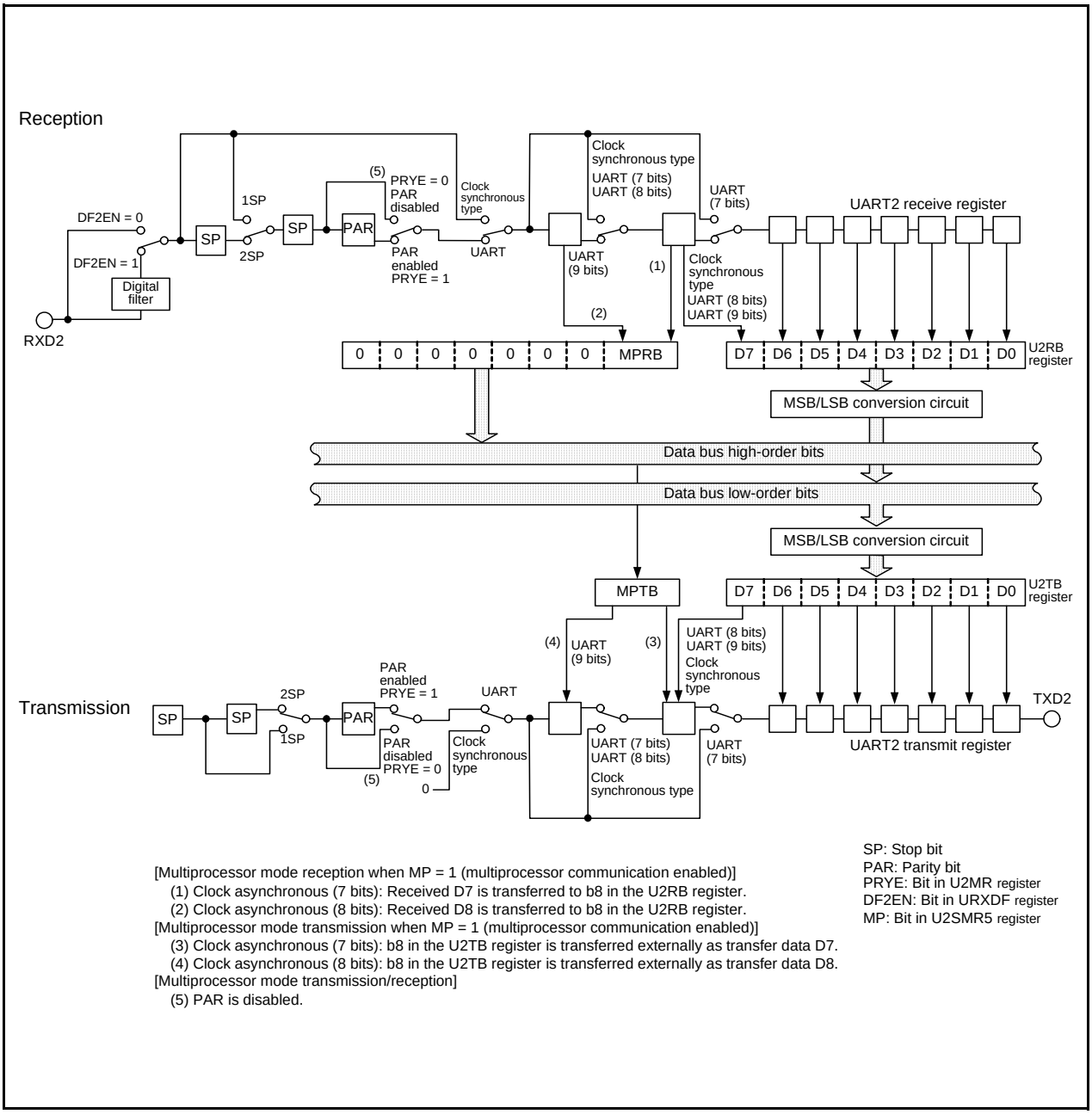


Figure 21.14 Block Diagram of Multiprocessor Communication Function

Table 21.9 Registers and Settings in Multiprocessor Communication Function

Register	Bit	Function
U2TB (1)	b0 to b7	Set transmit data.
	MPTB	Set to 0 or 1.
U2RB (2)	b0 to b7	Receive data can be read.
	MPRB	Multiprocessor bit
	OER, FER, SUM	Error flag
U2BRG	b0 to b7	Set the transfer rate.
U2MR	SMD2 to SMD0	Set to 100b when transfer data is 7 bits long.
		Set to 101b when transfer data is 8 bits long.
	CKDIR	Select the internal clock or external clock.
	STPS	Select the stop bit.
	PRY, PRYE	Parity detection function disabled
	IOPOL	Set to 0.
U2C0	CLK0, CLK1	Select the U2BRG count source.
	CRS	$\overline{\text{CTS}}$ or $\overline{\text{RTS}}$ function disabled
	TXEPT	Transmit register empty flag
	CRD	Set to 0.
	NCH	Select TXD2 pin output mode.
	CKPOL	Set to 0.
	UFORM	Set to 0.
U2C1	TE	Set to 1 to enable transmission.
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Receive complete flag
	U2IRS	Select the UART2 transmit interrupt source.
	U2LCH	Set to 0.
	U2ERE	Set to 0.
U2SMR	b0 to b7	Set to 0.
U2SMR2	b0 to b7	Set to 0.
U2SMR3	b0 to b7	Set to 0.
U2SMR4	b0 to b7	Set to 0.
U2SMR5	MP	Set to 1.
	MPIE	Set to 1.
URXDF	DF2EN	Select the digital filter enabled or disabled.

Notes:
1. Set the MPTB bit to 1 when the ID data frame is transmitted. Set this bit to 0 when the data frame is transmitted.
2. If the MPRB bit is set to 1, received D7 to D0 are ID fields. If the MPRB bit is set to 0, received D7 to D0 are data fields.

21.5.1 Multiprocessor Transmission

Figure 21.15 shows a Sample Flowchart of Multiprocessor Data Transmission. Set the MPBT bit in the U2TB register to 1 for ID transmission cycles. Set the MPBT bit in the U2TB register to 0 for data transmission cycles. Other operations are the same as in universal asynchronous receiver/transmitter mode (UART mode).

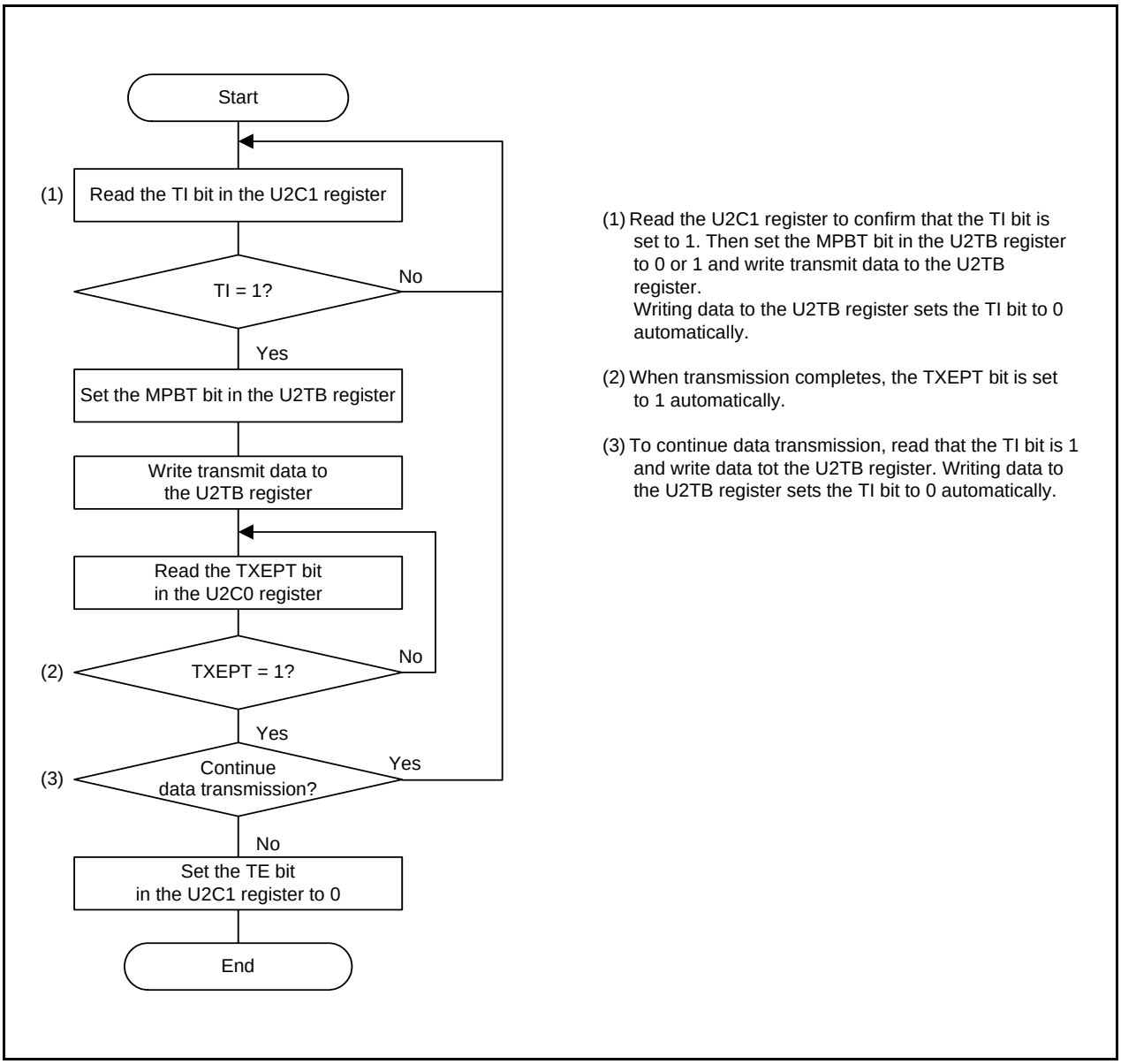


Figure 21.15 Sample Flowchart of Multiprocessor Data Transmission

21.5.2 Multiprocessor Reception

Figure 21.16 shows a Sample Flowchart of Multiprocessor Data Reception. When the MPIE bit in the U2SMR5 register is set to 1, communication data is ignored until data in which the multiprocessor bit is 1 is received. Communication data with a 1 multiprocessor bit added is transferred to the U2RB register as receive data. At this time, a reception complete interrupt request is generated. Other operations are the same as in universal asynchronous receiver/transmitter mode (UART mode). Figure 21.17 shows a Receive Operation Example during Multiprocessor Communication (with 8-Bit Data/Multiprocessor Bit/One-Stop Bit).

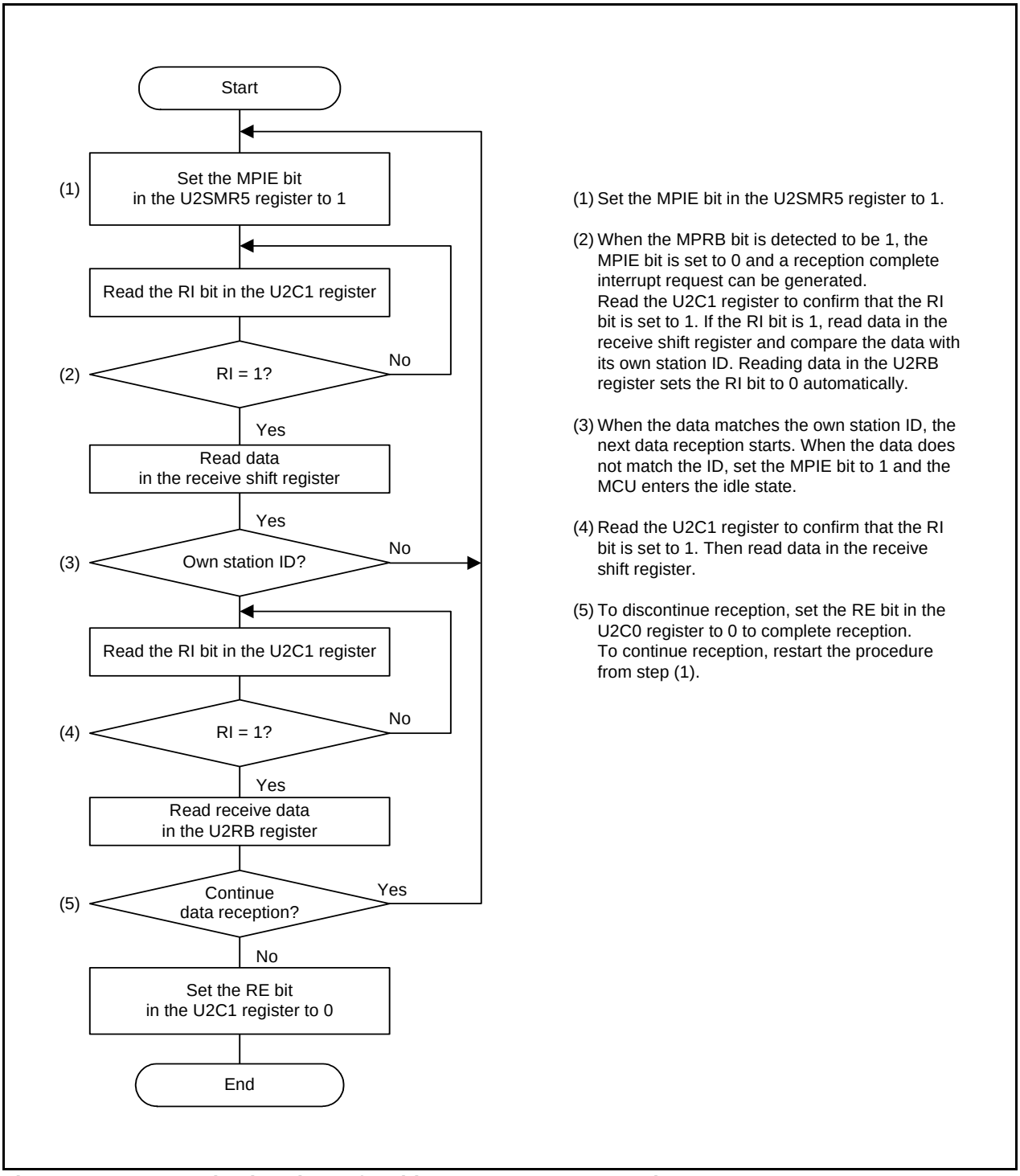


Figure 21.16 Sample Flowchart of Multiprocessor Data Reception

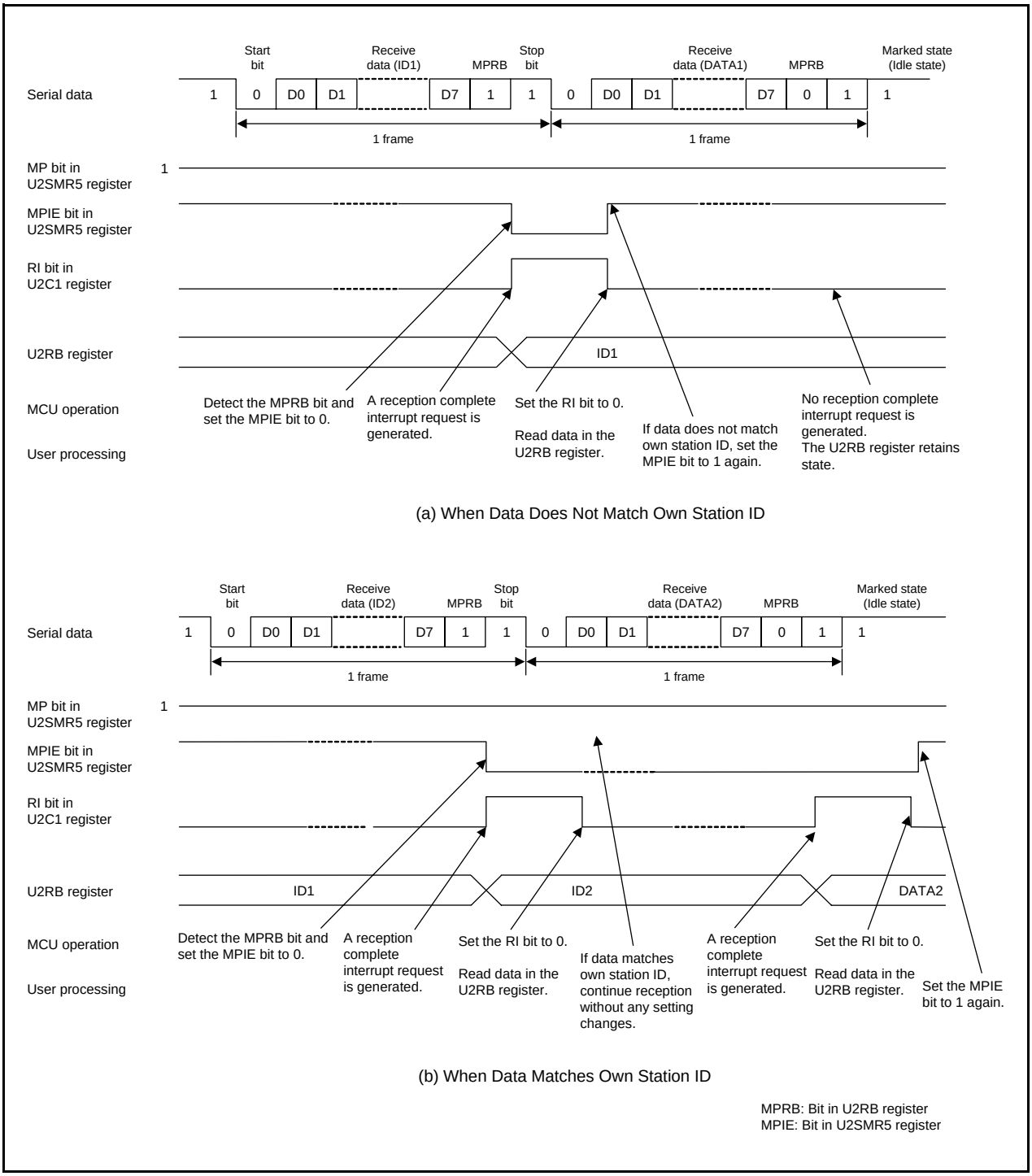
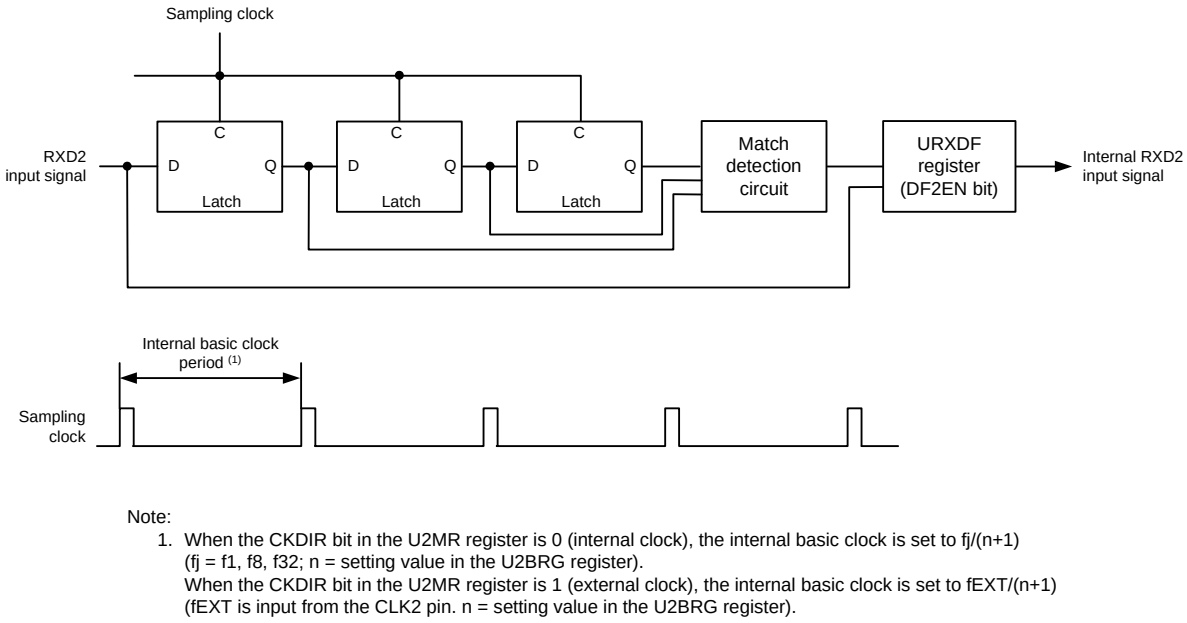


Figure 21.17 Receive Operation Example during Multiprocessor Communication (with 8-Bit Data/Multiprocessor Bit/One-Stop Bit)

21.5.3 RXD2 Digital Filter Select Function

When the DF2EN bit in the URXDF register is set to 1 (RXD2 digital filer enabled), the RXD2 input signal is loaded internally via the digital filter circuit for noise reduction. The noise canceller consists of three cascaded latch circuits and a match detection circuit. The RXD2 input signal is sampled on the internal basic clock with a frequency 16 times the bit rate. It is recognized as a signal and the level is passed forward to the next circuit when three latch outputs match. When the outputs do not match, the previous value is retained.
In other words, when the level is changed within three clocks, the change is recognized as not a signal but noise.
Figure 21.18 shows a Block Diagram of RXD2 Digital Filter Circuit.



Note:
1. When the CKDIR bit in the U2MR register is 0 (internal clock), the internal basic clock is set to fj/(n+1) (fj = f1, f8, f32; n = setting value in the U2BRG register).
When the CKDIR bit in the U2MR register is 1 (external clock), the internal basic clock is set to fEXT/(n+1) (fEXT is input from the CLK2 pin. n = setting value in the U2BRG register).

Figure 21.18 Block Diagram of RXD2 Digital Filter Circuit

21.6 Notes on Serial Interface (UART2)

21.6.1 Clock Synchronous Serial I/O Mode

21.6.1.1 Transmission/Reception

When the $\overline{\text{RTS}}$ function is used with an external clock, the $\overline{\text{RTS2}}$ pin outputs “L,” which informs the transmitting side that the MCU is ready for a receive operation. The $\overline{\text{RTS2}}$ pin outputs “H” when a receive operation starts. Therefore, the transmit timing and receive timing can be synchronized by connecting the $\overline{\text{RTS2}}$ pin to the $\overline{\text{CTS2}}$ pin of the transmitting side. The $\overline{\text{RTS}}$ function is disabled when an internal clock is selected.

21.6.1.2 Transmission

If an external clock is selected, the following conditions must be met while the external clock is held high when the CKPOL bit in the U2C0 register is set to 0 (transmit data output at the falling edge and receive data input at the rising edge of the transfer clock), or while the external clock is held low when the CKPOL bit is set to 1 (transmit data output at the rising edge and receive data input at the falling edge of the transfer clock).

- The TE bit in the U2C1 register = 1 (transmission enabled)
- The TI bit in the U2C1 register = 0 (data present in the U2TB register)
- If the $\overline{\text{CTS}}$ function is selected, input on the $\overline{\text{CTS2}}$ pin = “L”

21.6.1.3 Reception

In clock synchronous serial I/O mode, the shift clock is generated by activating the transmitter. Set the UART2-associated registers for transmit operation even if the MCU is used for receive operation only. Dummy data is output from the TXD2 pin while receiving.

When an internal clock is selected, the shift clock is generated by setting the TE bit in the U2C1 register to 1 (transmission enabled) and placing dummy data in the U2TB register. When an external clock is selected, set the TE bit to 1 (transmission enabled), place dummy data in the U2TB register, and input an external clock to the CLK2 pin to generate the shift clock.

If data is received consecutively, an overrun error occurs when the RE bit in the U2C1 register is set to 1 (data present in the U2RB register) and the next receive data is received in the UART2 receive register. Then, the OER bit in the U2RB register is set to 1 (overrun error). At this time, the U2RB register value is undefined. If an overrun error occurs, the IR bit in the S2RIC register remains unchanged.

To receive data consecutively, set dummy data in the low-order byte in the U2TB register per each receive operation.

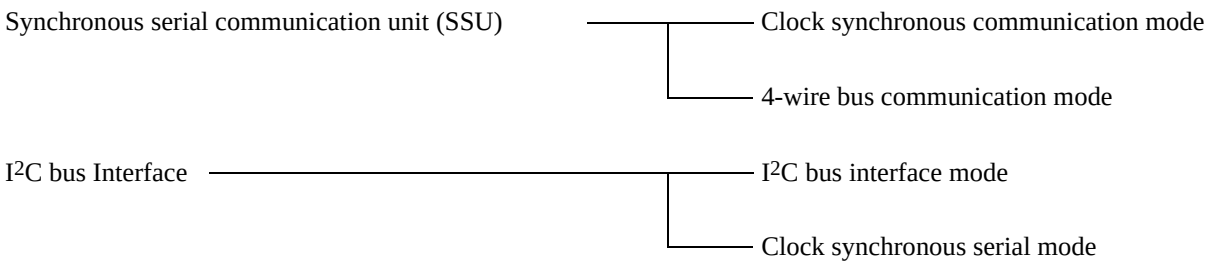
If an external clock is selected, the following conditions must be met while the external clock is held high when the CKPOL bit is set to 0, or while the external clock is held low when the CKPOL bit is set to 1.

- The RE bit in the U2C1 register = 1 (reception enabled)
- The TE bit in the U2C1 register = 1 (transmission enabled)
- The TI bit in the U2C1 register = 0 (data present in the U2TB register)

22. Clock Synchronous Serial Interface

The clock synchronous serial interface is configured as follows.

Clock synchronous serial interface



The clock synchronous serial interface uses the registers at addresses 0193h to 019Dh. Registers, bits, symbols, and functions vary even for the same addresses depending on the mode. Refer to the registers of each function for details. Also, the differences between clock synchronous communication mode and clock synchronous serial mode are the options of the transfer clock, clock output format, and data output format.

22.1 Mode Selection

The clock synchronous serial interface has four modes.

Table 22.1 lists the Mode Selections. Refer to **23. Synchronous Serial Communication Unit (SSU)**, **24. I2C bus Interface** and the sections that follow for details of each mode.

Table 22.1 Mode Selections

IICSEL Bit in SSUIICSR Register	Bit 7 in 0198h (ICE Bit in ICCR1 Register)	Bit 0 in 019Dh (SSUMS Bit in SSMR2 Register, FS Bit in SAR Register)	Function	Mode
0	0	0	Synchronous serial communication unit	Clock synchronous communication mode
0	0	1		4-wire bus communication mode
1	1	0	I2C bus interface	I2C bus interface mode
1	1	1		Clock synchronous serial mode

23. Synchronous Serial Communication Unit (SSU)

Synchronous serial communication unit (SSU) supports clock synchronous serial data communication.

23.1 Overview

Table 23.1 shows a Synchronous Serial Communication Unit Specifications and Figure 23.1 shows a Block Diagram of Synchronous Serial Communication Unit.

Table 23.1 Synchronous Serial Communication Unit Specifications

Item	Specification
Transfer data format	Transfer data length: 8 to 16 bits Continuous transmission and reception of serial data are supported since both transmitter and receiver have buffer structures.
Operating modes	• Clock synchronous communication mode • 4-wire bus communication mode (including bidirectional communication)
Master/slave device	Selectable
I/O pins	SSCK (I/O): Clock I/O pin SSI (I/O): Data I/O pin $\overline{\text{SSO}}$ (I/O): Data I/O pin $\overline{\text{SCS}}$ (I/O): Chip-select I/O pin
Transfer clocks	• When the MSS bit in the SSCRH register is set to 0 (operates as slave device), external clock is selected (input from SSCK pin). • When the MSS bit in the SSCRH register is set to 1 (operates as master device), internal clock (selectable among f1/256, f1/128, f1/64, f1/32, f1/16, f1/8 and f1/4, output from SSCK pin) is selected. • Clock polarity and phase of SSCK can be selected.
Receive error detection	Overrun error Overrun error occurs during reception and completes in error. While the RDRF bit in the SSSR register is set to 1 (data in the SSRDR register) and when next serial data receive is completed, the ORER bit is set to 1.
Multimaster error detection	• Conflict error When the SSUMS bit in the SSMR2 register is set to 1 (4-wire bus communication mode) and the MSS bit in the SSCRH register is set to 1 (operates as master device) and when starting a serial communication, the CE bit in the SSSR register is set to 1 if “L” applies to the $\overline{\text{SCS}}$ pin input. When the SSUMS bit in the SSMR2 register is set to 1 (4-wire bus communication mode), the MSS bit in the SSCRH register is set to 0 (operates as slave device) and the $\overline{\text{SCS}}$ pin input changes state from “L” to “H”, the CE bit in the SSSR register is set to 1.
Interrupt requests	5 interrupt requests (transmit-end, transmit-data-empty, receive-data-full, overrun error, and conflict error). (1)
Selectable functions	• Data transfer direction Selects MSB-first or LSB-first • SSCK clock polarity Selects “L” or “H” level when clock stops • SSCK clock phase Selects edge of data change and data download

Note:
1. Synchronous serial communication unit has only one interrupt vector table.

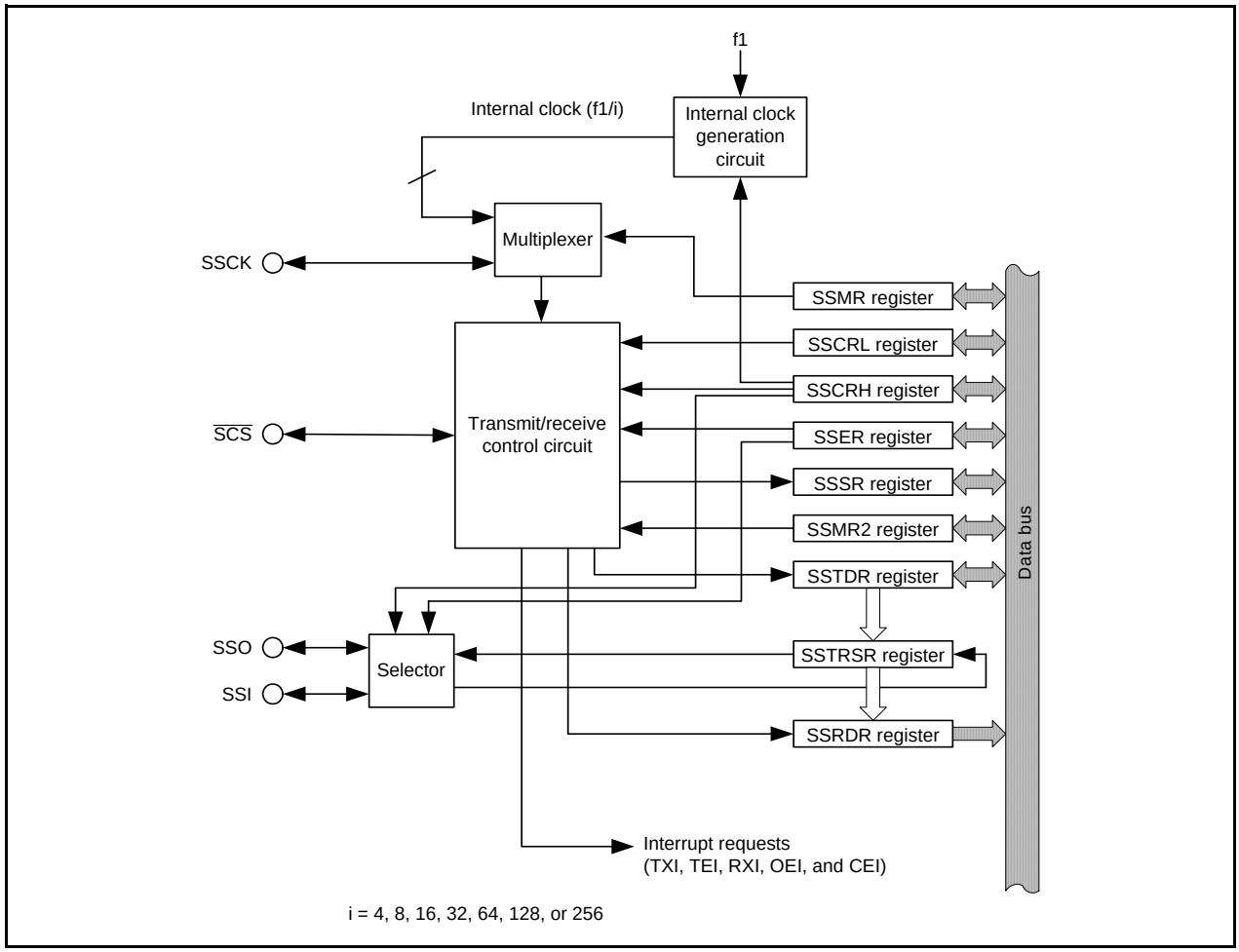


Figure 23.1 Block Diagram of Synchronous Serial Communication Unit

Table 23.2 Pin Configuration of Synchronous Serial Communication Unit

Pin Name	Assigned Pin	I/O	Function
SSI	P3_4	I/O	Data I/O pin
$\overline{\text{SCS}}$	P3_3	I/O	Chip-select signal I/O pin
SSCK	P3_5	I/O	Clock I/O pin
SSO	P3_7	I/O	Data I/O pin

23.2 Registers

23.2.1 Module Standby Control Register (MSTCR)

Address 0008h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	MSTTRC	—	MSTIIC	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	—			
b2	—			
b3	MSTIIC	SSU, I2C bus standby bit	0: Active 1: Standby (1)	R/W
b4	—	Reserved bit	Set to 0.	R/W
b5	MSTTRC	Timer RC standby bit	0: Active 1: Standby (2)	R/W
b6	—	Reserved bit	Set to 0.	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Notes:
1. Stop the SSU and the I2C bus functions before setting to standby. When the MSTIIC bit is set to 1 (standby), any access to the SSU or the I2C bus associated registers (addresses 0193h to 019Dh) is disabled.
2. Stop the timer RC function before setting to standby. When the MSTTRC bit is set to 1 (standby), any access to the timer RC associated registers (addresses 0120h to 0133h (0133h is not available in the R8C/3MU Group)) is disabled.

23.2.2 SSU/IIC Pin Select Register (SSUIICSR)

Address 018Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	IICSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IICSEL	SSU/I2C bus switch bit	0: SSU function selected 1: I2C bus function selected	R/W
b1	—	Reserved bit	Set to 0.	R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	—			
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—			
b7	—			

23.2.3 SS Bit Counter Register (SSBR)

Address 0193h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	BS3	BS2	BS1	BS0
After Reset	1	1	1	1	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	BS0	SSU data transfer length set bit (1)	b3 b2 b1 b0 0 0 0 0: 16 bits 1 0 0 0: 8 bits 1 0 0 1: 9 bits 1 0 1 0: 10 bits 1 0 1 1: 11 bits 1 1 0 0: 12 bits 1 1 0 1: 13 bits 1 1 1 0: 14 bits 1 1 1 1: 15 bits	R/W
b1	BS1			R/W
b2	BS2			R/W
b3	BS3			R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b5	—			
b6	—			
b7	—			

Note:
1. Do not write to bits BS0 to BS3 during SSU operation.

To set the SSBR register, set the RE bit in the SSER register to 0 (reception disabled) and the TE bit to 0 (transmission disabled).

Bits BS0 to BS3 (SSU Data Transfer Length Set Bit)

As the SSU data transfer length, 8 to 16 bits can be used.

23.2.4 SS Transmit Data Register (SSTDR)

Address 0195h to 0194h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
b15 to b0	—	Store the transmit data. (1) The stored transmit data is transferred to the SSTRSR register and transmission is started when it is detected that the SSTRSR register is empty. When the next transmit data is written to the SSTDR register during the data transmission from the SSTRSR register, the data can be transmitted continuously. When the MLS bit in the SSMR register is set to 1 (transfer data with LSB-first), the data in which MSB and LSB are reversed is read, after writing to the SSTDR register.	R/W

Note:
1. When the SSU data transfer length is set to 9 bits or more with the SSBR register, access the SSTDR register in 16-bit units.

23.2.5 SS Receive Data Register (SSRDR)

Address 0197h to 0196h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
b15 to b0	—	Store the receive data. (1, 2) The receive data is transferred to the SSRDR register and the receive operation is completed when 1 byte of data has been received by the SSTRSR register. At this time, the next receive operation is possible. Continuous reception is possible using registers SSTRSR and SSRDR.	R

Notes:
1. The SSRDR register retains the data received before an overrun error occurs (ORER bit in the SSSR register set to 1 (overrun error)). When an overrun error occurs, the receive data may contain errors and therefore should be discarded.
2. When the SSU data transfer length is set to 9 bits or more with the SSBR register, access the SSRDR register in 16-bit units.

23.2.6 SS Control Register H (SSCRH)

Address 0198h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	RSSTP	MSS	—	—	CKS2	CKS1	CKS0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CKS0	Transfer clock select bit (1)	b2 b1 b0 0 0 0: f1/256 0 0 1: f1/128 0 1 0: f1/64 0 1 1: f1/32 1 0 0: f1/16 1 0 1: f1/8 1 1 0: f1/4 1 1 1: Do not set.	R/W
b1	CKS1			R/W
b2	CKS2			R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—			
b5	MSS	Master/slave device select bit (2)	0: Operates as slave device 1: Operates as master device	R/W
b6	RSSTP	Receive single stop bit (3)	0: Maintains receive operation after receiving 1 byte of data 1: Completes receive operation after receiving 1 byte of data	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Notes:
1. The set clock is used when the MSS bit is set to 1 (operates as master device).
2. The SSCK pin functions as the transfer clock output pin when the MSS bit is set to 1 (operates as master device). The MSS bit is set to 0 (operates as slave device) when the CE bit in the SSSR register is set to 1 (conflict error occurs).
3. The RSSTP bit is disabled when the MSS bit is set to 0 (operates as slave device).

23.2.7 SS Control Register L (SSCRL)

Address 0199h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	SOL	SOLP	—	—	SRES	—
After Reset	0	1	1	1	1	1	0	1

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b1	SRES	SSU control unit reset bit	Writing 1 to this bit resets the SSU control unit and the SSTRSR register. The value in the SSU internal register (1) is retained.	R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b3	—			
b4	SOLP	SOL write protect bit (2)	The output level can be changed by the SOL bit when this bit is set to 0. The SOLP bit remains unchanged even if 1 is written to it. When read, the content is 1.	R/W
b5	SOL	Serial data output value setting bit	When read 0: The serial data output is set to “L”. 1: The serial data output is set to “H”. When written (2, 3) 0: The data output is “L”. 1: The data output is “H”.	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Notes:
1. Registers SSBR, SSCRH, SSCRL, SSMR, SSER, SSSR, SSMR2, SSTDR, and SSRDR.
2. For the data output after serial data transmission, the last bit value of the transmitted serial data is retained. If the content of the SOL bit is rewritten before or after serial data transmission, the change is immediately reflected in the data output. When writing to the SOL bit, set the SOLP bit to 0 and the SOL bit to 0 or 1 simultaneously by the MOV instruction.
3. Do not write to the SOL bit during data transfer.

23.2.8 SS Mode Register (SSMR)

Address 019Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	MLS	CPOS	CPHS	—	BC3	BC2	BC1	BC0
After Reset	0	0	0	1	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	BC0	Bits counter 3 to 0	b3 b2 b1 b0 0 0 0 0: 16 bits left 0 0 0 1: 1 bit left 0 0 1 0: 2 bits left 0 0 1 1: 3 bits left 0 1 0 0: 4 bits left 0 1 0 1: 5 bits left 0 1 1 0: 6 bits left 0 1 1 1: 7 bits left 1 0 0 0: 8 bits left 1 0 0 1: 9 bits left 1 0 1 0: 10 bits left 1 0 1 1: 11 bits left 1 1 0 0: 12 bits left 1 1 0 1: 13 bits left 1 1 1 0: 14 bits left 1 1 1 1: 15 bits left	R
b1	BC1			R
b2	BC2			R
b3	BC3			R
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b5	CPHS	SSCK clock phase select bit (1)	0: Change data at odd edge (Download data at even edge) 1: Change data at even edge (Download data at odd edge)	R/W
b6	CPOS	SSCK clock polarity select bit (1)	0: “H” when clock stops 1: “L” when clock stops	R/W
b7	MLS	MSB first/LSB first select bit	0: Transfers data MSB first 1: Transfers data LSB first	R/W

Note:

1. Refer to **23.3.1.1 Association between Transfer Clock Polarity, Phase, and Data** for the settings of the CPHS and CPOS bits.
   When the SSUMS bit in the SSMR2 register is set to 0 (clock synchronous communication mode), set the CPHS bit to 0 and the CPOS bit to 0.

23.2.9 SS Enable Register (SSER)

Address 019Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIE	TEIE	RIE	TE	RE	—	—	CEIE
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CEIE	Conflict error interrupt enable bit	0: Disables conflict error interrupt request 1: Enables conflict error interrupt request	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	—			
b3	RE	Receive enable bit	0: Disables receive 1: Enables receive	R/W
b4	TE	Transmit enable bit	0: Disables transmit 1: Enables transmit	R/W
b5	RIE	Receive interrupt enable bit	0: Disables receive data full and overrun error interrupt request 1: Enables receive data full and overrun error interrupt request	R/W
b6	TEIE	Transmit end interrupt enable bit	0: Disables transmit end interrupt request 1: Enables transmit end interrupt request	R/W
b7	TIE	Transmit interrupt enable bit	0: Disables transmit data empty interrupt request 1: Enables transmit data empty interrupt request	R/W

23.2.10 SS Status Register (SSSR)

Address 019Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TDRE	TEND	RDRF	—	—	ORER	—	CE
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CE	Conflict error flag (1)	0: No conflict errors generated 1: Conflict errors generated (2)	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	ORER	Overrun error flag (1)	0: No overrun errors generated 1: Overrun errors generated (3)	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—			
b5	RDRF	Receive data register full flag (1, 4)	0: No data in SSRDR register 1: Data in SSRDR register	R/W
b6	TEND	Transmit end flag (1, 5)	0: The TDRE bit is set to 0 when transmitting the last bit of transmit data 1: The TDRE bit is set to 1 when transmitting the last bit of transmit data	R/W
b7	TDRE	Transmit data empty flag (1, 5, 6)	0: Data is not transferred from registers SSTDR to SSTRSR 1: Data is transferred from registers SSTDR to SSTRSR	R/W

Notes:

1. Writing 1 to CE, ORER, RDRF, TEND, or TDRE bits is invalid. To set any of these bits to 0, first read 1 then write 0.
2. When the serial communication is started while the SSUMS bit in the SSMR2 register is set to 1 (four-wire bus communication mode) and the MSS bit in the SSCRH register is set to 1 (operates as master device), the CE bit is set to 1 if “L” is applied to the $\overline{\text{SCS}}$ pin input. Refer to **23.5.4 SCS Pin Control and Arbitration** for more information.
   When the SSUMS bit in the SSMR2 register is set to 1 (four-wire bus communication mode), the MSS bit in the SSCRH register is set to 0 (operates as slave device) and the $\overline{\text{SCS}}$ pin input changes the level from “L” to “H” during transfer, the CE bit is set to 1.
3. Indicates when overrun errors occur and receive completes by error reception. If the next serial data receive operation is completed while the RDRF bit is set to 1 (data in the SSRDR register), the ORER bit is set to 1.
   After the ORER bit is set to 1 (overrun error), receive operation is disabled while the bit remains 1.
4. The RDRF bit is set to 0 when reading out the data from the SSRDR register.
5. Bits TEND and TDRE are set to 0 when writing data to the SSTDR register.
   When reading these bits immediately after writing to the SSTDR register, insert three or more NOP instructions between the instructions used for writing and reading.
6. The TDRE bit is set to 1 when the TE bit in the SSER register is set to 1 (transmit enabled).

If the SSSR register is accessed continuously, insert one or more NOP instructions between the instructions used for access.

23.2.11 SS Mode Register 2 (SSMR2)

Address 019Dh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	BIDE	SCKS	CSS1	CSS0	SCKOS	SOOS	CSOS	SSUMS
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	SSUMS	SSU mode select bit (1)	0: Clock synchronous communication mode 1: Four-wire bus communication mode	R/W
b1	CSOS	$\overline{SCS}$ pin open drain output select bit	0: CMOS output 1: N-channel open-drain output	R/W
b2	SOOS	Serial data pin open output drain select bit (1)	0: CMOS output (5) 1: N-channel open-drain output	R/W
b3	SCKOS	SSCK pin open drain output select bit	0: CMOS output 1: N-channel open-drain output	R/W
b4	CSS0	$\overline{SCS}$ pin select bit (2)	b5 b4 0 0: Functions as port 0 1: Functions as $\overline{SCS}$ input pin 1 0: Functions as $\overline{SCS}$ output pin (3) 1 1: Functions as $\overline{SCS}$ output pin (3)	R/W
b5	CSS1			R/W
b6	SCKS	SSCK pin select bit	0: Functions as port 1: Functions as serial clock pin	R/W
b7	BIDE	Bidirectional mode enable bit (1, 4)	0: Standard mode (communication using 2 pins of data input and data output) 1: Bidirectional mode (communication using 1 pin of data input and data output)	R/W

Notes:
1. Refer to **23.3.2.1 Association between Data I/O Pins and SS Shift Register** for information on combinations of data I/O pins.
2. The $\overline{SCS}$ pin functions as a port, regardless of the values of bits CSS0 and CSS1 when the SSUMS bit is set to 0 (clock synchronous communication mode).
3. This bit functions as the $\overline{SCS}$ input pin before starting transfer.
4. The BIDE bit is disabled when the SSUMS bit is set to 0 (clock synchronous communication mode).
5. When the SOOS bit is set to 0 (CMOS output), set the port direction register bits corresponding to pins SSI and SSO to 0 (input mode).

23.3 Common Items for Multiple Modes

23.3.1 Transfer Clock

The transfer clock can be selected from among seven internal clocks (f1/256, f1/128, f1/64, f1/32, f1/16, f1/8, and f1/4) and an external clock.
When using synchronous serial communication unit, set the SCKS bit in the SSMR2 register to 1 and select the SSCK pin as the serial clock pin.
When the MSS bit in the SSCRH register is set to 1 (operates as master device), an internal clock can be selected and the SSCK pin functions as output. When transfer is started, the SSCK pin outputs clocks of the transfer rate selected by bits CKS0 to CKS2 in the SSCRH register.
When the MSS bit in the SSCRH register is set to 0 (operates as slave device), an external clock can be selected and the SSCK pin functions as input.

23.3.1.1 Association between Transfer Clock Polarity, Phase, and Data

The association between the transfer clock polarity, phase and data changes according to the combination of the SSUMS bit in the SSMR2 register and bits CPHS and CPOS in the SSMR register. Figure 23.2 shows the Association between Transfer Clock Polarity, Phase, and Transfer Data.
Also, the MSB-first transfer or LSB-first transfer can be selected by setting the MLS bit in the SSMR register. When the MLS bit is set to 1, transfer is started from the LSB and proceeds to the MSB. When the MLS bit is set to 0, transfer is started from the MSB and proceeds to the LSB.

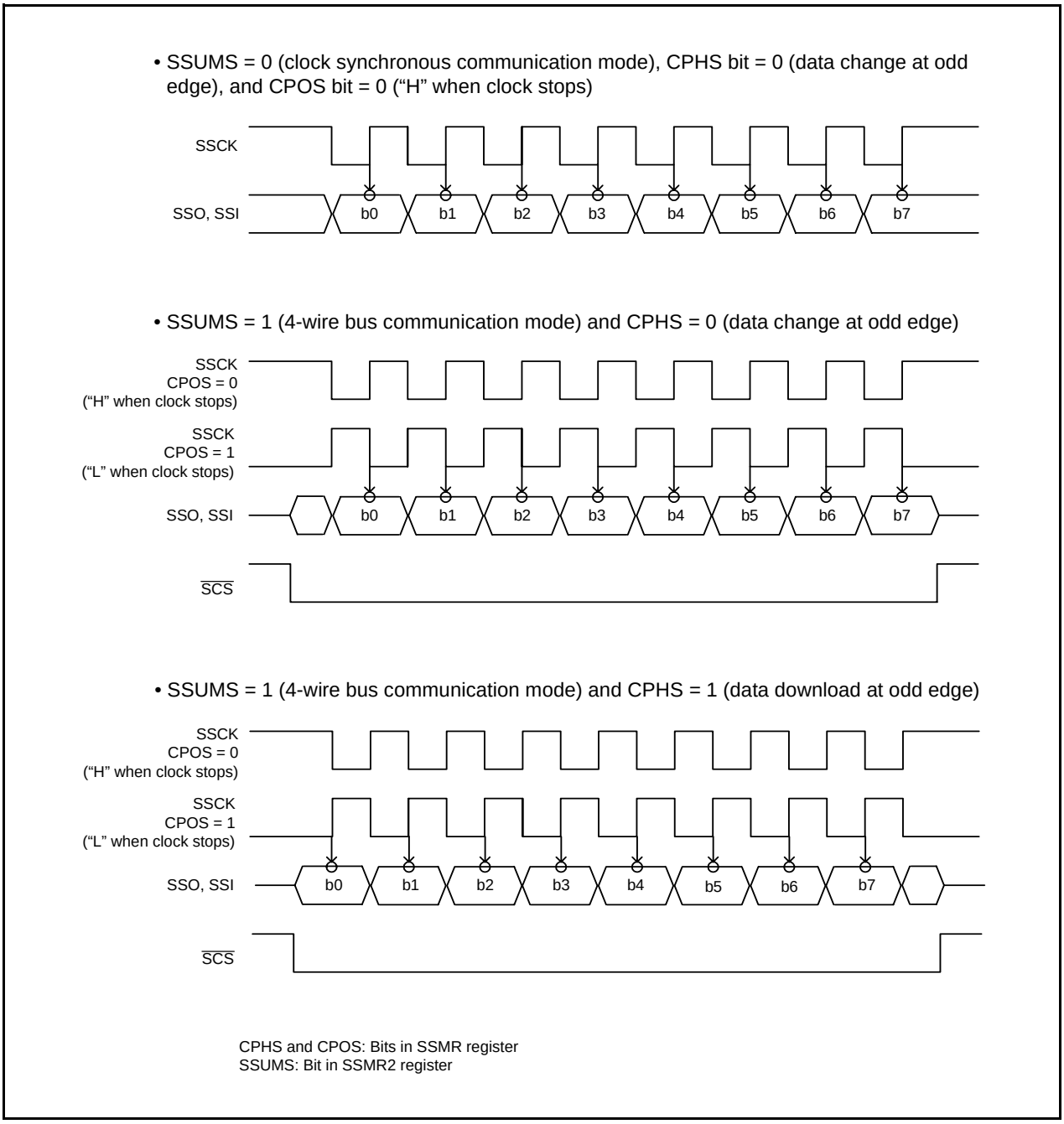


Figure 23.2 Association between Transfer Clock Polarity, Phase, and Transfer Data

23.3.2 SS Shift Register (SSTRSR)

The SSTRSR register is a shift register for transmitting and receiving serial data.
When transmit data is transferred from the SSTDR register to the SSTRSR register and the MLS bit in the SSMR register is set to 0 (MSB-first), the bit 0 in the SSTDR register is transferred to bit 0 in the SSTRSR register. When the MLS bit is set to 1 (LSB-first), bit 7 in the SSTDR register is transferred to bit 0 in the SSTRSR register.

23.3.2.1 Association between Data I/O Pins and SS Shift Register

The connection between the data I/O pins and SSTRSR register (SS shift register) changes according to a combination of the MSS bit in the SSCRH register and the SSUMS bit in the SSMR2 register. The connection also changes according to the BIDE bit in the SSMR2 register. Figure 23.3 shows the Association between Data I/O Pins and SSTRSR Register.

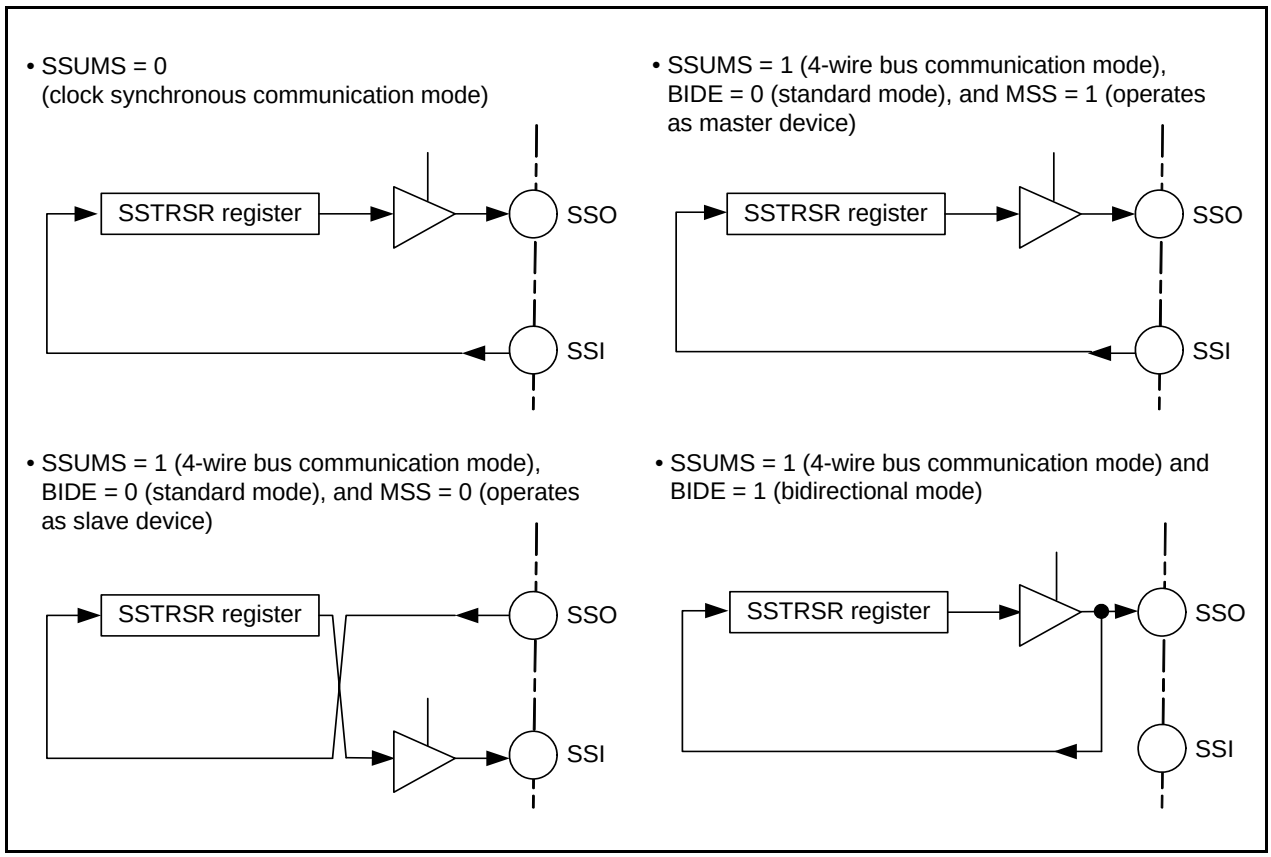


Figure 23.3 Association between Data I/O Pins and SSTRSR Register

23.3.3 Interrupt Requests

Synchronous serial communication unit has five interrupt requests: transmit data empty, transmit end, receive data full, overrun error, and conflict error. Since these interrupt requests are assigned to the synchronous serial communication unit interrupt vector table, determining interrupt sources by flags is required. Table 23.3 shows the Synchronous Serial Communication Unit Interrupt Requests.

Table 23.3 Synchronous Serial Communication Unit Interrupt Requests

Interrupt Request	Abbreviation	Generation Condition
Transmit data empty	TXI	TIE = 1, TDRE = 1
Transmit end	TEI	TEIE = 1, TEND = 1
Receive data full	RXI	RIE = 1, RDRF = 1
Overrun error	OEI	RIE = 1, ORER = 1
Conflict error	CEI	CEIE = 1, CE = 1

CEIE, RIE, TEIE and TIE: Bits in SSER register
ORER, RDRF, TEND and TDRE: Bits in SSSR register

If the generation conditions in Table 23.3 are met, a synchronous serial communication unit interrupt request is generated. Set each interrupt source to 0 by a synchronous serial communication unit interrupt routine.

However, the TDRE and TEND bits are automatically set to 0 by writing transmit data to the SSTDR register and the RDRF bit is automatically set to 0 by reading the SSRDR register. In particular, the TDRE bit is set to 1 (data transmitted from registers SSTDR to SSTRSR) at the same time transmit data is written to the SSTDR register. Setting the TDRE bit to 0 (data not transmitted from registers SSTDR to SSTRSR) can cause an additional byte of data to be transmitted.

23.3.4 Communication Modes and Pin Functions

Synchronous serial communication unit switches the functions of the I/O pins in each communication mode according to the setting of the MSS bit in the SSCRH register and bits RE and TE in the SSER register. Table 23.4 shows the Association between Communication Modes and I/O Pins.

Table 23.4 Association between Communication Modes and I/O Pins

Communication Mode	Bit Setting					Pin State		
	SSUMS	BIDE	MSS	TE	RE	SSI	SSO	SSCK
Clock synchronous communication mode	0	Disabled	0	0	1	Input	— (1)	Input
				1	0	— (1)	Output	Input
					1	Input	Output	Input
			1	0	1	Input	— (1)	Output
				1	0	— (1)	Output	Output
					1	Input	Output	Output
4-wire bus communication mode	1	0	0	0	1	— (1)	Input	Input
				1	0	Output	— (1)	Input
					1	Output	Input	Input
			1	0	1	Input	— (1)	Output
				1	0	— (1)	Output	Output
					1	Input	Output	Output
4-wire bus (bidirectional) communication mode (2)	1	1	0	0	1	— (1)	Input	Input
				1	0	— (1)	Output	Input
			1	0	1	— (1)	Input	Output
				1	0	— (1)	Output	Output

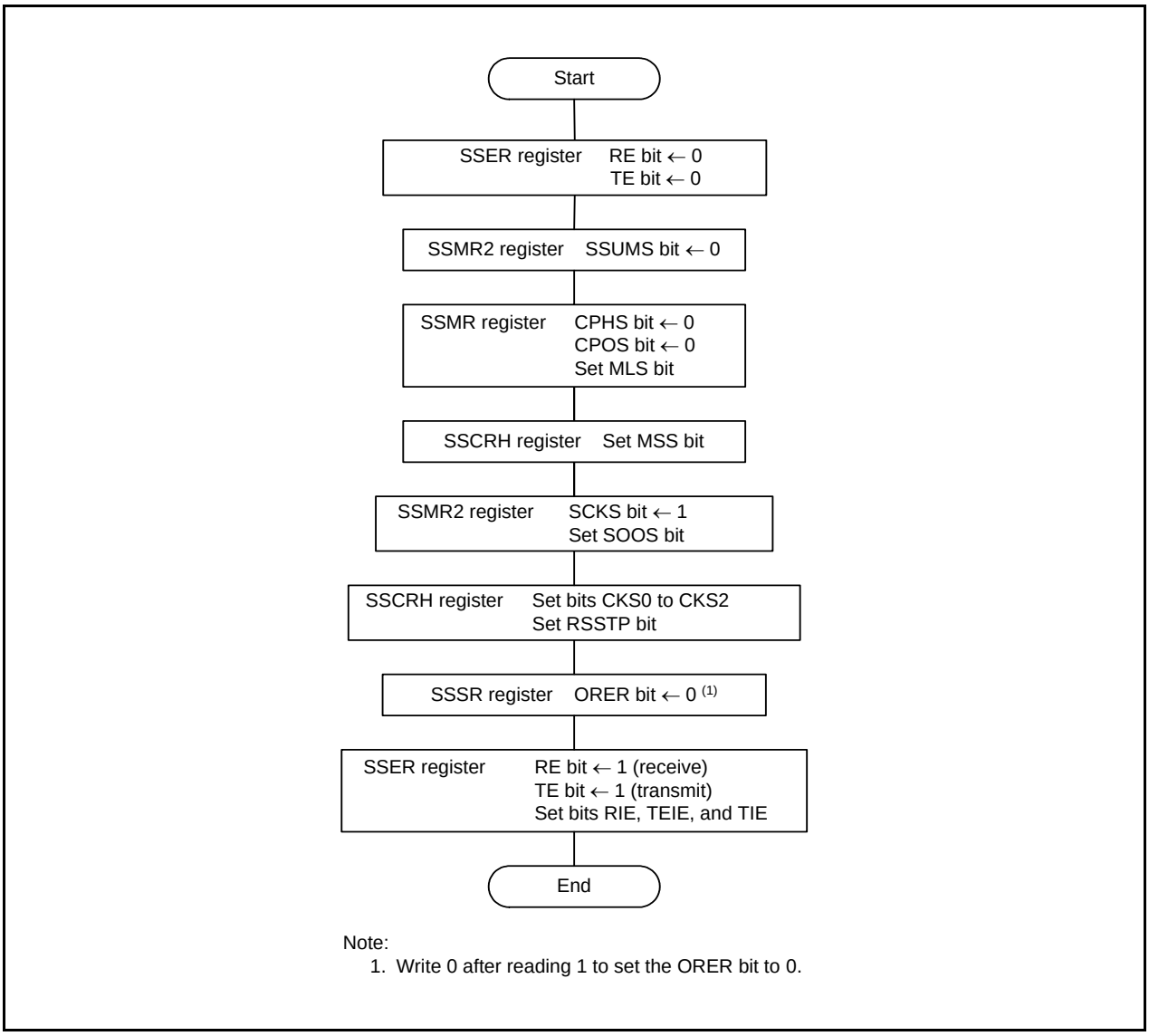
Notes:
1. This pin can be used as a programmable I/O port.
2. Do not set both bits TE and RE to 1 in 4-wire bus (bidirectional) communication mode.

SSUMS and BIDE: Bits in SSMR2 register
MSS: Bit in SSCRH register
TE and RE: Bits in SSER register

23.4 Clock Synchronous Communication Mode

23.4.1 Initialization in Clock Synchronous Communication Mode

Figure 23.4 shows Initialization in Clock Synchronous Communication Mode. To initialize, set the TE bit in the SSER register to 0 (transmit disabled) and the RE bit to 0 (receive disabled) before data transmission or reception.
Set the TE bit to 0 and the RE bit to 0 before changing the communication mode or format.
Setting the RE bit to 0 does not change the contents of flags RDRF and ORER or the contents of the SSRDR register.



Note:
1. Write 0 after reading 1 to set the ORER bit to 0.

Figure 23.4 Initialization in Clock Synchronous Communication Mode

23.4.2 Data Transmission

Figure 23.5 shows an Example of Synchronous Serial Communication Unit Operation for Data Transmission (Clock Synchronous Communication Mode, 8-Bit SSU Data Transfer Length). During data transmission, the synchronous serial communication unit operates as described below. (The data transfer length can be set from 8 to 16 bits using the SSBR register.)

When synchronous serial communication unit is set as a master device, it outputs a synchronous clock and data. When synchronous serial communication unit is set as a slave device, it outputs data synchronized with the input clock.

When the TE bit is set to 1 (transmit enabled) before writing the transmit data to the SSTDR register, the TDRE bit is automatically set to 0 (data not transferred from registers SSTDR to SSTRSR) and the data is transferred from registers SSTDR to SSTRSR.

After the TDRE bit is set to 1 (data transferred from registers SSTDR to SSTRSR), transmission starts. When the TIE bit in the SSER register is set to 1, the TXI interrupt request is generated. When one frame of data is transferred while the TDRE bit is set to 0, data is transferred from registers SSTDR to SSTRSR and transmission of the next frame is started. If the 8th bit is transmitted while the TDRE bit is set to 1, the TEND bit in the SSSR register is set to 1 (the TDRE bit is set to 1 when the last bit of the transmit data is transmitted) and the state is retained. The TEI interrupt request is generated when the TEIE bit in the SSER register is set to 1 (transmit-end interrupt request enabled). The SSCK pin is fixed “H” after transmit-end.

Transmission cannot be performed while the ORER bit in the SSSR register is set to 1 (overrun error). Confirm that the ORER bit is set to 0 before transmission.

Figure 23.6 shows a Sample Flowchart of Data Transmission (Clock Synchronous Communication Mode).

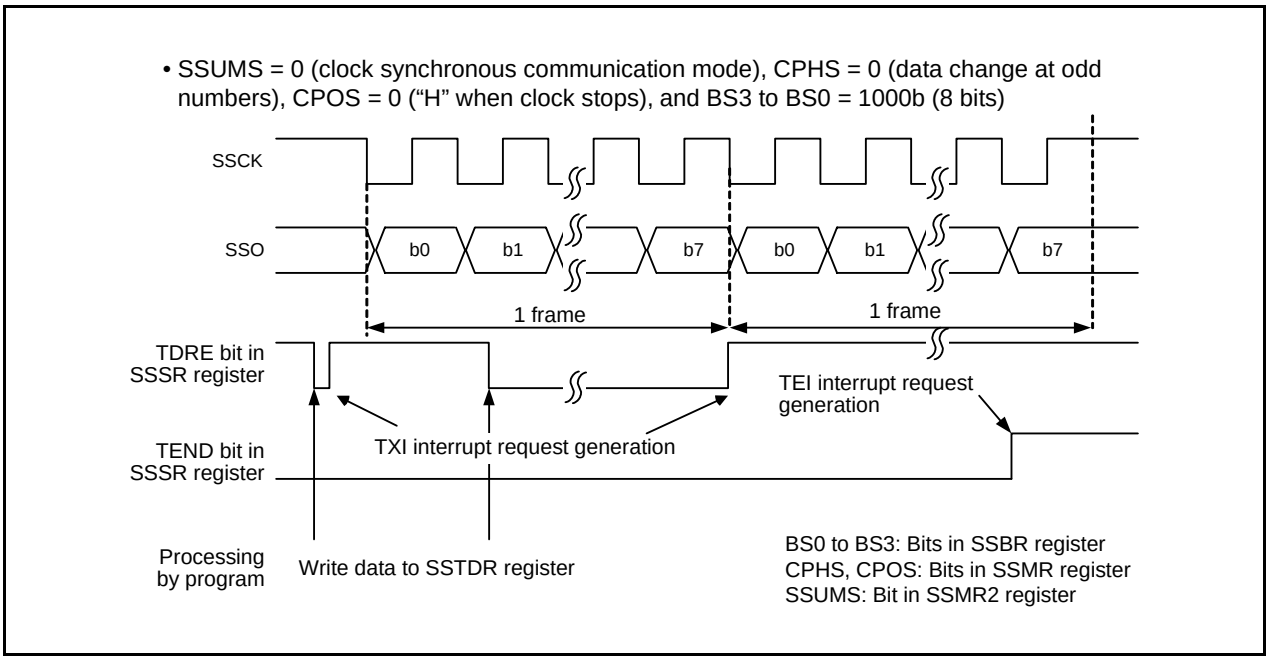


Figure 23.5 Example of Synchronous Serial Communication Unit Operation for Data Transmission (Clock Synchronous Communication Mode, 8-Bit SSU Data Transfer Length)

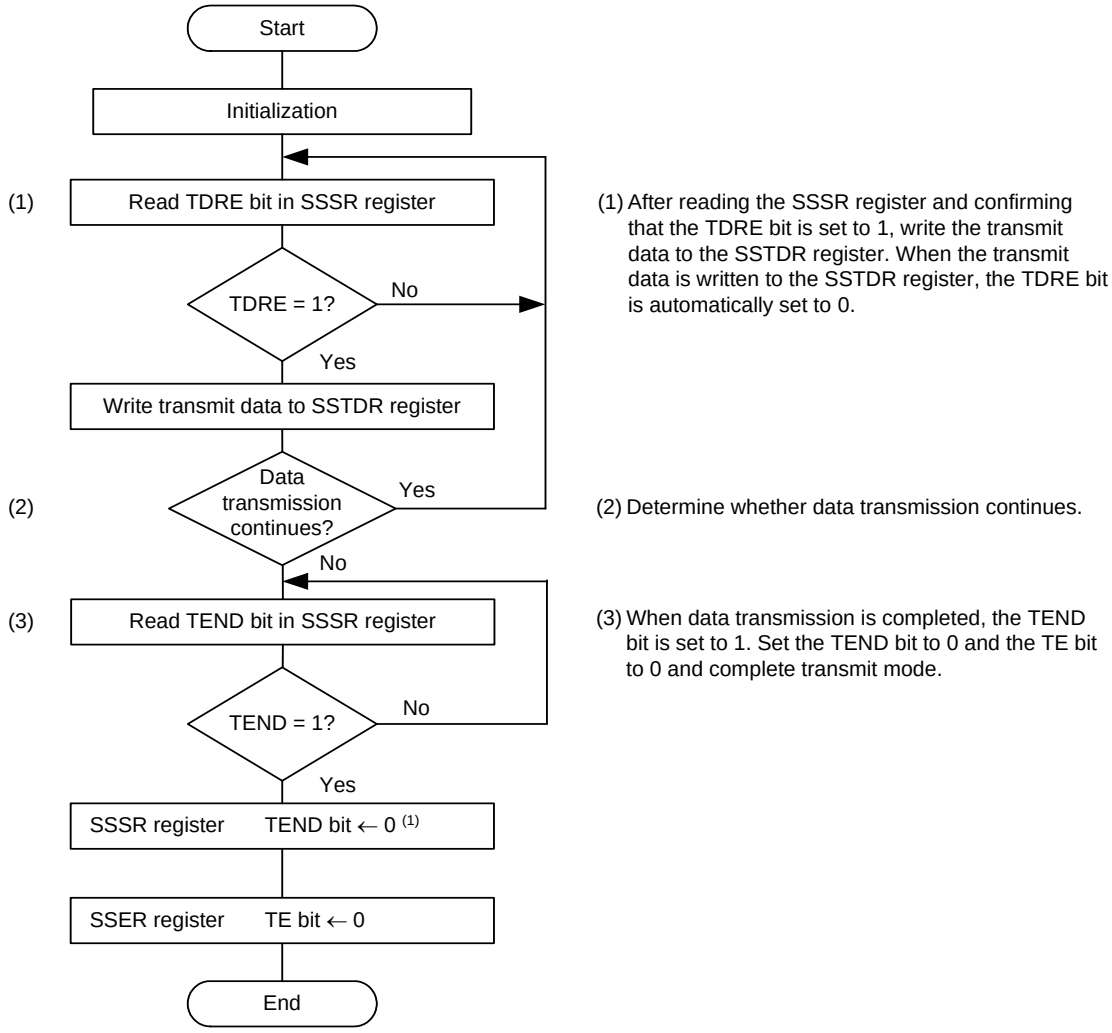


Figure 23.6 Sample Flowchart of Data Transmission (Clock Synchronous Communication Mode)

23.4.3 Data Reception

Figure 23.7 shows an Example of Synchronous Serial Communication Unit Operation for Data Reception (Clock Synchronous Communication Mode, 8-Bit SSU Data Transfer Length). During data reception, synchronous serial communication unit operates as described below. (The data transfer length can be set from 8 to 16 bits using the SSBR register.)

When the synchronous serial communication unit is set as the master device, it outputs a synchronous clock and inputs data. When synchronous serial communication unit is set as a slave device, it inputs data synchronized with the input clock.

When synchronous serial communication unit is set as a master device, it outputs a receive clock and starts receiving by performing dummy read of the SSRDR register.

After 8 bits of data are received, the RDRF bit in the SSSR register is set to 1 (data in the SSRDR register) and receive data is stored in the SSRDR register. When the RIE bit in the SSER register is set to 1 (RXI and OEI interrupt requests enabled), the RXI interrupt request is generated. If the SSDR register is read, the RDRF bit is automatically set to 0 (no data in the SSRDR register).

Read the receive data after setting the RSSTP bit in the SSCRH register to 1 (after receiving 1 byte of data, the receive operation is completed). Synchronous serial communication unit outputs a clock for receiving 8 bits of data and stops. After that, set the RE bit in the SSER register to 0 (receive disabled) and the RSSTP bit to 0 (receive operation is continued after receiving the 1 byte of data) and read the receive data. If the SSRDR register is read while the RE bit is set to 1 (receive enabled), a receive clock is output again.

When the 8th clock rises while the RDRF bit is set to 1, the ORER bit in the SSSR register is set to 1 (overrun error: OEI) and the operation is stopped. When the ORER bit is set to 1, receive cannot be performed. Confirm that the ORER bit is set to 0 before restarting receive.

Figure 23.8 shows a Sample Flowchart of Data Reception (MSS = 1) (Clock Synchronous Communication Mode).

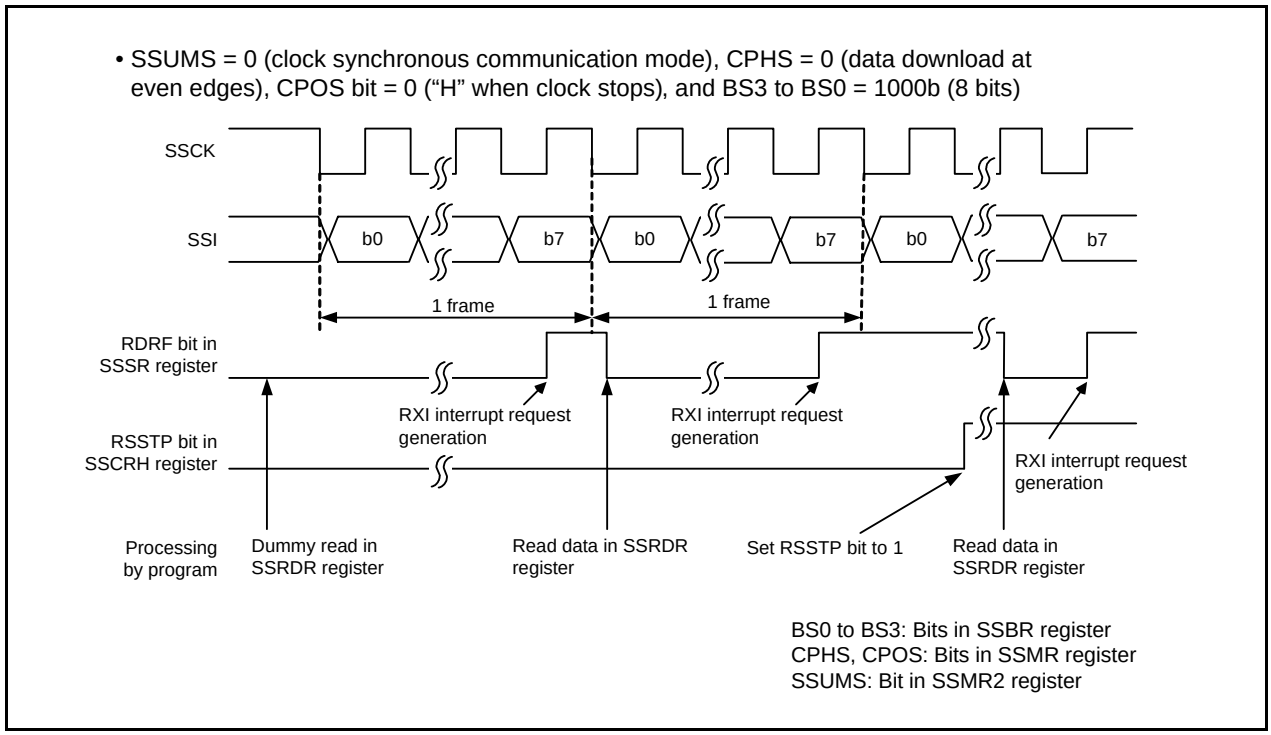


Figure 23.7 Example of Synchronous Serial Communication Unit Operation for Data Reception (Clock Synchronous Communication Mode, 8-Bit SSU Data Transfer Length)

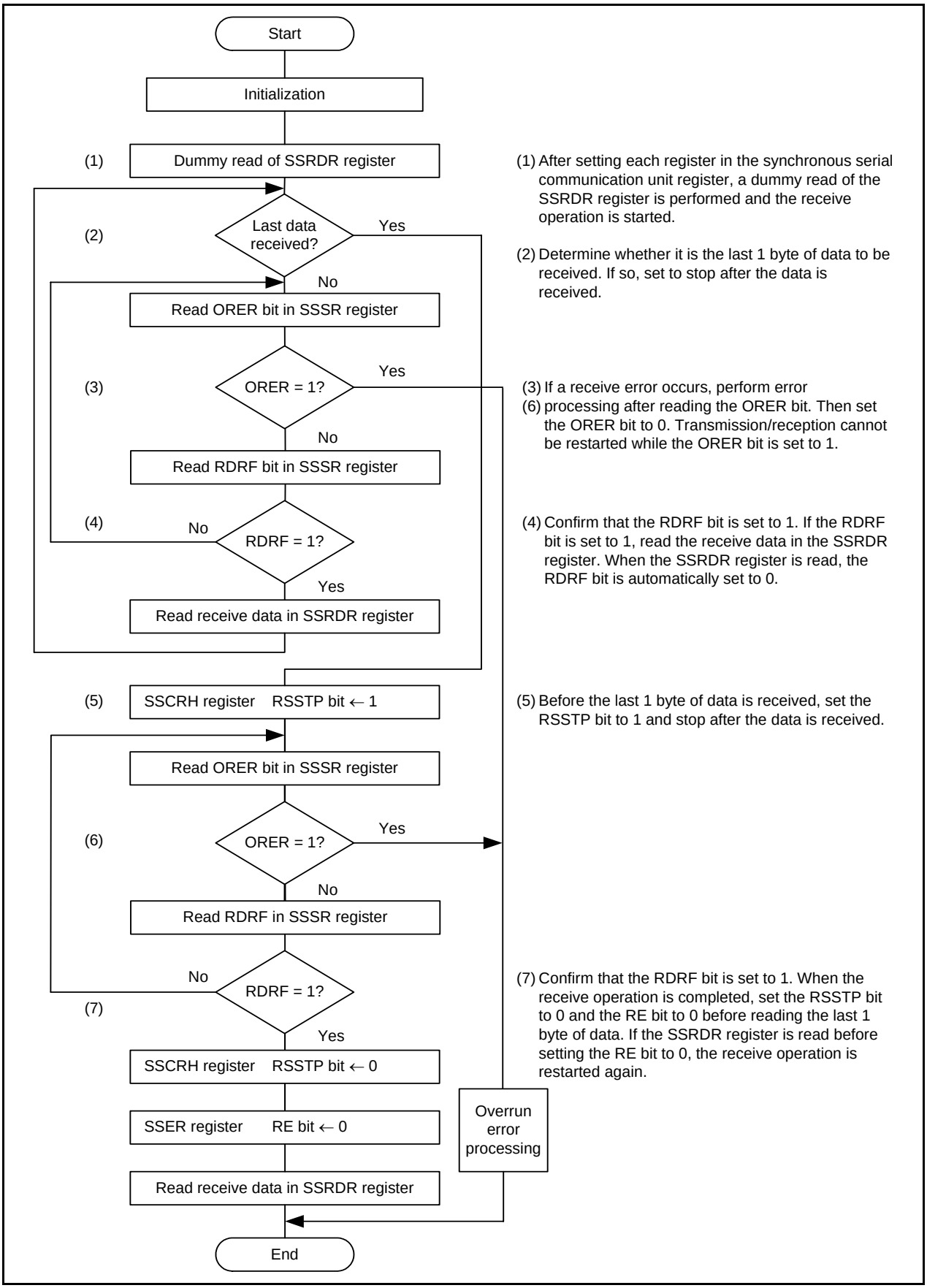


Figure 23.8 Sample Flowchart of Data Reception (MSS = 1) (Clock Synchronous Communication Mode)

23.4.3.1 Data Transmission/Reception

Data transmission/reception is an operation combining data transmission and reception which were described earlier. Transmission/reception is started by writing data to the SSTDR register.
When the last transfer clock (the data transfer length can be set from 8 to 16 bits using the SSBR register) rises or the ORER bit is set to 1 (overrun error) while the TDRE bit is set to 1 (data is transferred from registers SSTDR to SSTRSR), the transmit/receive operation is stopped.
When switching from transmit mode (TE = 1) or receive mode (RE = 1) to transmit/receive mode (TE = RE = 1), set the TE bit to 0 and RE bit to 0 before switching. After confirming that the TEND bit is set to 0 (the TDRE bit is set to 0 when the last bit of the transmit data is transmitted), the RDRF bit is set to 0 (no data in the SSRDR register), and the ORER bit is set to 0 (no overrun error), set bits TE and RE to 1.
Figure 23.9 shows a Sample Flowchart of Data Transmission/Reception (Clock Synchronous Communication Mode).
When exiting transmit/receive mode after this mode is used (TE = RE = 1), a clock may be output if transmit/receive mode is exited after reading the SSRDR register. To avoid any clock outputs, perform either of the following:

- First set the RE bit to 0, and then set the TE bit to 0.
- Set bits TE and RE to 0 at the same time.

When subsequently switching to receive mode (TE = 0 and RE = 1), first set the SRES bit to 1, and set this bit to 0 to reset the SSU control unit and the SSTRSR register. Then, set the RE bit to 1.

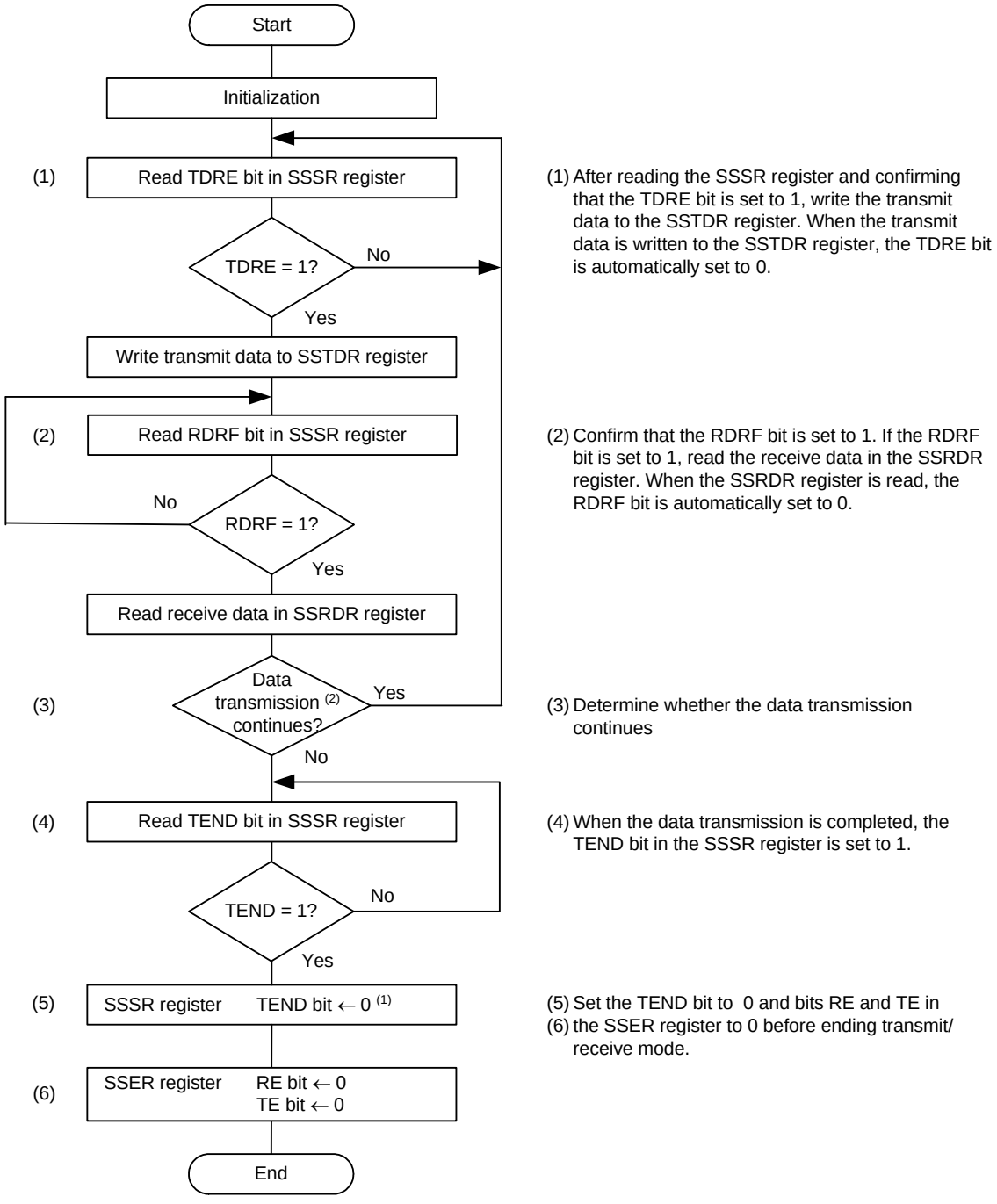


Figure 23.9 Sample Flowchart of Data Transmission/Reception (Clock Synchronous Communication Mode)

23.5 Operation in 4-Wire Bus Communication Mode

In 4-wire bus communication mode, a 4-wire bus consisting of a clock line, a data input line, a data output line, and a chip select line is used for communication. This mode includes bidirectional mode in which the data input line and data output line function as a single pin.

The data input line and output line change according to the settings of the MSS bit in the SSCRH register and the BIDE bit in the SSMR2 register. For details, refer to **23.3.2.1 Association between Data I/O Pins and SS Shift Register**. In this mode, clock polarity, phase, and data settings are performed by bits CPOS and CPHS in the SSMR register. For details, refer to **23.3.1.1 Association between Transfer Clock Polarity, Phase, and Data**.

When this MCU is set as the master device, the chip select line controls output. When synchronous serial communication unit is set as a slave device, the chip select line controls input. When it is set as the master device, the chip select line controls output of the $\overline{\text{SCS}}$ pin or controls output of a general port according to the setting of the CSS1 bit in the SSMR2 register. When the MCU is set as a slave device, the chip select line sets the $\overline{\text{SCS}}$ pin as an input pin by setting bits CSS1 and CSS0 in the SSMR2 register to 01b.

In 4-wire bus communication mode, the MLS bit in the SSMR register is set to 0 and communication is performed MSB-first.

23.5.1 Initialization in 4-Wire Bus Communication Mode

Figure 23.10 shows Initialization in 4-Wire Bus Communication Mode. Before the data transit/receive operation, set the TE bit in the SSER register to 0 (transmit disabled), the RE bit in the SSER register to 0 (receive disabled), and initialize the synchronous serial communication unit.
To change the communication mode or format, set the TE bit to 0 and the RE bit to 0 before making the change. Setting the RE bit to 0 does not change the settings of flags RDRF and ORER or the contents of the SSRDR register.

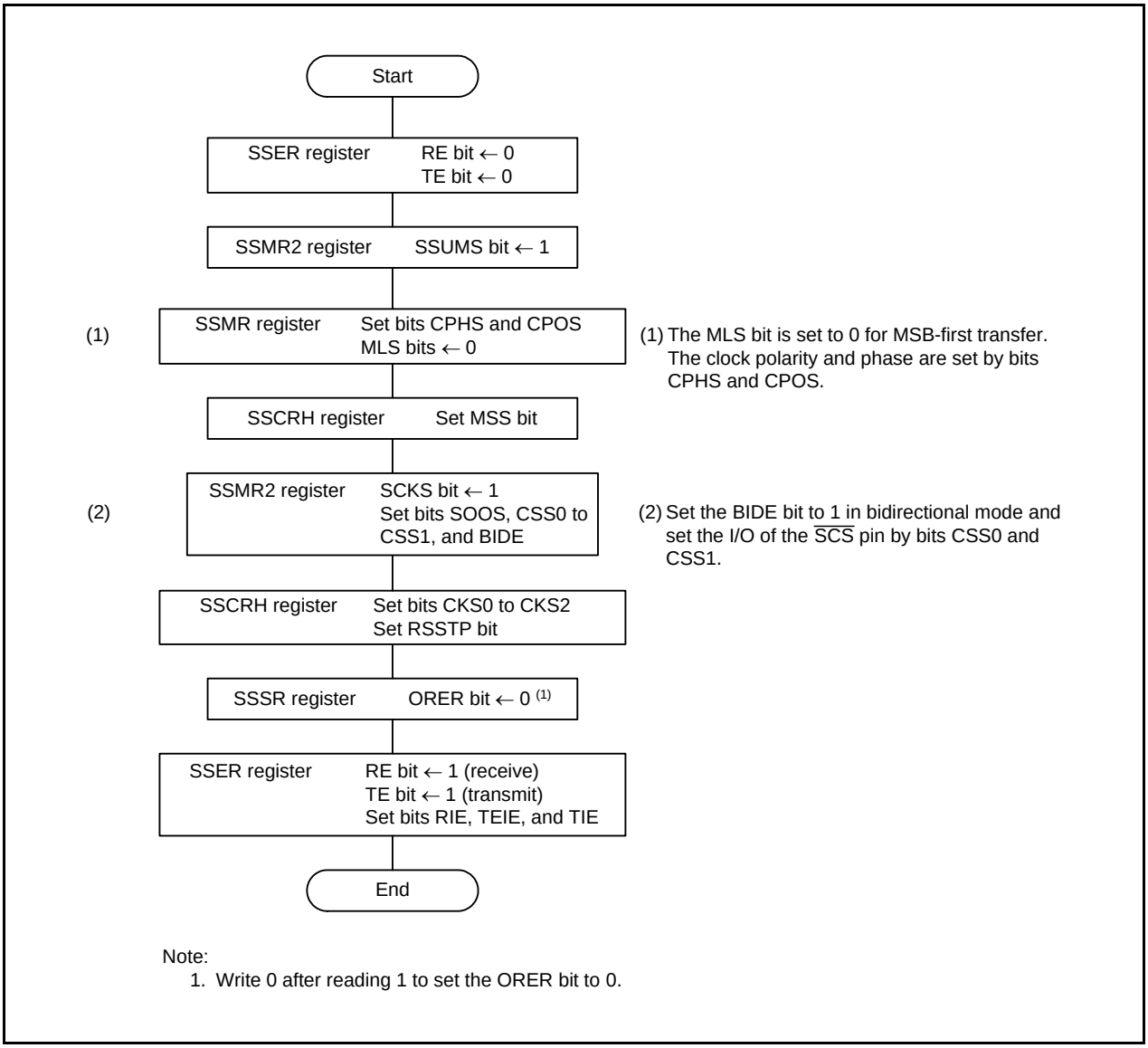


Figure 23.10 Initialization in 4-Wire Bus Communication Mode

23.5.2 Data Transmission

Figure 23.11 shows an Example of Synchronous Serial Communication Unit Operation during Data Transmission (4-Wire Bus Communication Mode, 8-Bit SSU Data Transfer Length). During the data transmit operation, synchronous serial communication unit operates as described below. (The data transfer length can be set from 8 to 16 bits using the SSBR register.)

When the MCU is set as the master device, it outputs a synchronous clock and data. When the MCU is set as a slave device, it outputs data in synchronization with the input clock while the $\overline{SCS}$ pin is "L".

When the transmit data is written to the SSTDR register after setting the TE bit to 1 (transmit enabled), the TDRE bit is automatically set to 0 (data has not been transferred from registers SSTDR to SSTRSR) and the data is transferred from registers SSTDR to SSTRSR. After the TDRE bit is set to 1 (data is transferred from registers SSTDR to SSTRSR), transmission starts. When the TIE bit in the SSER register is set to 1, a TXI interrupt request is generated.

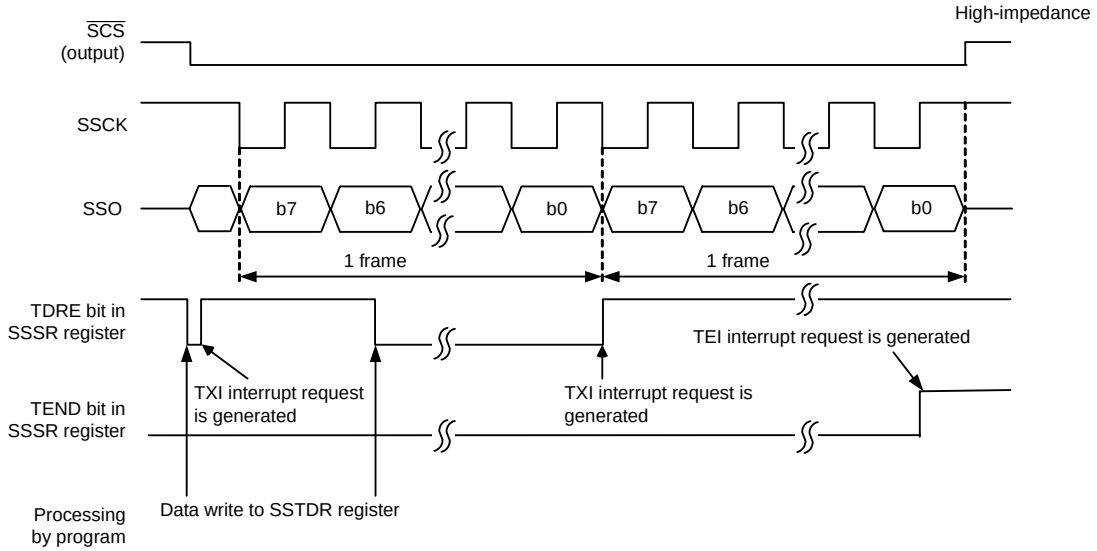
After 1 frame of data is transferred while the TDRE bit is set to 0, the data is transferred from registers SSTDR to SSTRSR and transmission of the next frame is started. If the 8th bit is transmitted while TDRE is set to 1, TEND in the SSSR register is set to 1 (when the last bit of the transmit data is transmitted, the TDRE bit is set to 1) and the state is retained. If the TEIE bit in the SSER register is set to 1 (transmit-end interrupt requests enabled), a TEI interrupt request is generated. The SSCK pin remains "H" after transmit-end and the $\overline{SCS}$ pin is held "H". When transmitting continuously while the $\overline{SCS}$ pin is held "L", write the next transmit data to the SSTDR register before transmitting the 8th bit.

Transmission cannot be performed while the ORER bit in the SSSR register is set to 1 (overrun error). Confirm that the ORER bit is set to 0 before transmission.

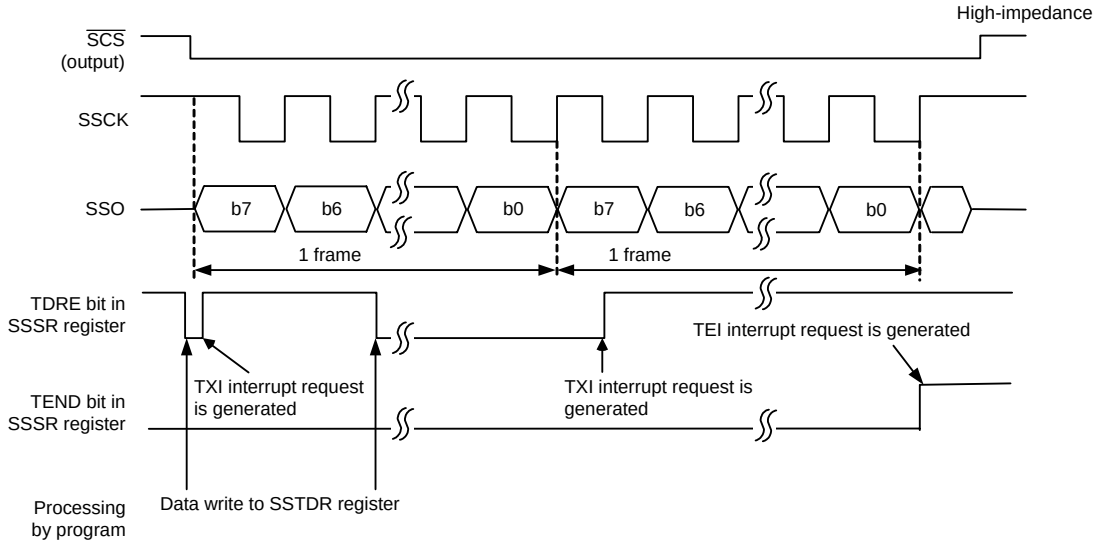
In contrast to the clock synchronous communication mode, the SSO pin is placed in high-impedance state while the $\overline{SCS}$ pin is placed in high-impedance state when operating as a master device and the SSI pin is placed in high-impedance state while the $\overline{SCS}$ pin is placed in "H" input state when operating as a slave device.

The sample flowchart is the same as that for the clock synchronous communication mode (refer to **Figure 23.6 Sample Flowchart of Data Transmission (Clock Synchronous Communication Mode)**).

• CPHS bit = 0 (data change at odd edges), CPOS bit = 0 (“H” when clock stops), and BS3 to BS0 = 1000b (8 bits)



• CPHS bit = 1 (data change at even edges). CPOS bit = 0 (“H” when clock stops), and BS3 to BS0 = 1000b (8 bits)



BS0 to BS3: Bits in SSBR register
CPHS, CPOS: Bits in SSMR register

Figure 23.11 Example of Synchronous Serial Communication Unit Operation during Data Transmission (4-Wire Bus Communication Mode, 8-Bit SSU Data Transfer Length)

23.5.3 Data Reception

Figure 23.12 shows an Example of Synchronous Serial Communication Unit Operation during Data Reception (4-Wire Bus Communication Mode, 8-Bit SSU Data Transfer Length). During data reception, synchronous serial communication unit operates as described below. (The data transfer length can be set from 8 to 16 bits using the SSBR register.)

When the MCU is set as the master device, it outputs a synchronous clock and inputs data. When the MCU is set as a slave device, it outputs data synchronized with the input clock while the $\overline{SCS}$ pin receives “L” input. When the MCU is set as the master device, it outputs a receive clock and starts receiving by performing a dummy read of the SSRDR register.

After 8 bits of data are received, the RDRF bit in the SSSR register is set to 1 (data in the SSRDR register) and receive data is stored in the SSRDR register. When the RIE bit in the SSER register is set to 1 (RXI and OEI interrupt requests enabled), an RXI interrupt request is generated. When the SSRDR register is read, the RDRF bit is automatically set to 0 (no data in the SSRDR register).

Read the receive data after setting the RSSTP bit in the SSCRH register to 1 (after receiving 1-byte data, the receive operation is completed). Synchronous serial communication unit outputs a clock for receiving 8 bits of data and stops. After that, set the RE bit in the SSER register to 0 (receive disabled) and the RSSTP bit to 0 (receive operation is continued after receiving 1-byte data) and read the receive data. When the SSRDR register is read while the RE bit is set to 1 (receive enabled), a receive clock is output again.

When the 8th clock rises while the RDRF bit is set to 1, the ORER bit in the SSSR register is set to 1 (overrun error: OEI) and the operation is stopped. When the ORER bit is set to 1, reception cannot be performed. Confirm that the ORER bit is set to 0 before restarting reception.

The timing with which bits RDRF and ORER are set to 1 varies depending on the setting of the CPHS bit in the SSMR register. Figure 23.12 shows when bits RDRF and ORER are set to 1.

When the CPHS bit is set to 1 (data download at the odd edges), bits RDRF and ORER are set to 1 at some point during the frame.

The sample flowchart is the same as that for the clock synchronous communication mode (refer to **Figure 23.8 Sample Flowchart of Data Reception (MSS = 1) (Clock Synchronous Communication Mode)**).

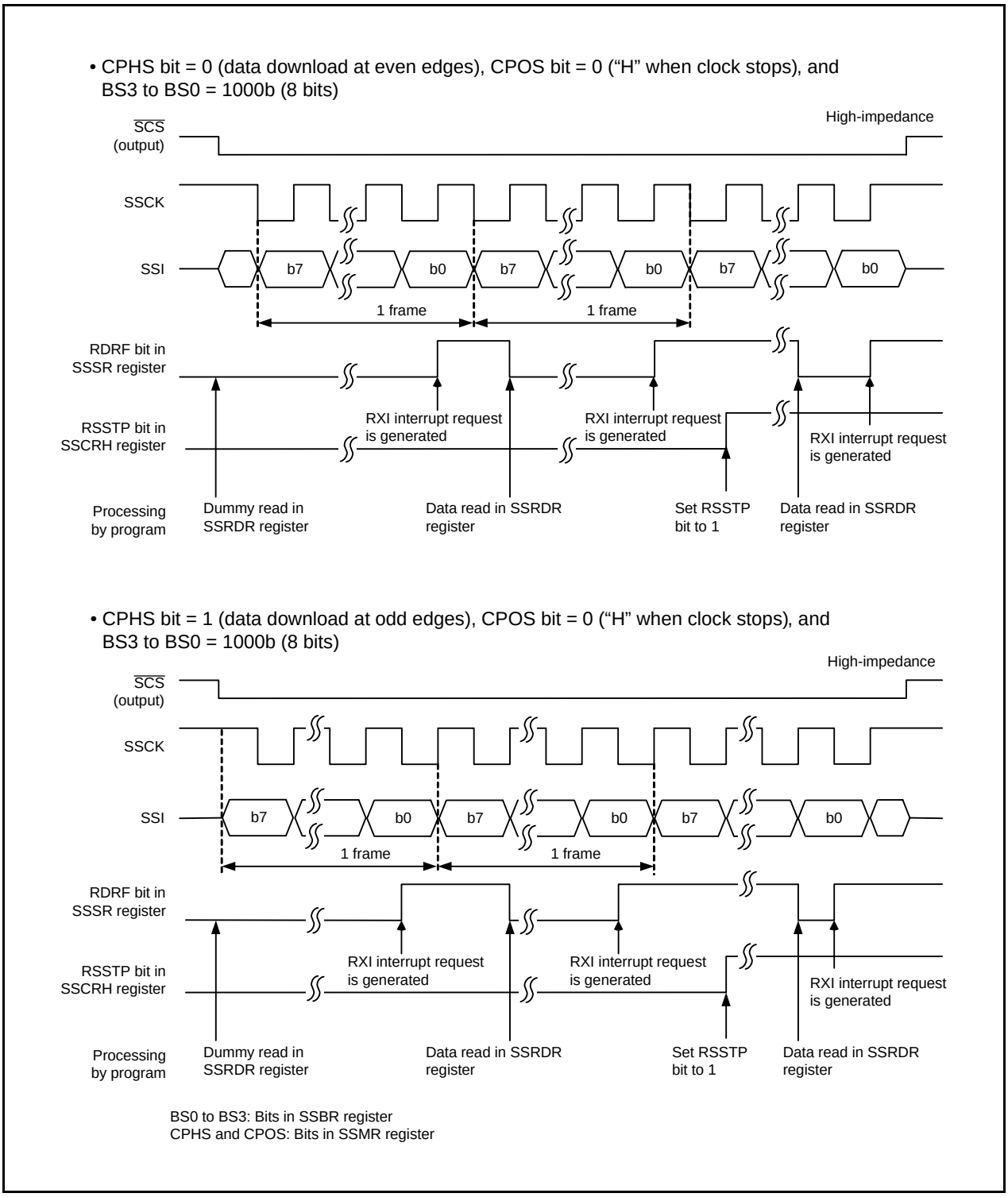


Figure 23.12 Example of Synchronous Serial Communication Unit Operation during Data Reception (4-Wire Bus Communication Mode, 8-Bit SSU Data Transfer Length)

23.5.4 $\overline{\text{SCS}}$ Pin Control and Arbitration

When setting the SSUMS bit in the SSMR2 register to 1 (4-wire bus communication mode) and the CSS1 bit in the SSMR2 register to 1 (functions as $\overline{\text{SCS}}$ output pin), set the MSS bit in the SSCRH register to 1 (operates as the master device) and check the arbitration of the $\overline{\text{SCS}}$ pin before starting serial transfer. If synchronous serial communication unit detects that the synchronized internal $\overline{\text{SCS}}$ signal is held "L" in this period, the CE bit in the SSSR register is set to 1 (conflict error) and the MSS bit is automatically set to 0 (operates as a slave device).
Figure 23.13 shows the Arbitration Check Timing.

Future transmit operations are not performed while the CE bit is set to 1. Set the CE bit to 0 (no conflict error) before starting transmission.

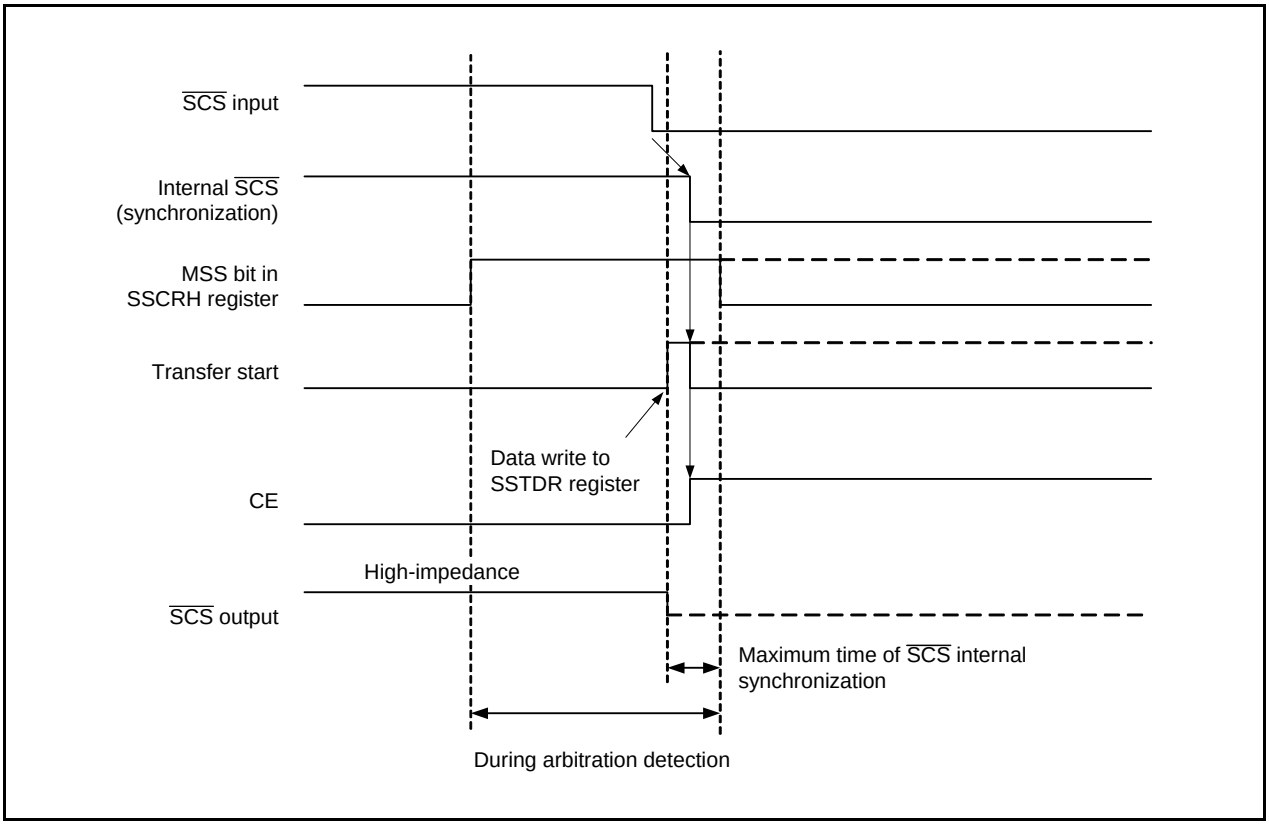


Figure 23.13 Arbitration Check Timing

23.6 Notes on Synchronous Serial Communication Unit

Set the IICSEL bit in the SSUIICSR register to 0 (select SSU function) to use the synchronous serial communication unit function.

24. I2C bus Interface

The I2C bus interface is the circuit that performs serial communication based on the data transfer format of the Philips I2C bus.

24.1 Overview

Table 24.1 lists the I2C bus Interface Specifications, Figure 24.1 shows an I2C bus interface Block Diagram, and Figure 24.2 shows the External Circuit Connection Example of Pins SCL and SDA, Table 24.2 lists the Pin Configuration of I2C bus Interface.

Table 24.1 I2C bus Interface Specifications

Item	Specification
Communication formats	• I2C bus format - Selectable as master/slave device. - Continuous transmit/receive operation (because the shift register, transmit data register, and receive data register are independent.) - Start/stop conditions are automatically generated in master mode. - Automatic loading of the acknowledge bit during transmission - Bit synchronization/wait function (In master mode, the state of the SCL signal is monitored per bit and the timing is synchronized automatically. If the transfer is not possible yet, the SCL signal goes “L” and the interface stands by.) - Support for direct drive of pins SCL and SDA (N-channel open-drain output) • Clock synchronous serial format - Continuous transmit/receive operation (because the shift register, transmit data register, and receive data register are independent.)
I/O pins	SCL (I/O): Serial clock I/O pin SDA (I/O): Serial data I/O pin
Transfer clocks	• When the MST bit in the ICCR1 register is set to 0. External clock (input from the SCL pin) • When the MST bit in the ICCR1 register is set to 1. Internal clock selected by bits CKS0 to CKS3 in the ICCR1 register and bits IICTCTWI and IICTCHALF in the PINSR register (output from the SCL pin)
Receive error detection	• Overrun error detection (clock synchronous serial format) Indicates an overrun error during reception. When the last bit of the next unit of data is received while the RDRF bit in the ICSR register is set to 1 (data in the ICDRR register), the AL bit is set to 1.
Interrupt sources	• I2C bus format ..... 6 sources (1) Transmit data empty (including when slave address matches), end of transmission, receive data full (including when slave address matches), arbitration lost, NACK detection, and stop condition detection • Clock synchronous serial format ..... 4 sources (1) Transmit data empty, end of transmission, receive data full, and overrun error
Selectable functions	• I2C bus format - Selectable output level for the acknowledge signal during reception. • Clock synchronous serial format - MSB-first or LSB-first selectable as the data transfer direction. • SDA digital delay - Digital delay value for the SDA pin selectable by bits SDADLY0 to SDADLY1 in the PINSR register.

Note:
1. All sources use one interrupt vector for I2C bus interface.

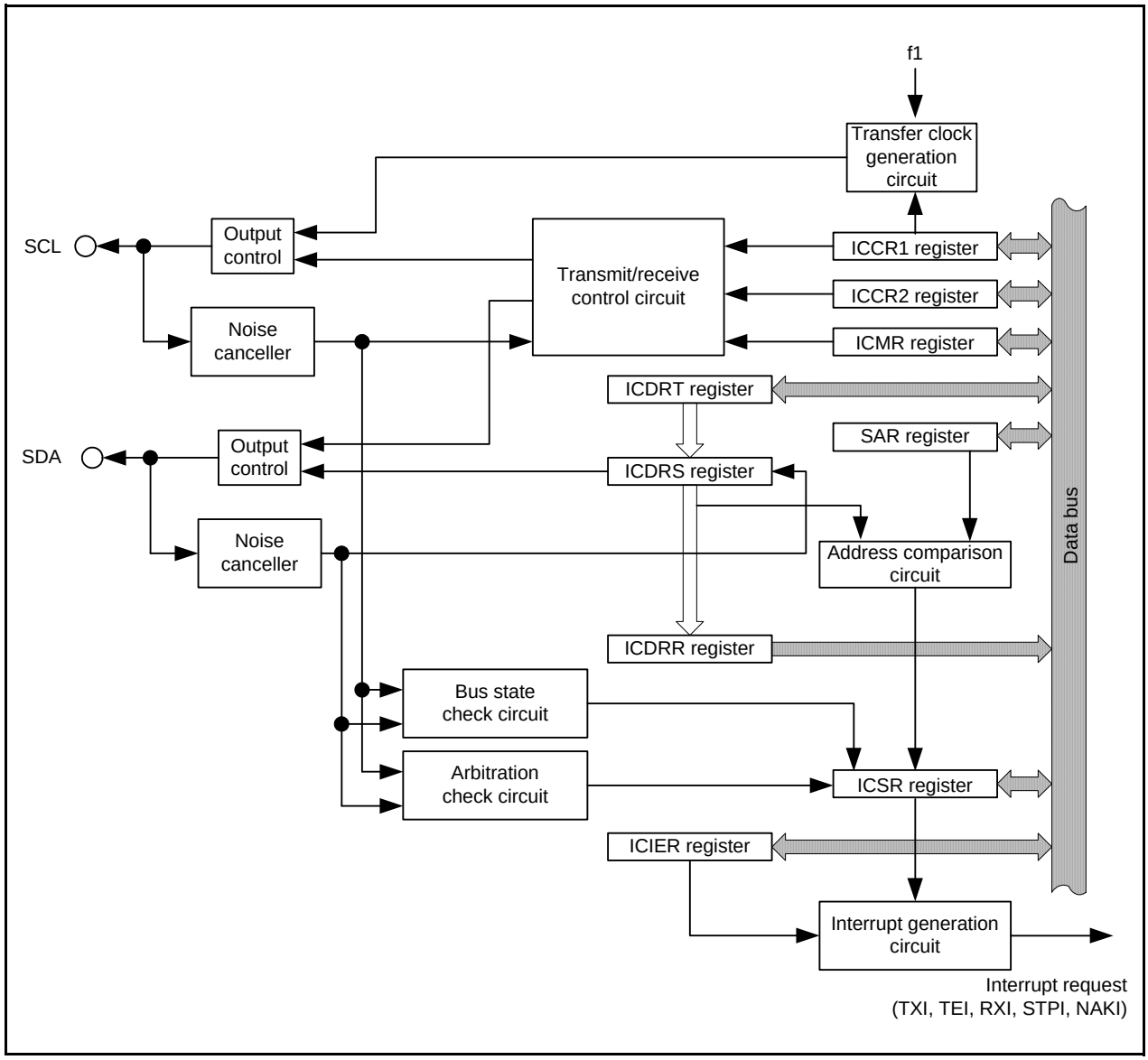


Figure 24.1 I2C bus interface Block Diagram

Table 24.2 Pin Configuration of I2C bus Interface

Pin Name	Assigned Pin	Function
SCL	P3_5	Clock I/O pin
SDA	P3_7	Data I/O pin

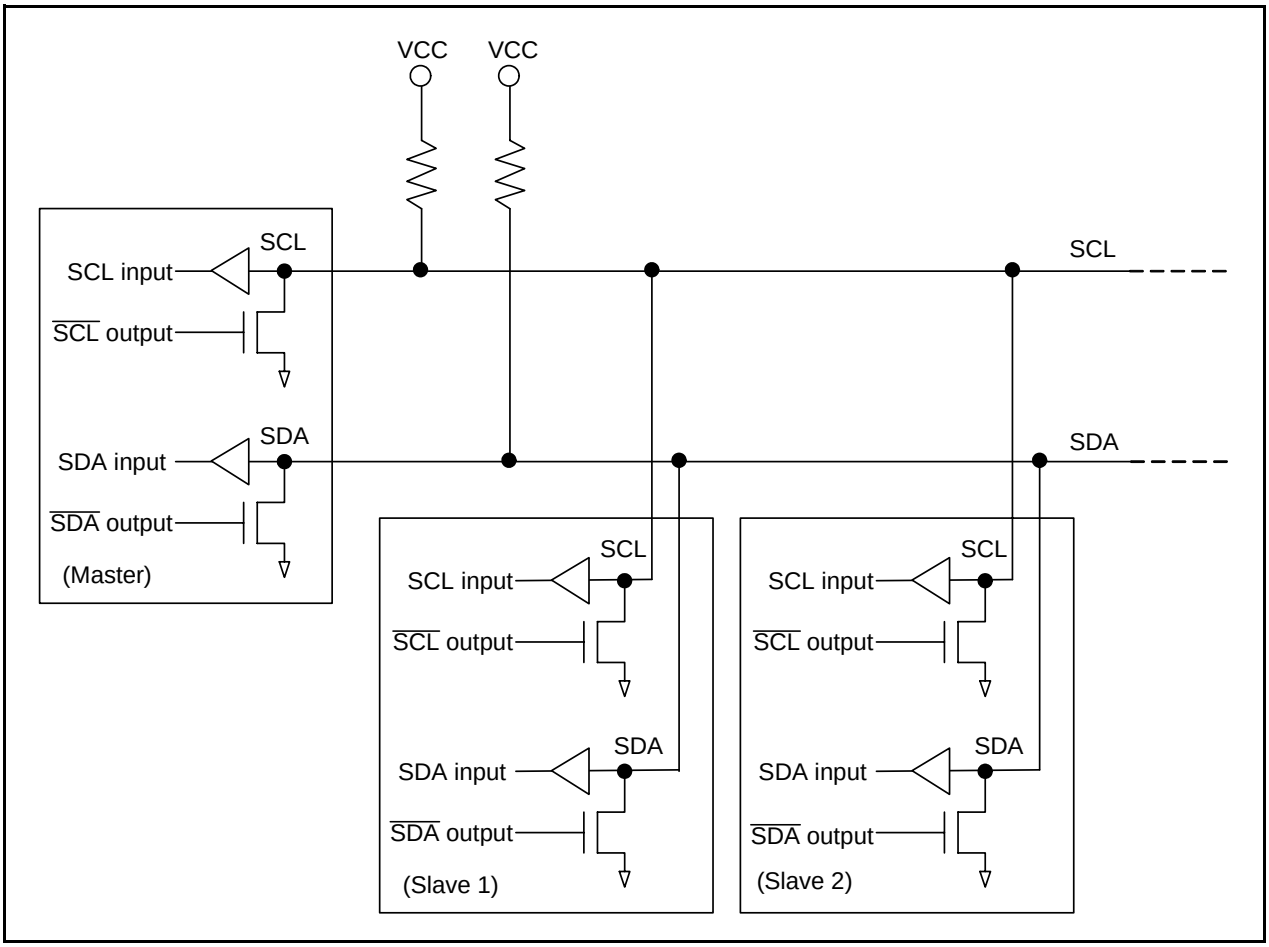


Figure 24.2 External Circuit Connection Example of Pins SCL and SDA

24.2 Registers

24.2.1 Module Standby Control Register (MSTCR)

Address 0008h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	MSTTRC	—	MSTIIC	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	—			
b2	—			
b3	MSTIIC	SSU, I2C bus standby bit	0: Active 1: Standby (1)	R/W
b4	—	Reserved bit	Set to 0.	R/W
b5	MSTTRC	Timer RC standby bit	0: Active 1: Standby (2)	R/W
b6	—	Reserved bit	Set to 0.	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Notes:
1. Stop the SSU and the I2C bus functions before setting to standby. When the MSTIIC bit is set to 1 (standby), any access to the SSU or the I2C bus associated registers (addresses 0193h to 019Dh) is disabled.
2. Stop the timer RC function before setting to standby. When the MSTTRC bit is set to 1 (standby), any access to the timer RC associated registers (addresses 0120h to 0133h (0133h is not available in the R8C/3MU Group)) is disabled.

24.2.2 SSU/IIC Pin Select Register (SSUIICSR)

Address 018Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	IICSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IICSEL	SSU/I2C bus switch bit	0: SSU function selected 1: I2C bus function selected	R/W
b1	—	Reserved bit	Set to 0.	R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	—			
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—			
b7	—			

24.2.3 I/O Function Pin Select Register (PINSR)

Address 018Fh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	SDADLY1	SDADLY0	IICTCHALF	IICTCTWI	IOINSEL	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	IOINSEL	I/O port input function select bit	0: The I/O port input function depends on the PDi (i = 0, 1, 3, 4, 6 to 8) register. When the PDi_j (j = 0 to 7) bit in the PDi register is set to 0 (input mode), the pin input level is read. When the PDi_j bit in the PDi register is set to 1 (output mode), the port latch is read. 1: The I/O port input function reads the pin input level regardless of the PDi register	R/W
b4	IICTCTWI	I2C double transfer rate select bit	0: Transfer rate is the same as the value set with bits CKS0 to CKS3 in the ICCR1 register 1: Transfer rate is twice the value set with bits CKS0 to CKS3 in the ICCR1 register	R/W
b5	IICTCHALF	I2C half transfer rate select bit	0: Transfer rate is the same as the value set with bits CKS0 to CKS3 in the ICCR1 register 1: Transfer rate is half the value set with bits CKS0 to CKS3 in the ICCR1 register	R/W
b6	SDADLY0	SDA digital delay select bit	b7 b6 0 0: Digital delay of 3 × f1 cycles 0 1: Digital delay of 11 × f1 cycles 1 0: Digital delay of 19 × f1 cycles 1 1: Do not set.	R/W
b7	SDADLY1			R/W

IOINSEL Bit (I/O port input function select bit)

The IOINSEL bit is used to select the pin level of an I/O port when the PDi_j (j = 0 to 7) bit in the PDi (i = 0, 1, 3, 4, 6 to 8) register is set to 1 (output mode). When this bit is set to 1, the I/O port input function reads the pin input level regardless of the PDi register.

Table 24.3 lists I/O Port Values Read by Using IOINSEL Bit. The IOINSEL bit can be used to change the input function of all I/O ports.

Table 24.3 I/O Port Values Read by Using IOINSEL Bit

PDi_j bit in PDi register	0 (input mode)		1 (output mode)	
IOINSEL bit	0	1	0	1
I/O port values read	Pin input level		Port latch value	Pin input level

24.2.4 IIC bus Transmit Data Register (ICDRT)

Address 0194h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Function	R/W
b7 to b0	This register stores transmit data. When the ICDRS register is detected as empty, the stored transmit data item is transferred to the ICDRS register and data transmission starts. When the next unit of transmit data is written to the ICDRT register while data is transmitted to the ICDRS register, continuous transmission is enabled. When the MLS bit in the ICMR register is set to 1 (data transfer with LSB-first), the MSB-LSB inverted data is read after the data is written to the ICDRT register.	R/W

24.2.5 IIC bus Receive Data Register (ICDRR)

Address 0196h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Function	R/W
b7 to b0	This register stores receive data. When the ICDRS register receives 1 byte of data, the receive data is transferred to the ICDRR register and the next receive operation is enabled.	R

24.2.6 IIC bus Control Register 1 (ICCR1)

Address 0198h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ICE	RCVD	MST	TRS	CKS3	CKS2	CKS1	CKS0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CKS0	Transmit clock select bits 3 to 0 (1)	b3 b2 b1 b0 0 0 0 0: f1/28 0 0 0 1: f1/40 0 0 1 0: f1/48 0 0 1 1: f1/64 0 1 0 0: f1/80 0 1 0 1: f1/100 0 1 1 0: f1/112 0 1 1 1: f1/128 1 0 0 0: f1/56 1 0 0 1: f1/80 1 0 1 0: f1/96 1 0 1 1: f1/128 1 1 0 0: f1/160 1 1 0 1: f1/200 1 1 1 0: f1/224 1 1 1 1: f1/256	R/W
b1	CKS1			R/W
b2	CKS2			R/W
b3	CKS3			R/W
b4	TRS	Transfer/receive select bit (2, 3, 6)	b5 b4 0 0: Slave Receive Mode (4) 0 1: Slave Transmit Mode 1 0: Master Receive Mode 1 1: Master Transmit Mode	R/W
b5	MST	Master/slave select bit (5, 6)		R/W
b6	RCVD	Receive disable bit	After reading the ICDRR register while the TRS bit is set to 0 0: Next receive operation continues 1: Next receive operation disabled	R/W
b7	ICE	I2C bus interface enable bit (7)	0: This module is halted (Pins SCL and SDA are set to a port function) 1: This module is enabled for transfer operations (Pins SCL and SDA are in a bus drive state)	R/W

Notes:

1. Set according to the necessary transfer rate in master mode. Refer to **Tables 24.4 and 24.5 Transfer Rate Examples** for the transfer rate. This bit is used for maintaining the setup time in transmit mode of slave mode. The time is 10Tcyc when the CKS3 bit is set to 0 and 20Tcyc when the CKS3 bit is set to 1. (1Tcyc = 1/f1(s))
2. Rewrite the TRS bit between transfer frames.
3. When the first 7 bits after the start condition in slave receive mode match the slave address set in the SAR register and the 8th bit is set to 1, the TRS bit is set to 1.
4. In master mode with the I2C bus format, if arbitration is lost, bits MST and TRS are set to 0 and the IIC enters slave receive mode.
5. When an overrun error occurs in master receive mode with the clock synchronous serial format, the MST bit is set to 0 and the I2C bus enters slave receive mode.
6. In multimaster operation, use the MOV instruction to set bits TRS and MST.
7. When writing 0 to the ICE bit or 1 to the IICRST bit in the ICCR2 register during an I2C bus interface operation, the BBSY bit in the ICCR2 register and the STOP bit in the ICSR register may become undefined. Refer to **24.9 Notes on I2C bus Interface**.

24.2.7 IIC bus Control Register 2 (ICCR2)

Address 0199h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	BBSY	SCP	SDAO	SDAOP	SCLO	—	IICRST	—
After Reset	0	1	1	1	1	1	0	1

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b1	IICRST	I2C bus control block reset bit (5)	When hang-up occurs due to communication failure during I2C bus interface operation, writing 1 resets the control block of the I2C bus interface without setting ports or initializing registers.	R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b3	SCLO	SCL monitor flag	0: SCL pin is set to “L” 1: SCL pin is set to “H”	R
b4	SDAOP	SDAO write protect bit	When rewriting the SDAO bit, write 0 simultaneously. (1) When read, the content is 1.	R/W
b5	SDAO	SDA output value control bit	When read 0: SDA pin output is held “L” 1: SDA pin output is held “H” When written (1, 2) 0: SDA pin output is changed to “L” 1: SDA pin output is changed to high-impedance (“H” output via external pull-up resistor)	R/W
b6	SCP	Start/stop condition generation disable bit	When writing to the to BBSY bit, write 0 simultaneously. (3) When read, the content is 1. Writing 1 is invalid.	R/W
b7	BBSY	Bus busy bit (4, 5)	When read: 0: Bus is released (SDA signal changes from “L” to “H” while SCL signal is held “H”) 1: Bus is occupied (SDA signal changes from “H” to “L” while SCL signal is held “H”) When written (3): 0: Stop condition generated 1: Start condition generated	R/W

Notes:
1. When rewriting the SDAO bit, write 0 to the SDAOP bit simultaneously using the MOV instruction.
2. Do not write to the SDAO bit during a transfer operation.
3. Enabled in master mode. When writing to the BBSY bit, write 0 to the SCP bit simultaneously using the MOV instruction. Execute the same way when a start condition is regenerated.
4. Disabled when the clock synchronous serial format is used.
5. When writing 0 to the ICE bit in the ICCR1 register or 1 to the IICRST bit during an I2C bus interface operation, the BBSY bit and the STOP bit in the ICSR register may become undefined. Refer to **24.9 Notes on I2C bus Interface**.

24.2.8 IIC bus Mode Register (ICMR)

Address 019Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	MLS	WAIT	—	—	BCWP	BC2	BC1	BC0
After Reset	0	0	0	1	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	BC0	Bit counters 2 to 0	I2C bus format (Read: Number of remaining transfer bits; Write: Number of next transfer data bits) (1, 2) b2 b1 b0 0 0 0: 9 bits (3) 0 0 1: 2 bits 0 1 0: 3 bits 0 1 1: 4 bits 1 0 0: 5 bits 1 0 1: 6 bits 1 1 0: 7 bits 1 1 1: 8 bits Clock synchronous serial format (Read: Number of remaining transfer bits; Write: Always 000b) b2 b1 b0 0 0 0: 8 bits 0 0 1: 1 bit 0 1 0: 2 bits 0 1 1: 3 bits 1 0 0: 4 bits 1 0 1: 5 bits 1 1 0: 6 bits 1 1 1: 7 bits	R/W
b1	BC1			R/W
b2	BC2			R/W
b3	BCWP	BC write protect bit	When rewriting bits BC0 to BC2, write 0 simultaneously. (2, 4) When read, the content is 1.	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b5	—	Reserved bit	Set to 0.	R/W
b6	WAIT	Wait insertion bit (5)	0: No wait states (Data and the acknowledge bit are transferred consecutively) 1: Wait state (After the clock of the last data bit falls, a “L” period is extended for two transfer clocks)	R/W
b7	MLS	MSB-first/LSB-first select bit	0: Data transfer with MSB-first (6) 1: Data transfer with LSB-first	R/W

Notes:
1. Rewrite between transfer frames. When writing values other than 000b, write when the SCL signal is “L”.
2. When writing to bits BC0 to BC2, write 0 to the BCWP bit simultaneously using the MOV instruction.
3. After data including the acknowledge bit is transferred, these bits are automatically set to 000b. When a start condition is detected, these bits are automatically set to 000b.
4. Do not rewrite when the clock synchronous serial format is used.
5. The setting value is valid in master mode with the I2C bus format. It is invalid in slave mode with the I2C bus format or when the clock synchronous serial format is used.
6. Set to 0 when the I2C bus format is used.

24.2.9 IIC bus Interrupt Enable Register (ICIER)

Address 019Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIE	TEIE	RIE	NAKIE	STIE	ACKE	ACKBR	ACKBT
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ACKBT	Transmit acknowledge select bit	0: In receive mode, 0 is transmitted as the acknowledge bit. 1: In receive mode, 1 is transmitted as the acknowledge bit.	R/W
b1	ACKBR	Receive acknowledge bit	0: In transmit mode, the acknowledge bit received from receive device is set to 0. 1: In transmit mode, the acknowledge bit received from receive device is set to 1.	R
b2	ACKE	Acknowledge bit detection select bit	0: Content of the receive acknowledge bit is ignored and continuous transfer is performed. 1: When the receive acknowledge bit is set to 1, continuous transfer is halted.	R/W
b3	STIE	Stop condition detection interrupt enable bit	0: Stop condition detection interrupt request disabled 1: Stop condition detection interrupt request enabled (2)	R/W
b4	NAKIE	NACK receive interrupt enable bit	0: NACK receive interrupt request and arbitration lost/overrun error interrupt request disabled 1: NACK receive interrupt request and arbitration lost/overrun error interrupt request (1)	R/W
b5	RIE	Receive interrupt enable bit	0: Receive data full and overrun error interrupt request disabled 1: Receive data full and overrun error interrupt request enabled (1)	R/W
b6	TEIE	Transmit end interrupt enable bit	0: Transmit end interrupt request disabled 1: Transmit end interrupt request enabled	R/W
b7	TIE	Transmit interrupt enable bit	0: Transmit data empty interrupt request disabled 1: Transmit data empty interrupt request enabled	R/W

Notes:
1. An overrun error interrupt request is generated when the clock synchronous format is used.
2. Set the STIE bit to 1 (stop condition detection interrupt request enabled) when the STOP bit in the ICSR register is set to 0.

24.2.10 IIC bus Status Register (ICSR)

Address 019Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TDRE	TEND	RDRF	NACKF	STOP	AL	AAS	ADZ
After Reset	0	0	0	0	X	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ADZ	General call address recognition flag (1, 2)	This flag is set to 1 when a general call address is detected.	R/W
b1	AAS	Slave address recognition flag (1)	This flag is set to 1 when the first frame immediately after the start condition matches bits SVA0 to SVA6 in the SAR register in slave receive mode (slave address detection and general call address detection)	R/W
b2	AL	Arbitration lost flag/overrun error flag (1)	I2C bus format: This flag indicates that arbitration has been lost in master mode. This flag is set to 1 (3) when: • The internal SDA signal and SDA pin level do not match at the rising edge of the SCL signal in master transmit mode • The SDA pin is held “H” at start condition detection in master transmit/receive mode Clock synchronous format: This flag indicates an overrun error. This flag is set to 1 when: • The last bit of the next unit of data is received while the RDRF bit is set to 1	R/W
b3	STOP	Stop condition detection flag (1, 7)	This flag is set to 1 when a stop condition is detected after the frame is transferred.	R/W
b4	NACKF	No acknowledge detection flag (1, 4)	This flag is set to 1 when no ACKnowledge is detected from the receive device after transmission.	R/W
b5	RDRF	Receive data register full flag (1, 5)	This flag is set to 1 when receive data is transferred from registers ICDRS to ICDRR.	R/W
b6	TEND	Transmit end flag (1, 6)	I2C bus format: This flag is set to 1 at the rising edge of the 9th clock cycle of the SCL signal while the TDRE bit is set to 1. Clock synchronous format: This flag is set to 1 when the last bit of the transmit frame is transmitted.	R/W
b7	TDRE	Transmit data empty flag (1, 6)	This flag is set to 1 when: • Data is transferred from registers ICDRT to ICDRS and the CDRT register is empty • The TRS bit in the ICCR1 register is set to 1 (transmit mode) • A start condition is generated (including retransmission) • Slave receive mode is changed to slave transmit mode	R/W

Notes:
1. Each bit is set to 0 by reading 1 before writing 0.
2. This flag is enabled in slave receive mode with the I2C bus format.
3. When two or more master devices attempt to occupy the bus at nearly the same time, if the I2C bus Interface monitors the SDA pin and the data which the I2C bus Interface transmits is different, the AL flag is set to 1 and the bus is occupied by another master.
4. The NACKF bit is enabled when the ACKE bit in the ICIER register is set to 1 (when the receive acknowledge bit is set to 1, transfer is halted).
5. The RDRF bit is set to 0 when data is read from the ICDRR register.
6. Bits TEND and TDRE are set to 0 when data is written to the ICDRT register.
   When reading these bits immediately after writing to the ICDRT register, insert three or more NOP instructions between the instructions used for writing and reading.
7. When writing 0 to the ICE bit in the ICCR1 register or 1 to the IICRST bit in the ICCR2 register during an I2C bus interface operation, the BBSY bit in the ICCR2 register and the STOP bit may become undefined. Refer to **24.9 Notes on I2C bus Interface**.

When accessing the ICSR register continuously, insert one or more NOP instructions between the instructions to access it.

24.2.11 Slave Address Register (SAR)

Address 019Dh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	SVA6	SVA5	SVA4	SVA3	SVA2	SVA1	SVA0	FS
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	FS	Format select bit	0: I2C bus format 1: Clock synchronous serial format	R/W
b1	SVA0	Slave addresses 6 to 0	Set an address different from that of the other slave devices connected to the I2C bus. When the 7 high-order bits of the first frame transmitted after the start condition match bits SVA0 to SVA6 in slave mode of the I2C bus format, the MCU operates as a slave device.	R/W
b2	SVA1			R/W
b3	SVA2			R/W
b4	SVA3			R/W
b5	SVA4			R/W
b6	SVA5			R/W
b7	SVA6			R/W

24.2.12 IIC bus Shift Register (ICDRS)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—

Bit	Function	R/W
b7 to b0	This register transmits and receives data. During transmission, data is transferred from registers ICRDT to ICDRS and transmitted from the SDA pin. During reception, data is transferred from registers ICDRS to the ICDRR after 1 byte of data reception ends.	—

24.3 Common Items for Multiple Modes

24.3.1 Transfer Clock

When the MST bit in the ICCR1 register is set to 0, the transfer clock is the external clock input from the SCL pin.

When the MST bit in the ICCR1 register is set to 1, the transfer clock is the internal clock selected by bits CKS0 to CKS3 in the ICCR1 register and bits IICTCTWI and IICTCHALF in the PINSR register and the transfer clock is output from the SCL pin. Tables 24.4 and 24.5 list the Transfer Rate Examples.

Table 24.4 Transfer Rate Examples (1)

PINSR Register		ICCR1 Register				Transfer Clock	Transfer Rate				
IICTCHALF	IICTCTWI	CKS3	CKS2	CKS1	CKS0		f1 = 5 MHz	f1 = 8 MHz	f1 = 10 MHz	f1 = 16 MHz	f1 = 20 MHz
0	0	0	0	0	0	f1/28	179 kHz	286 kHz	357 kHz	571 kHz	714 kHz
					1	f1/40	125 kHz	200 kHz	250 kHz	400 kHz	500 kHz
				1	0	f1/48	104 kHz	167 kHz	208 kHz	333 kHz	417 kHz
					1	f1/64	78.1 kHz	125 kHz	156 kHz	250 kHz	313 kHz
			1	0	0	f1/80	62.5 kHz	100 kHz	125 kHz	200 kHz	250 kHz
					1	f1/100	50.0 kHz	80.0 kHz	100 kHz	160 kHz	200 kHz
				1	0	f1/112	44.6 kHz	71.4 kHz	89.3 kHz	143 kHz	179 kHz
					1	f1/128	39.1 kHz	62.5 kHz	78.1 kHz	125 kHz	156 kHz
		1	0	0	0	f1/56	89.3 kHz	143 kHz	179 kHz	286 kHz	357 kHz
					1	f1/80	62.5 kHz	100 kHz	125 kHz	200 kHz	250 kHz
				1	0	f1/96	52.1 kHz	83.3 kHz	104 kHz	167 kHz	208 kHz
					1	f1/128	39.1 kHz	62.5 kHz	78.1 kHz	125 kHz	156 kHz
			1	0	0	f1/160	31.3 kHz	50.0 kHz	62.5 kHz	100 kHz	125 kHz
					1	f1/200	25.0 kHz	40.0 kHz	50.0 kHz	80.0 kHz	100 kHz
				1	0	f1/224	22.3 kHz	35.7 kHz	44.6 kHz	71.4 kHz	89.3 kHz
					1	f1/256	19.5 kHz	31.3 kHz	39.1 kHz	62.5 kHz	78.1 kHz

Table 24.5 Transfer Rate Examples (2)

PINSR Register		ICCR1 Register				Transfer Clock	Transfer Rate				
IICTCHALF	IICTCTWI	CKS3	CKS2	CKS1	CKS0		f1 = 5 MHz	f1 = 8 MHz	f1 = 10 MHz	f1 = 16 MHz	f1 = 20 MHz
0	1	0	0	0	0	f1/28	358 kHz	572 kHz	714 kHz	1142 kHz	1428 kHz
					1	f1/40	250 kHz	400 kHz	500 kHz	800 kHz	1000 kHz
				1	0	f1/48	208 kHz	334 kHz	416 kHz	666 kHz	834 kHz
					1	f1/64	156 kHz	250 kHz	312 kHz	500 kHz	626 kHz
			1	0	0	f1/80	125 kHz	200 kHz	250 kHz	400 kHz	500 kHz
					1	f1/100	100 kHz	160 kHz	200 kHz	320 kHz	400 kHz
				1	0	f1/112	89 kHz	143 kHz	179 kHz	286 kHz	358 kHz
					1	f1/128	78 kHz	125 kHz	156 kHz	250 kHz	312 kHz
		1	0	0	0	f1/56	179 kHz	286 kHz	358 kHz	572 kHz	714 kHz
					1	f1/80	125 kHz	200 kHz	250 kHz	400 kHz	500 kHz
				1	0	f1/96	104 kHz	167 kHz	208 kHz	334 kHz	416 kHz
					1	f1/128	78 kHz	125 kHz	156 kHz	250 kHz	312 kHz
			1	0	0	f1/160	63 kHz	100 kHz	125 kHz	200 kHz	250 kHz
					1	f1/200	50 kHz	80 kHz	100 kHz	160 kHz	200 kHz
				1	0	f1/224	45 kHz	71 kHz	89 kHz	143 kHz	179 kHz
					1	f1/256	39 kHz	63 kHz	78 kHz	125 kHz	156 kHz
1	0	0	0	0	0	f1/28	90 kHz	143 kHz	179 kHz	286 kHz	357 kHz
					1	f1/40	63 kHz	100 kHz	125 kHz	200 kHz	250 kHz
				1	0	f1/48	52 kHz	84 kHz	104 kHz	167 kHz	209 kHz
					1	f1/64	39 kHz	63 kHz	78 kHz	125 kHz	157 kHz
			1	0	0	f1/80	31 kHz	50 kHz	63 kHz	100 kHz	125 kHz
					1	f1/100	25 kHz	40 kHz	50 kHz	80 kHz	100 kHz
				1	0	f1/112	22 kHz	36 kHz	45 kHz	72 kHz	90 kHz
					1	f1/128	20 kHz	31 kHz	39 kHz	63 kHz	78 kHz
		1	0	0	0	f1/56	45 kHz	72 kHz	90 kHz	143 kHz	179 kHz
					1	f1/80	31 kHz	50 kHz	63 kHz	100 kHz	125 kHz
				1	0	f1/96	26 kHz	42 kHz	52 kHz	84 kHz	104 kHz
					1	f1/128	20 kHz	31 kHz	39 kHz	63 kHz	78 kHz
			1	0	0	f1/160	16 kHz	25 kHz	31 kHz	50 kHz	63 kHz
					1	f1/200	13 kHz	20 kHz	25 kHz	40 kHz	50 kHz
				1	0	f1/224	11 kHz	18 kHz	22 kHz	36 kHz	45 kHz
					1	f1/256	10 kHz	16 kHz	20 kHz	31 kHz	39 kHz

24.3.2 SDA Pin Digital Delay Selection

The digital delay value for the SDA pin can be selected by bits SDADLY0 to SDADLY1 in the PINSR register. Figure 24.3 shows the Operating Example of Digital Delay for SDA Pin.

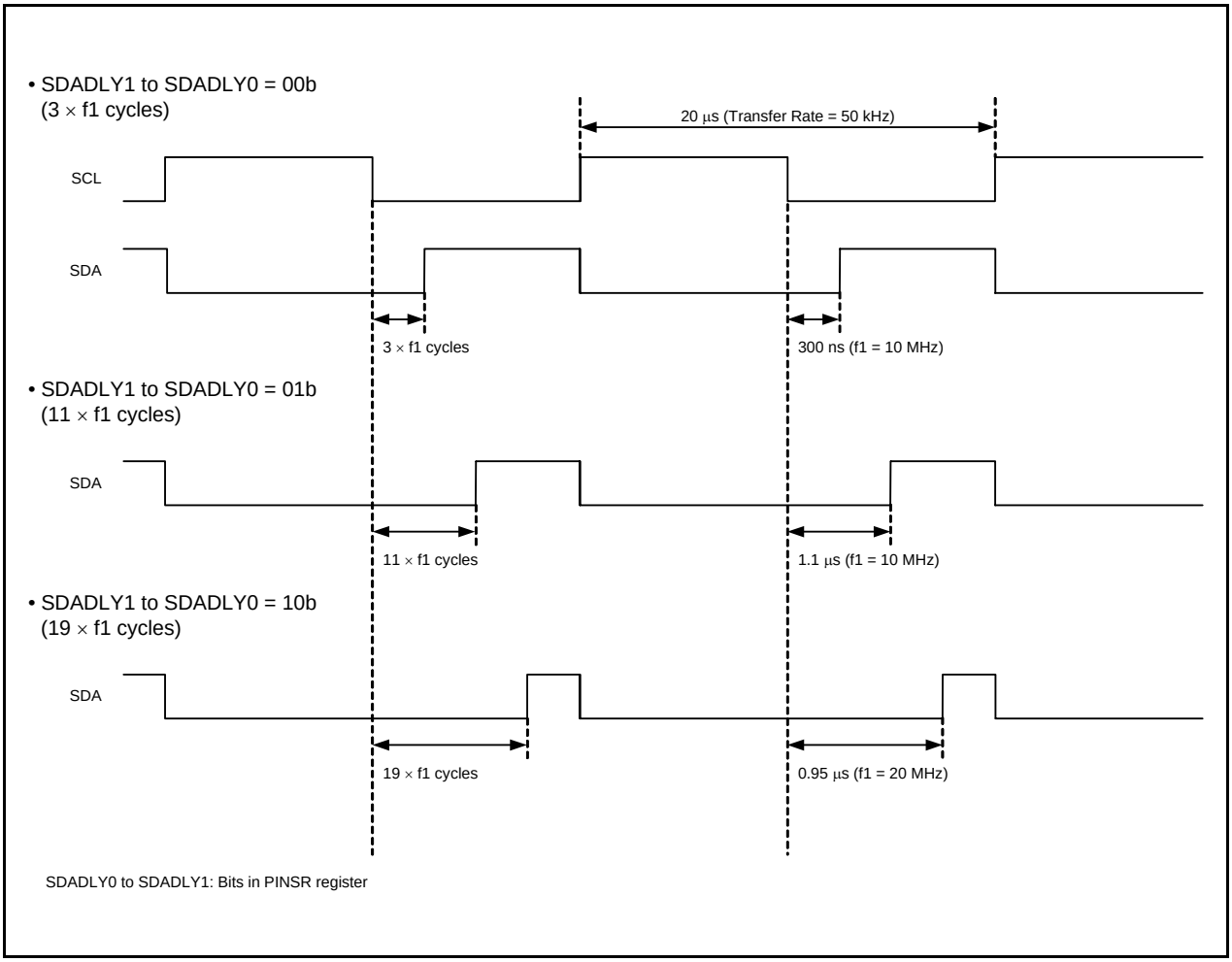


Figure 24.3 Operating Example of Digital Delay for SDA Pin

24.3.3 Interrupt Requests

The I2C bus interface has six interrupt requests when the I2C bus format is used and four interrupt requests when the clock synchronous serial format is used. Table 24.6 lists the Interrupt Requests of I2C bus Interface. Because these interrupt requests are allocated at the I2C bus interface interrupt vector table, the source must be determined bit by bit.

Table 24.6 Interrupt Requests of I2C bus Interface

Interrupt Request		Generation Condition	Format	
			I2C bus	Clock Synchronous Serial
Transmit data empty	TXI	TIE = 1 and TDRE = 1	Enabled	Enabled
Transmit ends	TEI	TEIE = 1 and TEND = 1	Enabled	Enabled
Receive data full	RXI	RIE = 1 and RDRF = 1	Enabled	Enabled
Stop condition detection	STPI	STIE = 1 and STOP = 1	Enabled	Disabled
NACK detection	NAKI	NAKIE = 1 and AL = 1 (or NAKIE = 1 and NACKF = 1)	Enabled	Disabled
Arbitration lost/overrun error			Enabled	Enabled

STIE, NAKIE, RIE, TEIE, TIE: Bits in ICIER register
AL, STOP, NACKF, RDRF, TEND, TDRE: Bits in ICSR register

When generation conditions listed in Table 24.6 are met, an I2C bus interface interrupt request is generated. Set the interrupt generation conditions to 0 by the I2C bus interface interrupt routine.
Note that bits TDRE and TEND are automatically set to 0 by writing transmit data to the ICDRT register and that the RDRF bit is automatically set to 0 by reading the ICDRR register. Especially, the TDRE bit is set to 0 when writing transmit data to the ICDRT register and set to 1 when transferring data from the ICDRT register to the ICDRS register. If the TDRE bit is further set to 0, additional 1 byte may be transmitted.
Also, set the STIE bit to 1 (stop condition detection interrupt request enabled) when the STOP bit is set to 0.

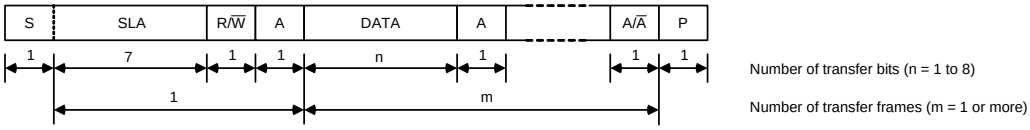
24.4 I2C bus Interface Mode

24.4.1 I2C bus Format

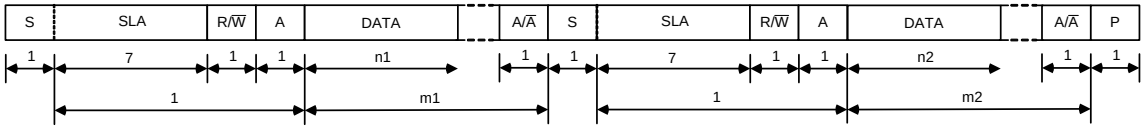
When the FS bit in the SAR register is set to 0, the I2C bus format is used for communication.
Figure 24.4 shows the I2C bus Format and Bus Timing. The first frame following the start condition consists of 8 bits.

(1) I2C bus format

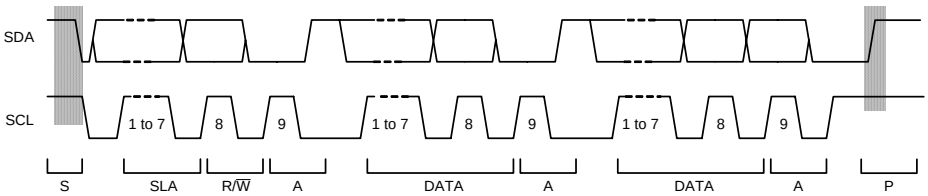
(a) I2C bus format (FS = 0)



(b) I2C bus format When Start Condition is Retransmitted (FS = 0)



(2) I2C bus timing



Legend:
S : Start condition
The master device changes the SDA signal from “H” to “L” while the SCL signal is held “H”.
SLA : Slave address
R/W : Indicates the direction of data transmission/reception
Data is transmitted when:
R/W value is 1: From the slave device to the master device
R/W value is 0: From the master device to the slave device
A : Acknowledge
The receive device sets the SDA signal to “L”.
DATA : Transmit/receive data
P : Stop condition
The master device changes the SDA signal from “L” to “H” while the SCL signal is held “H”.

Figure 24.4 I2C bus Format and Bus Timing

24.4.2 Master Transmit Operation

In master transmit mode, the master device outputs the transmit clock and data, and the slave device returns an acknowledge signal. Figures 24.5 and 24.6 show the Operating Timing in Master Transmit Mode (I2C bus Interface Mode).

The transmit procedure and operation in master transmit mode are as follows.

(1) Set the STOP bit in the ICSR register to 0 for initialization, and set the ICE bit in the ICCR1 register to 1 (transfer operation enabled). Then, set bits WAIT and MLS in the ICMR register and bits CKS0 to CKS3 in the ICCR1 register (initial setting).
(2) After confirming that the bus is released by reading the BBSY bit in the ICCR2 register, set bits TRS and MST in the ICCR1 register to master transmit mode. Then, write 1 to the BBSY bit and 0 to the SCP bit with the MOV instruction (start condition generated). This will generate a start condition.
(3) After confirming that the TDRE bit in the ICSR register is set to 1 (data is transferred from registers ICDRT to ICDRS), write transmit data to the ICDRT register (data in which a slave address and R/$\overline{W}$ are indicated in the 1st byte). At this time, the TDRE bit is automatically set to 0. When data is transferred from registers ICDRT to ICDRS, the TDRE bit is set to 1 again.
(4) When 1 byte of data transmission is completed while the TDRE bit is set to 1, the TEND bit in the ICSR register is set to 1 at the rising edge of the 9th clock cycle of the transmit clock. After confirming that the slave device is selected by reading the ACKBR bit in the ICIER register, write the 2nd byte of data to the ICDRT register. Since the slave device is not acknowledged when the ACKBR bit is set to 1, generate a stop condition. Stop condition generation is enabled by writing 0 to the BBSY bit and 0 to the SCP bit with the MOV instruction. The SCL signal is fixed “L” until data is ready or a stop condition is generated.
(5) Write the transmit data after the 2nd byte to the ICDRT register every time the TDRE bit is set to 1.
(6) When the number of bytes to be transmitted is written to the ICDRT register, wait until the TEND bit is set to 1 while the TDRE bit is set to 1. Or wait for NACK (NACKF bit in ICSR register = 1) from the receive device while the ACKE bit in the ICIER register is set to 1 (when the receive acknowledge bit is set to 1, transfer is halted). Then, generate a stop condition before setting the TEND bit or the NACKF bit to 0.
(7) When the STOP bit in the ICSR register is set to 1, return to slave receive mode.

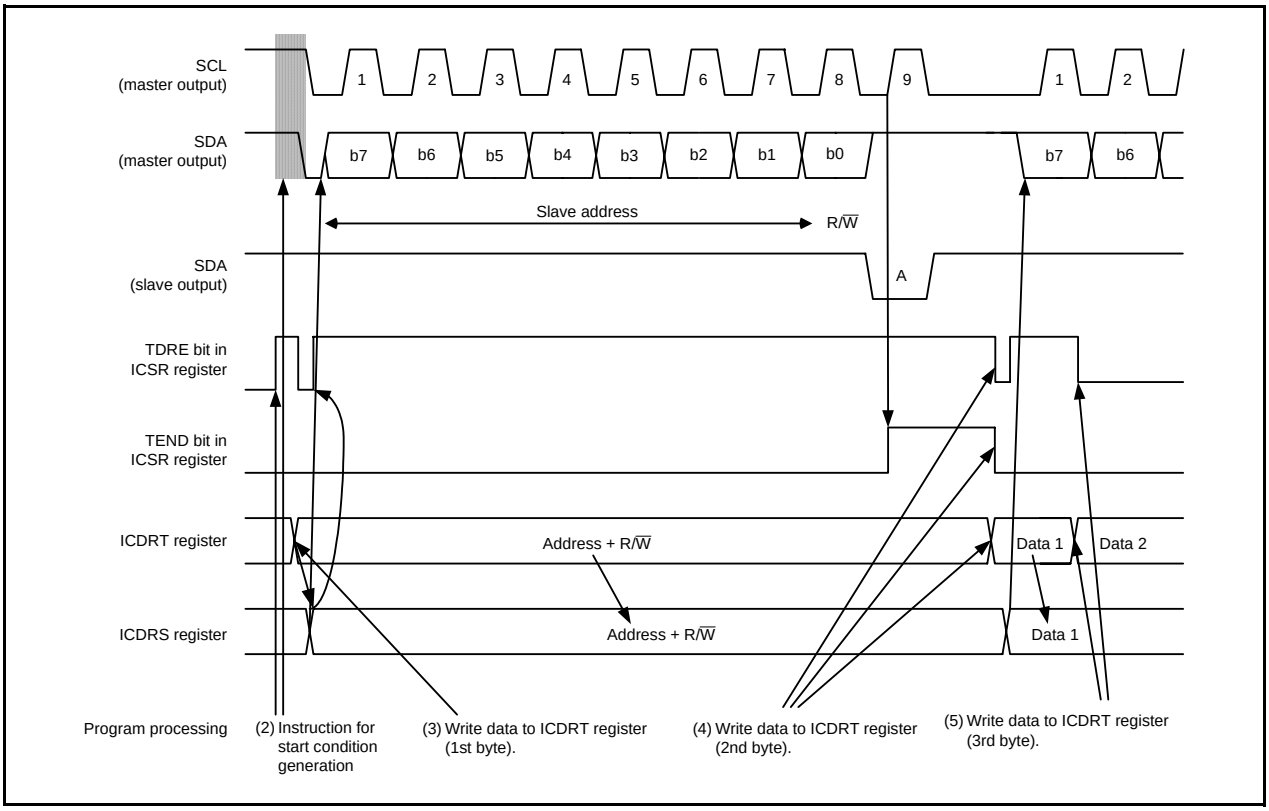


Figure 24.5 Operating Timing in Master Transmit Mode (I2C bus Interface Mode) (1)

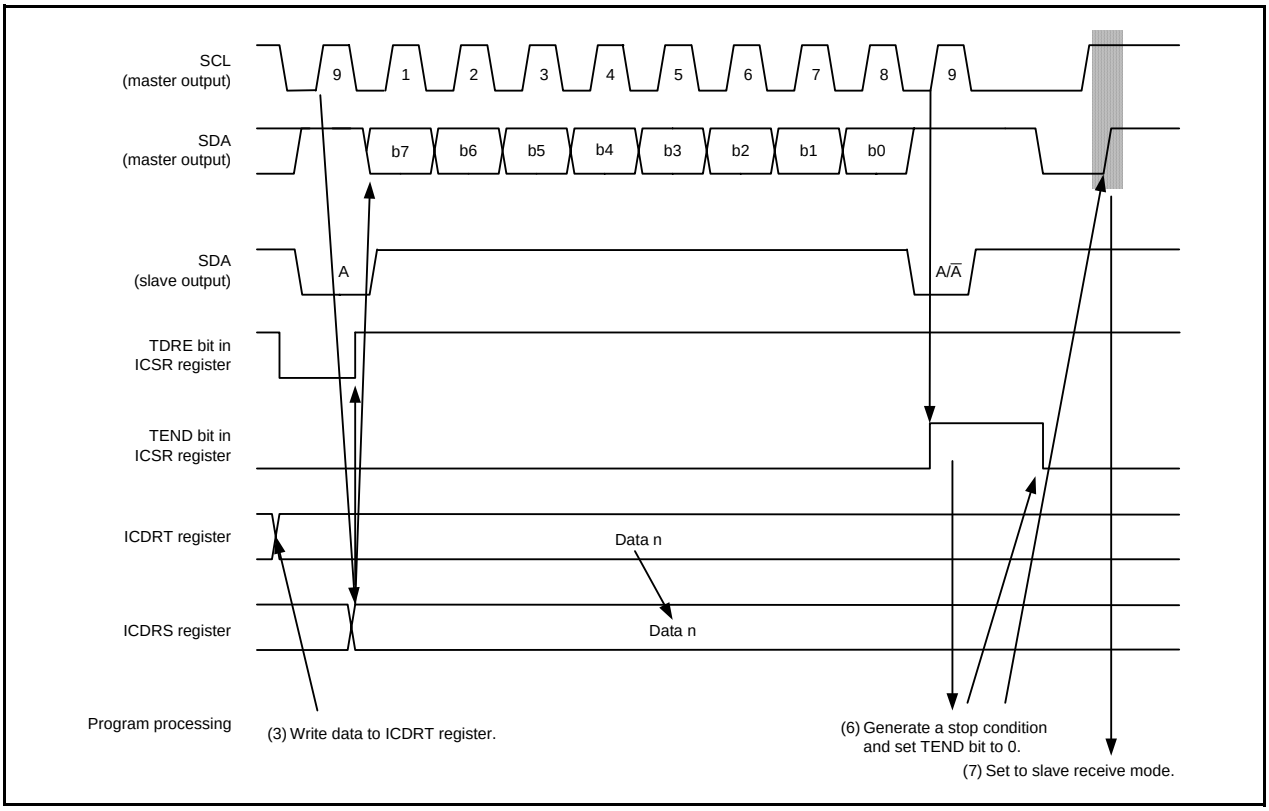


Figure 24.6 Operating Timing in Master Transmit Mode (I2C bus Interface Mode) (2)

24.4.3 Master Receive Operation

In master receive mode, the master device outputs the receive clock, receives data from the slave device, and returns an acknowledge signal. Figures 24.7 and 24.8 show the Operating Timing in Master Receive Mode (I^2C bus Interface Mode).

The receive procedure and operation in master receive mode are shown below.

(1) After setting the TEND bit in the ICSR register to 0, set the TRS bit in the ICCR1 register to 0 to switch from master transmit mode to master receive mode. Then set the TDRE bit in the ICSR register to 0.
(2) Dummy reading the ICDRR register starts receive operation. The receive clock is output in synchronization with the internal clock and data is received. The master device outputs the level set by the ACKBT bit in the ICIER register to the SDA pin at the rising edge of the 9th clock cycle of the receive clock.
(3) When 1-frame of data reception is completed, the RDRF bit in the ICSR register is set to 1 at the rising edge of the 9th clock cycle of the receive clock. At this time, if the ICDRR register is read, the received data can be read and the RDRF bit is set to 0 simultaneously.
(4) Continuous receive operation is enabled by reading the ICDRR register every time the RDRF bit is set to 1. If reading the ICDRR register is delayed by another process and the 8th clock cycle falls while the RDRF bit is set to 1, the SCL signal is fixed “L” until the ICDRR register is read.
(5) If the next frame is the last receive frame and the RCVD bit in the ICCR1 register is set to 1 (next receive operation disabled) before reading the ICDRR register, stop condition generation is enabled after the next receive operation.
(6) When the RDRF bit is set to 1 at the rising edge of the 9th clock cycle of the receive clock, generate a stop condition. When a stop condition generation or a start condition regeneration overlaps with the falling edge of the ninth clock cycle of SCL, an additional cycle is output after the ninth clock cycle. Refer to **24.9 Notes on I^2C bus Interface**.
(7) When the STOP bit in the ICSR register is set to 1, read the ICDRR register and set the RCVD bit to 0 (next receive operation continues).
(8) Return to slave receive mode.

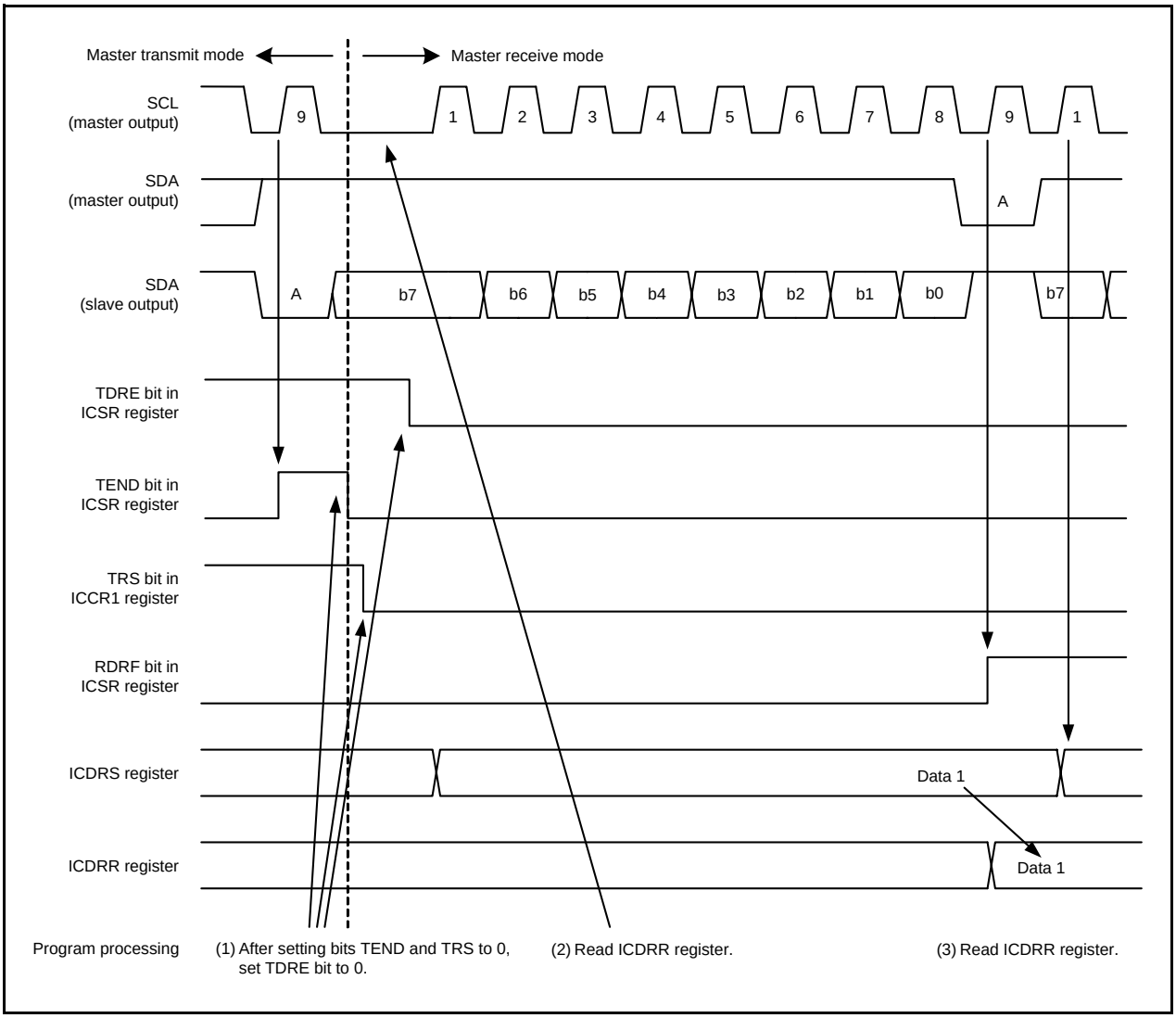


Figure 24.7 Operating Timing in Master Receive Mode (I2C bus Interface Mode) (1)

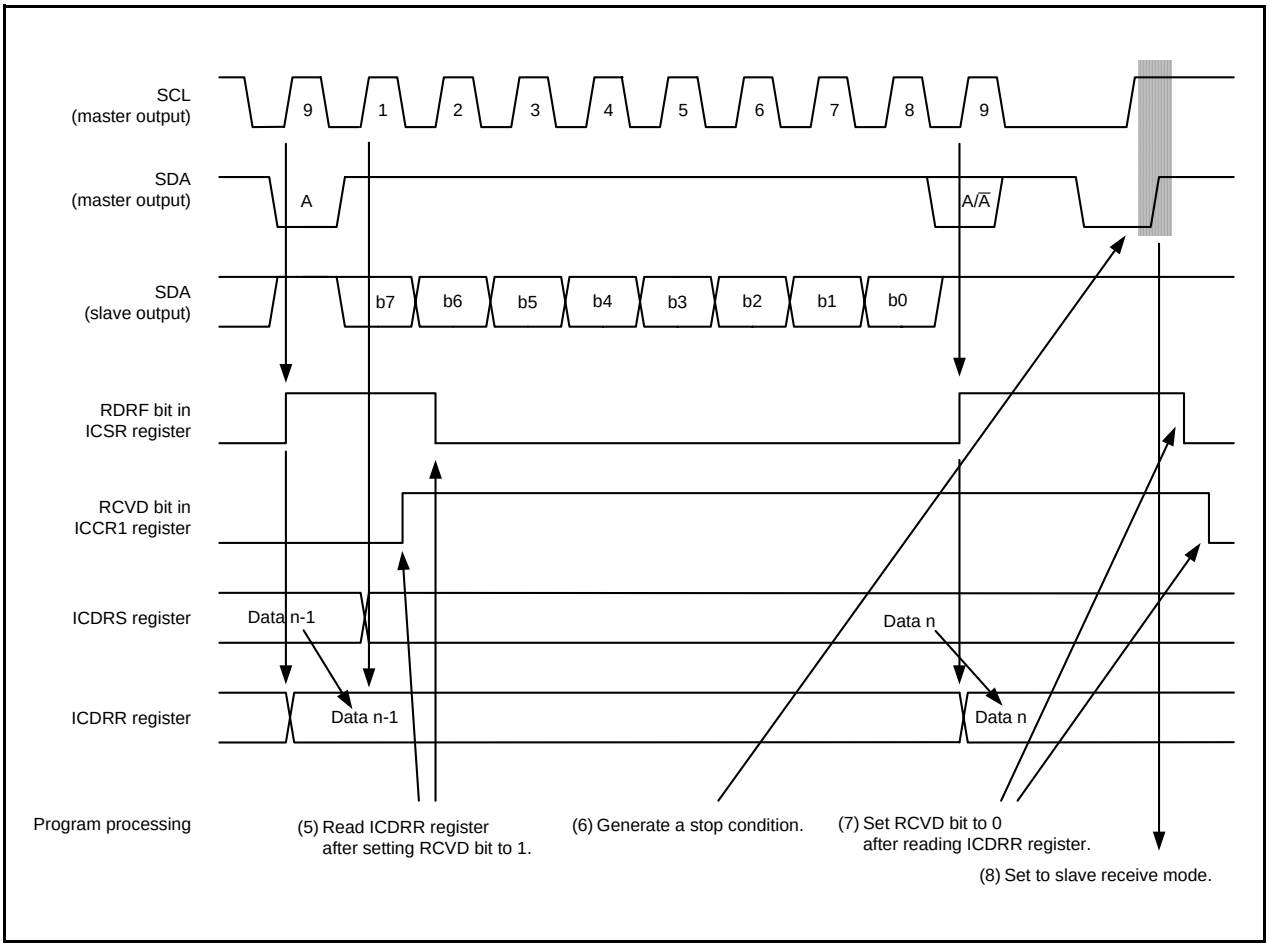


Figure 24.8 Operating Timing in Master Receive Mode (I2C bus Interface Mode) (2)

24.4.4 Slave Transmit Operation

In slave transmit mode, the slave device outputs the transmit data while the master device outputs the receive clock and returns an acknowledge signal. Figures 24.9 and 24.10 show the Operating Timing in Slave Transmit Mode (I2C bus Interface Mode).

The transmit procedure and operation in slave transmit mode are as follows.

(1) Set the ICE bit in the ICCR1 register to 1 (transfer operation enabled), and set bits WAIT and MLS in the ICMR register and bits CKS0 to CKS3 in the ICCR1 register (initial setting). Then, set bits TRS and MST in the ICCR1 register to 0 and wait until the slave address matches in slave receive mode.

(2) When the slave address matches at the first frame after detecting the start condition, the slave device outputs the level set by the ACKBT bit in the ICIER register to the SDA pin at the rising edge of the 9th clock cycle. At this time, if the 8th bit of data (R/$\overline{W}$) is 1, bits TRS and TDRE in the ICSR register are set to 1, and the mode is switched to slave transmit mode automatically. Continuous transmission is enabled by writing transmit data to the ICDRT register every time the TDRE bit is set to 1.

(3) When the TDRE bit in the ICDRT register is set to 1 after the last transmit data is written to the ICDRT register, wait until the TEND bit in the ICSR register is set to 1 while the TDRE bit is set to 1. When the TEND bit is set to 1, set the TEND bit to 0.

(4) Set the TRS bit to 0 and dummy read the ICDRR register to end the process. This will release the SCL signal.

(5) Set the TDRE bit to 0.

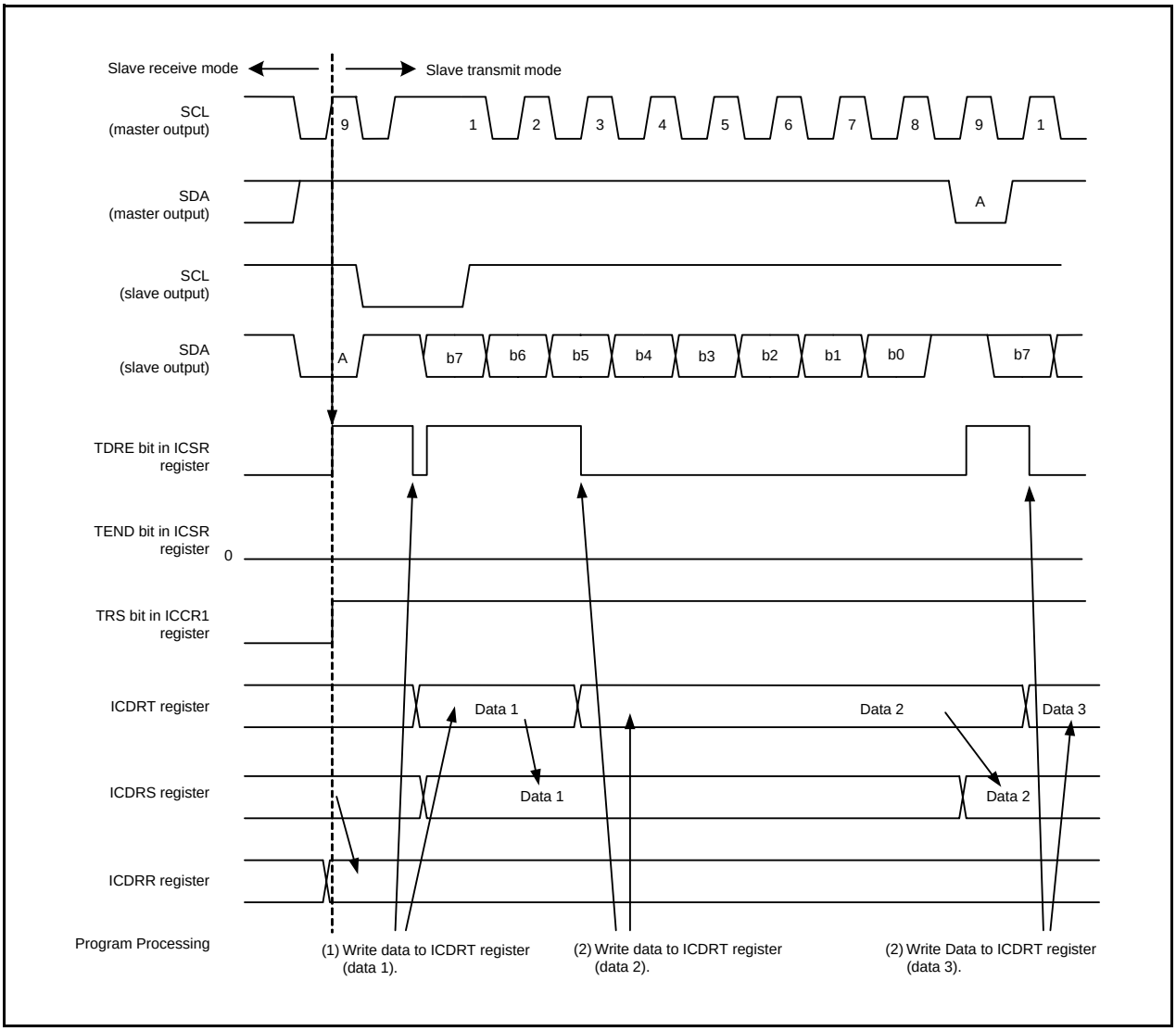


Figure 24.9 Operating Timing in Slave Transmit Mode (I2C bus Interface Mode) (1)

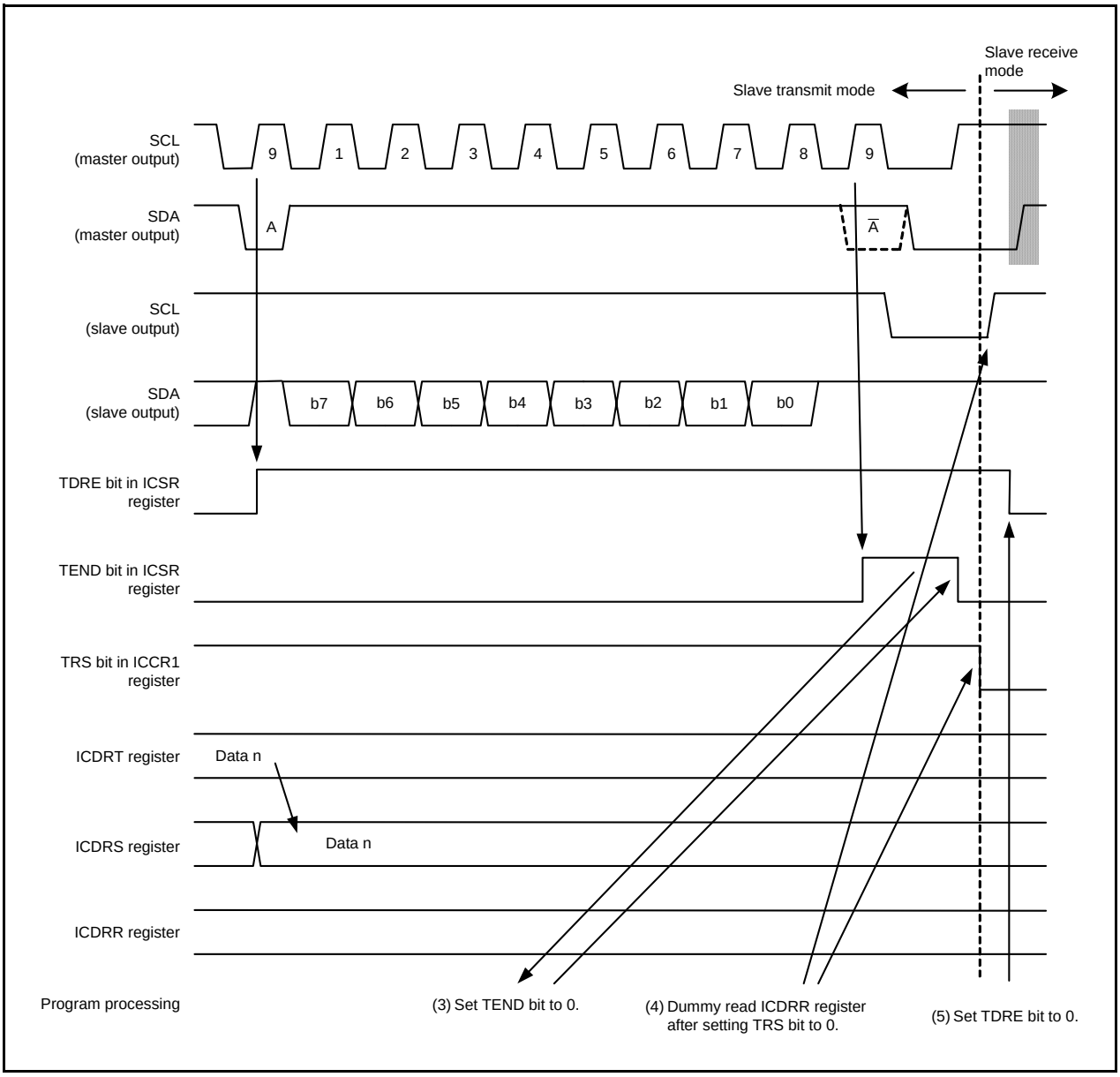


Figure 24.10 Operating Timing in Slave Transmit Mode (I2C bus Interface Mode) (2)

24.4.5 Slave Receive Operation

In slave receive mode, the master device outputs the transmit clock and data, and the slave device returns an acknowledge signal. Figures 24.11 and 24.12 show the Operating Timing in Slave Receive Mode (I2C bus Interface Mode).

The receive procedure and operation in slave receive mode are as follows.

(1) Set the ICE bit in the ICCR1 register to 1 (transfer operation enabled), and set bits WAIT and MLS in the ICMR register and bits CKS0 to CKS3 in the ICCR1 register (initial setting). Then, set bits TRS and MST in the ICCR1 register to 0 and wait until the slave address matches in slave receive mode.

(2) When the slave address matches at the first frame after detecting the start condition, the slave device outputs the level set in the ACKBT bit in the ICIER register to the SDA pin at the rising edge of the 9th clock cycle. Since the RDRF bit in the ICSR register is set to 1 simultaneously, dummy read the ICDRR register (the read data is unnecessary because it indicates the slave address and R/$\overline{W}$).

(3) Read the ICDRR register every time the RDRF bit is set to 1. If the 8th clock cycle falls while the RDRF bit is set to 1, the SCL signal is fixed “L” until the ICDRR register is read. The setting change of the acknowledge signal returned to the master device before reading the ICDRR register takes affect from the following transfer frame.

(4) Reading the last byte is also performed by reading the ICDRR register.

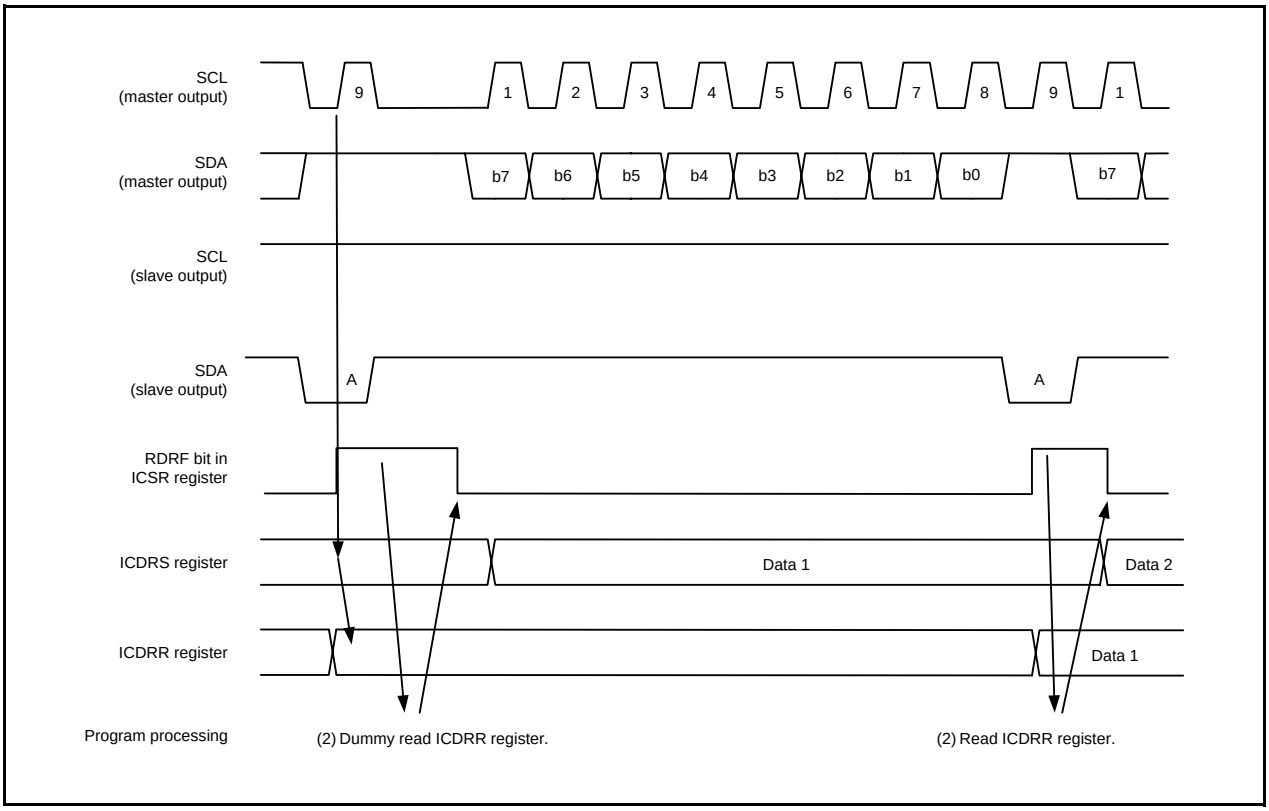


Figure 24.11 Operating Timing in Slave Receive Mode (I2C bus Interface Mode) (1)

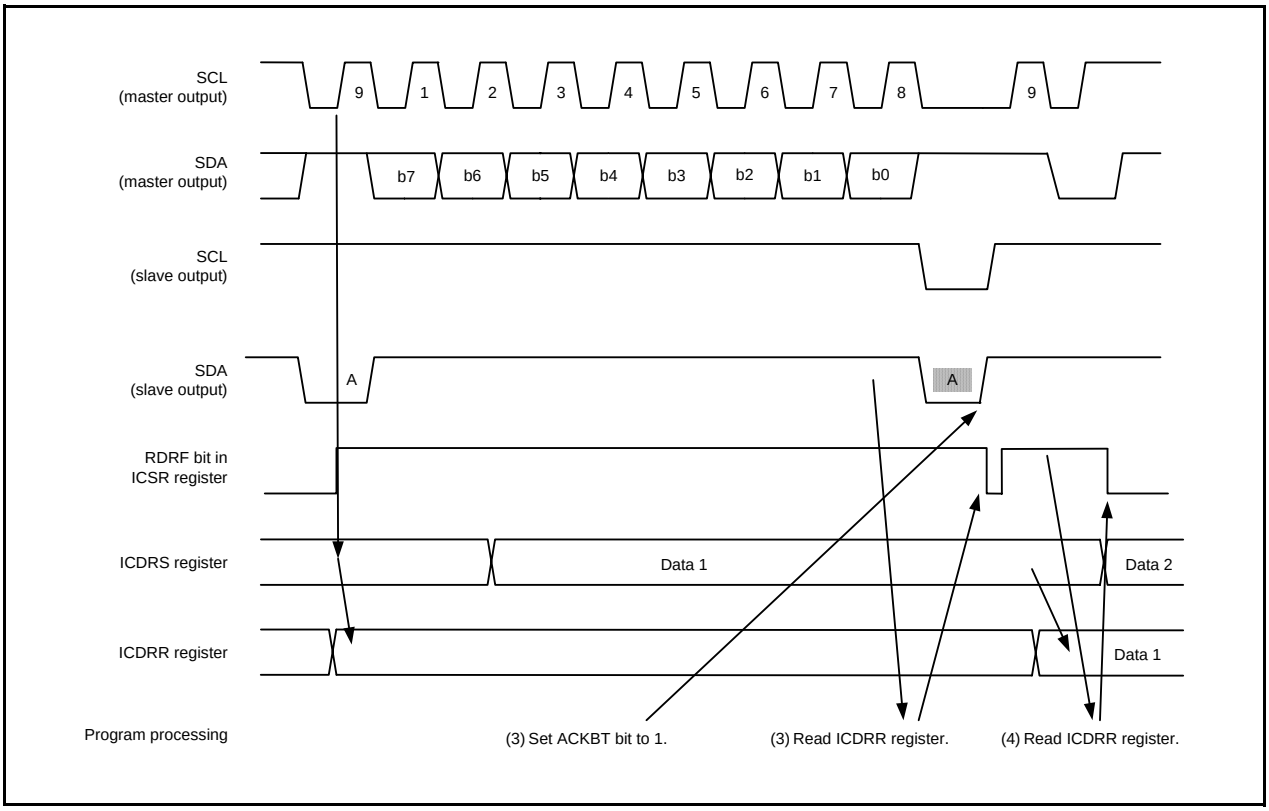


Figure 24.12 Operating Timing in Slave Receive Mode (I2C bus Interface Mode) (2)

24.5 Clock Synchronous Serial Mode

24.5.1 Clock Synchronous Serial Format

When the FS bit in the SAR register is set to 1, the clock synchronous serial format is used for communication. Figure 24.13 shows the Transfer Format of Clock Synchronous Serial Format.

When the MST bit in the ICCR1 register is set to 1, the transfer clock is output from the SCL pin. When the MST bit is set to 0, the external clock is input.

The transfer data is output between successive falling edges of the SCL clock, and data is determined at the rising edge of the SCL clock. MSB-first or LSB-first can be selected as the order of the data transfer by setting the MLS bit in the ICMR register. The SDA output level can be changed by the SDAO bit in the ICCR2 register during transfer standby.

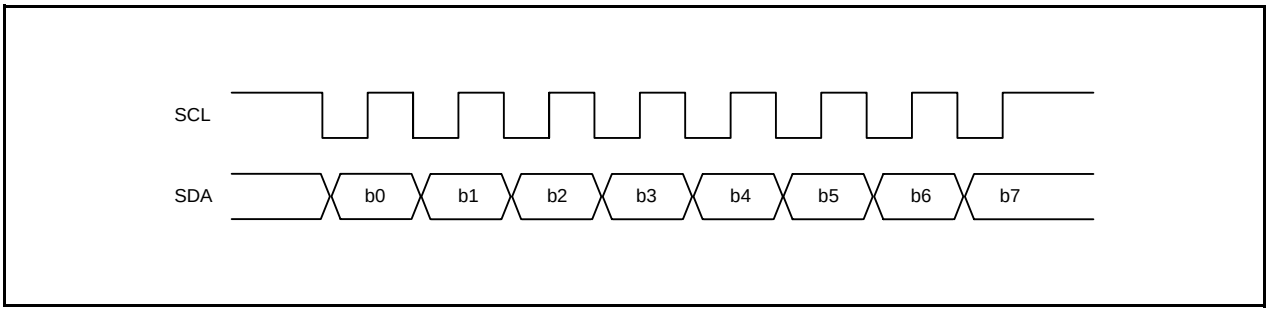


Figure 24.13 Transfer Format of Clock Synchronous Serial Format

24.5.2 Transmit Operation

In transmit mode, transmit data is output from the SDA pin in synchronization with the falling edge of the transfer clock. The transfer clock is output when the MST bit in the ICCR1 register is set to 1 and input when the MST bit is set to 0.
Figure 24.14 shows the Operating Timing in Transmit Mode (Clock Synchronous Serial Mode).

The transmit procedure and operation in transmit mode are as follows.

(1) Set the ICE bit in the ICCR1 register to 1 (transfer operation enabled). Then set bits CKS0 to CKS3 in the ICCR1 register and the MST bit (initial setting).
(2) Set the TRS bit in the ICCR1 register to 1 to select transmit mode. This will set the TDRE bit in the ICSR register is to 1.
(3) After confirming that the TDRE bit is set to 1, write transmit data to the ICDRT register. Data is transferred from registers ICDRT to ICDRS and the TDRE bit is automatically set to 1. Continuous transmission is enabled by writing data to the ICDRT register every time the TDRE bit is set to 1. To switch from transmit to receive mode, set the TRS bit to 0 while the TDRE bit is set to 1.

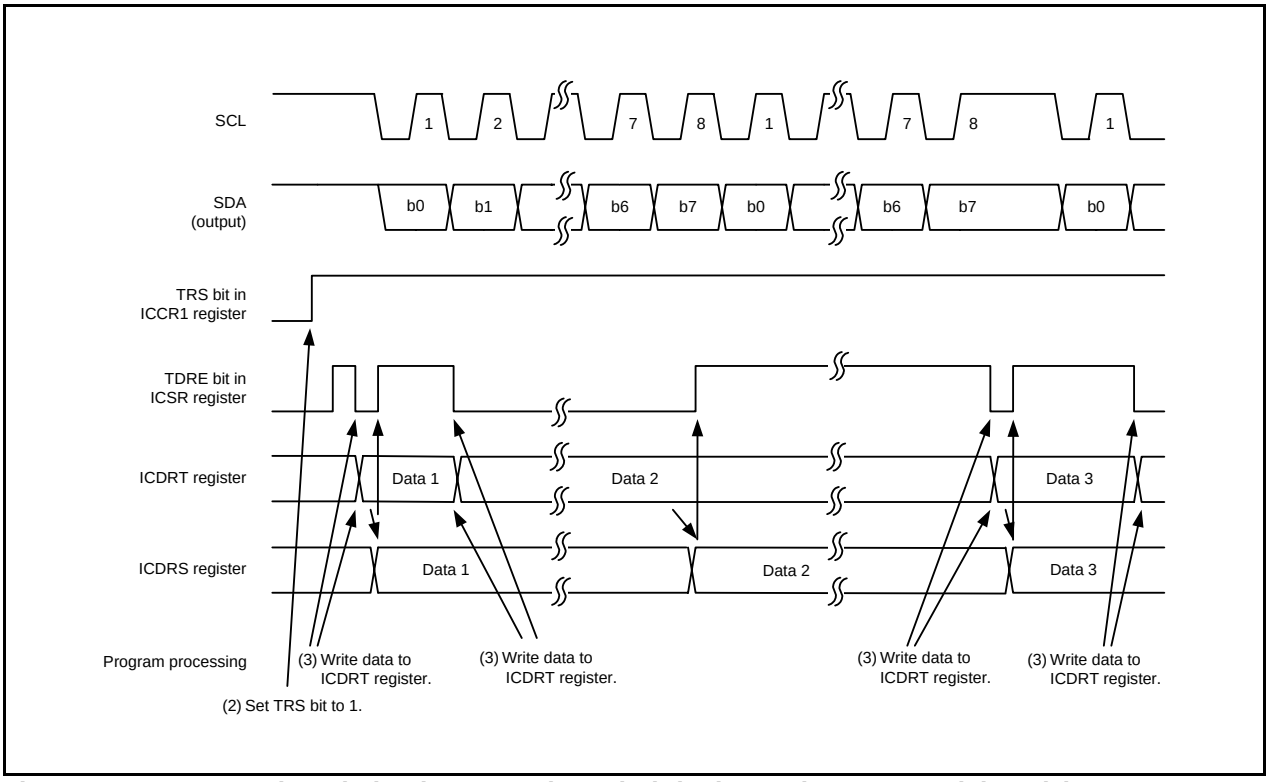


Figure 24.14 Operating Timing in Transmit Mode (Clock Synchronous Serial Mode)

24.5.3 Receive Operation

In receive mode, data is latched at the rising edge of the transfer clock. The transfer clock is output when the MST bit in the ICCR1 register is set to 1 and input when the MST bit is set to 0.
Figure 24.15 shows the Operating Timing in Receive Mode (Clock Synchronous Serial Mode).

The receive procedure and operation in receive mode are as follows.

(1) Set the ICE bit in the ICCR1 register to 1 (transfer operation enabled). Then set bits CKS0 to CKS3 in the ICCR1 register and the MST bit (initial setting).
(2) Set the MST bit to 1 while the transfer clock is being output. This will start the output of the receive clock.
(3) When the receive operation is completed, data is transferred from registers ICDRS to ICDRR and the RDRF bit in the ICSR register is set to 1. When the MST bit is set to 1, the clock is output continuously since the next byte of data is enabled for reception. Continuous reception is enabled by reading the ICDRR register every time the RDRF bit is set to 1. If the 8th clock cycle falls while the RDRF bit is set to 1, an overrun is detected and the AL bit in the ICSR register is set to 1. At this time, the last receive data is retained in the ICDRR register.
(4) When the MST bit is set to 1, set the RCVD bit in the ICCR1 register to 1 (next receive operation disabled) and read the ICDRR register. The SCL signal is fixed “H” after the following byte of data reception is completed.

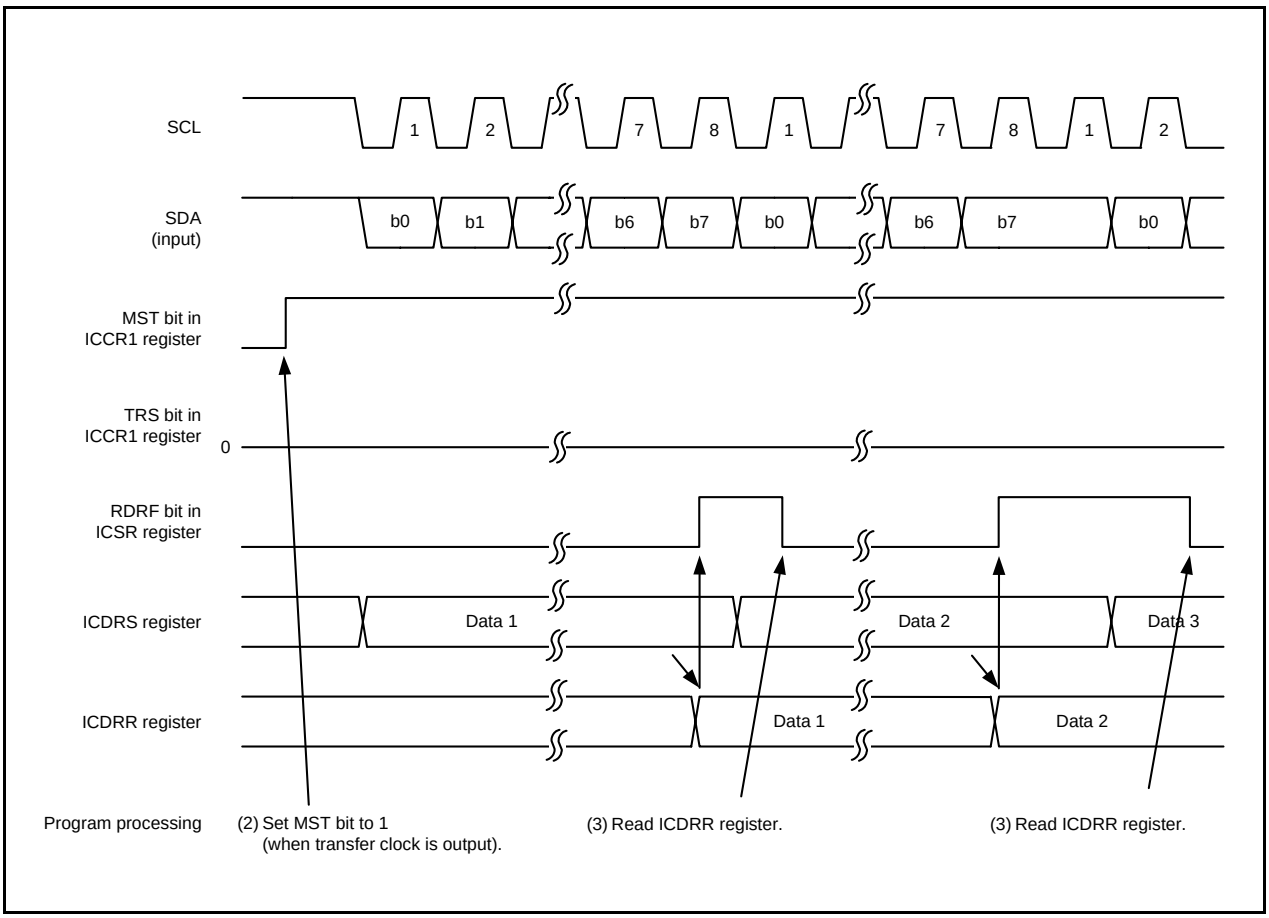


Figure 24.15 Operating Timing in Receive Mode (Clock Synchronous Serial Mode)

24.6 Examples of Register Setting

Figures 24.16 to 24.19 show Examples of Register Setting When Using I2C bus interface.

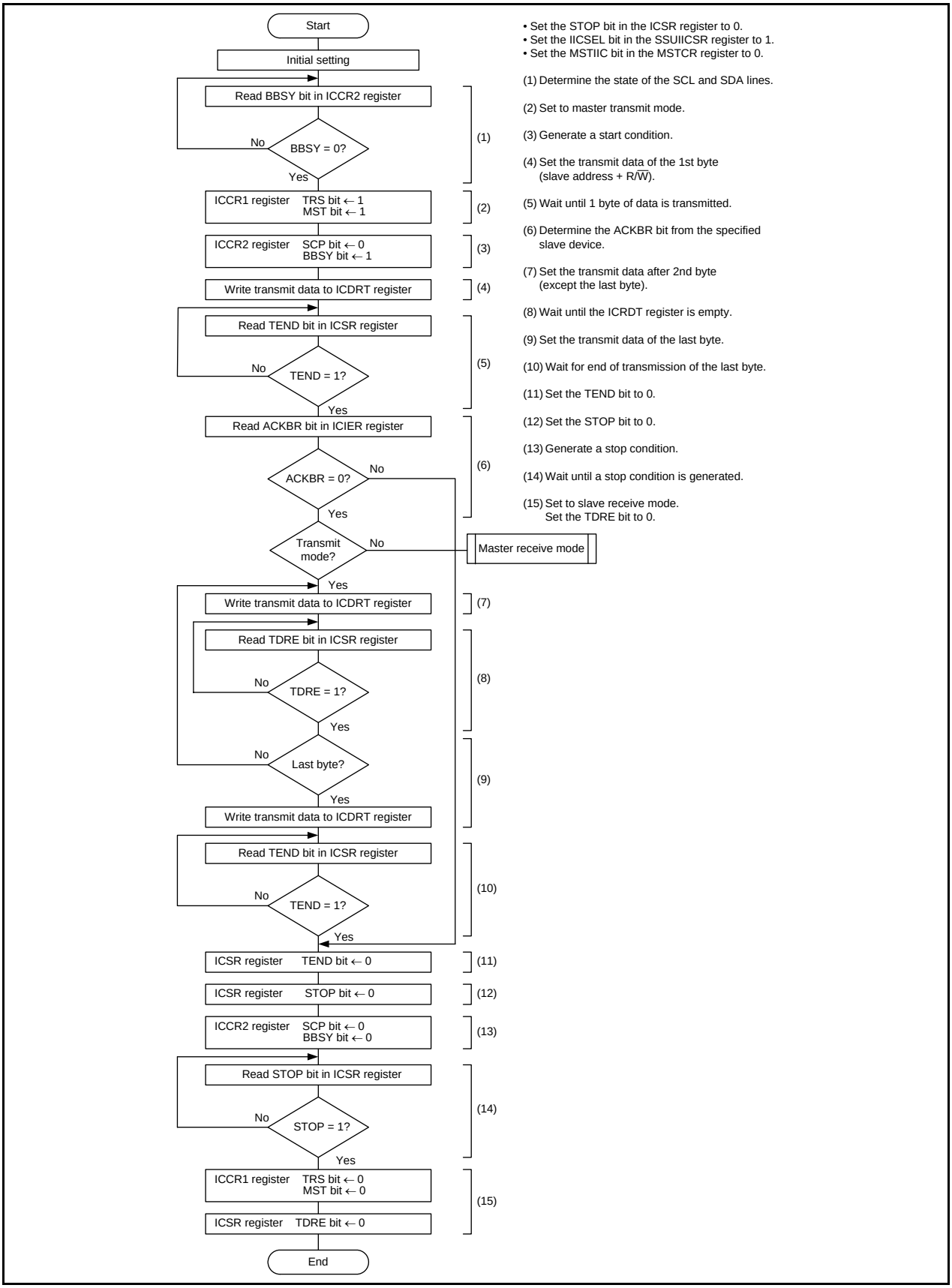
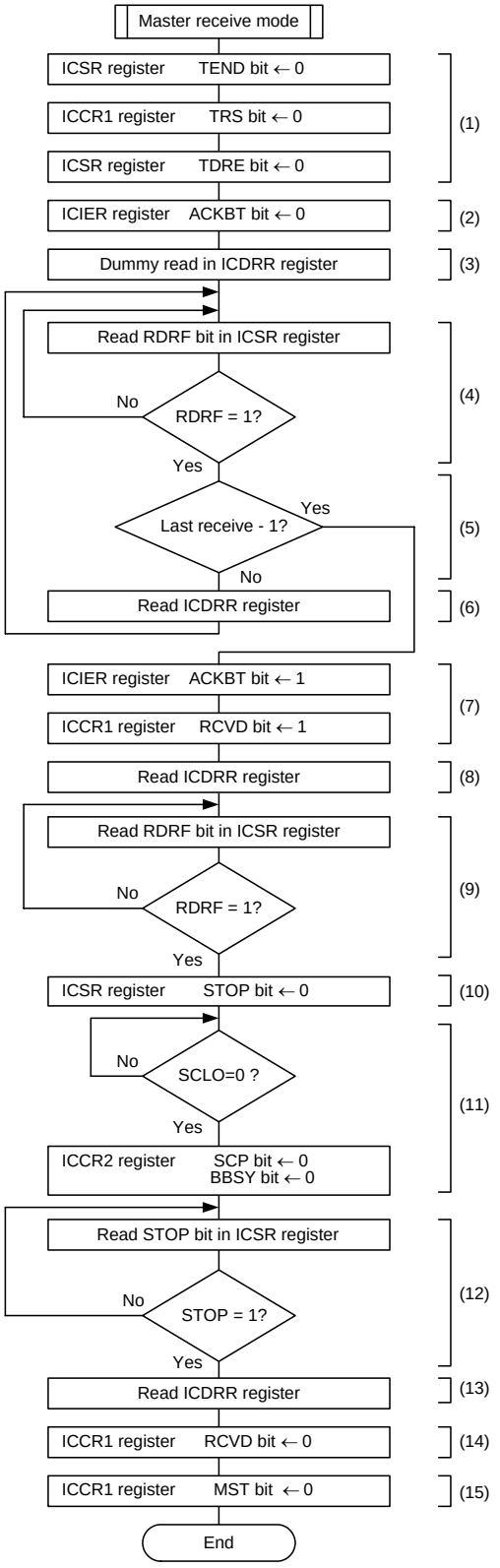


Figure 24.16 Register Setting Example in Master Transmit Mode (I2C bus Interface Mode)



(1) Set the TEND bit to 0 and set to master receive mode. Set the TDRE bit to 0. (1,2)

(2) Set the ACKBT bit to the transmit device. (1)

(3) Dummy read the ICDRR register. (1)

(4) Wait until 1 byte is received.

(5) Determine (last receive – 1).

(6) Read the receive data.

(7) Set the ACKBT bit of the last byte and set continuous receive operation to disable (RCVD = 1). (2)

(8) Read the receive data of (last byte – 1).

(9) Wait until the last byte is received.

(10) Set the STOP bit to 0.

(11) Generate a stop condition. (3)

(12) Wait until a stop condition is generated.

(13) Read the receive data of the last byte.

(14) Set the RCVD bit to 0.

(15) Set to slave receive mode.

Notes:
1. Do not generate interrupts while processing steps (1) to (3).
2. For 1 byte of data reception, skip steps (2) to (6) after step (1) and jump to process step (7). Process step (8) is a dummy read from the ICDRR register.
3. After confirming the falling edge of the 9th clock cycle of SCL, generate a stop condition. Refer to **24.9.1 Master Receive Mode**.

Figure 24.17 Register Setting Example in Master Receive Mode (I2C bus Interface Mode)

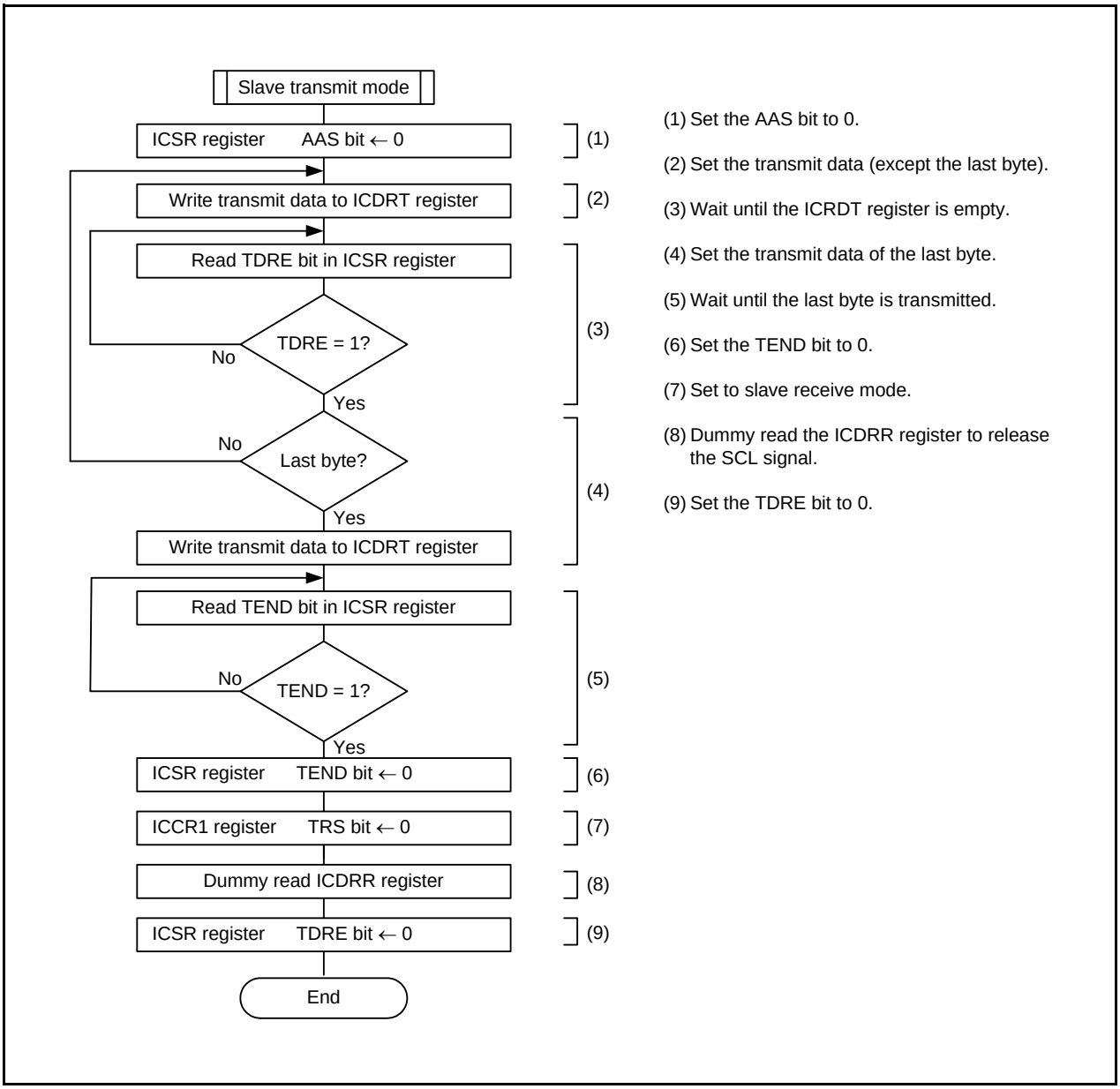
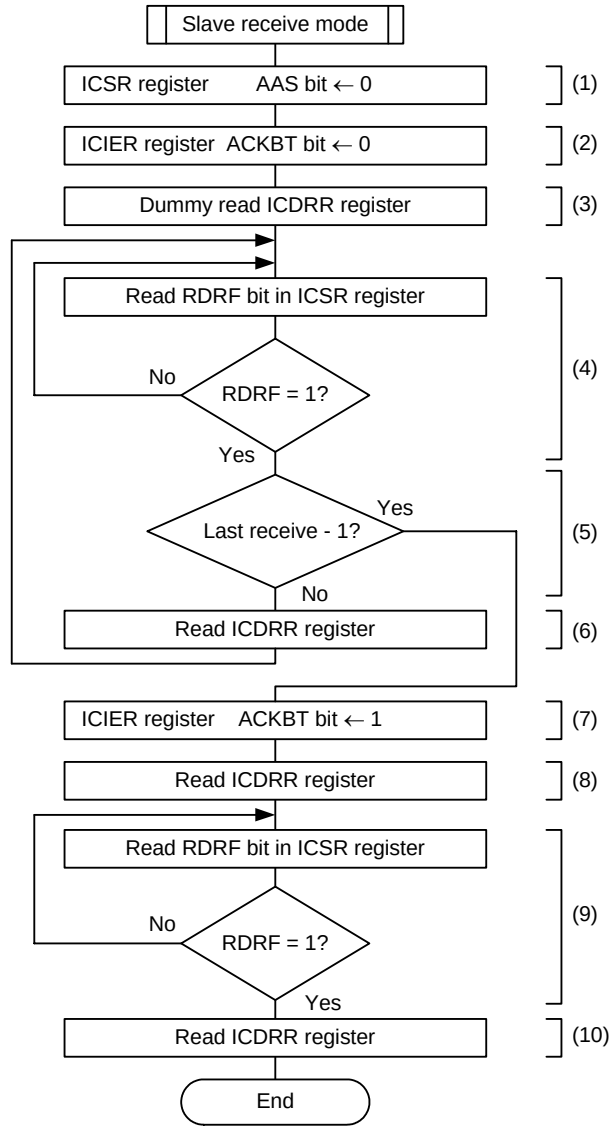


Figure 24.18 Register Setting Example in Slave Transmit Mode (I2C bus Interface Mode)



(1) Set the AAS bit to 0. (1)

(2) Set the ACKBT bit to the transmit device.

(3) Dummy read the ICDRR register.

(4) Wait until 1 byte is received.

(5) Determine (last receive – 1).

(6) Read the receive data.

(7) Set the ACKBT bit of the last byte. (1)

(8) Read the receive data of (last byte – 1).

(9) Wait until the last byte is received.

(10) Read the receive data of the last byte.

Note:
1. For 1 byte of data reception, skip steps (2) to (6) after (1) and jump to process step (7). Process step (8) is a dummy read from the ICDRR register.

Figure 24.19 Register Setting Example in Slave Receive Mode (I2C bus Interface Mode)

24.7 Noise Canceller

The states of pins SCL and SDA are routed through the noise canceller before being latched internally. Figure 24.20 shows a Noise Canceller Block Diagram.

The noise canceller consists of two cascaded latch and match detector circuits. When the SCL pin input signal (or SDA pin input signal) is sampled on f1 and two latch outputs match, the level is passed forward to the next circuit. When they do not match, the former value is retained.

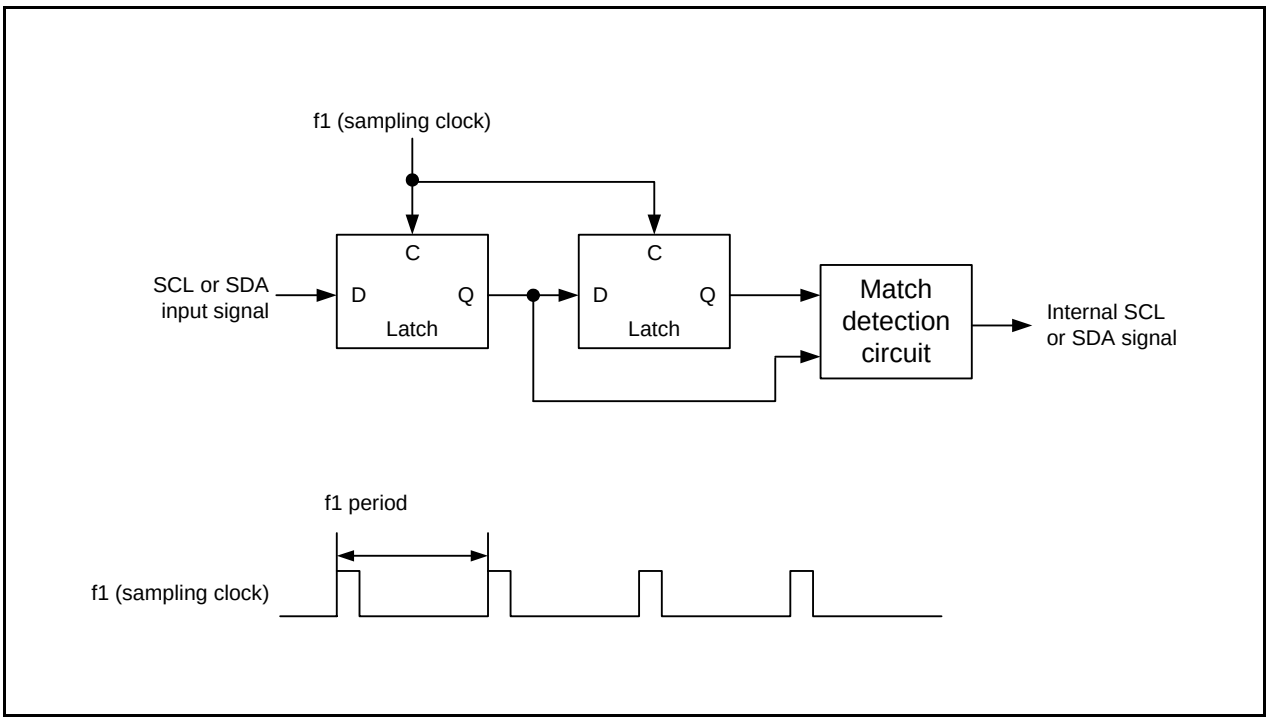


Figure 24.20 Noise Canceller Block Diagram

24.8 Bit Synchronization Circuit

When the I2C bus interface is set to master mode, the high-level period may become shorter if:

- The SCL signal is driven L level by a slave device
- The rise speed of the SCL signal is reduced by a load (load capacity or pull-up resistor) on the SCL line.

Therefore, the SCL signal is monitored and communication is synchronized bit by bit.

Figure 24.21 shows the Bit Synchronization Circuit Timing and Table 24.7 lists the Time between Changing SCL Signal from “L” Output to High-Impedance and Monitoring SCL Signal.

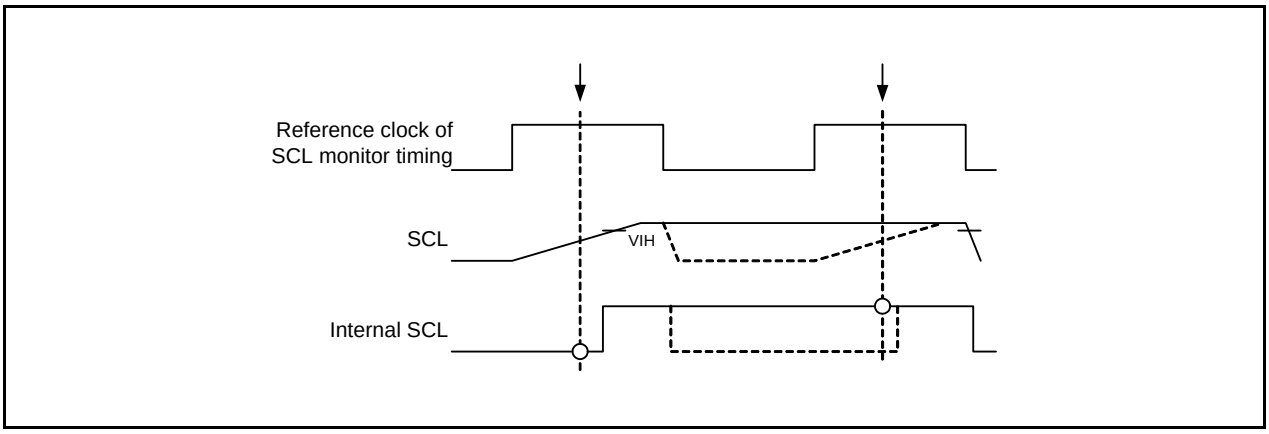


Figure 24.21 Bit Synchronization Circuit Timing

Table 24.7 Time between Changing SCL Signal from “L” Output to High-Impedance and Monitoring SCL Signal

ICCR1 Register		SCL Monitoring Time
CKS3	CKS2	
0	0	7.5Tcyc
	1	19.5Tcyc
1	0	17.5Tcyc
	1	41.5Tcyc

1Tcyc = 1/f1(s)

24.9 Notes on I2C bus Interface

To use the I2C bus interface, set the IICSEL bit in the SSUIICSR register to 1 (I2C bus interface function selected).

24.9.1 Master Receive Mode

After a master receive operation is completed, when a stop condition generation or a start condition regeneration overlaps with the falling edge of the ninth clock cycle of SCL, an additional cycle is output after the ninth clock cycle.

24.9.1.1 Countermeasure

After a master receive operation is completed, confirm the falling edge of the ninth clock cycle of SCL and generate a stop condition or regenerate a start condition.
Confirm the falling edge of the ninth clock cycle of SCL as follows: Confirm the SCLO bit in the ICCR2 register (SCL monitor flag) becomes 0 (SCL pin is low) after confirming the RDRF bit in the ICSR register (receive data register full flag) becomes 1.

24.9.2 The ICE Bit in the ICCR1 Register and the IICRST Bit in the ICCR2 Register

When writing 0 to the ICE bit or 1 to the IICRST bit during an I2C bus interface operation, the BBSY bit in the ICCR2 register and the STOP bit in the ICSR register may become undefined.

24.9.2.1 Conditions When Bits Become Undefined

- When this module occupies the bus in master transmit mode (bits MST and TRS in the ICCR1 register are 1).
- When this module occupies the bus in master receive mode (the MST bit is 1 and the TRS bit is 0).
- When this module transmits data in slave transmit mode (the MST bit is 0 and the TRS bit is 1).
- When this module transmits an acknowledge in slave receive mode (bits MST and TRS are 0).

24.9.2.2 Countermeasures

- When the start condition (the SDA falling edge when SCL is high) is input, the BBSY bit becomes 1.
- When the stop condition (the SDA rising edge when SCL is high) is input, the BBSY bit becomes 0.
- When writing 1 to the BBSY bit, 0 to the SCP bit, and the start condition (the SDA falling edge when SCL is high) is output while SCL and SDA are high in master transmit mode, the BBSY bit becomes 1.
- When writing 0 to bits BBSY and SCP, the stop condition (the SDA rising edge when SCL is high) is output while SDA is low, and this is the only module that holds SCL low in master transmit mode or master receive mode, the BBSY bit becomes 0.
- When writing 1 to the FS bit in the SAR register, the BBSY bit becomes 0.

24.9.2.3 Additional Descriptions Regarding the IICRST Bit

- When writing 1 to the IICRST bit, bits SDAO and SCLO in the ICCR2 register become 1.
- When writing 1 to the IICRST bit in master transmit mode and slave transmit mode, the TDRE bit in the ICSR register becomes 1.
- While the control block of the I2C bus interface is reset by setting the IICRST bit to 1, writing to bits BBSY, SCP, and SDAO is disabled. Write 0 to the IICRST bit before writing to the BBSY bit, SCP bit, or SDAO bit.
- Even when writing 1 to the IICRST bit, the BBSY bit does not become 0. However, the stop condition (the SDA rising edge when SCL is high) may be generated depending on the states of SCL and SDA and the BBSY bit may become 0. There may also be a similar effect on other bits.
- While the control block of the I2C bus interface is reset by setting the IICRST bit to 1, data transmission/reception is stopped. However, the function to detect the start condition, stop condition, or arbitration lost operates. The values in the ICCR1 register, ICCR2 register, or ICSR register may be updated depending on the signals applied to pins SCL and SDA.

25. Hardware LIN

The hardware LIN performs LIN communication in cooperation with timer RA and UART0.

25.1 Overview

The hardware LIN has the features listed below.
Figure 25.1 shows a Hardware LIN Block Diagram.
The wake-up function for each mode is detected using $\overline{\text{INT1}}$.

Master mode
- Synch Break generation
- Bus collision detection

Slave mode
- Synch Break detection
- Synch Field measurement
- Control function for Synch Break and Synch Field signal inputs to UART0
- Bus collision detection

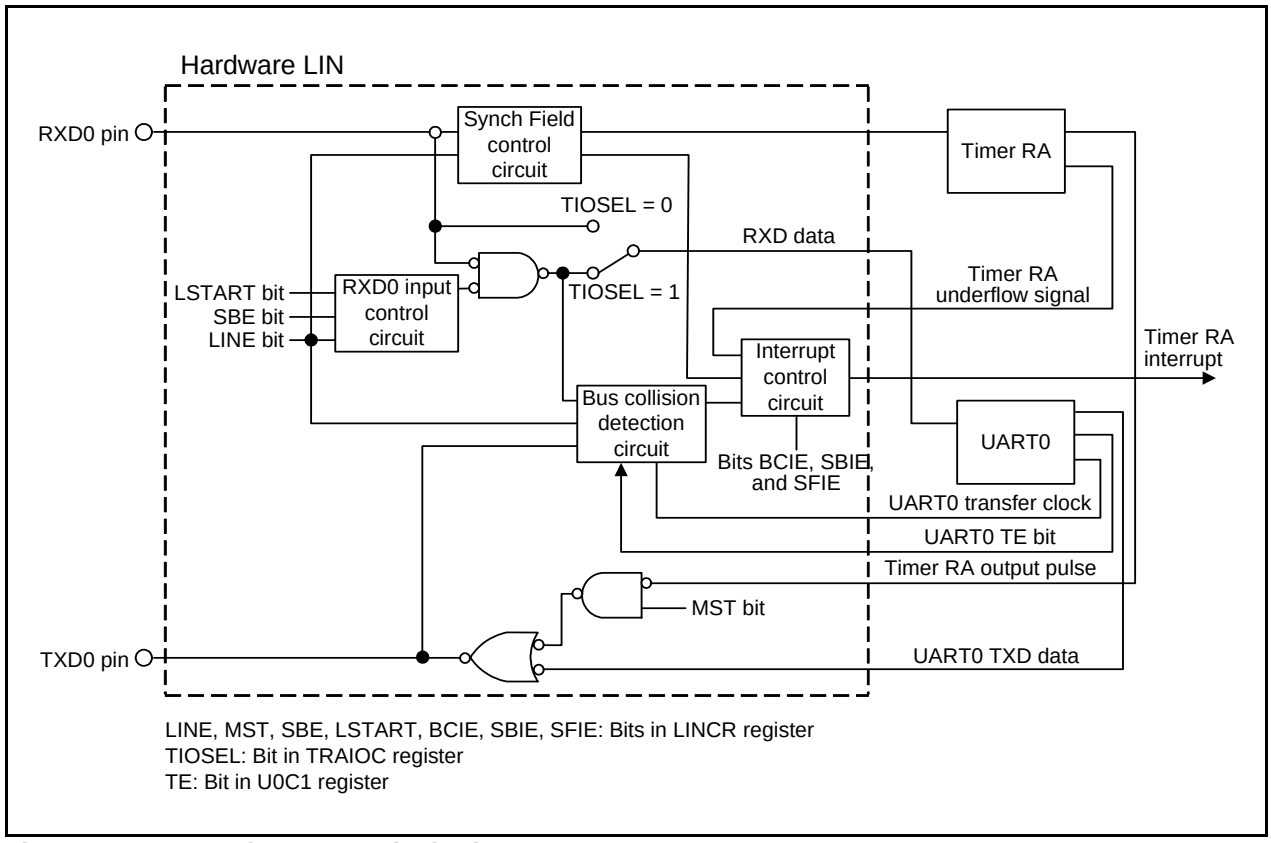


Figure 25.1 Hardware LIN Block Diagram

25.2 Input/Output Pins

Table 25.1 lists the Hardware LIN Pin Configuration.

Table 25.1 Hardware LIN Pin Configuration

Name	Pin Name	Assigned Pin	I/O	Function
Receive data input	RXD0	P1_5 (1)	Input	Receive data input pin for the hardware LIN
Transmit data output	TXD0	P1_4 (2)	Output	Transmit data output pin for the hardware LIN

Notes:
1. To use the hardware LIN, refer to **Table 7.16**.
2. To use the hardware LIN, set the TXD0SEL0 bit in the U0SR register to 1.

25.3 Registers

The hardware LIN contains the following registers:

- LIN Control Register 2 (LINCR2)
- LIN Control Register (LINCR)
- LIN Status Register (LINST)

25.3.1 LIN Control Register 2 (LINCR2)

Address 0105h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	BCE
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	BCE	Bus collision detection during Sync Break transmission enable bit	0: Bus collision detection disabled 1: Bus collision detection enabled	R/W
b1	—	Reserved bits	Set to 0.	R/W
b2	—			
b3	—			
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

25.3.2 LIN Control Register (LINCR)

Address 0106h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	LINE	MST	SBE	LSTART	RXDSF	BCIE	SBIE	SFIE
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	SFIE	Synch Field measurement-completed interrupt enable bit	0: Synch Field measurement-completed interrupt disabled 1: Synch Field measurement-completed interrupt enabled	R/W
b1	SBIE	Synch Break detection interrupt enable bit	0: Synch Break detection interrupt disabled 1: Synch Break detection interrupt enabled	R/W
b2	BCIE	Bus collision detection interrupt enable bit	0: Bus collision detection interrupt disabled 1: Bus collision detection interrupt enabled	R/W
b3	RXDSF	RXD0 input status flag	0: RXD0 input enabled 1: RXD0 input disabled	R
b4	LSTART	Synch Break detection start bit (1)	When this bit is set to 1, timer RA input is enabled and RXD0 input is disabled. When read, the content is 0.	R/W
b5	SBE	RXD0 input unmasking timing select bit (effective only in slave mode)	0: Unmasked after Synch Break detected 1: Unmasked after Synch Field measurement completed	R/W
b6	MST	LIN operation mode setting bit (2)	0: Slave mode (Synch Break detection circuit operation) 1: Master mode (timer RA output OR'ed with TXD0)	R/W
b7	LINE	LIN operation start bit	0: LIN operation stops 1: LIN operation starts (3)	R/W

Notes:
1. After setting the LSTART bit, confirm that the RXDSF flag is set to 1 before Synch Break input starts.
2. Before switching LIN operation modes, stop the LIN operation (LINE bit = 0) once.
3. Inputs to timer RA and UART0 are disabled immediately after the LINE bit is set to 1 (LIN operation starts) (refer to **Figure 25.3 Header Field Transmission Flowchart Example (1)** and **Figure 25.7 Header Field Reception Flowchart Example (2)**).

25.3.3 LIN Status Register (LINST)

Address 0107h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	B2CLR	B1CLR	B0CLR	BCDCT	SBDCT	SFDCT
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	SFDCT	Synch Field measurement-completed flag	When this bit is set to 1, Synch Field measurement is completed.	R
b1	SBDCT	Synch Break detection flag	when this bit is set to 1, Synch Break is detected or Synch Break generation is completed.	R
b2	BCDCT	Bus collision detection flag	When this bit is set to 1, bus collision is detected.	R
b3	B0CLR	SFDCT bit clear bit	When this bit is set to 1, the SFDCT bit is set to 0. When read, the content is 0.	R/W
b4	B1CLR	SBDCT bit clear bit	When this bit is set to 1, the SBDCT bit is set to 0. When read, the content is 0.	R/W
b5	B2CLR	BCDCT bit clear bit	When this bit is set to 1, the BCDCT bit is set to 0. When read, the content is 0.	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	—			

25.4 Function Description

25.4.1 Master Mode

Figure 25.2 shows an Operating Example during Header Field Transmission in master mode. Figures 25.3 and 25.4 show Examples of Header Field Transmission Flowchart.
During header field transmission, the hardware LIN operates as follows:

(1) When 1 is written to the TSTART bit in the TRACR register for timer RA, a “L” level is output from the TXD0 pin for the period set in registers TRAPRE and TRA for timer RA.
(2) When timer RA underflows, the TXD0 pin output is inverted and the SBDCT flag in the LINST register is set to 1. If the SBIE bit in the LINCR register is set to 1, a timer RA interrupt is generated.
(3) The hardware LIN transmits “55h” via UART0.
(4) After the hardware LIN completes transmitting “55h”, it transmits an ID field via UART0.
(5) After the hardware LIN completes transmitting the ID field, it performs communication for a response field.

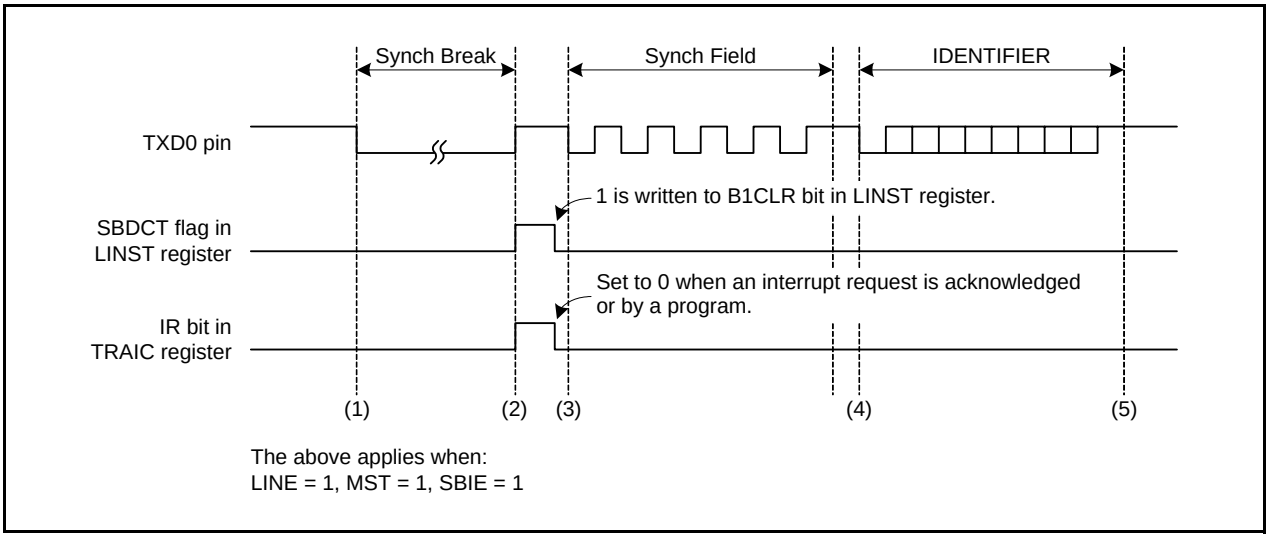
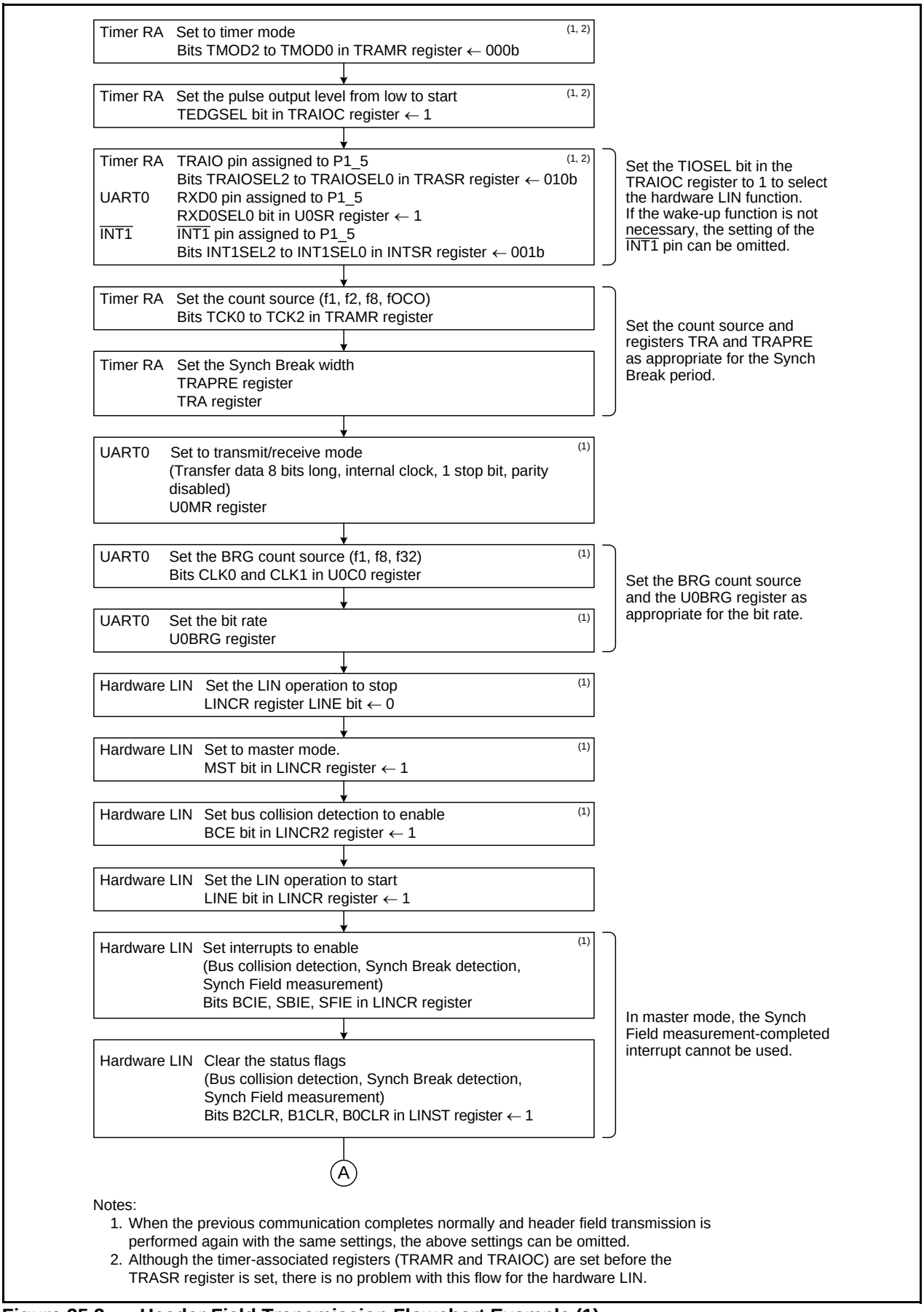


Figure 25.2 Operating Example during Header Field Transmission



Notes:
1. When the previous communication completes normally and header field transmission is performed again with the same settings, the above settings can be omitted.
2. Although the timer-associated registers (TRAMR and TRAIOC) are set before the TRASR register is set, there is no problem with this flow for the hardware LIN.

Figure 25.3 Header Field Transmission Flowchart Example (1)

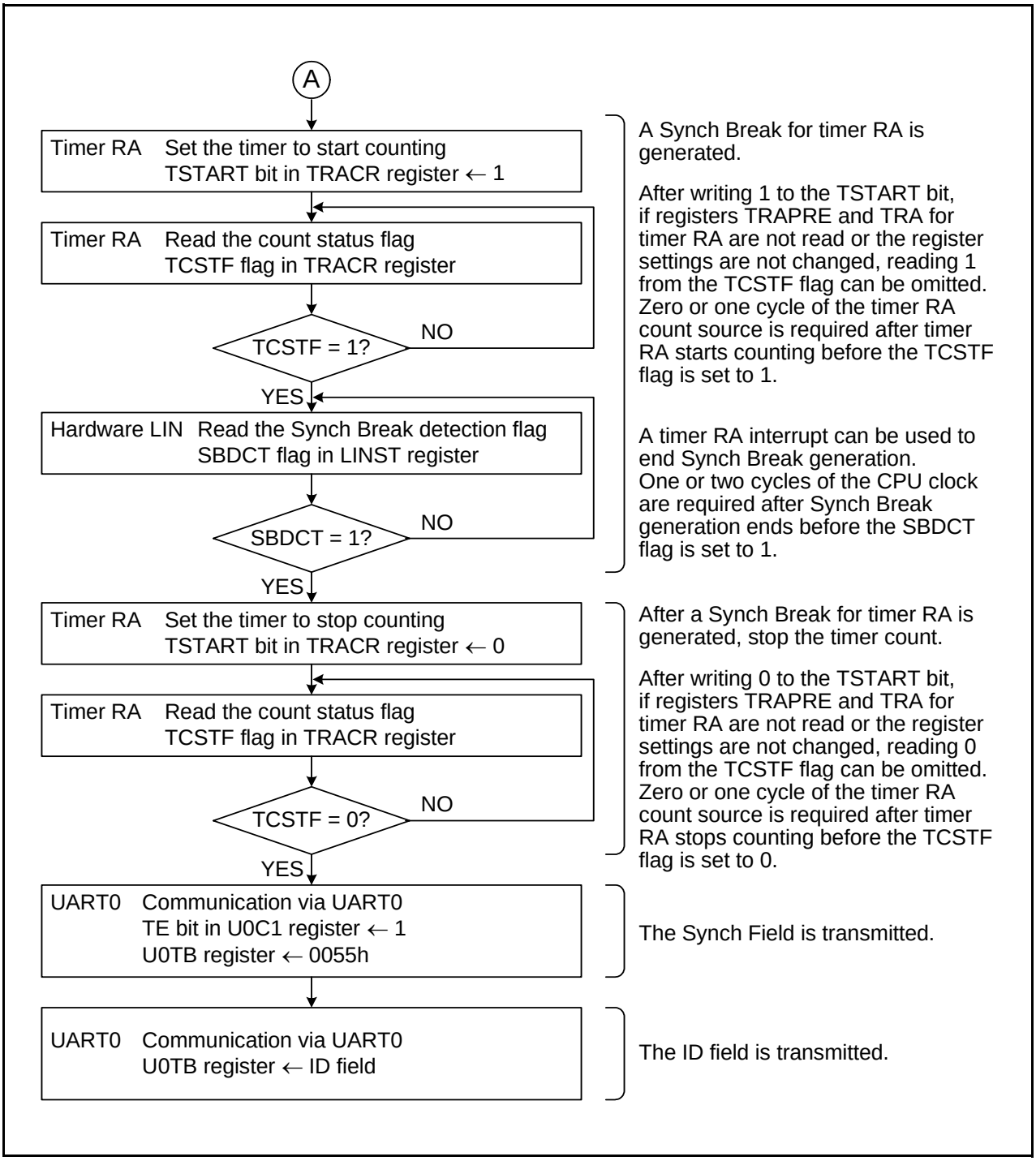


Figure 25.4 Header Field Transmission Flowchart Example (2)

25.4.2 Slave Mode

Figure 25.5 shows an Operating Example during Header Field Reception in slave mode. Figure 25.6 through Figure 25.8 show examples of Header Field Reception Flowchart.
During header field reception, the hardware LIN operates as follows:

(1) When 1 is written to the LSTART bit in the LINCR register for the hardware LIN, Synch Break detection is enabled.
(2) If a “L” level is input for a duration equal to or longer than the period set in timer RA, the hardware LIN detected it as a Synch Break. At this time, the SBDCT flag in the LINST register is set to 1. If the SBIE bit in the LINCR register is set to 1, a timer RA interrupt is generated. Then the hardware LIN enters the Synch Field measurement.
(3) The hardware LINA receives a Synch Field (55h) and measures the period of the start bit and bits 0 to 6 is using timer RA. At this time, whether to input the Synch Field signal to RXD0 of UART0 can be selected by the SBE bit in the LINCR register.
(4) When the Synch Field measurement is completed, the SFDCT flag in the LINST register is set to 1. If the SFIE bit in the LINCR register is set to 1, a timer RA interrupt is generated.
(5) After the Synch Field measurement is completed, a transfer rate is calculated from the timer RA count value. The rate is set in UART0 and registers TRAPRE and TRA for timer RA are set again. Then the hardware LIN receives an ID field via UART0.
(6) After the hardware LIN completes receiving the ID field, it performs communication for a response field.

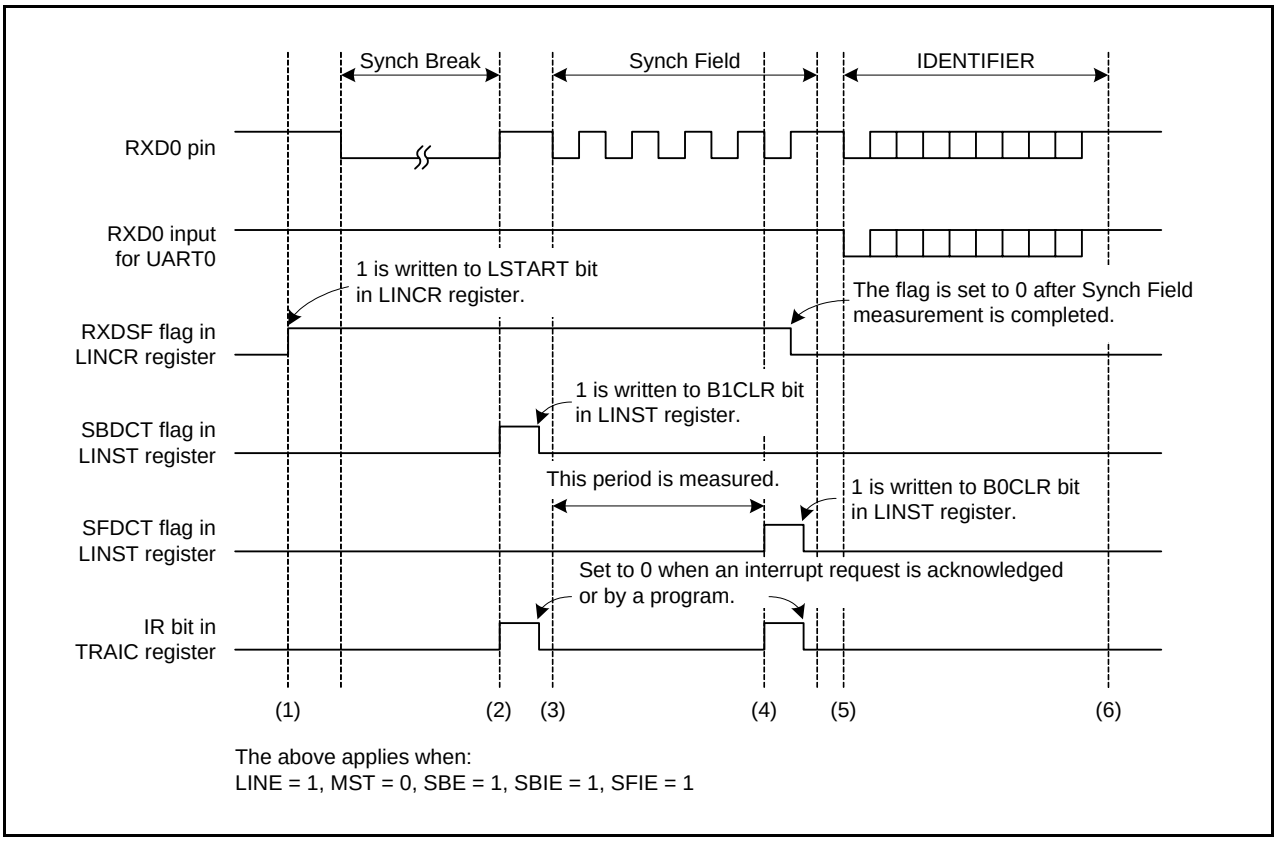
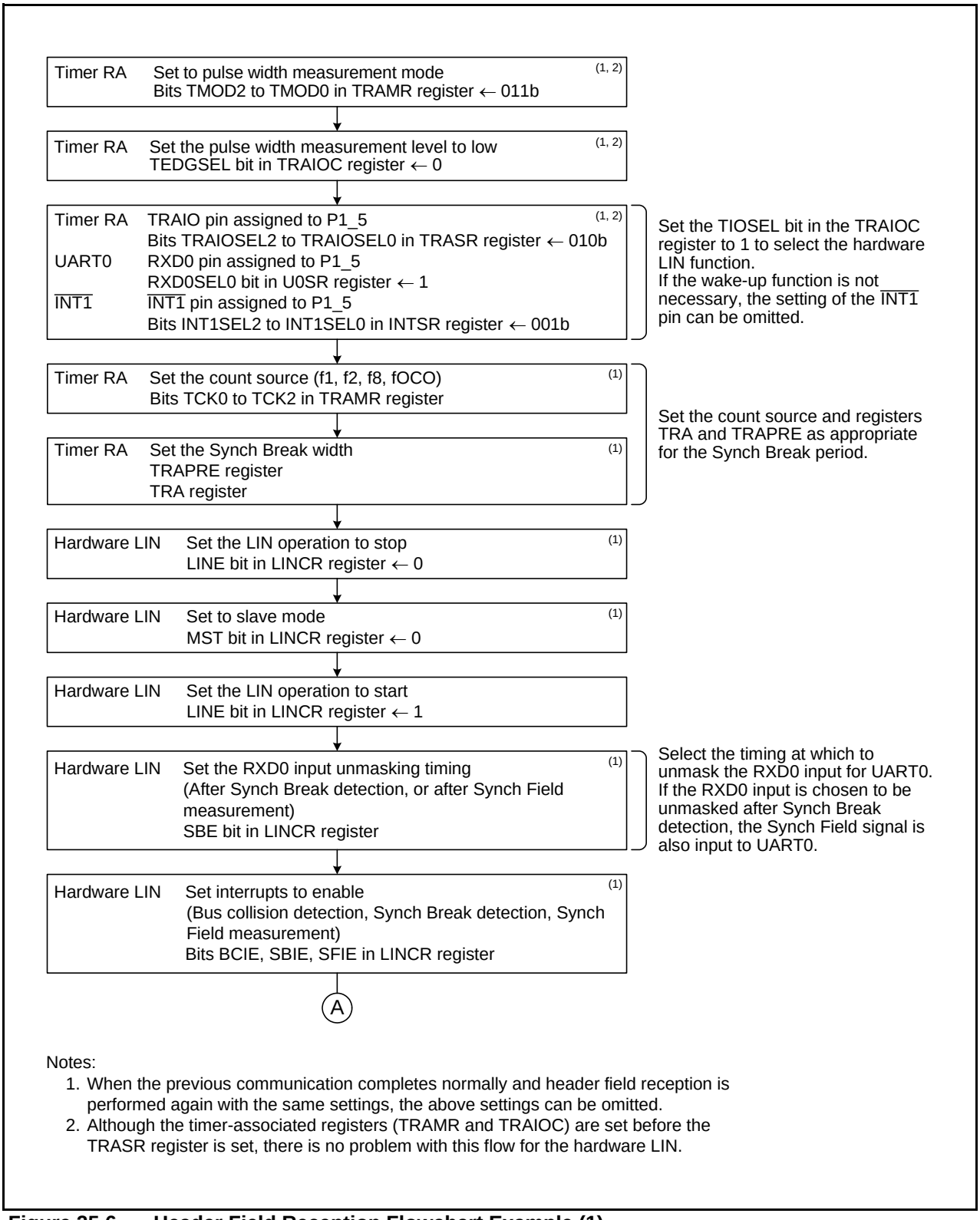


Figure 25.5 Operating Example during Header Field Reception



Notes:
1. When the previous communication completes normally and header field reception is performed again with the same settings, the above settings can be omitted.
2. Although the timer-associated registers (TRAMR and TRAIOC) are set before the TRASR register is set, there is no problem with this flow for the hardware LIN.

Figure 25.6 Header Field Reception Flowchart Example (1)

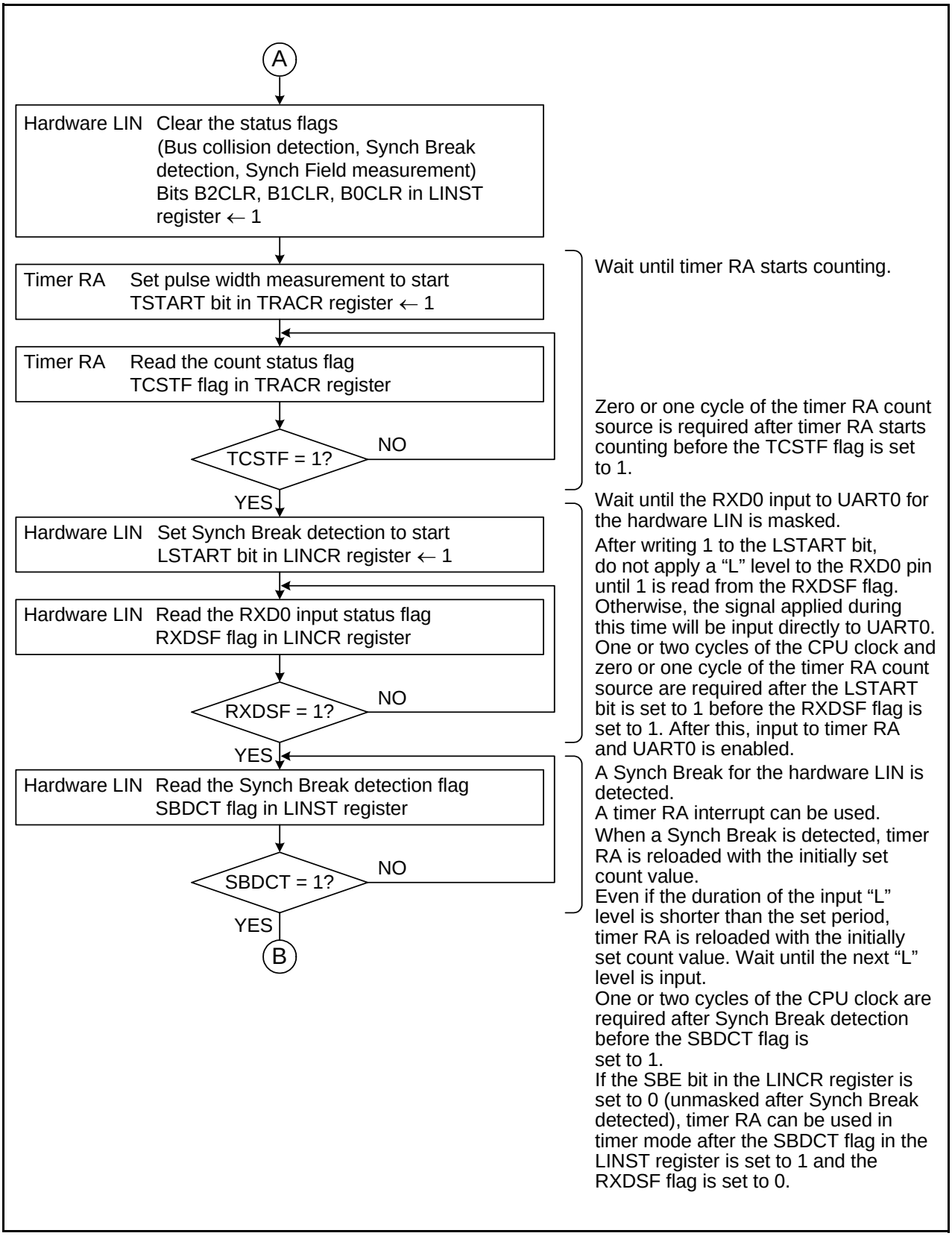


Figure 25.7 Header Field Reception Flowchart Example (2)

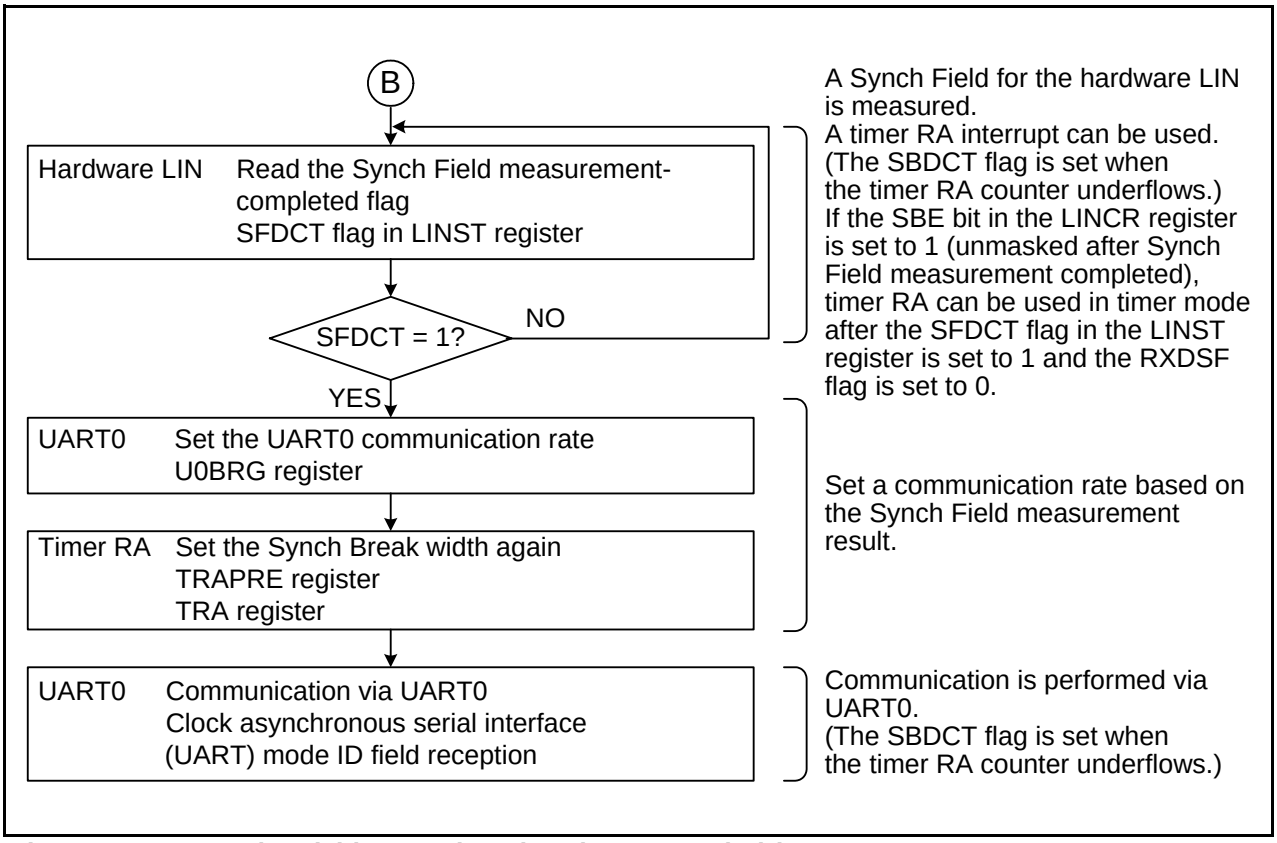


Figure 25.8 Header Field Reception Flowchart Example (3)

25.4.3 Bus Collision Detection Function

The bus collision detection function can be used if UART0 is enabled for transmission (TE bit in U0C1 register = 1). To detect a bus collision during Synch Break transmission, set the BCE bit in the LINCR2 register to 1 (bus collision detection enabled).
Figure 25.9 shows an Operating Example When Bus Collision is Detected.

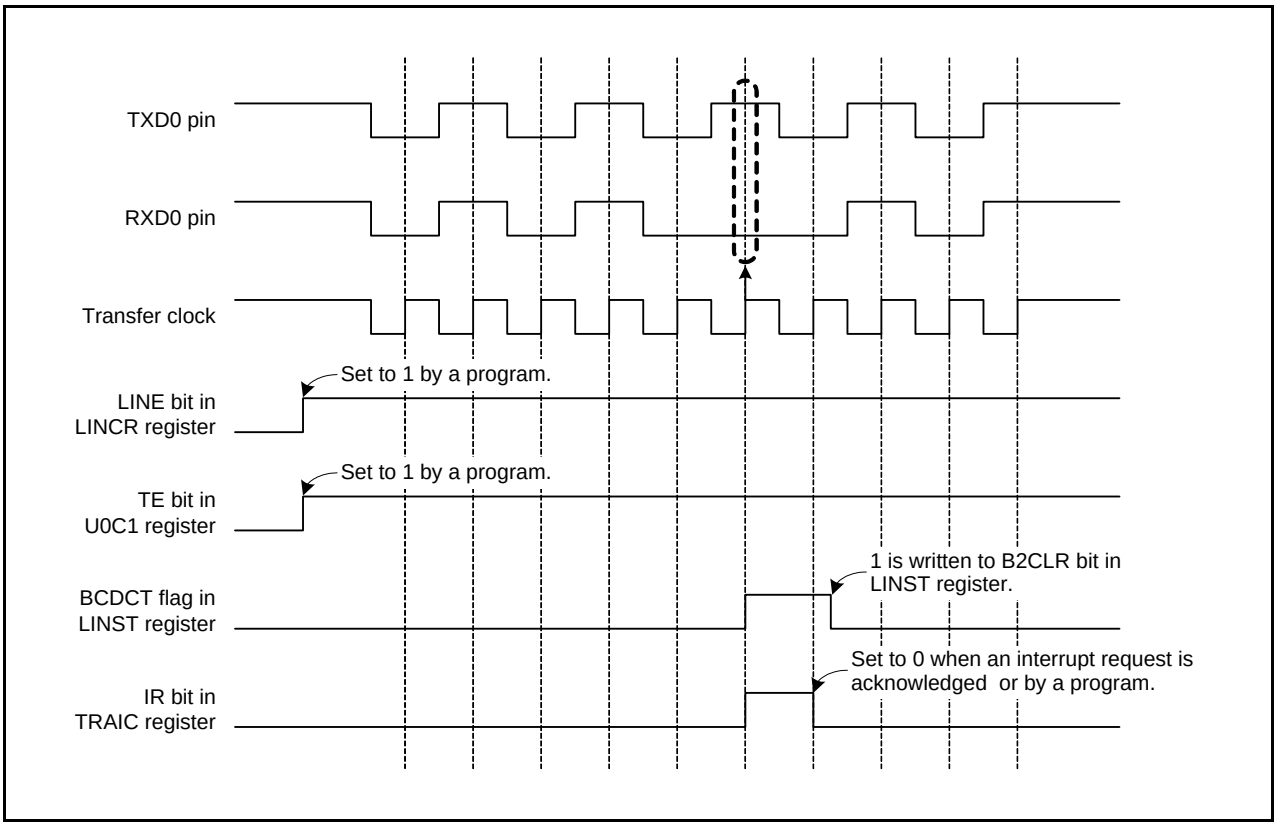


Figure 25.9 Operating Example When Bus Collision is Detected

25.4.4 Hardware LIN End Processing

Figure 25.10 shows an Example of Hardware LIN Communication Completion Flowchart.
Use the following timing for hardware LIN end processing:

- If the hardware bus collision detection function is used
  Perform hardware LIN end processing after checksum transmission completes.
- If the bus collision detection function is not used
  Perform hardware LIN end processing after header field transmission and reception complete.

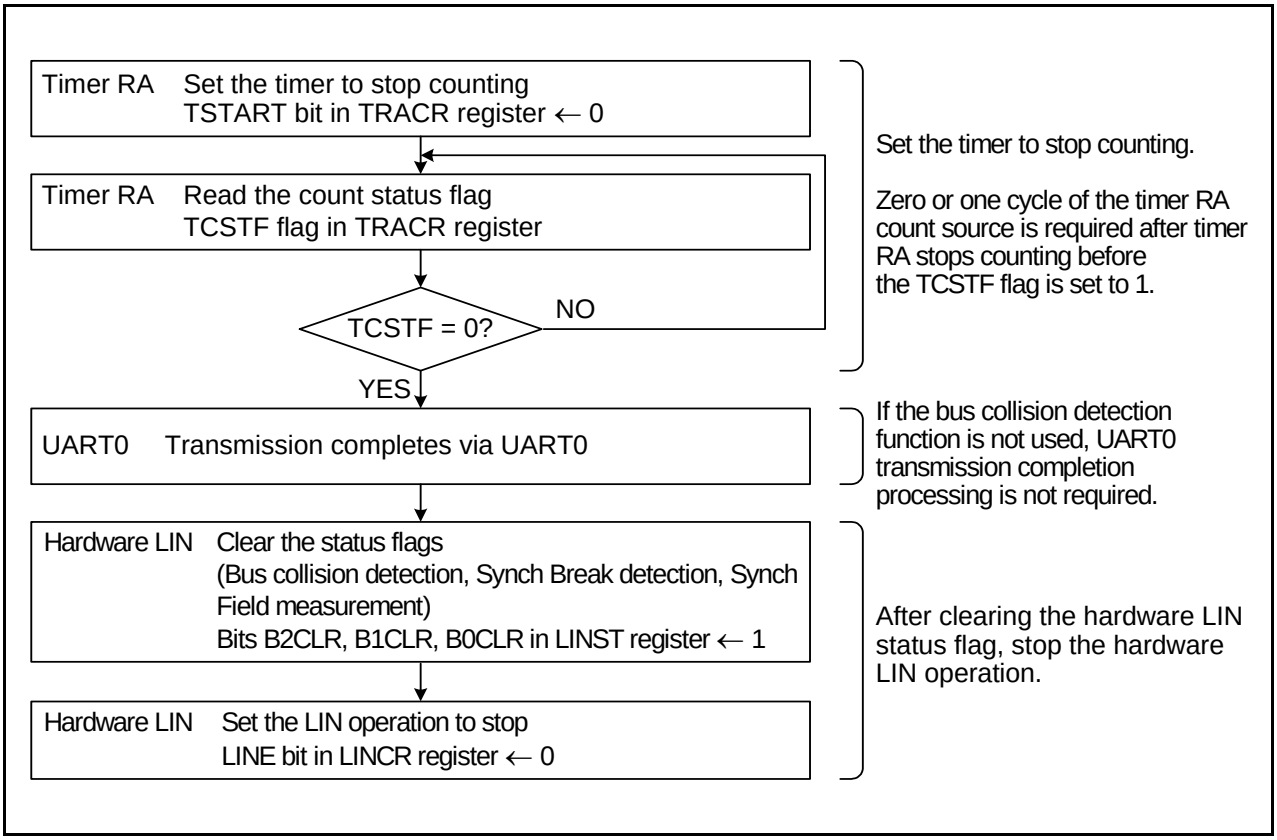


Figure 25.10 Example of Hardware LIN Communication Completion Flowchart

25.5 Interrupt Requests

There are four interrupt requests generated by the hardware LIN: Synch Break detection, Completion of Synch Break generation, Completion of Synch Field measurement, and bus collision detection. These interrupts are shared with timer RA.
Table 25.2 lists the Hardware LIN Interrupt Requests.

Table 25.2 Hardware LIN Interrupt Requests

Interrupt Request	Status Flag	Interrupt Source
Synch Break detection	SBDCT	Generated when timer RA underflows after the “L” level duration for the RXD0 input is measured, or when a “L” level is input for a duration longer than the Synch Break period during communication.
Completion of Synch Break generation		Generated when a “L” level output to TXD0 for the duration set by timer RA is completed.
Completion of Synch Field measurement	SFDCT	Generated when measurement for 6 bits of the Lynch Field by timer RA is completed.
Bus collision detection	BCDCT	Generated when the RXD0 input and TXD0 output values are different at data latch timing while UART0 is enabled for transmission.

25.6 Notes on Hardware LIN

For the time-out processing of the header and response fields, use another timer to measure the duration of time with a Synch Break detection interrupt as the starting point.

26. USB 2.0 Host/Function Module (USB)

Note

The description offered in this chapter is based on the R8C/3MK Group.
For R8C/3MU Group, refer to **1.1.2 Differences between Groups**.

26.1 Overview

R8C/3MK Group provides one port of USB2.0 host/function module (USB).
The USB is a USB controller which provides capabilities as a USB host controller and a USB function controller. The USB supports full-speed transfer defined by the USB (universal serial bus) Specifications 2.0 when used as the host controller, and supports control transfer, bulk transfer, and interrupt transfer when used as the function controller. Also, the USB has a USB transceiver and supports all of the transfer types defined by the USB Specifications.
The USB has buffer memory for data transfer, providing a maximum of five pipes. Any endpoint numbers can be assigned to PIPE4 to PIPE7, based on the peripheral devices or user system for communication.
Table 26.1 shows the USB Specifications.

Table 26.1 USB Specifications

Item	Specifications
Features	• USB Device Controller (UDC) and transceiver for USB2.0 are incorporated. • The USB host controller and USB function controller are incorporated (can be switched by software). • Self-power mode or bus-power mode can be selected. (1) Features of the USB host controller • Full-speed transfer (12 Mbps) is supported • Automatic scheduling for SOF and packet transmissions • Programmable intervals for interrupt transfers (2) Features of the USB function controller • Full-speed transfer (12 Mbps) is supported • Control transfer stage control function • Device state control function • Auto response function for SET_ADDRESS request • SOF interpolation function
Communication data transfer type	• Control transfer • Bulk transfer • Interrupt transfer
Pipe configuration	• Buffer memory for USB communications is provided. • Up to five pipes can be selected (including the default control pipe). • Usable pipe numbers are 0, 4, 5, 6, and 7. • Endpoint numbers can be assigned flexibly to PIPE4 to PIPE7. • Transfer conditions that can be set for each pipe: PIPE0: Control transfer only (default control pipe: DCP), 64 bytes (single buffer) • PIPE4 and PIPE5: Bulk transfer only Buffer size: 64 bytes (double buffer can be specified) • PIPE6 and PIPE7: Interrupt transfer only Buffer size: 64 bytes (single buffer)
Others	• Reception ending function using transaction count • Function that changes the BRDY interrupt event notification timing (BFRE) • NAK setting function for response PID generated by end of transfer (SHTNAK)

Figure 26.1 shows the USB Block Diagram.

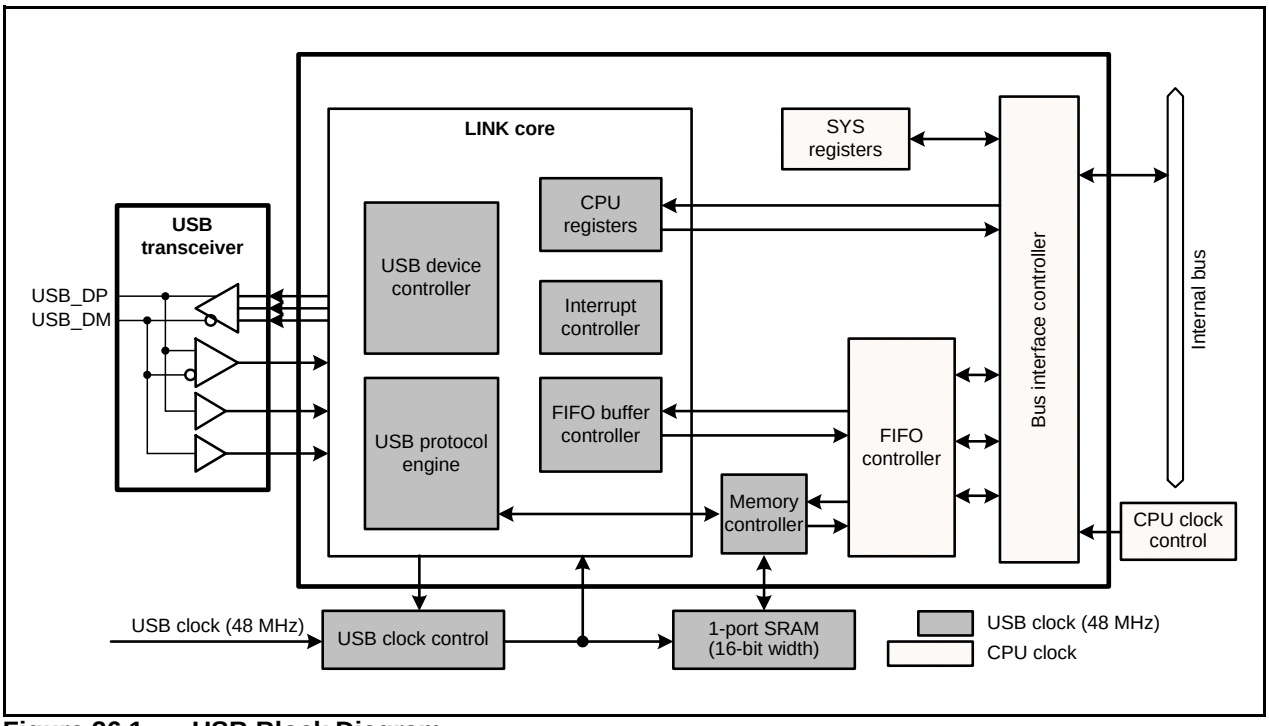


Figure 26.1 USB Block Diagram

Table 26.2 shows the USB I/O Pins.

Table 26.2 USB I/O Pins

Pin Name	I/O	Function
USB_DP	I/O	D+ I/O pin of the USB on-chip transceiver This pin should be connected to the D+ pin of the USB bus.
USB_DM	I/O	D– I/O pin of the USB on-chip transceiver This pin should be connected to the D– pin of the USB bus.
USB_VBUS	Input	USB cable connection monitor pin This pin should be connected to VBUS of the USB bus. Whether VBUS is connected or disconnected can be detected during operation as a function controller.
USB_VBUSEN	Output	VBUS (5 V) supply enable signal for external power supply chip
USB_OVRCURA	Input	External overcurrent detection signals should be connected to these pins.
USB_DPUPE	Output	1.5-kΩ pull-up resistor control signal for USB D+ signal during operation as a function controller
USB_VCC	Input	USB power supply pin

26.2 Registers

Table 26.3 lists the USB Registers.

Table 26.3 USB Registers

Register Name	Symbol	After Reset	Address	Access Size
System configuration control register	SYSCFG	0000h	2E01h, 2E00h	16
System configuration status register 0	SYSSTS0	XX000000b 00000X00b	2E05h, 2E04h	16
Device state control register 0	DVSTCTR0	0000h	2E09h, 2E08h	16
CFIFO port register	CFIFO	0000h	2E15h, 2E14h	8, 16
CFIFO port select register	CFIFOSEL	0000h	2E21h, 2E20h	16
CFIFO port control register	CFIFOCTR	0000h	2E23h, 2E22h	16
Interrupt enable register 0	INTENB0	0000h	2E31h, 2E30h	16
Interrupt enable register 1	INTENB1	0000h	2E33h, 2E32h	16
BRDY interrupt enable register	BRDYENB	0000h	2E37h, 2E36h	16
NRDY interrupt enable register	NRDYENB	0000h	2E39h, 2E38h	16
BEMP interrupt enable register	BEMPENB	0000h	2E3Bh, 2E3Ah	16
SOF output configuration register	SOFCFG	0000h	2E3Dh, 2E3Ch	16
Interrupt status register 0	INTSTS0	X0000000b X0000000b	2E41h, 2E40h	16
Interrupt status register 1	INTSTS1	XX0X0000b 00h	2E43h, 2E42h	16
BRDY interrupt status register	BRDYSTS	0000h	2E47h, 2E46h	16
NRDY interrupt status register	NRDYSTS	0000h	2E49h, 2E48h	16
BEMP interrupt status register	BEMPSTS	0000h	2E4Bh, 2E4Ah	16
Frame number register	FRMNUM	0000h	2E4Dh, 2E4Ch	16
USB address register	USBADDR	0000h	2E51h, 2E50h	16
USB request type register	USBREQ	0000h	2E55h, 2E54h	16
USB request value register	USBVAL	0000h	2E57h, 2E56h	16
USB request index register	USBINDX	0000h	2E59h, 2E58h	16
USB request length register	USBLENG	0000h	2E5Bh, 2E5Ah	16
DCP configuration register	DCPCFG	0000h	2E5Dh, 2E5Ch	16
DCP maximum packet size register	DCPMAXP	0040h	2E5Fh, 2E5Eh	16
DCP control register	DCPCTR	0000h	2E61h, 2E60h	16
Pipe window select register	PIPESEL	0000h	2E65h, 2E64h	16
Pipe configuration register	PIPECFG	0000h	2E69h, 2E68h	16
Pipe maximum packet size register	PIPEMAXP	0000h/0040h (1)	2E6Dh, 2E6Ch	16
Pipe cycle control register	PIPEPERI	0000h	2E6Fh, 2E6Eh	16
Pipe 4 control register	PIPE4CTR	0000h	2E77h, 2E76h	16
Pipe 5 control register	PIPE5CTR	0000h	2E79h, 2E78h	16
Pipe 6 control register	PIPE6CTR	0000h	2E7Bh, 2E7Ah	16
Pipe 7 control register	PIPE7CTR	0000h	2E7Dh, 2E7Ch	16
Pipe 4 transaction counter enable register	PIPE4TRE	0000h	2E9Dh, 2E9Ch	16
Pipe 4 transaction counter register	PIPE4TRN	0000h	2E9Fh, 2E9Eh	16
Pipe 5 transaction counter enable register	PIPE5TRE	0000h	2EA1h, 2EA0h	16
Pipe 5 transaction counter register	PIPE5TRN	0000h	2EA3h, 2EA2h	16
Device address 0 configuration register	DEVADD0	0000h	2ED1h, 2ED0h	16
Device address 1 configuration register	DEVADD1	0000h	2ED3h, 2ED2h	16
Device address 2 configuration register	DEVADD2	0000h	2ED5h, 2ED4h	16
Device address 3 configuration register	DEVADD3	0000h	2ED7h, 2ED6h	16
Device address 4 configuration register	DEVADD4	0000h	2ED9h, 2ED8h	16
Device address 5 configuration register	DEVADD5	0000h	2EDBh, 2EDAh	16
USB module control register	USBMC	00X10000b	2F00h	8

Note:
1. The initial value of this register differs according to the setting of the PIPESEL.PIPESEL[3:0] bits. The initial value is 0000h when the pipe is not selected and 0040h when selected.

26.2.1 System Configuration Control Register (SYSCFG)

Address 2E01h, 2E00h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	DCFM	—	DPRPU	—	—	—	USBE
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	SCKE	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	USBE	USB Module Operation Enable	0: USB module operation is disabled. 1: USB module operation is enabled.	R/W
b3 to b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	DPRPU	D+ Line Resistor Control	0: Pulling up the line is disabled. 1: Pulling up the line is enabled.	R/W
b5	—	Reserved bit	Set to 0.	R/W
b6	DCFM	Controller Function Select	0: Function controller function is selected. 1: Host controller function is selected.	R/W
b9 to b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b10	SCKE	USB Module Clock Enable	0: Stops supplying the clock signal to the USB module. 1: Enables supplying the clock signal to the USB module.	R/W
b15 to b11	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

SYSCFG selects the host controller function or function controller function, controls the USB_DP and USB_DM pins, and enables operation of the USB module.

USBE Bit (USB Module Operation Enable)

The USBE bit enables or disables operation of the USB module.
Modifying the USBE bit from 1 to 0 initializes some register bits as listed in Table 26.4 and Table 26.5.
This bit should be modified while the SYSCFG.SCKE bit is 1.
When the host controller function is selected, this bit should be set to 1 after setting the SYSCFG.DRPD bit to 1, eliminating LNST bit chattering, and checking that the USB bus state has been settled.

DPRPU Bit (D+ Line Resistor Control)

The DPRPU bit enables or disables pulling up the D+ line when the function controller function is selected.
When the DPRPU bit is set to 1 while the function controller function is selected, the USB module asserts the USB_DPUPE pin to notify the USB host of connection.
Setting the DPRPU bit to 1 when the function controller function is selected allows the USB module to assert the USB_DPUPE pin, thus notifying the USB host of connection. Modifying the DPRPU bit from 1 to 0 allows the USB module to negate the USB_DPUPE pin, thus notifying the USB host of disconnection.
This bit should be set to 1 if the function controller function is selected, and should be set to 0 if the host controller function is selected.

DCFM Bit (Controller Function Select)

The DCFM bit selects the function of the USB module.
This bit should be modified while the SYSCFG.DPRPU bit is 0.

SCKE Bit (USB Module Clock Enable)

The SCKE bit stops or enables supplying 48-MHz clock signals to the USB module.
When this bit is 0, only SYSCFG can be read from and written to; the other registers in the USB module cannot be read from or written to.

Table 26.4 Registers Initialized by Writing SYSCFG.USBE = 0 (When Function Controller Function is Selected)

Register	Symbol	Remarks
SYSSTS0	LNST	The value is retained when the host controller function is selected.
DVSTCTR0	RHST	
INTSTS0	DVSQ	The value is retained when the host controller function is selected.
USBADDR	USBADDR	The value is retained when the host controller function is selected.
USBREQ	BREQUEST, BMREQUESTTYPE	The value is retained when the host controller function is selected.
USBVAL	WVALUE	The value is retained when the host controller function is selected.
USBINDX	WINDEX	The value is retained when the host controller function is selected.
USBLENG	WLENGTH	The value is retained when the host controller function is selected.

Table 26.5 Registers Initialized by Writing SYSCFG.USBE = 0 (When Host Controller Function is Selected)

Register	Symbol	Remarks
DVSTCTR0	RHST	
FRMNUM	FRNM	The value is retained when the function controller function is selected.

26.2.2 System Configuration Status Register 0 (SYSSTS0)

Address 2E05h, 2E04h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	HTACT	—	—	—	—	LNST[1:0]	
After Reset	0	0	0	0	0	X	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	OVCMON1	—	—	—	—	—	—	—
After Reset	X	X	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b1, b0	LNST[1:0]	USB Data Line Status Monitor	Indicates the status of the USB data bus lines (D+ and D-) as shown in Table 26.6.	R
b2	—	Reserved bit	When read, the content is undefined.	R
b4, b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—	Reserved bit	When read, the content is undefined.	R
b6	HTACT	USB Host Sequencer Status Monitor	0: Host sequencer of the USB module is completely stopped. 1: Host sequencer of the USB module is not completely stopped.	R
b13 to b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b14	—	Reserved bit	When read, the content is undefined.	R
b15	OVCMON1	External USB_OVRCURA Input Pin Monitor	The OVCMON1 bit indicates the status of the USB_OVRCURA pin. When read, the content is undefined.	R

SYSSTS0 monitors the line status (D+ and D- lines) of the USB data bus.

LNST[1:0] Bits (USB Data Line Status Monitor)

The LNST[1:0] bits should be read after the connection processing (SYSCFG.DPRPU = 1 is set) when the function controller function is selected.

Table 26.6 USB Data Bus Line Status

LNST[1]	LNST[0]	Status
0	0	SE0
0	1	J-state
1	0	K-state
1	1	SE1

HTACT Bit (USB Host Sequencer Status Monitor)

The HTACT bit is 0 when the host sequencer of the USB module is completely stopped.
Make sure the HTACT bit is 0 when stopping the clock supply to the USB module.

OVCMON1 Bits (External USB_OVRCURA Input Pin Monitor)

The OCVMON[1:0] bits indicate the status of overcurrent from an external power-supply chip.

26.2.3 Device State Control Register 0 (DVSTCTR0)

Address 2E09h, 2E08h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	RWUPE	USBRST	RESUME	UACT	—	RHST[2:0]		
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	VBUSEN	WKUP
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b2 to b0	RHST[2:0]	USB Bus Reset Status	• When the host controller function is selected b2 b1 b0 0 0 0: Communication speed not determined (powered state or no connection) 1 x x: USB bus reset in progress 0 0 1: Low-speed connection (1) 0 1 0: Full-speed connection [Legend] x: Don't care • When the function controller function is selected b2 b1 b0 0 0 0: Communication speed not determined 1 0 0: USB bus reset in progress 0 1 0: Full-speed connection	R
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	UACT	USB Bus Enable	0: Downstream port is disabled (SOF transmission is disabled). 1: Downstream port is enabled (SOF transmission is enabled).	R/W
b5	RESUME	Resume Output	0: Resume signal is not output. 1: Resume signal is output.	R/W
b6	USBRST	USB Bus Reset Output	0: USB bus reset signal is not output. 1: USB bus reset signal is output.	R/W
b7	RWUPE	Wakeup Detection Enable	0: Downstream port wakeup is disabled. 1: Downstream port wakeup is enabled.	R/W
b8	WKUP	Wakeup Output	0: Remote wakeup signal is not output. 1: Remote wakeup signal is output.	R/W (2)
b9	VBUSEN	USB_VBUSEN Output Pin Control	The VBUSEN bit value is output as the status of the external USB_VBUSEN pin without change.	R/W
b10	—	Reserved bits	Set to 0.	R/W
b11	—			
b14 to b12	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b15	—	Reserved bit	Set to 0.	R/W

Notes:
1. The USB controller does not support communication with a low-speed device. When this value is read, abnormal connection processing should be executed in a higher application.
2. Only 1 can be written.

DVSTCTR0 controls and confirms the state of the USB data bus.

RHST[2:0] Bits (USB Bus Reset Status)

The RHST[2:0] bits indicate the status of the USB bus reset.
When the host controller function is selected, the RHST[2:0] bits indicate 100b after software has written 1 to the USBRST bit.
The USB module fixes the value of the RHST[2:0] bits when software writes 0 to the USBRST bit and the USB module completes SE0 driving.
When the function controller function is selected, a DVST interrupt is generated as soon as the USB module detects the USB bus reset and then the RHST[2:0] bits are fixed to 010b.

UACT Bit (USB Bus Enable)

The UACT bit enables operation of the USB bus (controls the SOF packet transmission to the USB bus) when the host controller function is selected.
With this bit set to 1, the USB module puts the USB port to the USB-bus enabled state and performs SOF output and data transmission and reception.
This module starts outputting SOF packets within one frame after software has written 1 to the UACT bit.
With this bit set to 0, the USB module enters the idle state after outputting SOF packets.
The USB module sets the UACT bit to 0 on any of the following conditions.
- A DTCH interrupt is detected during communication (while UACT = 1).
- An EOFERR interrupt is detected during communication (while UACT = 1).

Writing 1 to this bit should be done at the end of the USB reset processing (writing 0 to the USBRST bit) or at the end of the resume processing from the suspended state (writing 0 to the RESUME bit).
This bit should be set to 0 if the function controller function is selected.

RESUME Bit (Resume Output)

The RESUME bit controls the resume signal output when the host controller function is selected.
Setting the RESUME bit to 1 allows the USB module to drive the port to the K-state and output the resume signal.
The USB module continues outputting K-state while RESUME = 1 (until software sets the RESUME bit to 0).
The RESUME bit should be 1 (= resume period) for the time defined by the USB Specifications 2.0.
This bit should be set to 1 in the suspended state.
Write 1 to the UACT bit simultaneously with the end of the resume processing (writing 0 to the RESUME bit).
This bit should be set to 0 if the function controller function is selected.

USBRST Bit (USB Bus Reset Output)

The USBRST bit controls the USB bus reset signal output when the host controller function is selected.
When the host controller function is selected, setting this bit to 1 allows the USB module to drive SE0 of the USB port to reset the USB bus.
The USB module continues outputting SE0 while USBRST = 1 (until software sets the USBRST bit to 0). The USBRST bit should be 1 (= USB bus reset period) for the time defined by the USB Specifications 2.0.
Writing 1 to this bit during communication (UACT = 1) or during the resume processing (RESUME = 1) prevents the USB module from starting the USB bus reset processing until both the UACT and RESUME bits become 0.
Write 1 to the UACT bit simultaneously with the end of the USB bus reset processing (writing 0 to the USBRST bit).
This bit should be set to 0 if the function controller function is selected.

RWUPE Bit (Wakeup Detection Enable)

The RWUPE bit enables or disables the downstream port peripheral device to use the remote wakeup function (resume signal output) when the host controller function is selected.
With this bit set to 1, on detecting the remote wakeup signal, the USB module detects the resume signal (K-state for 2.5 μs) from the downstream port device and performs the resume processing (drives the port to the K-state).
With this bit set to 0, the USB module ignores the detected remote wakeup signal (K-state) from the peripheral device connected to the USB port.
While the PWUPE bit is 1, the internal clock should not be stopped even in the suspended state (SCKE should be set to 1).
This bit should be set to 0 if the function controller function is selected.

WKUP Bit (Wakeup Output)

The WKUP bit enables or disables outputting the remote wakeup signal (resume signal) to the USB bus when the function controller function is selected.
The USB module controls the output time of a remote wakeup signal. When this bit is set to 1, the USB module clears this bit to 0 after outputting the 10-ms K-state.
According to the USB Specifications, the USB bus idle state must be kept for 5 ms or longer before a remote wakeup signal is sent. If the USB module writes 1 to this bit right after detection of the suspended state, the K-state will be output after 2 ms.
Do not write 1 to this bit, unless the device state is in the suspended state (INTSTS0.DVSQ bit = 1xx) and the USB host enables the remote wakeup signal. When this bit is set to 1, the internal clock must not be stopped even in the suspended state (write 1 to this bit while SYSCFG.SCKE = 1).
This bit should be set to 0 if the host controller function is selected.

26.2.4 CFIFO Port Register (CFIFO)

Address 2E15h, 2E14h

Bit	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	FIFOPORT [15:0]															
After Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b15 to b0	FIFOPORT [15:0]	FIFO Port	The valid bits in a FIFO port register depend on the settings of the corresponding MBW and BIGEND bits as shown in Table 26.7 and Table 26.8	R/W

CFIFO is a port register that is used to read data from the FIFO buffer memory and write data to the FIFO buffer memory.
The FIFO port is configured of a FIFO port register (CFIFO) that handles reading of data from the FIFO buffer memory and writing of data to the FIFO buffer memory, a select register (CFIFOSEL) that is used to select the pipe assigned to the FIFO port, and a control register (CFIFOCTR).
The FIFO port has the following features.

- The FIFO buffer for DCP (control transfer) should be accessed through the CFIFO port.
- When using functions specific to the FIFO port, the pipe number (selected pipe) specified by the CURPIPE bits cannot be changed.
- There are two FIFO buffer states: the access right is on the CPU side and it is on the SIE side. When the FIFO buffer access right is on the SIE side, the FIFO buffer cannot be accessed from the CPU.

[FIFOPORT15 to FIFOPORT0] (FIFO Port)

Accessing the FIFOPORT bits allow reading the received data from the FIFO buffer or writing the transmit data to the FIFO buffer.
The FIFO port register can be accessed only while the FRDY bit in the control register (CFIFOCTR) is 1.
The valid bits in the FIFO port register depend on the settings of the corresponding MBW and BIGEND bits as shown in Table 26.7 and Table 26.8.

Table 26.7 Endian Operation in 16-Bit Access

CFIFOSEL.BIGEND Bit	Bits 15 to 8	Bits 7 to 0
0	N + 1 data	N + 0 data
1	N + 0 data	N + 1 data

Table 26.8 Endian Operation in 8-Bit Access

CFIFOSEL.BIGEND Bit	Bits 15 to 8	Bits 7 to 0
x (Setting is invalid)	Access prohibited (1)	N + 0 data

Note:
1. Accessing an access-prohibited area to read data is not allowed.

26.2.5 CFIFO Port Select Register (CFIFOSEL)

Address 2E21h, 2E20h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	ISEL	—	CURPIPE [3:0]			
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	RCNT	REW	—	—	—	MBW	—	BIGEND
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b3 to b0	CURPIPE [3:0]	CFIFO Port Access Pipe Specification	b3 b2 b1 b0 0 0 0 0: DCP (Default control pipe) 0 1 0 0: Pipe 4 0 1 0 1: Pipe 5 0 1 1 0: Pipe 6 0 1 1 1: Pipe 7 Other than above: Do not set.	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	ISEL	CFIFO Port Access Direction When DCP is Selected	0: Reading from the buffer memory is selected 1: Writing to the buffer memory is selected	R/W
b7, b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b8	BIGEND	CFIFO Port Endian Control	0: Little endian 1: Big endian	R/W
b9	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b10	MBW	CFIFO Port Access Bit Width	0: 8-bit width 1: 16-bit width	R/W
b13 to b11	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b14	REW	Buffer Pointer Rewind	0: The buffer pointer is not rewound. 1: The buffer pointer is rewound.	R/W (1)
b15	RCNT	Read Count Mode	0: When all of the receive data has been read from the CFIFO, 0 is written to the DTLN bit. (In double buffer mode, the DTLN bit value is cleared when all the data has been read from only a single plane.) 1: The DTLN bit is decremented each time the receive data is read from the CFIFO.	R/W

Note:
1. Only 0 can be read.

CFIFOSEL assigns the pipe to the FIFO port, and controls access to the CFIFO port.

CURPIPE[3:0] Bits (CFIFO Port Access Pipe Specification)

The CURPIPE[3:0] bits specify the pipe number using which data is read or written through the CFIFO port.
After writing to these bits, read these bits to check that the written value agrees with the read value before proceeding to the next process.
Even if an attempt is made to modify the setting of these bits during access to the FIFO buffer, the current access setting is retained until the access is completed. Then, the modification becomes effective, thus enabling continuous access.

ISEL Bit (CFIFO Port Access Direction When DCP is Selected)

After writing to the ISEL bit with the DCP being a selected pipe, read this bit to check that the written value agrees with the read value before proceeding to the next process.
Set this bit and the CURPIPE bits simultaneously.

BIGEND Bit (CFIFO Port Endian Control)

The BIGEND bit specifies the byte endian for the CFIFO port.

MBW Bit (CFIFO Port Access Bit Width)

The MBW bit specifies the bit width for accessing the CFIFO port.
When the selected pipe is in the receiving direction, once reading data is started after setting this bit, this bit should not be modified until all the data has been read.
When the selected pipe is in the receiving direction, set the CURPIPE and MBW bits simultaneously.
When the selected pipe is in the transmitting direction, the bit width cannot be changed from 8-bit width to 16-bit width while data is being written to the buffer memory.
An odd number of bytes can also be written through byte-access control even when 16-bit width is selected.

REW Bit (Buffer Pointer Rewind)

The REW bit specifies whether or not to rewind the buffer pointer.
When the selected pipe is in the receiving direction, setting the REW bit to 1 while the FIFO buffer is being read allows re-reading the FIFO buffer from the first data (in double buffer mode, re-reading the currently-read FIFO buffer plane from the first data is allowed).
Do not set the REW bit to 1 simultaneously with modifying the CURPIPE bits. Before setting the REW bit to 1, be sure to check that the FRDY bit is 1.
To re-write to the FIFO buffer again from the first data for the pipe in the transmitting direction, use the BCLR bit.

RCNT Bit (Read Count Mode)

The RCNT bit specifies the read mode for the value in the DTLN[8:0] bits in CFIFOCTR.

26.2.6 CFIFO Port Control Register (CFIFOCTR)

Address 2E23h, 2E22h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	DTLN[8:0]							
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	BVAL	BCLR	FRDY	—	—	—	—	DTLN[8:0]
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b8 to b0	DTLN[8:0]	Receive Data Length	Indicates the length of the receive data. These bits indicate different values depending on the setting of the RCNT bit in the port select register. For details, refer to the description on the DTLN[8:0] bits shown below.	R
b12 to b9	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b13	FRDY	FIFO Port Ready	0: FIFO port access is disabled. 1: FIFO port access is enabled.	R
b14	BCLR	CPU Buffer Clear	0: Invalid 1: Clears the buffer memory on the CPU side.	R/W (1)
b15	BVAL	Buffer Memory Valid Flag	0: Invalid 1: Writing ended	R/W (2)

Notes:
1. Only 0 can be read and 1 can be written.
2. Only 1 can be written.

CFIFOCTR determines whether or not writing to the buffer memory has been finished, the buffer accessed from the CPU has been cleared, and the FIFO port is accessible.

DTLN[8:0] Bits (Receive Data Length)

The DTLN[8:0] bits indicate the length of the receive data.
While the FIFO buffer is being read, the DTLN[8:0] bits indicate different values depending on the CFIFOSEL.RCNT bit value as described below.

- RCNT = 0
  The USB module sets the DTLN[8:0] bits to indicate the length of the receive data until the CPU has read all the received data from a single FIFO buffer plane.
  While PIPECFG.BFRE = 1, these bits retain the length of the receive data until the BCLR bit is set to 1 even after all the data has been read.
- RCNT = 1
  The USB module decrements the value indicated by these bits each time data is read from the FIFO buffer. (The value is decremented by one when the MBW bit is 0, and by two when the MBW bit is 1.)

The USB module sets these bits to 0 when all the data has been read from one FIFO buffer plane. However, in double buffer mode, if data has been received in one FIFO buffer plane before all the data has been read from the other plane, the USB module sets these bits to indicate the length of the receive data in the former plane when all the data has been read from the latter plane.

FRDY Bit (FIFO Port Ready)

The FRDY bit indicates whether the FIFO port can be accessed by the CPU.
In the following cases, the USB module sets the FRDY bit to 1 but data cannot be read via the FIFO port because there is no data to be read. In these cases, set the BCLR bit to 1 to clear the FIFO buffer, and enable transmission and reception of the next data.

- A zero-length packet is received when the FIFO buffer assigned to the selected pipe is empty.
- A short packet is received and the data is completely read while PIPECFG.BFRE = 1.

BCLR Bit (CPU Buffer Clear)

The BCLR bit should be set to 1 to clear the FIFO buffer on the CPU side for the selected pipe.
When double buffer mode is set for the FIFO buffer assigned to the selected pipe, the USB module clears only one plane of the FIFO buffer even when both planes are read-enabled.
When the selected pipe is the DCP, setting the BCLR bit to 1 allows the USB module to clear the FIFO buffer regardless of whether the FIFO buffer is on the CPU side or SIE side. To clear the buffer on the SIE side, set the PID bits for the DCP control register to NAK before setting the BCLR bit to 1.
When the selected pipe is in the transmitting direction, if 1 is written to the BVAL and BCLR bits simultaneously, the USB module clears the data that has been written before it, enabling transmission of a zero-length packet.
When the selected pipe is not the DCP, writing 1 to the BCLR bit should be done while the FRDY bit in the FIFO port control register is 1 (set by the USB module).

BVAL Bit (Buffer Memory Valid Flag)

The BVAL bit should be set to 1 when data has been completely written to the FIFO buffer on the CPU side for the pipe selected using the CURPIPE bits (selected pipe).
When the selected pipe is in the transmitting direction, set the BVAL bit to 1 in the following cases. Then, the USB module switches the FIFO buffer from the CPU side to the SIE side, thus enabling transmission.

- To transmit a short packet, set the BVAL bit to 1 after data has been written.
- To transmit a zero-length packet, set the BVAL bit to 1 before data is written to the FIFO buffer.

When data of the maximum packet size has been written for the pipe in continuous transfer mode, the USB module sets the BVAL bit to 1 and switches the FIFO buffer from the CPU side to the SIE side, thus enabling transmission.
Writing 1 to the BVAL bit should be done while the FRDY bit is 1 (set by the USB module).
When the selected pipe is in the receiving direction, do not set the BVAL bit to 1.

26.2.7 Interrupt Enable Register 0 (INTENB0)

Address 2E31h, 2E30h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	VBSE	RSME	SOFE	DVSE	CTRE	BEMPE	NRDYE	BRDYE
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b7 to b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b8	BRDYE	Buffer Ready Interrupt Enable	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b9	NRDYE	Buffer Not Ready Response Interrupt Enable	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b10	BEMPE	Buffer Empty Interrupt Enable	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b11	CTRE	Control Transfer Stage Transition Interrupt Enable (1)	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b12	DVSE	Device State Transition Interrupt Enable (1)	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b13	SOFE	Frame Number Update Interrupt Enable	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b14	RSME	Resume Interrupt Enable (1)	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b15	VBSE	VBUS Interrupt Enable	0: Interrupt output disabled 1: Interrupt output enabled	R/W

Note:
1. The RSME, DVSE, and CTRE bits can be set to 1 only when the function controller function is selected; do not set these bits to 1 to enable the corresponding interrupt output when the host controller function is selected.

INTENB0 specifies the various interrupt masks. On detecting the interrupt corresponding to the bit in INTENB0 to which software has set 1, the USB module generates the USB interrupt.
The USB module sets 1 to each status bit in INTSTS0 when a detection condition of the corresponding interrupt source has been satisfied regardless of the setting in INTENB0 (regardless of whether the interrupt output is enabled or disabled).
While the status bit in INTSTS0 corresponding to the interrupt source indicates 1, the USB module generates the USB interrupt when software modifies the corresponding interrupt enable bit in INTENB0 from 0 to 1.

BRDYE Bit (Buffer Ready Interrupt Enable)

Enables or disables the USB interrupt output when the BRDY interrupt is detected.

NRDYE Bit (Buffer Not Ready Response Interrupt Enable)

Enables or disables the USB interrupt output when the NRDY interrupt is detected.

BEMPE Bit (Buffer Empty Interrupt Enable)

Enables or disables the USB interrupt output when the BEMP interrupt is detected.

CTRE Bit (Control Transfer Stage Transition Interrupt Enable)

Enables or disables the USB interrupt output when the CTRT interrupt is detected.

DVSE Bit (Device State Transition Interrupt Enable)

Enables or disables the USB interrupt output when the DVST interrupt is detected.

SOFE Bit (Frame Number Update Interrupt Enable)

Enables or disables the USB interrupt output when the SOFR interrupt is detected.

RSME Bit (Resume Interrupt Enable)

Enables or disables the USB interrupt output when the RESM interrupt is detected.

VBSE Bit (VBUS Interrupt Enable)

Enables or disables the USB interrupt output when the VBINT interrupt is detected.
Set the VBINT bit in interrupt status register 0 (INTSYS0) to 0 before setting this bit to 1.

26.2.8 Interrupt Enable Register 1 (INTENB1)

Address 2E33h, 2E32h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	EOFERRE	SIGNE	SACKE	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	OVRCRE	BCHGE	—	DTCHE	ATTCHE	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b3 to b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	SACKE	Setup Transaction Normal Response Interrupt Enable	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b5	SIGNE	Setup Transaction Error Interrupt Enable	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b6	EOFERRE	EOF Error Detection Interrupt Enable	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b10 to b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b11	ATTCHE	Connection Detection Interrupt Enable	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b12	DTCHE	Disconnection Detection Interrupt Enable	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b13	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b14	BCHGE	USB Bus Change Interrupt Enable	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b15	OVRCRE	Overcurrent Input Change Interrupt Enable	0: Interrupt output disabled 1: Interrupt output enabled	R/W

Note:

1. The bits in INTENB1 can be set to 1 only when the host controller function is selected; do not set these bits to 1 to enable the corresponding interrupt output when the function controller function is selected.

INTENB1 specifies the various interrupt masks when the host controller function is selected. INTENB1 also specifies the interrupt mask for the setup transaction.
On detecting the interrupt corresponding to the bit in INTENB1 to which software has set 1, the USB module generates the USB interrupt.
The USB module sets 1 to each status bit in INTSTS1 when a detection condition of the corresponding interrupt source has been satisfied regardless of the setting in INTENB1 (regardless of whether the interrupt output is enabled or disabled).
While the status bit in INTSTS1 corresponding to the interrupt source indicates 1, the USB module generates the USB interrupt when software modifies the corresponding interrupt enable bit in INTENB1 from 0 to 1.
If operation as a USB-function controller has been selected, do not make any of the interrupt-enabling settings in INTENB1.

SACKE Bit (Setup Transaction Normal Response Interrupt Enable)

Enables or disables the USB interrupt output when the SACK interrupt is detected.

SIGNE Bit (Setup Transaction Error Interrupt Enable)

Enables or disables the USB interrupt output when the SIGN interrupt is detected.

EOFERRE Bit (EOF Error Detection Interrupt Enable)

Enables or disables the USB interrupt output when the EOFERR interrupt is detected.

ATTCHE Bit (Connection Detection Interrupt Enable)

Enables or disables the USB interrupt output when the ATTCH interrupt is detected.

DTCHE Bit (Disconnection Detection Interrupt Enable)

Enables or disables the USB interrupt output when the DTCH interrupt is detected.

BCHGE Bit (USB Bus Change Interrupt Enable)

Enables or disables the USB interrupt output when the BCHG interrupt is detected.

OVRCRE Bit (Overcurrent Input Change Interrupt Enable)

Enables or disables the USB interrupt output when the OVRCR interrupt is detected.

26.2.9 BRDY Interrupt Enable Register (BRDYENB)

Address 2E37h, 2E36h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PIPE7 BRDYE	PIPE6 BRDYE	PIPE5 BRDYE	PIPE4 BRDYE	—	—	—	PIPE0 BRDYE
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PIPE0 BRDYE	BRDY Interrupt Enable for PIPE0	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b1	—	Reserved bits	Set to 0.	R/W
b2	—			
b3	—			
b4	PIPE4 BRDYE	BRDY Interrupt Enable for PIPE4	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b5	PIPE5 BRDYE	BRDY Interrupt Enable for PIPE5	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b6	PIPE6 BRDYE	BRDY Interrupt Enable for PIPE6	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b7	PIPE7 BRDYE	BRDY Interrupt Enable for PIPE7	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b8	—	Reserved bits	Set to 0.	R/W
b9	—			
b15 to b10	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

BRDYENB enables or disables the BRDY bit in INTSTS0 to be set to 1 when the BRDY interrupt is detected for each pipe.

On detecting the BRDY interrupt for the pipe corresponding to the bit in BRDYENB to which software has set 1, the USB module sets 1 to the corresponding PIPEBRDY bit in BRDYSTS and the BRDY bit in INTSTS0, and generates the BRDY interrupt.

While at least one PIPEBRDY bit in BRDYSTS indicates 1, the USB module generates the BRDY interrupt when software modifies the corresponding interrupt enable bit in BRDYENB from 0 to 1.

26.2.10 NRDY Interrupt Enable Register (NRDYENB)

Address 2E39h, 2E38h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PIPE7 NRDYE	PIPE6 NRDYE	PIPE5 NRDYE	PIPE4 NRDYE	—	—	—	PIPE0 NRDYE
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PIPE0 NRDYE	NRDY Interrupt Enable for PIPE0	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b1	—	Reserved bits	Set to 0.	R/W
b2	—			
b3	—			
b4	PIPE4 NRDYE	NRDY Interrupt Enable for PIPE4	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b5	PIPE5 NRDYE	NRDY Interrupt Enable for PIPE5	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b6	PIPE6 NRDYE	NRDY Interrupt Enable for PIPE6	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b7	PIPE7 NRDYE	NRDY Interrupt Enable for PIPE7	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b8	—	Reserved bits	Set to 0.	R/W
b9	—			
b15 to b10	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NRDYENB enables or disables the NRDY bit in INTSTS0 to be set to 1 when the NRDY interrupt is detected for each pipe.

On detecting the NRDY interrupt for the pipe corresponding to the bit in NRDYENB to which software has set 1, the USB module sets 1 to the corresponding PIPENRDY bit in NRDYSTS and the NRDY bit in INTSTS0, and generates the NRDY interrupt.

While at least one PIPENRDY bit in NRDYSTS indicates 1, the USB module generates the NRDY interrupt when software modifies the corresponding interrupt enable bit in NRDYENB from 0 to 1.

26.2.11 BEMP Interrupt Enable Register (BEMPENB)

Address 2E3Bh, 2E3Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PIPE7 BEMPE	PIPE6 BEMPE	PIPE5 BEMPE	PIPE4 BEMPE	—	—	—	PIPE0 BEMPE
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PIPE0 BEMPE	BEMP Interrupt Enable for PIPE0	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b1	—	Reserved bits	Set to 0.	R/W
b2	—			
b3	—			
b4	PIPE4 BEMPE	BEMP Interrupt Enable for PIPE4	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b5	PIPE5 BEMPE	BEMP Interrupt Enable for PIPE5	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b6	PIPE6 BEMPE	BEMP Interrupt Enable for PIPE6	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b7	PIPE7 BEMPE	BEMP Interrupt Enable for PIPE7	0: Interrupt output disabled 1: Interrupt output enabled	R/W
b8	—	Reserved bits	Set to 0.	R/W
b9	—			
b15 to b10	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

BEMPENB enables or disables the BEMP bit in INTSTS0 to be set to 1 when the BEMP interrupt is detected for each pipe.

On detecting the BEMP interrupt for the pipe corresponding to the bit in BEMPENB to which software has set 1, the USB module sets 1 to the corresponding PIPEBEMP bit in BEMPSTS and the BEMP bit in INTSTS0, and generates the BEMP interrupt.

While at least one PIPEBEMP bit in BEMPSTS indicates 1, the USB module generates the BEMP interrupt when software modifies the corresponding interrupt enable bit in BEMPENB from 0 to 1.

26.2.12 SOF Output Configuration Register (SOFCFG)

Address 2E3Dh, 2E3Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	BRDYM	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b3 to b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—	Reserved bit	When read, the content is undefined.	R
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b6	BRDYM	BRDY Interrupt Status Clear Timing for each Pipe	0: Software clears the status. 1: The USB module clears the status when data has been read from the FIFO buffer or data has been written to the FIFO buffer.	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b8	—	Reserved bit	Set to 0.	R/W
b15 to b9	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

SOFCFG specifies the BRDY interrupt status clear timing.

BRDYM Bit (BRDY Interrupt Status Clear Timing for each Pipe)

The BRDYM bit specifies the timing for clearing the BRDY interrupt status for each pipe.

26.2.13 Interrupt Status Register 0 (INTSTS0)

Address 2E41h, 2E40h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	VBSTS	DVSQ[2:0]			VALID	CTSQ[2:0]		
After Reset	X (3)	0	0	0/1 (2)	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	VBINT	RESM	SOFR	DVST	CTRT	BEMP	NRDY	BRDY
After Reset	X	0	0	0 (1)	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b2 to b0	CTSQ[2:0]	Control Transfer Stage	b2 b1 b0 0 0 0: Idle or setup stage 0 0 1: Control read data stage 0 1 0: Control read status stage 0 1 1: Control write data stage 1 0 0: Control write status stage 1 0 1: Control write (no data) status stage 1 1 0: Control transfer sequence error 1 1 1: Do not set.	R
b3	VALID	USB Request Reception	0: Not detected 1: Setup packet reception	R/W (1)
b6 to b4	DVSQ[2:0]	Device State	b6 b5 b4 0 0 0: Powered state 0 0 1: Default state 0 1 0: Address state 0 1 1: Configured state 1 x x: Suspended state [Legend] x: Don't care	R
b7	VBSTS	VBUS Input Status	0: USB_VBUS pin is low. 1: USB_VBUS pin is high.	R
b8	BRDY	Buffer Ready Interrupt Status	0: BRDY interrupts are not generated. 1: BRDY interrupts are generated.	R
b9	NRDY	Buffer Not Ready Interrupt Status	0: NRDY interrupts are not generated. 1: NRDY interrupts are generated.	R
b10	BEMP	Buffer Empty Interrupt Status	0: BEMP interrupts are not generated. 1: BEMP interrupts are generated.	R
b11	CTRT	Control Transfer Stage Transition Interrupt Status (3)	0: Control transfer stage transition interrupts are not generated. 1: Control transfer stage transition interrupts are generated.	R/W (1)
b12	DVST	Device State Transition Interrupt Status (3)	0: Device state transition interrupts are not generated. 1: Device state transition interrupts are generated.	R/W (1)
b13	SOFR	Frame Number Refresh Interrupt Status	0: SOF interrupts are not generated. 1: SOF interrupts are generated. (1) When the host controller function is selected The USB module sets the SOFR bit to 1 on updating the frame number when software has set the UACT bit to 1. (A SOFR interrupt is detected every 1 ms.) (2) When the function controller function is selected The USB module sets the SOFR bit to 1 on updating the frame number. (A SOFR interrupt is detected every 1 ms.) The USB module can detect an SOFR interrupt through the internal interpolation function even when a damaged SOF packet is received from the USB host.	R/W (1)
b14	RESM	Resume Interrupt Status (2, 3)	0: Resume interrupts are not generated. 1: Resume interrupts are generated.	R/W (1)
b15	VBINT	VBUS Interrupt Status (2)	0: VBUS interrupts are not generated. 1: VBUS interrupts are generated.	R/W (1)

Notes:
1. To clear the VBINT, RESM, SOFR, DVST, CTRT, or VALID bit, write 0 only to the bits to be cleared; write 1 to the other bits. Do not write 0 to the status bits indicating 0.
2. A change in the status indicated by the VBINT and RESM bits can be detected even while the clock supply is stopped (SCKE = 0), and the interrupts are output when the corresponding interrupt enable bits are enabled. Clearing the status through software should be done after enabling the clock supply.
3. A change in the status of the RESM, DVST, and CTRT bits occur only when the function controller function is selected; disable the corresponding interrupt enable bits (set to 0) when the host controller function is selected.

INTSTS0 indicates the status of the various interrupts detected.
The DVSQ[2:0] bits are initialized to 001b and the DVST bit is initialized to 1b by a USB bus reset.

CTSQ[2:0] Bits (Control Transfer Stage)

When the host controller function is selected, the read value is invalid.

VALID Bit (USB Request Reception)

When the host controller function is selected, the read value is invalid.

DVSQ[2:0] Bits (Device State)

When the host controller function is selected, the read value is invalid.

BRDY Bit (Buffer Ready Interrupt Status)

Indicates the BRDY interrupt status.
The USB module sets the BRDY bit to 1 when at least one PIPEBRDY bit in BRDYSTS is set to 1 among the PIPEnBRDY bits corresponding to the PIPEBRDYE bits in BRDYENB to which 1 has been set (when the USB module detects the BRDY interrupt status in at least one pipe among the pipes for which software enables the BRDY interrupt output).
For the conditions for PIPEBRDY status assertion, refer to **26.3.3.1 BRDY Interrupt**.
The USB module clears the BRDY bit to 0 when software writes 0 to all the PIPEnBRDY bits corresponding to the PIPEBRDYE bits to which 1 has been set.
The BRDY bit cannot be cleared to 0 even if software writes 0 to this bit.

NRDY Bit (Buffer Not Ready Interrupt Status)

The USB module sets the NRDY bit to 1 when at least one PIPENRDY bit in NRDYSTS is set to 1 among the PIPENRDY bits corresponding to the PIPENRDYE bits in NRDYENB to which 1 has been set (when the USB module detects the NRDY interrupt status in at least one pipe among the pipes for which software enables the NRDY interrupt output).
For the conditions for PIPENRDY status assertion, refer to **26.3.3.2 NRDY Interrupt**.
The USB module clears the NRDY bit to 0 when software writes 0 to all the PIPENRDY bits corresponding to the PIPENRDYE bits to which 1 has been set.
The NRDY bit cannot be cleared to 0 even if software writes 0 to this bit.

BEMP Bit (Buffer Empty Interrupt Status)

The USB module sets the BEMP bit to 1 when at least one PIPEBEMP bit in BEMPSTS is set to 1 among the PIPEBEMP bits corresponding to the PIPEBEMPE bits in BEMPENB to which 1 has been set (when the USB module detects the BEMP interrupt status in at least one pipe among the pipes for which software enables the BEMP interrupt output).
For the conditions for PIPEBEMP status assertion, refer to **26.3.3.3 BEMP Interrupt**.
The USB module clears the BEMP bit to 0 when software writes 0 to all the PIPEBEMP bits corresponding to the PIPEBEMPE bits to which 1 has been set.
The BEMP bit cannot be cleared to 0 even if software writes 0 to this bit.

CTRT Bit (Control Transfer Stage Transition Interrupt Status)

When the function controller function is selected, the USB module updates the CTSQ value and sets the CTRT bit to 1 on detecting a change in the control transfer stage.
When a control transfer stage transition interrupt is generated, clear the status before the USB module detects the next control transfer stage transition.
When the host controller function is selected, the read value is invalid.

DVST Bit (Device State Transition Interrupt Status)

When the function controller function is selected, the USB module updates the DVSQ value and sets the DVST bit to 1 on detecting a change in the device state.
When a device state transition interrupt is generated, clear the status before the USB module detects the next device state transition.
When the host controller function is selected, the read value is invalid.

SOFR Bit (Frame Number Refresh Interrupt Status)

(1) When the host controller function is selected
The USB module sets the SOFR bit to 1 on updating the frame number when software has set the UACT bit in DVSTCTR0 to 1. (A frame number refresh interrupt is detected every 1 ms.)
(2) When the function controller function is selected
The USB module sets the SOFR bit to 1 on updating the frame number. (A frame number refresh interrupt is detected every 1 ms.)
The USB module can detect an SOFR interrupt through the internal interpolation function even when a damaged SOF packet is received from the USB host.

RESM Bit (Resume Interrupt Status)

When the function controller function is selected, the USB module sets the RESM bit to 1 on detecting the falling edge of the signal on the USB_DP pin in the suspended state (DVSQ = 1xx).
When the host controller function is selected, the read value is invalid.

VBINT Bit (VBUS Interrupt Status)

The USB module sets the VBINT bit to 1 on detecting a level change (high to low or low to high) in the USB_VBUS pin input value. The USB module sets the VBSTS bit to indicate the USB_VBUS pin input value. When the VBUS interrupt is generated, use software to repeat reading the VBSTS bit until the same value is read three or more times, and eliminate chattering. Set the VBINT bit to 0 before setting the VBUS interrupt enable bit (VBSE) bit in interrupt enable register 0 (INTENB0) to 1.

26.2.14 Interrupt Status Register 1 (INTSTS1)

Address 2E43h, 2E42h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	EOFERR	SIGN	SACK	—			
After Reset	0	0	0	0/1	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	OVRCR	BCHG	—	DTCH	ATTCH	—	—	—
After Reset	X	0	0	0/1	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b3 to b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	SACK	Setup Transaction Normal Response Interrupt Status	0: SACK interrupts are not generated. 1: SACK interrupts are generated.	R/W (1)
b5	SIGN	Setup Transaction Error Interrupt Status	0: SIGN interrupts are not generated. 1: SIGN interrupts are generated.	R/W (1)
b6	EOFERR	EOF Error Detection Interrupt Status	0: EOFERR interrupts are not generated. 1: EOFERR interrupts are generated.	R/W (1)
b10 to b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b11	ATTCH	ATTCH Interrupt Status	0: ATTCH interrupts are not generated. 1: ATTCH interrupts are generated.	R/W (1)
b12	DTCH	USB Disconnection Detection Interrupt Status	0: DTCH interrupts are not generated. 1: DTCH interrupts are generated.	R/W (1)
b13	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b14	BCHG	USB Bus Change Interrupt Status (2)	0: BCHG interrupts are not generated. 1: BCHG interrupts are generated.	R/W (1)
b15	OVRCR	Overcurrent Input Change Interrupt Status (2)	0: OVRCR interrupts are not generated. 1: OVRCR interrupts are generated.	R/W (1)

Notes:
1. To clear the status indicated by the bits in INTSTS1, write 0 only to the bits to be cleared; write 1 to the other bits.
2. A change in the status indicated by the OVRCR or BCHG bit can be detected even while the clock supply is stopped (while SCKE = 0), and the interrupt is output when the corresponding interrupt enable bit is enabled. Clearing the status through software should be done after enabling the clock supply.
   No interrupts other than those indicated by the BCHG and OVRCR bits can be detected while the clock supply is stopped (while SCKE = 0).

INTSTS1 is used to confirm the status of each interrupt when the host controller function is selected.
The various status change interrupts indicated by the bits in INTSTS1 should be enabled only when the host controller function is selected.

SACK Bit (Setup Transaction Normal Response Interrupt Status)

Indicates the status of the setup transaction normal response interrupt when the host controller function is selected.
The USB module detects the SACK interrupt when ACK response is returned from the peripheral device during the setup transactions issued by the USB module, and sets the SACK bit to 1. Here, if software has set the corresponding interrupt enable bit to 1, the USB module generates the SACK interrupt.
When the function controller function is selected, the read value is invalid.

SIGN Bit (Setup Transaction Error Interrupt Status)

Indicates the status of the setup transaction error interrupt when the host controller function is selected.
The USB module detects the SIGN interrupt when ACK response is not returned from the peripheral device three consecutive times during the setup transactions issued by this module, and sets the SIGN bit to 1. Here, if software has set the corresponding interrupt enable bit to 1, the USB module generates the SIGN interrupt.
Specifically, the USB module detects the SIGN interrupt when any of the following response conditions occur for three consecutive setup transactions.

- Timeout is detected by the USB module when the peripheral device has returned no response.
- A damaged ACK packet is received.·
- A handshake other than ACK (NAK, NYET, or STALL) is received.

When the function controller function is selected, the read value is invalid.

EOFERR Bit (EOF Error Detection Interrupt Status)

Indicates the status of the EOFERR interrupt when the host controller function is selected.
The USB module detects the EOFERR interrupt on detecting that communication is not completed at the EOF2 timing prescribed by the USB Specifications 2.0, and sets the EOFERR bit to 1. Here, if software has set the corresponding interrupt enable bit to 1, the USB module generates the EOFERR interrupt.
After detecting the EOFERR interrupt, the USB module controls hardware as described below (irrespective of the setting of the corresponding interrupt enable bit). Software should terminate all the pipes in which communications are currently carried for the USB port and perform re-enumeration of the USB port.

- Modifies the UACT bit for the port in which an EOFERR interrupt has been detected to 0.
- Puts the port in which an EOFERR interrupt has been generated into the idle state.

When the function controller function is selected, the read value is invalid.

ATTCH Bit (ATTCH Interrupt Status)

Indicates the status of the ATTCH interrupt when the host controller function is selected.
The USB module detects the ATTCH interrupt on detecting J-state or K-state of the full-speed signal level for 2.5 µs, and sets the ATTCH bit to 1. Here, if software has set the corresponding interrupt enable bit to 1, the USB module generates the interrupt.
Specifically, the USB module detects the ATTCH interrupt on any of the following conditions.

- K-state, SE0, or SE1 changes to J-state, and J-state continues for 2.5 µs.
- J-state, SE0, or SE1 changes to K-state, and K-state continues for 2.5 µs.

When the function controller function is selected, the read value is invalid.

DTCH Bit (USB Disconnection Detection Interrupt Status)

Indicates the status of the USB disconnection detection interrupt when the host controller function is selected.
The USB module detects the DTCH interrupt on detecting USB bus disconnection, and sets the DTCH bit to 1. Here, if software has set the corresponding interrupt enable bit to 1, the USB module generates the interrupt.
The USB module detects bus disconnection based on the USB Specifications 2.0.
After detecting the DTCH interrupt, the USB module controls hardware as described below (irrespective of the setting of the corresponding interrupt enable bit). Software should terminate all the pipes in which communications are currently carried out for the USB port and make a transition to the wait state for bus connection to the USB port (wait state for ATTCH interrupt generation).

- Modifies the UACT bit for the port in which a DTCH interrupt has been detected to 0.
- Puts the port in which a DTCH interrupt has been generated into the idle state.

When the function controller function is selected, the read value is invalid.

BCHG Bit (USB Bus Change Interrupt Status)

Indicates the status of the USB bus change interrupt.
The USB module detects the BCHG interrupt when a change in the full-speed signal level occurs on the USB port (a change from J-state, K-state, or SE0 to J-state, K-state, or SE0), and sets the BCHG bit to 1. Here, if software has set the corresponding interrupt enable bit to 1, the USB module generates the interrupt.
The USB module sets the LNST bits in SYSSTS0 to indicate the current input state of the USB port. When the BCHG interrupt is generated, use software to repeat reading the LNST bits until the same value is read three or more times, and eliminate chattering.
A change in the USB bus state can be detected even while the internal clock supply is stopped.
When the function controller function is selected, the read value is invalid.

OVRCR Bit (Overcurrent Input Change Interrupt Status)

Indicates the status of the USB_OVRCURA input pin change interrupt.
The USB module detects the OVRCR interrupt when a change (high to low or low to high) occurs in the input values to the USB_OVRCURA pin, and sets the OVRCR bit to 1. Here, if software has set the corresponding interrupt enable bit to 1, the USB module generates the interrupt.

26.2.15 BRDY Interrupt Status Register (BRDYSTS)

Address 2E47h, 2E46h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PIPE7BRDY	PIPE6BRDY	PIPE5BRDY	PIPE4BRDY	—	—	—	PIPE0BRDY
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PIPE0BRDY	BRDY Interrupt Status for PIPE0 (2)	0: Interrupts are not generated. 1: Interrupts are generated.	R/W (1)
b1	—	Reserved bits	Set to 0.	R/W
b2	—			
b3	—			
b4	PIPE4BRDY	BRDY Interrupt Status for PIPE4 (2)	0: Interrupts are not generated. 1: Interrupts are generated.	R/W (1)
b5	PIPE5BRDY	BRDY Interrupt Status for PIPE5 (2)	0: Interrupts are not generated. 1: Interrupts are generated.	R/W (1)
b6	PIPE6BRDY	BRDY Interrupt Status for PIPE6 (2)	0: Interrupts are not generated. 1: Interrupts are generated.	R/W (1)
b7	PIPE7BRDY	BRDY Interrupt Status for PIPE7 (2)	0: Interrupts are not generated. 1: Interrupts are generated.	R/W (1)
b8	—	Reserved bits	Set to 0.	R/W
b9	—			
b15 to b10	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Notes:
1. When the BRDYM bit is set to 0, to clear the status indicated by the bits in BRDYSTS, write 0 only to the bits to be cleared; write 1 to the other bits.
2. When the BRDYM bit is set to 0, clearing BRDY Interrupts should be done before accessing the FIFO.

BRDYSTS indicates the BRDY interrupt status for each pipe.

26.2.16 NRDY Interrupt Status Register (NRDYSTS)

Address 2E49h, 2E48h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PIPE7NRDY	PIPE6NRDY	PIPE5NRDY	PIPE4NRDY	—	—	—	PIPE0NRDY
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PIPE0NRDY	NRDY Interrupt Status for PIPE0	0: Interrupts are not generated. 1: Interrupts are generated.	R/W (1)
b1	—	Reserved bits	Set to 0.	R/W
b2	—			
b3	—			
b4	PIPE4NRDY	NRDY Interrupt Status for PIPE4	0: Interrupts are not generated. 1: Interrupts are generated.	R/W (1)
b5	PIPE5NRDY	NRDY Interrupt Status for PIPE5	0: Interrupts are not generated. 1: Interrupts are generated.	R/W (1)
b6	PIPE6NRDY	NRDY Interrupt Status for PIPE6	0: Interrupts are not generated. 1: Interrupts are generated.	R/W (1)
b7	PIPE7NRDY	NRDY Interrupt Status for PIPE7	0: Interrupts are not generated. 1: Interrupts are generated.	R/W (1)
b8	—	Reserved bits	Set to 0.	R/W
b9	—			
b15 to b10	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Note:
1. To clear the status indicated by the bits in NRDYSTS, write 0 only to the bits to be cleared; write 1 to the other bits.

NRDYSTS indicates the NRDY interrupt status for each pipe.

26.2.17 BEMP Interrupt Status Register (BEMPSTS)

Address 2E4Bh, 2E4Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PIPE7BEMP	PIPE6BEMP	PIPE5BEMP	PIPE4BEMP	—	—	—	PIPE0BEMP
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PIPE0BEMP	BEMP Interrupt Status for PIPE0	0: Interrupts are not generated. 1: Interrupts are generated.	R/W (1)
b1	—	Reserved bits	Set to 0.	R/W
b2	—			
b3	—			
b4	PIPE4BEMP	BEMP Interrupt Status for PIPE4	0: Interrupts are not generated. 1: Interrupts are generated.	R/W (1)
b5	PIPE5BEMP	BEMP Interrupt Status for PIPE5	0: Interrupts are not generated. 1: Interrupts are generated.	R/W (1)
b6	PIPE6BEMP	BEMP Interrupt Status for PIPE6	0: Interrupts are not generated. 1: Interrupts are generated.	R/W (1)
b7	PIPE7BEMP	BEMP Interrupt Status for PIPE7	0: Interrupts are not generated. 1: Interrupts are generated.	R/W (1)
b8	—	Reserved bits	Set to 0.	R/W
b9	—			
b15 to b10	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Note:
1. To clear the status indicated by the bits in BEMPSTS, write 0 only to the bits to be cleared; write 1 to the other bits.

BEMPSTS indicates the BEMP interrupt status for each pipe.

26.2.18 Frame Number Register (FRMNUM)

Address 2E4Dh, 2E4Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	FRNM[10:0]							
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	FRNM[10:0]		
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b10 to b0	FRNM[10:0]	Frame Number	The USB module sets the FRNM[10:0] bits to indicate the latest frame number, which is updated every time an SOF packet is issued or received (every 1 ms). Repeat reading the FRNM[10:0] bits until the same value is read twice.	R
b12 to b11	—	Reserved bit	Set to 0.	R/W
b13	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b14	—	Reserved bits	Set to 0.	R/W
b15	—			

FRMNUM indicates the frame number.

26.2.19 USB Address Register (USBADDR)

Address 2E51h, 2E50h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	USBADDR [6:0]						
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b6 to b0	USBADDR [6:0]	USB Address	When the function controller function is selected, these bits indicate the USB address assigned by the host when the SET_ADDRESS request is successfully processed.	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b11 to b8	—	Reserved bits	Set to 0.	R/W
b15 to b12	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

USBADDR indicates the USB address.

USBADDR[6:0] Bits (USB Address)

On detecting the USB bus reset, the USB module sets the USBADDR[6:0] bits to 00h.
When the host controller function is selected, the USBADDR[6:0] bits are invalid.
The USBADDR[6:0] bits are initialized by a USB bus reset detection.

26.2.20 USB Request Type Register (USBREQ)

Address 2E55h, 2E54h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	BMREQUESTTYPE[7:0]							
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	BREQUEST [7:0]							
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b7 to b0	BMREQUESTTYPE[7:0]	Request Type	These bits store the USB request bmRequestType value. • When the host controller function is selected The USB request data value for the setup transaction to be transmitted should be set in these bits. Do not modify these bits while the SUREQ bit is 1. • When the function controller function is selected These bits indicate the USB request data value received during the setup transaction. Writing to these bits is invalid.	R/W (1)
b15 to b8	BREQUEST [7:0]	Request	These bits store the USB request bRequest value. • When the host controller function is selected The USB request data value for the setup transaction to be transmitted should be set in these bits. Do not modify these bits while the SUREQ bit is 1. • When the function controller function is selected These bits indicate the USB request data value received during the setup transaction. Writing to these bits is invalid.	R/W (1)

Note:
1. When the function controller function is selected, these bits can only be read from, and writing to these bits is invalid. When the host controller function is selected, these bits can be read from and written to.

USBREQ stores setup requests for control transfers.
When the function controller function is selected, the values of bRequest and bmRequestType that have been received are stored. When the host controller function is selected, the values of bRequest and bmRequestType to be transmitted are set.
USBREQ is initialized by a USB bus reset.

26.2.21 USB Request Value Register (USBVAL)

Address 2E57h, 2E56h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	WVALUE [15:0]							
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	WVALUE [15:0]							
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b15 to b0	WVALUE [15:0]	Value	These bits store the USB request wValue value. • When the host controller function is selected The USB request wValue value for the setup transaction to be transmitted should be set in these bits. Do not modify these bits while the SUREQ bit is 1. • When the function controller function is selected These bits indicate the USB request wValue value received during the setup transaction. Writing to these bits is invalid.	R/W (1)

Note:

1. When the function controller function is selected, these bits can only be read from, and writing to these bits is invalid. When the host controller function is selected, these bits can be read from and written to.

When the function controller function is selected, the value of wValue that has been received is stored in USBVAL. When the host controller function is selected, the value of wValue to be transmitted is set. USBVAL is initialized by a USB bus reset.

26.2.22 USB Request Index Register (USBINDX)

Address 2E59h, 2E58h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	WINDEX [15:0]							
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	WINDEX [15:0]							
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b15 to b0	WINDEX [15:0]	Index	These bits store the USB request wIndex value. • When the host controller function is selected The USB request wIndex value for the setup transaction to be transmitted should be set in these bits. Do not modify these bits while the SUREQ bit in DCPCTR is 1. • When the function controller function is selected These bits indicate the USB request wIndex value received during the setup transaction. Writing to these bits is invalid.	R/W (1)

Note:
1. When the function controller function is selected, these bits can only be read from, and writing to these bits is invalid. When the host controller function is selected, these bits can be read from and written to.

USBINDX stores setup requests for control transfers.
When the function controller function is selected, the value of wIndex that has been received is stored. When the host controller function is selected, the value of wIndex to be transmitted is set.
USBINDX is initialized by a USB bus reset.

26.2.23 USB Request Length Register (USBLENG)

Address 2E5Bh, 2E5Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	WLENGTH [15:0]							
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	WLENGTH [15:0]							
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b15 to b0	WLENGTH [15:0]	Length	These bits store the USB request wLength value. • When the host controller function is selected The USB request wLength value for the setup transaction to be transmitted should be set in these bits. Do not modify these bits while the SUREQ bit in DCPCTR is 1. • When the function controller function is selected These bits indicate the USB request wLength value received during the setup transaction. Writing to these bits is invalid.	R/W (1)

Note:
1. When the function controller function is selected, these bits can only be read from, and writing to these bits is invalid. When the host controller function is selected, these bits can be read from and written to.

USBLENG stores setup requests for control transfers.
When the function controller function is selected, the value of wLength that has been received is stored. When the host controller function is selected, the value of wLength to be transmitted is set.
USBLENG is initialized by a USB bus reset.

26.2.24 DCP Configuration Register (DCPCFG)

Address 2E5Dh, 2E5Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	SHTNAK	—	—	DIR	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b3 to b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	DIR	Transfer Direction (1)	0: Data receiving direction 1: Data transmitting direction	R/W
b6, b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	SHTNAK	Pipe Disabled at End of Transfer (1)	0: Pipe continued at the end of transfer 1: Pipe disabled at the end of transfer	R/W
b15 to b8	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Note:
1. Modify these bits while PID is NAK. Before modifying these bits after modifying the PID bits for the DCP from BUF to NAK, check that the PBUSY bit is 0. However, if the PID bits have been modified to NAK by the USB module, checking the PBUSY bit through software is not necessary.

DCPCFG specifies the data transfer direction and disabling the pipe at the end of transfer for the default control pipe (DCP).

DIR Bit (Transfer Direction)

When the host controller function is selected, the DIR bit sets the transfer direction of the data stage and status stage.
When the function controller function is selected, the DIR bit should be set to 0.

SHTNAK Bit (Pipe Disabled at End of Transfer)

The SHTNAK bit specifies whether to modify PID to NAK upon the end of transfer when the selected pipe is in the receiving direction.
The SHTNAK bit is valid when the selected pipe in the receiving direction.
When the SHTNAK bit is set to 1, the USB module modifies the PID bits for the DCP to NAK on determining the end of the transfer. The USB module determines that the transfer has ended on the following condition.
- A short packet (including a zero-length packet) is successfully received.

26.2.25 DCP Maximum Packet Size Register (DCPMAXP)

Address 2E5Fh, 2E5Eh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	MXPS [6:0]						
After Reset	0	1	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	DEVSEL [3:0]				—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b6 to b0	MXPS [6:0]	Maximum Packet Size (1)	These bits specify the maximum data payload (maximum packet size) for the DCP. The initial value is 40h (64 bytes). These bits should be set to the value based on the USB Specifications. While MXPS = 0, do not write to the FIFO buffer or do not set PID to BUF.	R/W
b11 to b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b15 to b12	DEVSEL [3:0]	Device Select (2)	b15 b12 0 0 0 0: Address 0000 0 0 0 1: Address 0001 0 0 1 0: Address 0010 0 0 1 1: Address 0011 0 1 0 0: Address 0100 0 1 0 1: Address 0101 Other than above: Do not set.	R/W

Notes:
1. Modify the MXPS[6:0] bits while PID is NAK. Before modifying these bits after modifying the PID bits for the DCP from BUF to NAK, check that the PBUSY bit is 0. However, if the PID bits have been modified to NAK by the USB module, checking the PBUSY bit through software is not necessary. After modifying the MXPS[6:0] bits and the DCP has been set to the CURPIPE bits, clear the buffer by setting the BCLR bit to 1.
2. Modify the DEVSEL bits while PID is NAK and the SUREQ bit is 0. Before modifying these bits after modifying the PID bits for the DCP from BUF to NAK, check that the PBUSY bit is 0. However, if the PID bits have been modified to NAK by the USB module, checking the PBUSY bit through software is not necessary.

DCPMAXP specifies the maximum packet size for the DCP.

DEVSEL[3:0] Bits (Device Select)

When the host controller function is selected, these bits specify the address of the peripheral device which is the communication target during control transfer.
The DEVSEL[3:0] bits should be set after setting the address to the DEVADDn (n = 0 to 5) register corresponding to the value to be set in the DEVSEL[3:0] bits. For example, before setting the DEVSEL[3:0] bits to 0010, the address should be set to DEVADD2.
When the function controller function is selected, the DEVSEL[3:0] bits should be set to 0000b.

26.2.26 DCP Control Register (DCPCTR)

Address 2E61h, 2E60h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	SQSET	SQMON	PBUSY	—	—	CCPL	PID[1:0]	
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	BSTS	SUREQ	—	—	SUREQCLR	—	—	SQCLR
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b1, b0	PID[1:0]	Response PID	b1 b0 0 0: NAK response 0 1: BUF response (depending on the buffer state) 1 0: STALL response 1 1: STALL response	R/W
b2	CCPL	Control Transfer End Enable	0: Invalid 1: Completion of control transfer is enabled.	R/W
b4, b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	PBUSY	Pipe Busy	0: DCP is not used for the transaction. 1: DCP is used for the transaction.	R
b6	SQMON	Sequence Toggle Bit Monitor	0: DATA0 1: DATA1	R
b7	SQSET	Toggle Bit Set (3)	0: Invalid 1: Specifies DATA1.	R/W (1)
b8	SQCLR	Toggle Bit Clear (3)	0: Invalid 1: Specifies DATA0.	R/W (1)
b10, b9	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b11	SUREQCLR	SUREQ Bit Clear	0: Invalid 1: 0 is written to the SUREQ bit.	R/W (2)
b13, b12	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b14	SUREQ	Setup Token Transmission	0: Invalid 1: Transmits the setup packet.	R/W (2)
b15	BSTS	Buffer Status	0: Buffer access is disabled. 1: Buffer access is enabled.	R

Notes:
1. This bit is always read as 0. Only 1 can be written.
2. Only 1 can be written.
3. Write 1 to the SQSET and SQCLR bits while PID is NAK. Before modifying these bits after modifying the PID bits for the DCP from BUF to NAK, check that the PBUSY bit is 0. However, if the PID bits have been modified to NAK by the USB module, checking the PBUSY bit through software is not necessary.

DCPCTR is used to confirm the buffer memory status, change and confirm the data PID sequence bits, and set the response PID for the DCP.
The CCPL and PID[1:0] bits in DCPCTR are initialized by a USB bus reset.

PID[1:0] Bits (Response PID)

The PID[1:0] bits control the response type of the USB module during control transfer.

(1) When the host controller function is selected
Modify the setting of the PID[1:0] bits from NAK to BUF using the following procedure.
- When the transmitting direction is set
  Write all the transmit data to the FIFO buffer while UACT is 1 and PID is NAK, and then set PID to BUF. After PID has been set to BUF, the USB module executes the OUT transaction.
- When the receiving direction is set
  Check that the FIFO buffer is empty (or empty the buffer) while UACT is 1 and PID is NAK, and then set PID to BUF. After PID has been set to BUF, the USB module executes the IN transaction.

The USB module modifies the setting of the PID[1:0] bits as follows.
- The USB module sets PID to STALL (11) on receiving the data of a size exceeding the maximum packet size when software has set the PID[1:0] bits to BUF.
- The USB module sets PID to NAK on detecting a receive error, such as a CRC error, three consecutive times.·
- The USB module also sets PID to STALL (11) on receiving the STALL handshake.

(2) When the function controller function is selected
The USB module modifies the setting of the PID[1:0] bits as follows.
- The USB module modifies the PID[1:0] bits to NAK on receiving the setup packet. Here, the USB module sets VALID to 1. Software cannot modify the setting of the PID[1:0] bits until software sets VALID to 0.
- The USB module sets PID to STALL (11) on receiving the data of a size exceeding the maximum packet size when software has set the PID[1:0] bits to BUF.
- The USB module sets PID to STALL (1x) on detecting the control transfer sequence error.
- The USB module sets PID to NAK on detecting the USB bus reset.

The USB module does not reference to the setting of the PID[1:0] bits while the SET_ADDRESS request is processed (auto processing).

CCPL Bit (Control Transfer End Enable)

When the function controller function is selected, setting the CCPL bit to 1 enables the status stage of the control transfer to be completed.
When software sets the CCPL bit to 1 while the corresponding PID bits are set to BUF, the USB module completes the control transfer stage.
Specifically, during control read transfer, the USB module transmits the ACK handshake in response to the OUT transaction from the USB host, and transmits the zero-length packet in response to the IN transaction from the USB host during control write or no-data control transfer. However, on detecting the SET_ADDRESS request, the USB module operates in auto response mode from the setup stage up to the status stage completion irrespective of the setting of the CCPL bit.
The USB module modifies the CCPL bit from 1 to 0 on receiving a new setup packet.
Software cannot write 1 to the CCPL bit while the VALID bit is 1.
When the host controller function is selected, be sure to write 0 to the CCPL bit.

PBUSY Bit (Pipe Busy)

The PBUSY bit indicates whether DCP is used or not for the transaction when USB changes the PID bits from BUF to NAK.
The USB module modifies the PBUSY bit from 0 to 1 upon start of the USB transaction for the relevant pipe, and modifies the PBUSY bit from 1 to 0 upon completion of one transaction.
Reading the PBUSY bit after software has set PID to NAK allows checking whether modification of the pipe settings is possible.
For details, refer to **26.3.4.1 Pipe Control Register Switching Procedures**.

SQMON Bit (Sequence Toggle Bit Monitor)

The SQMON bit indicates the expected value of the sequence toggle bit for the next transaction during the DCP transfer.
The USB module allows the SQMON bit to toggle upon normal completion of the transaction. However, the SQMON bit is not allowed to toggle when a DATA-PID disagreement occurs during the transfer in the receiving direction.
When the function controller function is selected, the USB module sets the SQMON bit to 1 (specifies DATA1 as the expected value) upon successful reception of the setup packet.
When the function controller function is selected, the USB module does not reference the SQMON bit during the IN/OUT transaction of the status stage, and does not allow the SQMON bit to toggle upon normal completion.

SQSET Bit (Toggle Bit Set)

The SQSET bit specifies DATA1 as the expected value of the sequence toggle bit for the next transaction during the DCP transfer.
Do not set the SQCLR and SQSET bits to 1 simultaneously.

SQCLR Bit (Toggle Bit Clear)

The SQCLR bit specifies DATA0 as the expected value of the sequence toggle bit for the next transaction during the DCP transfer. The SQCLR bit always indicates 0
Do not set the SQCLR and SQSET bits to 1 simultaneously.

SUREQCLR Bit (SUREQ Bit Clear)

When the host controller function is selected, setting the SUREQCLR bit to 1 clears the SUREQ bit to 0. The SUREQCLR bit always indicates 0.
Set the SUREQCLR bit to 1 through software when communication has stopped with the SUREQ bit being 1 during the setup transaction. However, for normal setup transactions, the USB module automatically clears the SUREQ bit to 0 upon completion of the transaction; therefore, clearing the SUREQ bit through software is not necessary.
Controlling the SUREQ bit through the SUREQCLR bit must be done while the UACT bit is 0 and thus communication is halted or while no transfer is being performed with bus disconnection detected.
When the function controller function is selected, be sure to write 0 to the SUREQCLR bit.

SUREQ Bit (Setup Token Transmission)

The USB module transmits the setup packet by setting the SUREQ bit to 1 when the host controller function is selected.
After completing the setup transaction process, the USB module generates either the SACK or SIGN interrupt and clears the SUREQ bit to 0.
The USB module also clears the SUREQ bit to 0 when software sets the SUREQCLR bit to 1.
Before setting the SUREQ bit to 1, set the DEVSEL bits, USBREQ, USBVAL, USBINDX, and USBLENG appropriately to transmit the desired USB request in the setup transaction. Before setting this bit to 1, check that the PID bits for the DCP are set to NAK. After setting the SUREQ bit to 1, do not modify the DEVSEL bits, USBREQ, USBVAL, USBINDX, or USBLENG until the setup transaction is completed (SUREQ = 1).
Write 1 to the SUREQ bit only when transmitting the setup token; for other purposes, write 0.
When the function controller function is selected, be sure to write 0 to the SUREQ bit.

BSTS Bit (Buffer Status)

Indicates whether DCP FIFO buffer access is enabled or disabled.
The meaning of the BSTS bit depends on the ISEL bit setting as follows.
- When ISEL = 0, the BSTS bit indicates whether the received data can be read from the buffer.
- When ISEL = 1, the BSTS bit indicates whether the data to be transmitted can be written to the buffer.

26.2.27 Pipe Window Select Register (PIPESEL)

Address 2E65h, 2E64h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	PIPESEL [3:0]			
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b3 to b0	PIPESEL [3:0]	Pipe Window Select	b3 b2 b1 b0 0 0 0 0: No pipe selected 0 1 0 0: PIPE4 0 1 0 1: PIPE5 0 1 1 0: PIPE6 0 1 1 1: PIPE7 Other than above: Do not set.	R/W
b15 to b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

PIPESEL is a register to specify the pipe number.
PIPE4 to PIPE 7 should be set using PIPESEL, PIPECFG, PIPEMAXP, PIPEPERI, PIPEnCTR, PIPEnTRE, and PIPEnTRN.
After selecting the pipe using PIPESEL, functions of the pipe should be set using PIPECFG, PIPEMAXP, and PIPEPERI. PIPEnCTR, PIPEnTRE, and PIPEnTRN can be set regardless of the pipe selection in PIPESEL.

PIPESEL[3:0] Bits (Pipe Window Select)

The PIPESEL[3:0] bits select the pipe number corresponding to PIPECFG, PIPEMAXP, and PIPEPERI which data are written to or read from.
Selecting a pipe number through the PIPESEL[3:0] bits allows writing to and reading from PIPECFG, PIPEMAXP, and PIPEPERI which correspond to the selected pipe number.
When PIPESEL[3:0] = 0000, 0 is read from all of the bits in PIPECFG, PIPEMAXP, PIPEPERI, and PIPEnCTR. Writing to these bits is invalid.

26.2.28 Pipe Configuration Register (PIPECFG)

Address 2E69h, 2E68h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	SHTNAK	—	—	DIR	EPNUM[3:0]			
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	TYPE[1:0]		—	—	—	BFRE	DBLB	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b3 to b0	EPNUM[3:0]	Endpoint Number (1)	These bits specify the endpoint number for the selected pipe. Setting 0000 means unused pipe.	R/W
b4	DIR	Transfer Direction (2, 3)	0: Receiving direction 1: Transmitting direction	R/W
b6, b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	SHTNAK	Pipe Disabled at End of Transfer (1)	0: Pipe continued at the end of transfer 1: Pipe disabled at the end of transfer	R/W
b8	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b9	DBLB	Double Buffer Mode (2, 3)	0: Single buffer 1: Double buffer	R/W
b10	BFRE	BRDY Interrupt Operation Specification (2, 3)	0: BRDY interrupt upon transmitting or receiving data 1: BRDY interrupt upon completion of reading data	R/W
b13 to b11	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b15, b14	TYPE[1:0]	Transfer Type (1)	• PIPE4 and PIPE5 b15 b14 0 0: Pipe not used 0 1: Bulk transfer 1 0: Do not set. 1 1: Do not set. • PIPE6 and PIPE7 b15 b14 0 0: Pipe not used 0 1: Do not set. 1 0: Interrupt transfer 1 1: Do not set.	R/W

Notes:

1. Modify the TYPE, SHTNAK, and EPNUM bits while PID is NAK. Before modifying these bits after modifying the PID bits for the selected pipe from BUF to NAK, check that the PBUSY bit is 0. However, if the PID bits have been modified to NAK by the USB module, checking the PBUSY bit through software is not necessary.
2. Modify the BFRE, DBLB, and DIR bits while PID is NAK and before the pipe is selected by the CURPIPE bits. Before modifying these bits after modifying the PID bits for the selected pipe from BUF to NAK, check that the PBUSY bit is 0. However, if the PID bits have been modified to NAK by the USB module, checking the PBUSY bit through software is not necessary.
3. To modify the BFRE, DBLB, and DIR bits after completing USB communication using the selected pipe, write 1 and then 0 to the ACLRM bit continuously through software to clear the FIFO buffer assigned to the selected pipe while the PID and CURPIPE bits are in the state described in the above note 2.

PIPECFG specifies the transfer type, buffer memory access direction, and endpoint numbers for PIPE4 to PIPE7. It also selects single or double buffer mode, and whether to continue or disable pipe operation at the end of transfer.

EPNUM[3:0] Bits (Endpoint Number)

The EPNUM[3:0] bits specify the endpoint number for the selected pipe.
Setting 0000b means unused pipe.
Do not make the settings such that the combination of the settings of the DIR and EPNUM bits should be the same for two or more pipes (EPNUM = 0000 can be set for all of the pipes).

DIR Bit (Transfer Direction)

The DIR bit specifies the transfer direction for the selected pipe.
When software has set the DIR bit to 0, the USB module uses the selected pipe in the receiving direction, and when software has set the DIR bit to 1, the USB module uses the selected pipe in the transmitting direction.

SHTNAK Bit (Pipe Disabled at End of Transfer)

The SHTNAK bit specifies whether to modify PID to NAK upon the end of transfer when the selected pipe is in the receiving direction.
The SHTNAK bit is valid when the selected pipe is PIPE4 or PIPE5 in the receiving direction.
When software has set the SHTNAK bit to 1 for the selected pipe in the receiving direction, the USB module modifies the PID bits corresponding to the selected pipe to NAK on determining the end of the transfer. The USB module determines that the transfer has ended on any of the following conditions.

- A short packet (including a zero-length packet) is successfully received.
- The transaction counter is used and the number of packets specified by the counter are successfully received.

DBLB Bit (Double Buffer Mode)

The DBLB bit selects either single or double buffer mode for the FIFO buffer used by the selected pipe.
The DBLB bit is valid when PIPE4 and PIPE5 are selected.

BFRE Bit (BRDY Interrupt Operation Specification)

Specifies the BRDY interrupt generation timing from the USB module to the CPU with respect to the selected pipe.
When software has set the BFRE bit to 1 and the selected pipe is in the receiving direction, the USB module detects the transfer completion and generates the BRDY interrupt on having read the relevant packet.
When the BRDY interrupt is generated with the above conditions, software needs to write 1 to the BCLR bit. The FIFO buffer assigned to the selected pipe is not enabled for reception until 1 is written to the BCLR bit.
When software has set the BFRE bit to 1 and the selected pipe is in the transmitting direction, the USB module does not generate the BRDY interrupt.
For details, refer to **26.3.3.1 BRDY Interrupt**.

TYPE[1:0] Bits (Transfer Type)

The TYPE[1:0] bits select the transfer type for the pipe selected by the PIPESEL bits (selected pipe).
Before setting PID to BUF for the selected pipe (before starting USB communication using the selected pipe), be sure to set the TYPE[1:0] bits to bulk transfer or interrupt transfer.

26.2.29 Pipe Maximum Packet Size Register (PIPEMAXP)

Address 2E6Dh, 2E6Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	MXPS[8:0]							
After Reset	0	0/1(1)	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	DEVSEL [3:0]				—	—	—	MXPS[8:0]
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b8 to b0	MXPS[8:0]	Maximum Packet Size (2)	PIPE4 and PIPE5 8 bytes (008h), 16 bytes (010h), 32 bytes (020h), 64 bytes (040h) (Bits [8:7] and [2:0] are not provided.) PIPE6 and PIPE7 1 byte (001h) to 64 bytes (040h) (Bits [8:7] are not provided.)	R/W
b11 to b9	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b15 to b12	DEVSEL [3:0]	Device Select (3)	b3 b2 b1 b0 0 0 0 0: Address 0000 0 0 0 1: Address 0001 0 0 1 0: Address 0010 0 0 1 1: Address 0011 0 1 0 0: Address 0100 0 1 0 1: Address 0101 Other than above: Do not set.	R/W

Notes:
1. The initial value of the MXPS[8:0] bits is 0000h when no pipe is selected with the PIPESEL bits in PIPESEL and 0040h when a pipe is selected.
2. Modify the MXPS[8:0] bits while PID is NAK and before the pipe is selected by the CURPIPE bits. Before modifying these bits after modifying the PID bits for the selected pipe from BUF to NAK, check that the PBUSY bit is 0. However, if the PID bits have been modified to NAK by the USB module, checking the PBUSY bit through software is not necessary.
3. Modify the DEVSEL[3:0] bits while PID is NAK. Before modifying these bits after modifying the PID bits for the selected pipe from BUF to NAK, check that the PBUSY bit is 0. However, if the PID bits have been modified to NAK by the USB module, checking the PBUSY bit through software is not necessary.

PIPEMAXP specifies the maximum packet size for PIPE4 to PIPE7.

MXPS[8:0] Bits (Maximum Packet Size)

Specifies the maximum data payload (maximum packet size) for the selected pipe.
These bits should be set to the appropriate value for each transfer type based on the USB Specifications. While MXPS = 0, do not write to the FIFO buffer or set PID to BUF.

DEVSEL[3:0] Bits (Device Select)

When the host controller function is selected, these bits specify the USB device address of the peripheral device which is the communication target.
The DEVSEL[3:0] bits should be set after setting the address to the DEVADDn (n = 0 to 5) register corresponding to the value to be set in the DEVSEL[3:0] bits. For example, before setting the DEVSEL[3:0] bits to 0010, the address should be set to DEVADD2.
When the function controller function is selected, the DEVSEL[3:0] bits should be set to 0000b.

26.2.30 Pipe Cycle Control Register (PIPEPERI)

Address 2E6Fh, 2E6Eh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	IITV[2:0]		
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b2 to b0	IITV[2:0]	Interval Error Detection Interval	Specifies the interval error detection timing for the selected pipe in terms of frames, which is expressed as n-th power of 2. Before modifying the IITV[2:0] bits after USB communication has been completed with the IITV[2:0] bits set to a certain value, set PID to NAK and then set the ACLRM bit to 1 to initialize the interval timer. The IITV[2:0] bits are invalid for PIPE4 and PIPE5; set the IITV[2:0] bits to 000 for PIPE4 and PIPE5.	R/W
b11 to b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b12	—	Reserved bit	Set to 0	R/W
b15 to b13	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Note:

1. Modify the IITV bits while PID is NAK. Before modifying these bits after modifying the PID bits for the selected pipe from BUF to NAK, check that the PBUSY bit is 0. However, if the PID bits have been modified to NAK by the USB module, checking the PBUSY bit through software is not necessary.

PIPEPERI sets the interval error detection interval for PIPE6 and PIPE7.

26.2.31 PIPEn Control Registers (PIPEnCTR) (n = 4 to 7)

• PIPEnCTR (n = 4 to 5)

Address 2E77h, 2E76h, 2E79h, 2E78h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	SQSET	SQMON	PBUSY	—	—	—	PID[1:0]	
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	BSTS	INBUFM	—	—	—	ATREPM	ACLRM	SQCLR
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b1, b0	PID[1:0]	Response PID	b1 b0 0 0: NAK response 0 1: BUF response (depending on the buffer state) 1 0: STALL response 1 1: STALL response	R/W
b4 to b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	PBUSY	Pipe Busy	0: The relevant pipe is not used for the transaction. 1: The relevant pipe is used for the transaction.	R
b6	SQMON	Toggle Bit Confirmation	0: DATA0 1: DATA1	R
b7	SQSET	Toggle Bit Set (2)	0: Invalid 1: Specifies DATA1.	R/W (1)
b8	SQCLR	Toggle Bit Clear (2)	0: Invalid 1: Specifies DATA0.	R/W (1)
b9	ACLRM	Auto Buffer Clear Mode (3)	0: Disabled 1: Enabled (all buffers are initialized)	R/W
b10	ATREPM	Auto Response Mode (2)	0: Auto response is disabled. 1: Auto response is enabled.	R/W
b13 to b11	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b14	INBUFM	Transmit Buffer Monitor	0: There is no data to be transmitted in the buffer memory. 1: There is data to be transmitted in the buffer memory.	R
b15	BSTS	Buffer Status	0: Buffer access by the CPU is disabled. 1: Buffer access by the CPU is enabled.	R

Notes:
1. Only 0 can be read and 1 can be written.
2. Modify the ATREPM bit or write 1 to the SQCLR or SQSET bit while PID is NAK. Before modifying these bits after modifying the PID bits for the selected pipe from BUF to NAK, check that the PBUSY bit in DCPCTR is 0. However, if the PID bits have been modified to NAK by the USB module, checking the PBUSY bit in DCPCTR through software is not necessary.
3. Modify the ACLRM bit while PID is NAK and before the pipe is selected by the CURPIPE bits. Before modifying this bit after modifying the PID bits for the selected pipe from BUF to NAK, check that the PBUSY bit in DCPCTR is 0. However, if the PID bits have been modified to NAK by the USB module, checking the PBUSY bit in DCPCTR through software is not necessary.

PIPEnCTR is used to confirm the buffer memory status for the corresponding pipe, change and confirm the data PID sequence bit, determine whether auto response mode is set, determine whether auto buffer clear mode is set, and set a response PID for PIPE4 to PIPE7. PIPEnCTR can be set regardless of the pipe selection in PIPESEL.

PID[1:0] Bits (Response PID)

The PID[1:0] bits specify the response type for the next transaction of the relevant pipe.
The default setting of the PID[1:0] bits is NAK. Modify the setting of the PID[1:0] bits to BUF to use the relevant pipe for USB transfer. Table 26.9 and Table 26.10 show the basic operation (operation when there are no errors in the transmitted and received packets) of the USB module depending on the PID bit setting.
After modifying the setting of the PID[1:0] bits through software from BUF to NAK during USB communication using the relevant pipe, check that the PBUSY bit in DCPCTR is 1 to see if USB transfer using the relevant pipe has actually entered the NAK state. However, if the PID bits have been modified to NAK by the USB module, checking the PBUSY bit through software is not necessary.
The USB module modifies the setting of the PID[1:0] bits in the following cases.

- The USB module sets PID to NAK on recognizing the completion of the transfer when the relevant pipe is in the receiving direction and software has set the SHTNAK bit for the selected pipe to 1.·
- The USB module sets PID to STALL (11) on receiving a data packet with a payload exceeding the maximum packet size of the relevant pipe.
- The USB module sets PID to NAK on detecting a USB bus reset when the function controller function is selected.
- The USB module sets PID to NAK on detecting a receive error, such as a CRC error, three consecutive times when the host controller function is selected.
- The USB module sets PID to STALL (11) on receiving the STALL handshake when the host controller function is selected.

To specify each response type, set the PID[1:0] bits as follows.

- To make a transition from NAK (00) to STALL, set 10.
- To make a transition from BUF (01) to STALL, set 11.
- To make a transition from STALL (11) to NAK, set 10 and then 00.
- To make a transition from STALL to BUF, set 00 (NAK) and then 01 (BUF).

PBUSY Bit (Pipe Busy)

The PBUSY bit indicates whether the relevant pipe is being currently used or not for the transaction.
The USB module modifies the PBUSY bit from 0 to 1 upon start of the USB transaction for the relevant pipe, and modifies the PBUSY bit from 1 to 0 upon completion of one transaction.
Reading the PBUSY bit after software has set PID to NAK allows checking whether modification of the pipe settings is possible.
For details, refer to **26.3.4.1 Pipe Control Register Switching Procedures**.

SQMON Bit (Toggle Bit Confirmation)

The SQMON bit indicates the expected value of the sequence toggle bit for the next transaction of the relevant pipe.
The USB module allows the SQMON bit to toggle upon normal completion of the transaction of the relevant pipe. However, the SQMON bit is not allowed to toggle when a DATA-PID disagreement occurs during the transfer in the receiving direction.

SQSET Bit (Toggle Bit Set)

The SQSET bit should be set to 1 to set DATA1 as the expected value of the sequence toggle bit for the next transaction of the relevant pipe.
Setting the SQSET bit to 1 through software allows the USB module to set DATA1 as the expected value of the sequence toggle bit of the relevant pipe. The USB module always sets the SQSET bit to 0.

SQCLR Bit (Toggle Bit Clear)

The SQCLR bit should be set to 1 to clear the expected value (to set DATA0 as the expected value) of the sequence toggle bit for the next transaction of the relevant pipe.
Setting the SQCLR bit to 1 through software allows the USB module to set DATA0 as the expected value of the sequence toggle bit of the relevant pipe. The USB module always sets the SQCLR bit to 0.

ACLRM Bit (Auto Buffer Clear Mode)

Enables or disables auto buffer clear mode for the relevant pipe.
To delete the information in the FIFO buffer assigned to the relevant pipe completely, write 1 and then 0 to the ACLRM bit continuously.
Table 26.11 shows the information cleared by writing 1 and 0 to the ACLRM bit continuously and the cases in which clearing the information is necessary.

ATREPM Bit (Auto Response Mode)

Enables or disables auto response mode for the relevant pipe.
When the function controller function is selected and the relevant pipe is for bulk transfer, the ATREPM bit can be set to 1.
When the ATREPM bit is set to 1, the USB module responds to the token from the USB host as described below.

(1) When the relevant pipe is for bulk IN transfer (TYPE = 01 and DIR = 1)
When ATREPM = 1 and PID = BUF, the USB module transmits a zero-length packet in response to the IN token.
The USB module updates (allows toggling of) the sequence toggle bit (DATA-PID) each time the USB module receives ACK from the USB host (in a single transaction, IN token is received, zero-length packet is transmitted, and then ACK is received.).
In this case, the USB module does not generate the BRDY or BEMP interrupt.

(2) When the relevant pipe is for bulk OUT transfer (TYPE = 01 and DIR = 0)
When ATREPM = 1 and PID = BUF, the USB module returns NAK in response to the OUT token and generates the NRDY interrupt.
For USB communication in auto response mode, set the ATREPM bit to 1 while the FIFO buffer is empty.
Do not write to the FIFO buffer during USB communication in auto response mode.
When the host controller function is selected, be sure to set the ATREPM bit to 0.

INBUFM Bit (Transmit Buffer Monitor)

Indicates the relevant FIFO buffer status when the relevant pipe is in the transmitting direction.
When the relevant pipe is in the transmitting direction (DIR = 1), the USB module sets the INBUFM bit to 1 when software (or DMACA) completes writing data to at least one FIFO buffer plane.
The USB module sets the INBUFM bit to 0 when the USB module completes transmitting the data from the FIFO buffer plane to which all the data has been written. In double buffer mode (DBLB = 1), the USB module sets the INBUFM bit to 0 when the USB module completes transmitting the data from the two FIFO buffer planes before software (or DMACA) completes writing data to one FIFO buffer plane.
The INBUFM bit indicates the same value as the BSTS bit when the relevant pipe is in the receiving direction (DIR = 0).

BSTS Bit (Buffer Status)

Indicates the FIFO buffer status for the relevant pipe.
The meaning of the BSTS bit depends on the settings of the DIR and BFRE bits as shown in Table 26.12.

Table 26.9 Operation of USB Module depending on PID Bit Setting (When Host Controller Function is Selected)

PID Bit	Transfer Type	Transfer Direction (DIR Bit)	Operation of USB Module
00 (NAK)	Operation does not depend on the setting.	Operation does not depend on the setting.	Does not issue tokens.
01 (BUF)	Bulk or interrupt	Operation does not depend on the setting.	Issues tokens while the UACT bit is 1 and the FIFO buffer corresponding to the relevant pipe is ready for transmission and reception. Does not issue tokens while the UACT bit is 0 or the FIFO buffer corresponding to the relevant pipe is not ready for transmission or reception.
10 (STALL) or 11 (STALL)	Operation does not depend on the setting.	Operation does not depend on the setting.	Does not issue tokens.

Table 26.10 Operation of USB Module depending on PID Bit Setting (When Function Controller Function is Selected)

PID Bit	Transfer Type	Transfer Direction (DIR Bit)	Operation of USB Module
00 (NAK)	Bulk or interrupt	Operation does not depend on the setting.	Returns NAK in response to the token from the USB host. For the operation when the ATREPM bit is 1, refer to the description of the ATREPM bit.
01 (BUF)	Bulk	Receiving direction (DIR = 0)	Receives data and returns ACK in response to the OUT token from the USB host if the FIFO buffer corresponding to the relevant pipe is ready for reception.
	Interrupt	Receiving direction (DIR = 0)	Receives data and returns ACK in response to the OUT token from the USB host if the FIFO buffer corresponding to the relevant pipe is ready for reception.
	Bulk or interrupt	Transmitting direction (DIR = 1)	Transmits data in response to the token from the USB host if the corresponding FIFO buffer is ready for transmission. Returns NAK if not ready.
10 (STALL) or 11 (STALL)	Bulk or interrupt	Operation does not depend on the setting.	Returns STALL in response to the token from the USB host.

Table 26.11 Information Cleared by USB Module by Setting ACLRM = 1

No.	Information Cleared by ACLRM Bit Manipulation	Cases in which Clearing Information is Necessary
1	All the information in the FIFO buffer assigned to the relevant pipe (both FIFO buffer planes are cleared when double buffer mode is selected)	
2	Internal flags concerning the BFRE bit	When the BFRE setting is modified
3	FIFO buffer toggle control	When the DBLB setting is modified
4	Internal flags concerning the transaction count	When the transaction count function is forcibly terminated

Table 26.12 Operation of BSTS Bit

DIR Bit	BFRE Bit	BSTS Bit Function
0	0	1: The received data can be read from the FIFO buffer. 0: The received data has been completely read from the FIFO buffer.
	1	1: The received data can be read from the FIFO buffer. 0: Software has set the BCLR bit to 1 after the received data has been completely read from the FIFO buffer.
1	0	1: The transmit data can be written to the FIFO buffer. 0: The transmit data has been completely written to the FIFO buffer.
	1	Do not set.

• PIPEnCTR (n = 6 or 7)

Address 2E7Bh, 2E7Ah, 2E7Dh, 2E7Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	SQSET	SQMON	PBUSY	—	—	—	PID[1:0]	
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	BSTS	—	—	—	—	—	ACLRM	SQCLR
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b1, b0	PID[1:0]	Response PID	b1 b0 0 0: NAK response 0 1: BUF response (depending on the buffer state) 1 0: STALL response 1 1: STALL response	R/W
b4 to b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	PBUSY	Pipe Busy	0: The relevant pipe is not used at the USB bus. 1: The relevant pipe is used at the USB bus.	R
b6	SQMON	Toggle Bit Confirmation	0: DATA0 1: DATA1	R
b7	SQSET	Toggle Bit Set (2)	0: Invalid 1: Specifies DATA1.	R/W (1)
b8	SQCLR	Toggle Bit Clear (2)	0: Invalid 1: Specifies DATA0.	R/W (1)
b9	ACLRM	Auto Buffer Clear Mode (2, 3)	0: Auto buffer clear mode is disabled. 1: Auto buffer clear mode is enabled (all buffers are initialized)	R/W
b14 to b10	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b15	BSTS	Buffer Status	0: Buffer access is disabled. 1: Buffer access is enabled.	R

Notes:
1. Only 0 can be read and 1 can be written.
2. Write 1 to the SQCLR or SQSET bit while PID is NAK. Before modifying these bits after modifying the PID bits for the selected pipe from BUF to NAK, check that the PBUSY bit is 0. However, if the PID bits have been modified to NAK by the USB module, checking the PBUSY bit through software is not necessary.
3. Modify the ACLRM bit while PID is NAK and before the pipe is selected by the CURPIPE bits. Before modifying this bit after modifying the PID bits for the selected pipe from BUF to NAK, check that the PBUSY bit is 0. However, if the PID bits have been modified to NAK by the USB module, checking the PBUSY bit through software is not necessary.

PID[1:0] Bits (Response PID)

The PID[1:0] bits specify the response type for the next transaction of the relevant pipe.
The default setting of the PID[1:0] bits is NAK. Modify the setting of the PID[1:0] bits to BUF to use the relevant pipe for USB transfer. Table 26.9 and Table 26.10 show the basic operation (operation when there are no errors in the transmitted and received packets) of the USB module depending on the PID bit setting.
After modifying the setting of the PID[1:0] bits through software from BUF to NAK during USB communication using the relevant pipe, check that the PBUSY bit is 1 to see if USB transfer using the relevant pipe has actually entered the NAK state. However, if the PID bits have been modified to NAK by the USB module, checking the PBUSY bit through software is not necessary.
The USB module modifies the setting of the PID[1:0] bits in the following cases.

- The USB module sets PID to STALL (11) on receiving a data packet with a payload exceeding the maximum packet size of the relevant pipe.
- The USB module sets PID to NAK on detecting a USB bus reset when the function controller function is selected.
- The USB module sets PID to NAK on detecting a receive error, such as a CRC error, three consecutive times when the host controller function is selected.
- The USB module sets PID to STALL (11) on receiving the STALL handshake when the host controller function is selected.

To specify each response type, set the PID[1:0] bits as follows.

- To make a transition from NAK (00) to STALL, set 10.
- To make a transition from BUF (01) to STALL, set 11.
- To make a transition from STALL (11) to NAK, set 10 and then 00.
- To make a transition from STALL to BUF, set 00 (NAK) and then 01 (BUF).

PBUSY Bit (Pipe Busy)

The PBUSY bit indicates whether the relevant pipe is being currently used or not for the transaction.
The USB module modifies the PBUSY bit from 0 to 1 upon start of the USB transaction for the relevant pipe, and modifies the PBUSY bit from 1 to 0 upon completion of one transaction.
Reading the PBUSY bit after software has set PID to NAK allows checking whether modification of the pipe settings is possible.

SQMON Bit (Toggle Bit Confirmation)

The SQMON bit indicates the expected value of the sequence toggle bit for the next transaction of the relevant pipe.
The USB module allows the SQMON bit to toggle upon normal completion of the transaction. However, the SQMON bit is not allowed to toggle when a DATA-PID disagreement occurs during the transfer in the receiving direction.

SQSET Bit (Toggle Bit Set)

The SQSET bit should be set to 1 to set DATA1 as the expected value of the sequence toggle bit for the next transaction of the relevant pipe.
Setting the SQSET bit through software allows the USB module to set DATA1 as the expected value of the sequence toggle bit of the relevant pipe. The USB module always sets the SQSET bit to 0.

SQCLR Bit (Toggle Bit Clear)

The SQCLR bit should be set to 1 to clear the expected value (to set DATA0 as the expected value) of the sequence toggle bit for the next transaction of the relevant pipe.
Setting the SQCLR bit to 1 through software allows the USB module to set DATA0 as the expected value of the sequence toggle bit of the relevant pipe. The USB module always sets the SQCLR bit to 0.

ACLRM Bit (Auto Buffer Clear Mode)

Enables or disables auto buffer clear mode for the relevant pipe. To delete the information in the FIFO buffer assigned to the relevant pipe completely, write 1 and then 0 to the ACLRM bit continuously.
Table 26.13 shows the information cleared by writing 1 and 0 to the ACLRM bit continuously and the cases in which clearing the information is necessary.

BSTS Bit (Buffer Status)

Indicates the FIFO buffer status for the relevant pipe.
The meaning of the BSTS bit depends on the settings of the DIR and BFRE bits as shown in Table 26.12.

Table 26.13 Information Cleared by USB Module by Setting ACLRM = 1

No.	Information Cleared by ACLRM Bit Manipulation	Cases in which Clearing Information is Necessary
1	All the information in the FIFO buffer assigned to the selected pipe	
2	The interval count value when the selected pipe is for interrupt transfer and the host controller function is selected	When the interval count value is to be reset
3	Internal flags concerning the BFRE bit	When the BFRE setting is modified
4	Internal flags concerning the transaction count	When the transaction count function is forcibly terminated

26.2.32 PIPEn Transaction Counter Enable Registers (PIPEnTRE) (n = 4 or 5)

Address 2E9Dh, 2E9Ch, 2EA1h, 2EA0h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	TRENB	TRCLR
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b7 to b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b8	TRCLR	Transaction Counter Clear	0: Invalid 1: The current counter value is cleared.	R/W
b9	TRENB	Transaction Counter Enable	0: Transaction counter is disabled. 1: Transaction counter is enabled.	R/W
b15 to b10	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Note:
1. Modify each bit in PIPEnTRE while PID is NAK. Before modifying these bits after modifying the PID bits for the selected pipe from BUF to NAK, check that the PBUSY bit is 0. However, if the PID bits have been modified to NAK by the USB module, checking the PBUSY bit through software is not necessary.

PIPEnTRE enables or disables the transaction counter corresponding to PIPE4 and PIPE5, and clears the transaction counter.

TRCLR Bit (Transaction Counter Clear)

Clears the current value of the transaction counter corresponding to the relevant pipe and then sets the TRCLR bit to 0.

TRENB Bit (Transaction Counter Enable)

Enables or disables the transaction counter.
For the pipe in the receiving direction, setting the TRENB bit to 1 after setting the total number of the packets to be received in the TRNCNT bits through software allows the USB module to control hardware as described below on having received the number of packets equal to the setting of the TRNCNT bits.
- While the SHTNAK bit is 1, the USB module modifies the PID bits to NAK for the corresponding pipe on having received the number of packets equal to the setting of the TRNCNT bits.
- While the BFRE bit is 1, the USB module asserts the BRDY interrupt on having received the number of packets equal to the setting of the TRNCNT bits and then reading out the last received data.

For the pipe in the transmitting direction, set the TRENB bit to 0.
When the transaction counter is not used, set the TRENB bit to 0.
When the transaction counter is used, set the TRNCNT bits before setting the TRENB bit to 1. Set the TRENB bit to 1 before receiving the first packet to be counted by the transaction counter.

26.2.33 PIPEn Transaction Counter Registers (PIPEnTRN) (n = 4 or 5)

Address 2E9Fh, 2E9Eh, 2EA3h, 2EA2h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TRNCNT [15:0]							
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	TRNCNT [15:0]							
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b15 to b0	TRNCNT [15:0]	Transaction Counter	• When written to Specifies the number of packets (transaction count) to be received by the relevant pipe. • When read from Indicates the specified number of transactions if the TRENB bit is 0. Indicates the number of currently counted transactions if the TRENB bit is 1.	R/W

PIPEnTRN is a transaction counter corresponding to PIPE4 and PIPE5.
PIPEnTRN retains the setting by a USB bus reset.

TRNCNT[15:0] Bits (Transaction Counter)

The USB module increments the value of the TRNCNT bits by one when all of the following conditions are satisfied on receiving the packet.
- TRENB = 1
- (TRNCNT set value ≠ current counter value + 1) on receiving the packet.
- The payload of the received packet agrees with the setting of the MXPS bits.

The USB module clears the value of the TRNCNT bits to 0 when any of the following conditions are satisfied.
(1) All of the following conditions are satisfied.
  - TRENB = 1
  - (TRNCNT set value = current counter value + 1) on receiving the packet.
  - The payload of the received packet agrees with the setting of the MXPS bits.
(2) All of the following conditions are satisfied.
  - TRENB = 1
  - The USB module has received a short packet.
(3) All of the following conditions are satisfied.
  - TRENB = 1
  - Software has set the TRCLR bit to 1.

For the pipe in the transmitting direction, set the TRNCNT bits to 0.
When the transaction counter is not used, set the TRNCNT bits to 0.
Setting the number of transactions to be transferred to the TRNCNT bits is only enabled when the TRENB bit in PIPEnTRE register is 0. To modify the number of transactions to be transferred, set the TRCLR bit in the PIPEnTRE register to 1 (to clear the current counter value) before setting the TRENB bit to 1.

26.2.34 Device Address n Configuration Registers (DEVADDn) (n = 0 to 5)

Address 2ED1h, 2ED0h, 2ED3h, 2ED2h, 2ED5h, 2ED4h, 2ED7h, 2ED6h, 2ED9h, ED8h, 2EDBh, 2EDAh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	USBSPD [1:0]		—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bit	Set to 0.	R/W
b5 to b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7, b6	USBSPD [1:0]	Transfer Speed of Communication Target Device	b7 b6 0 0: DEVADDn is not used 0 1: Setting prohibited 1 0: Full speed 1 1: Setting prohibited	R/W
b15 to b8	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

DEVADDn specifies the transfer speed of the peripheral device which is the communication target for PIPE0, PIPE4, or PIPE5.

When the host controller function is selected, the bits in DEVADDn should be set before starting communication using each pipe.

The bits in DEVADDn should be modified while no valid pipes are using the settings of the bits. Valid pipes refer to the pipes satisfying both of the following conditions:

- DEVADDn is selected by the DEVSEL bits.
- The PID bits are set to BUF for the selected pipe or the selected pipe is the DCP with the SUREQ bit set to 1.

USBSPD[1:0] Bits (Transfer Speed of Communication Target Device)

Specifies the USB transfer speed of the communication target peripheral device.

Set these bits to 10b when a full-speed device is connected via the HUB.

When the host controller function is selected, the USB module refers to the setting of the USBSPD[1:0] bits to generate packets.

When the function controller function is selected, set these bits to 00b.

26.2.35 USB Module Control Register (USBMC)

Address 2F00h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	PXXCON	VDDUSBE	—	—	—
After Reset	0	0	X	1	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	—			
b3	VDDUSBE	USB internal power supply control 0	0: USB internal power supply stopped, USB_VCC pin input enabled 1: 3.3 V USB internal power supply supplied	R/W
b4	PXXCON	USB internal power supply control 1	0: VDDUSBE bit disabled 1: VDDUSBE bit enabled	R/W
b5	—	Reserved bit	When read, the content is undefined.	R
b6	—	Reserved bits	Set to 0.	R/W
b7	—			

VDDUSBE Bit (USB internal power supply control 0)

When the PXXCON bit is 1 (VDDUSBE bit enabled), the VDDUSBE bit is enabled.
When the VDDUSBE bit is 0 (USB_VCC pin input enabled), pins USB_DPUPE, D+, and D- function with the external power supply level applied to the USB_VCC pin as high.
When the VDDUSBE bit is 1 (3.3 V USB internal power supply supplied), pins USB_DPUPE, D+, and D- function with the USB internal voltage level of 3.3 V as high.
The USB_VCC pin outputs 3.3 V.

PXXCON Bit (USB internal power supply control 1)

In order to use the USB function, set the PXXCON bit to 1 (VDDUSBE bit enabled).
Select the USB_VCC pin function by the VDDUSBE bit.
When not using the USB function, set the PXXCON bit to 0 (VDDUSBE bit disabled).
The USB_VCC pin outputs the VCC level. Refer to **7.6 Unassigned Pin Handling**.

26.3 Operation

26.3.1 System Control

This section describes the register settings that are necessary for initialization of this module and power consumption control.

26.3.1.1 Starting Operation

Setting the SYSCFG.USBE bit to 1 after starting the clock supply to the USB module (SYSCFG.SCKE = 1) enables and starts USB module operation.

26.3.1.2 Controller Function Selection

For the USB module, the host controller function or function controller function can be selected using the DCFM bit in SYSCFG. The DCFM bit should be modified in the initial settings immediately after a power-on reset or in the D+ pull-up-disabled (DPRPU = 0) state.

26.3.1.3 Example of USB External Connection Circuit

Figure 26.2 shows a Functional Connection Example of USB Connector in Self-Powered State (the internal power supply for the USB is used when 4.0 V ≤ VCC ≤ 5.5 V).

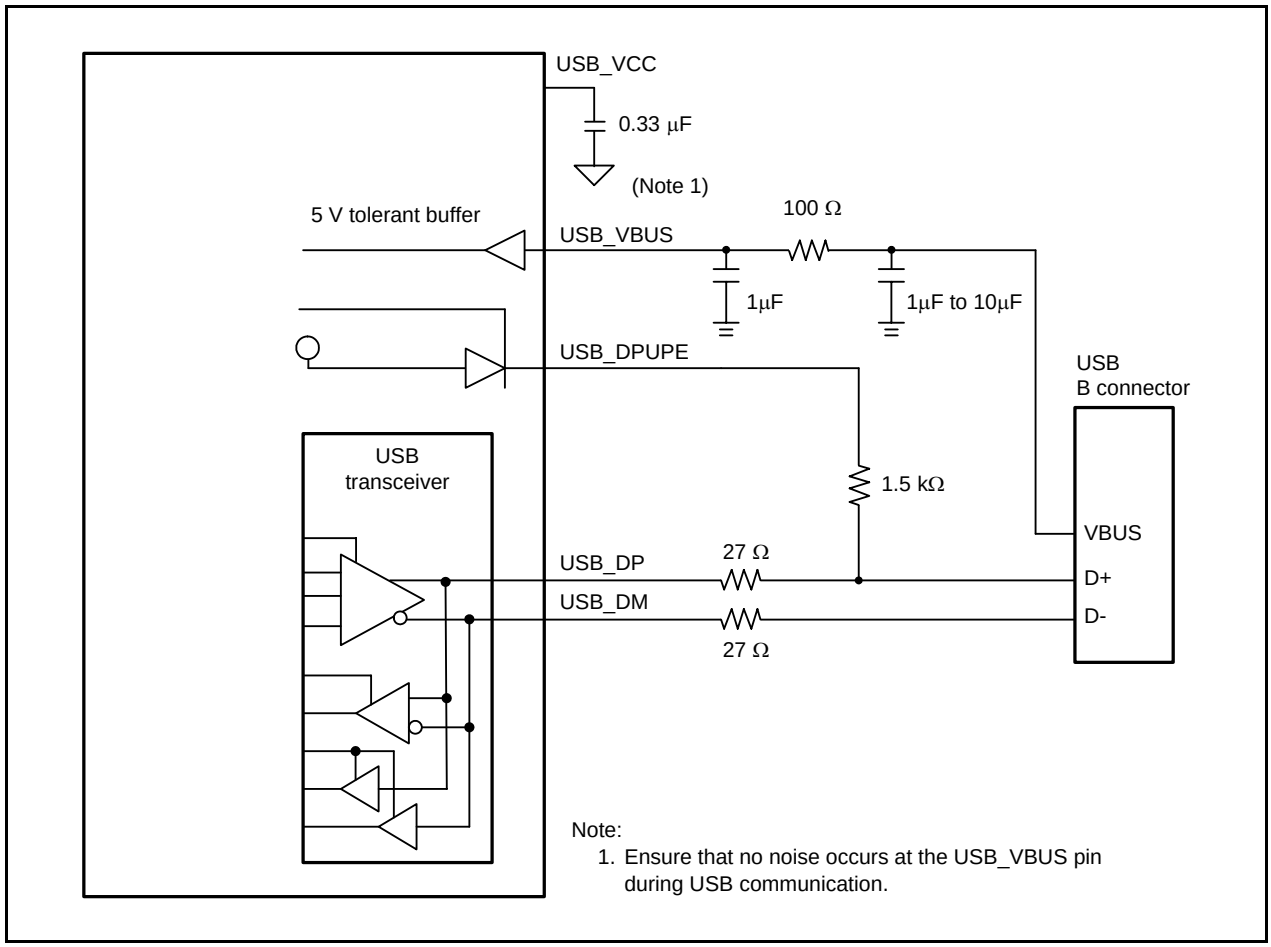


Figure 26.2 Functional Connection Example of USB Connector in Self-Powered State

Figure 26.3 shows a Host Connection Example of USB Connector.

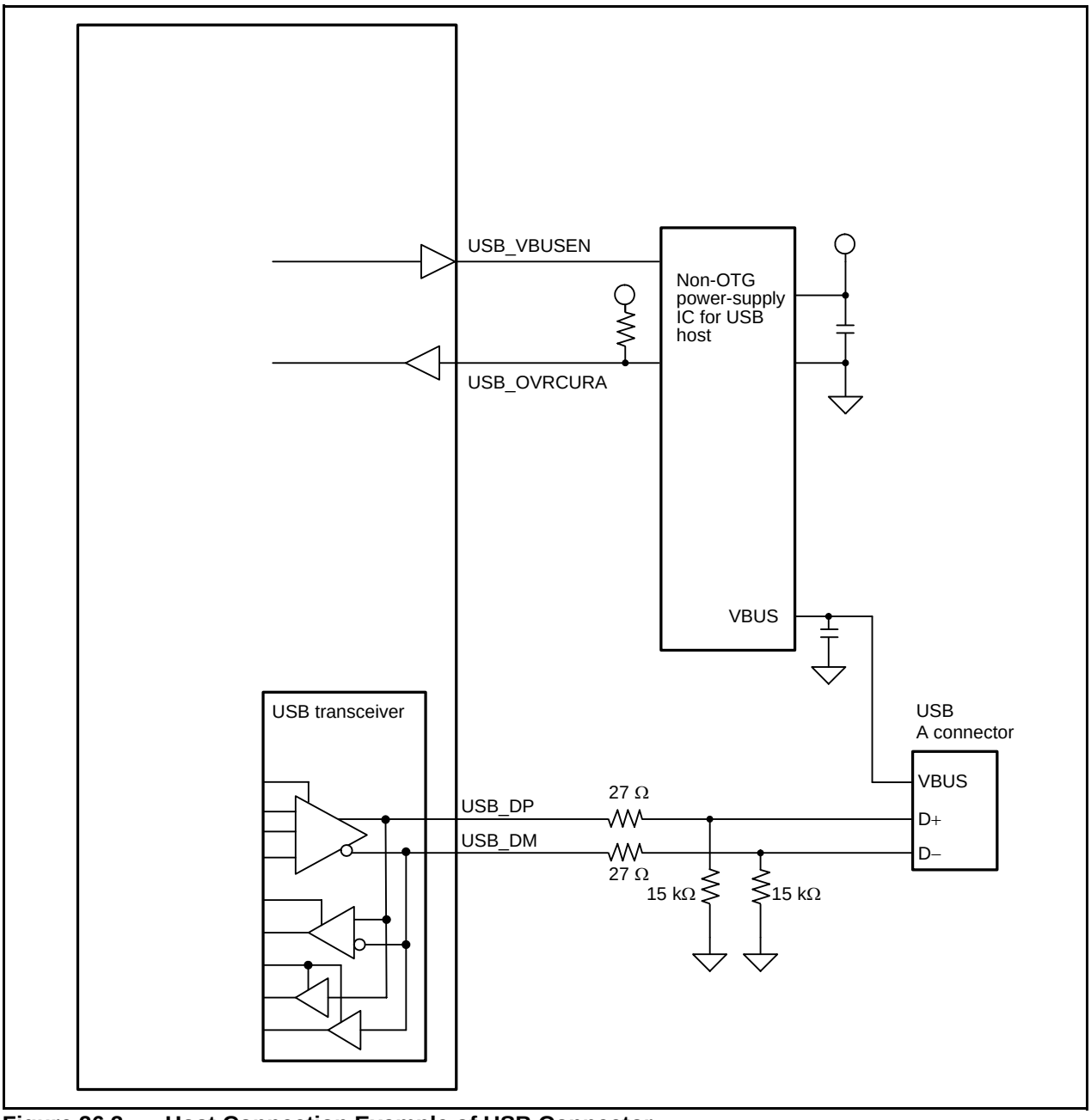


Figure 26.3 Host Connection Example of USB Connector

Figure 26.4 shows a Functional Connection Example of USB Connector in Bus-Powered State (the internal power supply for the USB cannot be used when 3.0 V ≤ VCC ≤ 3.6 V).

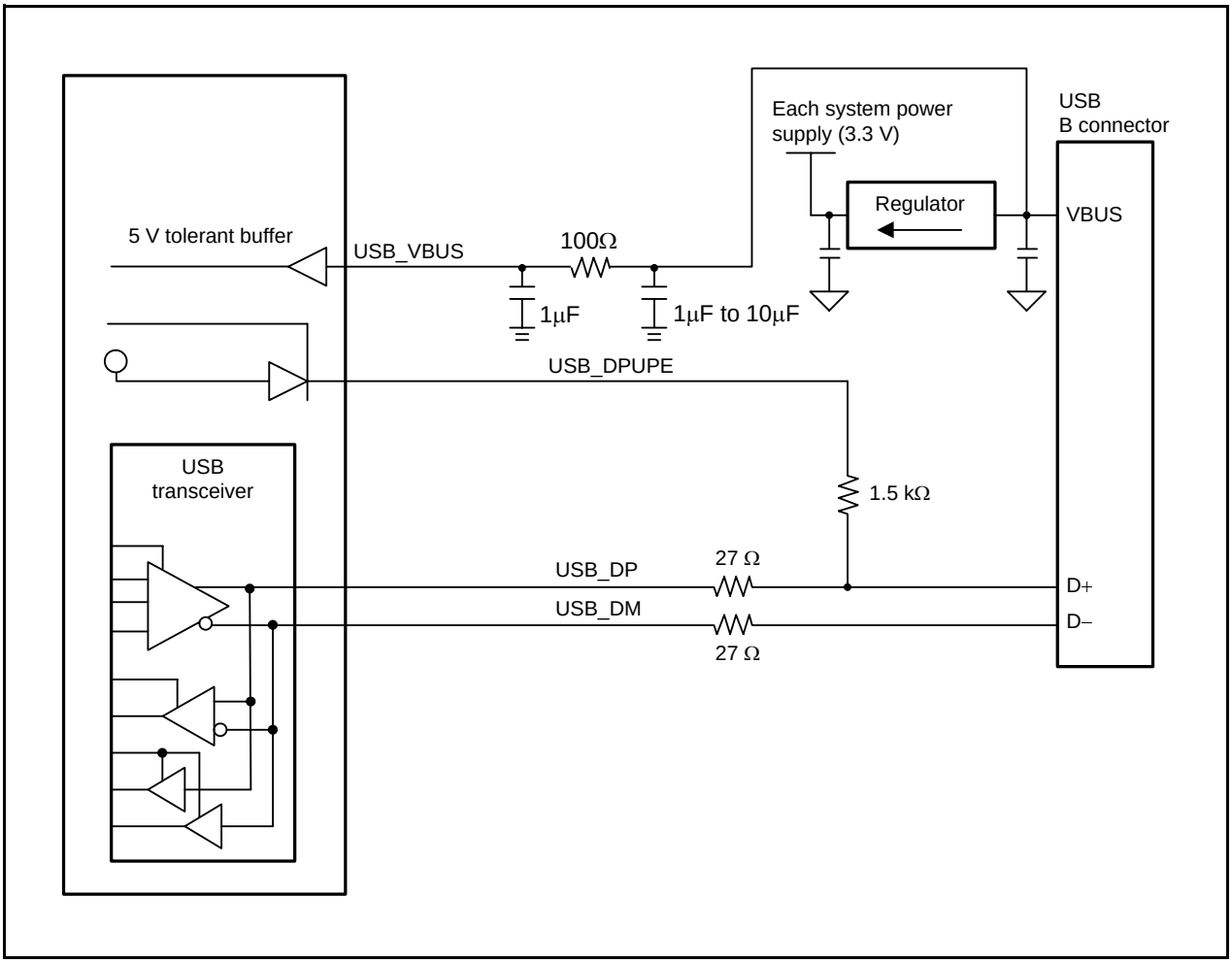


Figure 26.4 Functional Connection Example of USB Connector in Bus-Powered State

The examples of external circuits described in this section are only simplified circuits, and their operations are not guaranteed under any system.

26.3.2 Interrupt Sources

Table 26.14 lists the Interrupt Sources in the USB module.
When an interrupt generation condition is satisfied and the interrupt output is enabled using the corresponding interrupt enable register, the USB issues a USB interrupt request to the interrupt controller and an USB interrupt will be generated.

Table 26.14 Interrupt Sources

Bit to Be Set	Name	Interrupt Source	Function that Generates Interrupt	Status Flag
VBINT	VBUS interrupt	• When a change in the state of the USB_VBUS input pin has been detected (low to high or high to low)	Host/function (2)	VBSTS
RESM	Resume interrupt	• When a change in the state of the USB bus has been detected in the suspended state (J-state to K-state or J-state to SE0)	Function	—
SOFR	Frame number update interrupt	[Host controller function is selected] • When an SOF packet with a different frame number has been transmitted [Function controller function is selected] • When an SOF packet with a different frame number has been received	Host/function	—
DVST	Device state transition interrupt	• When a device state transition has been detected (any of the following conditions) A USB bus reset detected Suspend state detected SET_ADDRESS request received SET_CONFIGURATION request received	Function	DVSQ
CTRT	Control transfer stage transition interrupt	• When a stage transition has been detected in control transfer (any of the following conditions) Setup stage completed Control write transfer status stage transition Control read transfer status stage transition Control transfer completed A control transfer sequence error occurred	Function	CTSQ
BEMP	Buffer empty interrupt	• When transmission of all data in the buffer memory has been completed and the buffer has become empty • When a packet larger than the maximum packet size has been received	Host/function	BEMPSTS. PIPEBEMP
NRDY	Buffer not ready interrupt	[Host controller function is selected] • When STALL has been received from the peripheral device for the issued token • When a response has not been received correctly from the peripheral device for the issued token (no response was returned three consecutive times or a packet reception error occurred three consecutive times) [Function controller function is selected] • When NAK has been returned for an IN or OUT token while the PID bit = BUF	Host/function	NRDYSTS. PIPENRDY
BRDY	Buffer ready interrupt	• When the buffer has become ready (reading or writing is enabled)	Host/function	BRDYSTS. PIPEBRDY
OCRCR	Overcurrent input change interrupt	• When a change in the state of the USB_OVRCURA input pin has been detected (low to high or high to low)	Host	OVCMON
BCHG	Bus change interrupt	• When a change of USB bus state has been detected	Host	SYSSTS0 LNST
DTCH	Disconnection detection during full-speed operation	• When disconnection of a peripheral device has been detected in full-speed operation	Host	DCSTCTR0 RHST
ATTCH	Device connection detection	• When J-state or K-state is detected on the USB port for 2.5 s. Used for checking whether a peripheral device is connected.	Host	—
EOFERR	EOF error detection	• When an EOF error of a peripheral device has been detected	Host	—
SACK	Normal setup operation	• When the normal response (ACK) for the setup transaction has been received	Host	—
SIGN	Setup error	• When a setup transaction error (no response or ACK packet corruption) was detected three consecutive times	Host	—

Notes:
1. All bits without register name are in INTSTS0.
2. Though this interrupt can be generated while the host function is selected, it is not usually used with the host function.

Figure 26.5 shows the Circuits Related to Interrupts in the USB.

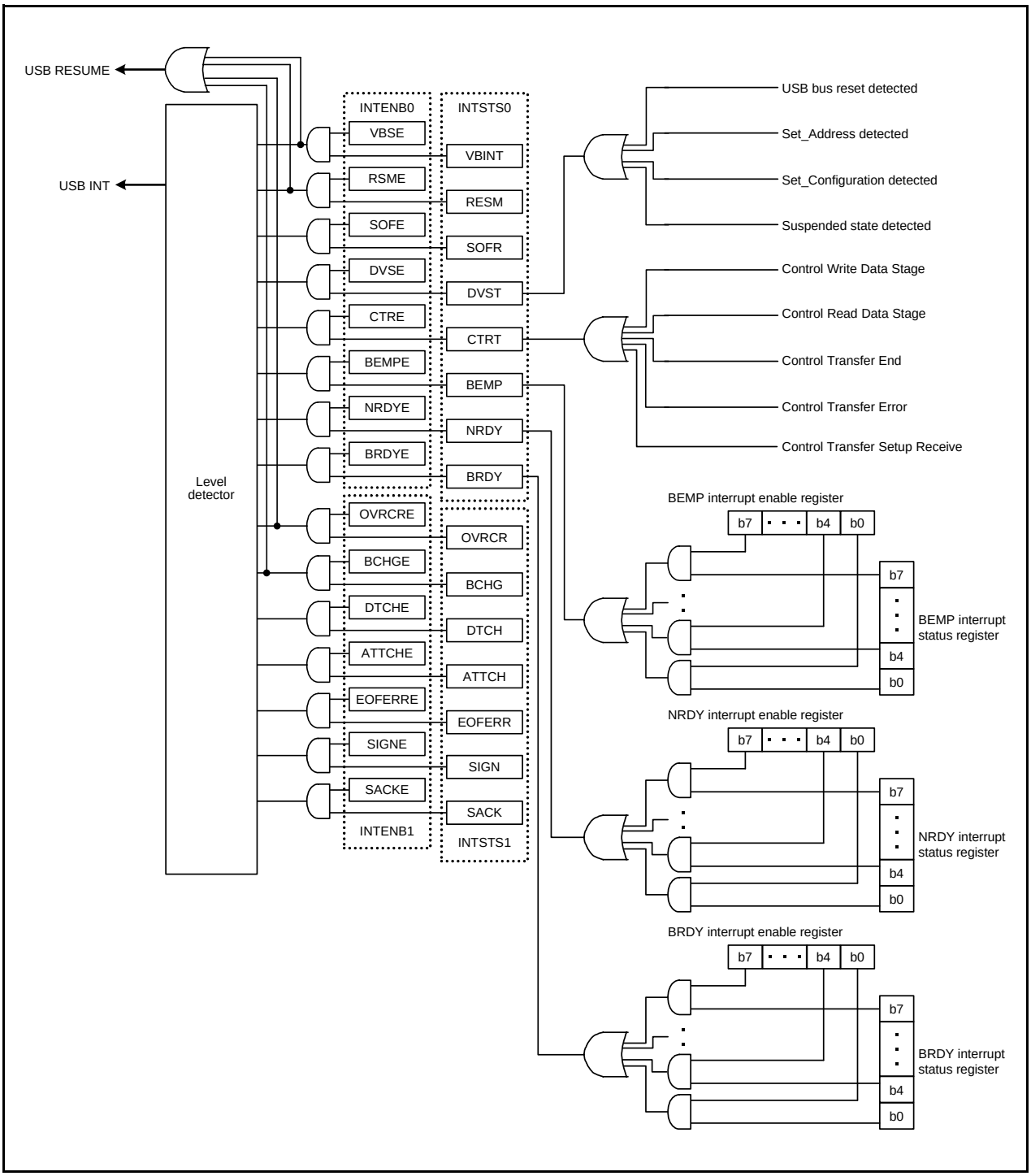


Figure 26.5 Circuits Related to Interrupts

Table 26.15 shows the USB Interrupts.

Table 26.15 USB Interrupts

Interrupt Name	Interrupt Flag	Priority
USB INT	VBUS interrupt, resume interrupt, frame number update interrupt, device state transition interrupt, control transfer stage transition interrupt, buffer empty interrupt, buffer not ready interrupt, buffer ready interrupt, overcurrent input change interrupt, bus change interrupt, disconnection detection during full-speed operation, device connection detection, EOF error detection, normal setup operation, and setup error	High ↑
USB RESUME	VBUS interrupt, resume interrupt, overcurrent input change interrupt, and bus change interrupt	↓ Low

26.3.3 Interrupts

26.3.3.1 BRDY Interrupt

The BRDY interrupt is generated when either of the host controller function or function controller function is selected. The following shows the conditions under which the USB module sets 1 to a corresponding bit in BRDYSTS. Under this condition, the USB module generates a BRDY interrupt if software has set 1 to the PIPEBRDYE bit in BRDYENB that corresponds to the pipe and 1 to the BRDYE bit in INTENB0.
The conditions for generating and clearing the BRDY interrupt depend on the settings of the BRDYM bit and BFRE bit for each pipe as described below.

(1) When BRDYM = 0 and BFRE = 0
With these settings, the BRDY interrupt indicates that the FIFO port is accessible.
On any of the following conditions, the USB module generates an internal BRDY interrupt request trigger and sets 1 to the PIPEBRDY bit corresponding to the pertinent pipe.

For the pipe in the transmitting direction:
- When software changes the DIR bit from 0 to 1.
- When packet transmission is completed using the pertinent pipe while write-access from the CPU to the FIFO buffer for the pertinent pipe is disabled (when the BSTS bit is read as 0).
- When one FIFO buffer is empty on completion of writing data to the other FIFO buffer in double buffer mode.
  No request trigger is generated until completion of writing data to the currently-written FIFO buffer even if transmission to the other FIFO buffer is completed.
- When 1 is written to the ACLRM bit, which causes the FIFO buffer to make transition from the write-disabled to write-enabled state.

No request trigger is generated for the DCP (that is, during data transmission for control transfers).

For the pipe in the receiving direction:
- When packet reception is completed successfully thus enabling the FIFO buffer to be read while read-access from the CPU to the FIFO buffer for the pertinent pipe is disabled (when the BSTS bit is read as 0).
  No request trigger is generated for the transaction in which DATA-PID disagreement has occurred.
- When one FIFO buffer is read-enabled on completion of reading data from the other FIFO buffer in double buffer mode.
  No request trigger is generated until completion of reading data from the currently-read FIFO buffer even if reception by the other FIFO buffer is completed.

When the function controller function is selected, the BRDY interrupt is not generated in the status stage of control transfers.
The PIPEBRDY interrupt status of the pertinent pipe can be cleared to 0 by writing 0 to the corresponding PIPEBRDY bit in BRDYSTS through software. In this case, 1s should be written to the PIPEBRDY bits for the other pipes.
Be sure to clear the BRDY status before accessing the FIFO buffer.

(2) When BRDYM = 0 and BFRE = 1

With these settings, the USB module generates a BRDY interrupt on completion of reading all data for a single transfer using the pipe in the receiving direction, and sets 1 to the bit in BRDYSTS corresponding to the pertinent pipe.

On any of the following conditions, the USB module determines that the last data for a single transfer has been received.

- When a short packet including a zero-length packet is received.
- When the transaction counter register (TRNCNT bits) is used and the number of packets specified by the TRNCNT bits are completely received.

When the pertinent data is completely read out after any of the above conditions has been satisfied, the USB module determines that all data for a single transfer has been completely read out.

When a zero-length packet is received while the FIFO buffer is empty, the USB module determines that all data for a single transfer has been completely read out upon passing the zero-length packet data to the CPU. In this case, to start the next transfer, write 1 to the BCLR bit in the corresponding FIFOCTR register through software.

With these settings, the USB module does not detect a BRDY interrupt for the pipe in the transmitting direction.

The PIPEBRDY interrupt status of the pertinent pipe can be cleared to 0 by writing 0 to the corresponding PIPEBRDY bit through software. In this case, 1s should be written to the PIPEBRDY bits for the other pipes.

In this mode, the BFRE bit setting should not be modified until all data for a single transfer has been processed. When it is necessary to modify the BFRE bit before completion of processing, all FIFO buffers for the pertinent pipe should be cleared using the ACLRM bit.

(3) When BRDYM = 1 and BFRE = 0

With these settings, the PIPEBRDY values are linked to the BSTS bit setting for each pipe. In other words, the BRDY interrupt status bits (PIPEBRDY) are set to 1 or 0 by the USB module depending on the FIFO buffer status.

- For the pipe in the transmitting direction:
  The BRDY interrupt status bits are set to 1 when the FIFO buffer is ready for write access, and are set to 0 when it is not ready.
  However, the BRDY interrupt is not generated even if the DCP in the transmitting direction is ready for write access.

- For the pipe in the receiving direction:
  The BRDY interrupt status bits are set to 1 when the FIFO buffer is ready for read access, and are set to 0 when all data have been read (not ready for read access).
  When a zero-length packet is received while the FIFO buffer is empty, the pertinent bit is set to 1 and the BRDY interrupt is continuously generated until BCLR = 1 is written through software.
  With this setting, the PIPEBRDY bit cannot be cleared to 0 through software.
  When BRDYM is set to 1, all BFRE bits (for all pipes) should be cleared to 0.

Figure 26.6 shows the Timing of BRDY Interrupt Generation.

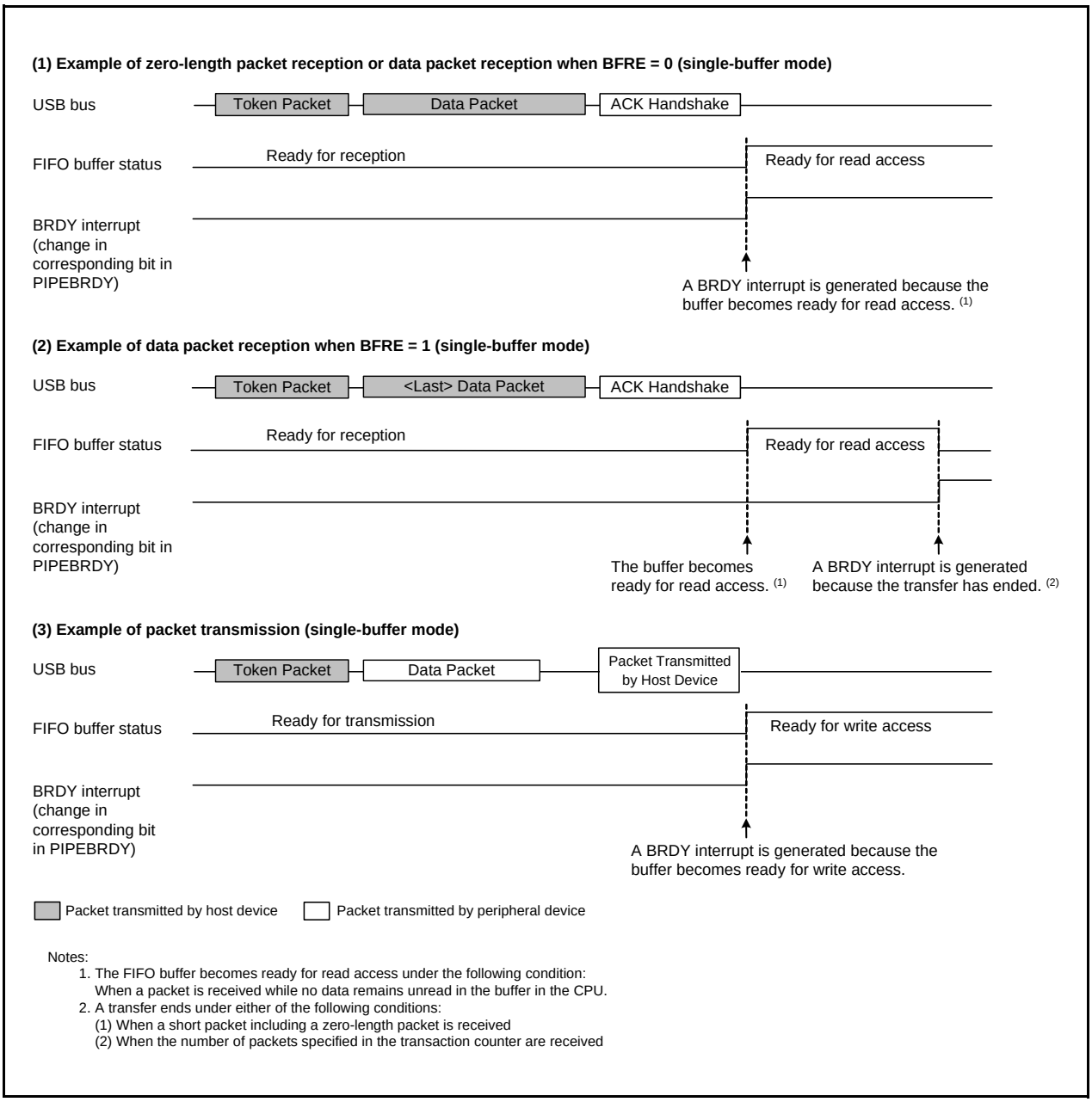


Figure 26.6 Timing of BRDY Interrupt Generation

The condition that USB module clears the BRDY bit in INTSTS0 depends on the SOFCFG.BRDYM bit setting. Table 26.16 shows the Condition for Clearing BRDY Bit.

Table 26.16 Condition for Clearing BRDY Bit

BRDYM	Condition for Clearing BRDY Bit
0	The USB module clears the BRDY bit in INTSTS0 when software has cleared all bits in BRDYSTS.
1	The USB module clears the BRDY bit in INTSTS0 when the BSTS bits for all piles have become 0.

26.3.3.2 NRDY Interrupt

On generating an internal NRDY interrupt request for the pipe whose PID bits are set to BUF by software, the USB module sets the corresponding PIPENRDY bit in NRDYSTS to 1. If the corresponding bit in NRDYENB has been set to 1 by software, the USB module sets the NRDY bit in INTSTS0 to 1 and generates a USB interrupt.
The following describes the conditions on which the USB module generates the internal NRDY interrupt request for a given pipe.
Note that the internal NRDY interrupt request is not generated during setup transaction execution when the host controller function is selected. During setup transactions when the host controller function is selected, the SACK or SIGN interrupt is detected.
The internal NRDY interrupt request is not generated during status stage execution of the control transfer when the function controller function is selected.

(1) When Host Controller Function is Selected

- For the pipe in the transmitting direction:
  On any of the following conditions, the USB module detects an NRDY interrupt.
  - During communications other than setup transactions, when any combination of the following two cases occur three consecutive times: 1) no response is returned from the peripheral device (when timeout is detected before detection of the handshake packet from the peripheral device) and 2) an error is detected in the packet from the peripheral device.
    In this case, the USB module sets the corresponding PIPENRDY bit to 1 and modifies the setting of the PID bits of the corresponding pipe to NAK.
  - During communications other than setup transactions, when the STALL handshake is received from the peripheral device
  - In this case, the USB module sets the corresponding PIPENRDY bit to 1 and modifies the setting of the PID bits of the corresponding pipe to STALL (11b).

- For the pipe in the receiving direction:
  - When any combination of the following two cases occur three consecutive times: 1) no response is returned from the peripheral device for the IN token issued by the USB module (when timeout is detected before detection of the DATA packet from the peripheral device) and 2) an error is detected in the packet from the peripheral device.
    In this case, the USB module sets the PIPENRDY bit corresponding to the pipe to 1 and modifies the setting of the PID bits of the corresponding pipe to NAK.
  - When the STALL handshake is received.
    In this case, the USB module sets the PIPENRDY bit corresponding to the pipe to 1 and modifies the setting of the PID bits of the corresponding pipe to STALL.

(2) When Function Controller Function is Selected

- For the pipe in the transmitting direction:
  - When an IN token is received while there is no data to be transmitted in the FIFO buffer.
    In this case, the USB module generates a NRDY interrupt request at the reception of the IN token and sets the PIPENRDY bit to 1.

- For the pipe in the receiving direction:
  - When an OUT token is received while there is no space available in the FIFO buffer.
    The USB module generates a NRDY interrupt request when a NAK handshake is transferred after the data following the OUT token is received, and sets the PIPENRDY bit to 1.
    However, during re-transmission (due to DATA-PID disagreement), the NRDY interrupt request is not generated. In addition, if an error occurs in the DATA packet, the NRDY interrupt request is not generated.

Figure 26.7 shows the Timing of NRDY Interrupt Generation (When Function Controller Function is Selected).

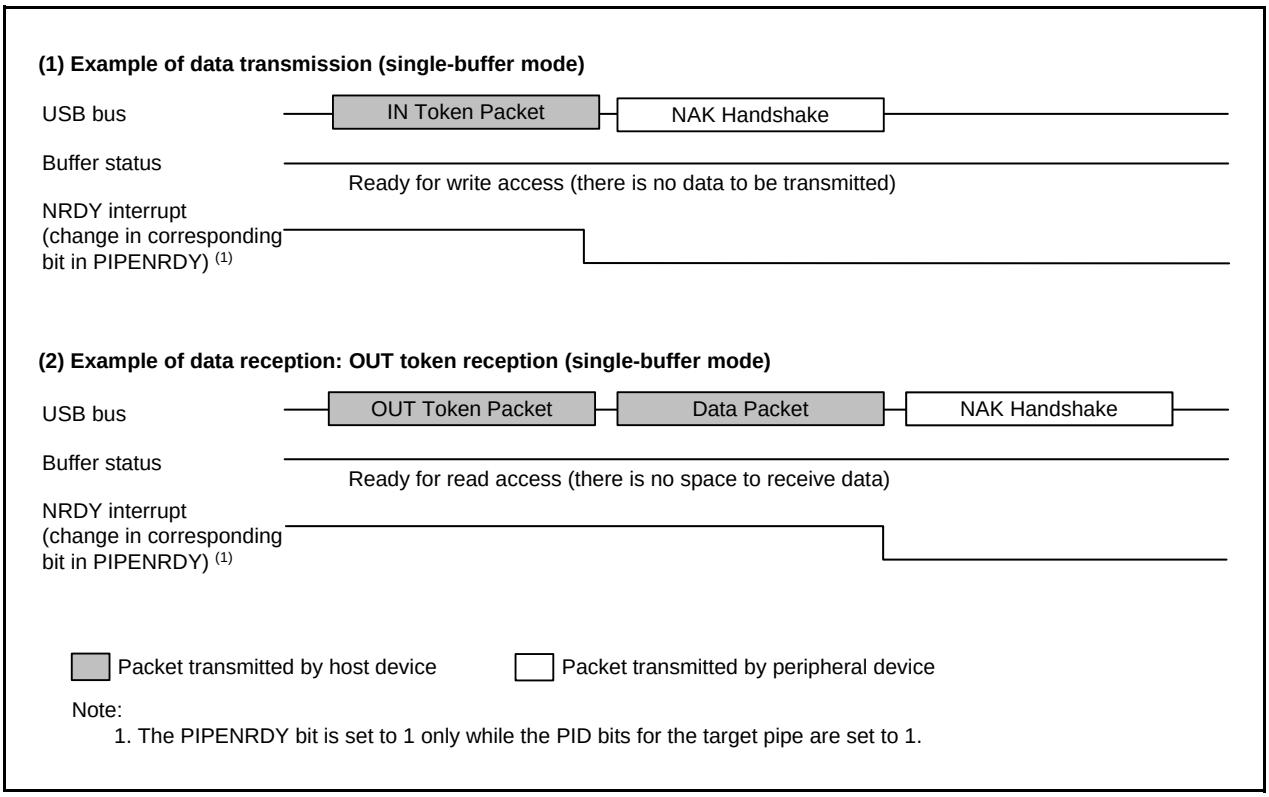


Figure 26.7 Timing of NRDY Interrupt Generation (When Function Controller Function is Selected)

26.3.3.3 BEMP Interrupt

On detecting a BEMP interrupt for the pipe whose PID bits are set to BUF by software, the USB module sets the corresponding PIPEBEMP bit in BEMPSTS to 1. If the corresponding bit in BEMPENB has been set to 1 by software, the USB module sets the BEMP bit in INTSTS0 to 1 and generates a USB interrupt.

The following describes the conditions on which the USB module generates an internal BEMP interrupt request.

- For the pipe in the transmitting direction:
  - When the FIFO buffer of the corresponding pipe is empty on completion of transmission (including zero-length packet transmission).
    In single buffer mode, an internal BEMP interrupt request is generated simultaneously with the BRDY interrupt for the pipe other than DCP. However, the internal BEMP interrupt request is not generated on any of the following conditions.
  - When software has already started writing data to the FIFO buffer of the CPU on completion of transmitting data from one FIFO buffer in double buffer mode.
  - When the buffer is cleared (emptied) by setting the ACLRM or BCLR bit to 1.
  - When IN transfer (zero-length packet transmission) is performed during the control transfer status stage while the function controller function is selected.

- For the pipe in the receiving direction:
  In this case, the USB module generates a BEMP interrupt request, sets the corresponding BEMPSTS.PIPEnBEMP bit to 1, discards the received data, and modifies the setting of the PID bits of the corresponding pipe to STALL (11b).
  Here, the USB module returns no response when used as the host controller, and returns STALL response when used as the function controller.
  However, the internal BEMP interrupt request is not generated on any of the following conditions.
  - When a CRC error or a bit stuffing error is detected in the received data.
  - When a setup transaction is being performed,
    Writing 0 to the BEMPSTS.PIPEnBEMP bit clears the status.
    Writing 1 to the BEMPSTS.PIPEnBEMP bit has no effect.

Figure 26.8 shows the Timing of BEMP Interrupt Generation (When Function Controller Function is Selected).

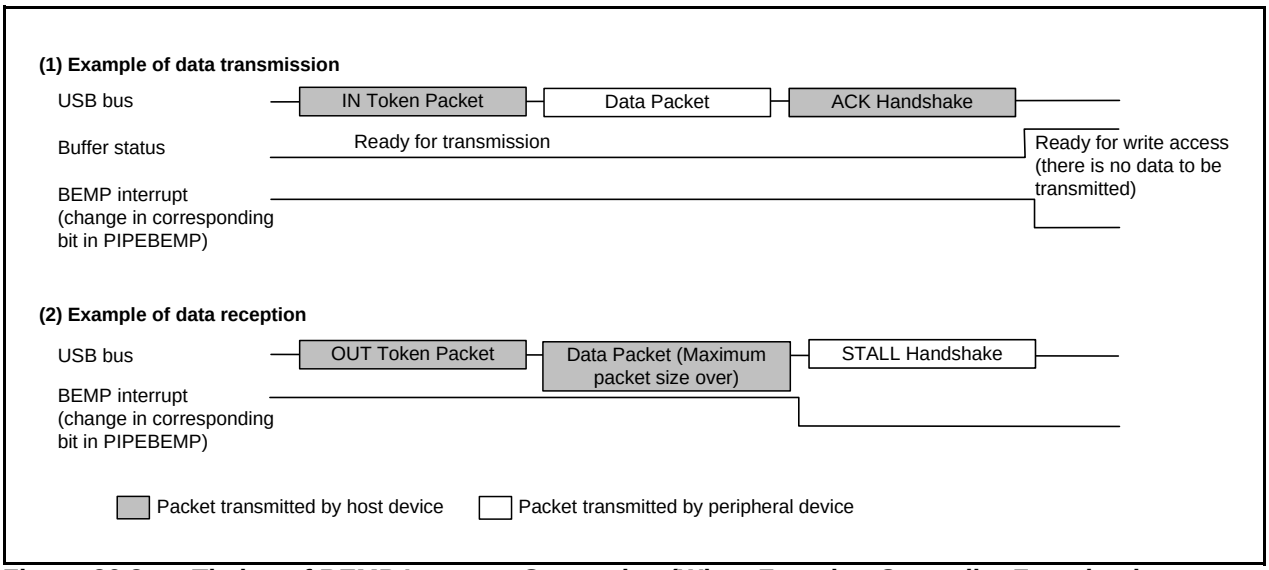


Figure 26.8 Timing of BEMP Interrupt Generation (When Function Controller Function is Selected)

26.3.3.4 Device State Transition Interrupt

Figure 26.9 is a diagram of Device State Transitions in the USB module. The USB module controls device state and generates device state transition interrupts. However, recovery from the suspended state (resume signal detection) is detected by means of the resume interrupt. The device state transition interrupts can be enabled or disabled individually using INTENB0. The device state to which a transition was made can be confirmed using the DVSQ bits in INTSTS0.

When a transition is made to the default state, a device state transition interrupt is generated after a USB bus reset is detected.

Device state can be controlled only when the function controller function is selected. The device state transition interrupts can also be generated only when the function controller function is selected.

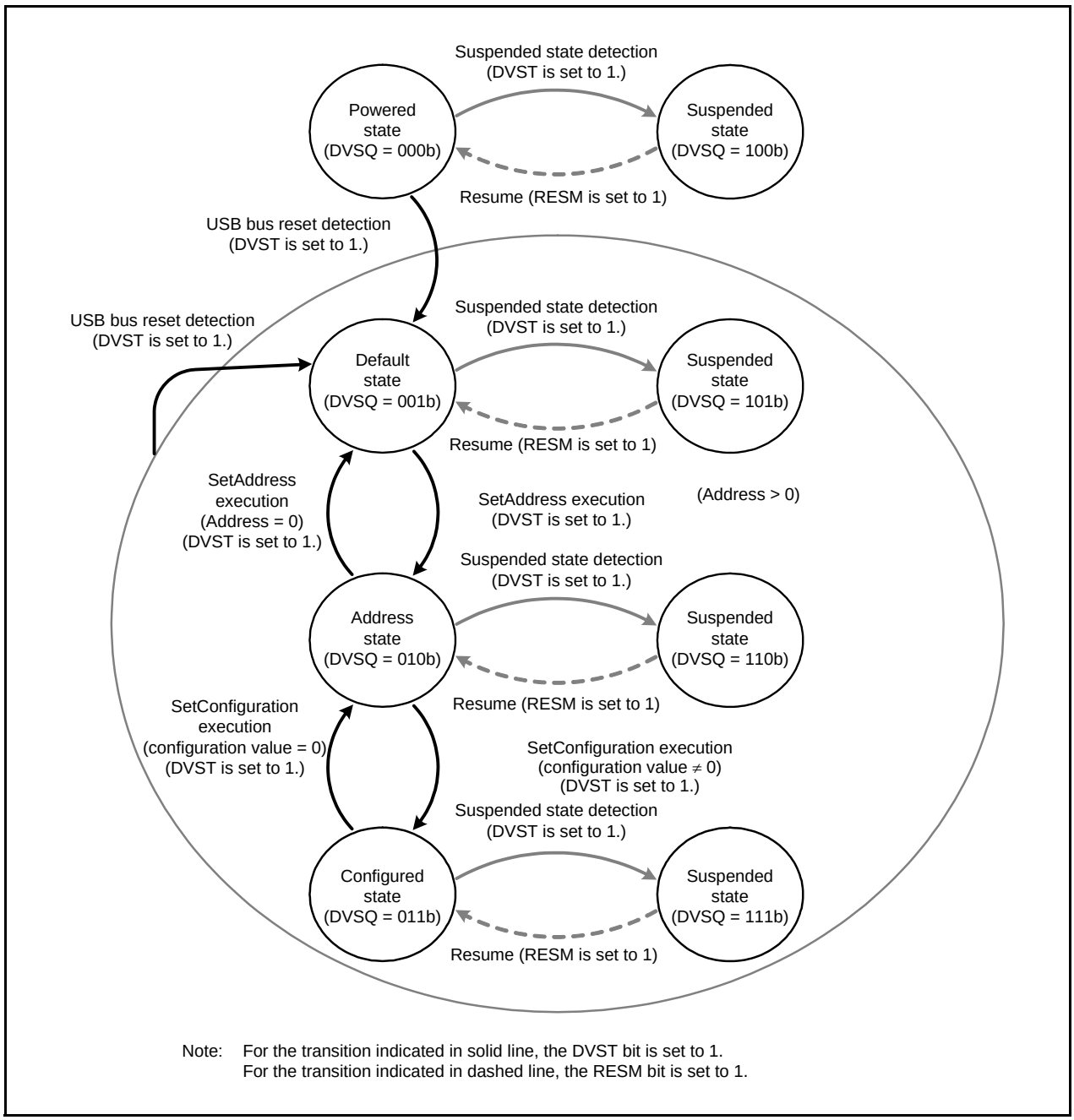


Figure 26.9 Device State Transitions

26.3.3.5 Control Transfer Stage Transition Interrupt

Figure 26.10 is a diagram of Control Transfer Stage Transitions in the USB module. The USB module controls the control transfer sequence and generates control transfer stage transition interrupts. The control transfer stage transition interrupts can be enabled or disabled individually using INTENB0. The transfer stage to which a transition was made can be confirmed using the CTSQ bits in INTSTS0.
Control transfer stage transition interrupts are generated only when the function controller function is selected. The control transfer sequence errors are listed below. If an error occurs, the PID bits in DCPCTR are set to 1xb (STALL response).
During control read transfer:

- An OUT token is received while no data has been transferred for the IN token at the data stage.
- An IN token is received at the status stage.
- A data packet with DATAPID = DATA0 is received at the status stage.

During control write transfer:

- An IN token is received while no ACK response has been returned for the OUT token at the data stage.
- A data packet with DATAPID = DATA0 is received for the first data packet at the data stage.
- An OUT token is received at the status stage

During no-data control transfers:

- An OUT token is received at the status stage.

At the control write transfer data stage, if the number of receive data exceeds the wLength value of the USB request, it cannot be recognized as a control transfer sequence error. At the control read transfer status stage, packets other than zero-length packets are received by an ACK response and the transfer ends normally.
When a CTRT interrupt occurs in response to a sequence error (SERR = 1), the CTSQ = 110 value is retained until CTRT = 0 is written from the system (the interrupt status is cleared). Therefore, while CTSQ = 110 is being held, the CTRT interrupt that ends the setup stage will not be generated even if a new USB request is received. (The USB module retains the setup stage end, and after the interrupt status has been cleared by software, a setup stage end interrupt is generated.)

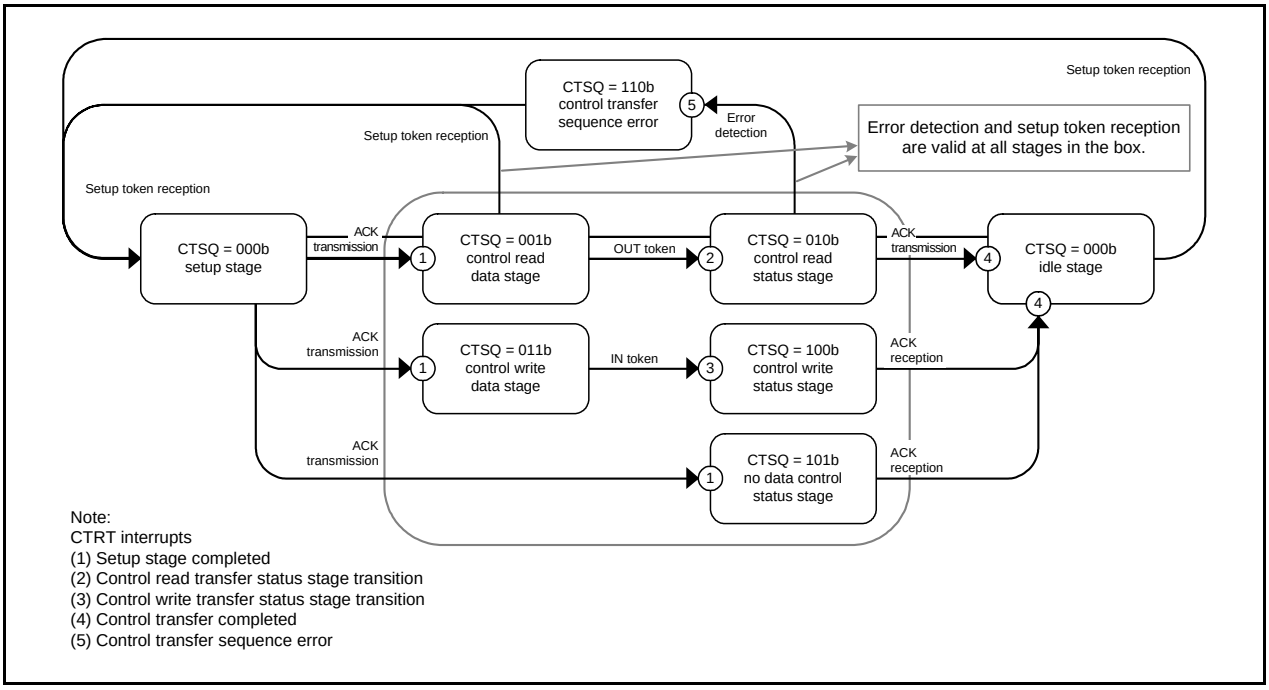


Figure 26.10 Control Transfer Stage Transitions

26.3.3.6 Frame Update Interrupt

With the host controller function selected, an interrupt is generated at the timing when the frame number is updated. With the function controller function selected, an SOFR interrupt is generated when the frame number is updated.
When the function controller function is selected, the USB module updates the frame number and generates an SOFR interrupt if it detects a new SOF packet during full-speed operation.

26.3.3.7 VBUS Interrupt

When the USB_VBUS pin level changes, a VBUS interrupt is generated. The level of the USB_VBUS pin can be checked with the VBSTS bit in INTSTS0. Whether the host controller is connected or disconnected can be confirmed using the VBUS interrupt. However, if the system is activated with the host controller connected, the first VBUS interrupt is not generated because there is no change in the USB_VBUS pin level.

26.3.3.8 Resume Interrupt

When the function controller function is selected, a resume interrupt is generated when the device state is the suspended state and the USB bus state has changed (from J-state to K-state, or from J-state to SE0). Recovery from the suspended state is detected by means of the resume interrupt.
When the host controller function is selected, no resume interrupt is generated. Use the BCHG interrupt to detect a change in the USB bus state.

26.3.3.9 OVRCR Interrupt

An OVRCR interrupt is generated when the USB_OVRCURA pin level has changed. The levels of the USB_OVRCURA pin can be checked with the OVCMON1 bit in SYSSTS0. The external power-supply IC can check whether overcurrent has been detected using the OVRCR interrupt.

26.3.3.10 BCHG Interrupt

A BCHG interrupt is generated when the USB bus state has changed. The BCHG interrupt can be used to detect whether the peripheral device is connected and can also be used to detect a remote wakeup when the host controller function is selected. The BCHG interrupt is generated regardless of whether the host controller function or function controller function is selected.

26.3.3.11 DTCH Interrupt

A DTCH interrupt is generated when disconnection of the USB bus is detected while the host controller function is selected. The USB module detects bus disconnection based on USB Specification 2.0.
After detecting a DTCH interrupt, the USB module controls hardware as described below (irrespective of the value set in the corresponding interrupt enable bit). Software should terminate all pipes in which communications are currently carried out for the pertinent port and make a transition to the wait state for bus connection to the pertinent port (wait state for ATTCH interrupt generation).

- Modifies the UACT bit for the port in which a DTCH interrupt has been detected to 0.
- Puts the port in which a DTCH interrupt has been generated into the idle state.

26.3.3.12 SACK Interrupt

A SACK interrupt is generated when an ACK response for the transmitted setup packet has been received from the peripheral device with the host controller function selected. The SACK interrupt can be used to confirm that the setup transaction has been completed successfully.

26.3.3.13 SIGN Interrupt

A SIGN interrupt is generated when an ACK response for the transmitted setup packet has not been correctly received from the peripheral device three consecutive times with the host controller function selected. The SIGN interrupt can be used to detect no ACK response transmitted from the peripheral device or corruption of an ACK packet.

26.3.3.14 ATTCH Interrupt

An ATTCH interrupt is generated when J-state or K-state of the full-speed signal level is detected on the USB port for 2.5 s with the host controller function selected. To be more specific, an ATTCH interrupt is detected on any of the following conditions.

- When K-state, SE0, or SE1 changes to J-state, and J-state continues 2.5 s.
- When J-state, SE0, or SE1 changes to K-state, and K-state continues 2.5 s.

26.3.3.15 EOFERR Interrupt

An EOFERR interrupt is generated when it is detected that communication is not completed at the EOF2 timing prescribed in USB Specification 2.0.

After detecting an EOFERR interrupt, the USB module controls hardware as described below (irrespective of the value set in the corresponding interrupt enable bit). Software should terminate all pipes in which communications are currently carried out for the pertinent port and perform re-enumeration of the pertinent port.

- Modifies the DVSTCTR0.UACT bit for the port in which an EOFERR interrupt has been detected to 0.
- Puts the port in which an EOFERR interrupt has been generated into the idle state.

26.3.4 Pipe Control

Table 26.17 lists the Pipe Settings in the USB module. With USB data transfer, data transfer has to be carried out using the logic pipe called the endpoint. The USB module has five pipes that are used for data transfer. Appropriate settings should be made for each of the pipes according to the specifications of the system.

Table 26.17 Pipe Settings

Register Name	Bit Name	Setting	Remarks
DCPCFG PIPECFG	TYPE	Specifies the transfer type	PIPE4 to PIPE7: Can be set
	BFRE	Selects the BRDY interrupt mode	PIPE4 and PIPE5: Can be set
	DBLB	Selects double buffer mode	PIPE4 and PIPE5: Can be set
	DIR	Selects transfer direction	IN or OUT can be set
	EPNUM	Endpoint number	PIPE4 to PIPE7: Can be set A value other than 0000 should be set when the pipe is used.
	SHTNAK	Selects disabled state for pipe when transfer ends	PIPE4 and PIPE5: Can be set
DCPMAXP PIPEMAXP	DEVSEL	Selects a device	Referenced only when the host controller function is selected.
	MXPS	Maximum packet size	Compliant with the USB standard.
PIPEPERI	IITV	Interval counter	PIPE4 and PIPE5: Cannot be set PIPE6 and PIPE7: Can be set (only when the host controller function has been selected)
DCPCTR PIPEnCTR	BSTS	Buffer status	For the DCP, receive buffer status and transmit buffer status are switched with the ISEL bit.
	INBUFM	IN buffer monitor	Available only for PIPE4 and PIPE5.
	SUREQ	SETUP request	Can be set only for the DCP. Can be controlled only when the host controller function has been selected.
	SUREQCLR	SUREQ clear	Can be set only for the DCP. Can be controlled only when the host controller function has been selected.
	ATREPM	Auto response mode	PIPE4 and PIPE5: Can be set Can be set only when the function controller function has been selected.
	ACLRM	Auto buffer clear	PIPE4 to PIPE7: Can be set
	SQCLR	Sequence clear	Clears the data toggle bit.
	SQSET	Sequence set	Sets the data toggle bit.
	SQMON	Sequence monitor	Monitors the data toggle bit.
	PBUSY	Pipe busy status	
	PID	Response PID	Refer to **26.3.4.6 Response PID**.
PIPEnTRE	TRENB	Transaction counter enable	PIPE4 and PIPE5: Can be set
	TRCLR	Current transaction counter clear	PIPE4 and PIPE5: Can be set
PIPEnTRN	TRNCNT	Transaction counter	PIPE4 and PIPE5: Can be set

26.3.4.1 Pipe Control Register Switching Procedures

The following bits in the pipe control registers can be modified only when USB communication is disabled (PID = NAK).

Registers that Should Not be Set in the USB Communication Enabled (PID = BUF) State:
- Bits in DCPCFG and DCPMAXP
- SQCLR and SQSET bits in DCPCTR
- Bits in PIPECFG, PIPEMAXP, and PIPEPERI
- ATREPM, ACLRM, SQCLR, and SQSET bits in PIPExCTR
- Bits in PIPExTRE and PIPExTRN

In order to modify the above bits in the USB communication enabled (PID = BUF) state, follow the procedure shown below:
1. A request to modify bits in the pipe control register occurs.
2. Modify the PID corresponding to the pipe to NAK.
3. Wait until the corresponding PBUSY bit is cleared to 0.
4. Modify the bits in the pipe control register.

The following bits in the pipe control registers can be modified only when the pertinent pipe information has not been set by the CURPIPE bit in the CFIFOSEL register.

Registers that Should Not be Set When CURPIPE in FIFO-PORT is set:
- Bits in DCPCFG and DCPMAXP
- Bits in PIPECFG, PIPEMAXP and PIPEPERI

In order to modify pipe information, the CURPIPE bits in the port select registers should be set to a pipe other than the pipe to be modified. For the DCP, the buffer should be cleared using BCLR after the pipe information is modified.

26.3.4.2 Transfer Types

The TYPE bits in PIPEPCFG are used to specify the transfer type for each pipe. The transfer types that can be set for the pipes are as follows.
- DCP: No setting is necessary (fixed at control transfer).
- PIPE4 and PIPE5: These should be set to bulk transfer.
- PIPE6 and PIPE7: These should be set to interrupt transfer.

26.3.4.3 Endpoint Number

The EPNUM bits in PIPEPCFG are used to set the endpoint number for each pipe. The DCP is fixed at endpoint 0. The other pipes can be set from endpoint 1 to endpoint 15.
- DCP: No setting is necessary (fixed at end point 0).
- PIPE4 to PIPE7: The endpoint numbers from 1 to 15 should be selected and set.
  These should be set so that the combination of the DIR bit and EPNUM bits is unique.

26.3.4.4 Maximum Packet Size Setting

The MXPS bits in DCPMAXP and PIPEMAXP are used to specify the maximum packet size for each pipe. DCP and PIPE4 and PIPE5 can be set to any of the maximum pipe sizes defined by the USB specification. For PIPE6 and PIPE7, 64 bytes are the upper limit of the maximum packet size. The maximum packet size should be set before beginning the transfer (PID = BUF).
- DCP: Set 8, 16, 32, or 64.
- PIPE4 and PIPE5: Set 8, 16, 32, or 64 when using bulk transfer.
- PIPE6 and PIPE7: Set a value between 1 and 64.

26.3.4.5 Transaction Counter (For PIPE4 and PIPE5 in Reading Direction)

When the specified number of transactions has been completed in the data packet receiving direction, the USB module recognizes that the transfer has ended. Two transaction counters are provided: one is the TRNCNT register that specifies the number of transactions to be executed and the other is the current counter that internally counts the number of executed transactions. With the SHTNAK bit set to 1, when the current counter value matches the specified number of transactions, the PID of the corresponding PIPE is set to NAK and the subsequent transfer is disabled. The transactions can be counted again from the beginning by initializing the current counter of the transaction counter function through the TRCLR bit. The information read from TRNCNT differs depending on the setting of the TRENB bit.

- TRENB = 0: The specified transaction counter value can be read.
- TRENB = 1: The current counter value indicating the internally counted number of executed transactions can be read.

When operating the TRCLR bit, the following should be noted.

- If the transactions are being counted and PID = BUF, the current counter cannot be cleared.
- If there is any data left in the buffer, the current counter cannot be cleared.

26.3.4.6 Response PID

The PID bits in DCPCTR and PIPEnCTR are used to set the response PID for each pipe.
The following shows the USB module operation with various response PID settings:

- Response PID settings when the host controller function is selected:

The response PID is used to specify the execution of transactions.
- NAK setting: Using pipes is disabled. No transaction is executed.
- BUF setting: Transactions are executed based on the status of the buffer memory.
  For OUT direction: If there are transmit data in the buffer memory, an OUT token is issued.
  For IN direction: If there is an area to receive data in the buffer memory, an IN token is issued.
- STALL setting: Using pipes is disabled. No transaction is executed.

Note: Setup transactions for the DCP are set with the SUREQ bit.

- Response PID settings when the function controller function is selected:

The response PID is used to specify the response to transactions from the host.
- NAK setting: The NAK response is always returned in response to the generated transaction.
- BUF setting: Responses are made to transactions according to the status of the buffer memory.
- STALL setting: The STALL response is always returned in response to the generated transaction.

Note: For setup transactions, an ACK response is always returned regardless of the PID setting, and the USB request is stored in the register.

The USB module may write to the PID bits, depending on the results of the transaction as described below.

- When the host controller function has been selected and the response PID is set by hardware:
- NAK setting: In the following cases, PID = NAK is set and issuing of tokens is automatically stopped:
  When an NRDY interrupt is generated. (For details, refer to **26.3.3.2 NRDY Interrupt**.)
  — If a short packet is received when the SHTNAK bit in PIPECFG has been set to 1 for bulk transfer.
  — If the transaction counting ends when the SHTNAK bit has been set to 1 for bulk transfer.
- BUF setting: There is no BUF writing by the USB module.
- STALL setting: In the following cases, PID = STALL is set and issuing of tokens is automatically stopped:
  When STALL is received in response to the transmitted token.
  When the size of the receive data packet exceeds the maximum packet size.

- When the function controller function has been selected and the response PID is set by hardware:
- NAK setting: In the following cases, PID = NAK is set and NAK is always returned in response to transactions:
  When the SETUP token is received normally (DCP only).
  If the transaction counting ends or a short packet is received when the SHTNAK bit in PIPECFG has been set to 1 for bulk transfer.

- BUF setting: There is no BUF writing by the USB module.
- STALL setting: In the following cases, PID = STALL is set and STALL is always returned in response to transactions:
  When a maximum packet size exceeded error is detected in the received data packet.
  When a control transfer sequence error has been detected (DCP only).

26.3.4.7 Data PID Sequence Bit

The USB module automatically toggles the sequence bit in the data PID when data is transferred successfully in the control transfer data stage, bulk transfer, and interrupt transfer. The sequence bit of the next data PID to be transmitted can be confirmed with the SQMON bit in DCPCTR and PIPEnCTR. When data is transmitted, the sequence bit switches at the timing of ACK handshake reception. When data is received, the sequence bit switches at the timing of ACK handshake transmission. The SQCLR bit in DCPCTR and the SQSET bit in PIPEnCTR can be used to change the data PID sequence bit.

When the function controller function has been selected and control transfer is used, the USB module automatically sets the sequence bit when a stage transition is made. DATA0 is returned when the setup stage is ended and DATA1 is returned in a status stage. Therefore, software settings are not required. However, when the host controller function has been selected and control transfer is used, the sequence bit should be set by software at a stage transition.

For the ClearFeature request transmission or reception, the data PID sequence bit should be set by software regardless of whether the host controller function or function controller function is selected.

26.3.4.8 Response PID = NAK Function

The USB module has a function that disables pipe operation (PID response = NAK) at the timing at which the final data packet of a transaction is received (the USB module automatically distinguishes this based on reception of a short packet or the transaction counter) by setting the SHTNAK bit in PIPECFG to 1.

When the double buffer mode is being used for the buffer memory, using this function enables reception of data packets in transfer units. If pipe operation has been disabled, software should set the pipe to the enabled state again (PID response = BUF).

The response PID = NAK function can be used only when bulk transfers are used.

26.3.4.9 Auto Response Mode

With the pipes for bulk transfer (PIPE4 and PIPE5), when the ATREPM bit in PIPEnCTR is set to 1, a transition is made to auto response mode. During an OUT transfer (DIR = 0), OUT-NAK mode is entered, and during an IN transfer (DIR = 1), null auto response mode is entered.

26.3.4.10 OUT-NAK Mode

With the pipes for bulk OUT transfer, NAK is returned in response to an OUT token and an NRDY interrupt is output when the ATREPM bit is set to 1. To make a transition from normal mode to OUT-NAK mode, OUT-NAK mode should be specified in the pipe operation disabled state (response PID = NAK) before enabling pipe operation (response PID = BUF). After pipe operation has been enabled, OUT-NAK mode becomes valid. However, if an OUT token is received immediately before pipe operation is disabled, the token data is normally received, and an ACK is retuned to the host.

To make a transition from OUT-NAK mode to normal mode, OUT-NAK mode should be canceled in the pipe operation disabled state (response PID = NAK) before enabling pipe operation (response PID = BUF). In normal mode, reception of OUT data is enabled.

26.3.4.11 Null Auto Response Mode

With the pipes for bulk IN transfer, zero-length packets are continuously transmitted when the ATREPM bit is set to 1.

To make a transition from normal mode to null auto response mode, null auto response mode should be set in the pipe operation disabled state (response PID = NAK) before enabling pipe operation (response PID = BUF). After pipe operation has been enabled, null auto response mode becomes valid. Before setting null auto response mode, INBUFM = 0 should be confirmed because the mode can be set only when the buffer is empty. If the INBUFM bit is 1, the buffer should be emptied with the ACLRM bit. While a transition to null auto response mode is being made, data should not be written from the FIFO port.

To make a transition from null auto response mode to normal mode, pipe operation disabled state (response PID = NAK) should be retained for the period of zero-length packet transmission (about 10 µs) before canceling null auto response mode. In normal mode, data can be written from the FIFO port; therefore, packet transmission to the host is enabled by enabling pipe operation (response PID = BUF).

26.3.5 FIFO Buffer Memory

26.3.5.1 FIFO Buffer Memory

The USB module has FIFO buffer memory for data transfer. The memory area used for each pipe is managed by the USB module. The FIFO buffer memory has two states depending on whether the access right is assigned to the system (CPU side) or the USB module (SIE side).

• Buffer Status

Table 26.18 and Table 26.19 show the buffer status in the USB module. The buffer memory status can be confirmed using the BSTS bit in DCPCTR and the INBUFM bit in PIPEnCTR. The access direction for the buffer memory can be specified using either the DIR bit in PIPEnCFG or the ISEL bit in CFIFOSEL (when DCP is selected).

The INBUFM bit is valid for PIPE4 and PIPE5 in the transmitting direction.

When a transmitting pipe uses the double buffer configuration, software can read the BSTS bit to monitor the buffer memory status on the CPU side and the INBUFM bit to monitor the buffer memory status on the SIE side. When the BEMP interrupt may not show the buffer empty status because the write access to the FIFO port by the CPU is slow, software can use the INBUFM bit to confirm the end of transmission.

Table 26.18 Buffer Status Indicated by BSTS Bit

ISEL or DIR	BSTS	Buffer Memory Status
0 (receiving direction)	0	There is no received data, or data is being received. Reading from the FIFO port is disabled.
0 (receiving direction)	1	There is received data, or a zero-length packet has been received. Reading from the FIFO port is allowed. Note that when a zero-length packet is received, reading is not possible and the buffer must be cleared.
1 (transmitting direction)	0	The transmission has not been completed. Writing to the FIFO port is disabled.
1 (transmitting direction)	1	The transmission has been completed. CPU write is allowed.

Table 26.19 Buffer Status Indicated by INBUFM Bit

DIR	INBUFM	Buffer Memory Status
0 (receiving direction)	Invalid	Invalid
1 (transmitting direction)	0	The transmission has been completed. There is no waiting data to be transmitted.
1 (transmitting direction)	1	The FIFO port has written data to the buffer. There is data to be transmitted.

26.3.5.2 FIFO Buffer Clearing

Table 26.20 shows the clearing of the FIFO buffer memory by the USB module. The buffer memory can be cleared using the BCLR and ACLRM bits in the port control register.

Table 26.20 Buffer Clearing Methods

FIFO Buffer Clearing Mode	Clearing Buffer Memory on CPU Side	Auto Buffer Clear Mode for Discarding All Received Packets
Register used	CFIFOCTR	PIPEnCTR
Bit used	BCLR	ACLRM
Clearing condition	Cleared by writing 1	1: Mode valid 0: Mode invalid

(1) Auto Buffer Clear Mode Function

With the USB module, all received data packets are discarded if the ACLRM bit in PIPEnCTR is set to 1. If a correct data packet has been received, the ACK response is returned to the host controller. The auto buffer clear mode function can be set only in the buffer memory reading direction.

If the ACLRM bit is set to 1 and then to 0, the buffer memory of the selected pipe can be cleared regardless of the access direction.

However, an access cycle of at least 100 ns is required for the internal hardware sequence processing time between ACLRM = 1 and ACLRM = 0.

(2) Buffer Memory Specifications (Single or Double Setting)

Either a single or double buffer configuration can be selected for PIPE4 and PIPE5, using the DBLB bit in PIPEnCFG.

26.3.5.3 FIFO Port Functions

Table 26.21 shows the FIFO Port Function Settings for the USB module. In write access, writing data until the maximum packet size is reached automatically enables transmission of the data. To enable transmission before the maximum packet size is reached, the BVAL bit in CFIFOCTR should be set to end writing. To send a zero-length packet, the BCLR bit in the register should be used to clear the buffer and then the BVAL bit set in order to end writing.

In read access, reception of new packets is automatically enabled when all data has been read. Data cannot be read when a zero-length packet has been received (DTLN = 0), so the BCLR bit in the register should be used to clear the buffer. The length of the receive data can be confirmed using the DTLN bits in CFIFOCTR.

Table 26.21 FIFO Port Function Settings

Register Name	Bit Name	Function
CFIFOSEL	RCNT	Selects DTLN read mode.
	REW	Buffer memory rewind (re-read, rewrite).
	MBW	FIFO port access bit width.
	BIGEND	Selects FIFO port endian.
	ISEL	FIFO port access direction (only for DCP).
	CURPIPE	Selects the current pipe.
CFIFOCTR	BVAL	Ends writing to the buffer memory.
	BCLR	Clears the buffer memory on the CPU side.
	DTLN	Checks the length of receive data.

(1) FIFO Port Selection

The pipe to be accessed should be selected using the CURPIPE bits in CFIFOSEL. After the pipe is selected, whether the written value can be correctly read from the CURPIPE bits should be checked. (If the previous pipe number is read, it indicates that the pipe modification is being executed by the USB controller.) Then, the FIFO port can be accessed after FRDY = 1 is checked using the CFIFO register.

In addition, the bus width to be accessed should be selected using the MBW bit. The buffer memory access direction conforms to the DIR bit in PIPEnCFG. Only for the DCP, the ISEL bit determines the direction.

(2) REW Bit

It is possible to temporarily stop access to the pipe currently being accessed, access a different pipe, and then continue processing for the current pipe again. The REW bit in CFIFOSEL is used for this processing.

If a pipe is selected through the CURPIPE bits in CFIFOSEL with the REW bit set to 1, the pointer used for reading from and writing to the buffer memory is reset, and reading or writing can be carried out from the first byte. If a pipe is selected with 0 set for the REW bit, data can be read and written in continuation from the previous selection, without the pointer being reset.

To access the FIFO port, FRDY = 1 should be checked after selecting a pipe.

26.3.6 Control Transfers (DCP)

In the data stage of control transfers, data is transferred using the default control pipe (DCP).
The DCP buffer memory is a 64-byte single buffer and is a fixed area that is shared for both control reading and control writing. The buffer memory can be accessed only through the CFIFO port.

26.3.6.1 Control Transfers when Host Controller Function is Selected

(1) Setup Stage
USQREQ, USBVAL, USBINDX, and USBLENG are the registers that are used to transmit a USB request for setup transactions. Writing setup packet data to the registers and writing 1 to the SUREQ bit in DCPCTR transmits the specified data for setup transactions. Upon completion of the transaction, the SUREQ bit is cleared to 0. The above USB request registers should not be modified while SUREQ = 1.
After the attached state of the connected function device is detected, the first setup transaction for the device should be issued by using the sequence described above with the DEVSEL bits in DCPMAXP set to 0 and the USBSPD bit in DEVADD0 set appropriately.
After the connected function device is shifted to the Address state, setup transactions should be issued by using the sequence described above with the assigned USB address set in the DEVSEL bits and the bits in DEVADDx corresponding to the specified USB address set appropriately. For example, when DEVSEL in PIPEMAXP = 0x2, make appropriate settings in DEVADD2; when DEVSEL = 0x5, make appropriate settings in DEVADD5.
When the setup transaction data has been sent, an interrupt request is generated according to the response received from the peripheral device (SIGN1 or SACK bit in INTSTS1), by means of which the result of the setup transactions can be confirmed.
A data packet of DATA0 (USB request) is transmitted as the data packet for a setup transaction regardless of the setting of the SQMON bit in DCPCTR.

(2) Data Stage
Data is transferred using the DCP buffer memory.
The access direction of the DCP buffer memory should be specified using the ISEL bit in CFIFOSEL. The transfer direction should be specified using the DIR bit in DCPCFG.
For the first data packet of the data stage, the data PID should be transferred as DATA1. Set data PID = DATA1 in the SQSET bit and the PID bits = BUF in DCPCFG. Completion of data transfer is detected using the BRDY or BEMP interrupt.
For control write transfers, when the number of data bytes to be sent is an integer multiple of the maximum packet size, software should control so as to send a zero-length packet at the end.

(3) Status Stage
Zero-length packet data is transferred in the direction opposite to that in the data stage. As in the data stage, data is transferred using the DCP buffer memory. Transactions are done in the same manner as the data stage.
For the data packets of the status stage, the data PID should be set to DATA1 using the SQSET bit in DCPCFG.
For reception of a zero-length packet, the received data length should be confirmed using the DTLN bits in CFIFOCTR after a BRDY interrupt is generated, and the buffer memory should then be cleared using the BCLR bit.

26.3.6.2 Control Transfers when Function Controller Function is Selected

(1) Setup Stage

The USB module always sends an ACK response for a correct setup packet targeted to the USB module. The operation of the USB module in the setup stage is described below.

When receiving a new setup packet, the USB module sets the following bits.

- Set the VALID bit in INTSTS0 to 1.
- Set the PID bits in DCPCTR to NAK.
- Set the CCPL bit in DCPCTR to 0.

When receiving a data packet right after the setup packet, the USB module stores the USB request parameters in USBREQ, USBVAL, USBINDX, and USBLENG.

Response processing with respect to the control transfer should always be carried out after setting VALID = 0. In the VALID = 1 state, PID = BUF cannot be set, and the data stage cannot be terminated.

Using the function of the VALID bit, the USB module can suspend the current request processing when receiving a new USB request during a control transfer, and can send a response to the newest request.

In addition, the USB module automatically detects the direction bit (bit 8 of bmRequestType) and the request data length (wLength) of the received USB request, distinguishes between control read transfer, control write transfer, and no-data control transfer, and controls stage transitions. For a wrong sequence, the sequence error of the control transfer stage transition interrupt is generated, and the software is notified of occurrence of the error. For the stage control of the USB module, refer to **Figure 26.10**.

(2) Data Stage

Data transfers corresponding to received USB requests should be done using the DCP. Before accessing the DCP buffer memory, the access direction should be specified using the ISEL bit in CFIFOSEL.

If the transfer data is larger than the size of the DCP buffer memory, the data transfer should be carried out using the BRDY interrupt for control write transfers and the BEMP interrupt for control read transfers.

(3) Status Stage

Control transfers are terminated by setting the CCPL bit to 1 while the PID bits in DCPCTR are set to BUF.

After the above settings have been made, the USB module automatically executes the status stage in accordance with the data transfer direction determined at the setup stage. The specific procedure is as follows.

- For control read transfers
  The USB module transmits a zero-length packet and receives an ACK response from the USB host.
- For control write transfers and no-data control transfers
  The USB module receives a zero-length packet from the USB host and sends an ACK response.

(4) Control Transfer Auto Response Function

The USB module automatically responds to a correct SET_ADDRESS request. If any of the following errors occurs in the SET_ADDRESS request, a response from the software is necessary.

- Any transfer other than a control read transfer: bmRequestType ≠ 00h
- Request error: wIndex ≠ 00h
- Any transfer other than a no-data control transfer: wLength ≠ 00h
- Request error: wValue > 7Fh
- Control transfer of a device state error: DVSQ = 011b (Configured)

For all requests other than the SET_ADDRESS request, a response is required from the corresponding software.

26.3.7 Bulk Transfers (PIPE4 and PIPE5)

The buffer memory usage (single/double buffer setting) can be selected for bulk transfers. The USB provides the following functions for bulk transfers.

- BRDY interrupt function (BFRE bit: refer to **26.3.3.1 (2)**, When BRDYM = 0 and BFRE = 1
- Transaction count function
  (TRENB, TRCLR, and TRNCNT bits: refer to **26.3.4.5 Transaction Counter (For PIPE4 and PIPE5 in Reading Direction)**
- Response PID = NAK function (SHTNAK bit: refer to **26.3.4.8 Response PID = NAK Function**
- Auto response mode (ATREPM bit: refer to **26.3.4.9 Auto Response Mode**)

26.3.8 Interrupt Transfers (PIPE6 and PIPE7)

When the function controller function is selected, the USB module carries out interrupt transfers in accordance with the timing controlled by the host controller.
When the host controller function is selected, the timing of issuing a token can be specified using the interval counter.

26.3.8.1 Interval Counter during Interrupt Transfers when Host Controller Function is Selected

For interrupt transfers, intervals between transactions are set in the IITV bits in PIPEPERI. The USB controller issues interrupt transfer tokens based on the specified intervals.

(1) Counter Initialization
The USB controller initializes the interval counter under the following conditions.

- MCU reset:
  The IITV bits are initialized.
- Buffer memory initialization using the ACLRM bit:
  The IITV bits are not initialized but the count value is initialized. Setting the ACLRM bit to 0 starts counting from the value set in the IITV bits.

Note that the interval counter is not initialized in the following case.

- USB bus reset or USB suspended
  The IITV bits are not initialized. Setting 1 to the UACT bit in DVSTCTR0 starts counting from the value before entering the USB bus reset state or USB suspended state.

(2) Operation when Transmission/Reception is Impossible at Token Issuance Timing
The USB module cannot issue tokens even at token issuance timing in the following cases. In such a case, the USB module attempts transactions at the subsequent interval.

- When the PID is set to NAK or STALL.
- When the buffer memory is full at the token sending timing in the receiving (IN) direction.
- When there is no data to be sent in the buffer memory at the token sending timing in the transmitting (OUT) direction.

26.3.9 SOF Interpolation Function

When the function controller function is selected and if data could not be received at intervals of 1 ms because an SOF packet was corrupted or missing, the USB module interpolates the SOF. The SOF interpolation operation begins when the USBE and SCKE bits in SYSCFG have been set to 1 and an SOF packet is received. The interpolation function is initialized under the following conditions.

- MCU reset
- USB bus reset
- Suspended state detected

The SOF interpolation operates as follows.

- The interpolation function is not activated until an SOF packet is received.
- After the first SOF packet is received, interpolation is carried out by counting 1 ms with an internal clock of 48 MHz.
- After the second and subsequent SOF packets are received, interpolation is carried out at the previous reception interval.
- Interpolation is not carried out in the suspended state or while a USB bus reset is being received.

The USB module supports the following functions based on the SOF packet reception. These functions also operate normally with SOF interpolation, if the SOF packet was missing.

- Updating of the frame number
- SOFR interrupt timing

If an SOF packet is missing, the FRNM bit in FRMNUM0 is not updated.

26.3.10 Pipe Schedule

26.3.10.1 Conditions for Generating a Transaction

When the host controller function is selected and UACT has been set to 1, the USB module generates a transaction under the conditions shown in Table 26.22.

Table 26.22 Conditions for Generating a Transaction

Transaction	Conditions for Generation				
	DIR	PID	IITV0	Buffer State	SUREQ
Setup	— (1)	— (1)	— (1)	— (1)	1 setting
Control transfer data stage, status stage, bulk transfer	IN	BUF	Invalid	Receive area exists	— (1)
	OUT	BUF	Invalid	Transmit data exists	— (1)
Interrupt transfer	IN	BUF	Valid	Receive area exists	— (1)
	OUT	BUF	Valid	Transmit data exists	— (1)

Notes:
1. Symbols (—) in the table indicate that the condition is unrelated to the generating of tokens. “Valid” indicates that, for interrupt transfers, a transaction is generated only in transfer frames that are based on the interval counter. “Invalid” indicates that a transaction is generated regardless of the interval counter.
2. This indicates that a transaction is generated regardless of whether there is a receive area. If there is no receive area, however, the received data is discarded.

26.3.10.2 Transfer Schedule

This section describes the transfer scheduling within a frame of the USB module. After the USB module sends an SOF, the transfer is carried out in the sequence described below.

(1) Execution of periodic transfers
A pipe is searched in the order of PIPE6 and PIPE7, and then, if there is a pipe for which an interrupt transfer transaction can be generated, the transaction is generated.
(2) Setup transactions for control transfers
The DCP is checked, and if a setup transaction is possible, it is sent.
(3) Execution of bulk transfers, control transfer data stages, and control transfer status stages
A pipe is searched in the order of DCP, PIPE4, and PIPE5, and then, if there is a pipe for which a transaction for a bulk transfer, a control transfer data stage, or a control transfer status stage can be generated, the transaction is generated.
When a transaction is generated, processing moves to the next pipe transaction regardless of whether the response from the peripheral device is ACK or NAK. If there is time for transfer within the frame, step 3 is repeated.

26.3.10.3 Enabling USB Communication

Setting the UACT bit of DVSTCTR to 1 initiates SOF transmission and transaction generation is enabled. Setting the UACT bit to 0 stops SOF transmission and a suspend state is entered. If the setting of the UACT bit is changed from 1 to 0, processing stops after the next SOF is sent.

26.3.11 USB Internal Power Supply and USB_VCC Pin

The USB internal power supply can be used when 4.0 V ≤ VCC ≤ 5.5 V. This power supply cannot be used when VCC < 4.0 V. The output of the USB internal power supply is connected to the USB_VCC pin. To use this power supply, connect a 0.33 μF capacitor to the USB_VCC pin.
Apply VCC to the USB_VCC pin when using the USB function while 3.0 V ≤ VCC ≤ 3.6 V.
When the PXXCON bit in the USBMC register is 1 (VDDUSBE bit enabled) and the VDDUSBE bit is 0 (USB internal power supply stopped), the USB_VCC pin input is enabled.
When not using the USB function, set the PXXCON bit in the USBMC register to 0 (VDDUSBE bit disabled) and leave the USB_VCC pin open. In this case, although the USB_VCC pin outputs the VCC voltage, this output cannot be used to operate any external devices.
When VCC is used at less than 3.0 V, do not apply 3.3 V to the USB associated pins (USB_DP and USB_DM).

27. A/D Converter

Note

The description offered in this chapter is based on the R8C/3MK Group.
For R8C/3MU Group, refer to **1.1.2 Differences between Groups**.

The A/D converter consists of one 10-bit successive approximation A/D converter circuit with a capacitive coupling amplifier. The analog input shares pins P0_0 to P0_4, P0_7, and P1_0 to P1_3.

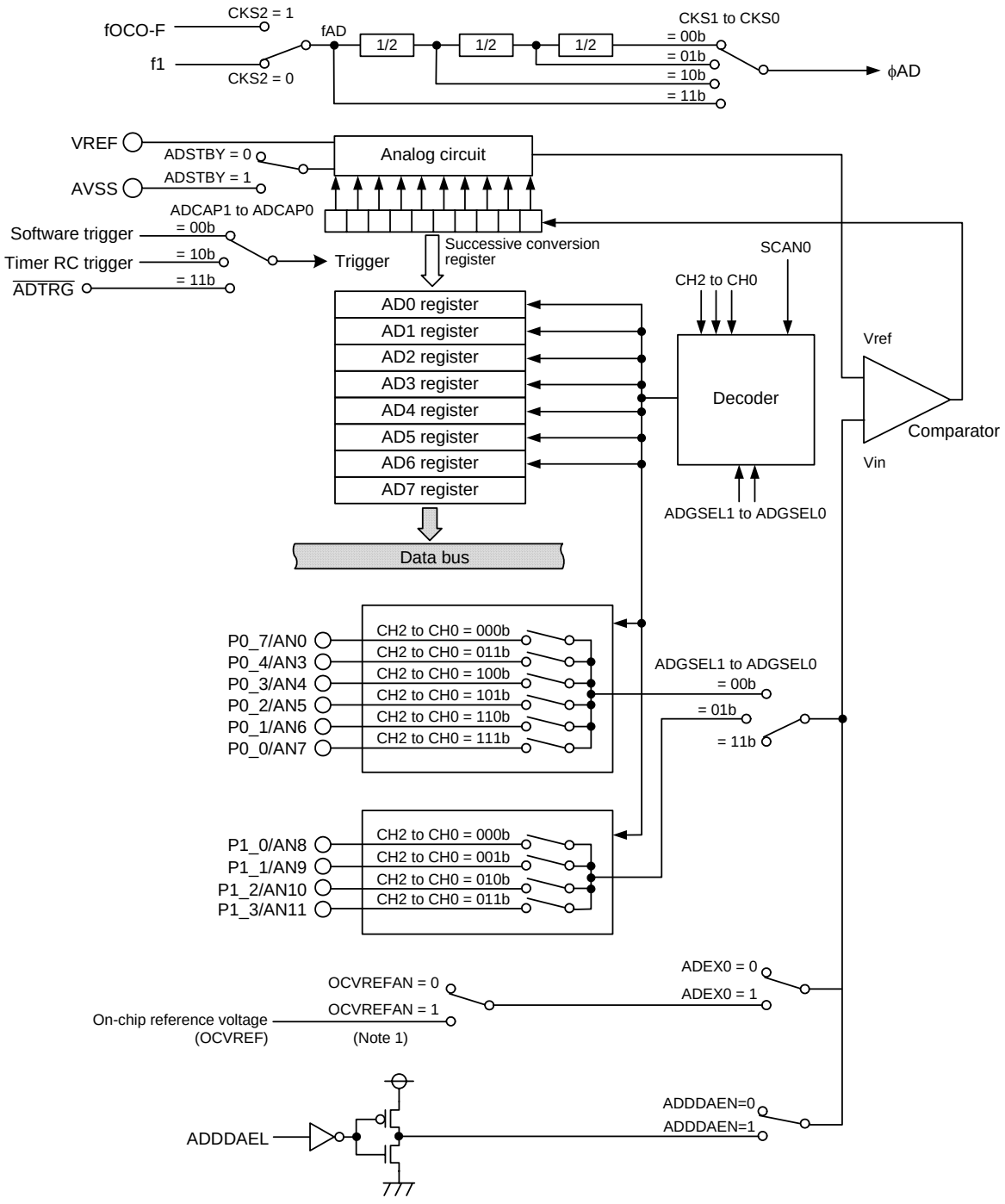
27.1 Overview

Table 27.1 lists the A/D Converter Performance. Figure 27.1 shows a Block Diagram of A/D Converter.

Table 27.1 A/D Converter Performance

Item	Performance
A/D conversion method	Successive approximation (with capacitive coupling amplifier)
Analog input voltage (1)	0 V to AVCC
Operating clock ϕAD (2)	fAD, fAD divided by 2, fAD divided by 4, fAD divided by 8 (fAD=f1 or fOCO-F)
Resolution	8 bits or 10 bits selectable
Absolute accuracy	AVCC = Vref = 5 V, ϕAD = 20 MHz • 8-bit resolution ±2 LSB • 10-bit resolution ±3 LSB AVCC = Vref = 3.3 V, ϕAD = 16 MHz • 8-bit resolution ±2 LSB • 10-bit resolution ±5 LSB AVCC = Vref = 3.0 V, ϕAD = 10 MHz • 8-bit resolution ±2 LSB • 10-bit resolution ±5 LSB AVCC = Vref = 2.2 V, ϕAD = 5 MHz • 8-bit resolution ±2 LSB • 10-bit resolution ±5 LSB
Operating mode	One-shot mode, repeat mode 0, repeat mode 1, single sweep mode, and repeat sweep mode
Analog input pin	10 pins (AN0, AN3 to AN11)
A/D conversion start condition	• Software trigger • Timer RC • External trigger (Refer to **27.3.3 A/D Conversion Start Condition**.)
Conversion rate per pin (3) (ϕAD = fAD)	Minimum 44 ϕAD cycles

Notes:
1. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.
2. Refer to **Table 31.36 A/D Converter Characteristics** for the operating clock ϕA/D.
3. The conversion rate per pin is minimum 44 ϕAD cycles for 8-bit and 10-bit resolution.



CKS0 to CKS2, ADCAP0 to ADCAP1: Bits in ADMOD register
CH0 to CH2, SCAN0, ADGSEL0 to ADGSEL1: Bits in ADINSEL register
ADEX0, ADSTBY, ADDDAEN, ADDDAEL: Bits in ADCON1 register
OCVREFAN: Bit in OCVREFCR register

Note:
1. When on-chip reference voltage is used as analog input, first set the ADEX0 bit to 1 (on-chip reference voltage selected) and then set the OCVREFAN bit to 1 (on-chip reference voltage and analog input are connected).
When on-chip reference voltage is not used as analog input, first set the OCVREFAN bit to 0 (on-chip reference voltage and analog input are cut off) and then set the ADEX0 bit to 0 (extended analog input pin not selected).

Figure 27.1 Block Diagram of A/D Converter

27.2 Registers

27.2.1 On-Chip Reference Voltage Control Register (OCVREFCR)

Address 0026h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	OCVREFAN
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	OCVREFAN	On-chip reference voltage to analog input connect bit (1)	0: On-chip reference voltage and analog input are cut off 1: On-chip reference voltage and analog input are connected	R/W
b1	—	Reserved bits	Set to 0.	R/W
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

Note:

1. When on-chip reference voltage is used as analog input, first set the ADEX0 bit in the ADCON1 register to 1 (on-chip reference voltage selected) and then set the OCVREFAN bit to 1 (on-chip reference voltage and analog input are connected).
   When on-chip reference voltage is not used as analog input, first set the OCVREFAN bit to 0 (on-chip reference voltage and analog input are cut off) and then set the ADEX0 bit to 0 (extended analog input pin not selected).

   Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the OCVREFCR register.
   If the contents of the OCVREFCR register are rewritten during A/D conversion, the conversion result is undefined.

27.2.2 A/D Register i (ADi) (i = 0 to 7)

Address 00C1h to 00C0h (AD0), 00C3h to 00C2h (AD1), 00C5h to 00C4h (AD2), 00C7h to 00C6h (AD3), 00C9h to 00C8h (AD4), 00CBh to 00CAh (AD5), 00CDh to 00CCh (AD6), 00CFh to 00CEh (AD7)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	X	X

Bit	Function		R/W
	10-Bit Mode (BITS Bit in ADCON1 Register = 1)	8-Bit Mode (BITS Bit in ADCON1 Register = 0)	
b0	8 low-order bits in A/D conversion result	A/D conversion result	R
b1			
b2			
b3			
b4			
b5			
b6			
b7			
b8	2 high-order bits in A/D conversion result	When read, the content is 0.	R
b9			
b10	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b11			
b12			
b13			
b14			
b15	Reserved bit	When read, the content is undefined.	R

If the contents of the ADCON1, ADMOD, ADINSEL, or OCVREFCR register are written during A/D conversion, the conversion result is undefined.

When using the A/D converter in 10-bit mode, repeat mode 0, repeat mode 1, or repeat sweep mode, access the ADi register in 16-bit units. Do not access it in 8-bit units.

27.2.3 A/D Mode Register (ADMOD)

Address 00D4h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ADCAP1	ADCAP0	MD2	MD1	MD0	CKS2	CKS1	CKS0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CKS0	Division select bit	b1 b0 0 0: fAD divided by 8 0 1: fAD divided by 4 1 0: fAD divided by 2 1 1: fAD divided by 1 (no division)	R/W
b1	CKS1			R/W
b2	CKS2	Clock source select bit (1)	0: Selects f1 1: Selects fOCO-F	R/W
b3	MD0	A/D operating mode select bit	b5 b4 b3 0 0 0: One-shot mode 0 0 1: Do not set. 0 1 0: Repeat mode 0 0 1 1: Repeat mode 1 1 0 0: Single sweep mode 1 0 1: Do not set. 1 1 0: Repeat sweep mode 1 1 1: Do not set.	R/W
b4	MD1			R/W
b5	MD2			R/W
b6	ADCAP0	A/D conversion trigger select bit	b7 b6 0 0: A/D conversion starts by software trigger (ADST bit in ADCON0 register) 0 1: Do not set. 1 0: A/D conversion starts by conversion trigger from timer RC 1 1: A/D conversion starts by external trigger ($\overline{\text{ADTRG}}$)	R/W
b7	ADCAP1			R/W

Note:
1. When the CKS2 bit is changed, wait for 3 ϕAD cycles or more before starting A/D conversion.

If the ADMOD register is rewritten during A/D conversion, the conversion result is undefined.

27.2.4 A/D Input Select Register (ADINSEL)

Address 00D5h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ADGSEL1	ADGSEL0	—	SCAN0	—	CH2	CH1	CH0
After Reset	1	1	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CH0	Analog input pin select bit	Refer to **Table 27.2 Analog Input Pin Selection**	R/W
b1	CH1			R/W
b2	CH2			R/W
b3	—	Reserved bit	Set to 0.	R/W
b4	SCAN0	A/D sweep pin count select bit	0: 2 pins 1: 4 pins (1)	R/W
b5	—	Reserved bit	Set to 0.	R/W
b6	ADGSEL0	A/D input group select bit	b7 b6 0 0: Port P0 group selected 0 1: Port P1 group selected 1 0: Do not set. 1 1: Port group not selected	R/W
b7	ADGSEL1			R/W

Note:
1. Set bits ADGSEL1 to ADGSEL0 to 01b (port P1 group selected) when the SCAN0 bit is set to 1 (4 pins).

If the ADINSEL register is rewritten during A/D conversion, the conversion result is undefined.

Table 27.2 Analog Input Pin Selection

Bits CH2 to CH0	Bits ADGSEL1, ADGSEL0 = 00b	Bits ADGSEL1, ADGSEL0 = 01b
000b	AN0	AN8
001b	Do not set.	AN9
010b		AN10
011b	AN3	AN11
100b	AN4	Do not set.
101b	AN5	
110b	AN6	
111b	AN7	

27.2.5 A/D Control Register 0 (ADCON0)

Address 00D6h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	ADST
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ADST	A/D conversion start flag	0: Stop A/D conversion 1: Start A/D conversion	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

ADST Bit (A/D conversion start flag)

[Conditions for setting to 1]
When A/D conversion starts and while A/D conversion is in progress.
[Condition for setting to 0]
When A/D conversion stops.

27.2.6 A/D Control Register 1 (ADCON1)

Address 00D7h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ADDDAEL	ADDDAEN	ADSTBY	BITS	—	—	—	ADEX0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ADEX0	Extended analog input pin select bit (1)	0: Extended analog input pin not selected 1: On-chip reference voltage selected (2, 6, 7)	R/W
b1	—	Reserved bits	Set to 0.	R/W
b2	—			
b3	—			
b4	BITS	8/10-bit mode select bit	0: 8-bit mode 1: 10-bit mode	R/W
b5	ADSTBY	A/D standby bit (3)	0: A/D operation stops (standby) (4) 1: A/D operation enabled	R/W
b6	ADDDAEN	A/D open-circuit detection assist function enable bit (5, 7)	0: Disabled 1: Enabled	R/W
b7	ADDDAEL	A/D open-circuit detection assist method select bit (5)	0: Discharge before conversion 1: Precharge before conversion	R/W

Notes:

1. When on-chip reference voltage is used as analog input, first set the ADEX0 bit to 1 (on-chip reference voltage selected) and then set the OCVREFAN bit in the OCVREFCR register to 1 (on-chip reference voltage and analog input are connected).
   When on-chip reference voltage is not used as analog input, first set the OCVREFAN bit to 0 (on-chip reference voltage and analog input are cut off) and then set the ADEX0 bit to 0 (extended analog input pin not selected).
2. Do not set to 1 (A/D conversion using comparison reference voltage as input) in single sweep mode or repeat sweep mode.
3. When the ADSTBY bit is changed from 0 (A/D operation stops) to 1 (A/D operation enabled), wait for 1 ϕAD cycle or more before starting A/D conversion.
4. Stop the A/D function before setting to standby. When the ADSBY bit is set to 1 (standby), any access to the A/D associated registers (addresses 00C0h to 00CFh, and 00D4h to 00D7h) is disabled.
5. To enable the A/D open-circuit detection assist function, select the conversion start state with the ADDDAEL bit after setting the ADDDAEN bit to 1 (enabled).
   The conversion result with an open circuit varies with external circuits. Careful evaluation should be performed according to the system before using this function.
6. When on-chip reference voltage is used (ADEX0 = 1), set bits CH2 to CH0 in the ADINSEL register to 000b.
7. When on-chip reference voltage is used (ADEX0 = 1), set the ADDDAEN bit to 0 (A/D open-circuit detection assist function disabled).

If the ADCON1 register is rewritten during A/D conversion, the conversion result is undefined.

27.3 Common Items for Multiple Modes

27.3.1 Input/Output Pins

The analog input shares pins P0_0 to P0_4, P0_7, and P1_0 to P1_3 in AN0, AN3 to AN11.
When using the ANi (i = 0, 3 to 11) pin as input, set the corresponding port direction bit to 0 (input mode).
After changing the A/D operating mode, select an analog input pin again.

27.3.2 A/D Conversion Cycles

Figure 27.2 shows a Timing Diagram of A/D Conversion. Figure 27.3 shows the A/D Conversion Cycles (ϕAD = fAD).

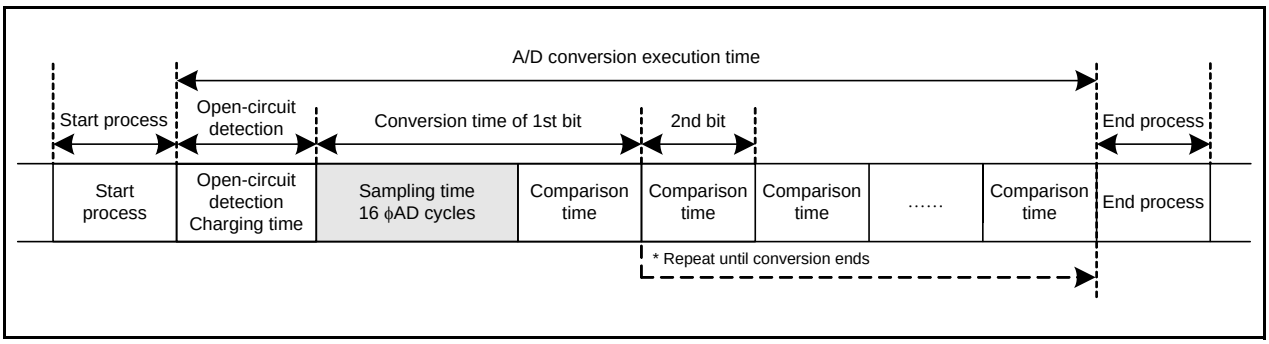
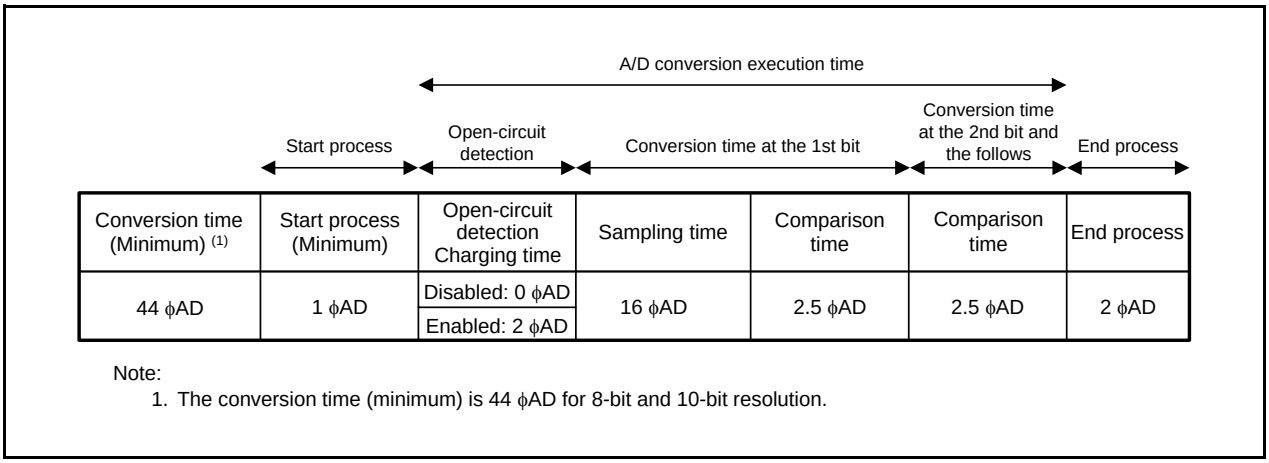


Figure 27.2 Timing Diagram of A/D Conversion



Conversion time (Minimum) (1)	Start process (Minimum)	Open-circuit detection Charging time	Sampling time	Comparison time	Comparison time	End process
44 ϕAD	1 ϕAD	Disabled: 0 ϕAD Enabled: 2 ϕAD	16 ϕAD	2.5 ϕAD	2.5 ϕAD	2 ϕAD

Note:
1. The conversion time (minimum) is 44 ϕAD for 8-bit and 10-bit resolution.

Figure 27.3 A/D Conversion Cycles (ϕAD = fAD)

Table 27.3 shows the Number of Cycles for A/D Conversion Items. The A/D conversion time is defined as follows.
The start process time varies depending on which ϕAD is selected.
When 1 (A/D conversion starts) is written to the ADST bit in the ADCON0 register, an A/D conversion starts after the start process time has elapsed. Reading the ADST bit before the A/D conversion returns 0 (A/D conversion stops).
In the modes where an A/D conversion is performed on multiple pins or multiple times, the between-execution process time is inserted between the A/D conversion execution time for one pin and the next A/D conversion time.
In one-shot mode and single sweep mode, the ADST bit is set to 0 during the end process time and the last A/D conversion result is stored in the ADi register.

- In on-shot mode
  Start process time + A/D conversion execution time + end process time

- When two pins are selected in single sweep mode
  Start process time + (A/D conversion execution time + between-execution process time + A/D conversion execution time) + end process time

Table 27.3 Number of Cycles for A/D Conversion Items

A/D Conversion Item		Number of Cycles
Start process time	ϕAD = fAD	1 or 2 fAD cycles
	ϕAD = fAD divided by 2	2 or 3 fAD cycles
	ϕAD = fAD divided by 4	3 or 4 fAD cycles
	ϕAD = fAD divided by 8	5 or 6 fAD cycles
A/D conversion execution time	Open-circuit detection disabled	40 ϕAD cycles + 1 to 3 fAD cycles
	Open-circuit detection enabled	42 ϕAD cycles + 1 to 3 fAD cycles
Between-execution process time		1 ϕAD cycle
End process time		2 or 3 fAD cycles

27.3.3 A/D Conversion Start Condition

A software trigger, trigger from timer RC, and external trigger are used as A/D conversion start triggers.
Figure 27.4 shows the Block Diagram of A/D Conversion Start Control Unit.

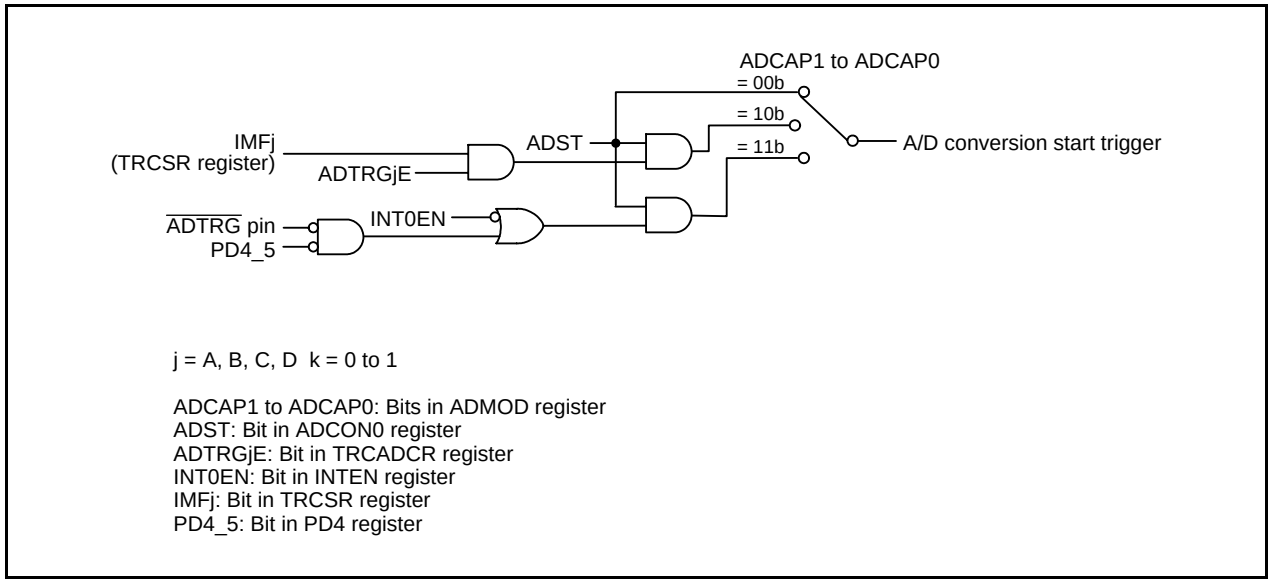


Figure 27.4 Block Diagram of A/D Conversion Start Control Unit

27.3.3.1 Software Trigger

A software trigger is selected when bits ADCAP1 to ADCAP0 in the ADMOD register are set to 00b (software trigger).
The A/D conversion starts when the ADST bit in the ADCON0 register is set to 1 (A/D conversion starts).

27.3.3.2 Trigger from Timer RC

This trigger is selected when bits ADCAP1 to ADCAP0 in the ADMOD register are set to 10b (timer RC).
To use this function, make sure the following conditions are met.

- Bits ADCAP1 to ADCAP0 in the ADMOD register are set to 10b (timer RC).
- Timer RC is used in the output compare function (timer mode, PWM mode, PWM2 mode).
- The ADTRGjE bit (j = A, B, C, D) in the TRCADCR register is set to 1 (A/D trigger occurs at compare match with TRCGRj register).
- The ADST bit in the ADCON0 register is set to 1 (A/D conversion starts).

When the IMFj bit in the TRCSR register is changed from 0 to 1, A/D conversion starts.
Refer to **19. Timer RC**, **19.5 Timer Mode (Output Compare Function)**, **19.6 PWM Mode**, **19.7 PWM2 Mode** for the details of timer RC and the output compare function (timer mode, PWM mode, and PWM2 mode).

27.3.3.3 External Trigger

This trigger is selected when bits ADCAP1 to ADCAP0 in the ADMOD register are set to 11b (external trigger ($\overline{\text{ADTRG}}$)).
To use this function, make sure the following conditions are met.

- Bits ADCAP1 to ADCAP0 in the ADMOD register are set to 11b (external trigger ($\overline{\text{ADTRG}}$)).
- Set the INT0EN bit in the INTEN register to 1 ($\overline{\text{INT0}}$ input enabled) and the INT0PL bit to 0 (one edge), and set the POL bit in the INT0IC register to 0 (falling edge selected).
- Set the PD4_5 bit in the PD4 register to 0 (input mode).
- Select the $\overline{\text{INT0}}$ digital filter by bits INT0F1 to INT0F0 in the INTF register.
- The ADST bit in the ADCON0 register is set to 1 (A/D conversion starts).

The IR bit in the INT0IC register is set to 1 (interrupt requested) in accordance with the setting of the POL bit in the INT0IC register and the INT0PL bit in the INTEN register, and a change in the $\overline{\text{ADTRG}}$ pin input (refer to **11.8 Notes on Interrupts**).
For details on interrupts, refer to **11. Interrupts**.

When the $\overline{\text{ADTRG}}$ pin input is changed from “H” to “L” under the above conditions, A/D conversion starts.

27.3.4 A/D Conversion Result

The A/D conversion result is stored in the ADi register (i = 0 to 7). The register where the result is stored varies depending on the A/D operating mode used. The contents of the ADi register are undefined after a reset. Values cannot be written to the ADi register.

In repeat mode 0, no interrupt request is generated. After the first AD conversion is completed, determine if the A/D conversion time has elapsed by a program.
In one-shot mode, repeat mode 1, single sweep mode, and repeat sweep mode, an interrupt request is generated at certain times, such as when an A/D conversion completes (the IR bit in the ADIC register is set to 1).
However, in repeat mode 1 and repeat sweep mode, A/D conversion continues after an interrupt request is generated. Read the ADi register before the next A/D conversion is completed, since at completion the ADi register is rewritten with the new value.

In one-shot mode and single sweep mode, when bits ADCAP1 to ADCAP0 in the ADMOD register is set to 00b (software trigger), the ADST bit in the ADCON0 register is used to determine whether the A/D conversion or sweep has completed.

During an A/D conversion operation, if the ADST bit in the ADCON0 register is set to 0 (A/D conversion stops) by a program to forcibly terminate A/D conversion, the conversion result of the A/D converter is undefined and no interrupt is generated. The value of the ADi register before A/D conversion may also be undefined.
If the ADST bit is set to 0 by a program, do not use the value of all the ADi register.

27.3.5 Low Current Consumption Function

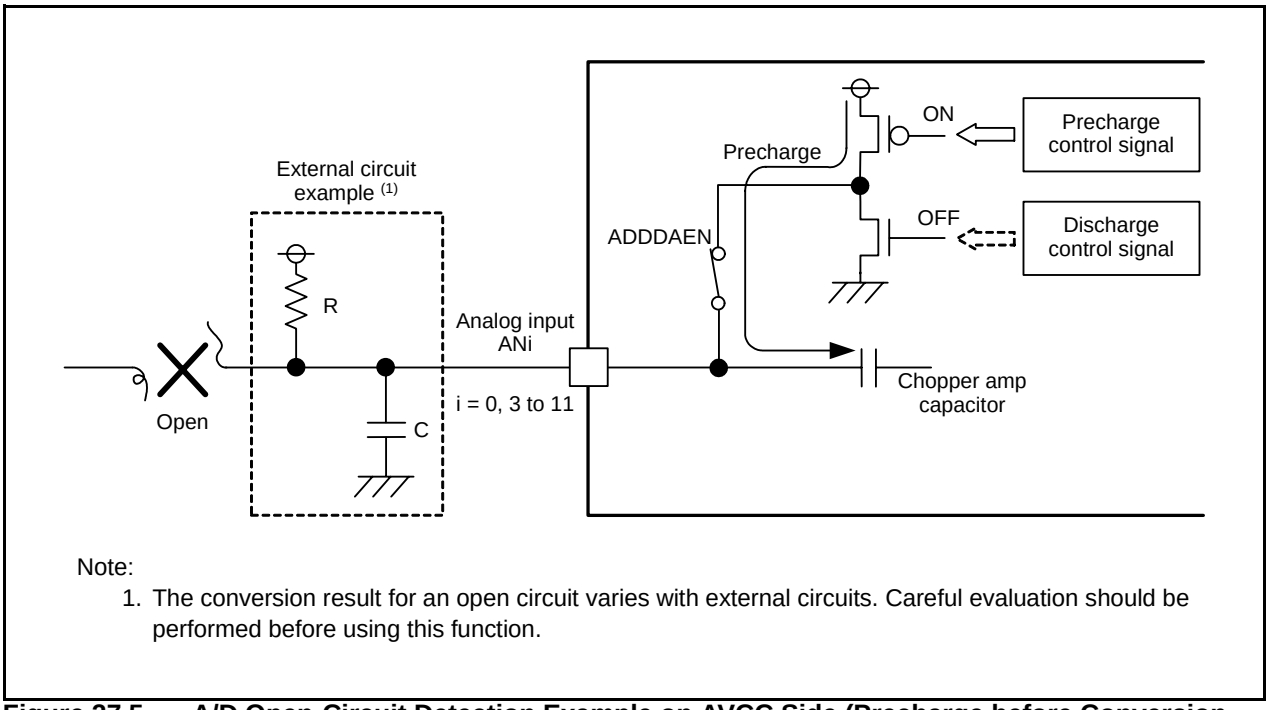
When the A/D converter is not used, power consumption can be reduced by setting the ADSTBY bit in the ADCON1 register to 0 (A/D operation stops (standby)) to shut off any analog circuit current flow.
To use the A/D converter, set the ADSTBY bit to 1 (A/D operation enabled) and wait for 1 ϕAD cycle or more before setting the ADST bit in the ADCON0 register to 1 (A/D conversion starts). Do not write 1 to bits ADST and ADSTBY at the same time.
Also, do not set the ADSTBY bit to 0 (A/D operation stops (standby)) during A/D conversion.

27.3.6 On-Chip Reference Voltage (OCVREF)

In one-shot mode, repeat mode 0, and repeat mode 1, the on-chip reference voltage (OCVREF) can be used as analog input.
Any variation in VREF can be confirmed using the on-chip reference voltage. Use the ADEX0 bit in the ADCON1 register and the OCVREFAN bit in the OCVREFCR register to select the on-chip reference voltage.
The A/D conversion result of the on-chip reference voltage in one-shot mode or in repeat mode 0 is stored in the AD0 register.

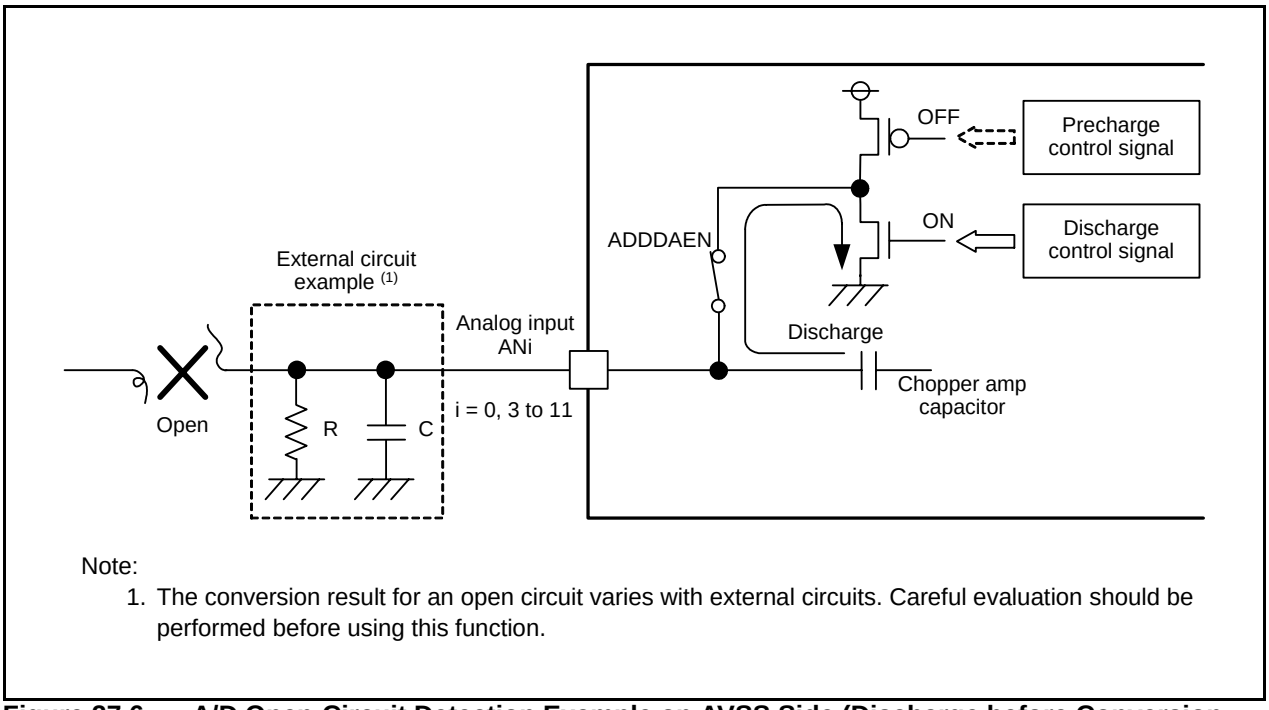
27.3.7 A/D Open-Circuit Detection Assist Function

To suppress influences of the analog input voltage leakage from the previously converted channel during A/D conversion operation, a function is incorporated to fix the electric charge on the chopper amp capacitor to the predetermined state (AVCC or GND) before starting conversion.
This function enables more reliable detection of an open circuit in the wiring connected to the analog input pins.
Figure 27.5 shows the A/D Open-Circuit Detection Example on AVCC Side (Precharge before Conversion Selected) and Figure 27.6 shows the A/D Open-Circuit Detection Example on AVSS Side (Discharge before Conversion Selected).



Note:
1. The conversion result for an open circuit varies with external circuits. Careful evaluation should be performed before using this function.

Figure 27.5 A/D Open-Circuit Detection Example on AVCC Side (Precharge before Conversion Selected)



Note:
1. The conversion result for an open circuit varies with external circuits. Careful evaluation should be performed before using this function.

Figure 27.6 A/D Open-Circuit Detection Example on AVSS Side (Discharge before Conversion Selected)

27.4 One-Shot Mode

In one-shot mode, the input voltage to one pin selected from among AN0, AN3 to AN11, or OCVREF is A/D converted once.
Table 27.4 lists the One-Shot Mode Specifications.

Table 27.4 One-Shot Mode Specifications

Item	Specification
Function	The input voltage to the pin selected by bits CH2 to CH0 and bits ADGSEL1 to ADGSEL0 in the ADINSEL register or the ADEX0 bit in the ADCON1 register is A/D converted once.
Resolution	8 bits or 10 bits
A/D conversion start condition	• Software trigger • Timer RC • External trigger (Refer to **27.3.3 A/D Conversion Start Condition)**
A/D conversion stop condition	• A/D conversion completes (If bits ADCAP1 to ADCAP0 in the ADMOD register are set to 00b (software trigger), the ADST bit in the ADCON0 register is set to 0.) • Set the ADST bit to 0
Interrupt request generation timing	When A/D conversion completes
Analog input pin	One pin selectable from among AN0, AN3 to AN11, or OCVREF.
Storage resister for A/D conversion result	AD0 register: AN0, AN8, OCVREF AD1 register: AN9 AD2 register: AN10 AD3 register: AN3, AN11 AD4 register: AN4 AD5 register: AN5 AD6 register: AN6 AD7 register: AN7
Reading of result of A/D converter	Read register AD0 to AD7 corresponding to the selected pin.

27.5 Repeat Mode 0

In repeat mode 0, the input voltage to one pin selected from among AN0, AN3 to AN11, or OCVREF is A/D converted repeatedly.
Table 27.5 lists the Repeat Mode 0 Specifications.

Table 27.5 Repeat Mode 0 Specifications

Item	Specification
Function	The input voltage to the pin selected by bits CH2 to CH0 and bits ADGSEL1 to ADGSEL0 in the ADINSEL register or the ADEX0 bit in the ADCON1 register is A/D converted repeatedly.
Resolution	8 bits or 10 bits
A/D conversion start condition	• Software trigger • Timer RC • External trigger (Refer to **27.3.3 A/D Conversion Start Condition)**
A/D conversion stop condition	Set the ADST bit in the ADCON0 register to 0
Interrupt request generation timing	Not generated
Analog input pin	One pin selectable from among AN0, AN3 to AN11, or OCVREF.
Storage resister for A/D conversion result	AD0 register: AN0, AN8, OCVREF AD1 register: AN9 AD2 register: AN10 AD3 register: AN3, AN11 AD4 register: AN4 AD5 register: AN5 AD6 register: AN6 AD7 register: AN7
Reading of result of A/D converter	Read register AD0 to AD7 corresponding to the selected pin.

27.6 Repeat Mode 1

In repeat mode 1, the input voltage to one pin selected from among AN0, AN3 to AN11, or OCVREF is A/D converted repeatedly.
Table 27.6 lists the Repeat Mode 1 Specifications. Figure 27.7 shows the Operating Example of Repeat Mode 1.

Table 27.6 Repeat Mode 1 Specifications

Item	Specification
Function	The input voltage to the pin selected by bits CH2 to CH0 and bits ADGSEL1 to ADGSEL0 in the ADINSEL register or the ADEX0 bit in the ADCON1 register is A/D converted repeatedly.
Resolution	8 bits or 10 bits
A/D conversion start condition	• Software trigger • Timer RC • External trigger (Refer to **27.3.3 A/D Conversion Start Condition)**
A/D conversion stop condition	Set the ADST bit in the ADCON0 register to 0
Interrupt request generation timing	When the A/D conversion result is stored in the AD7 register.
Analog input pin	One pin selectable from among AN0, AN3 to AN11, or OCVREF.
Storage resister for A/D conversion result	AD0 register: 1st A/D conversion result, 9th A/D conversion result... AD1 register: 2nd A/D conversion result, 10th A/D conversion result... AD2 register: 3rd A/D conversion result, 11th A/D conversion result... AD3 register: 4th A/D conversion result, 12th A/D conversion result... AD4 register: 5th A/D conversion result, 13th A/D conversion result... AD5 register: 6th A/D conversion result, 14th A/D conversion result... AD6 register: 7th A/D conversion result, 15th A/D conversion result... AD7 register: 8th A/D conversion result, 16th A/D conversion result...
Reading of result of A/D converter	Read registers AD0 to AD7

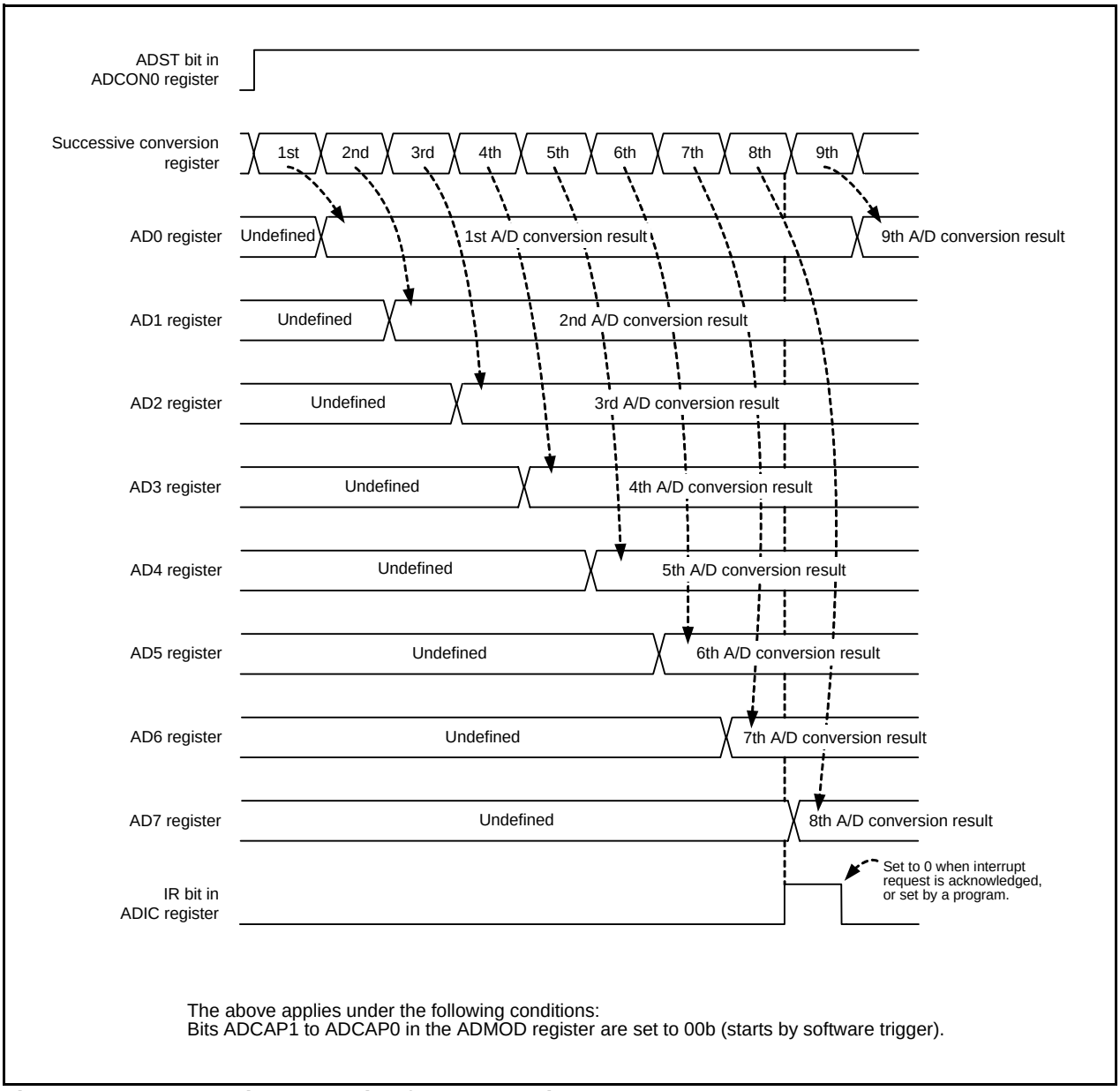


Figure 27.7 Operating Example of Repeat Mode 1

27.7 Single Sweep Mode

In single sweep mode, the input voltage to two or four pins selected from among AN0, AN3 to AN11 are A/D converted once.
Table 27.7 lists the Single Sweep Mode Specifications. Figure 27.8 shows the Operating Example of Single Sweep Mode.

Table 27.7 Single Sweep Mode Specifications

Item	Specification
Function	The input voltage to the pins selected by bits ADGSEL1 to ADGSEL0 and the SCAN0 bit in the ADINSEL register is A/D converted once.
Resolution	8 bits or 10 bits
A/D conversion start condition	• Software trigger • Timer RC • External trigger (Refer to **27.3.3 A/D Conversion Start Condition)**
A/D conversion stop condition	• If two pins are selected, when A/D conversion of the two selected pins completes (the ADST bit in the ADCON0 register is set to 0). • If four pins are selected, when A/D conversion of the four selected pins completes (the ADST bit is set to 0). • Set the ADST bit to 0.
Interrupt request generation timing	• If two pins are selected, when A/D conversion of the two selected pins completes. • If four pins are selected, when A/D conversion of the four selected pins completes.
Analog input pin	AN0 to AN1 (2 pins), AN8 to AN9 (2 pins), AN8 to AN11 (4 pins) (Selectable by the SCAN0 bit and bits ADGSEL1 to ADGSEL0.)
Storage resister for A/D conversion result	AD0 register: AN0, AN8 AD1 register: AN9 AD2 register: AN10 AD3 register: AN11
Reading of result of A/D converter	Read the registers from AD0 to AD3 corresponding to the selected pin.

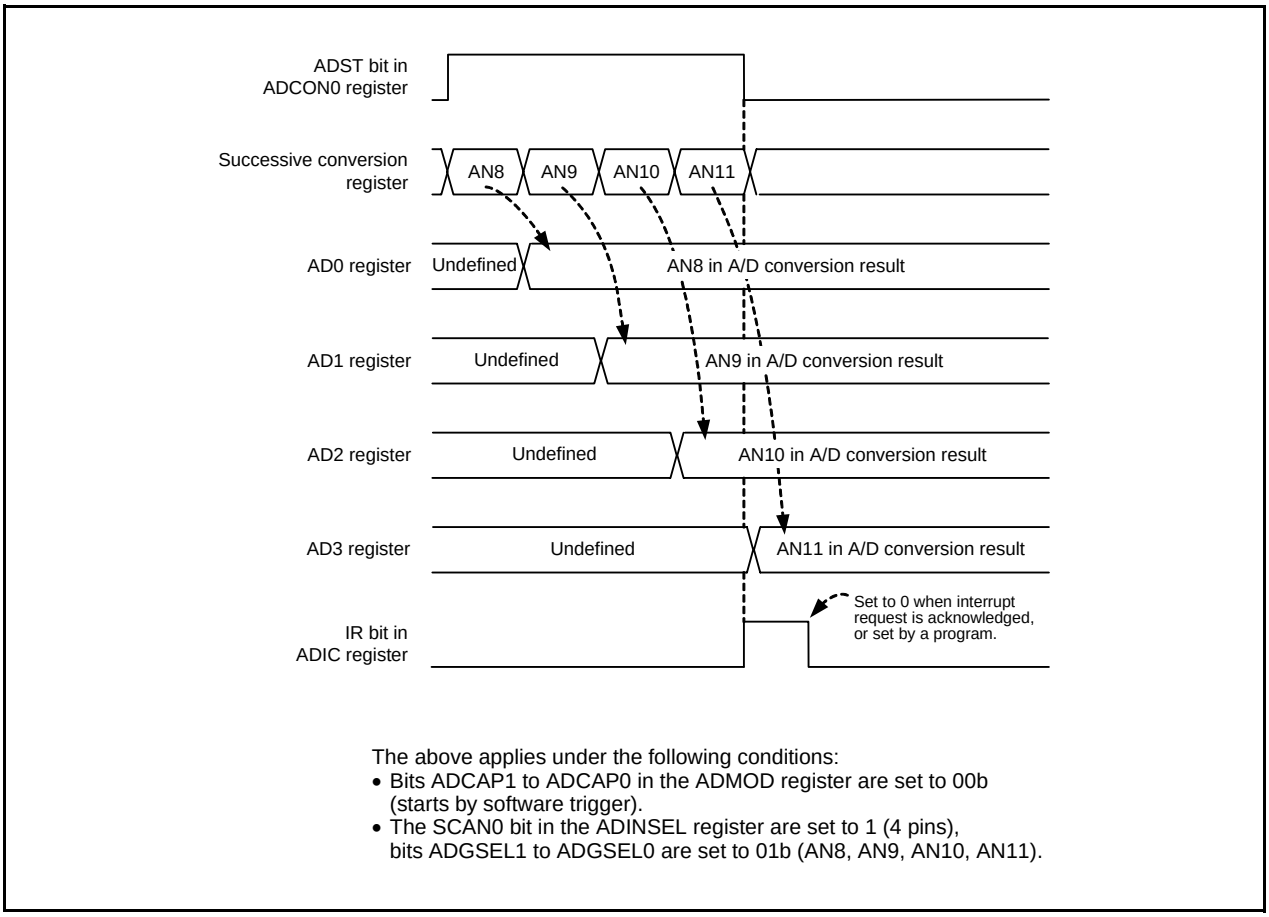


Figure 27.8 Operating Example of Single Sweep Mode

27.8 Repeat Sweep Mode

In repeat sweep mode, the input voltage to two or four pins selected from among AN0, AN3 to AN11 are A/D converted repeatedly.
Table 27.8 lists the Repeat Sweep Mode Specifications. Figure 27.9 shows the Operating Example of Repeat Sweep Mode.

Table 27.8 Repeat Sweep Mode Specifications

Item	Specification
Function	The input voltage to the pins selected by bits ADGSEL1 to ADGSEL0 and the SCAN0 bit in the ADINSEL register are A/D converted repeatedly.
Resolution	8 bits or 10 bits
A/D conversion start condition	• Software trigger • Timer RC • External trigger (Refer to **27.3.3 A/D Conversion Start Condition)**
A/D conversion stop condition	Set the ADST bit in the ADCON0 register to 0
Interrupt request generation timing	• If two pins are selected, when A/D conversion of the two selected pins completes. • If four pins are selected, when A/D conversion of the four selected pins completes.
Analog input pin	AN0 to AN1 (2 pins), AN8 to AN9 (2 pins), AN8 to AN11 (4 pins) (Selectable by the SCAN0 bit and bits ADGSEL1 to ADGSEL0.)
Storage resister for A/D conversion result	AD0 register: AN0, AN8 AD1 register:AN9 AD2 register: AN10 AD3 register: AN11
Reading of result of A/D converter	Read the registers from AD0 to AD3 corresponding to the selected pin.

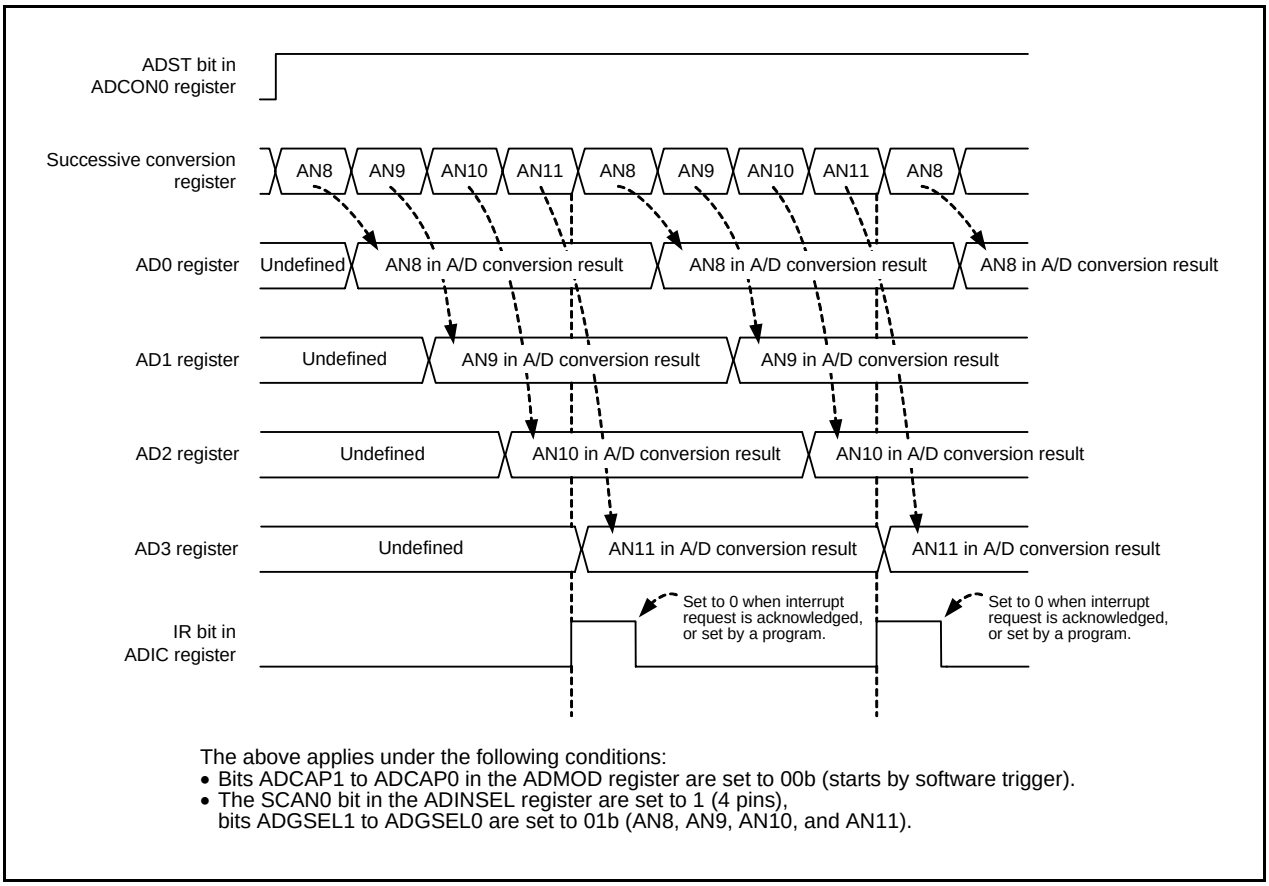


Figure 27.9 Operating Example of Repeat Sweep Mode

27.9 Output Impedance of Sensor under A/D Conversion

To carry out A/D conversion properly, charging the internal capacitor C shown in Figure 27.10 has to be completed within a specified period of time. T (sampling time) as the specified time. Let output impedance of sensor equivalent circuit be R0, internal resistance of microcomputer be R, precision (error) of the A/D converter be X, and the resolution of A/D converter be Y (Y is 1024 in the 10-bit mode, and 256 in the 8-bit mode).

VC is generally $VC = VIN\left\{1 - e^{-\frac{1}{C(R0+R)}t}\right\}$

And when t = T, $VC = VIN - \frac{X}{Y}VIN = VIN\left(1 - \frac{X}{Y}\right)$

$$e^{-\frac{1}{C(R0+R)}T} = \frac{X}{Y}$$

$$-\frac{1}{C(R0+R)}T = \ln\frac{X}{Y}$$

Hence, $R0 = -\frac{T}{C \bullet \ln\frac{X}{Y}} - R$

Figure 27.10 shows the Analog Input Pin and External Sensor Equivalent Circuit. When the difference between VIN and VC becomes 0.1LSB, we find impedance R0 when voltage between pins VC changes from 0 to VIN-(0.1/1024) VIN in time T. (0.1/1024) means that A/D precision drop due to insufficient capacitor charge is held to 0.1LSB at time of A/D conversion in the 10-bit mode. Actual error however is the value of absolute precision added to 0.1LSB.
T = 0.8 µs when ϕAD = 20 MHz. Output impedance R0 for sufficiently charging capacitor C within time T is determined as follows.

T = 0.8 µs, R = 10 kΩ, C = 6.0 pF, X = 0.1, and Y = 1024. Hence,

$$R0 = -\frac{0.8 \times 10^{-6}}{6.0 \times 10^{-12} \bullet \ln\frac{0.1}{1024}} - 10 \times 10^{3} \approx 4.4 \times 10^{3}$$

Thus, the allowable output impedance of the sensor equivalent circuit, making the precision (error) 0.1LSB or less, is approximately 4.4 kΩ maximum.

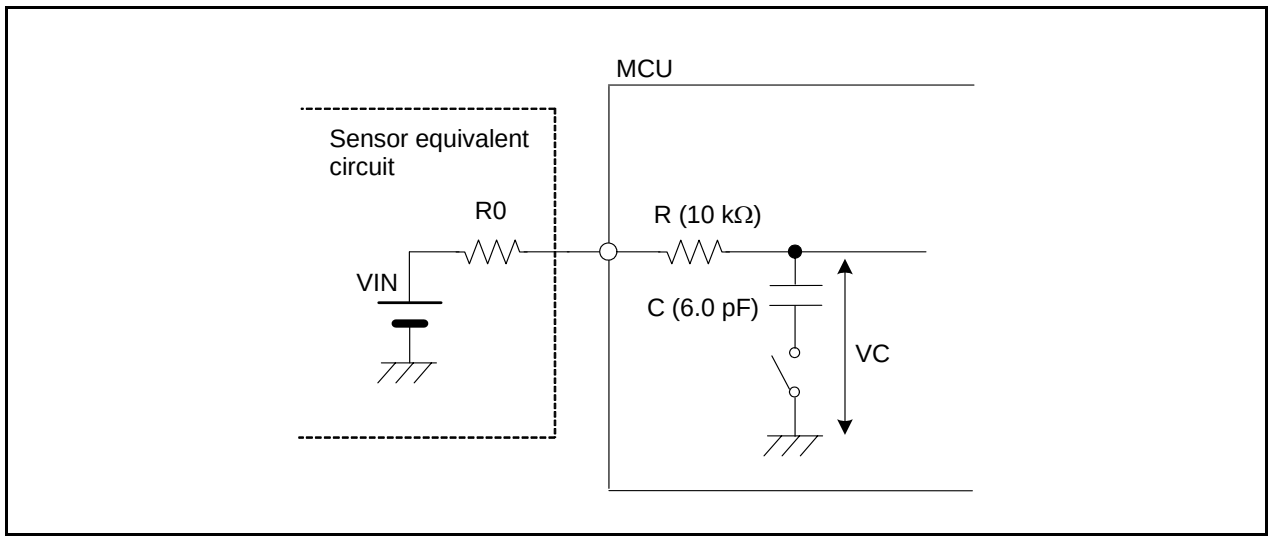


Figure 27.10 Analog Input Pin and External Sensor Equivalent Circuit

27.10 Notes on A/D Converter

- Write to the ADMOD register, the ADINSEL register, the ADCON0 register (other than ADST bit), the ADCON1 register, the OCVREFCR register when A/D conversion is stopped (before a trigger occurs).
- To use the A/D converter in repeat mode 0, repeat mode 1, or repeat sweep mode, select the frequency of the A/D converter operating clock ϕAD or more for the CPU clock during A/D conversion.
  Do not select fOCO-F as ϕAD.
- Connect 0.1 μF capacitor between the VREF pin and AVSS pin.
- Do not enter stop mode during A/D conversion.
- Do not enter wait mode during A/D conversion regardless of the state of the CM02 bit in the CM0 register (1: Peripheral function clock stops in wait mode or 0: Peripheral function clock does not stop in wait mode).
- Do not set the FMSTP bit in the FMR0 register to 1 (flash memory stops) during A/D conversion.
- Do not change the CKS2 bit in the ADMOD register while fOCO-F is stopped.
- During an A/D conversion operation, if the ADST bit in the ADCON0 register is set to 0 (A/D conversion stops) by a program to forcibly terminate A/D conversion, the conversion result of the A/D converter is undefined and no interrupt is generated. The value of the ADi register before A/D conversion may also be undefined.
  If the ADST bit is set to 0 by a program, do not use the value of all the ADi register.
- When the A/D converter is not used, power consumption can be reduced by setting the ADSTBY bit in the ADCON1 register to 0 (A/D operation stops (standby)) to shut off any analog circuit current flow.

28. Comparator B

Comparator B compares a reference input voltage and an analog input voltage. Comparator B1 and comparator B3 are independent of each other.

28.1 Overview

The comparison result of the reference input voltage and analog input voltage can be read by software. An input to the IVREFi (i = 1 or 3) pin can be used as the reference input voltage.
Table 28.1 lists the Comparator B Specifications, Figure 28.1 shows a Comparator B Block Diagram, and Table 28.2 lists the I/O Pins.

Table 28.1 Comparator B Specifications

Item	Specification
Analog input voltage	Input voltage to the IVCMPi pin
Reference input voltage	Input voltage to the IVREFi pin
Comparison result	Read from the INTiCOUT bit in the INTCMP register
Interrupt request generation timing	When the comparison result changes.
Selectable functions	Digital filter function Whether the digital filter is applied or not and the sampling frequency can be selected.

i = 1 or 3

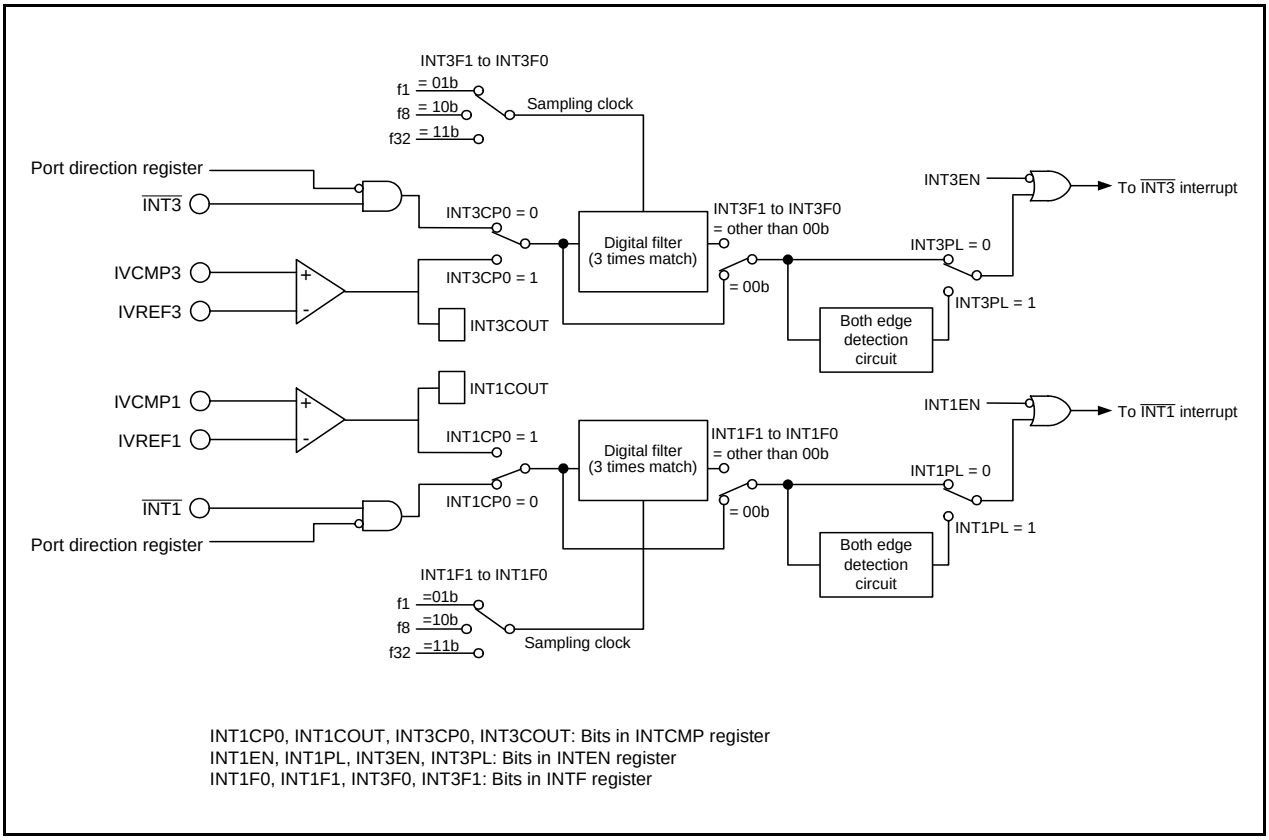


Figure 28.1 Comparator B Block Diagram

Table 28.2 I/O Pins

Pin Name	I/O	Function
IVCMP1	Input	Comparator B1 analog pin
IVREF1	Input	Comparator B1 reference voltage pin
IVCMP3	Input	Comparator B3 analog pin
IVREF3	Input	Comparator B3 reference voltage pin

28.2 Registers

28.2.1 Comparator B Control Register 0 (INTCMP)

Address 01F8h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	INT3COUT	—	—	INT3CP0	INT1COUT	—	—	INT1CP0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	INT1CP0	Comparator B1 operation enable bit	0: Comparator B1 operation disabled 1: Comparator B1 operation enabled	R/W
b1	—	Reserved bits	Set to 0.	R/W
b2	—			
b3	INT1COUT	Comparator B1 monitor flag	0: IVCMP1 < IVREF1 or comparator B1 operation disabled 1: IVCMP1 > IVREF1	R
b4	INT3CP0	Comparator B3 operation enable bit	0: Comparator B3 operation disabled 1: Comparator B3 operation enabled	R/W
b5	—	Reserved bits	Set to 0.	R/W
b6	—			
b7	INT3COUT	Comparator B3 monitor flag	0: IVCMP3 < IVREF3 or comparator B3 operation disabled 1: IVCMP3 > IVREF3	R

28.2.2 External Input Enable Register 0 (INTEN)

Address 01FAh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	INT3PL	INT3EN	INT2PL	INT2EN	INT1PL	INT1EN	INT0PL	INT0EN
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	INT0EN	$\overline{\text{INT0}}$ input enable bit	0: Disabled 1: Enabled	R/W
b1	INT0PL	$\overline{\text{INT0}}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W
b2	INT1EN	$\overline{\text{INT1}}$ input enable bit	0: Disabled 1: Enabled	R/W
b3	INT1PL	$\overline{\text{INT1}}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W
b4	INT2EN	$\overline{\text{INT2}}$ input enable bit	0: Disabled 1: Enabled	R/W
b5	INT2PL	$\overline{\text{INT2}}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W
b6	INT3EN	$\overline{\text{INT3}}$ input enable bit	0: Disabled 1: Enabled	R/W
b7	INT3PL	$\overline{\text{INT3}}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W

Notes:
1. To set the INTiPL bit (i = 0 to 3) to 1 (both edges), set the POL bit in the INTiIC register to 0 (falling edge selected).
2. The IR bit in the INTiIC register may be set to 1 (interrupt requested) if the INTEN register is rewritten. Refer to **11.8.4 Changing Interrupt Sources**.

28.2.3 INT Input Filter Select Register 0 (INTF)

Address 01FCh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	INT3F1	INT3F0	INT2F0	INT2F0	INT1F1	INT1F0	INT0F1	INT01F0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	INT01F0	$\overline{\text{INT0}}$ input filter select bit	b1 b0 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b1	INT0F1			
b2	INT1F0	$\overline{\text{INT1}}$ input filter select bit	b3 b2 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b3	INT1F1			R/W
b4	INT2F0	$\overline{\text{INT2}}$ input filter select bit	b5 b4 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b5	INT2F0			
b6	INT3F0	$\overline{\text{INT3}}$ input filter select bit	b7 b6 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b7	INT3F1			R/W

28.3 Functional Description

Comparator B1 and comparator B3 operate independently. Their operations are the same.
Table 28.3 lists the Procedure for Setting Registers Associated with Comparator B.

Table 28.3 Procedure for Setting Registers Associated with Comparator B

Step	Register	Bit	Setting Value
1	Select the function of pins IVCMPi and IVREFi. Refer to **7.5 Port Settings**. However, set registers and bits other than listed in step 2 and the following steps.		
2	INTF	Select whether to enable or disable the filter. Select the sampling clock.	
3	INTCMP	INTiCP0	1 (operation enabled)
4	Wait for comparator stability time (100 μs max.)		
5	INTEN	INTiEN	When using an interrupt: 1 (interrupt enabled)
		INTiPL	When using an interrupt: Select the input polarity.
6	INTiIC	ILVL2 to ILVL0	When using an interrupt: Select the interrupt priority level.
		IR	When using an interrupt: 0 (no interrupt requested: initialization)

i = 1 or 3

Figure 28.2 shows an Operating Example of Comparator Bi (i = 1 or 3).
If the analog input voltage is higher than the reference input voltage, the INTiCOUT bit in the INTCMP register is set to 1. If the analog input voltage is lower than the reference input voltage, the INTiCOUT bit is set to 0. To use the comparator Bi interrupt, set the INTiEN bit in the INTEN register to 1 (interrupt enabled). If the comparison result changes at this time, a comparator Bi interrupt request is generated. Refer to **28.4 Comparator B1 and Comparator B3 Interrupts** for details of interrupts.

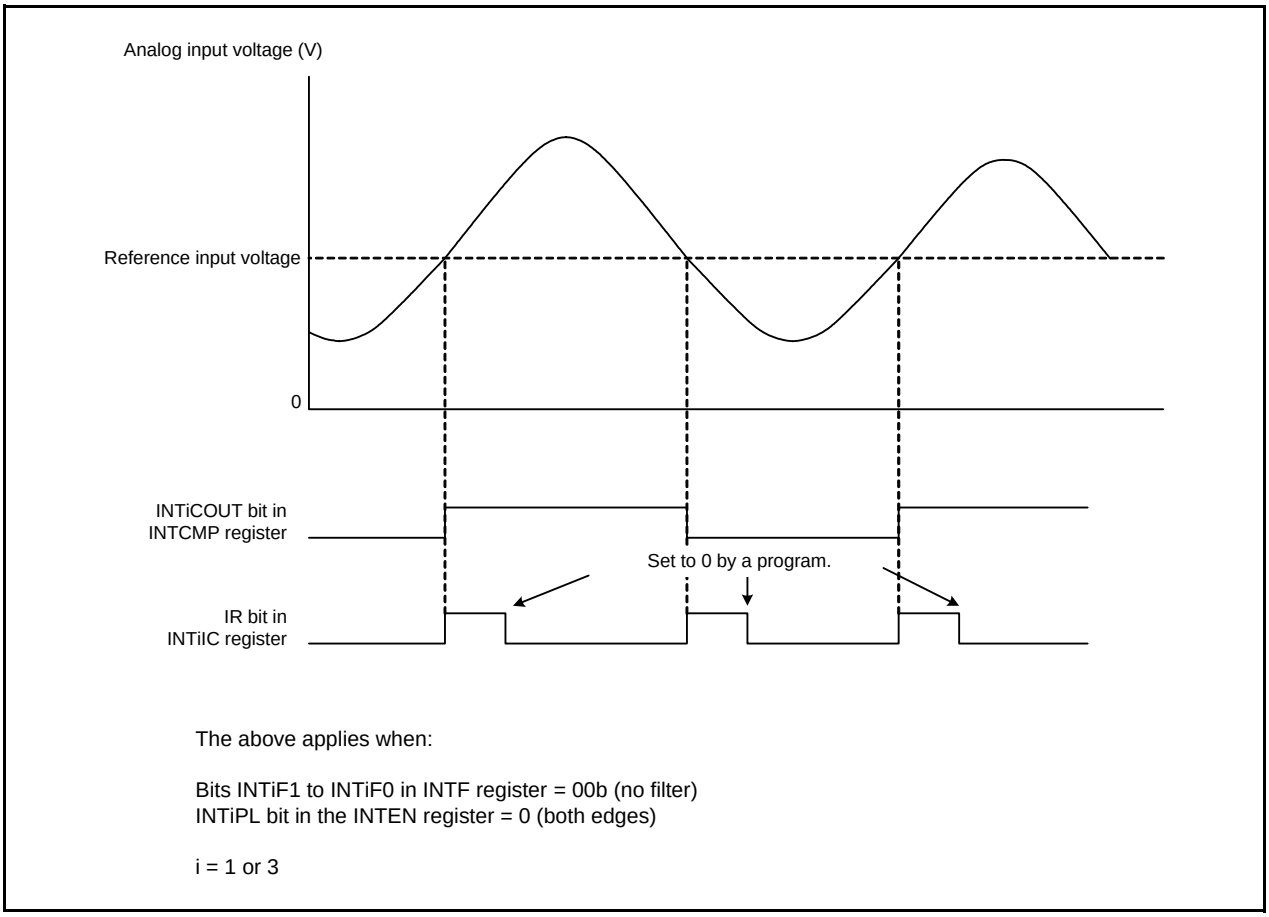


Figure 28.2 Operating Example of Comparator Bi (i = 1 or 3)

28.3.1 Comparator Bi Digital Filter (i = 1 or 3)

Comparator Bi can use the same digital filter as the $\overline{\text{INTi}}$ input. The sampling clock can be selected by bits INTiF1 and INTiF0 in the INTF register. The INTiCOUT signal output from comparator Bi is sampled every sampling clock. When the level matches three times, the IR bit in the INTiIC register is set to 1 (interrupt requested).

Figure 28.3 shows a Configuration of Comparator Bi Digital Filter and Figure 28.4 shows an Operating Example of Comparator Bi Digital Filter.

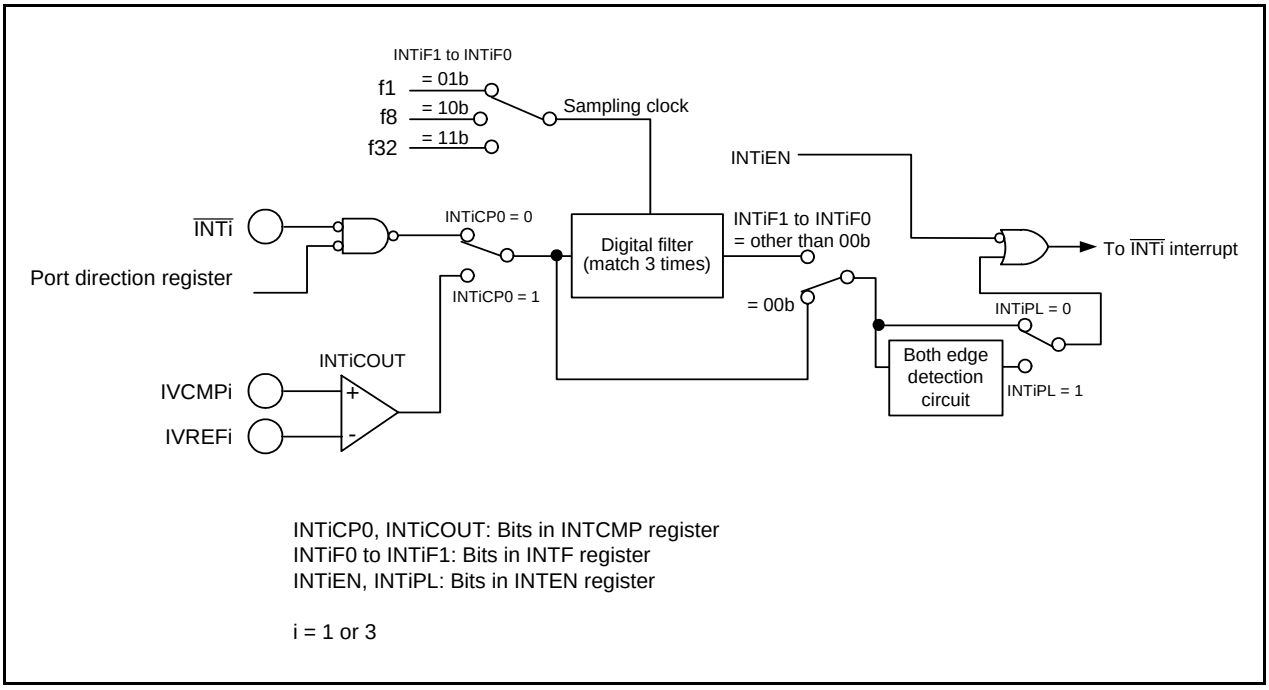


Figure 28.3 Configuration of Comparator Bi Digital Filter

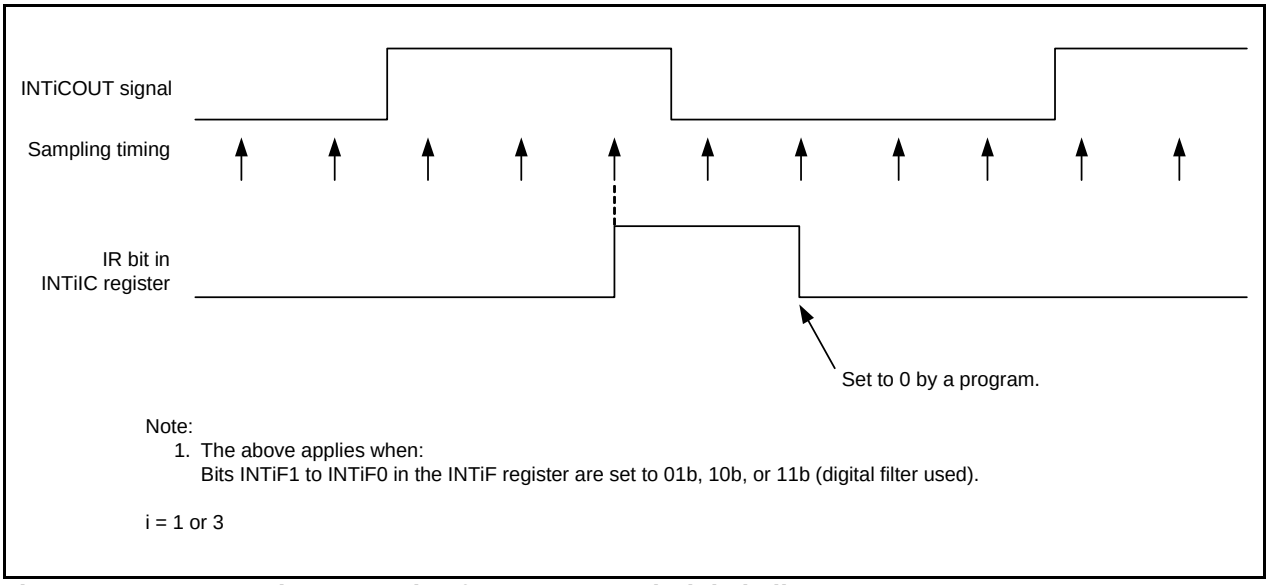


Figure 28.4 Operating Example of Comparator Bi Digital Filter

28.4 Comparator B1 and Comparator B3 Interrupts

Comparator B generates an interrupt request from two sources, comparator B1 and comparator B3. The comparator Bi (i = 1 or 3) interrupt uses the same INTiIC register (bits IR and ILVL0 to ILVL2) as the $\overline{\text{INTi}}$ (i = 1 or 3) and a single vector.

To use the comparator Bi interrupt, set the INTiEN bit in the INTEN register to 1 (interrupt enabled). In addition, the polarity can be selected by the INTiPL bit in the INTEN register and the POL bit in the INTiIC register.

Inputs can also be passed through the digital filter with three different sampling clocks.

29. Flash Memory

The flash memory can perform in the following three rewrite modes: CPU rewrite mode, standard serial I/O mode, and parallel I/O mode.

29.1 Overview

Table 29.1 lists the Flash Memory Version Performance (refer to **Tables 1.2 and 1.3 Specifications for R8C/3MU Group, R8C/3MK Group** for items not listed in Table 29.1).

Table 29.1 Flash Memory Version Performance

Item		Specification
Flash memory operating mode		3 modes (CPU rewrite, standard serial I/O, and parallel I/O)
Division of erase blocks		Refer to **Figures 29.1 and 29.2**.
Programming method		Byte units
Erasure method		Block erase
Programming and erasure control method (1)		Program and erase control by software commands
Rewrite control method	Blocks 0 to 6 (Program ROM) (3)	Rewrite protect control in block units by the lock bit
	Blocks A, B, C, and D (Data flash)	Individual rewrite protect control on blocks A, B, C, and D by bits FMR14, FMR15, FMR16, and FMR17 in the FMR1 register
Number of commands		7 commands
Programming and erasure endurance (2)	Blocks 0 to 6 (Program ROM) (3)	1,000 times
	Blocks A, B, C, and D (Data flash)	10,000 times
ID code check function		Standard serial I/O mode supported
ROM code protection		Parallel I/O mode supported

Notes:
1. To perform programming and erasure, use VCC = 2.7 to 5.5 V as the supply voltage. Do not perform programming and erasure at less than 2.7 V.
2. Definition of programming and erasure endurance
   The programming and erasure endurance is defined on a per-block basis. If the programming and erasure endurance is n (n = 1,000 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1-Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. When performing 100 or more rewrites, the actual erase count can be reduced by executing program operations in such a way that all blank areas are used before performing an erase operation. Avoid rewriting only particular blocks and try to average out the programming and erasure endurance of the blocks. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
3. The number of blocks and block division vary with the MCU. Refer to **Figures 29.1** and **29.2 Flash Memory Block Diagram of Each Group** for details.

Table 29.2 Flash Memory Rewrite Mode

Flash Memory Rewrite Mode	CPU Rewrite Mode	Standard Serial I/O Mode	Parallel I/O Mode
Function	User ROM area is rewritten by executing software commands from the CPU.	User ROM area is rewritten using a dedicated serial programmer.	User ROM area is rewritten using a dedicated parallel programmer.
Rewritable area	User ROM	User ROM	User ROM
Rewrite programs	User program	Standard boot program	—

29.2 Memory Map

The flash memory contains a user ROM area and a boot ROM area (reserved area).
Figure 29.1 shows Flash Memory Block Diagram of R8C/3MU Group, and Figure 29.2 shows the Flash Memory Block Diagram of R8C/3MK Group.
The user ROM area contains program ROM and data flash.
Program ROM: Flash memory mainly used for storing programs
Data flash: Flash memory mainly used for storing data to be rewritten
The user ROM area is divided into several blocks. The user ROM area can be rewritten in CPU rewrite mode, standard serial I/O mode, or parallel I/O mode.
The rewrite control program (standard boot program) for standard serial I/O mode is stored in the boot ROM area before shipment. The boot ROM area is allocated separately from the user ROM area.

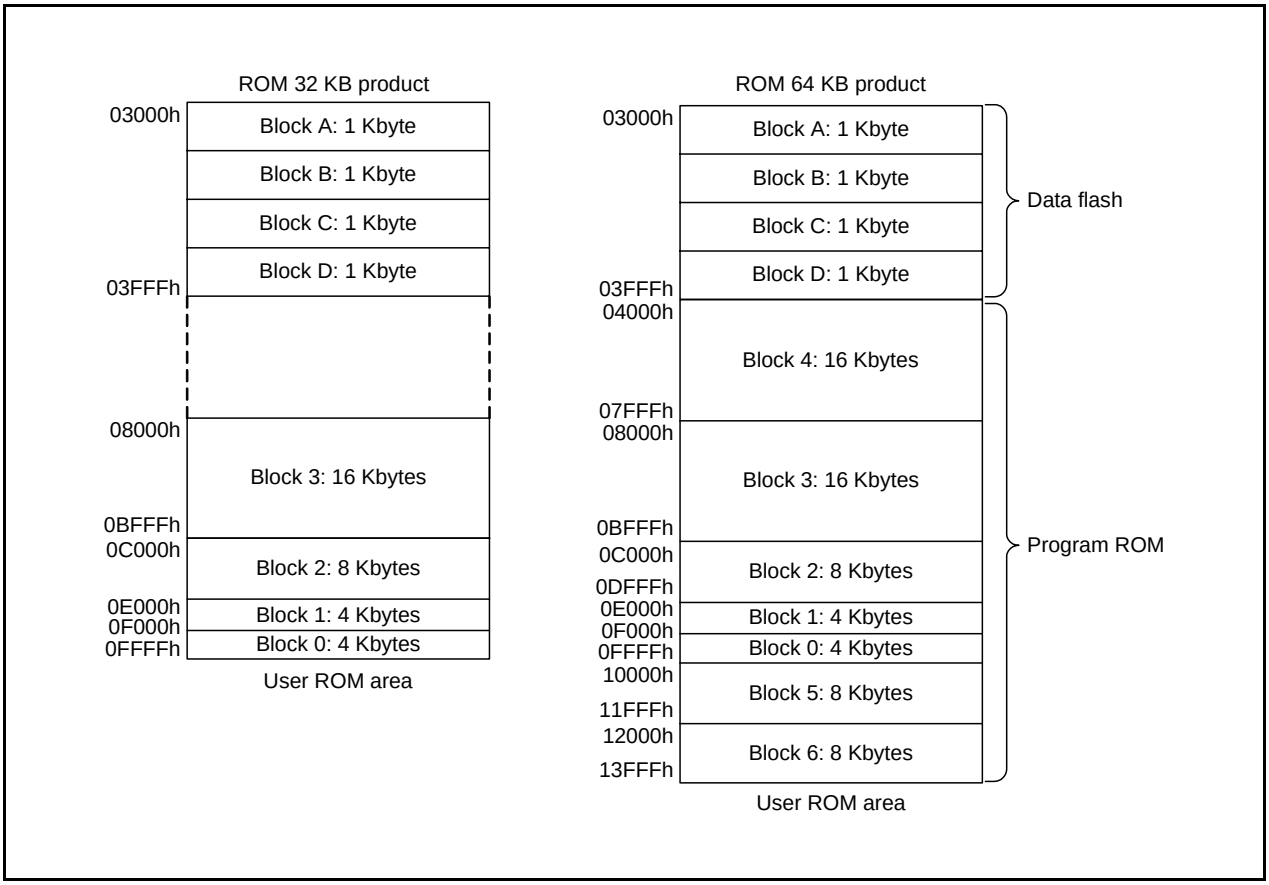


Figure 29.1 Flash Memory Block Diagram of R8C/3MU Group

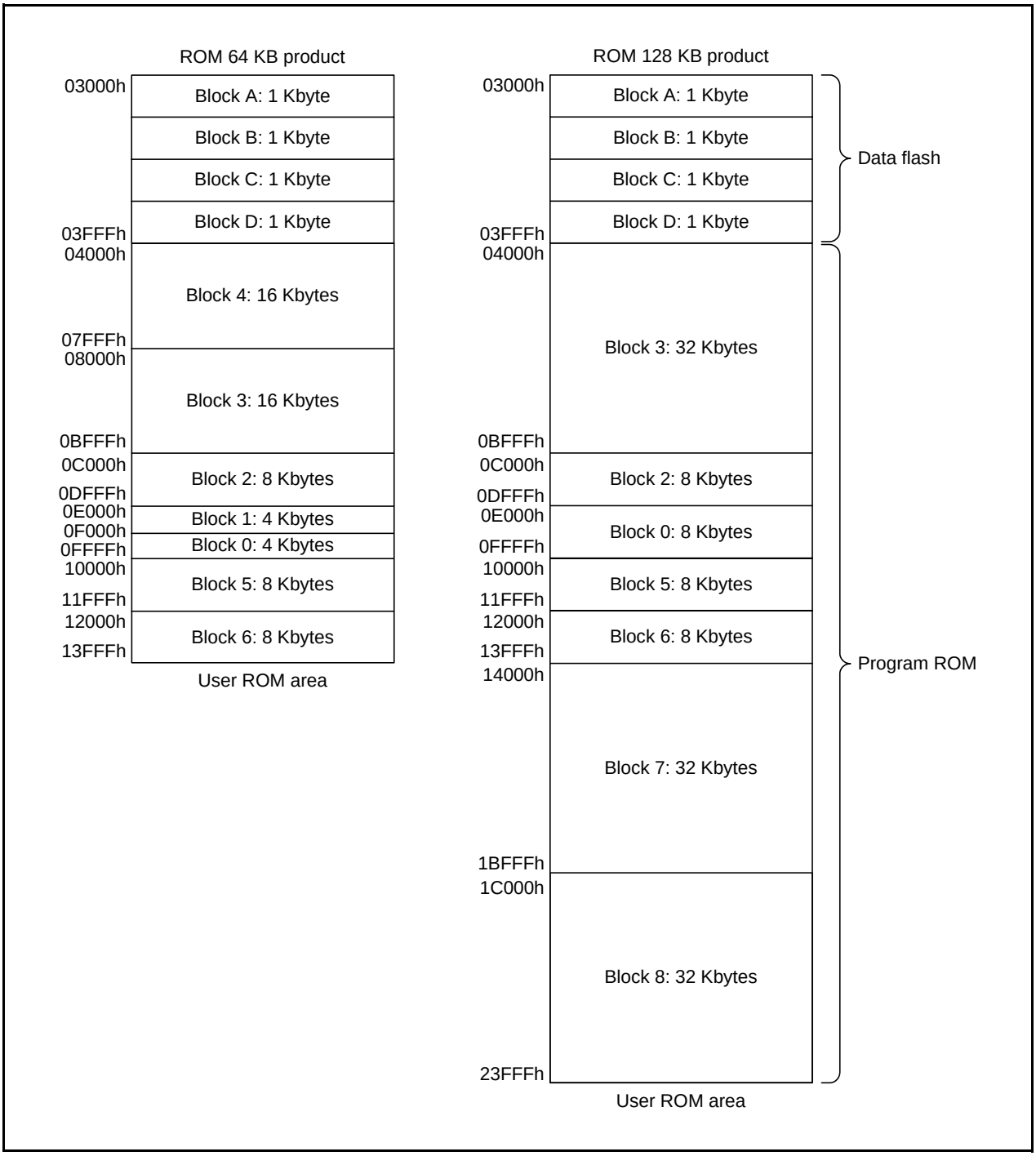


Figure 29.2 Flash Memory Block Diagram of R8C/3MK Group

29.3 Functions to Prevent Flash Memory from being Rewritten

Standard serial I/O mode has an ID code check function, and parallel I/O mode has a ROM code protect function to prevent the flash memory from being read or rewritten easily.

29.3.1 ID Code Check Function

The ID code check function is used in standard serial I/O mode. Unless 3 bytes (addresses 0FFFCh to 0FFFEh) of the reset vector are set to FFFFFFh, the ID codes sent from the serial programmer or the on-chip debugging emulator and the 7-byte ID codes written in the flash memory are checked to see if they match. If the ID codes do not match, the commands sent from the serial programmer or the on-chip debugging emulator are not accepted. For details of the ID code check function, refer to **12. ID Code Areas**.

29.3.2 ROM Code Protect Function

The ROM protect function prevents the contents of the flash memory from being read, rewritten, or erased using the OFS register in parallel I/O mode.
Refer to **13. Option Function Select Area** for details of the option function select area.

The ROM code protect function is enabled by writing 1 to the ROMCR bit and writing 0 to the ROMCP1 bit. This prevents the contents of the on-chip flash memory from being read or rewritten.
Once ROM code protection is enabled, the content of the internal flash memory cannot be rewritten in parallel I/O mode. To disable ROM code protection, erase the block including the OFS register using CPU rewrite mode or standard serial I/O mode.

29.3.3 Option Function Select Register (OFS)

Address 0FFFFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CSPROINI	LVDAS	VDSEL1	VDSEL0	ROMCP1	ROMCR	—	WDTON
After Reset	User Setting Value (1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTON	Watchdog timer start select bit	0: Watchdog timer automatically starts after reset 1: Watchdog timer is stopped after reset	R/W
b1	—	Reserved bit	Set to 1.	R/W
b2	ROMCR	ROM code protect disable bit	0: ROM code protect disabled 1: ROMCP1 bit enabled	R/W
b3	ROMCP1	ROM code protect bit	0: ROM code protect enabled 1: ROM code protect disabled	R/W
b4	VDSEL0	Voltage detection 0 level select bit (2)	b5 b4 0 0: 3.80 V selected (Vdet0_3) 0 1: 2.85 V selected (Vdet0_2) 1 0: 2.35 V selected (Vdet0_1) 1 1: 1.90 V selected (Vdet0_0)	R/W
b5	VDSEL1			R/W
b6	LVDAS	Voltage detection 0 circuit start bit (3)	0: Voltage monitor 0 reset enabled after reset 1: Voltage monitor 0 reset disabled after reset	R/W
b7	CSPROINI	Count source protection mode after reset select bit	0: Count source protect mode enabled after reset 1: Count source protect mode disabled after reset	R/W

Notes:
1. The OFS register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the OFS register. If the block including the OFS register is erased, the OFS register is set to FFh.
   When blank products are shipped, the OFS register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS register is the value programmed by the user.
2. The same level of the voltage detection 0 level selected by bits VDSEL0 and VDESL1 is set in both functions of voltage monitor 0 reset and power-on reset.
3. To use power-on reset and voltage monitor 0 reset, set the LVDAS bit to 0 (voltage monitor 0 reset enabled after reset).

For a setting example of the OFS register, refer to **13.3.1 Setting Example of Option Function Select Area**.

LVDAS Bit (Voltage Detection 0 Circuit Start Bit)

The Vdet0 voltage to be monitored by the voltage detection 0 circuit is selected by bits VDSEL0 and VDSEL1.

29.4 CPU Rewrite Mode

In CPU rewrite mode, the user ROM area can be rewritten by executing software commands from the CPU. Therefore, the user ROM area can be rewritten directly while the MCU is mounted on a board without using a ROM programmer. Execute the software command only to blocks in the user ROM area.
The flash module has an erase-suspend function which halts the erase operation temporarily during an erase operation in CPU rewrite mode. During erase-suspend, the flash memory can be read or programmed.
Erase-write 0 mode (EW0 mode) and erase-write 1 mode (EW1 mode) are available in CPU rewrite mode.
Table 29.3 lists the Differences between EW0 Mode and EW1 Mode.

Table 29.3 Differences between EW0 Mode and EW1 Mode

Item	EW0 Mode	EW1 Mode
Operating mode	Single-chip mode	Single-chip mode
Rewrite control program allocatable area	User ROM	User ROM
Rewrite control program executable areas	RAM (The rewrite control program must be transferred before being executed.) However, the program can be executed in the program ROM area when rewriting the data flash area.	User ROM or RAM
Rewritable area	User ROM	User ROM However, blocks which contain the rewrite control program are excluded.
Software command restrictions	—	Program and block erase commands Cannot be executed to any block which contains the rewrite control program.
Mode after programming or block erasure or after entering erase-suspend	Read array mode	Read array mode
CPU and DTC state during programming and block erasure	The CPU operates.	• The CPU or DTC operates while the data flash area is being programmed or block erased. • The CPU or DTC is put in a hold state while the program ROM area is being programmed or block erased (I/O ports retain the state before the command execution).
Flash memory status detection	Read bits FST7, FST5, and FST4 in the FST register by a program.	Read bits FST7, FST5, and FST4 in the FST register by a program.
Conditions for entering erase-suspend	• Set bits FMR20 and FMR21 in the FMR2 register to 1 by a program. • Set bits FMR20 and FMR22 in the FMR2 register to 1 and the enabled maskable interrupt is generated.	• Set bits FMR20 and FMR21 in the FMR2 register to 1 by a program (while rewriting the data flash area). • Set bits FMR20 and FMR22 in the FMR2 register to 1 and the enabled maskable interrupt is generated.
CPU clock	Max. 20 MHz	Max. 20 MHz

29.4.1 Flash Memory Status Register (FST)

Address 01B2h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	FST7	FST6	FST5	FST4	—	LBDATA	BSYAEI	RDYSTI
After Reset	1	0	0	0	0	X	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	RDYSTI	Flash ready status interrupt request flag (1, 4)	0: No flash ready status interrupt request 1: Flash ready status interrupt request	R/W
b1	BSYAEI	Flash access error interrupt request flag (2, 4)	0: No flash access error interrupt request 1: Flash access error interrupt request	R/W
b2	LBDATA	LBDATA monitor flag	0: Locked 1: Not locked	R
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	FST4	Program error flag (3)	0: No program error 1: Program error	R
b5	FST5	Erase error/blank check error flag (3)	0: No erase error/blank check error 1: Erase error/blank check error	R
b6	FST6	Erase-suspend status flag	0: Other than erase-suspend 1: During erase-suspend	R
b7	FST7	Ready/busy status flag	0: Busy 1: Ready	R

Notes:
1. The RDYSTI bit cannot be set to 1 (flash ready status interrupt request) by a program.
   When writing 0 (no flash ready status interrupt request) to the RDYSTI bit, read this bit (dummy read) before writing to it.
   Make sure the DTC is not activated by the flash ready status source between reading and writing.
   To confirm this bit, set the RDYSTIE bit in the FMR0 register to 1 (flash ready status interrupt enabled).
2. The BSYAEI bit cannot be set to 1 (flash access error interrupt request) by a program.
   When writing 0 (no flash access error interrupt request) to the BSYAEI bit, read this bit (dummy read) before writing to it.
   To confirm this bit, set the BSYAEIE bit in the FMR0 register to 1 (flash access error interrupt enabled) or set the CMDERIE bit in the FMR0 register to 1 (erase/write error interrupt enabled).
3. This bit is also set to 1 (error) when a command error occurs.
4. When this bit is set to 1, do not set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled).

RDYSTI Bit (Flash Ready Status Flag Interrupt Request Flag)

When the RDYSTIE bit in the FMR0 register is set to 1 (flash ready status interrupt enabled) and auto-programming or auto-erasure completes, or erase-suspend mode is entered, the RDYSTI bit is set to 1 (flash ready status interrupt request).
During interrupt handling, set the RDYSTI bit to 0 (no flash ready status interrupt request).

[Condition for setting to 0]
Set to 0 by an interrupt handling program.
[Condition for setting to 1]
When the flash memory status changes from busy to ready while the RDYSTIE bit in the FRMR0 register is set to 1, the RDYSTI bit is set to 1.
The status is changed from busy to ready in the following states:
- Completion of erasing/programming the flash memory
- Suspend acknowledgement
- Completion of forcible termination
- Completion of the lock bit program
- Completion of the read lock bit status
- Completion of the block blank check
- When the flash memory can be read after it has been stopped.

BSYAEI Bit (Flash Access Error Interrupt Request Flag)

The BSYAEI bit is set to 1 (flash access error interrupt request) when the BSYAEIE bit in the FMR0 register is set to 1 (flash access error interrupt enabled) and the block during auto-programming/auto-erasure is accessed. This bit is also set to 1 if an erase or program error occurs when the CMDERIE bit in the FMR0 register is set to 1 (erase/write error interrupt enabled).
During interrupt handling, set the BSYAEI bit to 0 (no flash access error interrupt request).

[Conditions for setting to 0]
(1) Set to 0 by an interrupt handling program.
(2) Execute the clear status register command.
[Conditions for setting to 1]
(1) Read or write the area that is being erased/written when the BSYAEIE bit in the FRMR0 register is set to 1 and while the flash memory is busy.
Or, read the data flash area while erasing/writing to the program ROM area. (Note that the read value is undefined in both cases. Writing has no effect.)
(2) If a command sequence error, erase error, blank check error, or program error occurs when the CMDERIE bit in the FMR0 register is set to 1 (erase/write error interrupt enabled).

LBDATA Bit (LBDATA Monitor Flag)

This is a read-only bit indicating the lock bit status. To confirm the lock bit status, execute the read lock bit status command and read the LBDATA bit after the FST7 bit is set to 1 (ready).
The condition for updating this bit is when the program, erase, read lock bit status commands are generated.
When the read lock bit status command is input, the FST7 bit is set to 0 (busy). At the time when the FST7 bit is set to 1 (ready), the lock bit status is stored in the LBDATA bit. The data in the LBDATA bit is retained until the next command is input.

FST4 Bit (Program Error Flag)

This is a read-only bit indicating the auto-programming status. The bit is set to 1 if a program error occurs; otherwise, it is set to 0. For details, refer to the description in **29.4.12 Full Status Check**.

FST5 Bit (Erase Error/Blank Check Error Flag)

This is a read-only bit indicating the status of auto-programming or the block blank check command. The bit is set to 1 if an erase error or blank check error occurs; otherwise, it is set to 0. Refer to **29.4.12 Full Status Check** for details.

FST6 Bit (Erase Suspend Status Flag)

This is a read-only bit indicating the suspend status. The bit is set to 1 when an erase-suspend request is acknowledged and a suspend status is entered; otherwise, it is set to 0.

FST7 Bit (Ready/Busy Status Flag)

When the FST7 bit is set to 0 (busy), the flash memory is in one of the following states:
- During programming
- During erasure
- During the lock bit program
- During the read lock bit status
- During the block blank check
- During forced stop operation
- The flash memory is being stopped
- The flash memory is being activated

Otherwise, the FST7 bit is set to 1 (ready).

29.4.2 Flash Memory Control Register 0 (FMR0)

Address 01B4h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	RDYSTIE	BSYAEIE	CMDERIE	CMDRST	FMSTP	FMR02	FMR01	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bit	Set to 0.	R/W
b1	FMR01	CPU rewrite mode select bit (1, 4)	0: CPU rewrite mode disabled 1: CPU rewrite mode enabled	R/W
b2	FMR02	EW1 mode select bit (1)	0: EW0 mode 1: EW1 mode	R/W
b3	FMSTP	Flash memory stop bit (2)	0: Flash memory operates 1: Flash memory stops (Low-power consumption state, flash memory initialization)	R/W
b4	CMDRST	Erase/write sequence reset bit (3)	When the CMDRST bit is set to 1, the erase/write sequence is reset and erasure/writing can be forcibly stopped. When read, the content is 0.	R/W
b5	CMDERIE	Erase/write error interrupt enable bit	0: Erase/write error interrupt disabled 1: Erase/write error interrupt enabled	R/W
b6	BSYAEIE	Flash access error interrupt enable bit	0: Flash access error interrupt disabled 1: Flash access error interrupt enabled	R/W
b7	RDYSTIE	Flash ready status interrupt enable bit	0: Flash ready status interrupt disabled 1: Flash ready status interrupt enabled	R/W

Notes:
1. To set this bit to 1, first write 0 and then 1 immediately. Disable interrupts and DTC activation between writing 0 and writing 1.
2. Write to the FMSTP bit by a program transferred to the RAM. The FMSTP bit is enabled when the FMR01 bit is set to 1 (CPU rewrite mode enabled). To set the FMSTP bit to 1 (flash memory stops), set it when the FST7 bit in the FST register is set to 1 (ready).
3. The CMDRST bit is enabled when the FMR01 bit is set to 1 (CPU rewrite mode enabled) and the FST7 bit in the FST register is set to 0 (busy).
4. To set the FMR01 bit to 0 (CPU rewrite mode disabled), set it when the RDYSTI bit in the FST register is set to 0 (no flash ready status interrupt request) and the BSYAEI bit is set to 0 (no flash access error interrupt request).

FMR01 Bit (CPU Rewrite Mode Select Bit)

When the FMR01 bit is set to 1 (CPU rewrite mode enabled), the MCU is made ready to accept software commands.

FMR02 Bit (EW1 Mode Select Bit)

When the FMR02 bit is set to 1 (EW1 mode), EW1 mode is selected.

FMSTP Bit (Flash Memory Stop Bit)

This bit is used to initialize the flash memory control circuits, and also to reduce the amount of current consumed by the flash memory. Access to the flash memory is disabled by setting the FMSTP bit to 1.
Write to the FMSTP bit by a program transferred to the RAM.
To reduce the power consumption further in high-speed on-chip oscillator mode, low-speed on-chip oscillator mode (XIN clock stopped), set the FMSTP bit to 1. Refer to **30.2.10 Stopping Flash Memory** for details.
When entering stop mode or wait mode while CPU rewrite mode is disabled, the FMR0 register does not need to be set because the power for the flash memory is automatically turned off and is turned back on when exiting stop or wait mode.
When the FMSTP bit is set to 1 (including during the busy status (the period while the FST7 bit is 0) immediately after the FMSTP bit is changed from 1 to 0), do not set to low-current-consumption read mode at the same time.

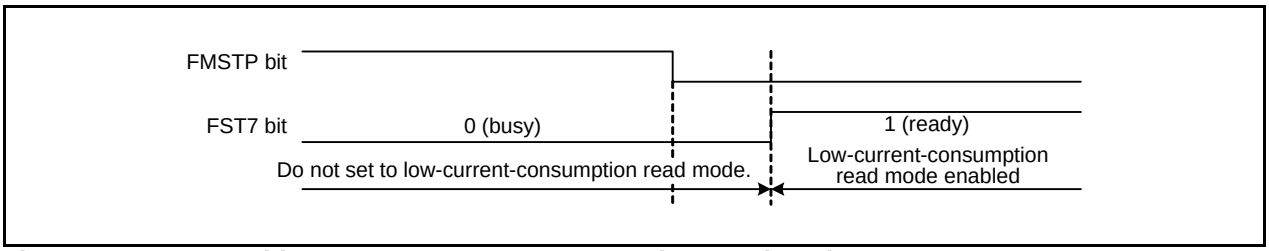


Figure 29.3 Transition to Low-Current-Consumption Read Mode

CMDRST Bit (Erase/Write Sequence Reset Bit)

This bit is used to initialize the flash memory sequence and forcibly stop a program or erase command. The program ROM area can be read when resetting the sequence of programming/erasing the data flash area.
If the program or erase command is forcibly stopped using the CMDRST bit in the FMR0 register, execute the clear status register command after the FST7 bit in the FST register is changed to 1 (ready). To program to the same address again, execute the block erase command again and ensure it has been completed normally before programming. If the addresses and blocks which the program or block erase command is forcibly stopped are allocated in the program area, set the FMR13 bit in the FMR1 register to 1 (lock bit disabled) before executing the block erasure command again.
When the CMDRST bit is set to 1 (erasure/writing stopped) during erase-suspend, the suspend status is also initialized. Thus execute block erasure again to the block which the block erasure is being suspended.
When td(CMDRST-READY) has elapsed after the CMDRST bit is set to 1 (erasure/writing stopped), the executing command is forcibly stopped and reading from the flash memory is enabled.

CMDERIE Bit (Erase/Write Error Interrupt Enable Bit)

This bit enables a flash command error interrupt to be generated if the following errors occur:
- Program error
- Block erase error
- Command sequence error
- Block blank check error

If the CMDERIE bit is set to 1 (erase/write error interrupt enabled), an interrupt is generated if the above errors occur.
If a flash command error interrupt is generated, execute the clear status register command during interrupt handling.

To change the CMDERIE bit from 0 (erase/write error interrupt disabled) to 1 (erase/write error interrupt enabled), make the setting as follows:
(1) Execute the clear status register command.
(2) Set the CMDERIE bit to 1.

BSYAEIE Bit (Flash Access Error Interrupt Enable Bit)

This bit enables a flash access error interrupt to be generated if the flash memory during rewriting is accessed.

To change the BSYAEIE bit from 0 (flash access error interrupt disabled) to 1 (flash access error interrupt enabled), make the setting as follows:
(1) Read the BSYAEI bit in the FST register (dummy read).
(2) Write 0 (no flash access error interrupt) to the BSYAEI bit.
(3) Set the BSYAEIE bit to 1 (flash access error interrupt enabled).

RDYSTIE Bit (Flash Ready Status Interrupt Enable Bit)

This bit enables a flash ready status error interrupt to be generated when the status of the flash memory sequence changes from the busy to ready status.

To change the RDYSTIE bit from 0 (flash ready status interrupt disabled) to 1 (flash ready status interrupt enabled), make the setting as follows:
(1) Read the RDYSTI bit in the FST register (dummy read).
(2) Write 0 (no flash ready status interrupt) to the RDYSTI bit.
(3) Set the RDYSTIE bit to 1 (flash ready status interrupt enabled).

29.4.3 Flash Memory Control Register 1 (FMR1)

Address 01B5h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	FMR17	FMR16	FMR15	FMR14	FMR13	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	—			
b2	—			
b3	FMR13	Lock bit disable select bit (1)	0: Lock bit enabled 1: Lock bit disabled	R/W
b4	FMR14	Data flash block A rewrite disable bit (2, 3)	0: Rewrite enabled (software command acceptable) 1: Rewrite disabled (software command not acceptable, no error occurred)	R/W
b5	FMR15	Data flash block B rewrite disable bit (2, 3)	0: Rewrite enabled (software command acceptable) 1: Rewrite disabled (software command not acceptable, no error occurred)	R/W
b6	FMR16	Data flash block C rewrite disable bit (2, 3)	0: Rewrite enabled (software command acceptable) 1: Rewrite disabled (software command not acceptable, no error occurred)	R/W
b7	FMR17	Data flash block D rewrite disable bit (2, 3)	0: Rewrite enabled (software command acceptable) 1: Rewrite disabled (software command not acceptable, no error occurred)	R/W

Notes:
1. To set the FMR13 bit to 1, first write 0 and then 1 immediately. Disable interrupts and DTC activation between writing 0 and writing 1.
2. To set this bit to 0, first write 1 and then 0 immediately. Disable interrupts and DTC activation between writing 1 and writing 0.
3. This bit is set to 0 when the FMR01 bit in the FMR0 register is set to 0 (CPU rewrite mode disabled).

FMR13 Bit (Lock Bit Disable Select Bit)

When the FMR13 bit is set to 1 (lock bit disabled), the lock bit is disabled. When the FMR13 bit is set to 0, the lock bit is enabled. Refer to **29.4.10 Data Protect Function** for the details of the lock bit.
The FMR13 bit enables the lock bit function only and the lock bit data does not change. However, when a block erase command is executed while the FMR13 bit is set to 1, the lock bit data set to 0 (locked) changes to 1 (not locked) after erasure completes.

[Conditions for setting to 0]
The FMR13 bit is set to 0 when one of the following conditions is met.
- Completion of the program command
- Completion of the erase command
- Generation of a command sequence error
- Transition to erase-suspend
- If the FMR01 bit in the FMR0 register is set to 0 (CPU rewrite mode disabled).
- If the FMSTP bit in the FMR0 register is set to 1 (flash memory stops).
- If the CMDRST bit in the FMR0 register is set to 1 (erasure/writing stopped).

[Condition for setting to 1]
Set to 1 by a program.

FMR14 Bit (Data Flash Block A Rewrite Disable Bit)

When the FMR 14 bit is set to 0, data flash block A accepts program and block erase commands.

FMR15 Bit (Data Flash Block B Rewrite Disable Bit)

When the FMR 15 bit is set to 0, data flash block B accepts program and block erase commands.

FMR16 Bit (Data Flash Block C Rewrite Disable Bit)

When the FMR 16 bit is set to 0, data flash block C accepts program and block erase commands.

FMR17 Bit (Data Flash Block D Rewrite Disable Bit)

When the FMR 17 bit is set to 0, data flash block D accepts program and block erase commands.

29.4.4 Flash Memory Control Register 2 (FMR2)

Address 01B6h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	FMR27	—	—	—	—	FMR22	FMR21	FMR20
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	FMR20	Erase-suspend enable bit (1)	0: Erase-suspend disabled 1: Erase-suspend enabled	R/W
b1	FMR21	Erase-suspend request bit (2)	0: Erase restart 1: Erase-suspend request	R/W
b2	FMR22	Interrupt request suspend request enable bit (1)	0: Erase-suspend request disabled by interrupt request 1: Erase-suspend request enabled by interrupt request	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—			
b7	FMR27	Low-current-consumption read mode enable bit (1, 3)	0: Low-current-consumption read mode disabled 1: Low-current-consumption read mode enabled	R/W

Notes:
1. To set this bit to 1, first write 0 and then 1 immediately. Disable interrupts and DTC activation between writing 0 and writing 1.
2. To set the FMR21 bit to 0 (erase restart), set it when the FMR01 bit in the FMR0 register is set to 1 (CPU rewrite mode enabled).
3. Set the FMR27 bit to 1 after setting either of the following:
   • Set the CPU clock to the low-speed on-chip oscillator clock divided by 4, 8, or 16.
   Enter wait mode or stop mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled).
   Do not enter wait mode or stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

FMR20 Bit (Erase-Suspend Enable Bit)

When the FMR20 bit is set to 1 (enabled), the erase-suspend function is enabled.

FMR21 Bit (Erase-Suspend Request Bit)

When the FMR21 bit is set to 1, erase-suspend mode is entered. If the FMR22 bit is set to 1 (erase-suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (erase-suspend request) when an interrupt request for the enabled interrupt is generated, and erase-suspend mode is entered. To restart auto-erasure, set the FMR21 bit to 0 (erase restart).

[Condition for setting to 0]
Set to 0 by a program.
[Conditions for setting to 1]
- When the FMR22 bit is set to 1 (erase-suspend request enabled by interrupt request) at the time an interrupt is generated.
- Set to 1 by a program.

FMR22 Bit (Interrupt Request Suspend-Request Enable Bit)

When the FMR 22 bit is set to 1 (erase-suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (erase-suspend request) at the time an interrupt request is generated during auto-erasure. Set the FMR22 bit to 1 when using erase-suspend while rewriting the user ROM area in EW1 mode.

FMR27 Bit (Low-Current-Consumption Read Mode Enable Bit)

When the FMR 27 bit is set to 1 (low-current-consumption read mode enabled) in low-speed on-chip oscillator mode (XIN clock stopped), power consumption when reading the flash memory can be reduced. Refer to **30.2.11 Low-Current-Consumption Read Mode** for details.

Low-current-consumption read mode can be used when the CPU clock is set to either of the following:

- The CPU clock is set to the low-speed on-chip oscillator clock divided by 4, 8, or 16.

However, do not use low-current-consumption read mode when the frequency of the selected CPU clock is 3 kHz or below.

After setting the divide ratio of the CPU clock, set the FMR27 bit to 1.

Enter wait mode or stop mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled).

Do not enter wait mode or stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

When the FMR27 bit is set to 1 (low-current-consumption read mode enabled), do not execute the program, block erase, or lock bit program command. To change the FMSTP bit from 1 (flash memory stops) to 0 (flash memory operates), make the setting when the FMR27 bit is set to 0 (low-current-consumption read mode disabled).

29.4.5 EW0 Mode

When the FMR01 bit in the FMR0 register is set to 1 (CPU rewrite mode enabled), the MCU enters CPU rewrite mode and software commands can be accepted. At this time, the FMR02 bit in the FMR0 register is set to 0 so that EW0 mode is selected.

Software commands are used to control program and erase operations. The FST register can be used to confirm whether programming or erasure has completed.

To enter erase-suspend during auto-erasure, set the FMR20 bit to 1 (erase-suspend enabled) and the FMR21 bit to 1 (erase-suspend request). Next, verify the FST7 bit in the FST register is set to 1 (ready), then verify the FST6 bit is set to 1 (during erase-suspend) before accessing the flash memory. When the FST6 bit is set to 0, erasure completes.

When the FMR21 bit in the FMR2 register is set to 0 (erase restart), auto-erasure restarts. To confirm whether auto-erasure has restarted, verify the FST7 bit in the FST register is set to 0, then verify the FST6 bit is set to 0 (other than erase-suspend).

29.4.6 EW1 Mode

After the FMR01 bit in the FMR0 register is set to 1 (CPU rewrite mode enabled), EW1 mode is selected by setting the FMR02 bit is set to 1.

The FST register can be used to confirm whether programming and erasure has completed.

To enable the erase-suspend function during auto-erasure, execute the block erase command after setting the FMR20 bit in the FMR2 register to 1 (suspend enabled). To enter erase-suspend while auto-erasing the user ROM area, set the FMR22 bit in the FMR2 register to 1 (erase-suspend request enabled by interrupt request). Also, the interrupt to enter erase-suspend must be enabled beforehand.

When an interrupt request is generated, the FMR21 bit in the FMR2 register is automatically set to 1 (erase-suspend request) and auto-erasure suspends after td(SR-SUS). After interrupt handling completes, set the FMR21 bit to 0 (erase restart) to restart auto-erasure.

29.4.7 Suspend Operation

The suspend function halts the auto-erase operation temporarily during auto-erasure.
When auto-erasure is suspended, the next operation can be executed (refer to **Table 29.4 Executable Operation during Suspend**).

- When suspending the auto-erasure of any block in data flash, auto-programming and reading another block can be executed.
- When suspending the auto-erasure of data flash, auto-programming and reading program ROM can be executed.
- When suspending the auto-erasure of any block in program ROM, auto-programming and reading another block can be executed.
- When suspending the auto-erasure of program ROM, auto-programming and reading data flash can be executed.
- To check the suspend, verify the FST7 bit is set to 1 (ready), then verify the FST6 bit is set to 1 (during erase-suspend) to confirm whether erasure has been suspended. When the FST6 bit is set to 0 (other than erase suspend), erasure completes.

Figure 29.4 shows the Suspend Operation Timing.

Table 29.4 Executable Operation during Suspend

		Operation during Suspend											
		Data flash (Block during erasure execution before entering suspend)			Data flash (Block during no erasure execution before entering suspend)			Program ROM (Block during erasure execution before entering suspend)			Program ROM (Block during no erasure execution before entering suspend)		
		Erase	Program	Read	Erase	Program	Read	Erase	Program	Read	Erase	Program	Read
Areas during erasure execution before entering suspend	Data flash	D	D	D	D	E	E	N/A	N/A	N/A	D	E	E (5)
	Program ROM	N/A	N/A	N/A	D	E	E	D	D	D	D	E	E

Notes:
1. E indicates operation is enabled by using the suspend function, D indicates operation is disabled, and N/A indicates no combination is available.
2. Operation cannot be suspended during programming.
3. The block erase command can be executed for erasure. The program, lock bit program, and read lock bit status commands can be executed for programming.
   The clear status register command can be executed when the FST7 bit in the FST register is set to 1 (ready).
   The operation of block blank check is disabled during suspend.
4. The MCU enters read array mode immediately after entering erase-suspend.
5. The program ROM area can be read with the BGO function while programming or block erasing data flash.

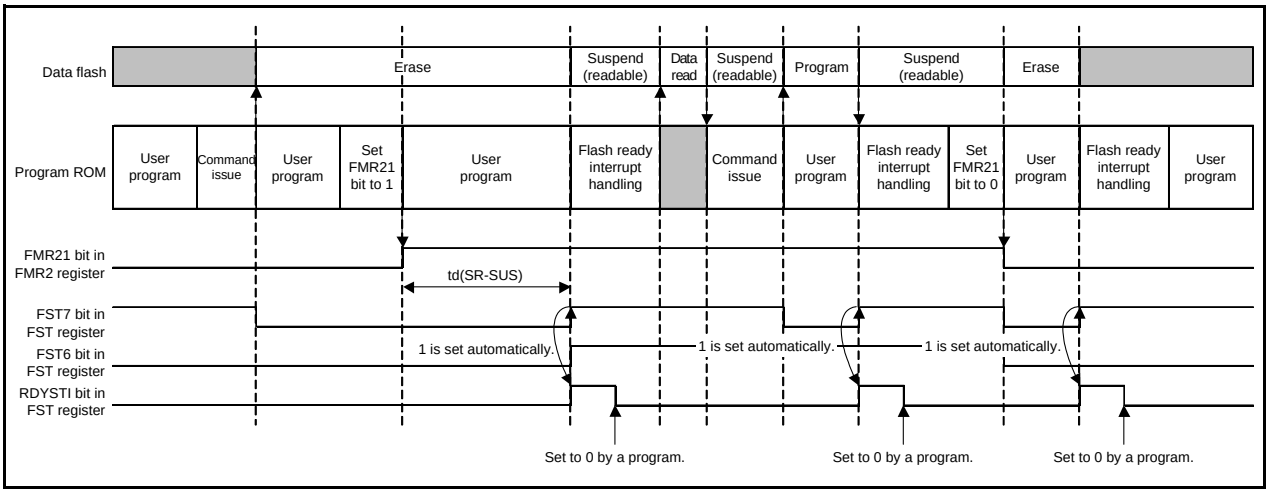


Figure 29.4 Suspend Operation Timing

29.4.8 How to Set and Exit Each Mode

Figure 29.5 shows How to Set and Exit EW0 Mode and Figure 29.6 shows How to Set and Exit EW0 Mode (When Rewriting Data Flash) and EW1 Mode.

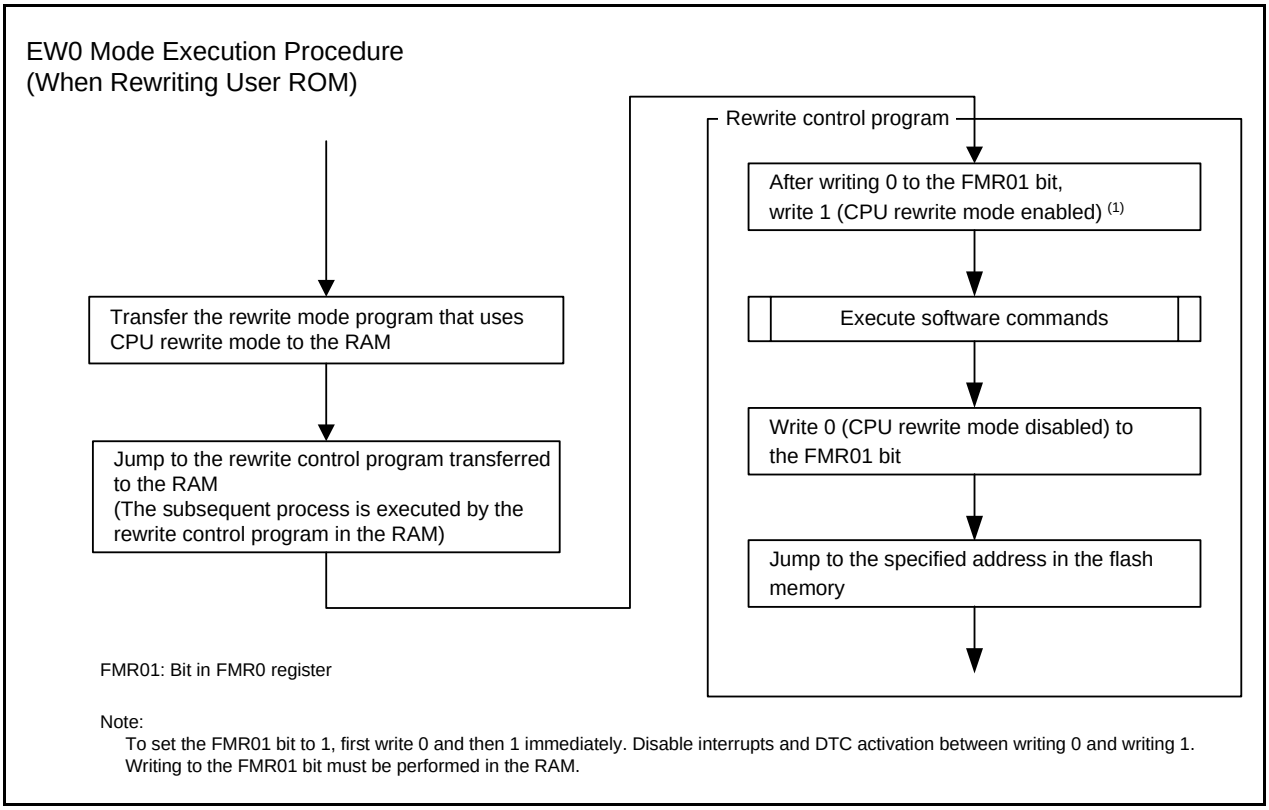


Figure 29.5 How to Set and Exit EW0 Mode

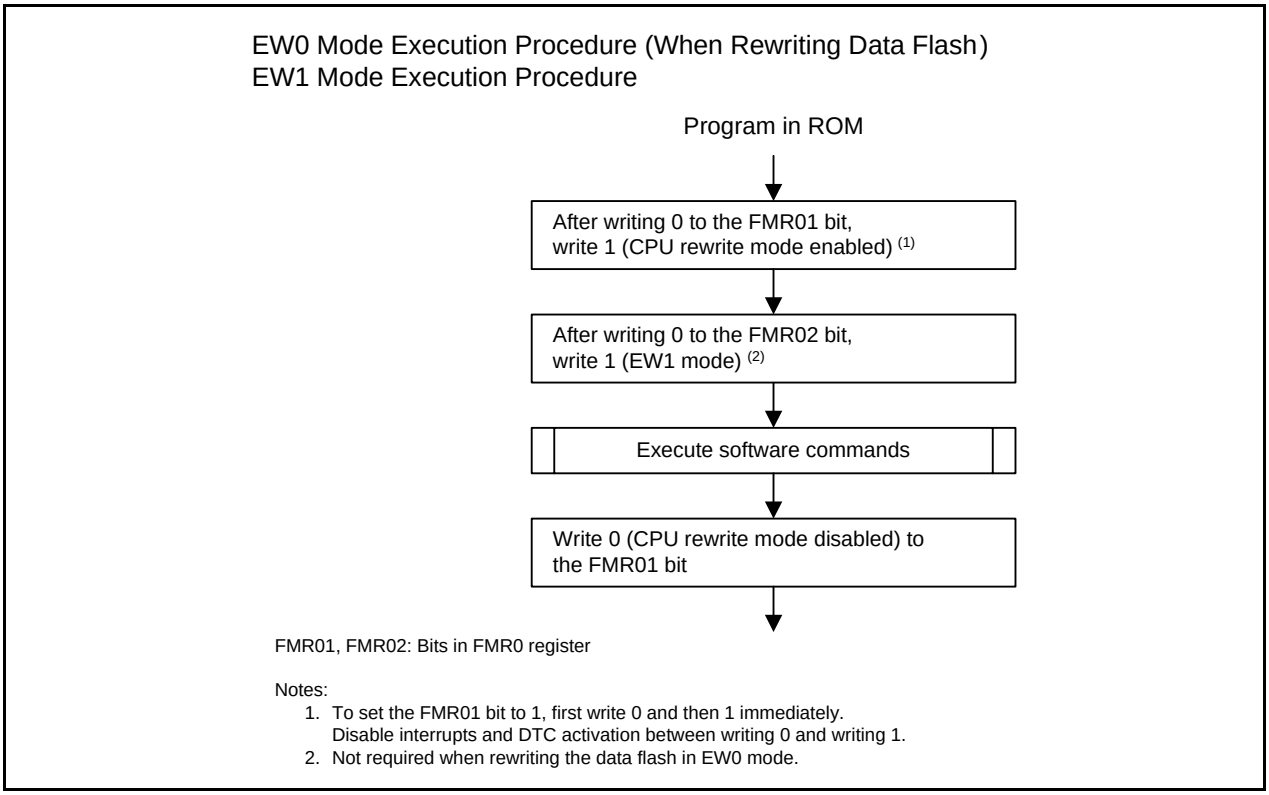


Figure 29.6 How to Set and Exit EW0 Mode (When Rewriting Data Flash) and EW1 Mode

29.4.9 BGO (BackGround Operation) Function

When the program ROM area is specified while a program or block erase operation to the data flash, array data can be read. This eliminates the need for writing software commands. Access time is the same as for normal read operations.
Any other block of the data flash cannot read during a program or block erase operation to the data flash.
Figure 29.7 shows the BGO Function.

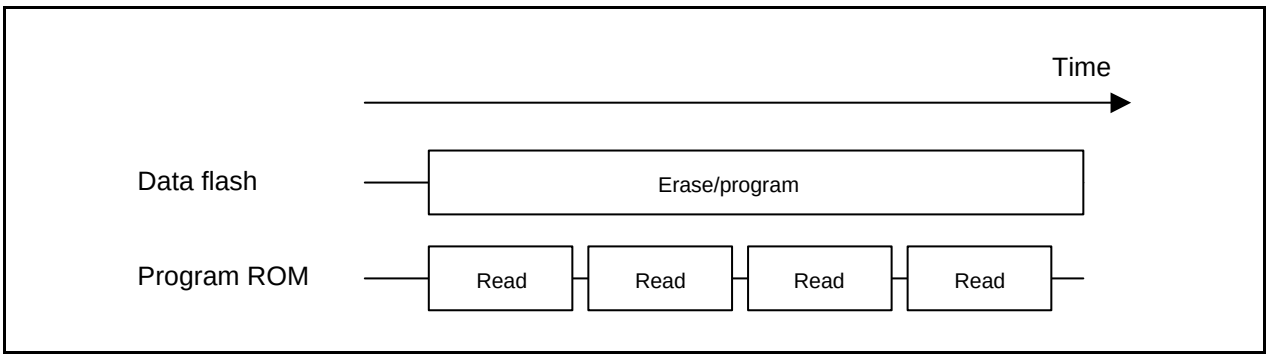


Figure 29.7 BGO Function

29.4.10 Data Protect Function

Each block in the flash memory has a nonvolatile lock bit. The lock bit is enabled by setting the FMR13 bit in the FMR1 register is set to 0 (lock bit enabled). The lock bit can be used to disable (lock) programming or erasing each block. This prevents data from being written or erased inadvertently. A block status changes according to the lock bit as follows:

- When the lock bit data is set to 0: locked (the block cannot be programmed or erased)
- When the lock bit data is set to 1: not locked (the block can be programmed and erased)

The lock bit data is set to 0 (locked) by executing the lock bit program command and to 1 (not locked) by erasing the block. No commands can be used to set only the lock bit data to 1.
The lock bit data can be read using the read lock bit status command.

When the FMR13 bit is set to 1 (lock bit disabled), the lock bit function is disabled and all blocks are not locked (each lock bit data remains unchanged). The lock bit function is enabled by setting the FMR13 bit to 0 (the lock bit data is retained).
When the block erase command is executed while the FMR13 bit is set to 1, the target block is erased regardless of the lock bit status. The lock bit of the erase target block is set to 1 after auto-erasure completes.
Refer to **29.4.11 Software Commands** for the details of individual commands.
The FMR13 bit is set to 0 after auto-erasure completes. This bit is also set to 0 if one of the following conditions is met. To erase or program a different locked block, set the FMR 13 bit to 1 again and execute the block erase or program command.

- If the FST7 bit in the FST register is changed from 0 (busy) to 1 (ready).
- If a command sequence error occurs.
- If the FMR01 bit in the FMR0 register is set to 0 (CPU mode disabled).
- If the FMSTP bit in the FM0 register is set to 1 (flash memory stops).
- If the CMDRST bit in the FMR0 register is set to 1 (erasure/writing stopped).

Figure 29.8 shows the FMR13 Bit Operation Timing.

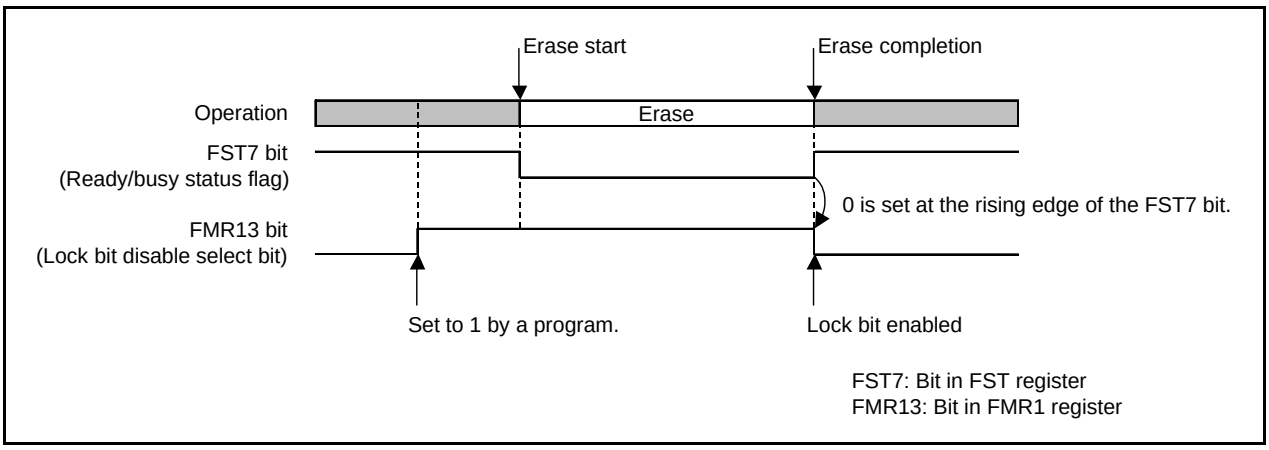


Figure 29.8 FMR13 Bit Operation Timing

29.4.11 Software Commands

The software commands are described below. Read or write commands and data in 8-bit units.
Do not input any command other than those listed in the table below.

Table 29.5 Software Commands

Command	First Bus Cycle			Second Bus Cycle		
	Mode	Address	Data	Mode	Address	Data
Read array	Write	×	FFh			
Clear status register	Write	×	50h			
Program	Write	WA	40h	Write	WA	WD
Block erase	Write	×	20h	Write	BA	D0h
Lock bit program	Write	BT	77h	Write	BT	D0h
Read lock bit status	Write	×	71h	Write	BT	D0h
Block blank check	Write	×	25h	Write	BA	D0h

WA: Write address
WD: Write data
BA: Any block address
BT: Starting block address
×: Any address in the user ROM area

29.4.11.1 Read Array Command

The read array command is used to read the flash memory.
When FFh is written in the first bus cycle, the MCU enters read array mode. When the read address is input in the following bus cycles, the content of the specified address can be read in 8-bit units.
Since read array mode remains until another command is written, the contents of multiple addresses can be read continuously.
In addition, after a reset, the MCU enters read array mode after a program, block erase, block blank check, read lock bit status, or clear status register command, or after entering erase-suspend.

29.4.11.2 Clear Status Register Command

The clear status register command is used to set bits FST4 and FST5 in the FST register to 0.
When 50h is written in the first bus cycle, bits FST4 and FST5 in the FST register are set to 0.

29.4.11.3 Program Command

The program command is used to write data to the flash memory in 1-byte units.
When 40h is written in the first bus cycle and data is written in the second bus cycle to the write address, auto-programming (data program and verify operation) starts. Make sure the address value specified in the first bus cycle is the same address as the write address specified in the second bus cycle.
The FST7 bit in the FST register can be used to confirm whether auto-programming has completed. The FST7 bit is set to 0 during auto-programming and is set to 1 when auto-programming completes.
After auto-programming has completed, the auto-program result can be confirmed by the FST4 bit in the FST register (refer to **29.4.12 Full Status Check**).
Do not write additions to the already programmed addresses.

The program command targeting each block in the program ROM can be disabled using the lock bit.
The following commands are not accepted under the following conditions:
- Block erase commands targeting data flash block A when the FMR14 bit in the FMR1 register is set to 1 (rewrite disabled).
- Block erase commands targeting data flash block B when the FMR15 bit is set to 1 (rewrite disabled).
- Block erase commands targeting data flash block C when the FMR16 bit is set to 1 (rewrite disabled).
- Block erase commands targeting data flash block D when the FMR17 bit is set to 1 (rewrite disabled).

Figure 29.9 shows a Program Flowchart (Flash Ready Status Interrupt Disabled) and Figure 29.10 shows a Program Flowchart (Flash Ready Status Interrupt Enabled).

In EW1 mode, do not execute this command to any address where a rewrite control program is allocated.

When the RDYSTIE bit in the FMR0 register is set to 1 (flash ready status interrupt enabled), a flash ready status interrupt can be generated upon completion of auto-programming. The auto-program result can be confirmed by reading the FST register during the interrupt routine.

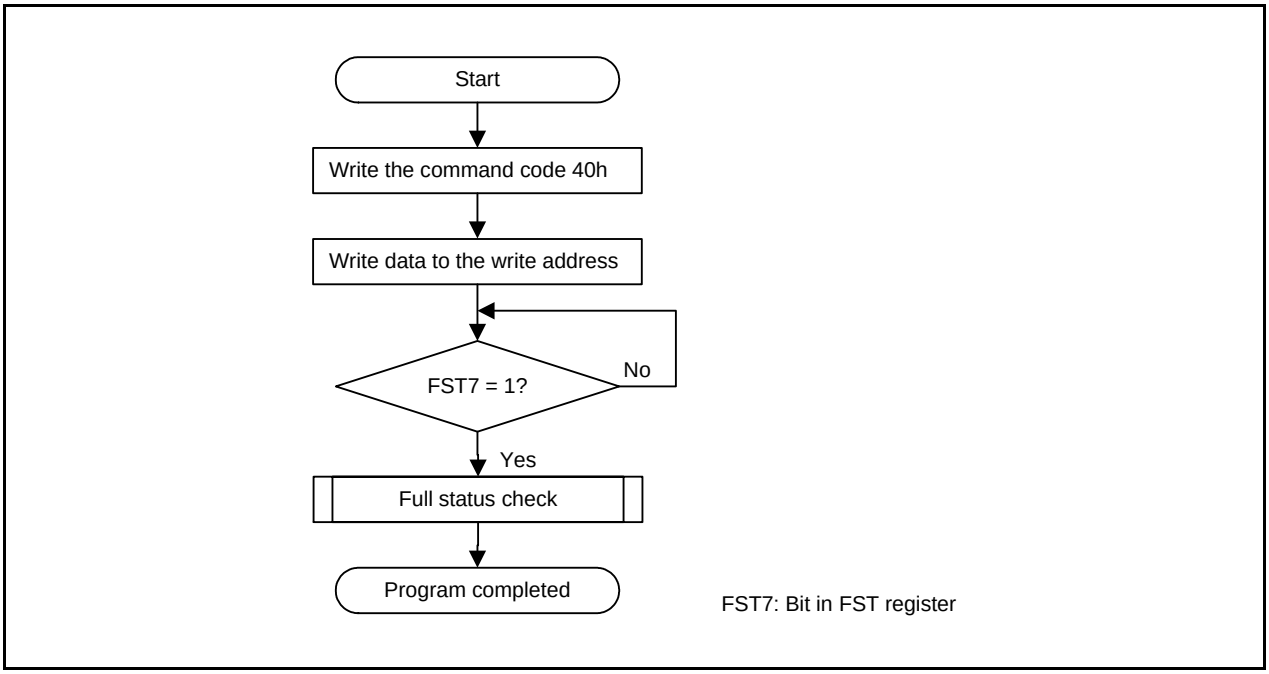


Figure 29.9 Program Flowchart (Flash Ready Status Interrupt Disabled)

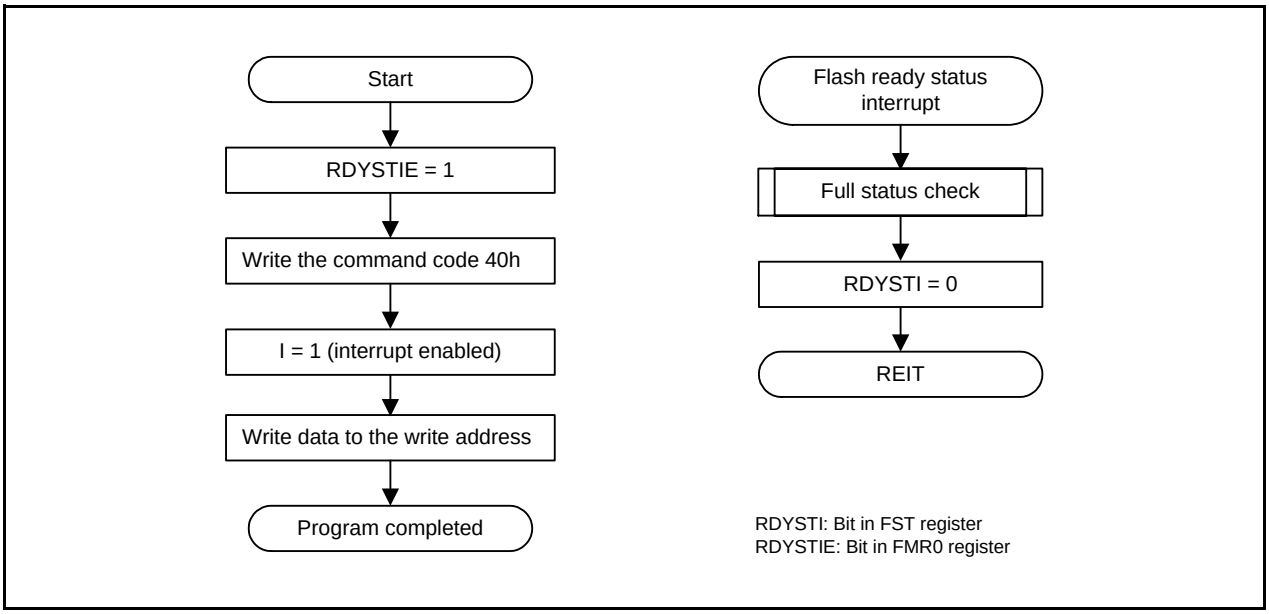


Figure 29.10 Program Flowchart (Flash Ready Status Interrupt Enabled)

29.4.11.4 Block Erase Command

When 20h is written in the first bus cycle and then D0h is written in the second bus cycle to any block address, auto-erasure (erase and erase verify operation) starts in the specified block.
The FST7 bit in the FST register can be used to confirm whether auto-erasure has completed. The FST7 bit is set to 0 during auto-erasure and is set to 1 when auto-erasure completes. After auto-erasure completes, all data in the block is set to FFh.
After auto-erasure has completed, the auto-erase result can be confirmed by the FST5 bit in the FST register (refer to **29.4.12 Full Status Check**).

The block erase command targeting each block in the program ROM can be disabled using the lock bit.
The following commands are not accepted under the following conditions:

- Block erase commands targeting data flash block A when the FMR14 bit in the FMR1 register is set to 1 (rewrite disabled).
- Block erase commands targeting data flash block B when the FMR15 bit is set to 1 (rewrite disabled).
- Block erase commands targeting data flash block C when the FMR16 bit is set to 1 (rewrite disabled).
- Block erase commands targeting data flash block D when the FMR17 bit is set to 1 (rewrite disabled).

Figure 29.11 shows a Block Erase Flowchart (Flash Ready Status Interrupt Disabled), Figure 29.12 shows a Block Erase Flowchart (Flash Ready Status Interrupt Disabled and Suspend Enabled), and Figure 29.13 shows a Block Erase Flowchart (Flash Ready Status Interrupt Enabled and Suspend Enabled).

In EW1 mode, do not execute this command to any block where a rewrite control program is allocated.

While the RDYSTIE bit in the FMR0 register is set to 1 (flash ready status interrupt enabled), a flash ready status interrupt can be generated upon completion of auto-erasure. While the RDYSTIE bit is set to 1 and the FMR20 bit in the FMR2 register is set to 1 (erase-suspend enabled), a flash ready status interrupt is generated when the FMR21 bit is set to 1 (erase-suspend request) and auto-erasure suspends. The auto-erase result can be confirmed by reading the FST register during the interrupt routine.

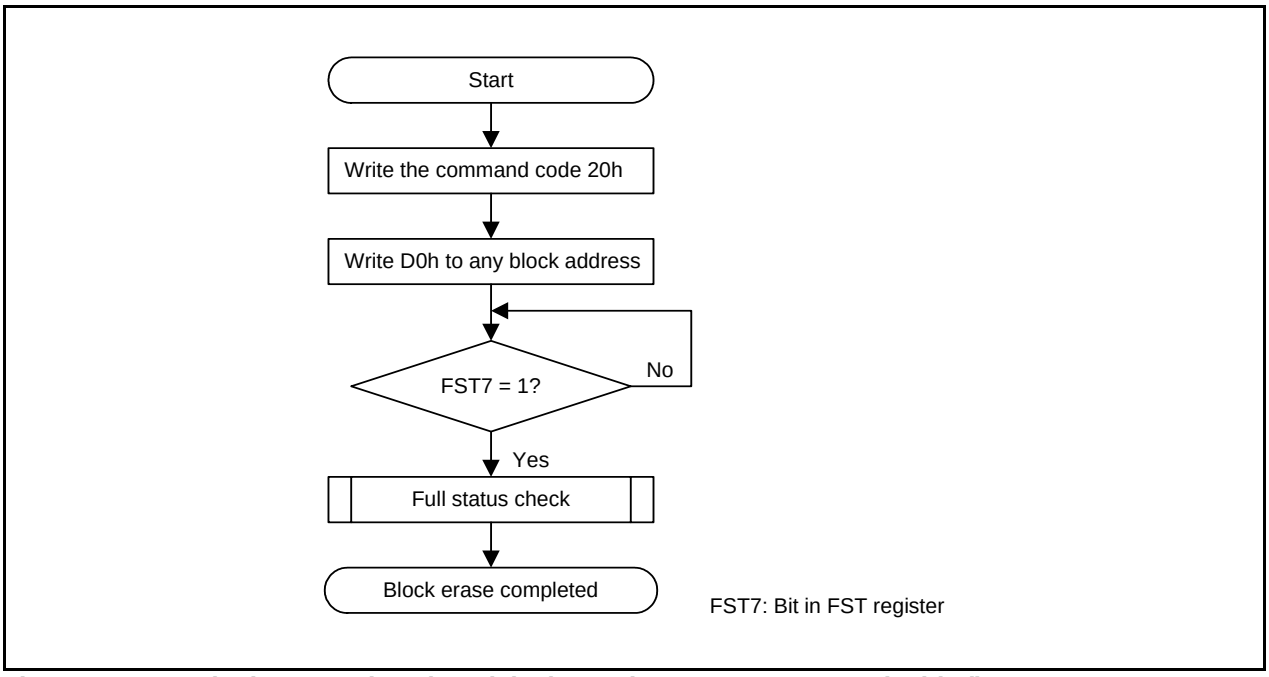
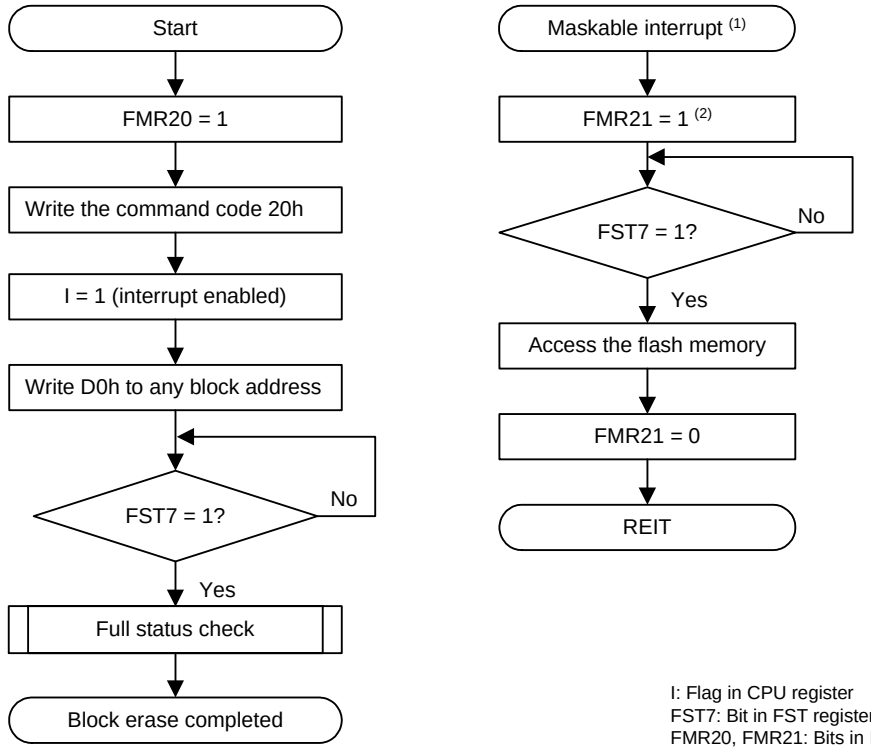
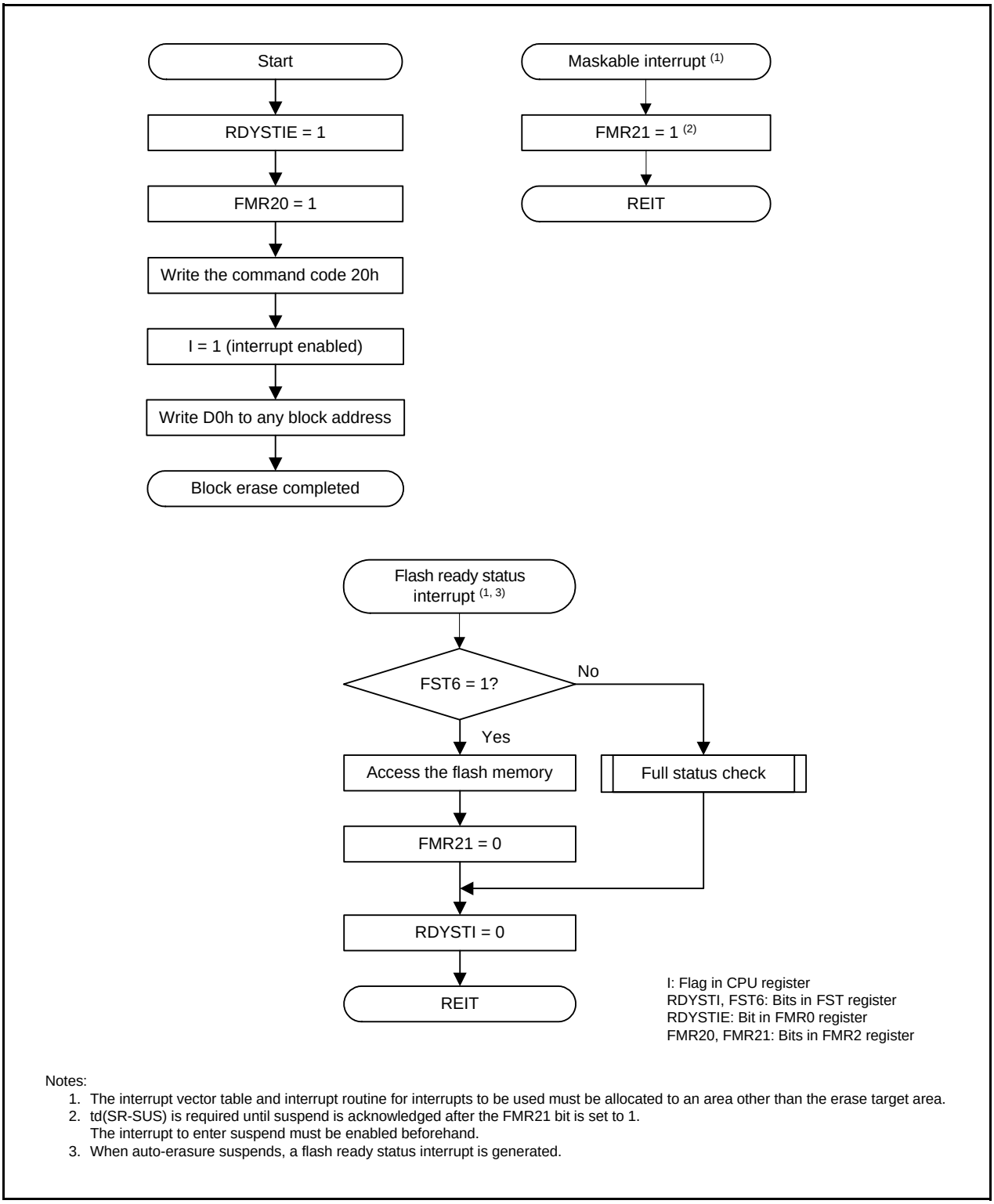


Figure 29.11 Block Erase Flowchart (Flash Ready Status Interrupt Disabled)



Notes:
1. The interrupt vector table and interrupt routine for interrupts to be used must be allocated to an area other than the erase target area.
2. td(SR-SUS) is required until suspend is acknowledged after the FMR21 bit is set to 1.
   The interrupt to enter suspend must be enabled beforehand.

Figure 29.12 Block Erase Flowchart (Flash Ready Status Interrupt Disabled and Suspend Enabled)



Notes:
1. The interrupt vector table and interrupt routine for interrupts to be used must be allocated to an area other than the erase target area.
2. td(SR-SUS) is required until suspend is acknowledged after the FMR21 bit is set to 1.
   The interrupt to enter suspend must be enabled beforehand.
3. When auto-erasure suspends, a flash ready status interrupt is generated.

Figure 29.13 Block Erase Flowchart (Flash Ready Status Interrupt Enabled and Suspend Enabled)

29.4.11.5 Lock Bit Program Command

This command is used to set the lock bit of any block in the program ROM area to 0 (locked).
When 77h is written in the first bus cycle and D0h is written in the second bus cycle to the starting block address, 0 is written to the lock bit of the specified block. Make sure the address value in the first bus cycle is the same address as the starting block address specified in the second bus cycle.
Figure 29.14 shows a Lock Bit Program Flowchart. The lock bit status (lock bit data) can be read using the read lock bit status command.
The FST7 bit in the FST register can be used to confirm whether writing to the lock bit has completed.
Refer to **29.4.10 Data Protect Function** for the lock bit function and how to set the lock bit to 1 (not locked).

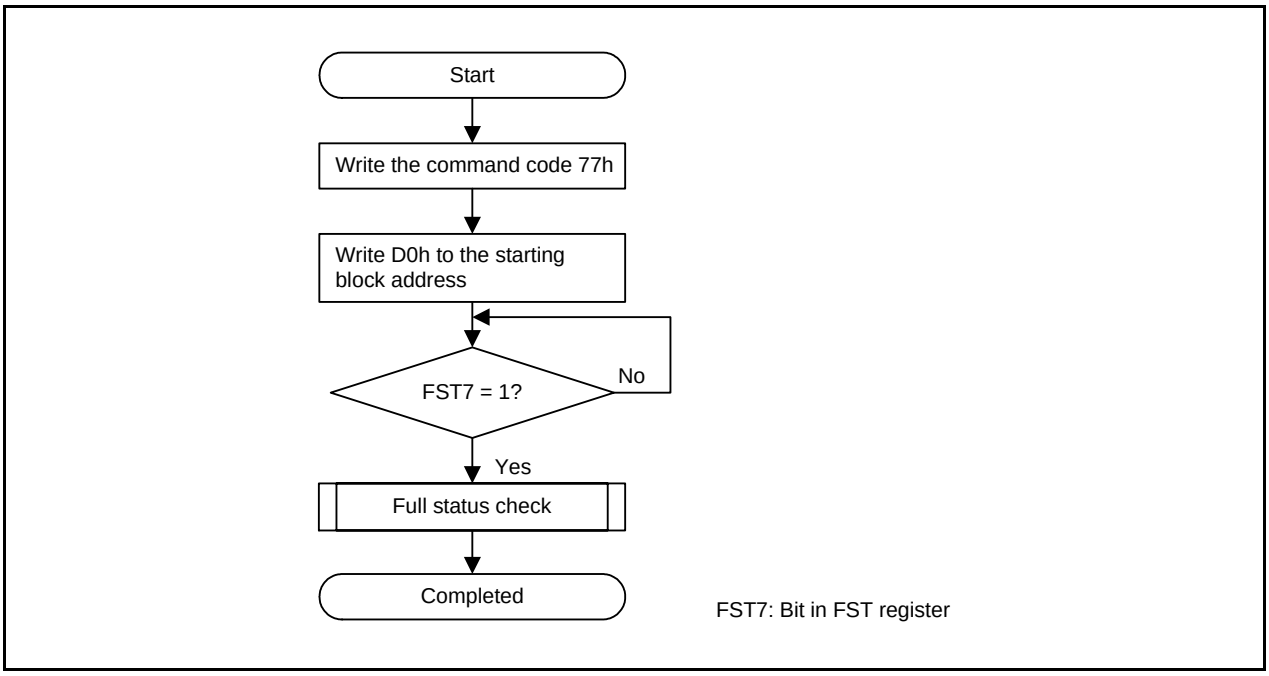


Figure 29.14 Lock Bit Program Flowchart

29.4.11.6 Read Lock Bit Status Command

This command is used to read the lock bit status of any address in the program ROM area.
When 71h written in the first bus cycle and D0h is written in the second cycle to the starting block address, the lock bit status of the specified block is stored in the LBDATA bit in the FST register. After the FST7 bit in the FST register has been set to 1 (ready), read the LBDATA bit.
Figure 29.15 shows a Read Lock Bit Status Flowchart.

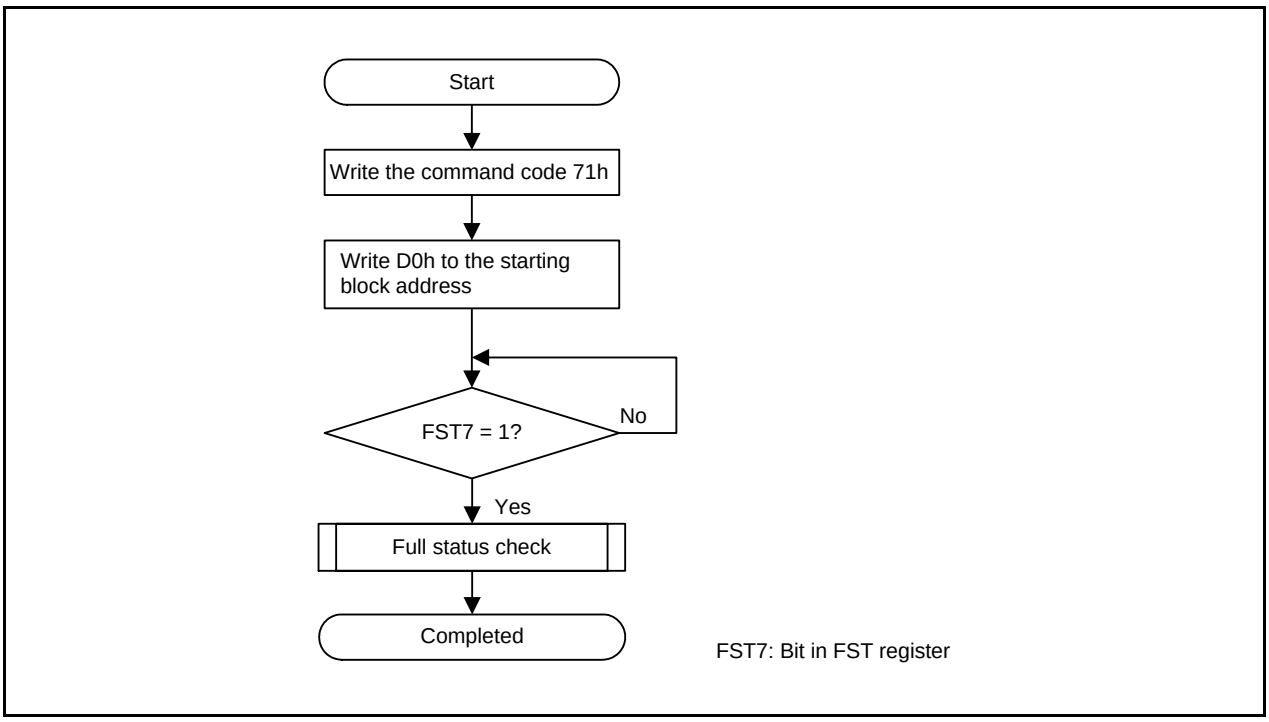


Figure 29.15 Read Lock Bit Status Flowchart

29.4.11.7 Block Blank Check Command

This command is used to confirm that all addresses in any block are blank data FFh.
When 25h is written in the first bus cycle and D0h is written in the second bus cycle to any block address, blank checking starts in the specified block. The FST7 bit in the FST register can be used to confirm whether blank checking has completed. The FST7 bit is set to 0 during the blank-check period and set to 1 when blank checking completes.
After blank checking has completed, the blank-check result can be confirmed by the FST5 bit in the FST register (refer to **29.4.12 Full Status Check**). This command is used to verify the target block has not been written to. To confirm whether erasure has completed normally, execute the full status check.

Do not execute the block blank check command when the FST6 bit is set to 1 (during erase-suspend).
Figure 29.16 shows a Block Blank Check Flowchart.

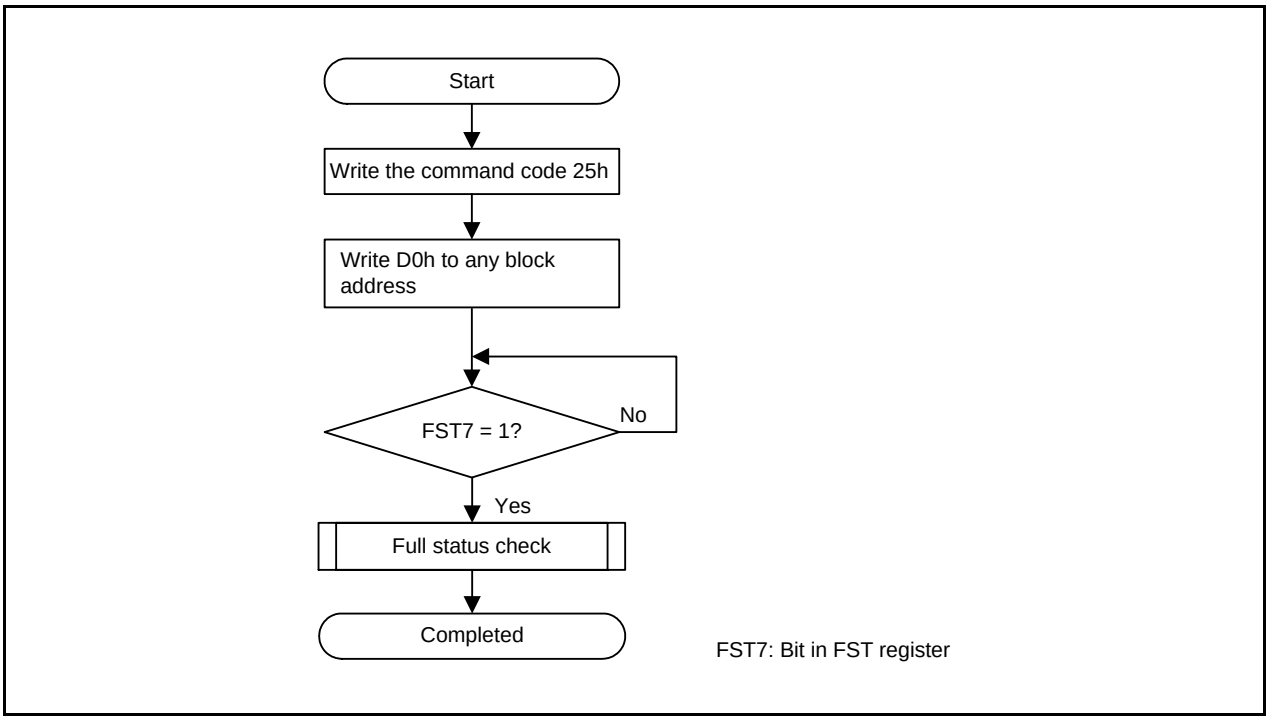


Figure 29.16 Block Blank Check Flowchart

This commanded is intended for programmer manufactures, not for general users.

29.4.12 Full Status Check

If an error occurs, bits FST4 and FST5 in the FST register are set to 1, indicating the occurrence of an error. The execution result can be confirmed by checking these status bits (full status check).
Table 29.6 lists the Errors and FST Register Status. Figure 29.17 shows the Full Status Check and Handling Procedure for Individual Errors.

Table 29.6 Errors and FST Register Status

FST Register Status		Error	Error Occurrence Condition
FST5	FST4		
1	1	Command sequence error	• When a command is not written correctly. • When data other than valid data (i.e., D0h or FFh) is written in the second bus cycle of the block erase command. (1) • The erase command is executed during suspend • The command is executed to the block during suspend
1	0	Erase error	When the block erase command is executed, but auto-erasure does not complete correctly.
		Blank check error	When the block blank check command is executed and data other than blank data FFh is read.
0	1	Program error	When the program command is executed, but auto-programming does not complete correctly.
		Lock bit program error	When the lock bit command is executed, but the lock bit is not set to 0(locked).

Note:
1. When FFh is written in the second bus cycle of these commands, the MCU enters read array mode. At the same time, the command code written in the first bus cycle is invalid.

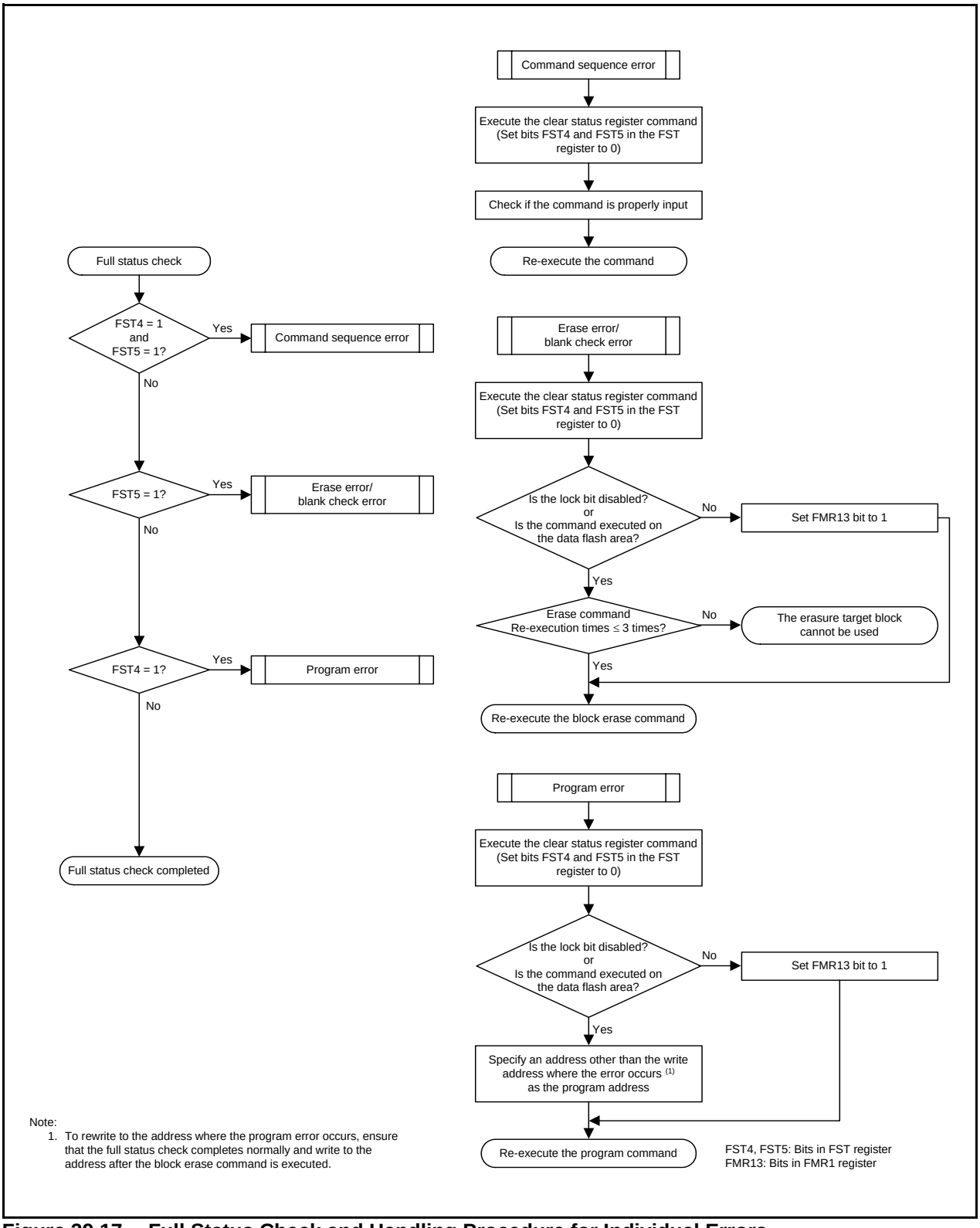


Figure 29.17 Full Status Check and Handling Procedure for Individual Errors

29.5 Standard Serial I/O Mode

In standard serial I/O mode, a serial programmer which supports the MCU can be used to rewrite the user ROM area while the MCU is mounted on-board.
There are three types of standard serial I/O modes:

- Standard serial I/O mode 1 ..... Clock synchronous serial I/O used to connect to a serial programmer
- Standard serial I/O mode 2 ..... Clock asynchronous serial I/O used to connect to a serial programmer
- Standard serial I/O mode 3 ..... Special clock asynchronous serial I/O used to connect to a serial programmer

Standard serial I/O mode 2 and standard serial I/O mode 3 can be used for the MCU.

Refer to **Appendix 2. Connection Examples between Serial Programmer and On-Chip Debugging Emulator** for examples of connecting to a serial programmer. Contact the serial programmer manufacturer for more information. Refer to the user's manual included with your serial programmer for instructions.

Table 29.7 lists the Pin Functions (Flash Memory Standard Serial I/O Mode 2) and Figure 29.18 shows Pin Handling in Standard Serial I/O Mode 2. Table 29.8 lists the Pin Functions (Flash Memory Standard Serial I/O Mode 3) and Figure 29.19 shows Pin Handling in Standard Serial I/O Mode 3.
After handling the pins shown in Table 29.8 and rewriting the flash memory using the programmer, apply a "H" level signal to the MODE pin and reset the hardware to run a program in the flash memory in single-chip mode.

29.5.1 ID Code Check Function

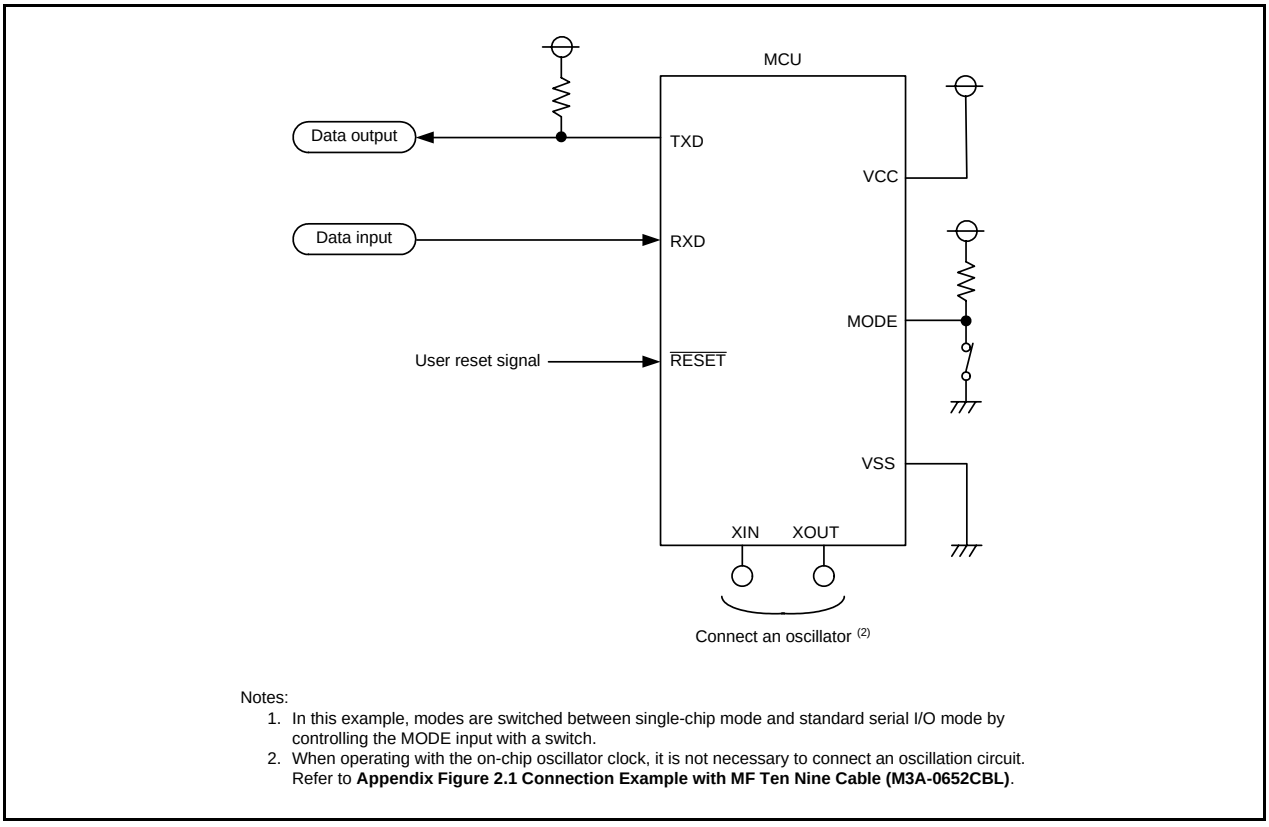
The ID code check function determines whether the ID codes sent from the serial programmer and those written in the flash memory match.
Refer to **12. ID Code Areas** for details of the ID code check.

Table 29.7 Pin Functions (Flash Memory Standard Serial I/O Mode 2)

Pin	Name	I/O	Description
VCC, VSS	Power supply input		Apply the guaranteed programming and erasure voltage to the VCC pin and 0 V to the VSS pin.
$\overline{\text{RESET}}$	Reset input	I	Reset input pin.
P4_6/XIN	P4_6 input/clock input	I	Connect a ceramic resonator or crystal oscillator between pins XIN and XOUT.
P4_7/XOUT	P4_7 input/clock output	I/O	
P0_0 to P0_4, P0_7	Input port P0	I	Input a “H” or “L” level signal or leave open.
P1_0 to P1_3, P1_6, P1_7	Input port P1	I	Input a “H” or “L” level signal or leave open.
P3_0, P3_3 to P3_5, P3_7	Input port P3	I	Input a “H” or “L” level signal or leave open.
P4_5	Input port P4	I	Input a “H” or “L” level signal or leave open.
P6_5 to P6_7	Input port P6	I	Input a “H” or “L” level signal or leave open.
P7_6, P7_7	Input port P7	I	Input a “H” or “L” level signal or leave open.
P8_1 to P8_3	Input port P8	I	Input a “H” or “L” level signal or leave open.
MODE	MODE	I/O	Input a “L” level signal.
P1_4	TXD output	O	Serial data I/O pin.
P1_5	RXD output	I	Serial data I/O pin.
USB_DP/USB_DM	D+ and D- I/O	I/O	D+ and D- I/O pins of the USB on-chip transceiver.
USB_VBUS	USB cable connection monitor	I	USB cable connection monitor pin.
USB_DPUPE	D+ signal pull-up resistor control	O	1.5-kΩ pull-up resistor control signal for USB D+ signal.
USB_VCC	USB power supply	I/O	USB power supply pin.
VREF (1)	Reference voltage input	I	Input a “H” level signal.
NC (2)	Non-Connection	I	Input a “H” level signal.

I: Input O: Output I/O: Input and output

Notes:
1. This pin is not available in the R8C/3MU Group.
2. This pin is not available in the R8C/3MK Group.



Notes:
1. In this example, modes are switched between single-chip mode and standard serial I/O mode by controlling the MODE input with a switch.
2. When operating with the on-chip oscillator clock, it is not necessary to connect an oscillation circuit. Refer to **Appendix Figure 2.1 Connection Example with MF Ten Nine Cable (M3A-0652CBL)**.

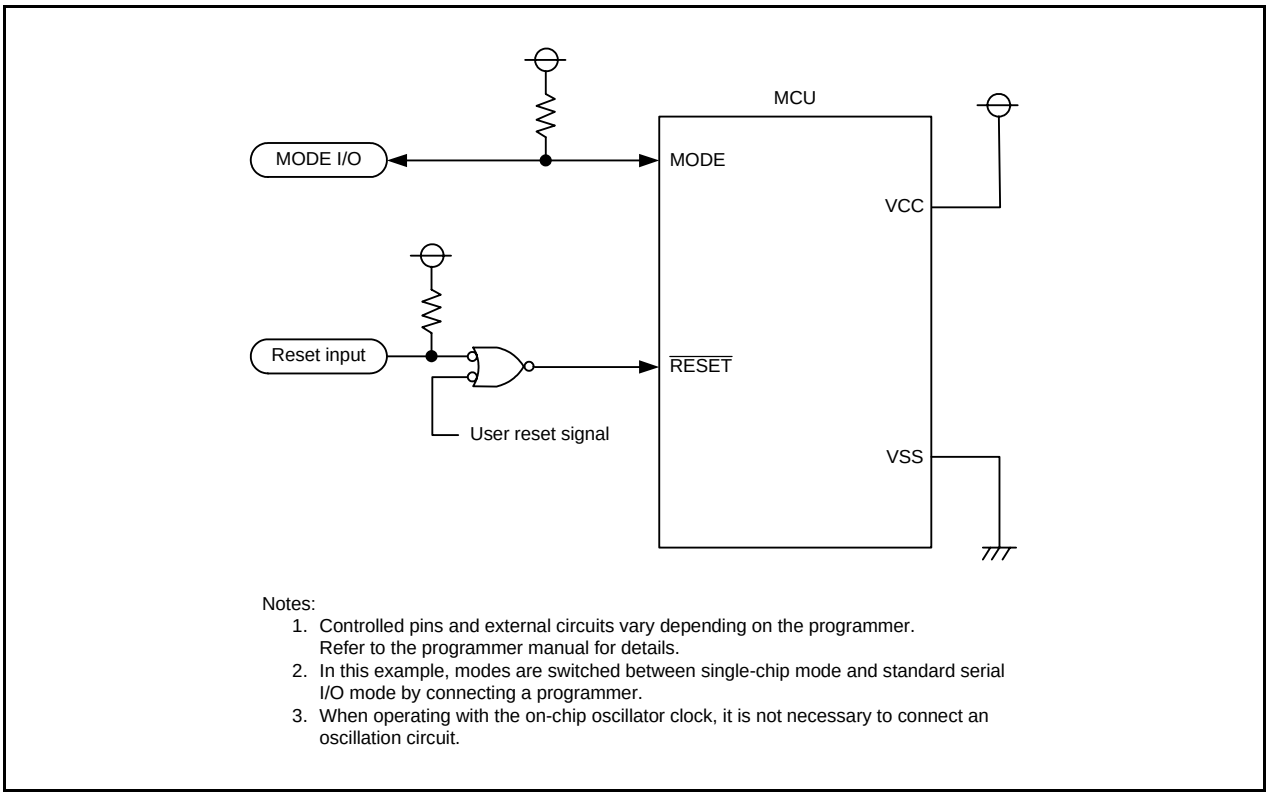
Figure 29.18 Pin Handling in Standard Serial I/O Mode 2

Table 29.8 Pin Functions (Flash Memory Standard Serial I/O Mode 3)

Pin	Name	I/O	Description
VCC, VSS	Power supply input		Apply the guaranteed programming and erasure voltage to the VCC pin and 0 V to the VSS pin.
$\overline{\text{RESET}}$	Reset input	I	Reset input pin.
P4_6/XIN	P4_6 input/clock input	I	If an external oscillator is connected, connect a ceramic resonator or crystal oscillator between pins XIN and XOUT. To use as an input port, input a “H” or “L” level signal or leave the pin open.
P4_7/XOUT	P4_7 input/clock output	I/O	
P0_0 to P0_4, P0_7	Input port P0	I	Input a “H” or “L” level signal or leave open.
P1_0 to P1_7	Input port P1	I	Input a “H” or “L” level signal or leave open.
P3_0, P3_3 to P3_5, P3_7	Input port P3	I	Input a “H” or “L” level signal or leave open.
P4_5	Input port P4	I	Input a “H” or “L” level signal or leave open.
P6_5 to P6_7	Input port P6	I	Input a “H” or “L” level signal or leave open.
P7_6, P7_7	Input port P7	I	Input a “H” or “L” level signal or leave open.
P8_1 to P8_3	Input port P8	I	Input a “H” or “L” level signal or leave open.
MODE	MODE	I/O	Serial data I/O pin. Connect the pin to a programmer.
USB_DP/USB_DM	D+ and D- I/O	I/O	D+ and D- I/O pins of the USB on-chip transceiver.
USB_VBUS	USB cable connection monitor	I	USB cable connection monitor pin.
USB_DPUPE	D+ signal pull-up resistor control	O	1.5-kΩ pull-up resistor control signal for USB D+ signal.
USB_VCC	USB power supply	I/O	USB power supply pin.
VREF (1)	Reference voltage input	I	Input a “H” level signal.
NC (2)	Non-Connection	I	Input a “H” level signal.

I: Input O: Output I/O: Input and output

Notes:
1. This pin is not available in the R8C/3MU Group.
2. This pin is not available in the R8C/3MK Group.



Notes:
1. Controlled pins and external circuits vary depending on the programmer. Refer to the programmer manual for details.
2. In this example, modes are switched between single-chip mode and standard serial I/O mode by connecting a programmer.
3. When operating with the on-chip oscillator clock, it is not necessary to connect an oscillation circuit.

Figure 29.19 Pin Handling in Standard Serial I/O Mode 3

29.6 Parallel I/O Mode

Parallel I/O mode is used to input and output software commands, addresses and data necessary to control (read, program, and erase) the on-chip flash memory.
Use a parallel programmer which supports the MCU. Contact the parallel programmer manufacturer for more information. Refer to the user's manual included with your parallel programmer for instructions.
In parallel I/O mode, the user ROM areas shown in Figures 29.1 and 29.2 can be rewritten.

29.6.1 ROM Code Protect Function

The ROM code protect function prevents the flash memory from being read and rewritten (refer to **29.3.2 ROM Code Protect Function**).

29.7 Notes on Flash Memory

29.7.1 CPU Rewrite Mode

29.7.1.1 Prohibited Instructions

The following instructions cannot be used while the program ROM area is being rewritten in EW0 mode because they reference data in the flash memory: UND, INTO, and BRK.

29.7.1.2 Interrupts

Tables 29.9 to 29.11 show CPU Rewrite Mode Interrupts.

Table 29.9 CPU Rewrite Mode Interrupts (1)

Mode	Erase/ Write Target	Status	Maskable Interrupt
EW0	Data flash	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, interrupt handling is executed. If the FMR22 bit is set to 1 (erase-suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (erase-suspend request). The flash memory suspends auto-erasure after td(SR-SUS). If erase-suspend is required while the FMR22 bit is set to 0 (erase-suspend request disabled by interrupt request), set the FMR21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. Auto-erasure can be restarted by setting the FMR21 bit to 0 (erase restart).
		During auto-erasure (suspend disabled or FMR22 = 0)	Interrupt handling is executed while auto-erasure or auto-programming is being performed.
		During auto-programming	
	Program ROM	During auto-erasure (suspend enabled)	Usable by allocating a vector in RAM.
		During auto-erasure (suspend disabled)	
		During auto-programming	
EW1	Data flash	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, interrupt handling is executed. If the FMR22 bit is set to 1, the FMR21 bit is automatically set to 1. The flash memory suspends auto-erasure after td(SR-SUS). If erase-suspend is required while the FMR22 bit is set to 0, set the FMR21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. Auto-erasure can be restarted by setting the FMR21 bit to 0.
		During auto-erasure (suspend disabled or FMR22 = 0)	Interrupt handling is executed while auto-erasure or auto-programming is being performed.
		During auto-programming	
	Program ROM	During auto-erasure (suspend enabled)	Auto-erasure suspends after td(SR-SUS) and interrupt handling is executed. Auto-erasure can be restarted by setting the FMR21 bit to 0 after interrupt handling completes. While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written.
		During auto-erasure (suspend disabled or FMR22 = 0)	Auto-erasure and auto-programming have priority and interrupt requests are put on standby. Interrupt handling is executed after auto-erase and auto-program complete.
		During auto-programming	

FMR21, FMR22: Bits in FMR2 register

Table 29.10 CPU Rewrite Mode Interrupts (2)

Mode	Erase/ Write Target	Status	• Watchdog Timer • Oscillation Stop Detection • Voltage Monitor 2 • Voltage Monitor 1	• Undefined Instruction • INTO Instruction • BRK Instruction • Single Step • Address Match • Address Break (Note 1)
EW0	Data flash	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, interrupt handling is executed. If the FMR22 bit is set to 1 (erase-suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (erase-suspend request). The flash memory suspends auto-erasure after td(SR-SUS). If erase-suspend is required while the FMR22 bit is set to 0 (erase-suspend request disabled by interrupt request), set the FMR21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. Auto-erasure can be restarted by setting the FMR21 bit is set to 0 (erase restart).	When an interrupt request is acknowledged, interrupt handling is executed. If erase-suspend is required, set the FMR21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. Auto-erasure can be restarted by setting the FMR21 bit in the FMR2 register is set to 0 (erase restart).
		During auto-erasure (suspend disabled or FMR22 = 0)	Interrupt handling is executed while auto-erasure or auto-programming is being performed.	
		During auto-programming		
	Program ROM	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, auto-erasure or auto-programming is forcibly stopped immediately and the flash memory is reset. Interrupt handling starts when the flash memory restarts after the fixed period. Since the block during auto-erasure or the address during auto-programming is forcibly stopped, the normal value may not be read. After the flash memory restarts, execute auto-erasure again and ensure it completes normally. The watchdog timer does not stop during the command operation, so interrupt requests may be generated. Initialize the watchdog timer regularly using the erase-suspend function.	Not usable during auto-erasure or auto-programming.
		During auto-erasure (suspend disabled)		
		During auto-programming		

FMR21, FMR22: Bits in FMR2 register

Note:

1. Do not use a non-maskable interrupt while block 0 is being auto-erased because the fixed vector is allocated in block 0.

Table 29.11 CPU Rewrite Mode Interrupts (3)

Mode	Erase/ Write Target	Status	• Watchdog Timer • Oscillation Stop Detection • Voltage Monitor 2 • Voltage Monitor 1	• Undefined Instruction • INTO Instruction • BRK Instruction • Single Step • Address Match • Address Break (Note 1)
EW1	Data flash	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, interrupt handling is executed. If the FMR22 bit is set to 1 (erase-suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (erase-suspend request). The flash memory suspends auto-erasure after td(SR-SUS). If erase-suspend is required while the FMR22 bit is set to 0 (erase-suspend request disabled by interrupt request), set the FMR21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. Auto-erasure can be restarted by setting the FMR21 bit is set to 0 (erase restart).	When an interrupt request is acknowledged, interrupt handling is executed. If erase-suspend is required, set the FMR21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. Auto-erasure can be restarted by setting the FMR21 bit in the FMR2 register is set to 0 (erase restart).
		During auto-erasure (suspend disabled or FMR22 = 0)	Interrupt handling is executed while auto-erasure or auto-programming is being performed.	
		During auto-programming		
	Program ROM	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, auto-erasure or auto-programming is forcibly stopped immediately and the flash memory is reset. Interrupt handling starts when the flash memory restarts after the fixed period. Since the block during auto-erasure or the address during auto-programming is forcibly stopped, the normal value may not be read. After the flash memory restarts, execute auto-erasure again and ensure it completes normally. The watchdog timer does not stop during the command operation, so interrupt requests may be generated. Initialize the watchdog timer regularly using the erase-suspend function.	Not usable during auto-erasure or auto-programming.
		During auto-erasure (suspend disabled or FMR22 = 0)		
		During auto-programming		

FMR21, FMR22: Bits in FMR2 register

Note:

1. Do not use a non-maskable interrupt while block 0 is being auto-erased because the fixed vector is allocated in block 0.

29.7.1.3 How to Access

To set one of the following bits to 1, first write 0 and then 1 immediately. Disable interrupts and DTC activation between writing 0 and writing 1.
- The FMR01 bit or FMR02 bit in the FMR0 register
- The FMR13 bit in the FMR1 register
- The FMR20 bit, FMR22 bit, or FMR 27 bit in the FMR2 register

To set one of the following bits to 0, first write 1 and then 0 immediately. Disable interrupts and DTC activation between writing 1 and writing 0.
- The FMR14 bit, FMR15 bit, FMR16 bit, or FMR17 bit in the FMR1 register

29.7.1.4 Rewriting User ROM Area

In EW0 mode, if the supply voltage drops while rewriting any block in which a rewrite control program is stored, it may not be possible to rewrite the flash memory because the rewrite control program cannot be rewritten correctly. In this case, use standard serial I/O mode.

29.7.1.5 Programming

Do not write additions to the already programmed address.

29.7.1.6 Entering Stop Mode or Wait Mode

Do not enter stop mode or wait mode during erase-suspend.
If the FST7 bit in the FST register is set to 0 (busy (during programming or erasure execution), do not enter to stop mode or wait mode.
Do not enter stop mode or wait mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

29.7.1.7 Programming and Erasure Voltage for Flash Memory

To perform programming and erasure, use VCC = 2.7 to 5.5 V as the supply voltage. Do not perform programming and erasure at less than 2.7 V.

29.7.1.8 Block Blank Check

Do not execute the block blank check command during erase-suspend.

29.7.1.9 Low-Current-Consumption Read Mode

In low-speed on-chip oscillator mode, the current consumption when reading the flash memory can be reduced by setting the FMR27 bit in the FMR2 register to 1 (low-current-consumption read mode enabled).
Low-current-consumption read mode can be used when the CPU clock is set to either of the following:
- The CPU clock is set to the low-speed on-chip oscillator clock divided by 4, 8, or 16.

However, do not use low-current-consumption read mode when the frequency of the selected CPU clock is 3 kHz or below. After setting the divide ratio of the CPU clock, set the FMR27 bit to 1 (low-current-consumption read mode enabled).
To reduce the power consumption, refer to **30. Reducing Power Consumption**.
Enter wait mode or stop mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled).
Do not enter wait mode or stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

30. Reducing Power Consumption

30.1 Overview

This chapter describes key points and processing methods for reducing power consumption.

30.2 Key Points and Processing Methods for Reducing Power Consumption

Key points for reducing power consumption are shown below. They should be referred to when designing a system or creating a program.

30.2.1 Voltage Detection Circuit

If voltage monitor 1 is not used, set the VCA26 bit in the VCA2 register to 0 (voltage detection 1 circuit disabled). If voltage monitor 2 is not used, set the VCA27 bit in the VCA2 register to 0 (voltage detection 2 circuit disabled).
If the power-on reset and voltage monitor 0 reset are not used, set the VCA25 bit in the VCA2 register to 0 (voltage detection 0 circuit disabled).

30.2.2 Ports

Even after the MCU enters wait mode or stop mode, the states of the I/O ports are retained. Current flows into the output ports in the active state, and shoot-through current flows into the input ports in the high-impedance state. Unnecessary ports should be set to input and fixed to a stable electric potential before the MCU enters wait mode or stop mode.

30.2.3 Clocks

Power consumption generally depends on the number of the operating clocks and their frequencies. The fewer the number of operating clocks or the lower their frequencies, the more power consumption decreases.
Unnecessary clocks should be stopped accordingly.

Stopping low-speed on-chip oscillator oscillation:	Set the CM14 bit in the CM1 register to 1 (low-speed on-chip oscillator off) and the OCD2 bit in the OCD register to 0 (XIN clock selected).
Stopping high-speed on-chip oscillator oscillation:	Set the FRA00 bit in the FRA0 register to 0.

30.2.4 Wait Mode, Stop Mode

Power consumption can be reduced in wait mode and stop mode. Refer to **9.7 Power Control** for details.

30.2.5 Stopping Peripheral Function Clocks

If the peripheral function f1, f2, f4, f8, and f32 clocks are not necessary in wait mode, set the CM02 bit in the CM0 register to 1 (peripheral function clock stops in wait mode). This will stop the f1, f2, f4, f8, and f32 clocks in wait mode.

30.2.6 Timers

If timer RA is not used, set the TCKCUT bit in the TRAMR register to 1 (count source cutoff).
If timer RB is not used, set the TCKCUT bit in the TRBMR register to 1 (count source cutoff).
If timer RC is not used, set the MSTTRC bit in the MSTCR register to 1 (standby).

30.2.7 Clock Synchronous Serial Interface

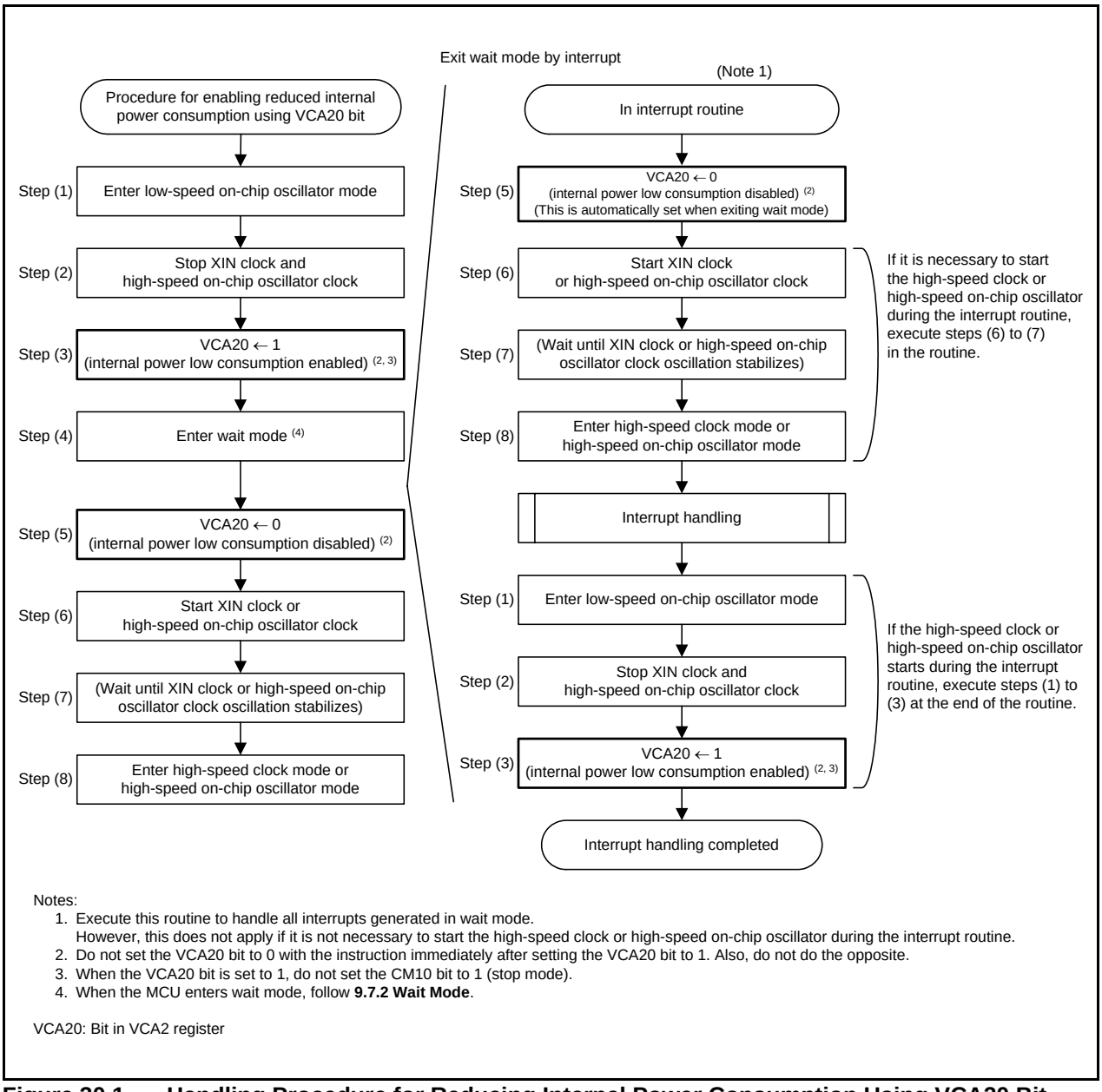
When the SSU or the I2C bus is not used, set the MSTIIC bit in the MSTCR register to 1 (standby).

30.2.8 A/D Converter

When the A/D converter is not used, power consumption can be reduced by setting the ADSTBY bit in the ADCON1 register to 0 (A/D operation stops (standby)) to shut off any analog circuit current flow.
Note: Not available in the R8C/3MU Group.

30.2.9 Reducing Internal Power Consumption

When the MCU enters wait mode using low-speed on-chip oscillator mode, internal power consumption can be reduced by using the VCA20 bit in the VCA2 register. Figure 30.1 shows the Handling Procedure for Reducing Internal Power Consumption Using VCA20 Bit. To enable reduced internal power consumption by the VCA20 bit, follow Figure 30.1 Handling Procedure for Reducing Internal Power Consumption Using VCA20 Bit.



Notes:
1. Execute this routine to handle all interrupts generated in wait mode.
   However, this does not apply if it is not necessary to start the high-speed clock or high-speed on-chip oscillator during the interrupt routine.
2. Do not set the VCA20 bit to 0 with the instruction immediately after setting the VCA20 bit to 1. Also, do not do the opposite.
3. When the VCA20 bit is set to 1, do not set the CM10 bit to 1 (stop mode).
4. When the MCU enters wait mode, follow **9.7.2 Wait Mode**.

VCA20: Bit in VCA2 register

Figure 30.1 Handling Procedure for Reducing Internal Power Consumption Using VCA20 Bit

30.2.10 Stopping Flash Memory

In low-speed on-chip oscillator mode, power consumption can be further reduced by stopping the flash memory using the FMSTP bit in the FMR0 register.

Access to the flash memory is disabled by setting the FMSTP bit to 1 (flash memory stops). The FMSTP bit must be written to by a program transferred to RAM.

When the MCU enters stop mode or wait mode while CPU rewrite mode is disabled, the power for the flash memory is automatically turned off. It is turned back on again after the MCU exits stop mode or wait mode. This eliminates the need to set the FMR0 register.

Figure 30.2 shows the Handling Procedure Example for Reducing Power Consumption Using FMSTP Bit.

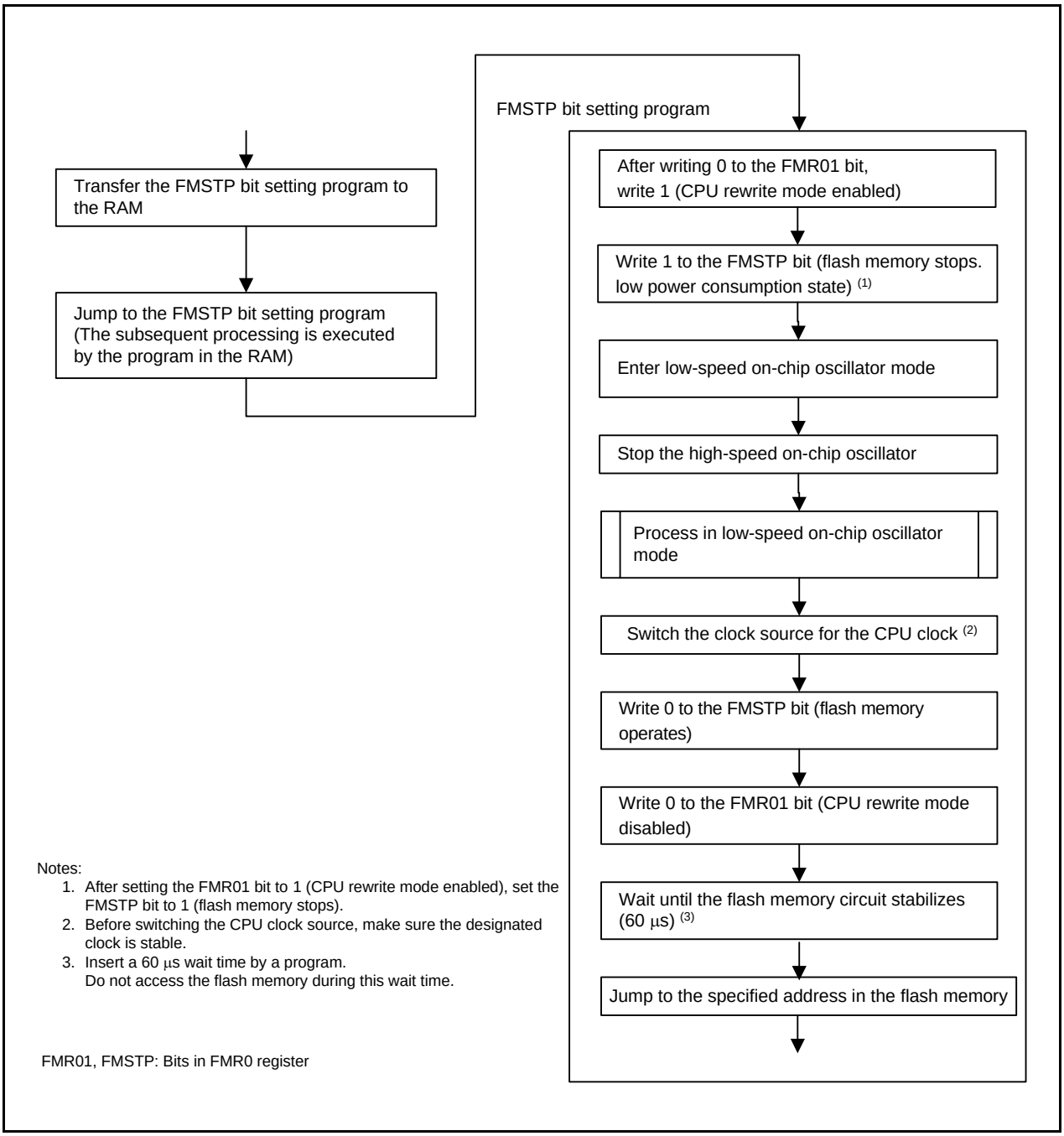


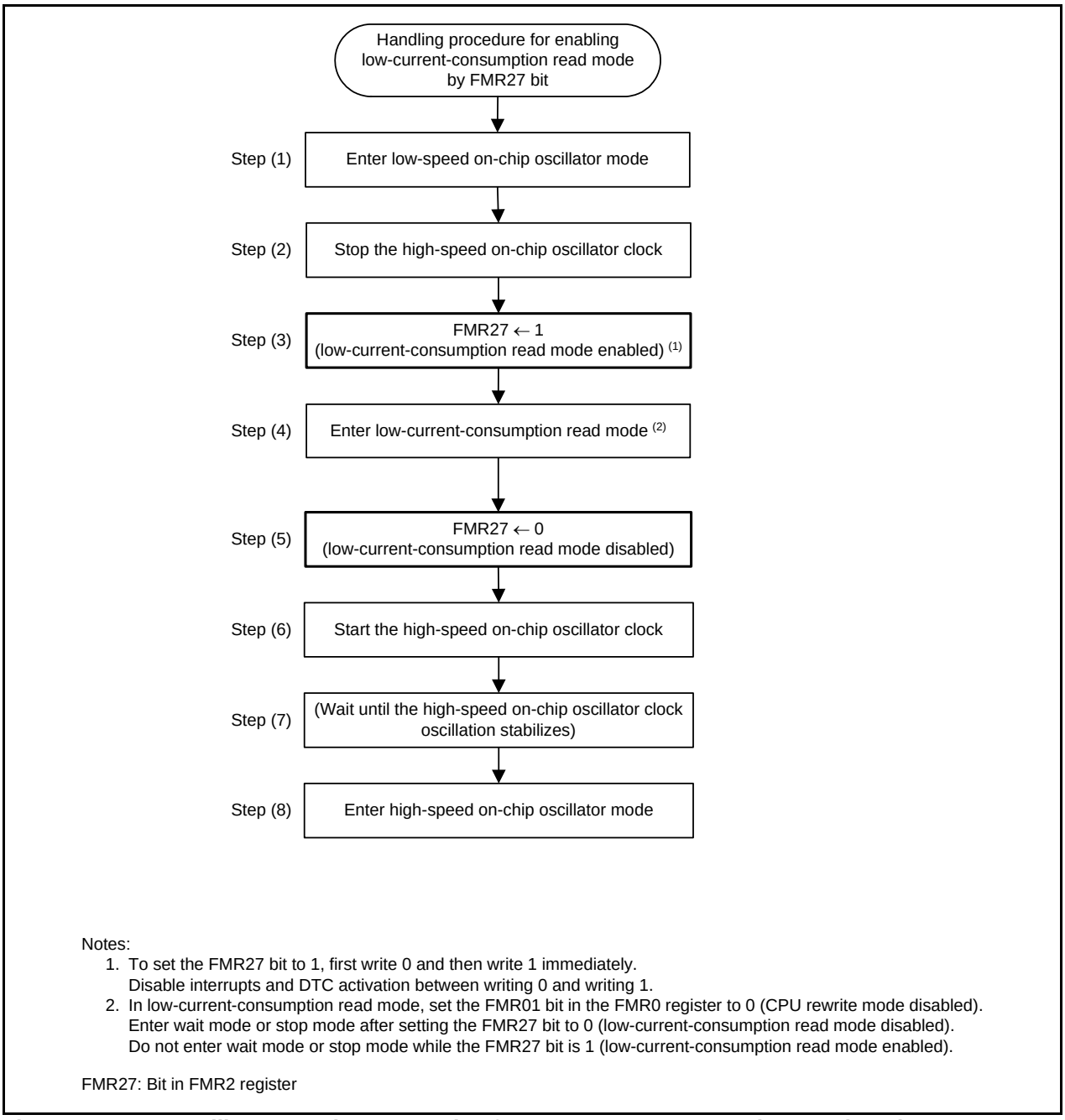
Figure 30.2 Handling Procedure Example for Reducing Power Consumption Using FMSTP Bit

30.2.11 Low-Current-Consumption Read Mode

In low-speed on-chip oscillator mode, the current consumption when reading the flash memory can be reduced by setting the FMR27 bit in the FMR2 register to 1 (low-current-consumption read mode enabled).
Low-current-consumption read mode can be used when the CPU clock is set to either of the following:

- The CPU clock is set to the low-speed on-chip oscillator clock divided by 4, 8, or 16.

However, do not use low-current-consumption read mode when the frequency of the selected CPU clock is 3 kHz or below.
After setting the divide ratio of the CPU clock, set the FMR27 bit to 1 (low-current-consumption read mode enabled).
Enter wait mode or stop mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled).
Do not enter wait mode or stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).
Figure 30.3 shows the Handling Procedure Example of Low-Current-Consumption Read Mode.



Notes:
1. To set the FMR27 bit to 1, first write 0 and then write 1 immediately.
   Disable interrupts and DTC activation between writing 0 and writing 1.
2. In low-current-consumption read mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled).
   Enter wait mode or stop mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled).
   Do not enter wait mode or stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

FMR27: Bit in FMR2 register

Figure 30.3 Handling Procedure Example of Low-Current-Consumption Read Mode

31. Electrical Characteristics

31.1 R8C/3MU Group

Table 31.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated Value	Unit
V_{CC}	Supply voltage		–0.3 to 6.5	V
V_I	Input voltage		–0.3 to V_{CC} + 0.3	V
V_O	Output voltage		–0.3 to V_{CC} + 0.3	V
P_d	Power dissipation	$-20°C \leq T_{opr} \leq 85°C$	500	mW
T_{opr}	Operating ambient temperature		–20 to 85 (N version)	°C
T_{stg}	Storage temperature		–65 to 150	°C

Table 31.2 Recommended Operating Conditions (1)

Symbol	Parameter				Conditions	Standard			Unit
						Min.	Typ.	Max.	
V_{CC}	Supply voltage	When USB function is used				3.0	5.0	5.5	V
		When USB function is not used				1.8	5.0	5.5	V
UV_{CC}	USB Supply Voltage (When UVCC pin is input)	When USB function is used			V_{CC} = 3.0 to 3.6 V	—	V_{CC} (4)	—	V
		When USB function is not used			V_{CC} = 1.8 to 5.5 V	—	V_{CC} (4)	—	V
V_{SS}	Supply voltage					—	0	—	V
V_{IH}	Input “H” voltage	Other than CMOS input				0.8 V_{CC}	—	V_{CC}	V
		CMOS input	Input level switching function (I/O port)	Input level selection: 0.35 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0.5 V_{CC}	—	V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0.55 V_{CC}	—	V_{CC}	V
					1.8 V ≤ V_{CC} < 2.7 V	0.65 V_{CC}	—	V_{CC}	V
				Input level selection: 0.5 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0.65 V_{CC}	—	V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0.7 V_{CC}	—	V_{CC}	V
					1.8 V ≤ V_{CC} < 2.7 V	0.8 V_{CC}	—	V_{CC}	V
				Input level selection: 0.7 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0.85 V_{CC}	—	V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0.85 V_{CC}	—	V_{CC}	V
					1.8 V ≤ V_{CC} < 2.7 V	0.85 V_{CC}	—	V_{CC}	V
		External clock input (XOUT)				1.2	—	V_{CC}	V
V_{IL}	Input “L” voltage	Other than CMOS input				0	—	0.2 V_{CC}	V
		CMOS input	Input level switching function (I/O port)	Input level selection: 0.35 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0	—	0.2 V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0	—	0.2 V_{CC}	V
					1.8 V ≤ V_{CC} < 2.7 V	0	—	0.2 V_{CC}	V
				Input level selection: 0.5 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0	—	0.4 V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0	—	0.3 V_{CC}	V
					1.8 V ≤ V_{CC} < 2.7 V	0	—	0.2 V_{CC}	V
				Input level selection: 0.7 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0	—	0.55 V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0	—	0.45 V_{CC}	V
					1.8 V ≤ V_{CC} < 2.7 V	0	—	0.35 V_{CC}	V
		External clock input (XOUT)				0	—	0.4	V
$I_{OH(sum)}$	Peak sum output “H” current		Sum of all pins $I_{OH(peak)}$			—	—	−160	mA
$I_{OH(sum)}$	Average sum output “H” current		Sum of all pins $I_{OH(avg)}$			—	—	−80	mA
$I_{OH(peak)}$	Peak output “H” current		Drive capacity Low			—	—	−10	mA
			Drive capacity High			—	—	−40	mA
$I_{OH(avg)}$	Average output “H” current		Drive capacity Low			—	—	−5	mA
			Drive capacity High			—	—	−20	mA
$I_{OL(sum)}$	Peak sum output “L” current		Sum of all pins $I_{OL(peak)}$			—	—	160	mA
$I_{OL(sum)}$	Average sum output “L” current		Sum of all pins $I_{OL(avg)}$			—	—	80	mA
$I_{OL(peak)}$	Peak output “L” current		Drive capacity Low			—	—	10	mA
			Drive capacity High			—	—	40	mA
$I_{OL(avg)}$	Average output “L” current		Drive capacity Low			—	—	5	mA
			Drive capacity High			—	—	20	mA
$f_{(XIN)}$	XIN clock input oscillation frequency				2.7 V ≤ V_{CC} ≤ 5.5 V	—	—	20	MHz
					1.8 V ≤ V_{CC} < 2.7 V	—	—	5	MHz
fOCO40M	When used as the count source for timer RC (3)				2.7 V ≤ V_{CC} ≤ 5.5 V	32	—	40	MHz
fOCO-F	fOCO-F frequency				2.7 V ≤ V_{CC} ≤ 5.5 V	—	—	20	MHz
					1.8 V ≤ V_{CC} < 2.7 V	—	—	5	MHz
—	System clock frequency				2.7 V ≤ V_{CC} ≤ 5.5 V	—	—	20	MHz
					1.8 V ≤ V_{CC} < 2.7 V	—	—	5	MHz
$f_{(BCLK)}$	CPU clock frequency				2.7 V ≤ V_{CC} ≤ 5.5 V	—	—	20	MHz
					1.8 V ≤ V_{CC} < 2.7 V	—	—	5	MHz
$t_{su(PLL)}$	PLL frequency symthesizer stabilization wait time				4.0 V ≤ V_{CC} ≤ 5.5 V	—	—	2	ms
					2.7 V ≤ V_{CC} < 4.0 V	—	—	3	ms

Notes:
1. V_{CC} = 1.8 to 5.5 V and T_{opr} = −20 to 85 °C (N version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.
3. fOCO40M can be used as the count source for timer RC in the range of V_{CC} = 2.7 to 5.5 V.
4. Connect V_{CC} for the UV_{CC} pin input.

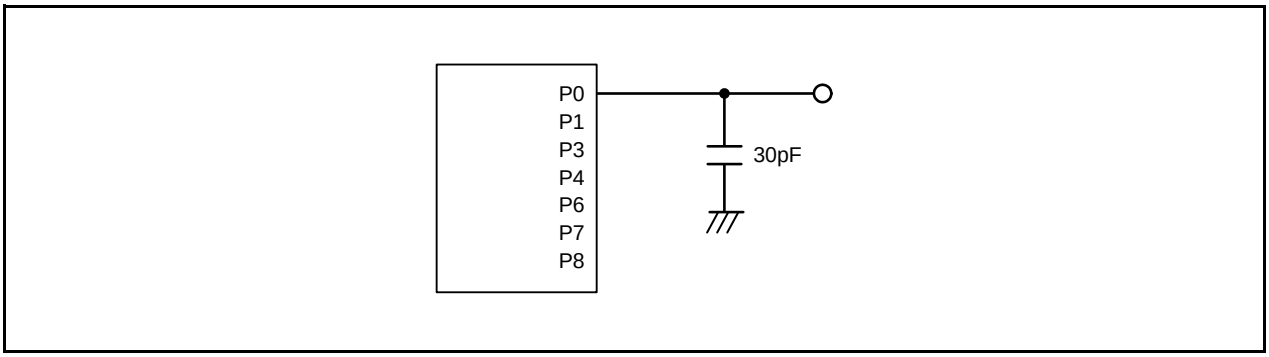


Figure 31.1 Ports P0, P1, P3, P4, P6, P7 and P8 Timing Measurement Circuit

Table 31.3 Comparator B Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{ref}	IVREF1, IVREF3 input reference voltage		0	—	V_{CC} – 1.4	V
V_I	IVCMP1, IVCMP3 input voltage		–0.3	—	V_{CC} + 0.3	V
—	Offset		—	5	100	mV
t_d	Comparator output delay time (2)	$V_I = V_{ref} \pm 100$ mV	—	0.1	—	µs
I_{CMP}	Comparator operating current	V_{CC} = 5.0 V	—	17.5	—	µA

Notes:
1. V_{CC} = 2.7 to 5.5 V and T_{opr} = –20 to 85 °C (N version), unless otherwise specified.
2. When the digital filter is disabled.

Table 31.4 USB Characteristics

Symbol	Parameter		Condition	Standard			Unit
				Min.	Typ.	Max.	
V_{IH}	Input characteristics	Input “H” voltage	Figures 31.2 and 31.3	2.0	—	—	V
V_{IL}		Input “L” voltage		—	—	0.8	V
V_{DI}		Differential input sensitivity		0.2	—	—	V
V_{CM}		Differential common mode range		0.8	—	2.5	V
V_{OH}	Output characteristics	Output “H” voltage	Figures 31.2 and 31.3 I_{CH} = 200µA	2.8	—	—	V
V_{OL}		Output “L” voltage	Figures 31.2 and 31.3 I_{CL} = 2 mA	—	—	0.3	V
V_{CRS}		Crossover voltage	Figures 31.2 and 31.3	1.3	—	2.0	V
t_R		Rise time	Figures 31.2 and 31.3	4.0	—	20.0	ns
t_F		Fall time	Figures 31.2 and 31.3	4.0	—	20.0	ns
t_{RFM}		Rise time / Fall time matching	Figures 31.2 and 31.3 (tR/tF)	90.0	—	111.1	%
Z_{DRV}		Output resistance	Figures 31.2 and 31.3 Includes R_S = 27Ω	28	—	44.0	Ω
UVCC	UVCC output voltage		V_{CC} = 4.0 to 5.5V, PXXCON = VDDUSBE = 1	3.0	3.3	3.6	V
			PXXCON = 0	—	V_{CC}	—	V
I_{susp}	Consumption current of the Internal power supply for USB		V_{CC} = 4.0 to 5.5 V UV_{CC} - V_{SS} 0.33 µF V_{CC} - V_{SS} 0.1 µF		50		µA

Note:
1. Referenced to V_{CC} = 3.0 to 5.5 V, UV_{CC} = 3.0 V, at T_{opr} = -20 to 85 °C (N version), unless otherwise specified.

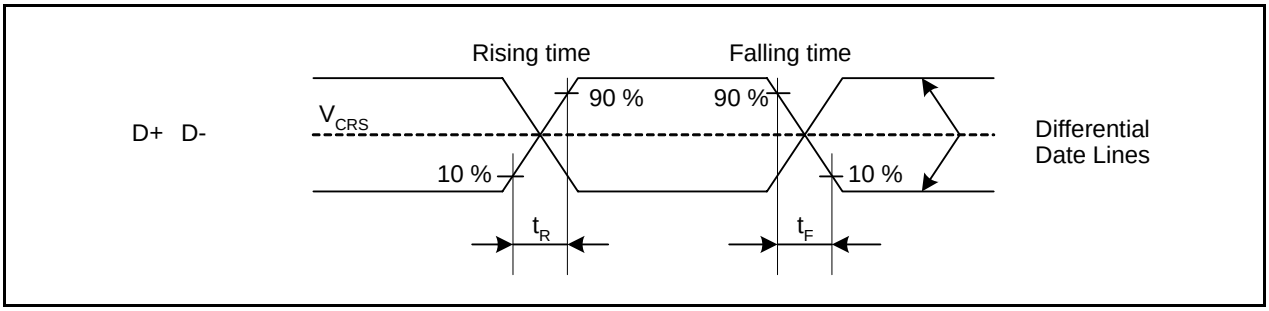


Figure 31.2 Data Signal Timing Diagram

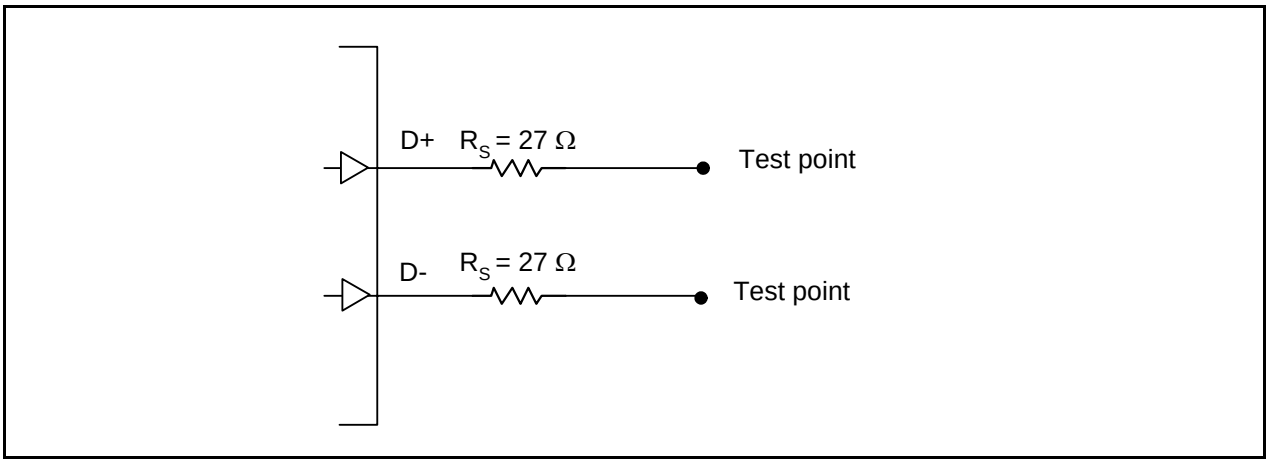


Figure 31.3 Load Condition

Table 31.5 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance (2)		1,000 (3)	—	—	times
—	Byte program time		—	80	500	µs
—	Block erase time		—	0.3	—	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		—	—	5 + CPU clock × 3 cycles	ms
—	Interval from erase start/restart until following suspend request		0	—	—	µs
—	Time from suspend until erase restart		—	—	30 + CPU clock × 1 cycle	µs
$t_{d(CMDRST-READY)}$	Time from when command is forcibly stopped until reading is enabled		–	–	30 + CPU clock × 1 cycle	µs
—	Program, erase voltage		2.7	—	5.5	V
—	Read voltage		1.8	—	5.5	V
—	Program, erase temperature		0	—	60	°C
—	Data hold time (7)	Ambient temperature = 55 °C	20	—	—	year

Notes:
1. V_{CC} = 2.7 to 5.5 V and T_{opr} = 0 to 60 °C, unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed.)
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 31.6 Flash Memory (Data flash Block A to Block D) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance (2)		10,000 (3)	—	—	times
—	Byte program time (program/erase endurance ≤ 1,000 times)		—	160	1500	µs
—	Byte program time (program/erase endurance > 1,000 times)		—	300	1500	µs
—	Block erase time (program/erase endurance ≤ 1,000 times)		—	0.2	1	s
—	Block erase time (program/erase endurance > 1,000 times)		—	0.3	1	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		—	—	5 + CPU clock × 3 cycles	ms
—	Interval from erase start/restart until following suspend request		0	—	—	µs
—	Time from suspend until erase restart		—	—	30 + CPU clock × 1 cycle	µs
$t_{d(CMDRST-READY)}$	Time from when command is forcibly stopped until reading is enabled		–	–	30 + CPU clock × 1 cycle	µs
—	Program, erase voltage		2.7	—	5.5	V
—	Read voltage		1.8	—	5.5	V
—	Program, erase temperature		–20	—	85	°C
—	Data hold time (7)	Ambient temperature = 55 °C	20	—	—	year

Notes:
1. V_{CC} = 2.7 to 5.5 V and T_{opr} = –20 to 85 °C (N version), unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed.)
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A to D can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

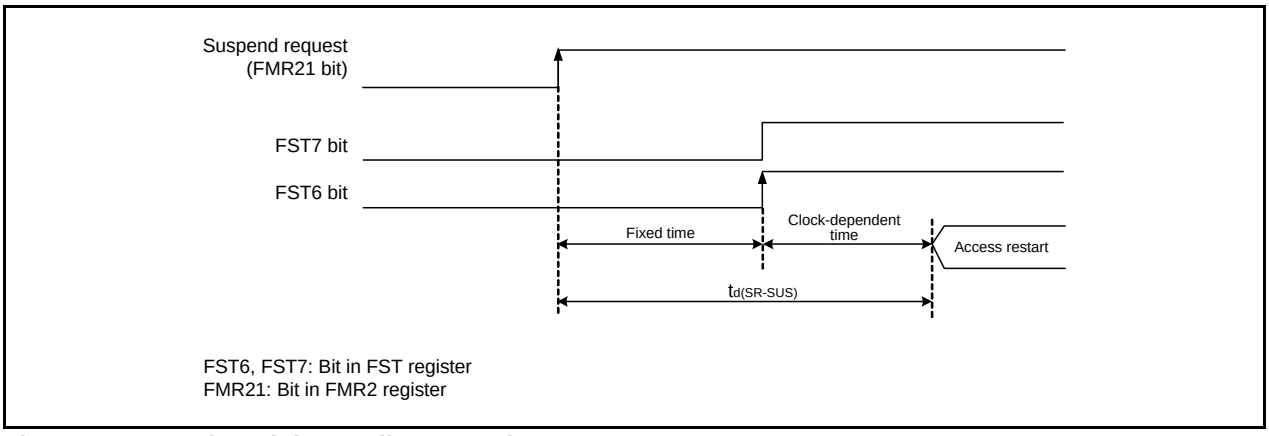


Figure 31.4 Time delay until Suspend

Table 31.7 Voltage Detection 0 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det0}	Voltage detection level Vdet0_0 (2)		1.80	1.90	2.05	V
	Voltage detection level Vdet0_1 (2)		2.15	2.35	2.50	V
	Voltage detection level Vdet0_2 (2)		2.70	2.85	3.05	V
	Voltage detection level Vdet0_3 (2)		3.55	3.80	4.05	V
—	Voltage detection 0 circuit response time (4)	At the falling of V_{CC} from 5.0 V to (Vdet0_0 – 0.1) V	—	6	150	µs
—	Voltage detection circuit self power consumption	VCA25 = 1, V_{CC} = 5.0 V	—	1.5	—	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (3)		—	—	100	µs

Notes:
1. The measurement condition is V_{CC} = 1.8 to 5.5 V and T_{opr} = –20 to 85 °C (N version).
2. Select the voltage detection level with bits VDSEL0 and VDSEL1 in the OFS register.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.
4. Time until the voltage monitor 0 reset is generated after the voltage passes V_{det0}.

Table 31.8 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det1}	Voltage detection level Vdet1_0 (2)	At the falling of V_{CC}	2.00	2.20	2.40	V
	Voltage detection level Vdet1_1 (2)	At the falling of V_{CC}	2.15	2.35	2.55	V
	Voltage detection level Vdet1_2 (2)	At the falling of V_{CC}	2.30	2.50	2.70	V
	Voltage detection level Vdet1_3 (2)	At the falling of V_{CC}	2.45	2.65	2.85	V
	Voltage detection level Vdet1_4 (2)	At the falling of V_{CC}	2.60	2.80	3.00	V
	Voltage detection level Vdet1_5 (2)	At the falling of V_{CC}	2.75	2.95	3.15	V
	Voltage detection level Vdet1_6 (2)	At the falling of V_{CC}	2.85	3.10	3.40	V
	Voltage detection level Vdet1_7 (2)	At the falling of V_{CC}	3.00	3.25	3.55	V
	Voltage detection level Vdet1_8 (2)	At the falling of V_{CC}	3.15	3.40	3.70	V
	Voltage detection level Vdet1_9 (2)	At the falling of V_{CC}	3.30	3.55	3.85	V
	Voltage detection level Vdet1_A (2)	At the falling of V_{CC}	3.45	3.70	4.00	V
	Voltage detection level Vdet1_B (2)	At the falling of V_{CC}	3.60	3.85	4.15	V
	Voltage detection level Vdet1_C (2)	At the falling of V_{CC}	3.75	4.00	4.30	V
	Voltage detection level Vdet1_D (2)	At the falling of V_{CC}	3.90	4.15	4.45	V
	Voltage detection level Vdet1_E (2)	At the falling of V_{CC}	4.05	4.30	4.60	V
	Voltage detection level Vdet1_F (2)	At the falling of V_{CC}	4.20	4.45	4.75	V
—	Hysteresis width at the rising of V_{CC} in voltage detection 1 circuit	Vdet1_0 to Vdet1_5 selected	—	0.07	—	V
		Vdet1_6 to Vdet1_F selected	—	0.10	—	V
—	Voltage detection 1 circuit response time (3)	At the falling of V_{CC} from 5.0 V to (Vdet1_0 – 0.1) V	—	60	150	µs
—	Voltage detection circuit self power consumption	VCA26 = 1, V_{CC} = 5.0 V	—	1.7	—	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (4)		—	—	100	µs

Notes:
1. The measurement condition is V_{CC} = 1.8 to 5.5 V and T_{opr} = –20 to 85 °C (N version).
2. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
3. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V_{det1}.
4. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

Table 31.9 Voltage Detection 2 Circuit Electrical Characteristics

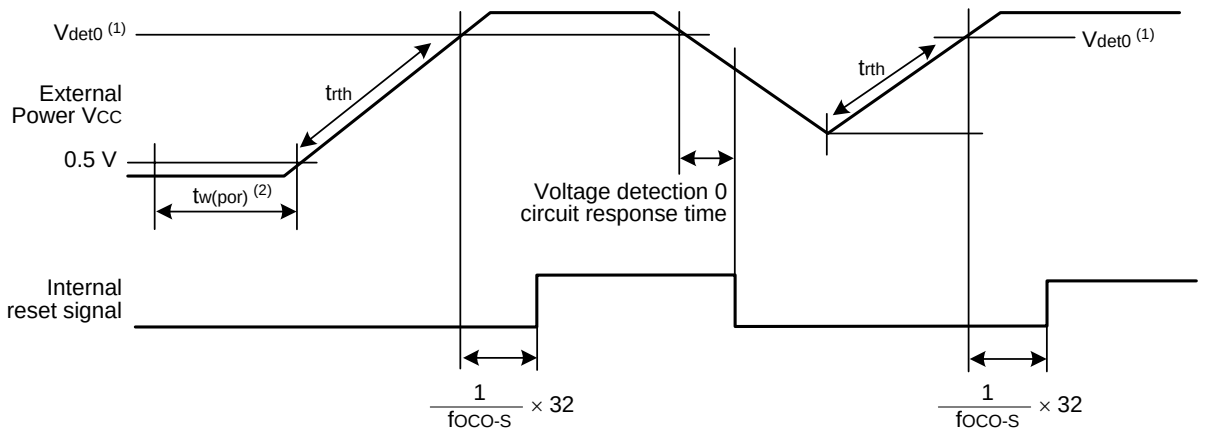
Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det2}	Voltage detection level Vdet2_0	At the falling of V_{CC}	3.70	4.00	4.30	V
—	Hysteresis width at the rising of V_{CC} in voltage detection 2 circuit		—	0.10	—	V
—	Voltage detection 2 circuit response time (2)	At the falling of V_{CC} from 5.0 V to (Vdet2_0 – 0.1) V	—	20	150	µs
—	Voltage detection circuit self power consumption	VCA27 = 1, V_{CC} = 5.0 V	—	1.7	—	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (3)		—	—	100	µs

Notes:
1. The measurement condition is V_{CC} = 1.8 to 5.5 V and T_{opr} = –20 to 85 °C (N version).
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes V_{det2}.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

Table 31.10 Power-on Reset Circuit (2)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t_{rth}	External power V_{CC} rise gradient	(1)	0	—	50,000	mV/msec

Notes:
1. The measurement condition is T_{opr} = –20 to 85 °C (N version), unless otherwise specified.
2. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.



Notes:
1. V_{det0} indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** for details.
2. $t_{w(por)}$ indicates the duration the external power V_{CC} must be held below the valid voltage (0.5 V) to enable a power-on reset. When turning on the power after it falls with voltage monitor 0 reset disabled, maintain $t_{w(por)}$ for 1 ms or more.

Figure 31.5 Power-on Reset Circuit Electrical Characteristics

Table 31.11 High-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
—	High-speed on-chip oscillator frequency after reset	V_{CC} = 1.8 V to 5.5 V	36.0	40	44.0	MHz
	High-speed on-chip oscillator frequency when the FRA4 register correction value is written into the FRA1 register and the FRA5 register correction value into the FRA3 register (2)	V_{CC} = 1.8 V to 5.5 V	33.178	36.864	40.550	MHz
	High-speed on-chip oscillator frequency when the FRA6 register correction value is written into the FRA1 register and the FRA7 register correction value into the FRA3 register	V_{CC} = 1.8 V to 5.5 V	28.8	32	35.2	MHz
—	Oscillation stability time	V_{CC} = 5.0 V, T_{opr} = 25 °C	—	0.5	3	ms
—	Self power consumption at oscillation	V_{CC} = 5.0 V, T_{opr} = 25 °C	—	400	—	µA

Notes:
1. V_{CC} = 1.8 to 5.5 V and T_{opr} = –20 to 85 °C (N version), unless otherwise specified.
2. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

Table 31.12 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		60	125	250	kHz
—	Oscillation stability time	V_{CC} = 5.0 V, T_{opr} = 25 °C	—	30	100	µs
—	Self power consumption at oscillation	V_{CC} = 5.0 V, T_{opr} = 25 °C	—	2	—	µA

Note:
1. V_{CC} = 1.8 to 5.5 V and T_{opr} = –20 to 85 °C (N version), unless otherwise specified.

Table 31.13 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during power-on (2)		—	—	2,000	µs

Notes:
1. The measurement condition is V_{CC} = 1.8 to 5.5 V and T_{opr} = 25 °C.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.

Table 31.14 Timing Requirements of Synchronous Serial Communication Unit (SSU)

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
t_{SUCYC}	SSCK clock cycle time			4	—	—	t_{CYC} (2)
t_{HI}	SSCK clock “H” width			0.4	—	0.6	t_{SUCYC}
t_{LO}	SSCK clock “L” width			0.4	—	0.6	t_{SUCYC}
t_{RISE}	SSCK clock rising time	Master		—	—	1	t_{CYC} (2)
		Slave		—	—	1	µs
t_{FALL}	SSCK clock falling time	Master		—	—	1	t_{CYC} (2)
		Slave		—	—	1	µs
t_{SU}	SSO, SSI data input setup time			100	—	—	ns
t_H	SSO, SSI data input hold time			1	—	—	t_{CYC} (2)
t_{LEAD}	$\overline{SCS}$ setup time	Slave		$1t_{CYC}$ + 50	—	—	ns
t_{LAG}	$\overline{SCS}$ hold time	Slave		$1t_{CYC}$ + 50	—	—	ns
t_{OD}	SSO, SSI data output delay time			—	—	1	t_{CYC} (2)
t_{SA}	SSI slave access time		2.7 V ≤ V_{CC} ≤ 5.5 V	—	—	$1.5t_{CYC}$ + 100	ns
			1.8 V ≤ V_{CC} < 2.7 V	—	—	$1.5t_{CYC}$ + 200	ns
t_{OR}	SSI slave out open time		2.7 V ≤ V_{CC} ≤ 5.5 V	—	—	$1.5t_{CYC}$ + 100	ns
			1.8 V ≤ V_{CC} < 2.7 V	—	—	$1.5t_{CYC}$ + 200	ns

Notes:
1. V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, and T_{opr} = –20 to 85 °C (N version), unless otherwise specified.
2. $1t_{CYC}$ = 1/f1(s)

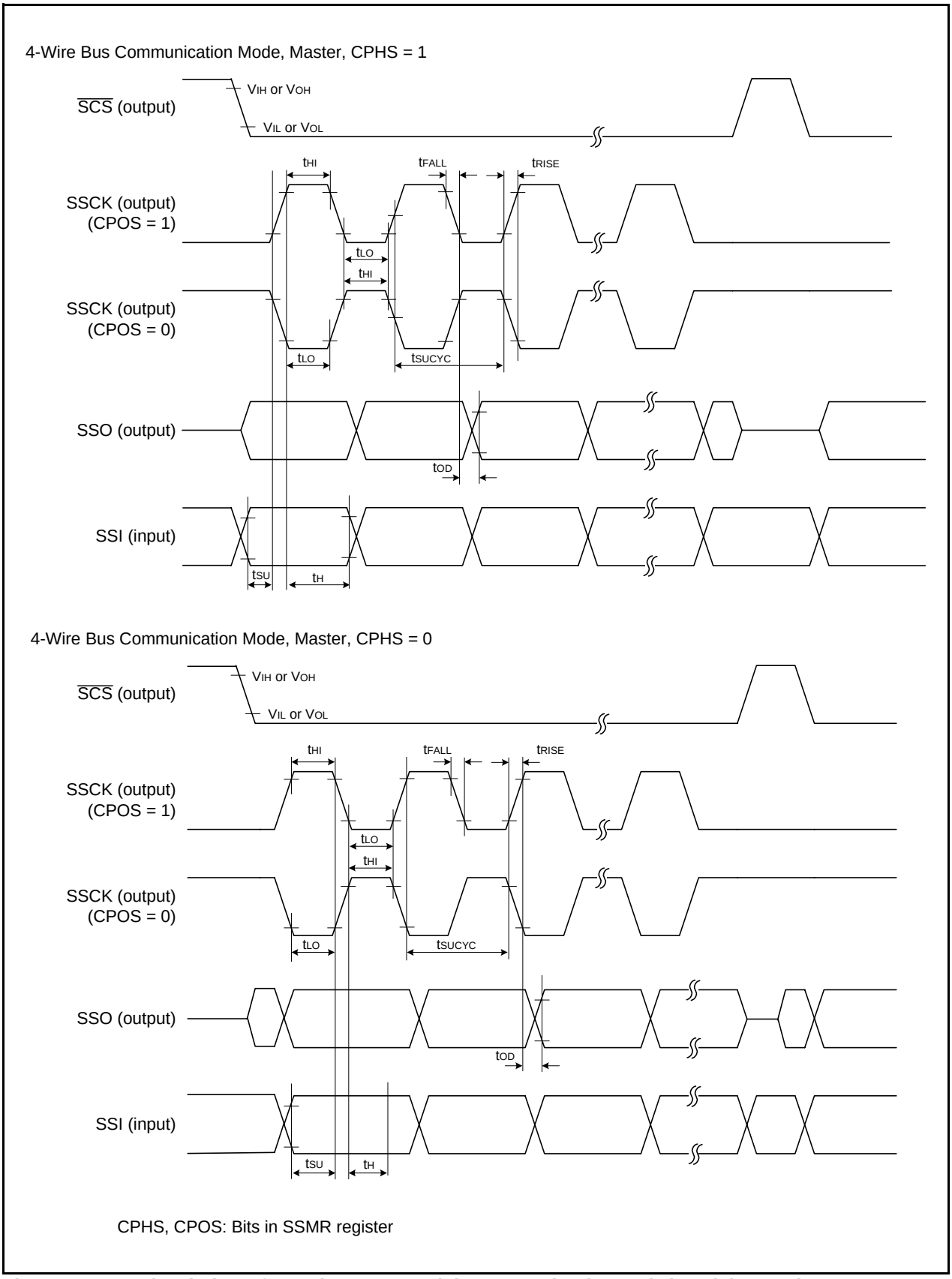


Figure 31.6 I/O Timing of Synchronous Serial Communication Unit (SSU) (Master)

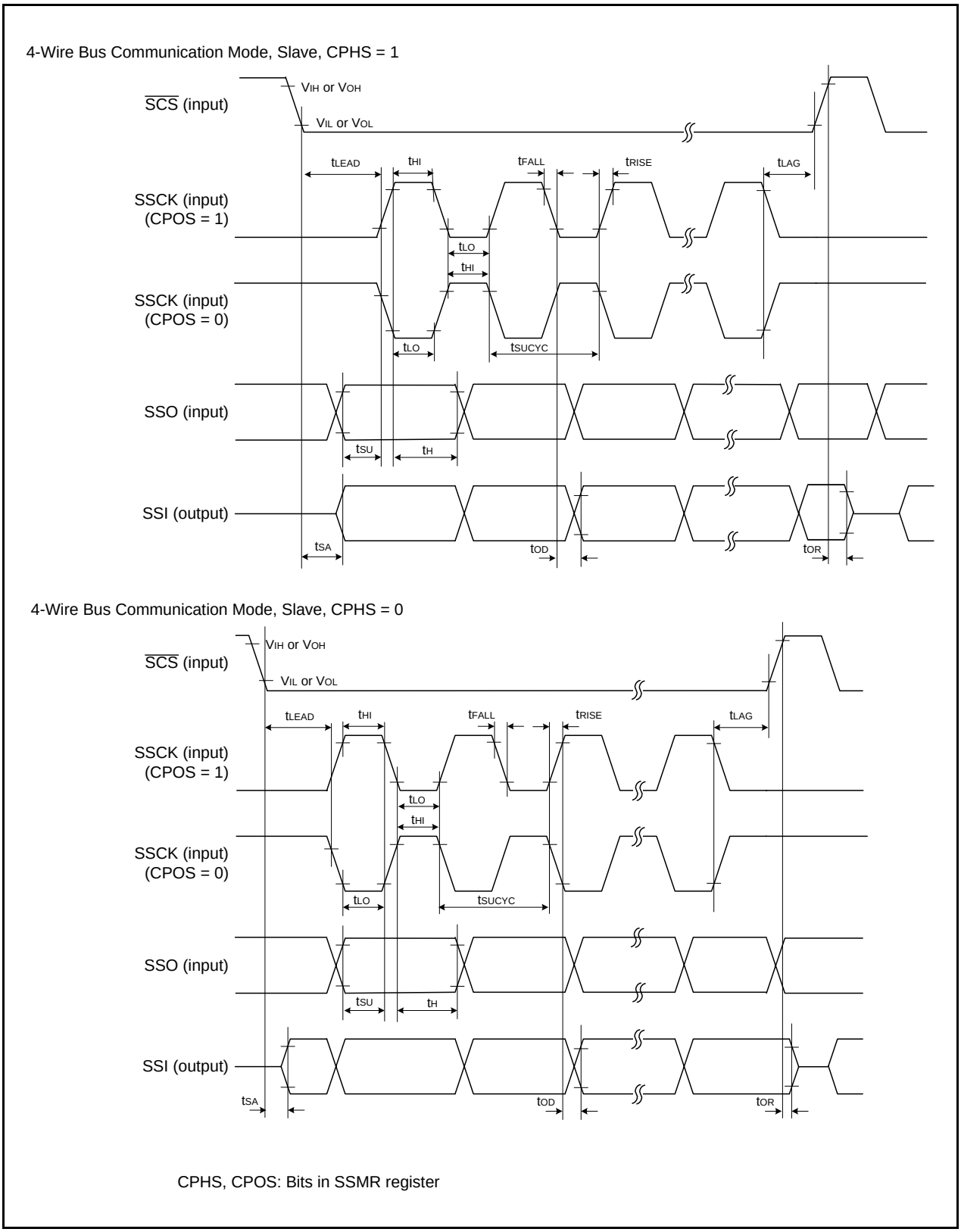


Figure 31.7 I/O Timing of Synchronous Serial Communication Unit (SSU) (Slave)

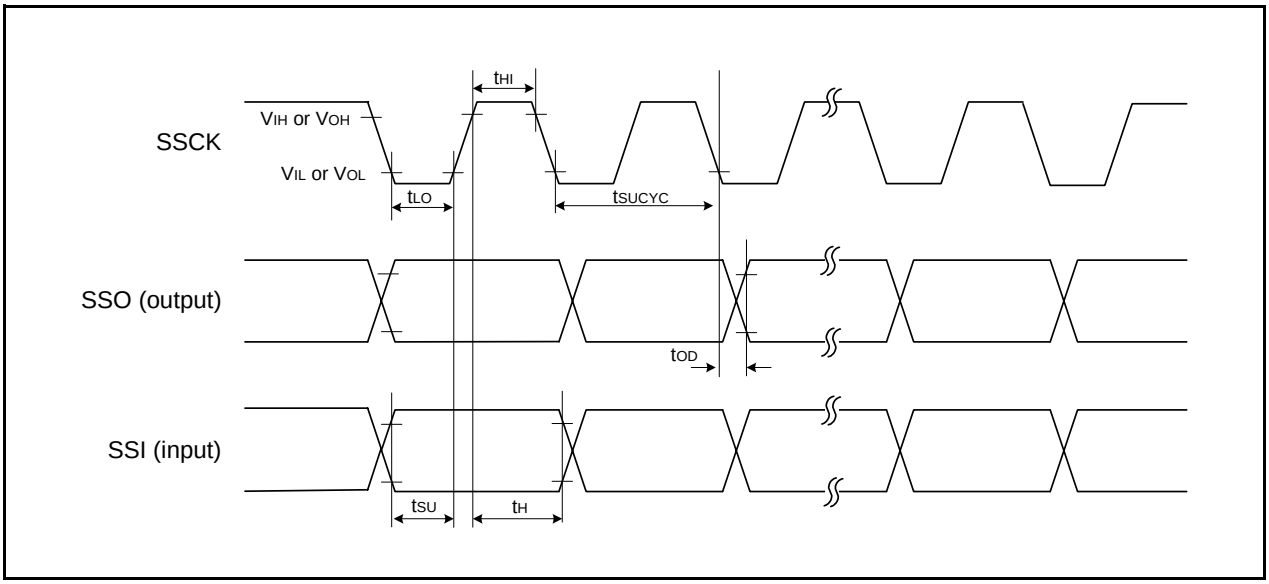
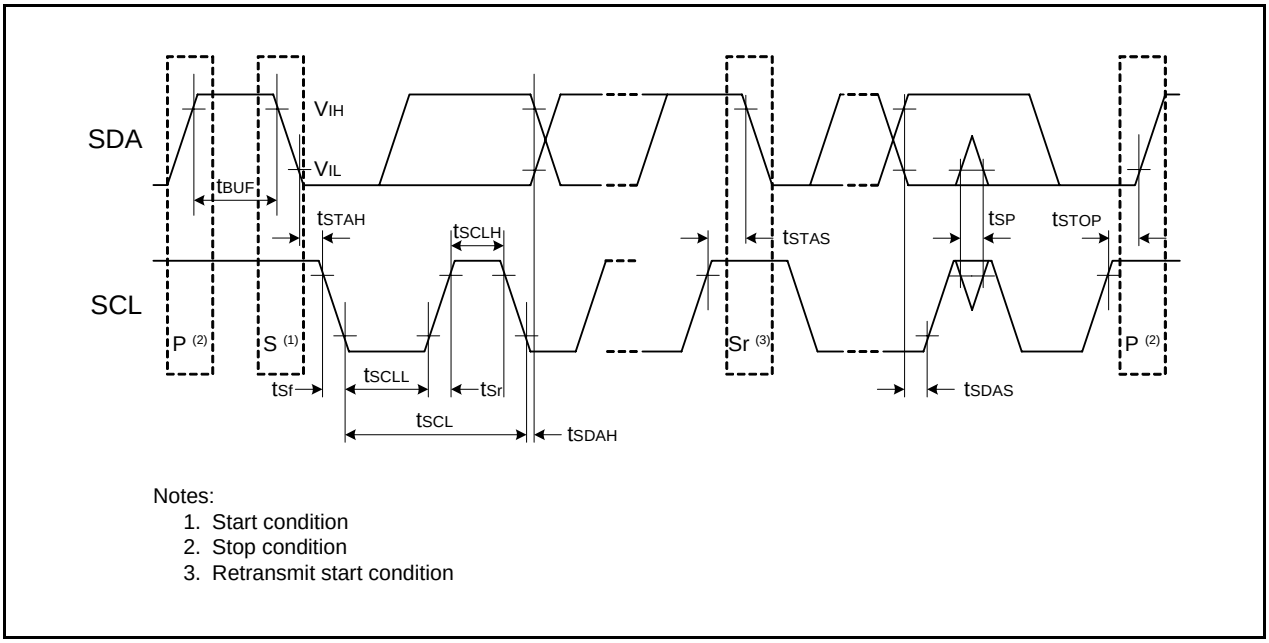


Figure 31.8 I/O Timing of Synchronous Serial Communication Unit (SSU) (Clock Synchronous Communication Mode)

Table 31.15 Timing Requirements of I²C bus Interface

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t_{SCL}	SCL input cycle time		$12t_{CYC} + 600$ (2)	—	—	ns
t_{SCLH}	SCL input “H” width		$3t_{CYC} + 300$ (2)	—	—	ns
t_{SCLL}	SCL input “L” width		$5t_{CYC} + 500$ (2)	—	—	ns
t_{sf}	SCL, SDA input fall time		—	—	300	ns
t_{SP}	SCL, SDA input spike pulse rejection time		—	—	$1t_{CYC}$ (2)	ns
t_{BUF}	SDA input bus-free time		$5t_{CYC}$ (2)	—	—	ns
t_{STAH}	Start condition input hold time		$3t_{CYC}$ (2)	—	—	ns
t_{STAS}	Retransmit start condition input setup time		$3t_{CYC}$ (2)	—	—	ns
t_{STOP}	Stop condition input setup time		$3t_{CYC}$ (2)	—	—	ns
t_{SDAS}	Data input setup time		$1t_{CYC} + 40$ (2)	—	—	ns
t_{SDAH}	Data input hold time		10	—	—	ns

Notes:
1. V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, and T_{opr} = –20 to 85 °C (N version), unless otherwise specified.
2. $1t_{CYC} = 1/f1(s)$



Notes:
1. Start condition
2. Stop condition
3. Retransmit start condition

Figure 31.9 I/O Timing of I²C bus Interface

Table 31.16 Electrical Characteristics (1) [4.2 V ≤ Vcc ≤ 5.5 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output "H" voltage	Other than XOUT	Drive capacity High V_{CC} = 5 V	I_{OH} = –20 mA	V_{CC} – 2.0	—	V_{CC}	V
			Drive capacity Low V_{CC} = 5 V	I_{OH} = –5 mA	V_{CC} – 2.0	—	V_{CC}	V
		XOUT	V_{CC} = 5 V	I_{OH} = –200 µA	1.0	—	V_{CC}	V
V_{OL}	Output "L" voltage	Other than XOUT	Drive capacity High V_{CC} = 5 V	I_{OL} = 20 mA	—	—	2.0	V
			Drive capacity Low V_{CC} = 5 V	I_{OL} = 5 mA	—	—	2.0	V
		XOUT	V_{CC} = 5 V	I_{OL} = 200 µA	—	—	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{INT4}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO,TRCIOA, TRCIOB, TRCIOC, TRCIOD, USB_VBUS, TRCTRG, TRCCLK, RXD0, RXD1, RXD2, RXD3, CLK0, $\overline{CLK1}$, CLK2, CLK3, $\overline{CTS2}$, SSI, SCL, SDA, SSO, SSCK, $\overline{SCS}$			0.1	1.2	—	V
		$\overline{RESET}$			0.1	1.2	—	V
I_{IH}	Input "H" current		V_I = 5 V, V_{CC} = 5.0 V		—	—	5.0	µA
I_{IL}	Input "L" current		V_I = 0 V, V_{CC} = 5.0 V		—	—	–5.0	µA
R_{PULLUP}	Pull-up resistance		V_I = 0 V, V_{CC} = 5.0 V		25	50	100	kΩ
R_{fXIN}	Feedback resistance	XIN			—	0.3	—	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

Note:
1. 4.2 V ≤ V_{CC} ≤ 5.5 V, T_{opr} = –20 to 85 °C (N version), and f(XIN) = 20 MHz, unless otherwise specified.

Table 31.17 Electrical Characteristics (2) [3.3 V ≤ Vcc ≤ 5.5 V] (Topr = –20 to 85 °C (N version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	6.5	15	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	5.3	12.5	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	3.6	—	mA
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	3.0	—	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	2.2	—	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	1.5	—	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	—	7.0	15	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	3.0	—	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-16, MSTIIC=MSTTRC=1	—	1	—	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	—	90	400	µA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	15	100	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	4	90	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	3.5	—	µA
		Stop mode	XIN clock off, Topr = 25 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	—	2.0	5.0	µA
			XIN clock off, Topr = 85 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	—	15	—	µA

Timing Requirements (Unless Otherwise Specified: V_{CC} = 5 V, V_{SS} = 0 V, T_{opr} = 25 °C)

Table 31.18 External Clock Input (XOUT)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XOUT)}$	XOUT input cycle time	50	—	ns
$t_{WH(XOUT)}$	XOUT input “H” width	24	—	ns
$t_{WL(XOUT)}$	XOUT input “L” width	24	—	ns

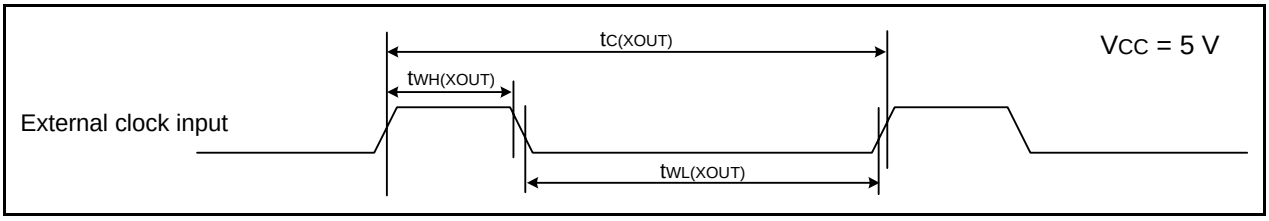


Figure 31.10 External Clock Input Timing Diagram when V_{CC} = 5 V

Table 31.19 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	100	—	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	40	—	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	40	—	ns

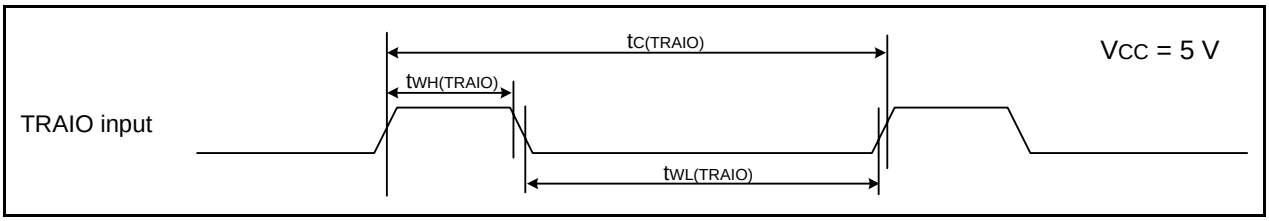


Figure 31.11 TRAIO Input Timing Diagram when V_{CC} = 5 V

Table 31.20 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200	—	ns
$t_{W(CKH)}$	CLKi input “H” width	100	—	ns
$t_{W(CKL)}$	CLKi input “L” width	100	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	50	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	50	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

i = 0 to 3

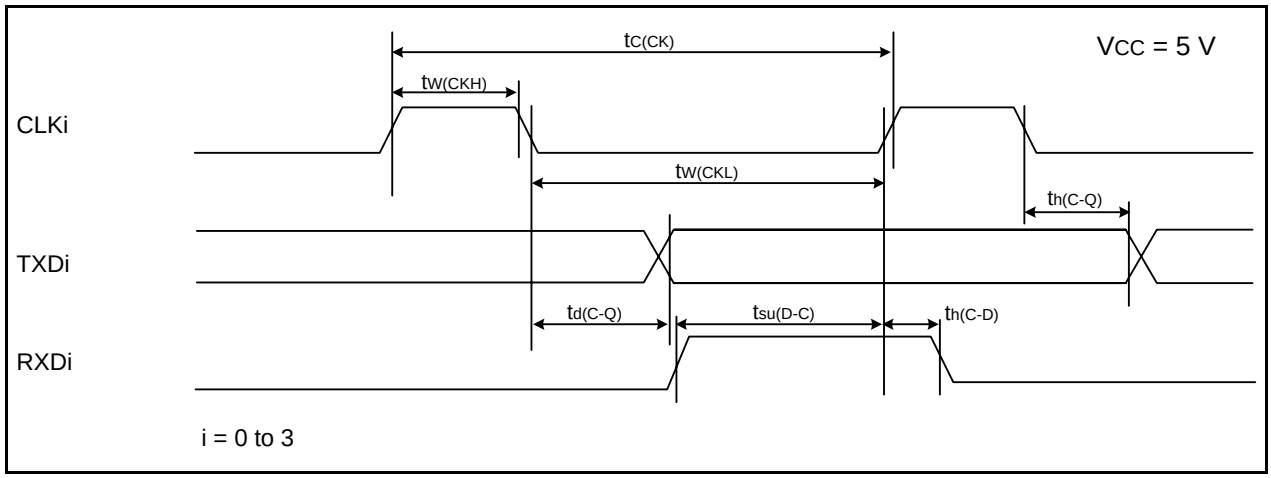


Figure 31.12 Serial Interface Timing Diagram when Vcc = 5 V

Table 31.21 External Interrupt $\overline{INTi}$ (i = 0 to 4) Input, Key Input Interrupt $\overline{KIi}$ (i = 0 to 3)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input “H” width, $\overline{KIi}$ input “H” width	250 (1)	—	ns
$t_{W(INL)}$	$\overline{INTi}$ input “L” width, $\overline{KIi}$ input “L” width	250 (2)	—	ns

Notes:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

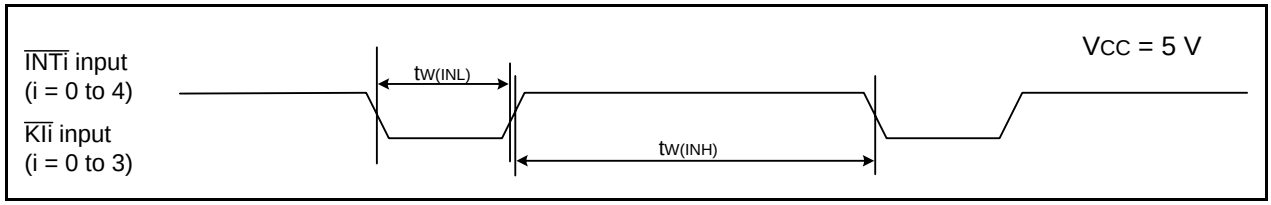


Figure 31.13 Input Timing Diagram for External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{KIi}$ when Vcc = 5 V

Table 31.22 Electrical Characteristics (3) [2.7 V ≤ Vcc < 4.2 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	Other than XOUT	Drive capacity High	I_{OH} = –5 mA	V_{CC} – 0.5	—	V_{CC}	V
			Drive capacity Low	I_{OH} = –1 mA	V_{CC} – 0.5	—	V_{CC}	V
		XOUT		I_{OH} = –200 μA	1.0	—	V_{CC}	V
V_{OL}	Output “L” voltage	Other than XOUT	Drive capacity High	I_{OL} = 5 mA	—	—	0.5	V
			Drive capacity Low	I_{OL} = 1 mA	—	—	0.5	V
		XOUT		I_{OL} = 200 μA	—	—	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{INT4}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, USB_VBUS, TRCTRG, TRCCLK, RXD0, RXD1, RXD2, RXD3, CLK0, $\overline{CLK1}$, CLK2, CLK3, $\overline{CTS2}$, SSI, SCL, SDA, $\overline{SSO}$, SSCK, $\overline{SCS}$	V_{CC} = 3.0 V		0.1	0.4	—	V
		$\overline{RESET}$	V_{CC} = 3.0 V		0.1	0.5	—	V
I_{IH}	Input “H” current		V_I = 3 V, V_{CC} = 3.0 V		—	—	4.0	μA
I_{IL}	Input “L” current		V_I = 0 V, V_{CC} = 3.0 V		—	—	–4.0	μA
R_{PULLUP}	Pull-up resistance		V_I = 0 V, V_{CC} = 3.0 V		42	84	168	kΩ
R_{fXIN}	Feedback resistance	XIN			—	0.3	—	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

Note:
1. 2.7 V ≤ V_{CC} < 4.2 V, T_{opr} = –20 to 85 °C (N version), and f(XIN) = 10 MHz, unless otherwise specified.
2. 3.0 V ≤ V_{CC} < 3.6 V for the USB associated pins.

Table 31.23 Electrical Characteristics (4) [2.7 V ≤ Vcc < 3.3 V]
(Topr = –20 to 85 °C (N version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode	XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	3.5	10	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	1.5	7.5	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	—	7.0	15	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	3.0	—	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	—	4.0	—	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	1.5	—	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-16, MSTIIC=MSTTRC=1	—	1	—	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	—	90	390	µA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	15	90	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	4	80	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	3.5	—	µA
		Stop mode	XIN clock off, Topr = 25 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	—	2.0	5.0	µA
			XIN clock off, Topr = 85 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	—	15	—	µA

Timing requirements (Unless Otherwise Specified: V_{CC} = 3 V, V_{SS} = 0 V, T_{opr} = 25 °C)

Table 31.24 External Clock Input (XOUT)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XOUT)}$	XOUT input cycle time	50	—	ns
$t_{WH(XOUT)}$	XOUT input “H” width	24	—	ns
$t_{WL(XOUT)}$	XOUT input “L” width	24	—	ns

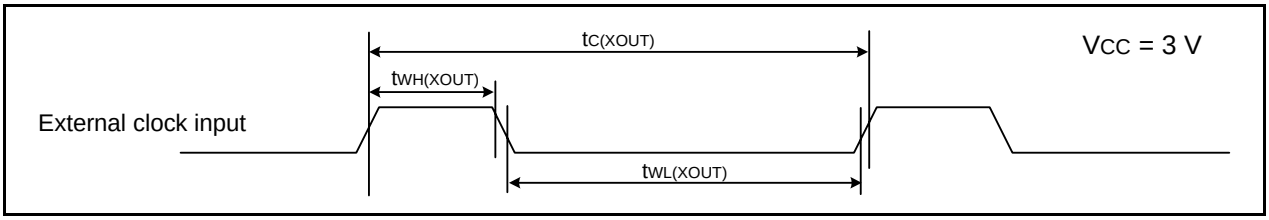


Figure 31.14 External Clock Input Timing Diagram when V_{CC} = 3 V

Table 31.25 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	300	—	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	120	—	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	120	—	ns

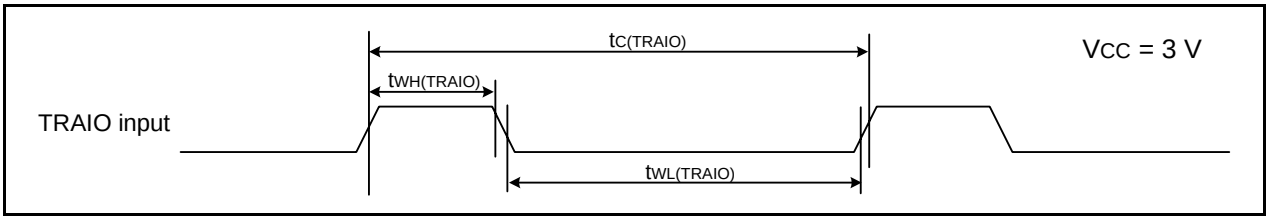


Figure 31.15 TRAIO Input Timing Diagram when V_{CC} = 3 V

Table 31.26 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300	—	ns
$t_{W(CKH)}$	CLKi input “H” width	150	—	ns
$t_{W(CKL)}$	CLKi Input “L” width	150	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	70	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

i = 0 to 3

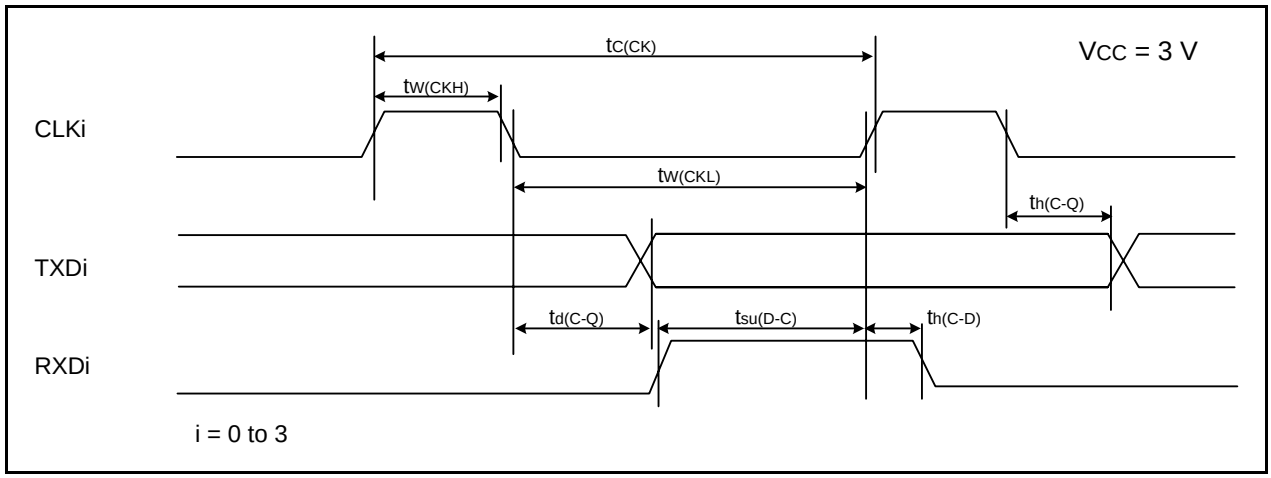


Figure 31.16 Serial Interface Timing Diagram when Vcc = 3 V

Table 31.27 External Interrupt $\overline{INTi}$ (i = 0 to 4) Input, Key Input Interrupt $\overline{KIi}$ (i = 0 to 3)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input “H” width, $\overline{KIi}$ input “H” width	380 (1)	—	ns
$t_{W(INL)}$	$\overline{INTi}$ input “L” width, $\overline{KIi}$ input “L” width	380 (2)	—	ns

Notes:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

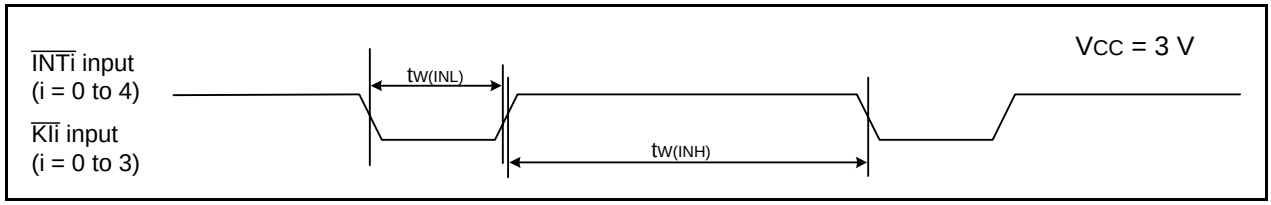


Figure 31.17 Input Timing Diagram for External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{KIi}$ when Vcc = 3 V

Table 31.28 Electrical Characteristics (5) [1.8 V ≤ Vcc < 2.7 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	Other than XOUT	Drive capacity High	I_{OH} = –2 mA	V_{CC} – 0.5	—	V_{CC}	V
			Drive capacity Low	I_{OH} = –1 mA	V_{CC} – 0.5	—	V_{CC}	V
		XOUT		I_{OH} = –200 μA	1.0	—	V_{CC}	V
V_{OL}	Output “L” voltage	Other than XOUT	Drive capacity High	I_{OL} = 2 mA	—	—	0.5	V
			Drive capacity Low	I_{OL} = 1 mA	—	—	0.5	V
		XOUT		I_{OL} = 200 μA	—	—	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{INT4}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRCTRG, TRCCLK, RXD0, RXD1, RXD2, RXD3, CLK0, $\overline{CLK1}$, CLK2, CLK3, $\overline{CTS2}$, SSI, SCL, SDA, SSO, SSCK, $\overline{SCS}$			0.05	0.20	—	V
		$\overline{RESET}$			0.05	0.20	—	V
I_{IH}	Input “H” current		V_I = 2.2 V, V_{CC} = 2.2 V		—	—	4.0	μA
I_{IL}	Input “L” current		V_I = 0 V, V_{CC} = 2.2 V		—	—	–4.0	μA
R_{PULLUP}	Pull-up resistance		V_I = 0 V, V_{CC} = 2.2 V		70	140	300	kΩ
R_{fXIN}	Feedback resistance	XIN			—	0.3	—	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

Note:
1. 1.8 V ≤ V_{CC} < 2.7 V, T_{opr} = –20 to 85 °C (N version), and f(XIN) = 5 MHz, unless otherwise specified.

Table 31.29 Electrical Characteristics (6) [1.8 V ≤ Vcc < 2.7 V] (Topr = –20 to 85 °C (N version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 1.8 to 2.7 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode	XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	2.2	—	mA
			XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	0.8	—	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO-F = 5 MHz Low-speed on-chip oscillator on = 125 kHz No division	—	2.5	10	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 5 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	1.7	—	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-16, MSTIIC=MSTTRC=1	—	1	—	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	—	90	300	µA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	15	90	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	4	80	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	3.5	—	µA
		Stop mode	XIN clock off, Topr = 25 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	—	2.0	5	µA
			XIN clock off, Topr = 85 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	—	15	—	µA

Timing requirements (Unless Otherwise Specified: V_{CC} = 2.2 V, V_{SS} = 0 V, T_{opr} = 25 °C)

Table 31.30 External Clock Input (XOUT)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XOUT)}$	XOUT input cycle time	200	—	ns
$t_{WH(XOUT)}$	XOUT input “H” width	90	—	ns
$t_{WL(XOUT)}$	XOUT input “L” width	90	—	ns

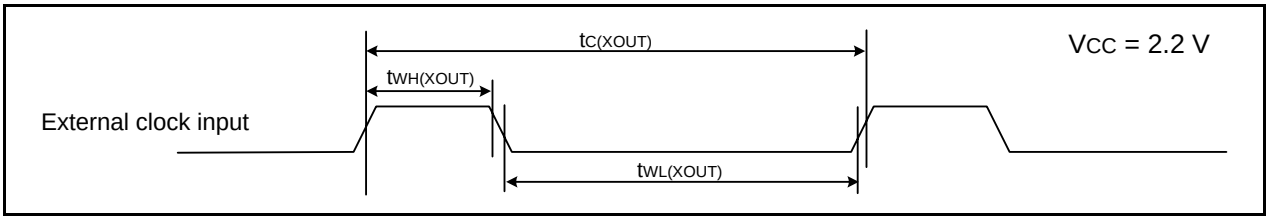


Figure 31.18 External Clock Input Timing Diagram when V_{CC} = 2.2 V

Table 31.31 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	500	—	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	200	—	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	200	—	ns

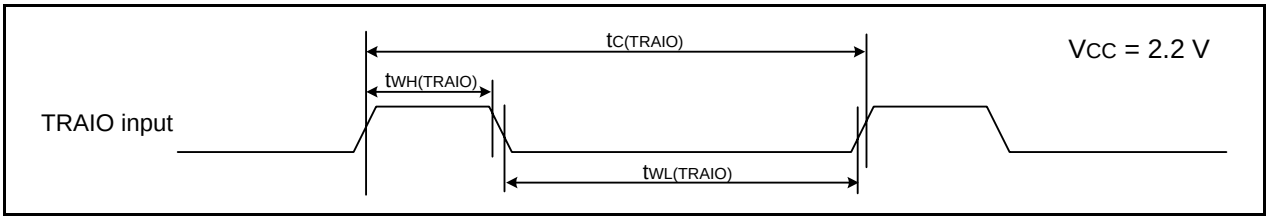


Figure 31.19 TRAIO Input Timing Diagram when V_{CC} = 2.2 V

Table 31.32 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	800	—	ns
$t_{W(CKH)}$	CLKi input “H” width	400	—	ns
$t_{W(CKL)}$	CLKi input “L” width	400	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	200	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	150	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

i = 0 to 3

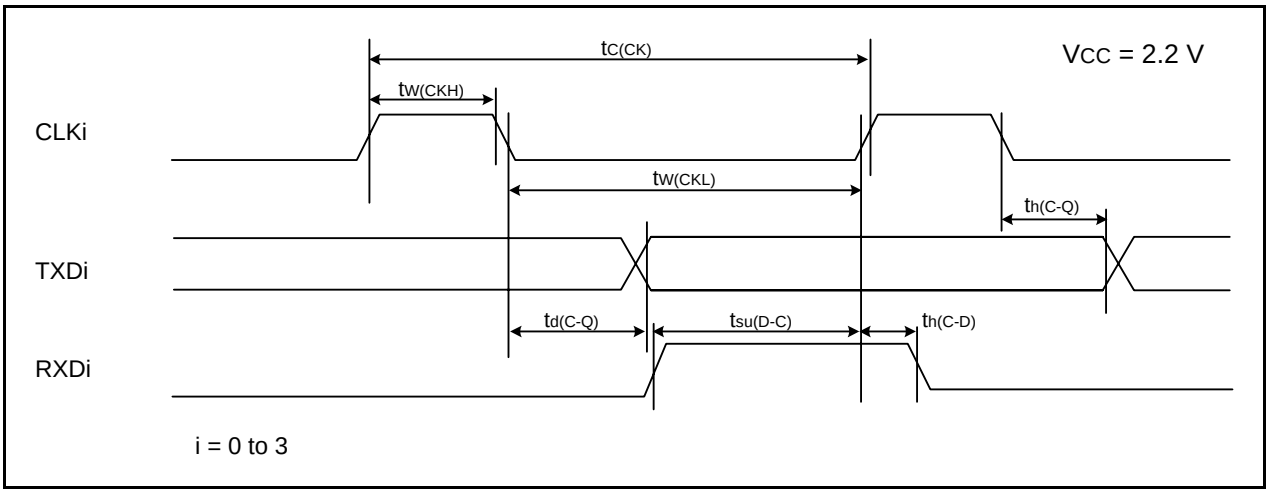


Figure 31.20 Serial Interface Timing Diagram when VCC = 2.2 V

Table 31.33 External Interrupt $\overline{INTi}$ (i = 0 to 4) Input, Key Input Interrupt $\overline{KIi}$ (i = 0 to 3)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input “H” width, $\overline{KIi}$ input “H” width	1000 (1)	—	ns
$t_{W(INL)}$	$\overline{INTi}$ input “L” width, $\overline{KIi}$ input “L” width	1000 (2)	—	ns

Notes:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

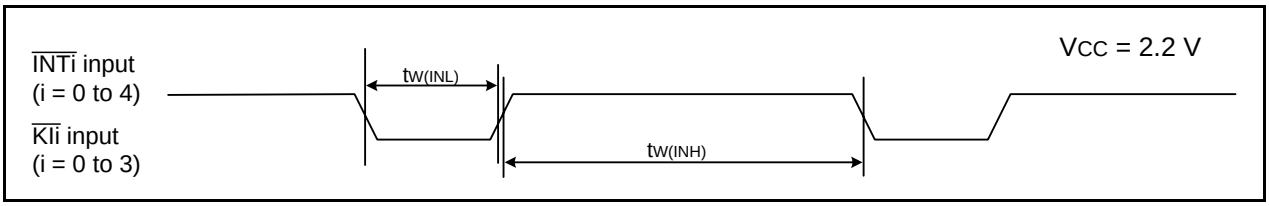


Figure 31.21 Input Timing Diagram for External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{KIi}$ when VCC = 2.2 V

31.2 R8C/3MK Group

Table 31.34 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated Value	Unit
V_{CC}/AV_{CC}	Supply voltage		–0.3 to 6.5	V
V_I	Input voltage		–0.3 to V_{CC} + 0.3	V
V_O	Output voltage		–0.3 to V_{CC} + 0.3	V
P_d	Power dissipation	–20°C ≤ T_{opr} ≤ 85°C	500	mW
T_{opr}	Operating ambient temperature		–20 to 85 (N version)	°C
T_{stg}	Storage temperature		–65 to 150	°C

Table 31.35 Recommended Operating Conditions (1)

Symbol	Parameter				Conditions	Standard			Unit
						Min.	Typ.	Max.	
V_{CC}/AV_{CC}	Supply voltage	When USB function is used				3.0	5.0	5.5	V
		When USB function is not used				1.8	5.0	5.5	V
UV_{CC}	USB Supply Voltage (When UVCC pin is input)	When USB function is used			V_{CC}/AV_{CC} = 3.0 to 3.6 V	—	V_{CC}/AV_{CC} (4)	—	V
		When USB function is not used			V_{CC}/AV_{CC} = 1.8 to 5.5 V	—	V_{CC}/AV_{CC} (4)	—	V
V_{SS}/AV_{SS}	Supply voltage					—	0	—	V
V_{IH}	Input “H” voltage	Other than CMOS input				0.8 V_{CC}	—	V_{CC}	V
		CMOS input	Input level switching function (I/O port)	Input level selection: 0.35 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0.5 V_{CC}	—	V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0.55 V_{CC}	—	V_{CC}	V
					1.8 V ≤ V_{CC} < 2.7 V	0.65 V_{CC}	—	V_{CC}	V
				Input level selection: 0.5 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0.65 V_{CC}	—	V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0.7 V_{CC}	—	V_{CC}	V
					1.8 V ≤ V_{CC} < 2.7 V	0.8 V_{CC}	—	V_{CC}	V
				Input level selection: 0.7 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0.85 V_{CC}	—	V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0.85 V_{CC}	—	V_{CC}	V
					1.8 V ≤ V_{CC} < 2.7 V	0.85 V_{CC}	—	V_{CC}	V
		External clock input (XOUT)				1.2	—	V_{CC}	V
V_{IL}	Input “L” voltage	Other than CMOS input				0	—	0.2 V_{CC}	V
		CMOS input	Input level switching function (I/O port)	Input level selection: 0.35 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0	—	0.2 V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0	—	0.2 V_{CC}	V
					1.8 V ≤ V_{CC} < 2.7 V	0	—	0.2 V_{CC}	V
				Input level selection: 0.5 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0	—	0.4 V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0	—	0.3 V_{CC}	V
					1.8 V ≤ V_{CC} < 2.7 V	0	—	0.2 V_{CC}	V
				Input level selection: 0.7 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0	—	0.55 V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0	—	0.45 V_{CC}	V
					1.8 V ≤ V_{CC} < 2.7 V	0	—	0.35 V_{CC}	V
		External clock input (XOUT)				0	—	0.4	V
$I_{OH(sum)}$	Peak sum output “H” current	Sum of all pins $I_{OH(peak)}$				—	—	−160	mA
$I_{OH(sum)}$	Average sum output “H” current	Sum of all pins $I_{OH(avg)}$				—	—	−80	mA
$I_{OH(peak)}$	Peak output “H” current	Drive capacity Low				—	—	−10	mA
		Drive capacity High				—	—	−40	mA
$I_{OH(avg)}$	Average output “H” current	Drive capacity Low				—	—	−5	mA
		Drive capacity High				—	—	−20	mA
$I_{OL(sum)}$	Peak sum output “L” current	Sum of all pins $I_{OL(peak)}$				—	—	160	mA
$I_{OL(sum)}$	Average sum output “L” current	Sum of all pins $I_{OL(avg)}$				—	—	80	mA
$I_{OL(peak)}$	Peak output “L” current	Drive capacity Low				—	—	10	mA
		Drive capacity High				—	—	40	mA
$I_{OL(avg)}$	Average output “L” current	Drive capacity Low				—	—	5	mA
		Drive capacity High				—	—	20	mA
$f_{(XIN)}$	XIN clock input oscillation frequency				2.7 V ≤ V_{CC} ≤ 5.5 V	—	—	20	MHz
					1.8 V ≤ V_{CC} < 2.7 V	—	—	5	MHz
fOCO40M	When used as the count source for timer RC (3)				2.7 V ≤ V_{CC} ≤ 5.5 V	32	—	40	MHz
fOCO-F	fOCO-F frequency				2.7 V ≤ V_{CC} ≤ 5.5 V	—	—	20	MHz
					1.8 V ≤ V_{CC} < 2.7 V	—	—	5	MHz
—	System clock frequency				2.7 V ≤ V_{CC} ≤ 5.5 V	—	—	20	MHz
					1.8 V ≤ V_{CC} < 2.7 V	—	—	5	MHz
$f_{(BCLK)}$	CPU clock frequency				2.7 V ≤ V_{CC} ≤ 5.5 V	—	—	20	MHz
					1.8 V ≤ V_{CC} < 2.7 V	—	—	5	MHz
$t_{su(PLL)}$	PLL frequency symthesizer stabilization wait time				4.0 V ≤ V_{CC} ≤ 5.5 V	—	—	2	ms
					2.7 V ≤ V_{CC} < 4.0 V	—	—	3	ms

Notes:
1. V_{CC} = 1.8 to 5.5 V and T_{opr} = −20 to 85 °C (N version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.
3. fOCO40M can be used as the count source for timer RC in the range of V_{CC} = 2.7 to 5.5 V.
4. Connect V_{CC}/AV_{CC} for the UV_{CC} pin input.

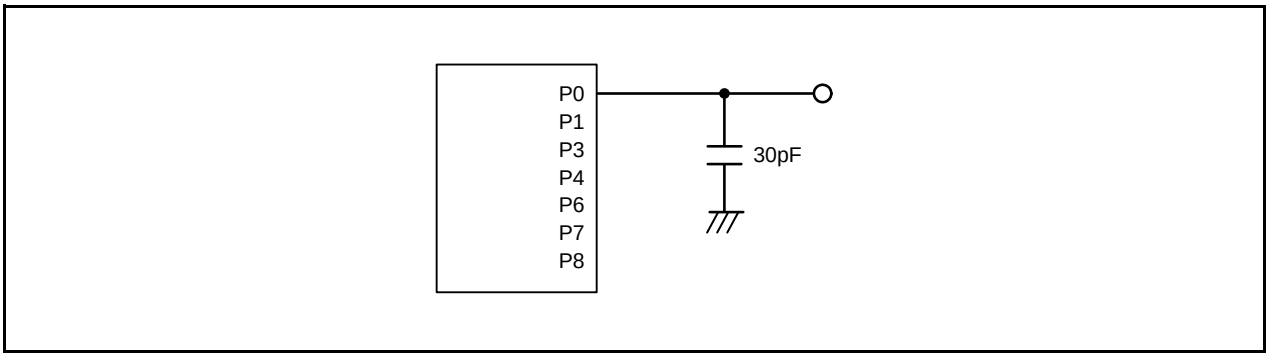


Figure 31.22 Ports P0, P1, P3, P4, P6, P7 and P8 Timing Measurement Circuit

Table 31.36 A/D Converter Characteristics

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
—	Resolution		V_{ref} = AV_{CC}		—	—	10	Bit
—	Absolute accuracy	10-bit mode	V_{ref} = AV_{CC} = 5.0 V	AN0, AN3 to AN7 input, AN8 to AN11 input	—	—	±3	LSB
			V_{ref} = AV_{CC} = 3.3 V	AN0, AN3 to AN7 input, AN8 to AN11 input	—	—	±5	LSB
			V_{ref} = AV_{CC} = 3.0 V	AN0, AN3 to AN7 input, AN8 to AN11 input	—	—	±5	LSB
			V_{ref} = AV_{CC} = 2.2 V	AN0, AN3 to AN7 input, AN8 to AN11 input	—	—	±5	LSB
		8-bit mode	V_{ref} = AV_{CC} = 5.0 V	AN0, AN3 to AN7 input, AN8 to AN11 input	—	—	±2	LSB
			V_{ref} = AV_{CC} = 3.3 V	AN0, AN3 to AN7 input, AN8 to AN11 input	—	—	±2	LSB
			V_{ref} = AV_{CC} = 3.0 V	AN0, AN3 to AN7 input, AN8 to AN11 input	—	—	±2	LSB
			V_{ref} = AV_{CC} = 2.2 V	AN0, AN3 to AN7 input, AN8 to AN11 input	—	—	±2	LSB
ϕAD	A/D conversion clock		4.0 V ≤ V_{ref} = AV_{CC} ≤ 5.5 V (2)		2	—	20	MHz
			3.2 V ≤ V_{ref} = AV_{CC} ≤ 5.5 V (2)		2	—	16	MHz
			2.7 V ≤ V_{ref} = AV_{CC} ≤ 5.5 V (2)		2	—	10	MHz
			2.2 V ≤ V_{ref} = AV_{CC} ≤ 5.5 V (2)		2	—	5	MHz
—	Tolerance level impedance				—	3	—	kΩ
t_{CONV}	Conversion time	10-bit mode	V_{ref} = AV_{CC} = 5.0 V, ϕAD = 20 MHz		2.2	—	—	µs
		8-bit mode	V_{ref} = AV_{CC} = 5.0 V, ϕAD = 20 MHz		2.2	—	—	µs
t_{SAMP}	Sampling time		ϕAD = 20 MHz		0.8	—	—	µs
I_{Vref}	V_{ref} current		V_{CC} = 5.0 V, XIN = f1 = ϕAD = 20 MHz		—	45	—	µA
V_{ref}	Reference voltage				2.2	—	AV_{CC}	V
VIA	Analog input voltage(3)				0	—	Vref	V
OCVREF	On-chip reference voltage		2 MHz ≤ ϕAD ≤ 4 MHz		1.19	1.34	1.49	V

Notes:
1. V_{CC}/AV_{CC} = V_{ref} = 2.2 to 5.5 V, V_{SS} = 0 V, and T_{opr} = –20 to 85 °C (N version), unless otherwise specified.
2. The A/D conversion result will be undefined in wait mode, stop mode, when the flash memory stops, and in low-current-consumption mode. Do not perform A/D conversion in these states or transition to these states during A/D conversion.
3. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

Table 31.37 Comparator B Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{ref}	IVREF1, IVREF3 input reference voltage		0	—	V_{CC} – 1.4	V
V_I	IVCMP1, IVCMP3 input voltage		–0.3	—	V_{CC} + 0.3	V
—	Offset		—	5	100	mV
t_d	Comparator output delay time (2)	$V_I = V_{ref} \pm 100$ mV	—	0.1	—	µs
I_{CMP}	Comparator operating current	V_{CC} = 5.0 V	—	17.5	—	µA

Notes:
1. V_{CC} = 2.7 to 5.5 V and T_{opr} = –20 to 85 °C (N version), unless otherwise specified.
2. When the digital filter is disabled.

Table 31.38 USB Characteristics

Symbol	Parameter		Condition	Standard			Unit
				Min.	Typ.	Max.	
V_{IH}	Input characteristics	Input “H” voltage	Figures 31.23 and 31.24	2.0	—	—	V
V_{IL}		Input “L” voltage		—	—	0.8	V
V_{DI}		Differential input sensitivity		0.2	—	—	V
V_{CM}		Differential common mode range		0.8	—	2.5	V
V_{OH}	Output characteristics	Output “H” voltage	Figures 31.23 and 31.24 I_{CH} = 200µA	2.8	—	—	V
V_{OL}		Output “L” voltage	Figures 31.23 and 31.24 I_{CL} = 2 mA	—	—	0.3	V
V_{CRS}		Crossover voltage	Figures 31.23 and 31.24	1.3	—	2.0	V
t_R		Rise time	Figures 31.23 and 31.24	4.0	—	20.0	ns
t_F		Fall time	Figures 31.23 and 31.24	4.0	—	20.0	ns
t_{RFM}		Rise time / Fall time matching	Figures 31.23 and 31.24 (tR/tF)	90.0	—	111.1	%
Z_{DRV}		Output resistance	Figures 31.23 and 31.24 Includes R_S = 27Ω	28	—	44.0	Ω
UVCC	UVCC output voltage		V_{CC} = 4.0 to 5.5V, PXXCON = VDDUSBE = 1	3.0	3.3	3.6	V
			PXXCON = 0	—	V_{CC}	—	V
I_{susp}	Consumption current of the Internal power supply for USB		V_{CC} = 4.0 to 5.5 V UV_{CC} - V_{SS} 0.33 µF V_{CC} - V_{SS} 0.1 µF		50		µA

Note:
1. Referenced to V_{CC} = 3.0 to 5.5 V, UV_{CC} = 3.0 V, at T_{opr} = -20 to 85 °C (N version) unless otherwise specified.

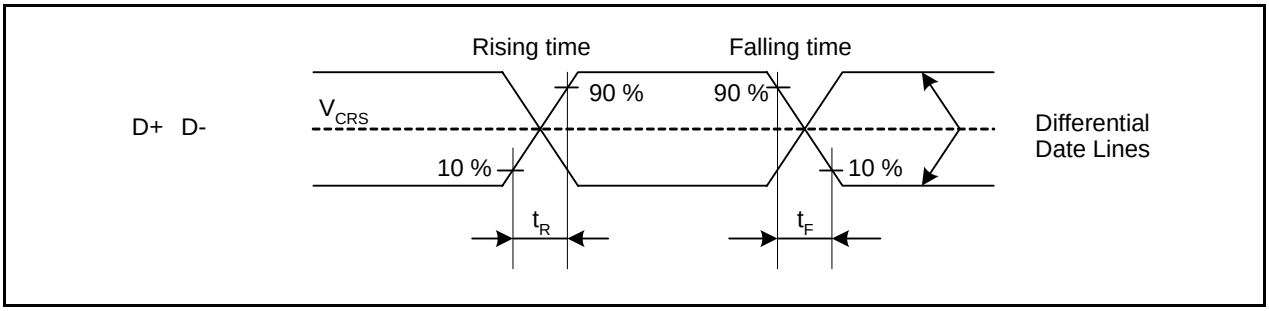


Figure 31.23 Data Signal Timing Diagram

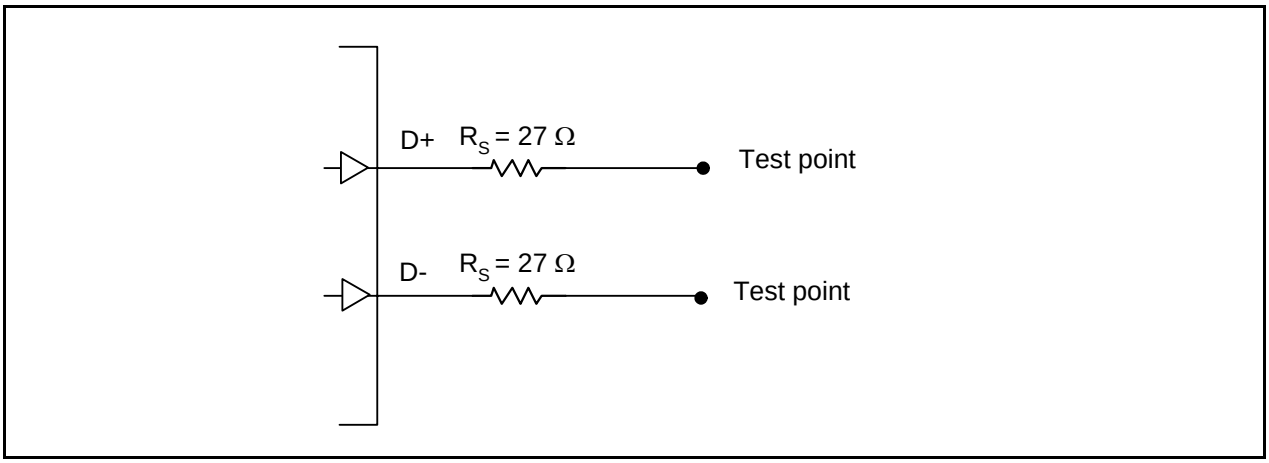


Figure 31.24 Load Condition

Table 31.39 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance (2)		1,000 (3)	—	—	times
—	Byte program time		—	80	500	µs
—	Block erase time		—	0.3	—	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		—	—	5 + CPU clock × 3 cycles	ms
—	Interval from erase start/restart until following suspend request		0	—	—	µs
—	Time from suspend until erase restart		—	—	30 + CPU clock × 1 cycle	µs
$t_{d(CMDRST-READY)}$	Time from when command is forcibly stopped until reading is enabled		–	–	30 + CPU clock × 1 cycle	µs
—	Program, erase voltage		2.7	—	5.5	V
—	Read voltage		1.8	—	5.5	V
—	Program, erase temperature		0	—	60	°C
—	Data hold time (7)	Ambient temperature = 55 °C	20	—	—	year

Notes:
1. V_{CC} = 2.7 to 5.5 V and T_{opr} = 0 to 60 °C, unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed.)
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 31.40 Flash Memory (Data flash Block A to Block D) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance (2)		10,000 (3)	—	—	times
—	Byte program time (program/erase endurance ≤ 1,000 times)		—	160	1500	µs
—	Byte program time (program/erase endurance > 1,000 times)		—	300	1500	µs
—	Block erase time (program/erase endurance ≤ 1,000 times)		—	0.2	1	s
—	Block erase time (program/erase endurance > 1,000 times)		—	0.3	1	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		—	—	5 + CPU clock × 3 cycles	ms
—	Interval from erase start/restart until following suspend request		0	—	—	µs
—	Time from suspend until erase restart		—	—	30 + CPU clock × 1 cycle	µs
$t_{d(CMDRST-READY)}$	Time from when command is forcibly stopped until reading is enabled		–	–	30 + CPU clock × 1 cycle	µs
—	Program, erase voltage		2.7	—	5.5	V
—	Read voltage		1.8	—	5.5	V
—	Program, erase temperature		–20	—	85	°C
—	Data hold time (7)	Ambient temperature = 55 °C	20	—	—	year

Notes:
1. V_{CC} = 2.7 to 5.5 V and T_{opr} = –20 to 85 °C (N version), unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed.)
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A to D can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

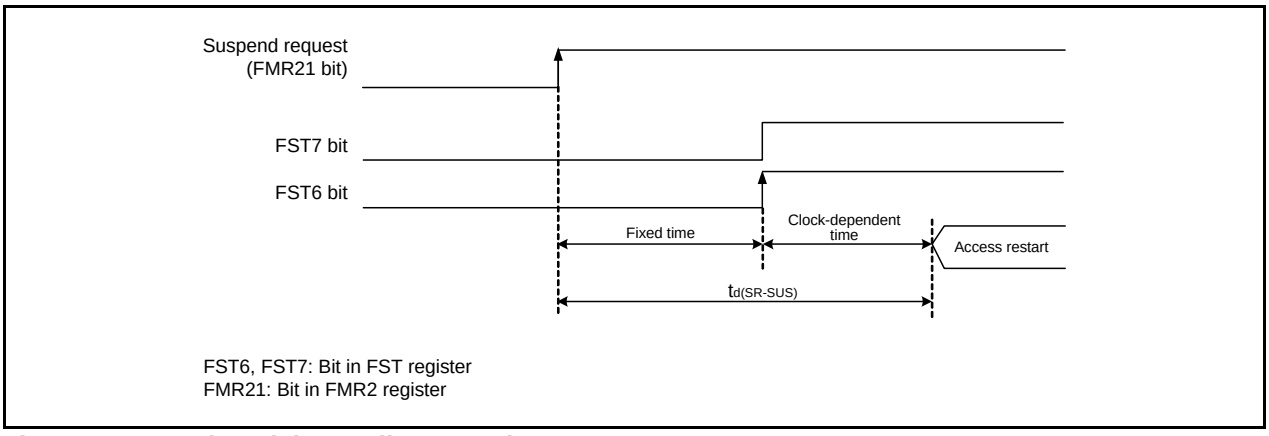


Figure 31.25 Time delay until Suspend

Table 31.41 Voltage Detection 0 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det0}	Voltage detection level Vdet0_0 (2)		1.80	1.90	2.05	V
	Voltage detection level Vdet0_1 (2)		2.15	2.35	2.50	V
	Voltage detection level Vdet0_2 (2)		2.70	2.85	3.05	V
	Voltage detection level Vdet0_3 (2)		3.55	3.80	4.05	V
—	Voltage detection 0 circuit response time (4)	At the falling of V_{CC} from 5.0 V to (Vdet0_0 – 0.1) V	—	6	150	µs
—	Voltage detection circuit self power consumption	VCA25 = 1, V_{CC} = 5.0 V	—	1.5	—	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (3)		—	—	100	µs

Notes:
1. The measurement condition is V_{CC} = 1.8 to 5.5 V and T_{opr} = –20 to 85 °C (N version).
2. Select the voltage detection level with bits VDSEL0 and VDSEL1 in the OFS register.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.
4. Time until the voltage monitor 0 reset is generated after the voltage passes V_{det0}.

Table 31.42 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det1}	Voltage detection level Vdet1_0 (2)	At the falling of V_{CC}	2.00	2.20	2.40	V
	Voltage detection level Vdet1_1 (2)	At the falling of V_{CC}	2.15	2.35	2.55	V
	Voltage detection level Vdet1_2 (2)	At the falling of V_{CC}	2.30	2.50	2.70	V
	Voltage detection level Vdet1_3 (2)	At the falling of V_{CC}	2.45	2.65	2.85	V
	Voltage detection level Vdet1_4 (2)	At the falling of V_{CC}	2.60	2.80	3.00	V
	Voltage detection level Vdet1_5 (2)	At the falling of V_{CC}	2.75	2.95	3.15	V
	Voltage detection level Vdet1_6 (2)	At the falling of V_{CC}	2.85	3.10	3.40	V
	Voltage detection level Vdet1_7 (2)	At the falling of V_{CC}	3.00	3.25	3.55	V
	Voltage detection level Vdet1_8 (2)	At the falling of V_{CC}	3.15	3.40	3.70	V
	Voltage detection level Vdet1_9 (2)	At the falling of V_{CC}	3.30	3.55	3.85	V
	Voltage detection level Vdet1_A (2)	At the falling of V_{CC}	3.45	3.70	4.00	V
	Voltage detection level Vdet1_B (2)	At the falling of V_{CC}	3.60	3.85	4.15	V
	Voltage detection level Vdet1_C (2)	At the falling of V_{CC}	3.75	4.00	4.30	V
	Voltage detection level Vdet1_D (2)	At the falling of V_{CC}	3.90	4.15	4.45	V
	Voltage detection level Vdet1_E (2)	At the falling of V_{CC}	4.05	4.30	4.60	V
	Voltage detection level Vdet1_F (2)	At the falling of V_{CC}	4.20	4.45	4.75	V
—	Hysteresis width at the rising of V_{CC} in voltage detection 1 circuit	Vdet1_0 to Vdet1_5 selected	—	0.07	—	V
		Vdet1_6 to Vdet1_F selected	—	0.10	—	V
—	Voltage detection 1 circuit response time (3)	At the falling of V_{CC} from 5.0 V to (Vdet1_0 – 0.1) V	—	60	150	µs
—	Voltage detection circuit self power consumption	VCA26 = 1, V_{CC} = 5.0 V	—	1.7	—	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (4)		—	—	100	µs

Notes:
1. The measurement condition is V_{CC} = 1.8 to 5.5 V and T_{opr} = –20 to 85 °C (N version).
2. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
3. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V_{det1}.
4. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

Table 31.43 Voltage Detection 2 Circuit Electrical Characteristics

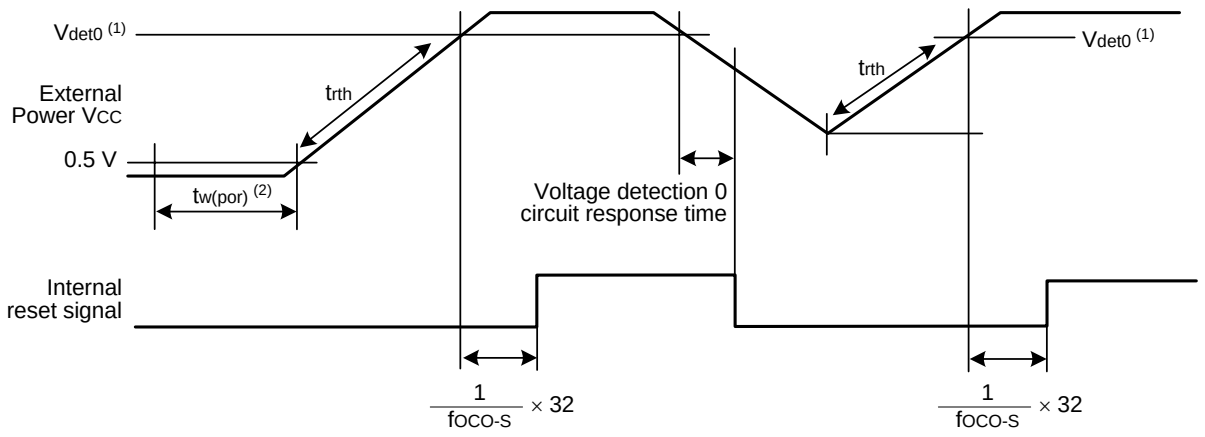
Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det2}	Voltage detection level Vdet2_0	At the falling of V_{CC}	3.70	4.00	4.30	V
—	Hysteresis width at the rising of V_{CC} in voltage detection 2 circuit		—	0.10	—	V
—	Voltage detection 2 circuit response time (2)	At the falling of V_{CC} from 5.0 V to (Vdet2_0 – 0.1) V	—	20	150	µs
—	Voltage detection circuit self power consumption	VCA27 = 1, V_{CC} = 5.0 V	—	1.7	—	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (3)		—	—	100	µs

Notes:
1. The measurement condition is V_{CC} = 1.8 to 5.5 V and T_{opr} = –20 to 85 °C (N version).
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes V_{det2}.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

Table 31.44 Power-on Reset Circuit (2)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t_{rth}	External power V_{CC} rise gradient	(1)	0	—	50,000	mV/msec

Notes:
1. The measurement condition is T_{opr} = –20 to 85 °C (N version), unless otherwise specified.
2. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.



Notes:
1. V_{det0} indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** for details.
2. $t_{w(por)}$ indicates the duration the external power V_{CC} must be held below the valid voltage (0.5 V) to enable a power-on reset. When turning on the power after it falls with voltage monitor 0 reset disabled, maintain $t_{w(por)}$ for 1 ms or more.

Figure 31.26 Power-on Reset Circuit Electrical Characteristics

Table 31.45 High-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
—	High-speed on-chip oscillator frequency after reset	V_{CC} = 1.8 V to 5.5 V	36.0	40	44.0	MHz
	High-speed on-chip oscillator frequency when the FRA4 register correction value is written into the FRA1 register and the FRA5 register correction value into the FRA3 register (2)	V_{CC} = 1.8 V to 5.5 V	33.178	36.864	40.550	MHz
	High-speed on-chip oscillator frequency when the FRA6 register correction value is written into the FRA1 register and the FRA7 register correction value into the FRA3 register	V_{CC} = 1.8 V to 5.5 V	28.8	32	35.2	MHz
—	Oscillation stability time	V_{CC} = 5.0 V, T_{opr} = 25 °C	—	0.5	3	ms
—	Self power consumption at oscillation	V_{CC} = 5.0 V, T_{opr} = 25 °C	—	400	—	µA

Notes:
1. V_{CC} = 1.8 to 5.5 V and T_{opr} = –20 to 85 °C (N version), unless otherwise specified.
2. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

Table 31.46 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		60	125	250	kHz
—	Oscillation stability time	V_{CC} = 5.0 V, T_{opr} = 25 °C	—	30	100	µs
—	Self power consumption at oscillation	V_{CC} = 5.0 V, T_{opr} = 25 °C	—	2	—	µA

Note:
1. V_{CC} = 1.8 to 5.5 V and T_{opr} = –20 to 85 °C (N version), unless otherwise specified.

Table 31.47 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during power-on (2)		—	—	2,000	µs

Notes:
1. The measurement condition is V_{CC} = 1.8 to 5.5 V and T_{opr} = 25 °C.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.

Table 31.48 Timing Requirements of Synchronous Serial Communication Unit (SSU)

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
t_{SUCYC}	SSCK clock cycle time			4	—	—	t_{CYC} (2)
t_{HI}	SSCK clock “H” width			0.4	—	0.6	t_{SUCYC}
t_{LO}	SSCK clock “L” width			0.4	—	0.6	t_{SUCYC}
t_{RISE}	SSCK clock rising time	Master		—	—	1	t_{CYC} (2)
		Slave		—	—	1	µs
t_{FALL}	SSCK clock falling time	Master		—	—	1	t_{CYC} (2)
		Slave		—	—	1	µs
t_{SU}	SSO, SSI data input setup time			100	—	—	ns
t_H	SSO, SSI data input hold time			1	—	—	t_{CYC} (2)
t_{LEAD}	$\overline{SCS}$ setup time	Slave		$1t_{CYC}$ + 50	—	—	ns
t_{LAG}	$\overline{SCS}$ hold time	Slave		$1t_{CYC}$ + 50	—	—	ns
t_{OD}	SSO, SSI data output delay time			—	—	1	t_{CYC} (2)
t_{SA}	SSI slave access time		2.7 V ≤ V_{CC} ≤ 5.5 V	—	—	$1.5t_{CYC}$ + 100	ns
			1.8 V ≤ V_{CC} < 2.7 V	—	—	$1.5t_{CYC}$ + 200	ns
t_{OR}	SSI slave out open time		2.7 V ≤ V_{CC} ≤ 5.5 V	—	—	$1.5t_{CYC}$ + 100	ns
			1.8 V ≤ V_{CC} < 2.7 V	—	—	$1.5t_{CYC}$ + 200	ns

Notes:
1. V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, and T_{opr} = –20 to 85 °C (N version), unless otherwise specified.
2. $1t_{CYC}$ = 1/f1(s)

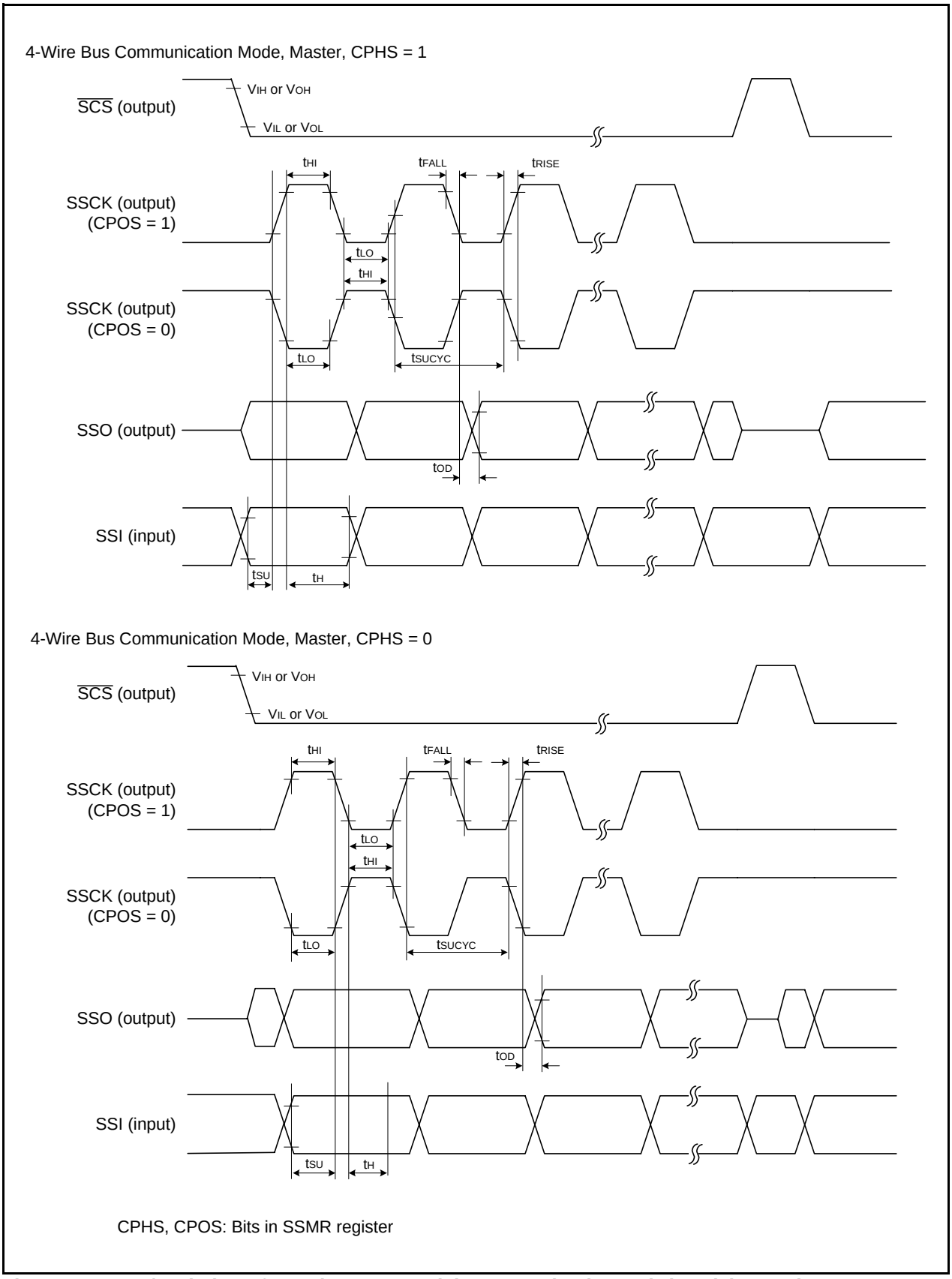


Figure 31.27 I/O Timing of Synchronous Serial Communication Unit (SSU) (Master)

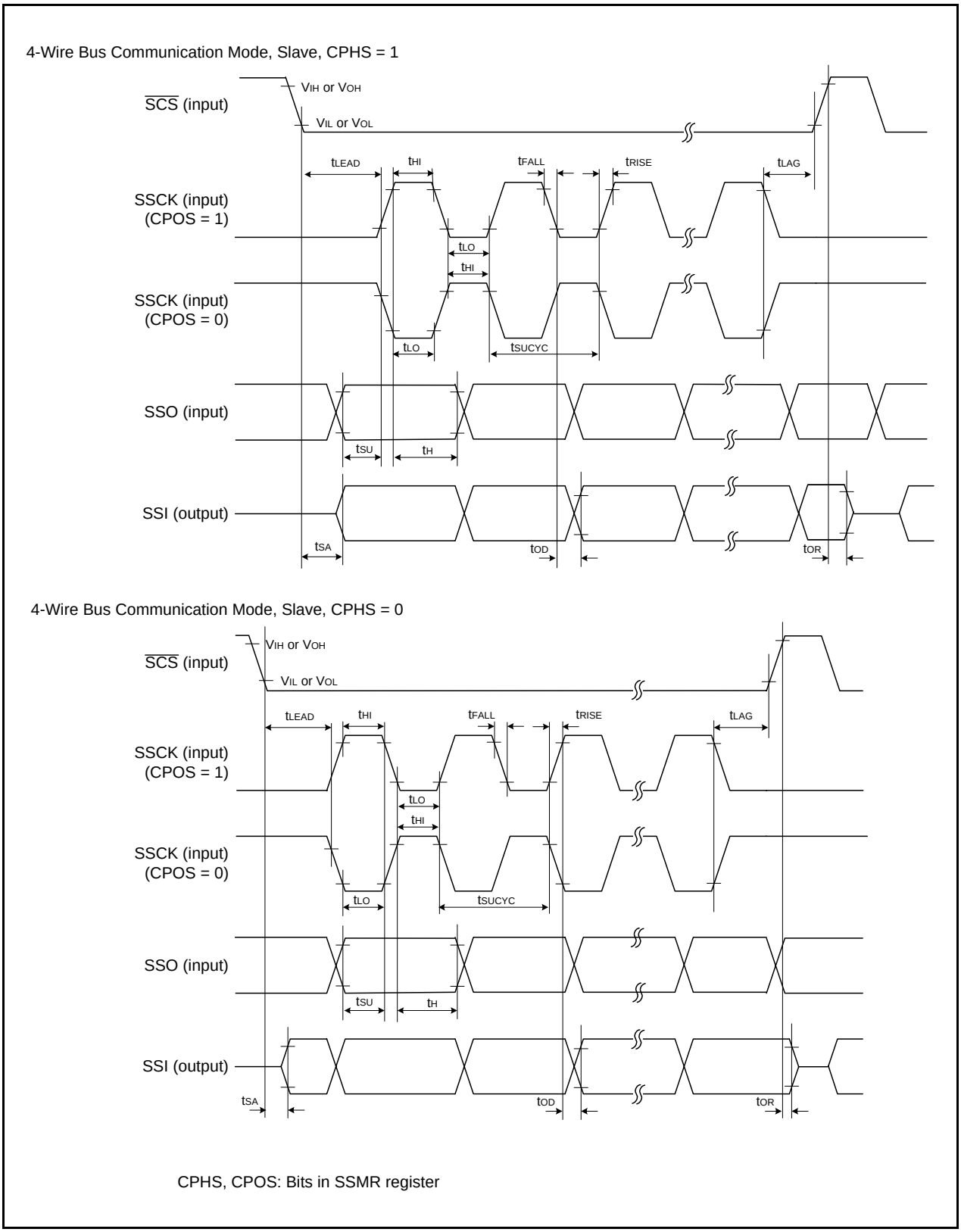


Figure 31.28 I/O Timing of Synchronous Serial Communication Unit (SSU) (Slave)

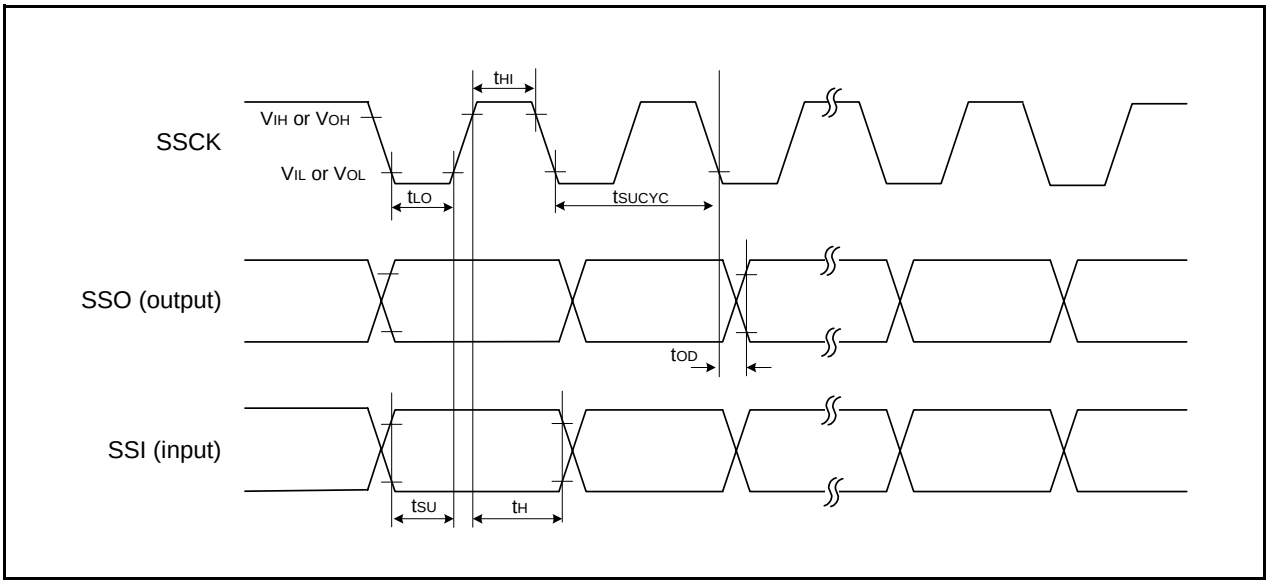
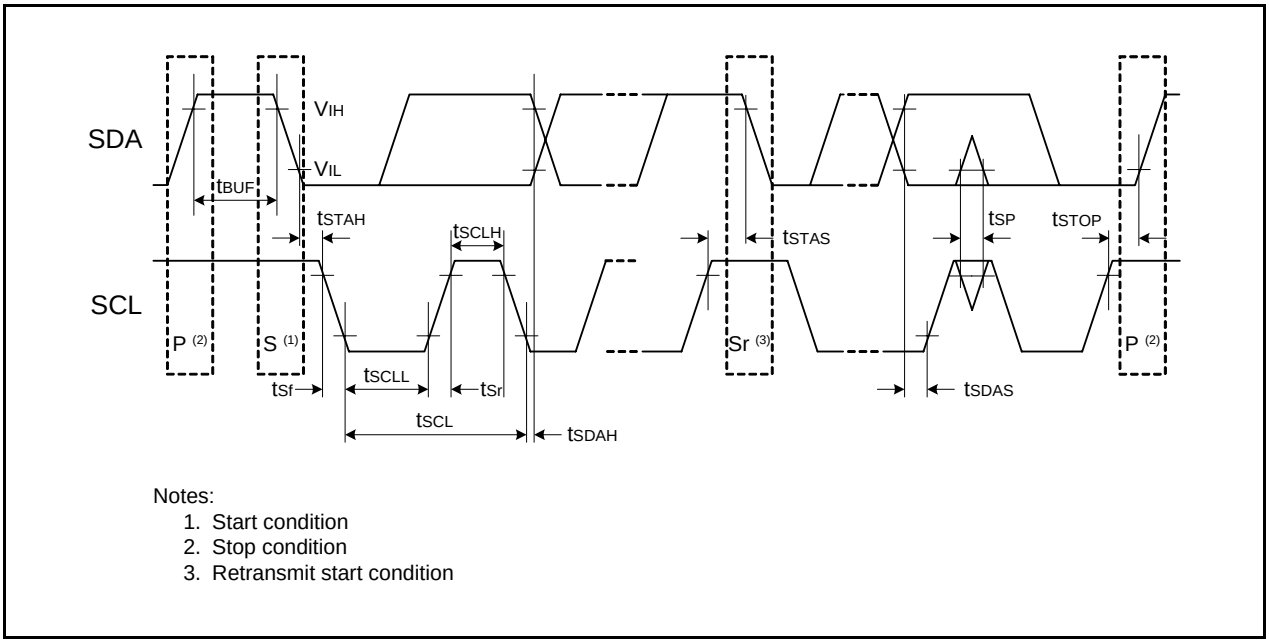


Figure 31.29 I/O Timing of Synchronous Serial Communication Unit (SSU) (Clock Synchronous Communication Mode)

Table 31.49 Timing Requirements of I²C bus Interface

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t_{SCL}	SCL input cycle time		$12t_{CYC} + 600$ (2)	—	—	ns
t_{SCLH}	SCL input “H” width		$3t_{CYC} + 300$ (2)	—	—	ns
t_{SCLL}	SCL input “L” width		$5t_{CYC} + 500$ (2)	—	—	ns
t_{sf}	SCL, SDA input fall time		—	—	300	ns
t_{SP}	SCL, SDA input spike pulse rejection time		—	—	$1t_{CYC}$ (2)	ns
t_{BUF}	SDA input bus-free time		$5t_{CYC}$ (2)	—	—	ns
t_{STAH}	Start condition input hold time		$3t_{CYC}$ (2)	—	—	ns
t_{STAS}	Retransmit start condition input setup time		$3t_{CYC}$ (2)	—	—	ns
t_{STOP}	Stop condition input setup time		$3t_{CYC}$ (2)	—	—	ns
t_{SDAS}	Data input setup time		$1t_{CYC} + 40$ (2)	—	—	ns
t_{SDAH}	Data input hold time		10	—	—	ns

Notes:
1. V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, and T_{opr} = –20 to 85 °C (N version), unless otherwise specified.
2. $1t_{CYC} = 1/f1(s)$



Notes:
1. Start condition
2. Stop condition
3. Retransmit start condition

Figure 31.30 I/O Timing of I²C bus Interface

Table 31.50 Electrical Characteristics (1) [4.2 V ≤ Vcc ≤ 5.5 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output "H" voltage	Other than XOUT	Drive capacity High V_{CC} = 5 V	I_{OH} = –20 mA	V_{CC} – 2.0	—	V_{CC}	V
			Drive capacity Low V_{CC} = 5 V	I_{OH} = –5 mA	V_{CC} – 2.0	—	V_{CC}	V
		XOUT	V_{CC} = 5 V	I_{OH} = –200 µA	1.0	—	V_{CC}	V
V_{OL}	Output "L" voltage	Other than XOUT	Drive capacity High V_{CC} = 5 V	I_{OL} = 20 mA	—	—	2.0	V
			Drive capacity Low V_{CC} = 5 V	I_{OL} = 5 mA	—	—	2.0	V
		XOUT	V_{CC} = 5 V	I_{OL} = 200 µA	—	—	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{INT4}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO,TRCIOA, TRCIOB, TRCIOC, TRCIOD, USB_OVRCURA, USB_VBUS, $\overline{TRCTRG}$, TRCCLK, $\overline{ADTRG}$, RXD0, RXD1, RXD2, RXD3, CLK0, $\overline{CLK1}$, CLK2, CLK3, $\overline{CTS2}$, SSI, SCL, SDA, SSO, SSCK, $\overline{SCS}$			0.1	1.2	—	V
		$\overline{RESET}$			0.1	1.2	—	V
I_{IH}	Input "H" current		V_I = 5 V, V_{CC} = 5.0 V		—	—	5.0	µA
I_{IL}	Input "L" current		V_I = 0 V, V_{CC} = 5.0 V		—	—	–5.0	µA
R_{PULLUP}	Pull-up resistance		V_I = 0 V, V_{CC} = 5.0 V		25	50	100	kΩ
R_{fXIN}	Feedback resistance	XIN			—	0.3	—	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

Note:
1. 4.2 V ≤ V_{CC} ≤ 5.5 V, T_{opr} = –20 to 85 °C (N version), and f(XIN) = 20 MHz, unless otherwise specified.

Table 31.51 Electrical Characteristics (2) [3.3 V ≤ Vcc ≤ 5.5 V] (Topr = –20 to 85 °C (N version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	6.5	15	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	5.3	12.5	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	3.6	—	mA
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	3.0	—	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	2.2	—	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	1.5	—	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	—	7.0	15	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	3.0	—	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-16, MSTIIC = MSTTRC = 1	—	1	—	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	—	90	400	µA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	15	100	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	4	90	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	3.5	—	µA
		Stop mode	XIN clock off, Topr = 25 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	—	2.0	5.0	µA
			XIN clock off, Topr = 85 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	—	15	—	µA

Timing Requirements (Unless Otherwise Specified: V_{CC} = 5 V, V_{SS} = 0 V, T_{opr} = 25 °C)

Table 31.52 External Clock Input (XOUT)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XOUT)}$	XOUT input cycle time	50	—	ns
$t_{WH(XOUT)}$	XOUT input “H” width	24	—	ns
$t_{WL(XOUT)}$	XOUT input “L” width	24	—	ns

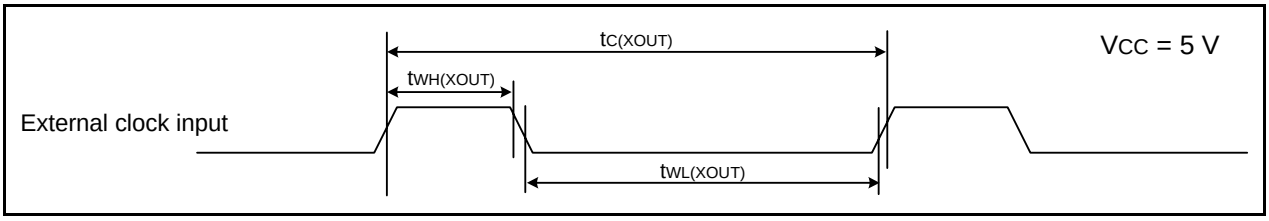


Figure 31.31 External Clock Input Timing Diagram when V_{CC} = 5 V

Table 31.53 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	100	—	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	40	—	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	40	—	ns

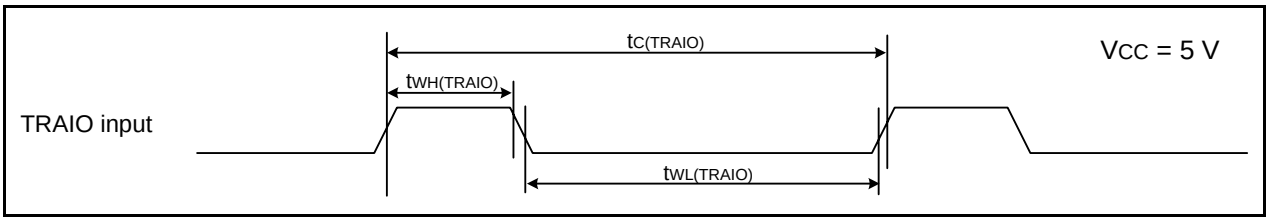


Figure 31.32 TRAIO Input Timing Diagram when V_{CC} = 5 V

Table 31.54 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200	—	ns
$t_{W(CKH)}$	CLKi input “H” width	100	—	ns
$t_{W(CKL)}$	CLKi input “L” width	100	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	50	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	50	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

i = 0 to 3

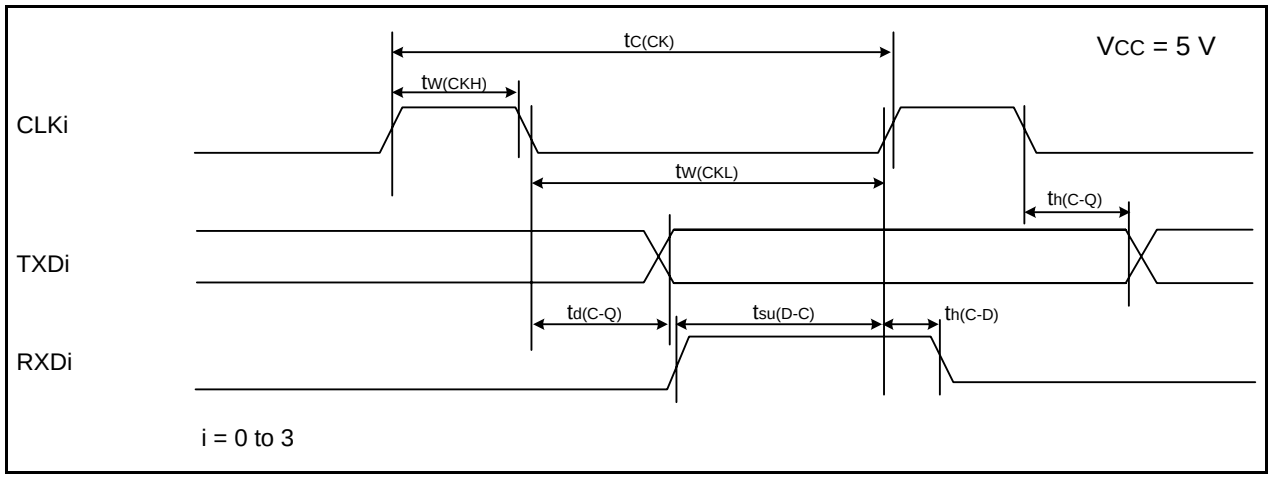


Figure 31.33 Serial Interface Timing Diagram when Vcc = 5 V

Table 31.55 External Interrupt $\overline{INTi}$ (i = 0 to 4) Input, Key Input Interrupt $\overline{KIi}$ (i = 0 to 3)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input “H” width, $\overline{KIi}$ input “H” width	250 (1)	—	ns
$t_{W(INL)}$	$\overline{INTi}$ input “L” width, $\overline{KIi}$ input “L” width	250 (2)	—	ns

Notes:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

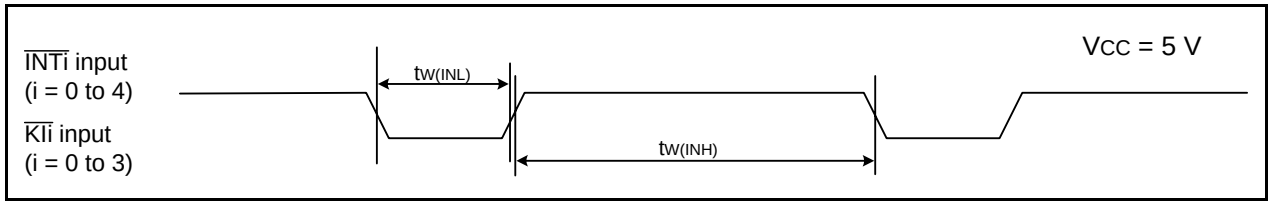


Figure 31.34 Input Timing Diagram for External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{KIi}$ when Vcc = 5 V

Table 31.56 Electrical Characteristics (3) [2.7 V ≤ Vcc < 4.2 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	Other than XOUT	Drive capacity High	I_{OH} = –5 mA	V_{CC} – 0.5	—	V_{CC}	V
			Drive capacity Low	I_{OH} = –1 mA	V_{CC} – 0.5	—	V_{CC}	V
		XOUT		I_{OH} = –200 μA	1.0	—	V_{CC}	V
V_{OL}	Output “L” voltage	Other than XOUT	Drive capacity High	I_{OL} = 5 mA	—	—	0.5	V
			Drive capacity Low	I_{OL} = 1 mA	—	—	0.5	V
		XOUT		I_{OL} = 200 μA	—	—	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{INT4}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, USB_OVRCURA, USB_VBUS, $\overline{TRCTRG}$, TRCCLK, $\overline{ADTRG}$, RXD0, RXD1, RXD2, RXD3, CLK0, $\overline{CLK1}$, CLK2, CLK3, $\overline{CTS2}$, SSI, SCL, $\overline{SDA}$, $\overline{SSO}$, SSCK, $\overline{SCS}$	V_{CC} = 3.0 V		0.1	0.4	—	V
		$\overline{RESET}$	V_{CC} = 3.0 V		0.1	0.5	—	V
I_{IH}	Input “H” current		V_I = 3 V, V_{CC} = 3.0 V		—	—	4.0	μA
I_{IL}	Input “L” current		V_I = 0 V, V_{CC} = 3.0 V		—	—	–4.0	μA
R_{PULLUP}	Pull-up resistance		V_I = 0 V, V_{CC} = 3.0 V		42	84	168	kΩ
R_{fXIN}	Feedback resistance	XIN			—	0.3	—	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

Note:
1. 2.7 V ≤ V_{CC} < 4.2 V, T_{opr} = –20 to 85 °C (N version), and f(XIN) = 10 MHz, unless otherwise specified.
2. 3.0 V ≤ VCC < 3.6 V for the USB associated pins.

Table 31.57 Electrical Characteristics (4) [2.7 V ≤ Vcc < 3.3 V]
(Topr = –20 to 85 °C (N version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode	XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	3.5	10	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	1.5	7.5	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	—	7.0	15	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	3.0	—	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	—	4.0	—	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	1.5	—	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-16, MSTIIC = MSTTRC = 1	—	1	—	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	—	90	390	µA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	15	90	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	4	80	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	3.5	—	µA
		Stop mode	XIN clock off, Topr = 25 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	—	2.0	5.0	µA
			XIN clock off, Topr = 85 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	—	15	—	µA

Timing requirements (Unless Otherwise Specified: V_{CC} = 3 V, V_{SS} = 0 V, T_{opr} = 25 °C)

Table 31.58 External Clock Input (XOUT)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XOUT)}$	XOUT input cycle time	50	—	ns
$t_{WH(XOUT)}$	XOUT input “H” width	24	—	ns
$t_{WL(XOUT)}$	XOUT input “L” width	24	—	ns

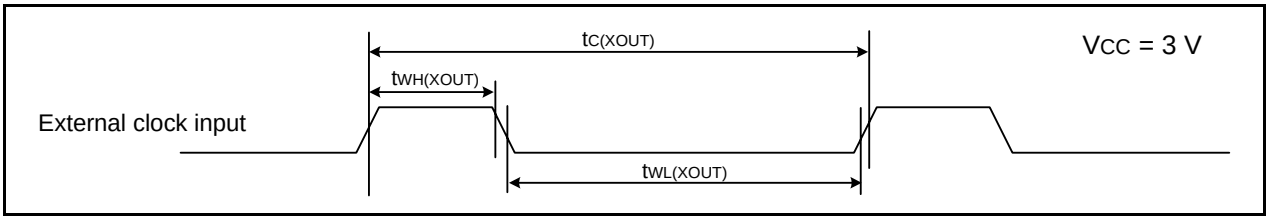


Figure 31.35 External Clock Input Timing Diagram when V_{CC} = 3 V

Table 31.59 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	300	—	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	120	—	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	120	—	ns

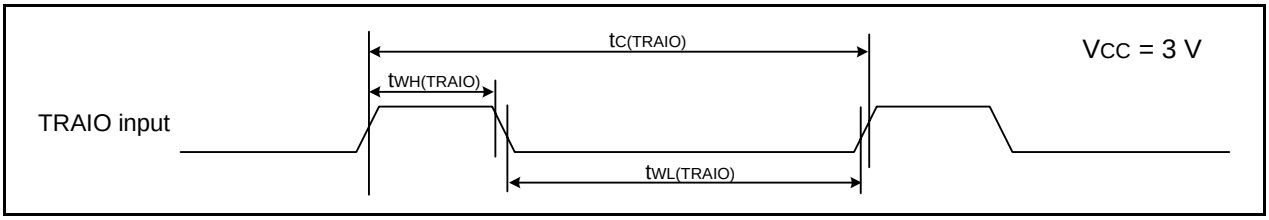


Figure 31.36 TRAIO Input Timing Diagram when V_{CC} = 3 V

Table 31.60 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300	—	ns
$t_{W(CKH)}$	CLKi input “H” width	150	—	ns
$t_{W(CKL)}$	CLKi Input “L” width	150	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	70	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

i = 0 to 3

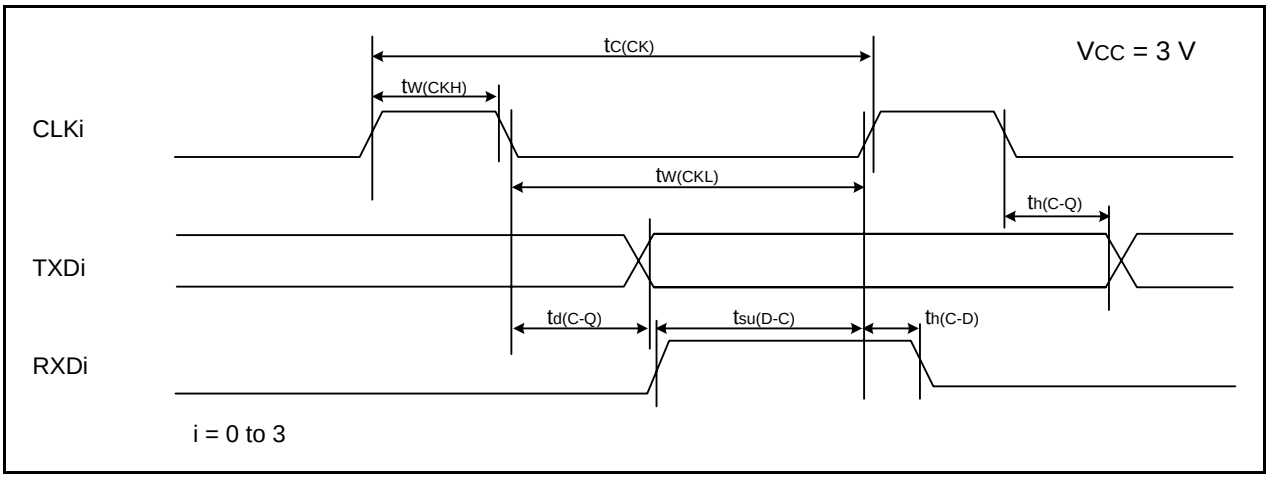


Figure 31.37 Serial Interface Timing Diagram when Vcc = 3 V

Table 31.61 External Interrupt $\overline{INTi}$ (i = 0 to 4) Input, Key Input Interrupt $\overline{KIi}$ (i = 0 to 3)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input “H” width, $\overline{KIi}$ input “H” width	380 (1)	—	ns
$t_{W(INL)}$	$\overline{INTi}$ input “L” width, $\overline{KIi}$ input “L” width	380 (2)	—	ns

Notes:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

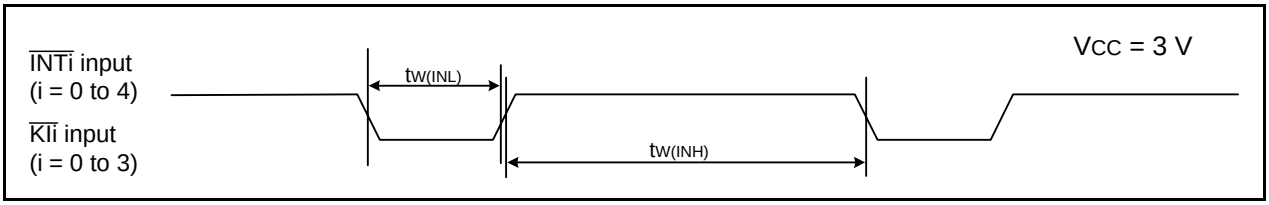


Figure 31.38 Input Timing Diagram for External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{KIi}$ when Vcc = 3 V

Table 31.62 Electrical Characteristics (5) [1.8 V ≤ Vcc < 2.7 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	Other than XOUT	Drive capacity High	I_{OH} = –2 mA	V_{CC} – 0.5	—	V_{CC}	V
			Drive capacity Low	I_{OH} = –1 mA	V_{CC} – 0.5	—	V_{CC}	V
		XOUT		I_{OH} = –200 μA	1.0	—	V_{CC}	V
V_{OL}	Output “L” voltage	Other than XOUT	Drive capacity High	I_{OL} = 2 mA	—	—	0.5	V
			Drive capacity Low	I_{OL} = 1 mA	—	—	0.5	V
		XOUT		I_{OL} = 200 μA	—	—	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{NT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{INT4}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, $\overline{TRCTRG}$, TRCCLK, $\overline{ADTRG}$, RXD0, RXD1, RXD2, RXD3, CLK0, $\overline{CLK1}$, CLK2, CLK3, $\overline{CTS2}$, SSI, SCL, SDA, SSO, SSCK, $\overline{SCS}$			0.05	0.20	—	V
		$\overline{RESET}$			0.05	0.20	—	V
I_{IH}	Input “H” current		V_I = 2.2 V, V_{CC} = 2.2 V		—	—	4.0	μA
I_{IL}	Input “L” current		V_I = 0 V, V_{CC} = 2.2 V		—	—	–4.0	μA
R_{PULLUP}	Pull-up resistance		V_I = 0 V, V_{CC} = 2.2 V		70	140	300	kΩ
R_{fXIN}	Feedback resistance	XIN			—	0.3	—	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

Note:
1. 1.8 V ≤ V_{CC} < 2.7 V, T_{opr} = –20 to 85 °C (N version), and f(XIN) = 5 MHz, unless otherwise specified.

Table 31.63 Electrical Characteristics (6) [1.8 V ≤ Vcc < 2.7 V] (Topr = –20 to 85 °C (N version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 1.8 to 2.7 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode	XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	—	2.2	—	mA
			XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	0.8	—	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO-F = 5 MHz Low-speed on-chip oscillator on = 125 kHz No division	—	2.5	10	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 5 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	—	1.7	—	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-16, MSTIIC = MSTTRC = 1	—	1	—	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	—	90	300	µA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	15	90	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	4	80	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	—	3.5	—	µA
		Stop mode	XIN clock off, Topr = 25 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	—	2.0	5	µA
			XIN clock off, Topr = 85 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	—	15	—	µA

Timing requirements (Unless Otherwise Specified: V_{CC} = 2.2 V, V_{SS} = 0 V, T_{opr} = 25 °C)

Table 31.64 External Clock Input (XOUT)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XOUT)}$	XOUT input cycle time	200	—	ns
$t_{WH(XOUT)}$	XOUT input “H” width	90	—	ns
$t_{WL(XOUT)}$	XOUT input “L” width	90	—	ns

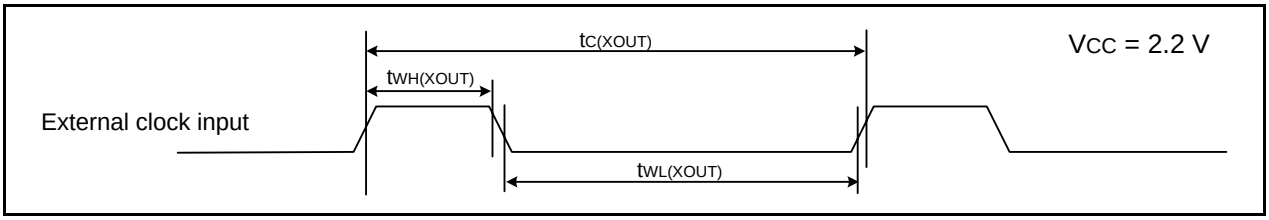


Figure 31.39 External Clock Input Timing Diagram when V_{CC} = 2.2 V

Table 31.65 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	500	—	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	200	—	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	200	—	ns

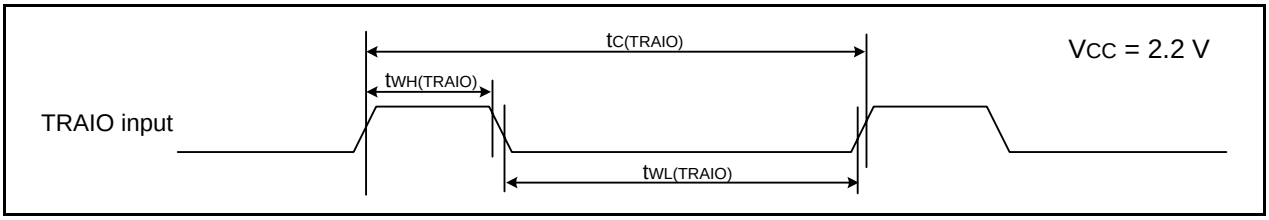


Figure 31.40 TRAIO Input Timing Diagram when V_{CC} = 2.2 V

Table 31.66 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	800	—	ns
$t_{W(CKH)}$	CLKi input “H” width	400	—	ns
$t_{W(CKL)}$	CLKi input “L” width	400	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	200	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	150	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

i = 0 to 3

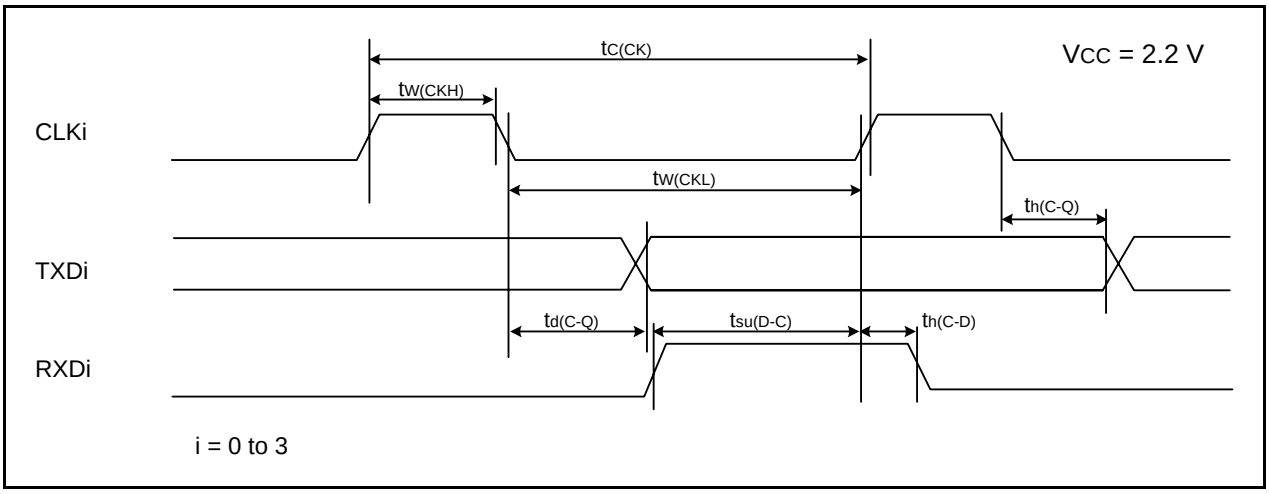


Figure 31.41 Serial Interface Timing Diagram when VCC = 2.2 V

Table 31.67 External Interrupt $\overline{INTi}$ (i = 0 to 4) Input, Key Input Interrupt $\overline{KIi}$ (i = 0 to 3)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input “H” width, $\overline{KIi}$ input “H” width	1000 (1)	—	ns
$t_{W(INL)}$	$\overline{INTi}$ input “L” width, $\overline{KIi}$ input “L” width	1000 (2)	—	ns

Notes:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

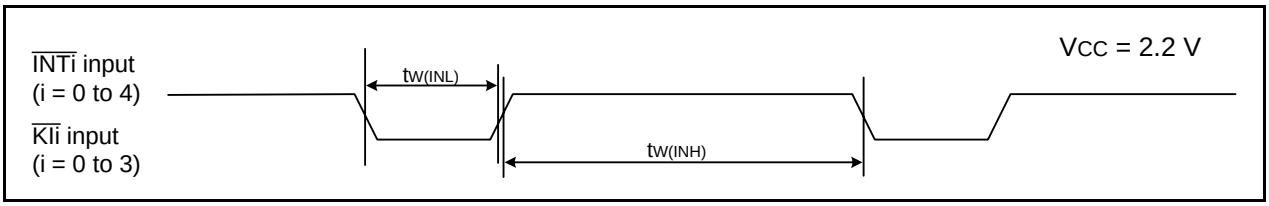


Figure 31.42 Input Timing Diagram for External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{KIi}$ when VCC = 2.2 V

32. Usage Notes

32.1 Notes on Clock Generation Circuit

32.1.1 Stop Mode

To enter stop mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) and then the CM10 bit in the CM1 register to 1 (stop mode). An instruction queue pre-reads 4 bytes from the instruction which sets the CM10 bit to 1 (stop mode) and the program stops.
Insert at least four NOP instructions following the JMP.B instruction after the instruction which sets the CM10 bit to 1.

• Program example to enter stop mode

```
        BCLR    1, FMR0     ; CPU rewrite mode disabled
        BCLR    7, FMR2     ; Low-current-consumption read mode disabled
        BSET    0, PRCR     ; Writing to CM1 register enabled
        FSET    I           ; Enable interrupt
        BSET    0, CM1      ; Stop mode
        JMP.B   LABEL_001
LABEL_001:
        NOP
        NOP
        NOP
        NOP
```

32.1.2 Wait Mode

To enter wait mode by setting the CM30 bit to 1, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) before setting the CM30 bit to 1.
To enter wait mode with the WAIT instruction, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) and then execute the WAIT instruction. An instruction queue pre-reads 4 bytes from the instruction to set the CM30 bit to 1 (MCU enters wait mode) or the WAIT instruction, and then the program stops. Insert at least four NOP instructions after the instruction to set the CM30 bit to 1 (MCU enters wait mode) or the WAIT instruction.

• Program example to execute the WAIT instruction

```
        BCLR    1, FMR0     ; CPU rewrite mode disabled
        BCLR    7, FMR2     ; Low-current-consumption read mode disabled
        FSET    I           ; Enable interrupt
        WAIT                ; Wait mode
        NOP
        NOP
        NOP
        NOP
```

• Program example to execute the instruction to set the CM30 bit to 1

```
        BCLR    1, FMR0     ; CPU rewrite mode disabled
        BCLR    7, FMR2     ; Low-current-consumption read mode disabled
        BSET    0, PRCR     ; Writing to CM3 register enabled
        FCLR    I           ; Interrupt disabled
        BSET    0, CM3      ; Wait mode
        NOP
        NOP
        NOP
        NOP
        BCLR    0, PRCR     ; Writing to CM3 register disabled
        FSET    I           ; Interrupt enabled
```

32.1.3 Oscillation Stop Detection Function

Since the oscillation stop detection function cannot be used if the XIN clock frequency is below 2 MHz, set bits OCD1 to OCD0 to 00b. In addition, the OCD3 bit cannot be used to confirm whether the XIN clock oscillation is stable.

32.1.4 Oscillation Circuit Constants

Consult the oscillator manufacturer to determine the optimal oscillation circuit constants for the user system.

32.2 Notes on Interrupts

32.2.1 Reading Address 00000h

Do not read address 00000h by a program. When a maskable interrupt request is acknowledged, the CPU reads interrupt information (interrupt number and interrupt request level) from 00000h in the interrupt sequence. At this time, the IR bit for the acknowledged interrupt is set to 0.
If address 00000h is read by a program, the IR bit for the interrupt which has the highest priority among the enabled interrupts is set to 0. This may cause the interrupt to be canceled, or an unexpected interrupt to be generated.

32.2.2 SP Setting

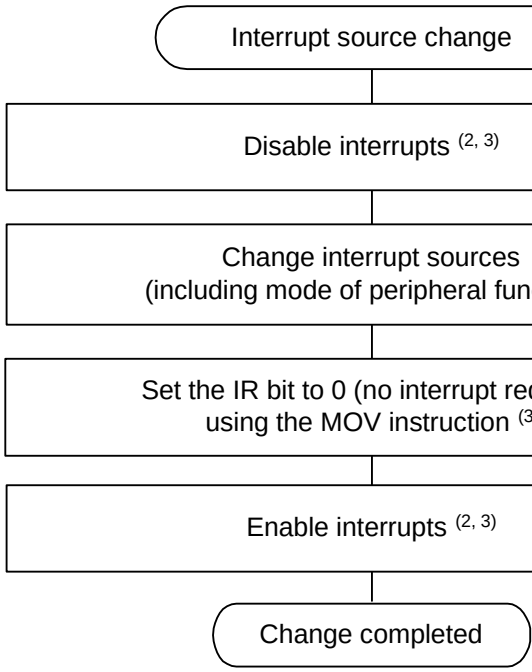
Set a value in the SP before an interrupt is acknowledged. The SP is set to 0000h after a reset. If an interrupt is acknowledged before setting a value in the SP, the program may run out of control.

32.2.3 External Interrupt and Key Input Interrupt

Either the “L” level width or “H” level width shown in the Electrical Characteristics is required for the signal input to pins $\overline{\text{INT0}}$ to $\overline{\text{INT4}}$ and pins $\overline{\text{KI0}}$ to $\overline{\text{KI3}}$, regardless of the CPU clock.
For details, refer to **Table 31.55** (VCC = 5 V), **Table 31.61** (VCC = 3 V), **Table 31.67** (VCC = 2.2 V) **External Interrupt $\overline{\text{INT}}$i (i = 0 to 4) Input, Key Input Interrupt $\overline{\text{KI}}$i (i = 0 to 3)**.

32.2.4 Changing Interrupt Sources

The IR bit in the interrupt control register may be set to 1 (interrupt requested) when the interrupt source changes. To use an interrupt, set the IR bit to 0 (no interrupt requested) after changing interrupt sources.
Changing interrupt sources as referred to here includes all factors that change the source, polarity, or timing of the interrupt assigned to a software interrupt number. Therefore, if a mode change of a peripheral function involves the source, polarity, or timing of an interrupt, set the IR bit to 0 (no interrupt requested) after making these changes. Refer to the descriptions of the individual peripheral functions for related interrupts.
Figure 32.1 shows a Procedure Example for Changing Interrupt Sources.



IR bit: The interrupt control register bit for the interrupt whose source is to be changed

Notes:
1. The above settings must be executed individually. Do not execute two or more settings simultaneously (using one instruction).
2. To prevent interrupt requests from being generated, disable the peripheral function before changing the interrupt source. In this case, use the I flag if all maskable interrupts can be disabled.
   If all maskable interrupts cannot be disabled, use bits ILVL0 to ILVL2 for the interrupt whose source is to be changed.
3. To change the interrupt source to the input with the digital filter used, wait for three or more cycles of the sampling clock of the digital filter before setting the IR bit to 0 (no interrupt request). Refer to **11.8.5 Rewriting Interrupt Control Register** for the instructions to use and related notes.

Figure 32.1 Procedure Example for Changing Interrupt Sources

32.2.5 Rewriting Interrupt Control Register

(a) The contents of the interrupt control register can be rewritten only while no interrupt requests corresponding to that register are generated. If an interrupt request may be generated, disable the interrupt before rewriting the contents of the interrupt control register.

(b) When rewriting the contents of the interrupt control register after disabling the interrupt, be careful to choose appropriate instructions.

Changing any bit other than the IR bit

If an interrupt request corresponding to the register is generated while executing the instruction, the IR bit may not be set to 1 (interrupt requested), and the interrupt may be ignored. If this causes a problem, use one of the following instructions to rewrite the contents of the register: AND, OR, BCLR, and BSET.

Changing the IR bit

Depending on the instruction used, the IR bit may not be set to 0 (no interrupt requested). Use the MOV instruction to set the IR bit to 0.

(c) When using the I flag to disable an interrupt, set the I flag as shown in the sample programs below. Refer to (b) regarding rewriting the contents of interrupt control registers using the sample programs.

Examples 1 to 3 shows how to prevent the I flag from being set to 1 (interrupts enabled) before the contents of the interrupt control register are rewritten for the effects of the internal bus and the instruction queue buffer.

Example 1: Use the NOP instructions to pause program until the interrupt control register is rewritten

```
INT_SWITCH1:
    FCLR    I               ; Disable interrupts
    AND.B   #00H, 0056H     ; Set the TRAIC register to 00h
    NOP                     ;
    NOP
    FSET    I               ; Enable interrupts
```

Example 2: Use a dummy read to delay the FSET instruction

```
INT_SWITCH2:
    FCLR    I               ; Disable interrupts
    AND.B   #00H, 0056H     ; Set the TRAIC register to 00h
    MOV.W   MEM, R0         ; Dummy read
    FSET    I               ; Enable interrupts
```

Example 3: Use the POPC instruction to change the I flag

```
INT_SWITCH3:
    PUSHC   FLG
    FCLR    I               ; Disable interrupts
    AND.B   #00H, 0056H     ; Set the TRAIC register to 00h
    POPC    FLG             ; Enable interrupts
```

32.3 Notes on ID Code Areas

32.3.1 Setting Example of ID Code Areas

The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. The following shows a setting example.

- To set 55h in all of the ID code areas

```
.org 00FFDCH
.lword dummy | (55000000h)   ; UND
.lword dummy | (55000000h)   ; INTO
.lword dummy                 ; BREAK
.lword dummy | (55000000h)   ; ADDRESS MATCH
.lword dummy | (55000000h)   ; SET SINGLE STEP
.lword dummy | (55000000h)   ; WDT
.lword dummy | (55000000h)   ; ADDRESS BREAK
.lword dummy | (55000000h)   ; RESERVE
```

(Programming formats vary depending on the compiler. Check the compiler manual.)

32.4 Notes on Option Function Select Area

32.4.1 Setting Example of Option Function Select Area

The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. The following shows a setting example.

- To set FFh in the OFS register

```
.org 00FFFCH
.lword reset | (0FF000000h)    ; RESET
```

(Programming formats vary depending on the compiler. Check the compiler manual.)

- To set FFh in the OFS2 register

```
.org 00FFDBH
.byte 0FFh
```

(Programming formats vary depending on the compiler. Check the compiler manual.)

32.5 Notes on DTC

32.5.1 DTC activation source

- Do not generate any DTC activation sources before entering wait mode or during wait mode.
- Do not generate any DTC activation sources before entering stop mode or during stop mode.

32.5.2 DTCENi (i = 0 to 3, 6) Registers

- Modify bits DTCENi0 to DTCENi7 only while an interrupt request corresponding to the bit is not generated.
- When the interrupt source flag in the status register for the peripheral function is 1, do not modify the corresponding activation source bit among bits DTCENi0 to DTCENi7.
- Do not access the DTCENi registers using DTC transfers.

32.5.3 Peripheral Modules

- Do not set the status register bit for the peripheral function to 0 using a DTC transfer.
- When the DTC activation source is SSU/I^{2}C bus receive data full, read the SSRDR register/the ICDRR register using a DTC transfer.
  The RDRF bit in the SSSR register/the ICSR register is set to 0 (no data in SSRDR/ICDRR register) by reading the SSRDR register/the ICDRR register.
  However, the RDRF bit is not set to 0 by reading the SSRDR register/the ICDRR register when the DTC data transfer setting is either of the following:
  -Transfer causing the DTCCTj (j = 0 to 23) register value to change from 1 to 0 in normal mode
  -Transfer causing the DTCCRj register value to change from 1 to 0 while the RPTINT bit in the DTCCRj register is 1 (interrupt generation enabled) in repeat mode.
- When the DTC activation source is SSU/I^{2}C bus transmit data empty, write to the SSTDR register/the ICDRT register using a DTC transfer. The TDRE bit in the SSSR register/the ICSR register is set to 0 (data is not transferred from registers SSTDR/ICDRT to SSTRSR/ICDRS) by writing to the SSTDR register/the ICDRT register.

32.5.4 Interrupt Request

No interrupt is generated for the CPU during DTC operation in any of the following cases:
- When the DTC activation source is SSU/I^{2}C transmit data empty or flash ready status
- When performing the data transfer causing the DTCCTj (j = 0 to 23) register value to change to 0 in normal mode
- When performing the data transfer causing the DTCCRj register value to change to 0 while the RPTINT bit in the DTCCRj register is 1 (interrupt generation enabled) in repeat mode

32.6 Notes on Timer RA

- Timer RA stops counting after a reset. Set the values in the timer RA and timer RA prescalers before the count starts.
- Even if the prescaler and timer RA are read out in 16-bit units, these registers are read 1 byte at a time by the MCU. Consequently, the timer value may be updated during the period when these two registers are being read.
- In pulse width measurement mode and pulse period measurement mode, bits TEDGF and TUNDF in the TRACR register can be set to 0 by writing 0 to these bits by a program. However, these bits remain unchanged if 1 is written. When using the READ-MODIFY-WRITE instruction for the TRACR register, the TEDGF or TUNDF bit may be set to 0 although these bits are set to 1 while the instruction is being executed. In this case, write 1 to the TEDGF or TUNDF bit which is not supposed to be set to 0 with the MOV instruction.
- When changing to pulse period measurement mode from another mode, the contents of bits TEDGF and TUNDF are undefined. Write 0 to bits TEDGF and TUNDF before the count starts.
- The TEDGF bit may be set to 1 by the first timer RA prescaler underflow generated after the count starts.
- When using the pulse period measurement mode, leave two or more periods of the timer RA prescaler immediately after the count starts, then set the TEDGF bit to 0.
- The TCSTF bit retains 0 (count stops) for 0 to 1 cycle of the count source after setting the TSTART bit to 1 (count starts) while the count is stopped.

  During this time, do not access registers associated with timer RA (1) other than the TCSTF bit. Timer RA starts counting at the first valid edge of the count source after the TCSTF bit is set to 1 (during count).

  The TCSTF bit remains 1 for 0 to 1 cycle of the count source after setting the TSTART bit to 0 (count stops) while the count is in progress. Timer RA counting is stopped when the TCSTF bit is set to 0.

  During this time, do not access registers associated with timer RA (1) other than the TCSTF bit.

  Note:
  1. Registers associated with timer RA: TRACR, TRAIOC, TRAMR, TRAPRE, and TRA.

- When the TRAPRE register is continuously written during count operation (TCSTF bit is set to 1), allow three or more cycles of the count source clock for each write interval.
- When the TRA register is continuously written during count operation (TCSTF bit is set to 1), allow three or more cycles of the prescaler underflow for each write interval.
- Do not set 00h to the TRA register in pulse width measurement mode and pulse period measurement mode.

32.7 Notes on Timer RB

- Timer RB stops counting after a reset. Set the values in the timer RB and timer RB prescalers before the count starts.
- Even if the prescaler and timer RB is read out in 16-bit units, these registers are read 1 byte at a time by the MCU. Consequently, the timer value may be updated during the period when these two registers are being read.
- In programmable one-shot generation mode and programmable wait one-shot generation mode, when setting the TSTART bit in the TRBCR register to 0 (stops counting) or setting the TOSSP bit in the TRBOCR register to 1 (stops one-shot), the timer reloads the value of reload register and stops. Therefore, in programmable one-shot generation mode and programmable wait one-shot generation mode, read the timer count value before the timer stops.
- The TCSTF bit remains 0 (count stops) for 1 to 2 cycles of the count source after setting the TSTART bit to 1 (count starts) while the count is stopped.
  During this time, do not access registers associated with timer RB (1) other than the TCSTF bit. Timer RB starts counting at the first valid edge of the count source after the TCSTF bit is set to 1 (during count).
  The TCSTF bit remains 1 for 1 to 2 cycles of the count source after setting the TSTART bit to 0 (count stops) while the count is in progress. Timer RB counting is stopped when the TCSTF bit is set to 0.
  During this time, do not access registers associated with timer RB (1) other than the TCSTF bit.

  Note:
  1. Registers associated with timer RB: TRBCR, TRBOCR, TRBIOC, TRBMR, TRBPRE, TRBSC, and TRBPR.

- If the TSTOP bit in the TRBCR register is set to 1 during timer operation, timer RB stops immediately.
- If 1 is written to the TOSST or TOSSP bit in the TRBOCR register, the value of the TOSSTF bit changes after one or two cycles of the count source have elapsed. If the TOSSP bit is written to 1 during the period between when the TOSST bit is written to 1 and when the TOSSTF bit is set to 1, the TOSSTF bit may be set to either 0 or 1 depending on the content state. Likewise, if the TOSST bit is written to 1 during the period between when the TOSSP bit is written to 1 and when the TOSSTF bit is set to 0, the TOSSTF bit may be set to either 0 or 1.
- To use the underflow signal of timer RA as the count source for timer RB, set timer RA in timer mode, pulse output mode, or event count mode.

32.7.1 Timer Mode

To write to registers TRBPRE and TRBPR during count operation (TCSTF bit in the TRBCR register is set to 1), note the following points:

- When the TRBPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

32.7.2 Programmable Waveform Generation Mode

To write to registers TRBPRE and TRBPR during count operation (TCSTF bit in the TRBCR register is set to 1), note the following points:

- When the TRBPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

32.7.3 Programmable One-shot Generation Mode

To write to registers TRBPRE and TRBPR during count operation (TCSTF bit in the TRBCR register is set to 1), note the following points:

- When the TRBPRE register is written continuously during count operation (TCSTF bit is set to 1), allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously during count operation (TCSTF bit is set to 1), allow three or more cycles of the prescaler underflow for each write interval.

32.7.4 Programmable Wait One-shot Generation Mode

To write to registers TRBPRE and TRBPR during count operation (TCSTF bit in the TRBCR register is set to 1), note the following points:

- When the TRBPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

32.8 Notes on Timer RC

32.8.1 TRC Register

- The following note applies when the CCLR bit in the TRCCR1 register is set to 1 (clear TRC register at compare match with TRCGRA register).
  When using a program to write a value to the TRC register while the TSTART bit in the TRCMR register is set to 1 (count starts), ensure that the write does not overlap with the timing with which the TRC register is set to 0000h.
  If the timing of the write to the TRC register and the setting of the TRC register to 0000h coincide, the write value will not be written to the TRC register and the TRC register will be set to 0000h.

- Reading from the TRC register immediately after writing to it can result in the value previous to the write being read out. To prevent this, execute the JMP.B instruction between the read and the write instructions.

```
Program Example     MOV.W   #XXXXh, TRC    ; Write
                    JMP.B   L1             ; JMP.B instruction
                L1: MOV.W   TRC, DATA      ; Read
```

32.8.2 TRCSR Register

Reading from the TRCSR register immediately after writing to it can result in the value previous to the write being read out. To prevent this, execute the JMP.B instruction between the read and the write instructions.

```
Program Example     MOV.B   #XXh, TRCSR    ; Write
                    JMP.B   L1             ; JMP.B instruction
                L1: MOV.B   TRCSR, DATA    ; Read
```

32.8.3 TRCCR1 Register

To set bits TCK2 to TCK0 in the TRCCR1 register to 111b (fOCO-F), set fOCO-F to the clock frequency higher than the CPU clock frequency.

32.8.4 Count Source Switching

- Stop the count before switching the count source.

Switching procedure
(1) Set the TSTART bit in the TRCMR register to 0 (count stops).
(2) Change the settings of bits TCK2 to TCK0 in the TRCCR1 register.

- After switching the count source from fOCO40M to another clock, allow a minimum of two cycles of f1 to elapse after changing the clock setting before stopping fOCO40M.

Switching procedure
(1) Set the TSTART bit in the TRCMR register to 0 (count stops).
(2) Change the settings of bits TCK2 to TCK0 in the TRCCR1 register.
(3) Wait for a minimum of two cycles of f1.
(4) Set the FRA00 bit in the FRA0 register to 0 (high-speed on-chip oscillator off).

• After switching the count source from fOCO-F to fOCO40M, allow a minimum of two cycles of fOCO-F to elapse after changing the clock setting before stopping fOCO-F.

Switching procedure

(1) Set the TSTART bit in the TRCMR register to 0 (count stops).
(2) Change the settings of bits TCK2 to TCK0 in the TRCCR1 register.
(3) Wait for a minimum of two cycles of fOCO-F.
(4) Set the FRA00 bit in the FRA0 register to 0 (high-speed on-chip oscillator off).

• After switching the count source from fOCO-F to a clock other than fOCO40M, allow a minimum of one cycle of fOCO-F + fOCO40M to elapse after changing the clock setting before stopping fOCO-F.

Switching procedure

(1) Set the TSTART bit in the TRCMR register to 0 (count stops).
(2) Change the settings of bits TCK2 to TCK0 in the TRCCR1 register.
(3) Wait for a minimum of one cycle of fOCO-F + fOCO40M.
(4) Set the FRA00 bit in the FRA0 register to 0 (high-speed on-chip oscillator off).

32.8.5 Input Capture Function

• Set the pulse width of the input capture signal as follows:
[When the digital filter is not used]
Three or more cycles of the timer RC operation clock (refer to **Table 19.1 Timer RC Operation Clocks**)
[When the digital filter is used]
Five cycles of the digital filter sampling clock + three cycles of the timer RC operating clock, minimum (refer to **Figure 19.5 Digital Filter Block Diagram**)
• The value of the TRC register is transferred to the TRCGRj register one or two cycles of the timer RC operation clock after the input capture signal is input to the TRCIOj (j = A, B, C, or D) pin (when the digital filter function is not used).

32.8.6 TRCMR Register in PWM2 Mode

When the CSEL bit in the TRCCR2 register is set to 1 (count stops at compare match with the TRCGRA register), do not set the TRCMR register at compare match timing of registers TRC and TRCGRA.

32.8.7 Count Source fOCO40M

The count source fOCO40M can be used with supply voltage VCC = 2.7 to 5.5 V. For supply voltage other than that, do not set bits TCK2 to TCK0 in the TRCCR1 register to 110b (select fOCO40M as the count source).

32.9 Notes on Serial Interface (UARTi (i = 0, 1, 3))

• When reading data from the UiRB (i = 0, 1, 3) register either in clock synchronous serial I/O mode or in clock asynchronous serial I/O mode, always read data in 16-bit units.
When the high-order byte of the UiRB register is read, bits PER and FER in the UiRB register and the RI bit in the UiC1 register are set to 0.
To check receive errors, read the UiRB register and then use the read data.

Program example to read the receive buffer register:

```
MOV.W    00A6H, R0    ; Read the U0RB register
```

• When writing data to the UiTB register in clock asynchronous serial I/O mode with 9-bit transfer data length, write data to the high-order byte first and then the low-order byte, in 8-bit units.

Program example to write to the transmit buffer register:

```
MOV.B    #XXH, 00A3H  ; Write to the high-order byte of the U0TB register
MOV.B    #XXH, 00A2H  ; Write to the low-order byte of the U0TB register
```

32.10 Notes on Serial Interface (UART2)

32.10.1 Clock Synchronous Serial I/O Mode

32.10.1.1 Transmission/Reception

When the $\overline{\text{RTS}}$ function is used with an external clock, the $\overline{\text{RTS2}}$ pin outputs “L,” which informs the transmitting side that the MCU is ready for a receive operation. The $\overline{\text{RTS2}}$ pin outputs “H” when a receive operation starts. Therefore, the transmit timing and receive timing can be synchronized by connecting the $\overline{\text{RTS2}}$ pin to the $\overline{\text{CTS2}}$ pin of the transmitting side. The $\overline{\text{RTS}}$ function is disabled when an internal clock is selected.

32.10.1.2 Transmission

If an external clock is selected, the following conditions must be met while the external clock is held high when the CKPOL bit in the U2C0 register is set to 0 (transmit data output at the falling edge and receive data input at the rising edge of the transfer clock), or while the external clock is held low when the CKPOL bit is set to 1 (transmit data output at the rising edge and receive data input at the falling edge of the transfer clock).

- The TE bit in the U2C1 register = 1 (transmission enabled)
- The TI bit in the U2C1 register = 0 (data present in the U2TB register)
- If the $\overline{\text{CTS}}$ function is selected, input on the $\overline{\text{CTS2}}$ pin = “L”

32.10.1.3 Reception

In clock synchronous serial I/O mode, the shift clock is generated by activating the transmitter. Set the UART2-associated registers for transmit operation even if the MCU is used for receive operation only. Dummy data is output from the TXD2 pin while receiving.

When an internal clock is selected, the shift clock is generated by setting the TE bit in the U2C1 register to 1 (transmission enabled) and placing dummy data in the U2TB register. When an external clock is selected, set the TE bit to 1 (transmission enabled), place dummy data in the U2TB register, and input an external clock to the CLK2 pin to generate the shift clock.

If data is received consecutively, an overrun error occurs when the RE bit in the U2C1 register is set to 1 (data present in the U2RB register) and the next receive data is received in the UART2 receive register. Then, the OER bit in the U2RB register is set to 1 (overrun error). At this time, the U2RB register value is undefined. If an overrun error occurs, the IR bit in the S2RIC register remains unchanged.

To receive data consecutively, set dummy data in the low-order byte in the U2TB register per each receive operation.

If an external clock is selected, the following conditions must be met while the external clock is held high when the CKPOL bit is set to 0, or while the external clock is held low when the CKPOL bit is set to 1.

- The RE bit in the U2C1 register = 1 (reception enabled)
- The TE bit in the U2C1 register = 1 (transmission enabled)
- The TI bit in the U2C1 register = 0 (data present in the U2TB register)

32.11 Notes on Synchronous Serial Communication Unit

Set the IICSEL bit in the SSUIICSR register to 0 (select SSU function) to use the synchronous serial communication unit function.

32.12 Notes on I²C bus Interface

To use the I²C bus interface, set the IICSEL bit in the SSUIICSR register to 1 (I²C bus interface function selected).

32.12.1 Master Receive Mode

After a master receive operation is completed, when a stop condition generation or a start condition regeneration overlaps with the falling edge of the ninth clock cycle of SCL, an additional cycle is output after the ninth clock cycle.

32.12.1.1 Countermeasure

After a master receive operation is completed, confirm the falling edge of the ninth clock cycle of SCL and generate a stop condition or regenerate a start condition.
Confirm the falling edge of the ninth clock cycle of SCL as follows: Confirm the SCLO bit in the ICCR2 register (SCL monitor flag) becomes 0 (SCL pin is low) after confirming the RDRF bit in the ICSR register (receive data register full flag) becomes 1.

32.12.2 The ICE Bit in the ICCR1 Register and the IICRST Bit in the ICCR2 Register

When writing 0 to the ICE bit or 1 to the IICRST bit during an I^2C bus interface operation, the BBSY bit in the ICCR2 register and the STOP bit in the ICSR register may become undefined.

32.12.2.1 Conditions When Bits Become Undefined

- When this module occupies the bus in master transmit mode (bits MST and TRS in the ICCR1 register are 1).
- When this module occupies the bus in master receive mode (the MST bit is 1 and the TRS bit is 0).
- When this module transmits data in slave transmit mode (the MST bit is 0 and the TRS bit is 1).
- When this module transmits an acknowledge in slave receive mode (bits MST and TRS are 0).

32.12.2.2 Countermeasures

- When the start condition (the SDA falling edge when SCL is high) is input, the BBSY bit becomes 1.
- When the stop condition (the SDA rising edge when SCL is high) is input, the BBSY bit becomes 0.
- When writing 1 to the BBSY bit, 0 to the SCP bit, and the start condition (the SDA falling edge when SCL is high) is output while SCL and SDA are high in master transmit mode, the BBSY bit becomes 1.
- When writing 0 to bits BBSY and SCP, the stop condition (the SDA rising edge when SCL is high) is output while SDA is low, and this is the only module that holds SCL low in master transmit mode or master receive mode, the BBSY bit becomes 0.
- When writing 1 to the FS bit in the SAR register, the BBSY bit becomes 0.

32.12.2.3 Additional Descriptions Regarding the IICRST Bit

- When writing 1 to the IICRST bit, bits SDAO and SCLO in the ICCR2 register become 1.
- When writing 1 to the IICRST bit in master transmit mode and slave transmit mode, the TDRE bit in the ICSR register becomes 1.
- While the control block of the I2C bus interface is reset by setting the IICRST bit to 1, writing to bits BBSY, SCP, and SDAO is disabled. Write 0 to the IICRST bit before writing to the BBSY bit, SCP bit, or SDAO bit.
- Even when writing 1 to the IICRST bit, the BBSY bit does not become 0. However, the stop condition (the SDA rising edge when SCL is high) may be generated depending on the states of SCL and SDA and the BBSY bit may become 0. There may also be a similar effect on other bits.
- While the control block of the I2C bus interface is reset by setting the IICRST bit to 1, data transmission/reception is stopped. However, the function to detect the start condition, stop condition, or arbitration lost operates. The values in the ICCR1 register, ICCR2 register, or ICSR register may be updated depending on the signals applied to pins SCL and SDA.

32.13 Notes on Hardware LIN

For the time-out processing of the header and response fields, use another timer to measure the duration of time with a Synch Break detection interrupt as the starting point.

32.14 Notes on A/D Converter

- Write to the ADMOD register, the ADINSEL register, the ADCON0 register (other than ADST bit), the ADCON1 register, the OCVREFCR register when A/D conversion is stopped (before a trigger occurs).
- To use the A/D converter in repeat mode 0, repeat mode 1, or repeat sweep mode, select the frequency of the A/D converter operating clock ϕAD or more for the CPU clock during A/D conversion.
  Do not select fOCO-F as ϕAD.
- Connect 0.1 μF capacitor between the VREF pin and AVSS pin.
- Do not enter stop mode during A/D conversion.
- Do not enter wait mode during A/D conversion regardless of the state of the CM02 bit in the CM0 register (1: Peripheral function clock stops in wait mode or 0: Peripheral function clock does not stop in wait mode).
- Do not set the FMSTP bit in the FMR0 register to 1 (flash memory stops) during A/D conversion.
- Do not change the CKS2 bit in the ADMOD register while fOCO-F is stopped.
- During an A/D conversion operation, if the ADST bit in the ADCON0 register is set to 0 (A/D conversion stops) by a program to forcibly terminate A/D conversion, the conversion result of the A/D converter is undefined and no interrupt is generated. The value of the ADi register before A/D conversion may also be undefined.
  If the ADST bit is set to 0 by a program, do not use the value of all the ADi register.
- When the A/D converter is not used, power consumption can be reduced by setting the ADSTBY bit in the ADCON1 register to 0 (A/D operation stops (standby)) to shut off any analog circuit current flow.

32.15 Notes on Flash Memory

32.15.1 CPU Rewrite Mode

32.15.1.1 Prohibited Instructions

The following instructions cannot be used while the program ROM area is being rewritten in EW0 mode because they reference data in the flash memory: UND, INTO, and BRK.

32.15.1.2 Interrupts

Tables 32.1 to 32.3 show CPU Rewrite Mode Interrupts.

Table 32.1 CPU Rewrite Mode Interrupts (1)

Mode	Erase/ Write Target	Status	Maskable Interrupt
EW0	Data flash	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, interrupt handling is executed. If the FMR22 bit is set to 1 (erase-suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (erase-suspend request). The flash memory suspends auto-erasure after td(SR-SUS). If erase-suspend is required while the FMR22 bit is set to 0 (erase-suspend request disabled by interrupt request), set the FMR21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. Auto-erasure can be restarted by setting the FMR21 bit to 0 (erase restart).
		During auto-erasure (suspend disabled or FMR22 = 0)	Interrupt handling is executed while auto-erasure or auto-programming is being performed.
		During auto-programming	
	Program ROM	During auto-erasure (suspend enabled)	Usable by allocating a vector in RAM.
		During auto-erasure (suspend disabled)	
		During auto-programming	
EW1	Data flash	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, interrupt handling is executed. If the FMR22 bit is set to 1, the FMR21 bit is automatically set to 1. The flash memory suspends auto-erasure after td(SR-SUS). If erase-suspend is required while the FMR22 bit is set to 0, set the FMR21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. Auto-erasure can be restarted by setting the FMR21 bit to 0.
		During auto-erasure (suspend disabled or FMR22 = 0)	Interrupt handling is executed while auto-erasure or auto-programming is being performed.
		During auto-programming	
	Program ROM	During auto-erasure (suspend enabled)	Auto-erasure suspends after td(SR-SUS) and interrupt handling is executed. Auto-erasure can be restarted by setting the FMR21 bit to 0 after interrupt handling completes. While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written.
		During auto-erasure (suspend disabled or FMR22 = 0)	Auto-erasure and auto-programming have priority and interrupt requests are put on standby. Interrupt handling is executed after auto-erase and auto-program complete.
		During auto-programming	

FMR21, FMR22: Bits in FMR2 register

Table 32.2 CPU Rewrite Mode Interrupts (2)

Mode	Erase/ Write Target	Status	• Watchdog Timer • Oscillation Stop Detection • Voltage Monitor 2 • Voltage Monitor 1	• Undefined Instruction • INTO Instruction • BRK Instruction • Single Step • Address Match • Address Break (Note 1)
EW0	Data flash	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, interrupt handling is executed. If the FMR22 bit is set to 1 (erase-suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (erase-suspend request). The flash memory suspends auto-erasure after td(SR-SUS). If erase-suspend is required while the FMR22 bit is set to 0 (erase-suspend request disabled by interrupt request), set the FMR21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. Auto-erasure can be restarted by setting the FMR21 bit is set to 0 (erase restart).	When an interrupt request is acknowledged, interrupt handling is executed. If erase-suspend is required, set the FMR21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. Auto-erasure can be restarted by setting the FMR21 bit in the FMR2 register is set to 0 (erase restart).
		During auto-erasure (suspend disabled or FMR22 = 0)	Interrupt handling is executed while auto-erasure or auto-programming is being performed.	
		During auto-programming		
	Program ROM	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, auto-erasure or auto-programming is forcibly stopped immediately and the flash memory is reset. Interrupt handling starts when the flash memory restarts after the fixed period. Since the block during auto-erasure or the address during auto-programming is forcibly stopped, the normal value may not be read. After the flash memory restarts, execute auto-erasure again and ensure it completes normally. The watchdog timer does not stop during the command operation, so interrupt requests may be generated. Initialize the watchdog timer regularly using the erase-suspend function.	Not usable during auto-erasure or auto-programming.
		During auto-erasure (suspend disabled)		
		During auto-programming		

FMR21, FMR22: Bits in FMR2 register

Note:

1. Do not use a non-maskable interrupt while block 0 is being auto-erased because the fixed vector is allocated in block 0.

Table 32.3 CPU Rewrite Mode Interrupts (3)

Mode	Erase/ Write Target	Status	• Watchdog Timer • Oscillation Stop Detection • Voltage Monitor 2 • Voltage Monitor 1	• Undefined Instruction • INTO Instruction • BRK Instruction • Single Step • Address Match • Address Break (Note 1)
EW1	Data flash	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, interrupt handling is executed. If the FMR22 bit is set to 1 (erase-suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (erase-suspend request). The flash memory suspends auto-erasure after td(SR-SUS). If erase-suspend is required while the FMR22 bit is set to 0 (erase-suspend request disabled by interrupt request), set the FMR21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. Auto-erasure can be restarted by setting the FMR21 bit is set to 0 (erase restart).	When an interrupt request is acknowledged, interrupt handling is executed. If erase-suspend is required, set the FMR21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. Auto-erasure can be restarted by setting the FMR21 bit in the FMR2 register is set to 0 (erase restart).
		During auto-erasure (suspend disabled or FMR22 = 0)	Interrupt handling is executed while auto-erasure or auto-programming is being performed.	
		During auto-programming		
	Program ROM	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, auto-erasure or auto-programming is forcibly stopped immediately and the flash memory is reset. Interrupt handling starts when the flash memory restarts after the fixed period. Since the block during auto-erasure or the address during auto-programming is forcibly stopped, the normal value may not be read. After the flash memory restarts, execute auto-erasure again and ensure it completes normally. The watchdog timer does not stop during the command operation, so interrupt requests may be generated. Initialize the watchdog timer regularly using the erase-suspend function.	Not usable during auto-erasure or auto-programming.
		During auto-erasure (suspend disabled or FMR22 = 0)		
		During auto-programming		

FMR21, FMR22: Bits in FMR2 register

Note:

1. Do not use a non-maskable interrupt while block 0 is being auto-erased because the fixed vector is allocated in block 0.

32.15.1.3 How to Access

To set one of the following bits to 1, first write 0 and then 1 immediately. Disable interrupts and DTC activation between writing 0 and writing 1.
- The FMR01 bit or FMR02 bit in the FMR0 register
- The FMR13 bit in the FMR1 register
- The FMR20 bit, FMR22 bit, or FMR 27 bit in the FMR2 register

To set one of the following bits to 0, first write 1 and then 0 immediately. Disable interrupts and DTC activation between writing 1 and writing 0.
- The FMR14 bit, FMR15 bit, FMR16 bit, or FMR17 bit in the FMR1 register

32.15.1.4 Rewriting User ROM Area

In EW0 mode, if the supply voltage drops while rewriting any block in which a rewrite control program is stored, it may not be possible to rewrite the flash memory because the rewrite control program cannot be rewritten correctly. In this case, use standard serial I/O mode.

32.15.1.5 Programming

Do not write additions to the already programmed address.

32.15.1.6 Entering Stop Mode or Wait Mode

Do not enter stop mode or wait mode during erase-suspend.
If the FST7 bit in the FST register is set to 0 (busy (during programming or erasure execution), do not enter to stop mode or wait mode.
Do not enter stop mode or wait mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

32.15.1.7 Programming and Erasure Voltage for Flash Memory

To perform programming and erasure, use VCC = 2.7 to 5.5 V as the supply voltage. Do not perform programming and erasure at less than 2.7 V.

32.15.1.8 Block Blank Check

Do not execute the block blank check command during erase-suspend.

32.15.1.9 Low-Current-Consumption Read Mode

In low-speed on-chip oscillator mode, the current consumption when reading the flash memory can be reduced by setting the FMR27 bit in the FMR2 register to 1 (low-current-consumption read mode enabled).
Low-current-consumption read mode can be used when the CPU clock is set to either of the following:
- The CPU clock is set to the low-speed on-chip oscillator clock divided by 4, 8, or 16.

However, do not use low-current-consumption read mode when the frequency of the selected CPU clock is 3 kHz or below. After setting the divide ratio of the CPU clock, set the FMR27 bit to 1 (low-current-consumption read mode enabled).
To reduce the power consumption, refer to **30. Reducing Power Consumption**.
Enter wait mode or stop mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled).
Do not enter wait mode or stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

32.16 Notes on Noise

32.16.1 Inserting a Bypass Capacitor between VCC and VSS Pins as a Countermeasure against Noise and Latch-up

Connect a bypass capacitor (approximately 0.1 μF) using the shortest and thickest wire possible.

32.16.2 Countermeasures against Noise Error of Port Control Registers

During rigorous noise testing or the like, external noise (mainly power supply system noise) can exceed the capacity of the MCU's internal noise control circuitry. In such cases the contents of the port related registers may be changed.

As a firmware countermeasure, it is recommended that the port registers, port direction registers, and pull-up control registers be reset periodically. However, examine the control processing fully before introducing the reset routine as conflicts may be created between the reset routine and interrupt routines.

32.17 Note on Supply Voltage Fluctuation

After reset is deasserted, the supply voltage applied to the VCC pin must meet either or both the allowable ripple voltage Vr (vcc) or ripple voltage falling gradient dVr (vcc)/dt shown in Figure 32.2.

Symbol	Parameter	Standard			Unit
		Min.	Typ.	Max.	
Vr (vcc)	Allowable ripple voltage			0.1 VCC	V
dVr (vcc)/dt	Ripple voltage falling gradient			10	V/ms

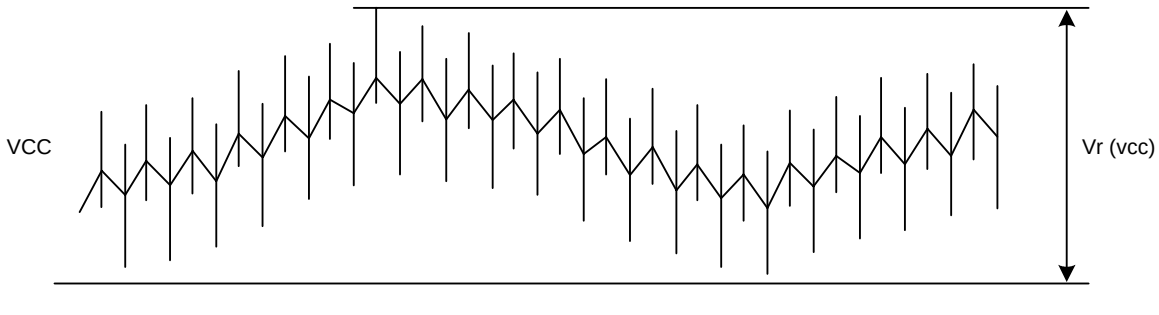


Figure 32.2 Definition of ripple voltage

33. Notes on On-Chip Debugger

When using the on-chip debugger to develop and debug programs for the R8C/3MU Group, R8C/3MK Group take note of the following.

(1) Some of the user flash memory and RAM areas are used by the on-chip debugger. These areas cannot be accessed by the user.
Refer to the on-chip debugger manual for which areas are used.
(2) Do not set the address match interrupt (registers AIER0, AIER1, RMAD0, and RMAD1 and fixed vector tables) in a user system.
(3) Do not use the BRK instruction in a user system.
(4) Debugging is available under the condition of supply voltage VCC = 1.8 to 5.5 V. Set the supply voltage to 2.7 V or above for rewriting the flash memory.
When using the USB, set the supply voltage in the range of 4.0 V ≤ VCC ≤ 5.5 V to use the USB internal power supply as the USB power supply, and 3.0 V ≤ VCC ≤ 3.6 V to use the power supply input from the USB_VCC pin.

Connecting and using the on-chip debugger has some special restrictions. Refer to the on-chip debugger manual for details.

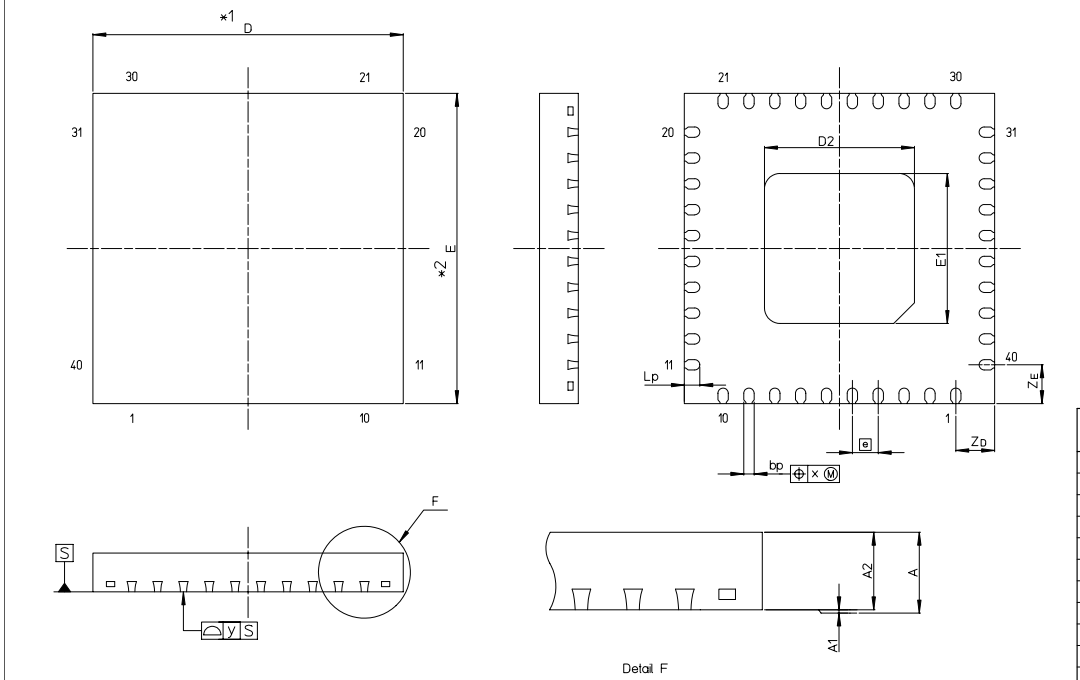
34. Notes on Emulator Debugger

Connecting and using the emulator debugger has some special restrictions. Refer to the emulator debugger manual for details.

Appendix 1. Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Electronics website.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-HWQFN40-6x6-0.50	PWQN0040KB-B	40PJS-B	0.07g

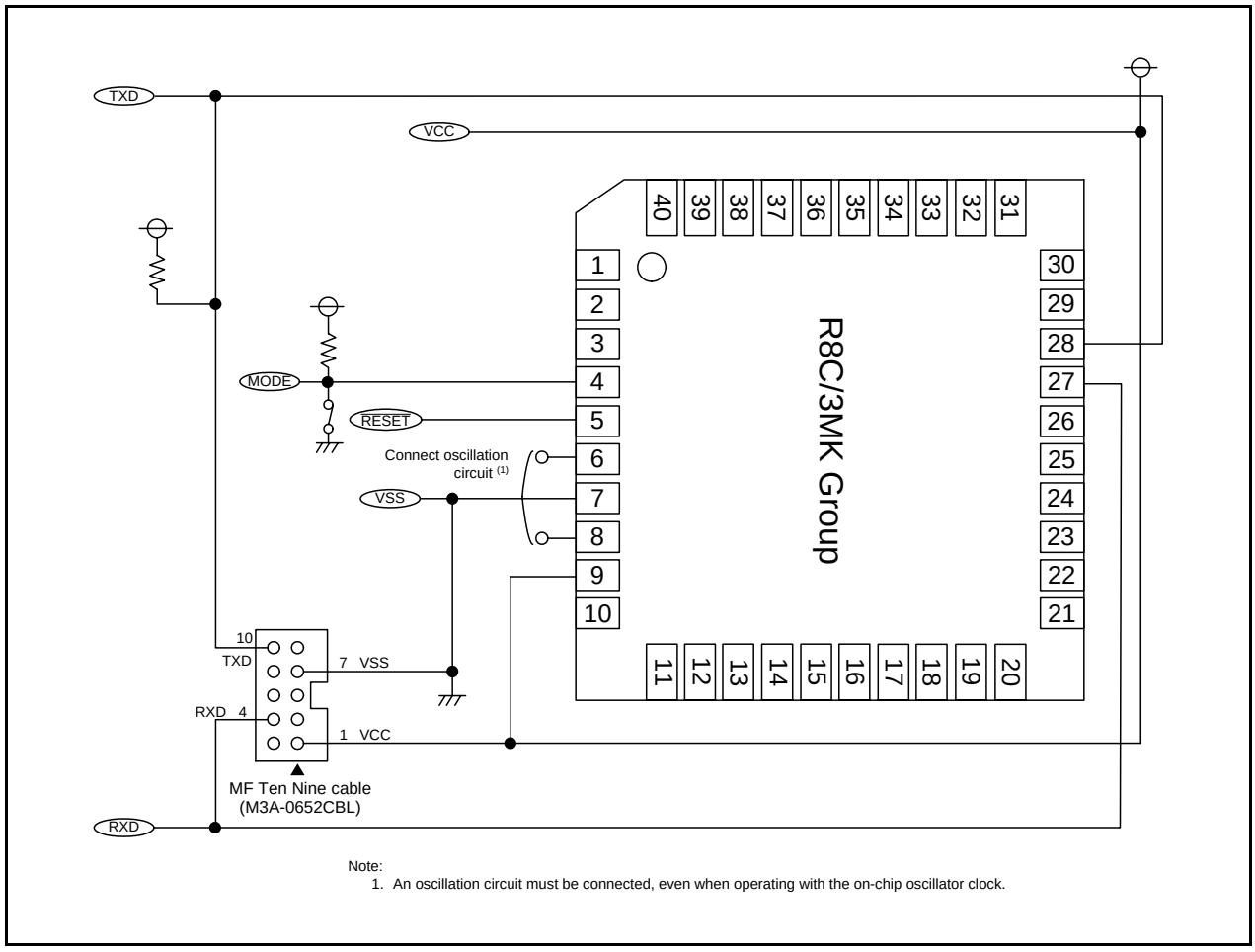


NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.

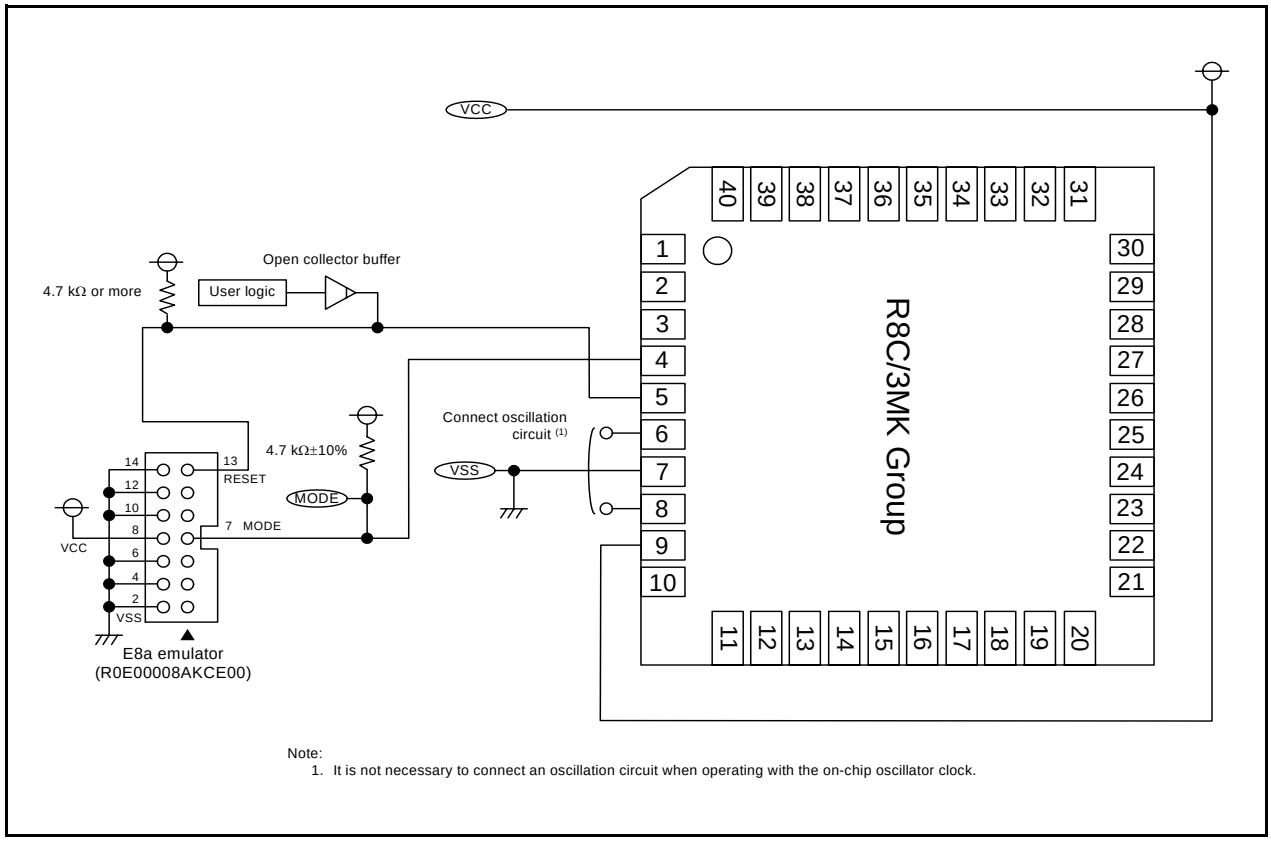
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	5.9	6.0	6.1
E	5.9	6.0	6.1
A2	—	0.75	—
A	—	—	0.8
A1	0	0	0.05
bp	0.15	0.2	0.25
e	—	0.5	—
Lp	0.2	0.3	0.4
x	—	—	0.05
y	—	—	0.05
ZD	—	0.75	—
ZE	—	0.75	—
D2	—	2.9	—
E1	—	2.9	—

Appendix 2. Connection Examples between Serial Programmer and On-Chip Debugging Emulator

Appendix Figure 2.1 shows a Connection Example with MF Ten Nine Cable (M3A-0652CBL) and Appendix Figure 2.2 shows a Connection Example with E8a Emulator (R0E00008AKCE00).



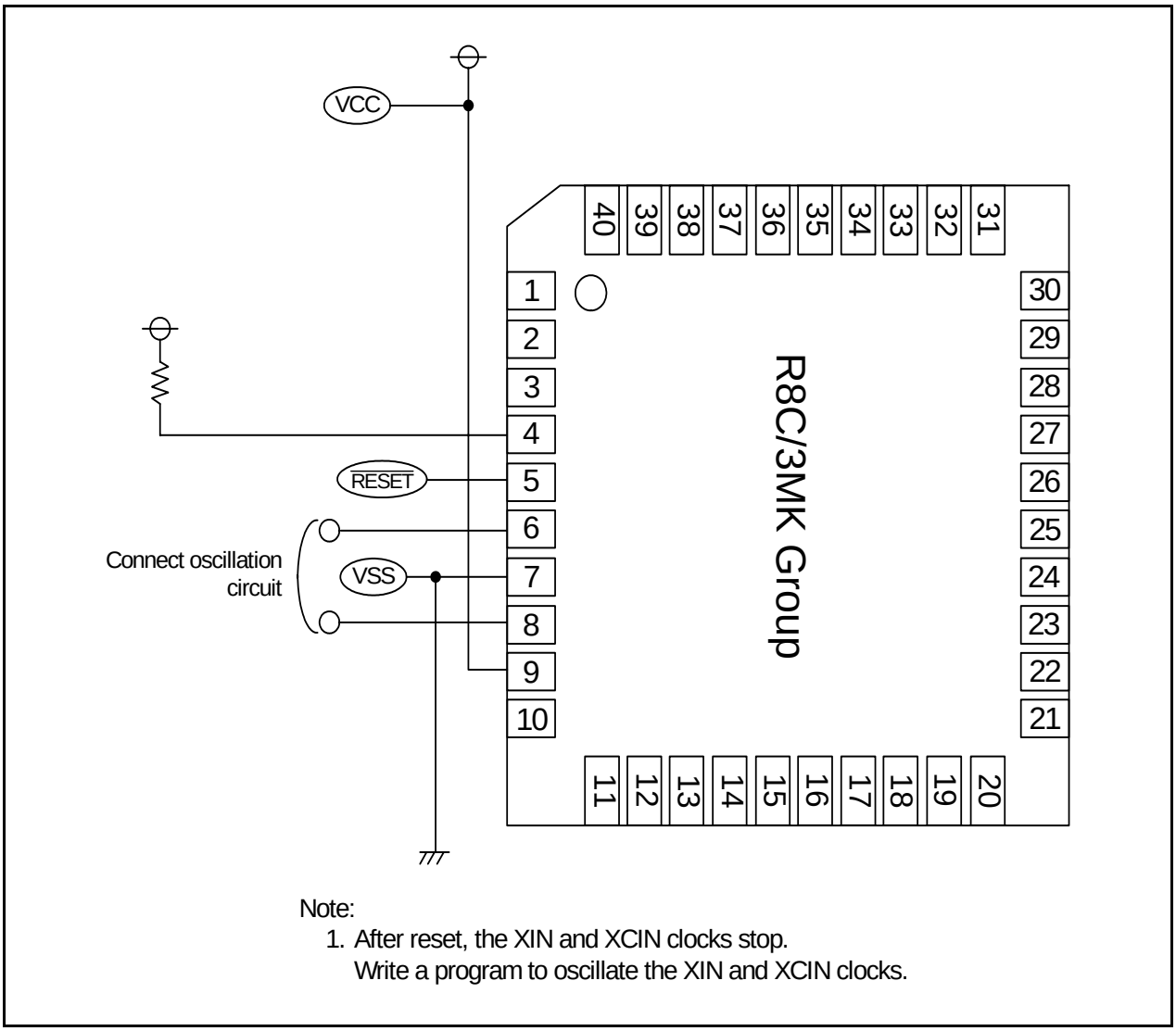
Appendix Figure 2.1 Connection Example with MF Ten Nine Cable (M3A-0652CBL)



Appendix Figure 2.2 Connection Example with E8a Emulator (R0E00008AKCE00)

Appendix 3. Example of Oscillation Evaluation Circuit

Appendix Figure 3.1 shows an Example of Oscillation Evaluation Circuit.



Note:
1. After reset, the XIN and XCIN clocks stop.
   Write a program to oscillate the XIN and XCIN clocks.

Appendix Figure 3.1 Example of Oscillation Evaluation Circuit

Index

REVISION HISTORY	R8C/3MU Group, R8C/3MK Group User's Manual: Hardware

Rev.	Date	Description	
		Page	Summary
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