CS51411DEMO/D

Demonstration Note for CS51411/3 5.0 V–16 V to 3.3 V/1.0 A Buck Regulator

ON Semiconductor™

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DEMONSTRATION NOTE

Description

The CS51411 demonstration board is a 1.0 A/3.3 V buck regulator running at 260 kHz (CS51411) or 520 kHz (CS51413). The switching frequency can be synchronized to a higher frequency through feeding clock signals to the SYNC input. Driving SHDNB input low shuts down the converter output and minimizes the power consumption. The regulator has superior line and load regulation due to the use of V^{2}™ control. This control method also enhances the load transient response.

Features

- V^2 Control for Superior Line and Load Regulation
- Small Board Space Requiring Only 1.0×0.7 in.^{2}
- Total of 11 Components Including IC
- Shutdown Mode Disables the Output and Reduces the Operating Current
- Frequency Synchronization to Higher Frequency
- 1.5 A Peak Current Protection which Folds Back 30% During Overload Conditions
- Built–In Soft Start to Eliminate Any In–Rush Current
- High Energy Transfer Efficiency of 83% at 1.0 A Load
- Line Regulation Better Than 0.1%
- Load Regulation Better Than 0.4%

Figure 1. CS51411/3 Demonstration Board

ABSOLUTE MAXIMUM RATINGS

Pin Name	Maximum Voltage	Maximum Current
V_{IN}	16 V	2.0 A
V_O	16 V	2.0 A
SHDNB	7.0 V	1.0 mA
SYNC	7.0 V	1.0 mA

ELECTRICAL CHARACTERISTICS (T_A = 25°C, 5.0 V ≤ V_{IN} ≤ 16 V, 0.1 A ≤ I_{OUT} ≤ 1.0 A, unless otherwise specified.)

Characteristic	Test Conditions	Typ	Unit
Output Voltage			
Voltage Accuracy	–	4.0	%
Line Regulation	I_{OUT} = 1.0 A	0.1	%
Load Regulation	V_{IN} = 5.0 V	0.3	%
Minimum Load	–	0.1	A
Transient Response	–	3.0	%
Transient Response Time	Load toggle between 0.1 A and 1.0 A	10	μs
Startup Time	–	5.0	ms
Input Voltage			
Start Threshold	–	3.3	V
Sync and Shutdown			
Sync Frequency	CS51411 CS51413	290 to 470 575 to 900	kHz kHz
Minimum Sync Threshold Voltage	–	1.0	V
Minimum Shutdown Threshold Voltage	–	0.3	V
Maximum Shutdown Bias Current	–	12	μA
General			
Switching Frequency	CS51411 CS51413	260 520	kHz kHz
Efficiency	I_{LOAD} = 100 mA I_{LOAD} = 1.0 A	77.5 83	% %
Shutdown Current	–	100	μA

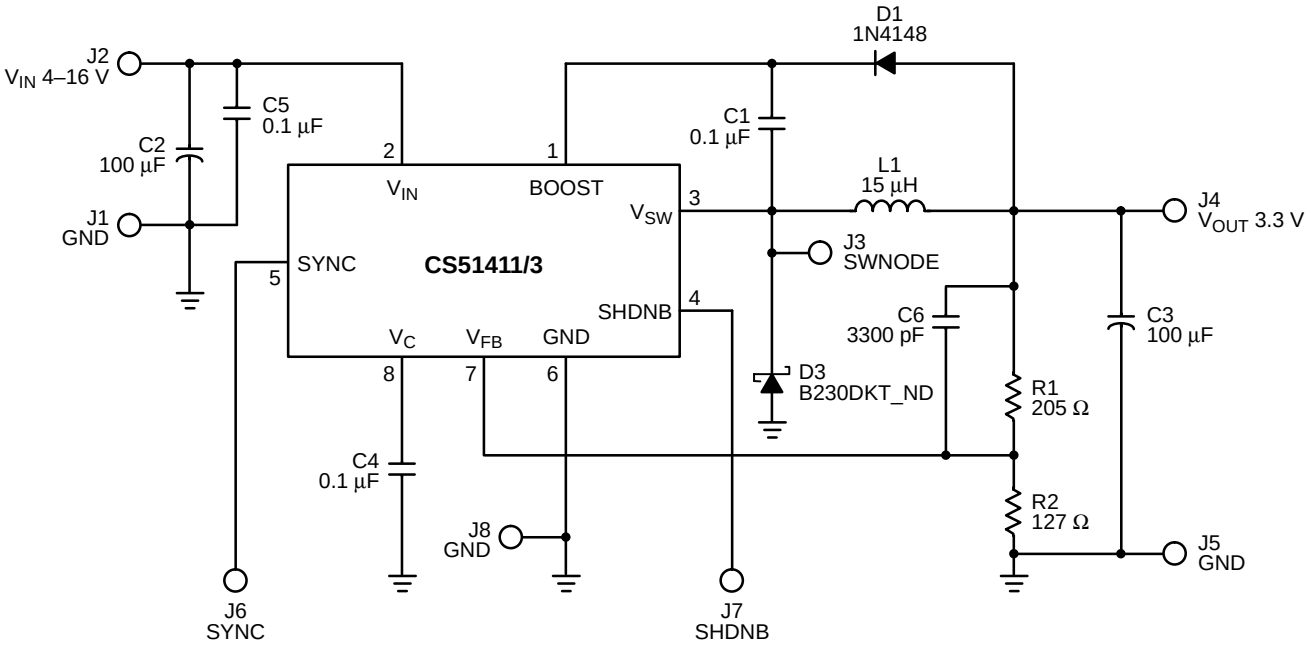

Figure 2. Application Diagram

Operation Guidelines

1. Connect input voltage between J2 and J1 on the left side of the board. The maximum input voltage is limited by the voltage rating of the input capacitor.
2. Connect the load between J4 and J5. The regulator requires 100 mA as minimum load. Without this minimum load, the output may exceed the regulation voltage.
3. Connect shutdown signal between J7 and J8. When the voltage on this input is below 0.3 V, the regulator enters a sleep mode. Pull this input high or leave it open if not used.
4. The sync signal can be applied between J6 and J8. The amplitude of the sync pulses needs to be greater than 1.0 V. The duty cycle can vary from 10% to 90%. Leave it open if not used.

Theory Of Operation

1. **Boost Strapping Circuit:** The boost strapping circuit, made of C1 and D1, provides a voltage higher than the input voltage to drive the power transistor (inside IC) into saturation. The operation of the boost strapping circuit works as follows. When the power transistor turns off, diode D3 turns on and pulls the V_{SW} node to ground. Diode D1 is forward biased, and the output voltage charges C1 to V_O. When the power transistor turns on, the V_{SW} node is pulled high and is approximately equal to V_{IN}. Now the voltage of the Boost pin, which connects to C1, is equal to $V_{IN} + V_O$. Diode D1 is reverse biased. The Boost pin voltage provides adequate base current to the power transistor, which lowers $V_{CE(SAT)}$ and improves the energy transfer efficiency.
2. **Soft Start:** The soft–start is implemented on the V_C pin. During the startup, the limited source current (25 μA) of the error amplifier charges the V_C pin capacitor. The rising slope of the V_C pin voltage clamps the duty cycle through the PWM comparator. The V_C pin voltage eventually settles down to a voltage roughly equal to the reference voltage 1.27 V. Therefore, the startup time can be easily calculated.
3. **Feedback Network:** V^2 control relies on the output ripple to provide pulse width modulation. When the output ripple is inadequate, pulse skipping or instability may be observed. Adding a capacitor C6 in parallel with R1 provides a low impedance pass for the output ripple. Therefore, the output ripple is not attenuated by the resistor divider. The use of this capacitor is optional.

Please see data sheet for more description on regulator operation and component selection (document number CS51411/D available through the Literature Distribution Center or via our website at http://www.onsemi.com).

TYPICAL PERFORMANCE CHARACTERISTICS

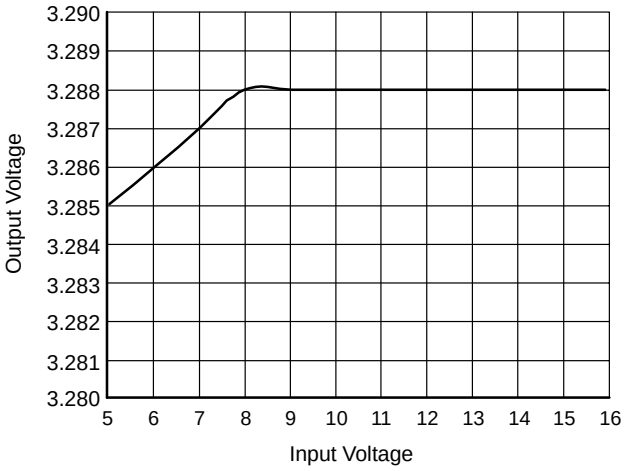

Figure 3. Line Regulation

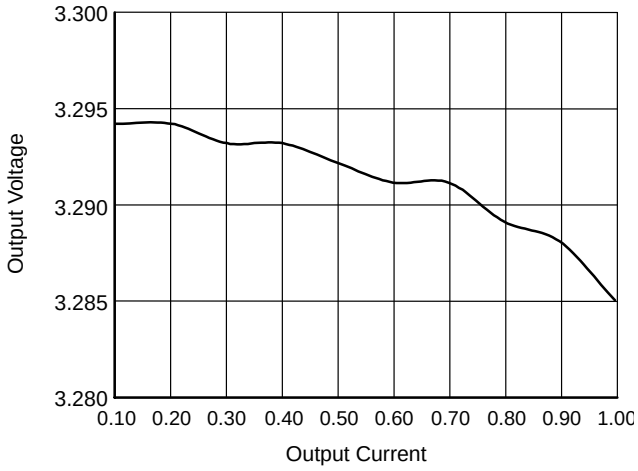

Figure 4. Load Regulation

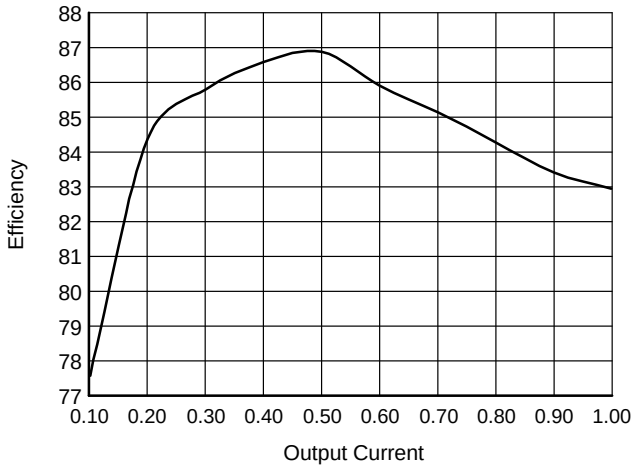

Figure 5. Efficiency vs. Output Current

BILL OF MATERIALS

Ref. Designator	Vendor	Part Number	Type	PC/Board
C1, C4, C5	DIGIKEY	PCC1762CT–ND	0.1 μF CERAMIC	3
C2, C3	AVX	TAJE107K016R	100 μF TANTALUM	2
C6	DIGIKEY	PCC1778CT–ND	3300 pF CERAMIC	1
D1	DIGIKEY	LL4148CT–ND	DIODE	1
D3	DIGIKEY	B230DICT–ND	2.0 A SCHOTTKY	1
J1–J8	DIGIKEY	V1055	TEST POINT	8
L1	COILTRONICS	UP2.8B150	15 μH INDUCTOR	1
R1	DIGIKEY	P205CTRND	205 Ω RESISTOR	1
R2	DIGIKEY	P127CTRND	127 Ω RESISTOR	1
U1	**ON SEMICONDUCTOR**	**CS51411/3**	**CONTROLLER**	**1**

DRAWINGS OF LAYERS

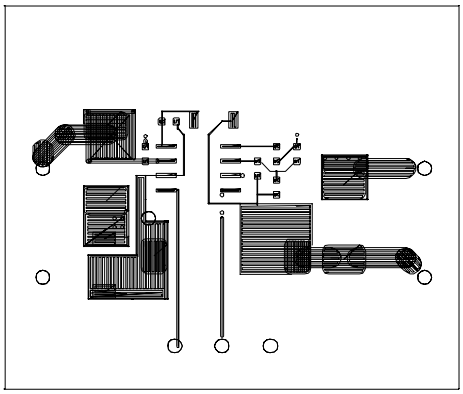

Figure 6. Top Copper

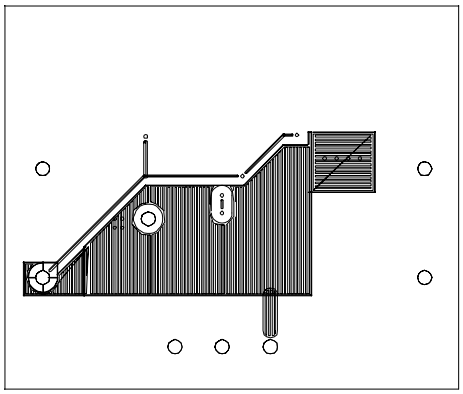

Figure 7. Bottom Copper

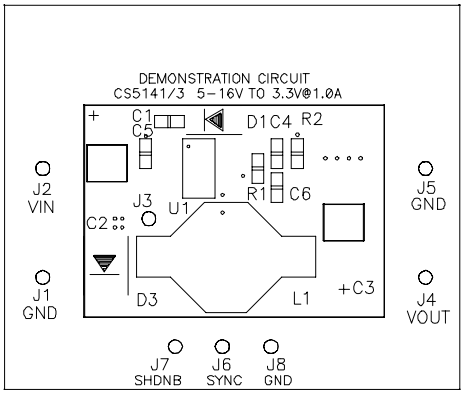

Figure 8. Top Silk

Notes

Notes

V^2 is a trademark of Switch Power, Inc.

PUBLICATION ORDERING INFORMATION

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