SPS Secondary-Side CC/CV Controller

General Description

The RT8481A is a secondary-side CC/CV controller for SPS applications. It integrates a Constant Current (CC) regulating amplifier, a Constant Voltage (CV) regulating amplifier, and 2 precision reference voltages.

The CC regulating amplifier is featured with an extended input common mode voltage below GND level to insure the performance of low-side current sense, and a very low input offset voltage to guarantee the sensing accuracy. A 60mV reference voltage is internally connected between the inverting input of the CC regulating amplifier and the CP pin. The non-inverting input is the CN pin, at which the voltage will be regulated 60mV higher than that at the CP pin. The inverting input pin CP is equiped with –5V anti-reverse immunity.

The CV regulating amplifier with low input offset voltage is biased with a 2.5V reference voltage at the inverting input. The non-inverting input is the FB pin, at which the voltage will be regulated with 2.5V from GND. The CC and CV amplifiers share an open-collector output pin to minimize application circuit.

The RT8481A is available in the SOT-23-6 package.

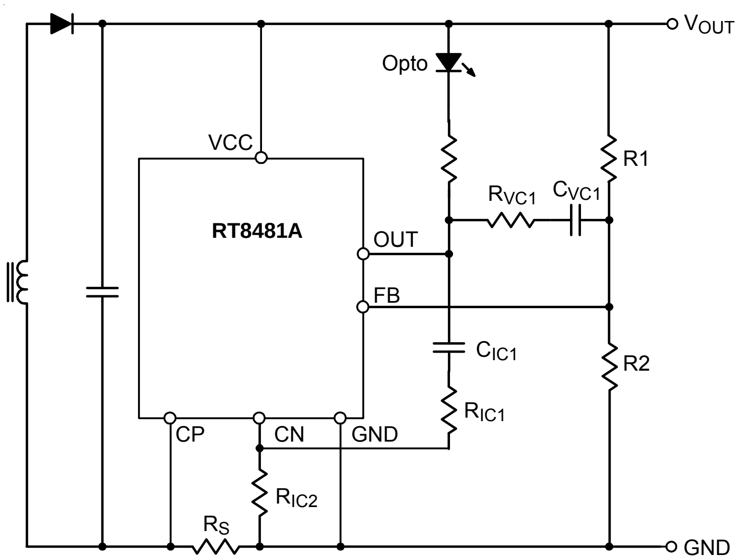
Features

- **Secondary-Side Constant Voltage (CV) and Constant Current (CC) Control**
- **4.75V to 50V Operation Voltage Range**
- **±1% Output Voltage Accuracy at Full Temperature Range**
- **0.6mA Quiescent Current**
- **Smooth Transition Between CC and CV Control Loops**
- **–5V Negative Voltage Tolerance at CP pin**

Applications

- Battery Chargers
- AC/DC Adaptors
- LED Drivers

Simplified Application Circuit



Ordering Information

RT8481A□□
- Package Type
  E : SOT-23-6
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

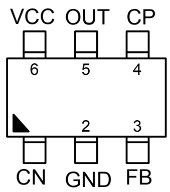
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

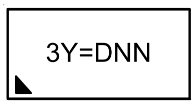
Pin Configurations

(TOP VIEW)



SOT-23-6

Marking Information



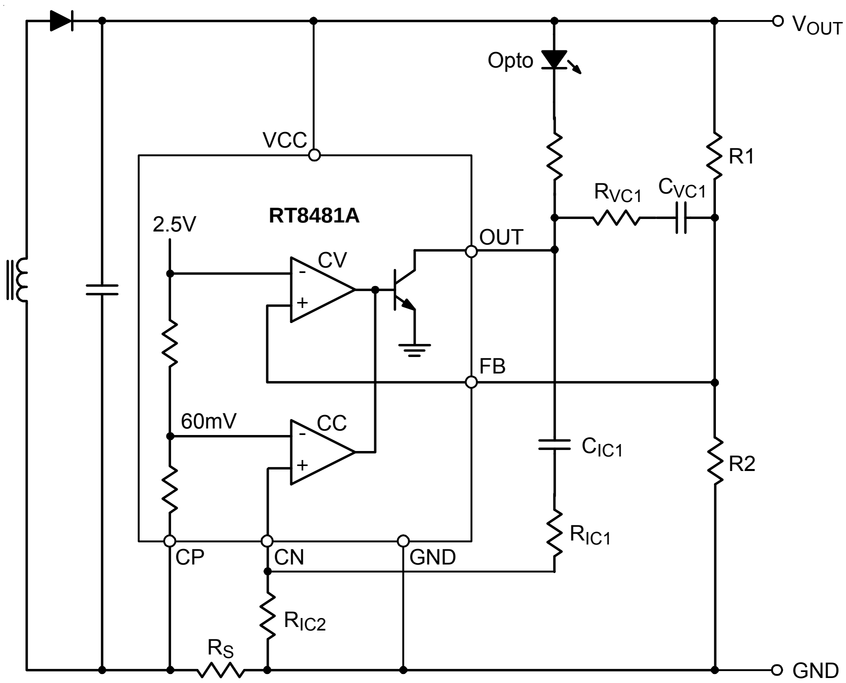
3Y= : Product Code

DNN : Date Code

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	CN	Non-inverting Input of the CC Regulating Amp. It has 60mV offset from the CP pin. The CN pin should be connected to the "current-in" node of the current sensing resistor, Rs.
2	GND	Ground.
3	FB	Non-inverting Input of the CV Regulating Amp. The pin should be connected to the mid-point of a resistor divider from "Secondary Side VOUT" (usually the VCC) to GND.
4	CP	Inverting Input of the CC Regulating Amp with –60mV offset from CN pin. The CP pin should be connected to the "current-out" node of the current sensing resistor.
5	OUT	Common Open-collector Output of CC and CV Regulating Amps. The pin sinks a regulated current and driver the opto-coupler to transmit the error signal to primary-side.
6	VCC	Supply Voltage Input. A 0.1μF bypass capacitor should be connected between VCC and GND.

Function Block Diagram & Typical Application Circuit



Operation

The available input voltage range is from 4.75V to 50V for the RT8481A. An internal 2.5V reference voltage is generated from VCC input power. The RT8481A can be used to monitor the transformer secondary-side output voltage by the CV control loop and regulate the output current by the CC control loop at the same time.

The transformer secondary-side output voltage can be monitored by the FB pin voltage. The sensed FB pin voltage is compared with the 2.5V internal reference. When the FB pin voltage is higher than 2.5V, the OUT pin will sink more current at the external opto-coupler and instruct the controller at primary-side to adjust the output voltage.

The output current can be regulated by the voltage across the CN and CP pins through the current sense resistor connected between the CN and CP pins. The voltage difference between CN and CP pins is compared with the 60mV internal reference. When the voltage difference between CN and CP pins is greater than 60mV, the OUT pin will sink more current at the external opto-coupler and instruct the controller at primary-side to adjust the output current.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, V_{CC} ---------- –0.3V to 60V
- CP ---------- –5V to 1V
- CN ---------- –0.3V to 1V
- FB ---------- –0.3V to V_{CC}
- OUT ---------- –0.3V to 50V
- OUT Current ---------- –20mA to 20mA
- Power Dissipation, P_D @ T_A = 25°C
  SOT-23-6 ---------- 0.41W
- Package Thermal Resistance (Note 2)
  SOT-23-6, θ_{JA} ---------- 243.3°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV
  MM (Machine Model) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, V_{CC} (Note 5) ---------- 4.75 to 50V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{CC} = 12V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Device Supply						
Quiescent Current	I_{CC}	CV Close Loop, V_{CN} = V_{CP} = 0V	--	500	600	μA
		CV Close Loop, V_{CN} = V_{CP} = 0V, T_A = –25°C to 105°C	--	--	800	
Voltage Control Loop OP Amp						
Transconductance	GM_V	V_{CC} = 4.75V to 45V	--	1	--	S
Power Supply Rejection Rate	PSRR	V_{CC} = 4.75V to 45V	--	60	--	dB
FB Voltage	V_{FB}	V_{CN} = V_{CP} = 0V	2.487	2.5	2.513	V
		V_{CN} = V_{CP} = 0V, T_A = –25°C to 105°C	2.475	--	2.525	
FB Line Regulation	$dV_{LINE\text{-}FB}$	V_{CN} = V_{CP} = 0V, V_{CC} = 4.75V to 45V	--	0.2	--	%
FB Input Bias Current	I_{FB}	V_{FB} = 2.4 to 2.6V	--	--	100	nA
		V_{FB} = 2.4 to 2.6V, T_A = –25°C to 105°C	--	--	200	
Current Control Loop						
Transconductance		V_{CC} = 4.75V to 45V	--	6	--	S
CN – CP Voltage	$V_{CN\text{-}CP}$	V_{FB} = 2.4V	59	61	63	mV
		T_A = –25°C to 105°C	58	--	64	

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
CN – CP Line Regulation	$dV_{LINE\text{-}CN\text{-}CP}$	V_{FB} = 2.4V, V_{CC} = 4.75V to 45V	--	0.2	--	%/V
CN Input Bias Current	I_{CN}	Close Loop	--	--	100	nA
		Close Loop, T_A = –25°C to 105°C	--	--	200	
Output Stage						
OUT Maximum Sink Current	I_{OUTH}	V_{OUT} = 1.5V	--	8	--	mA
		V_{OUT} = 1.5V, T_A = –25°C to 105°C	--	8	--	
OUT Minimum Voltage	V_{OUTL}	I_{OUT} = 2mA	--	1	1.2	V
		I_{OUT} = 2mA, T_A = –25°C to 105°C	--	--	1.5	

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7.

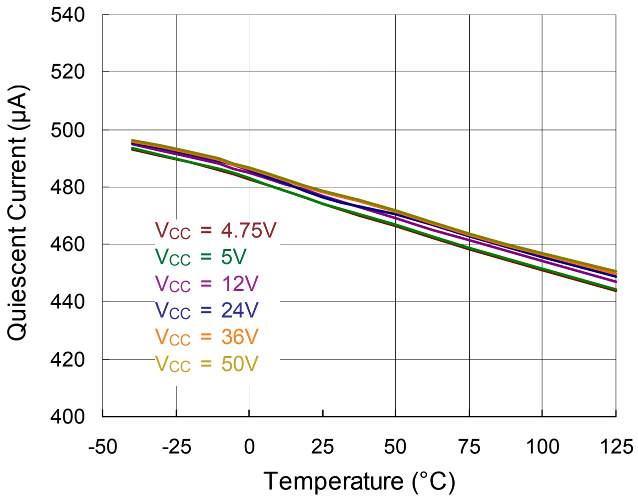
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

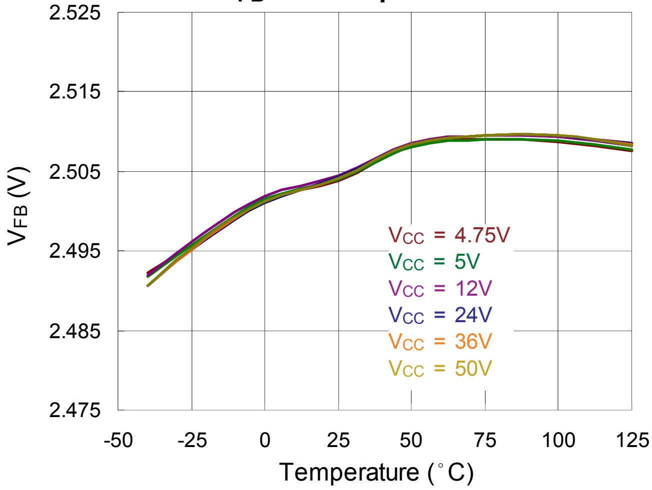
Note 5. RT8481A starts regulation at $V_{CC} \geq$ 4.5V, and meets all parameter specs at $V_{CC} \geq$ 4.75V.

Typical Operating Characteristics

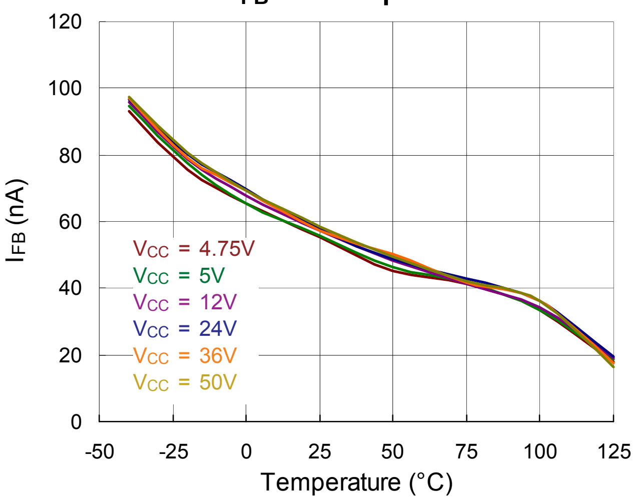
Quiescent Current vs. Temperature



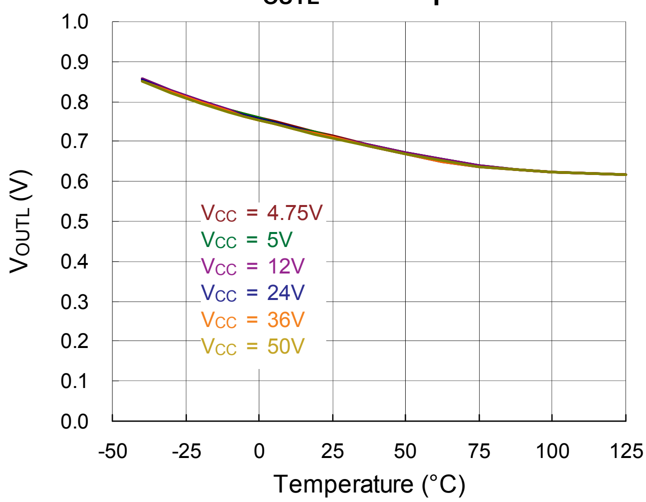
V_{FB} vs. Temperature



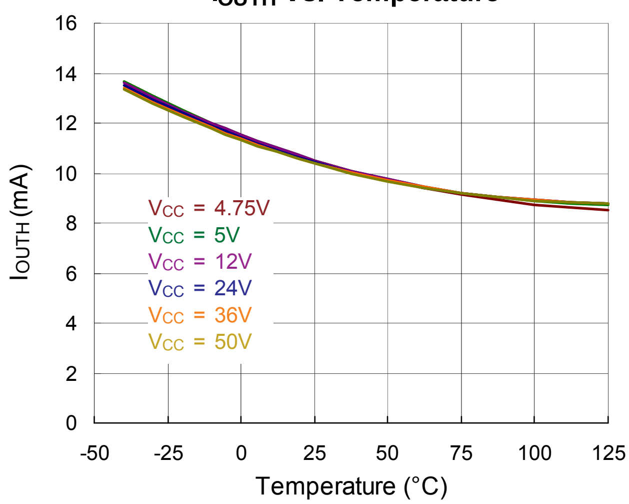
I_{FB} vs. Temperature



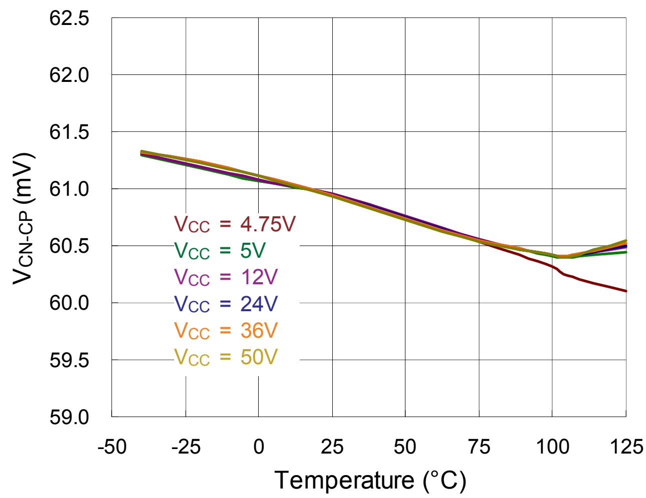
V_{OUTL} vs. Temperature

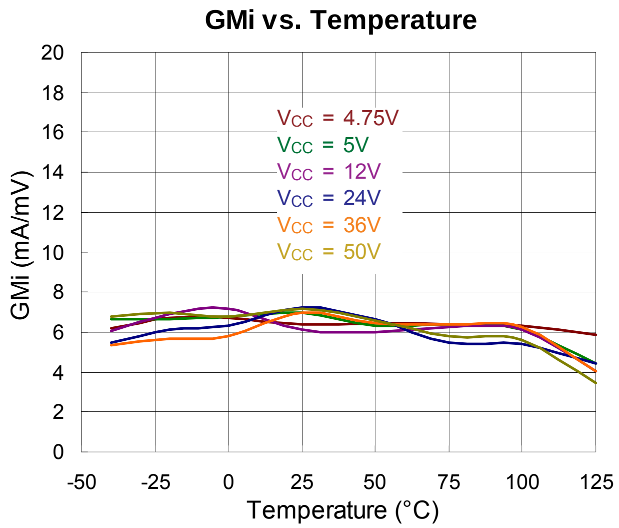


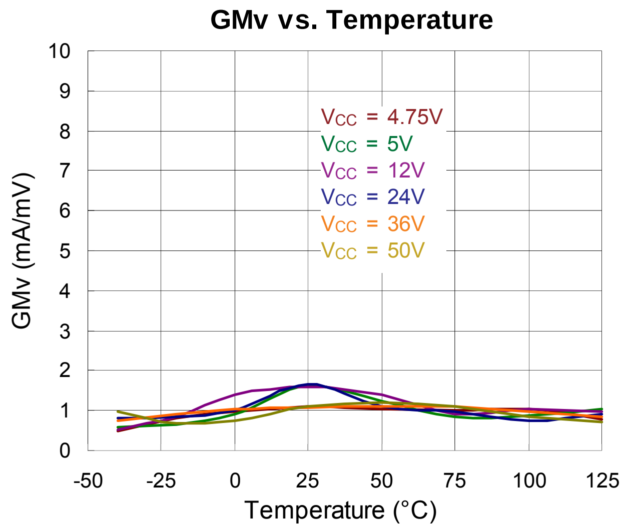
I_{OUTH} vs. Temperature



V_{CN-CP} vs. Temperature




GMi vs. Temperature
GMi (mA/mV)
Temperature (°C)
VCC = 4.75V
VCC = 5V
VCC = 12V
VCC = 24V
VCC = 36V
VCC = 50V
20
18
16
14
12
10
8
6
4
2
0
-50
-25
0
25
50
75
100
125


GMv vs. Temperature
GMv (mA/mV)
Temperature (°C)
VCC = 4.75V
VCC = 5V
VCC = 12V
VCC = 24V
VCC = 36V
VCC = 50V
10
9
8
7
6
5
4
3
2
1
0
-50
-25
0
25
50
75
100
125

Application Information

Output Voltage Setting

The voltage control loop is controlled via the first trans-conductance operational amplifier. An optocoupler which is directly connected to the output and an external resistor bridge is connected between the output positive line and the ground reference. The middle point is to be connected to the FB pin of RT8481A, where R2 is the upper resistor and R1 the lower resistor of the bridge. The relationship between R2 and R1 is shown below :

$$V_{OUT} = V_{FB} \times \frac{(R1 + R2)}{R2}$$

$$R1 = R2 \times \frac{(V_{OUT} - V_{FB})}{V_{FB}}$$

where V_{OUT} is the desired maximum output voltage and V_{FB} is the feedback voltage (2.5V typ). When under constant voltage control mode, the output voltage is fixed due to the R1/R2 resistor bridge. To avoid discharge of the load, the resistor bridge R1, R2, should be highly resistive. For this type of application a total value of 100kΩ (or more) would be appropriate for the resistors R1 and R2.

As an example, with R1 = 80kΩ and R2 = 20kΩ, V_{OUT} = 12.5V

Output Current Setting

The current control loop is controlled via the second transconductance operational amplifier. An optocoupler and the sense resistor, Rs, is placed in series on the output negative line. V_{CN-CP} threshold is achieved externally by a resistor bridge tied to the Vref voltage reference. Its middle point is tied to the positive input of the current control operational amplifier and its foot is to be connected to the lower potential point of the sense resistor. The resistors of the bridge are matched to provide the best precision. With V_{CN-CP} and Rs, the expected output current I_{OUT} can be obtained as below equation.

$$I_{OUT} = \frac{V_{CN\text{-}CP}}{R_S}$$

As an example, with R_S = 200mΩ

V_{CN-CP} = 60mV, I_{OUT} = 300mA

where I_{OUT} is the desired maximum output current, and V_{CN-CP} the threshold voltage for the current control loop. Note that R_{SENSE} resistor should be chosen taking into account its maximum power dissipation (P_{LIM}) during full load operation.

Compensation

Both the voltage control trans-conductance amplifier and the current control trans-conductance amplifier can be fully compensated. The output and negative inputs are directly accessible for external compensation components, as shown in the Typical Application Circuit.

The typical component values for the compensation network of voltage control loop is C_{VC1} = 2.2nF and R_{VC1} = 22kΩ. The typical component values for the compensation network of current control loop is C_{IC1} = 2.2nF, R_{IC1} = 22kΩ and R_{IC2} = 1kΩ. However, in many application conditions, the current control loop can be stable even without compensation network (R_{IC2} = 0, no C_{IC1} nor R_{IC1}).

When the voltage control loop is used as the voltage limit protection or the current control loop is used as the current limit protection, no compensation network is needed for the protecting control loop.

A resistor, R_{OPT}, must be connected in series with the opto-coupler since it is part of the compensation network. Although the value of R_{OPT} is not critical, it's recommended to be in the range from 0.33kΩ to (V_{OUT} – 2) / (0.005) Ω.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For SOT-23-6 packages, the thermal resistance, θ_{JA}, is 243.3°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C − 25°C) / (243.3°C/W) = 0.41W for SOT-23-6 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 1 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

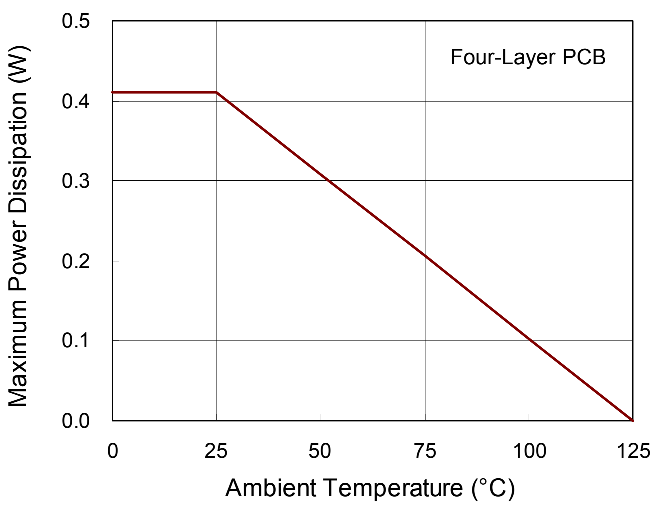


Figure 1. Derating Curve of Maximum Power Dissipation

Layout Consideration

For the best performance of the RT8481A, the following PCB Layout guidelines must be strictly followed.

- Place the R_{SENSE} resistor as close to IC as possible.
- Keep the input/output traces as wide and short as possible.

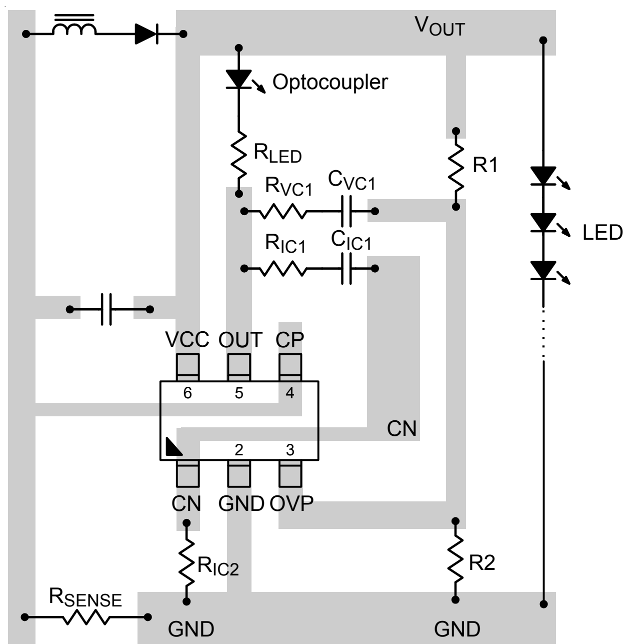
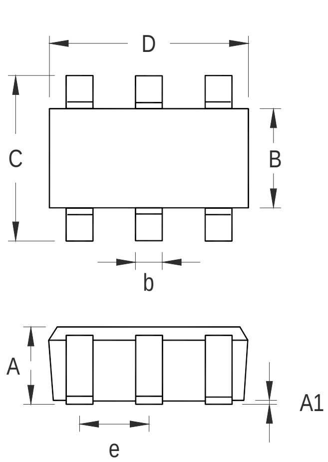


Figure 2. PCB Layout Guide

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.889	1.295	0.031	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.250	0.560	0.010	0.022
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

SOT-23-6 Surface Mount Package

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