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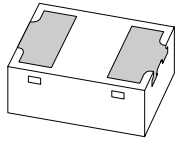
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Kind regards,

Team Nexperia



# PESD5V0S1BLD

Low capacitance bidirectional ESD protection diode

Rev. 1 — 12 October 2010

Product data sheet

## 1. Product profile

### 1.1 General description

Low capacitance bidirectional ElectroStatic Discharge (ESD) protection diode designed to protect one signal line from the damage caused by ESD and other transients. The device is housed in a SOD882D leadless ultra small Surface-Mounted Device (SMD) plastic package with visible and solderable side pads.

### 1.2 Features and benefits

- Bidirectional ESD protection of one line
- Ultra small SMD plastic package
- Solderable side pads
- Package height typ. 0.37 mm
- Low clamping voltage:  $V_{CL} = 14\text{ V}$
- AEC-Q101 qualified
- ESD protection up to 30 kV
- IEC 61000-4-2; level 4 (ESD)
- IEC 61000-4-5 (surge);  $I_{PP} = 12\text{ A}$
- Max. peak pulse power:  $P_{PP} = 130\text{ W}$
- Ultra low leakage current:  $I_{RM} = 5\text{ nA}$

### 1.3 Applications

- Computers and peripherals
- Audio and video equipment
- Cellular handsets and accessories
- Communication systems
- Portable electronics

### 1.4 Quick reference data

Table 1. Quick reference data

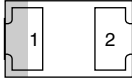
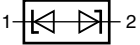
$T_{amb} = 25\text{ °C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Per diode</b>						
$V_{RWM}$	reverse standoff voltage		-	-	5.0	V
$C_d$	diode capacitance	$f = 1\text{ MHz}; V_R = 0\text{ V}$	-	35	45	pF



## 2. Pinning information

**Table 2. Pinning**

Pin	Description	Simplified outline	Graphic symbol
1	cathode 1 <a href="#">[1]</a>	 <p>Transparent top view</p>	 <p>006aab04:</p>
2	cathode 2		

[1] The marking bar indicates cathode 1.

## 3. Ordering information

**Table 3. Ordering information**

Type number	Package		
	Name	Description	Version
PESD5V0S1BLD	-	leadless ultra small plastic package; 2 terminals; body 1.0 × 0.6 × 0.4 mm	SOD882D

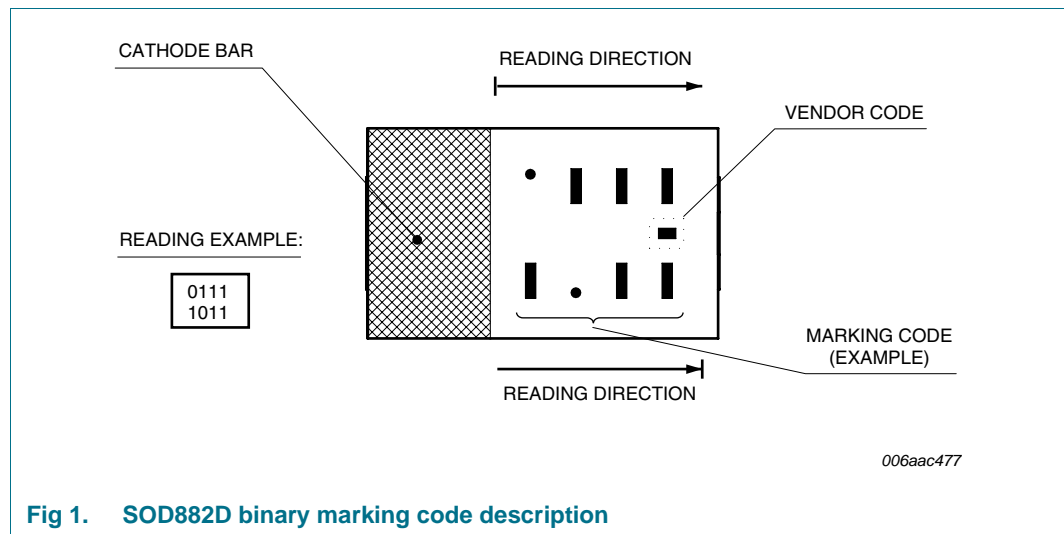
## 4. Marking

**Table 4. Marking codes**

Type number	Marking code <sup>[1]</sup>
PESD5V0S1BLD	1100 0000

[1] For SOD882D binary marking code description, see [Figure 1](#).

### 4.1 Binary marking code description



## 5. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
<b>Per diode</b>					
$P_{PP}$	peak pulse power	$t_p = 8/20 \mu\text{s}$	[1] -	130	W
$I_{PP}$	peak pulse current	$t_p = 8/20 \mu\text{s}$	[1] -	12	A
$T_j$	junction temperature		-	150	°C
$T_{amb}$	ambient temperature		-55	+150	°C
$T_{stg}$	storage temperature		-65	+150	°C

[1] Non-repetitive current pulse 8/20  $\mu\text{s}$  exponential decay waveform according to IEC 61000-4-5.

**Table 6. ESD maximum ratings**

$T_{amb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{ESD}$	electrostatic discharge voltage	IEC 61000-4-2 (contact discharge)	[1][2] -	30	kV
		MIL-STD-883 (human body model)	-	10	kV

[1] Device stressed with ten non-repetitive ESD pulses.

[2] Measured from pin 1 to pin 2.

**Table 7. ESD standards compliance**

Standard	Conditions
IEC 61000-4-2; level 4 (ESD)	> 15 kV (air); > 8 kV (contact)
MIL-STD-883; class 3 (human body model)	> 4 kV

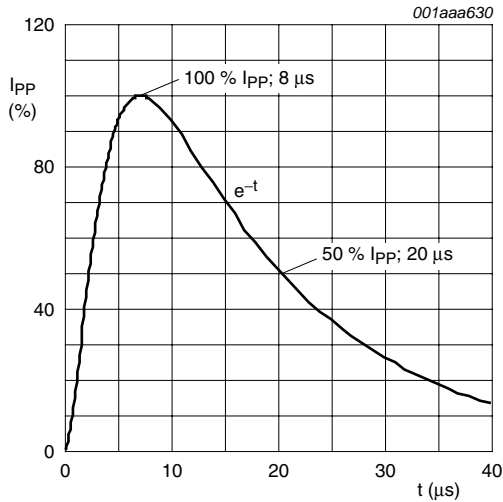


Fig 2. 8/20 μs pulse waveform according to IEC 61000-4-5

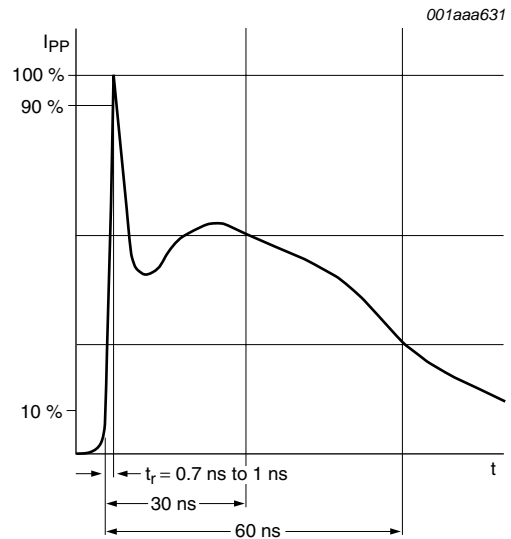


Fig 3. ESD pulse waveform according to IEC 61000-4-2

## 6. Characteristics

Table 8. Characteristics

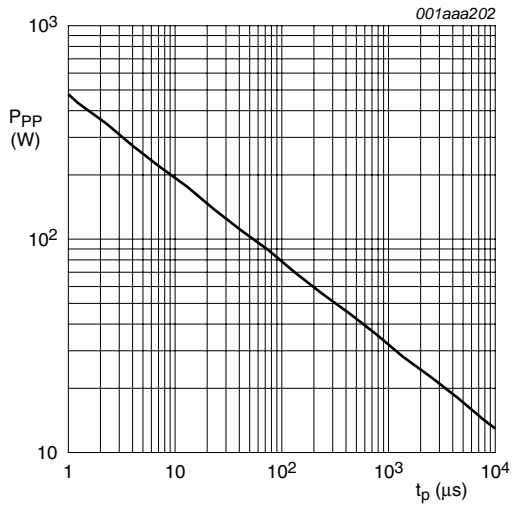
$T_{amb} = 25\text{ }^{\circ}\text{C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Per diode</b>						
$V_{RWM}$	reverse standoff voltage		-	-	5.0	V
$I_{RM}$	reverse leakage current	$V_{RWM} = 5.0\text{ V}$	-	5	100	nA
$V_{BR}$	breakdown voltage	$I_R = 1\text{ mA}$	5.5	-	9.5	V
$C_d$	diode capacitance	$f = 1\text{ MHz};$ $V_R = 0\text{ V}$	-	35	45	pF
$V_{CL}$	clamping voltage		<a href="#">[1][2]</a>			
		$I_{PP} = 1\text{ A}$	-	-	10	V
		$I_{PP} = 12\text{ A}$	-	-	14	V
$r_{dyn}$	dynamic resistance		<a href="#">[2][3]</a>			
		$I_R = 10\text{ A}$	-	0.1	-	$\Omega$
		$I_R = -10\text{ A}$	-	0.15	-	$\Omega$

[1] Non-repetitive current pulse 8/20 μs exponential decay waveform according to IEC 61000-4-5.

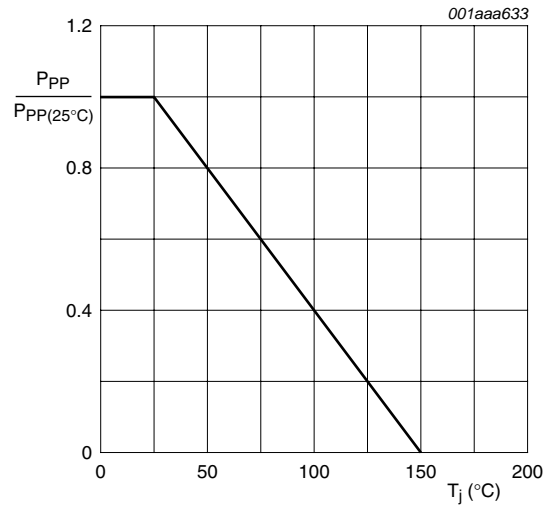
[2] Measured from pin 1 to pin 2.

[3] Non-repetitive current pulse; Transmission Line Pulse (TLP)  $t_p = 100\text{ ns}$ ; square pulse; ANSI/ESD STM5.1-2008.

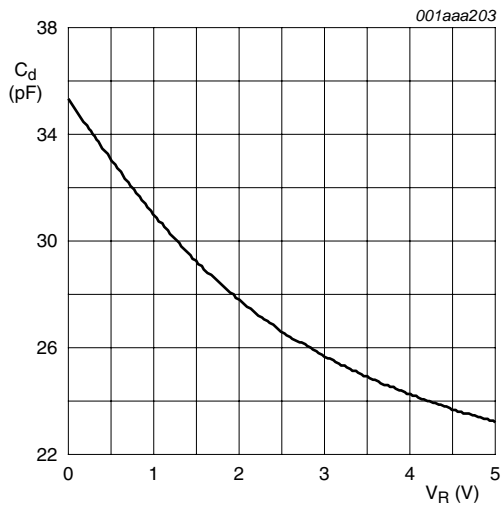


$T_{amb} = 25\text{ }^\circ\text{C}$

**Fig 4. Peak pulse power as a function of exponential pulse duration; typical values**

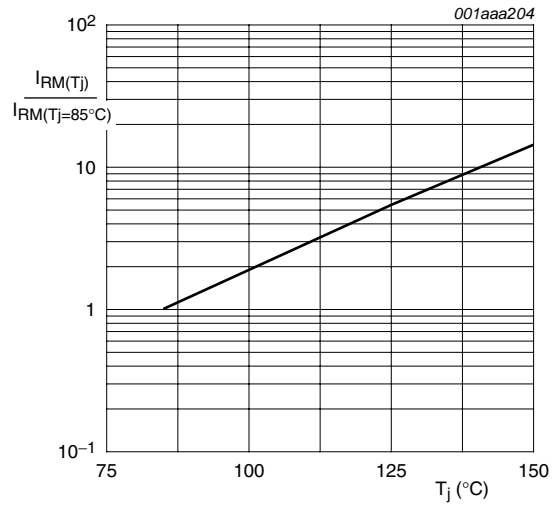


**Fig 5. Relative variation of peak pulse power as a function of junction temperature; typical values**

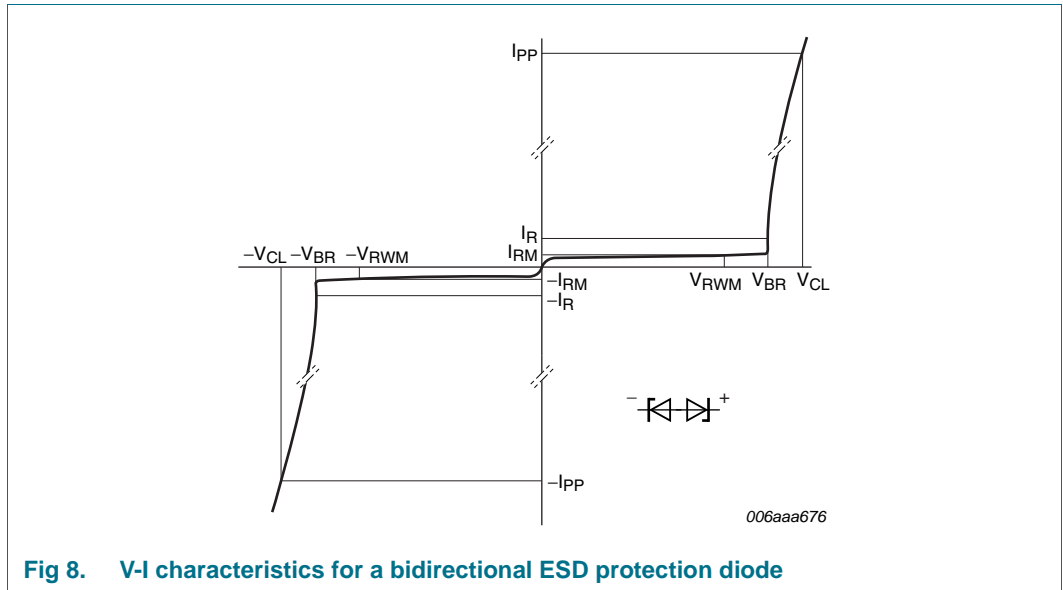


$f = 1\text{ MHz}; T_{amb} = 25\text{ }^\circ\text{C}$

**Fig 6. Diode capacitance as a function of reverse voltage; typical values**



**Fig 7. Relative variation of reverse leakage current as a function of junction temperature; typical values**



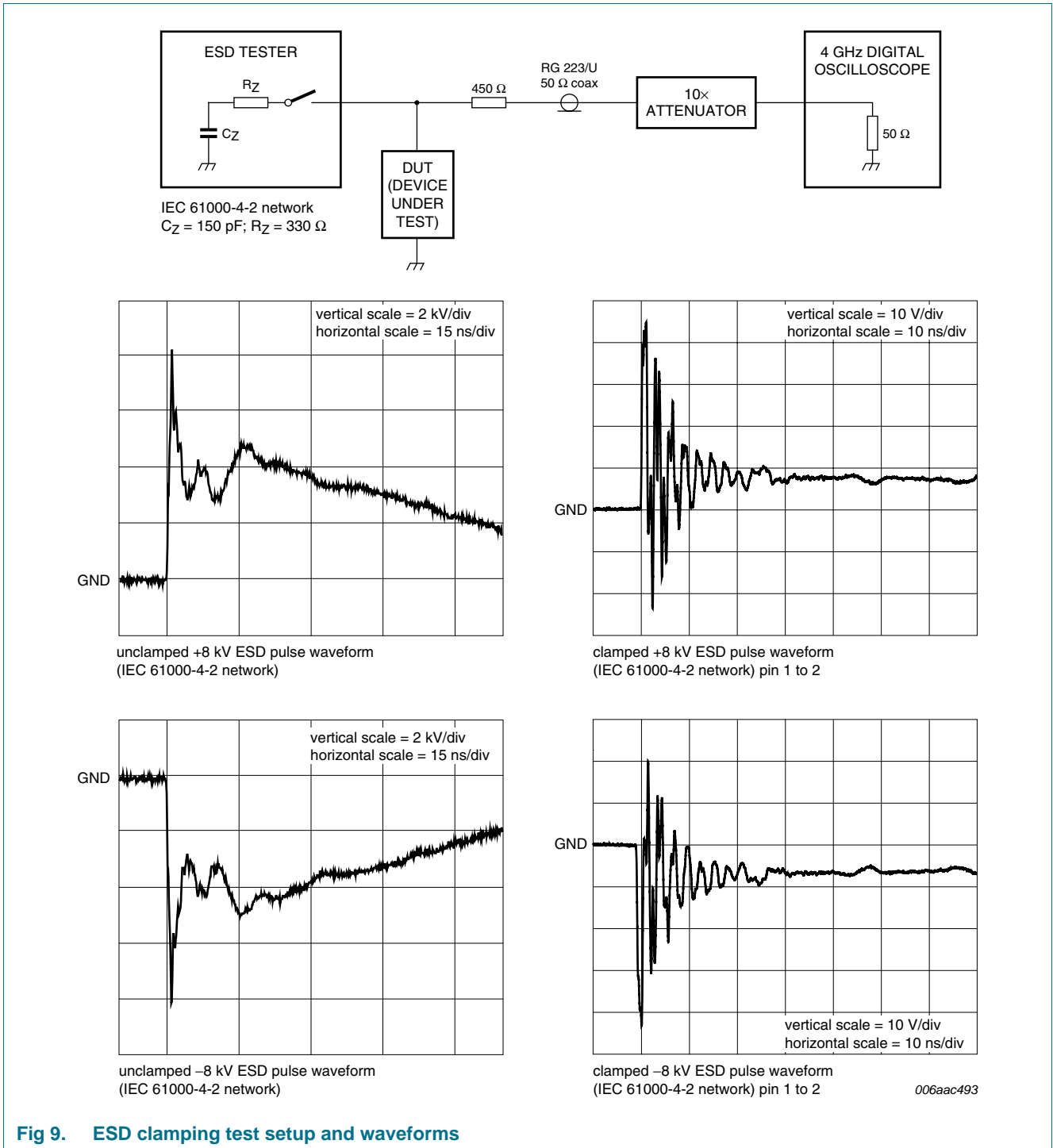


Fig 9. ESD clamping test setup and waveforms



## 7. Application information

The PESD5V0S1BLD is designed for the protection of one bidirectional data or signal line from the damage caused by ESD and surge pulses. The device may be used on lines where the signal polarities are both, positive and negative with respect to ground. The PESD5V0S1BLD provides a surge capability of 130 W per line for an 8/20  $\mu$ s waveform.

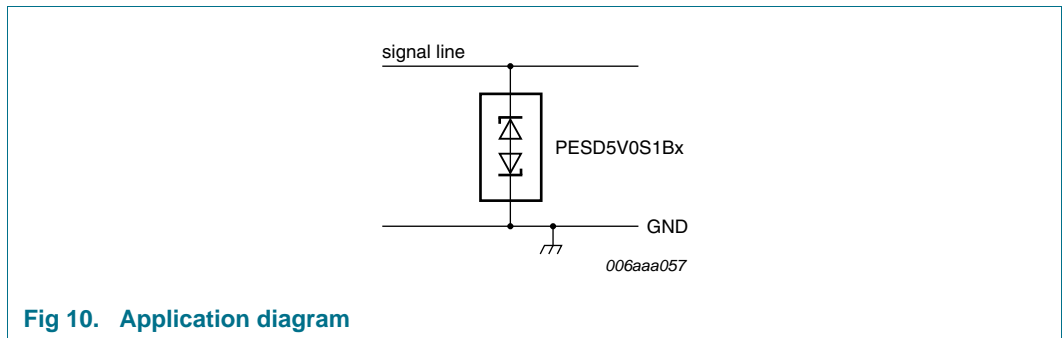


Fig 10. Application diagram

### Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

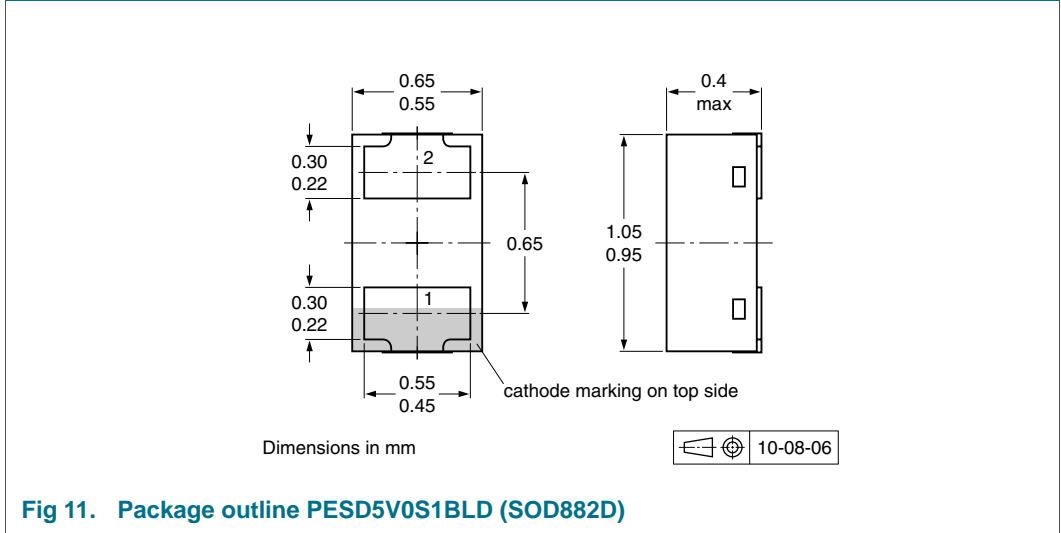
1. Place the device as close to the input terminal or connector as possible.
2. The path length between the device and the protected line should be minimized.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.

## 8. Test information

### 8.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

**9. Package outline**



**Fig 11. Package outline PESD5V0S1BLD (SOD882D)**

**10. Packing information**

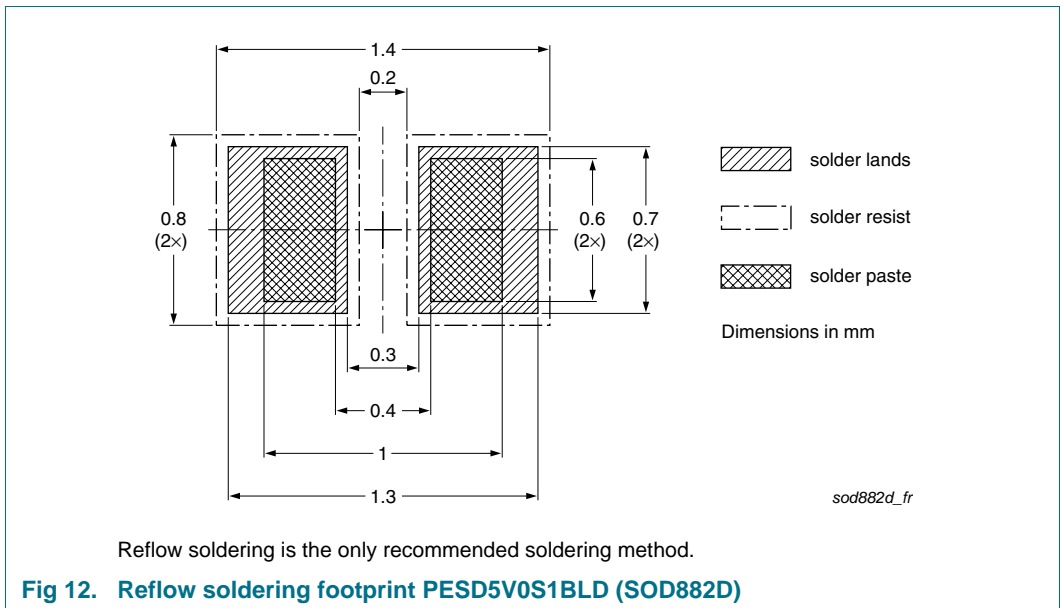
**Table 9. Packing methods**

The indicated -xxx are the last three digits of the 12NC ordering code.<sup>[1]</sup>

Type number	Package	Description	Packing quantity
PESD5V0S1BLD	SOD882D	2 mm pitch, 8 mm tape and reel	10000 -315

[1] For further information and the availability of packing methods, see [Section 14](#).

**11. Soldering**



**Fig 12. Reflow soldering footprint PESD5V0S1BLD (SOD882D)**

## 12. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PESD5V0S1BLD v.1	20101012	Product data sheet	-	-

## 13. Legal information

### 13.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

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