



# PCA9558

8-bit I<sup>2</sup>C-bus and SMBus I/O port with 5-bit multiplexed/1-bit latched 6-bit I<sup>2</sup>C-bus EEPROM DIP switch and 2-kbit EEPROM

Rev. 5 — 25 June 2012

Product data sheet

## 1. General description

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The PCA9558 is a highly integrated, multi-function device that is composed of a 5-bit multiplexed/1-bit latched 6-bit I<sup>2</sup>C-bus/SMBus EEPROM DIP switch, an 8-bit I/O expander and a 2-kbit serial EEPROM with write protect. The PCA9558 integrates these commonly used components into a single chip to reduce component count and board space requirements and is useful in computer, server and telecom/networking applications.

- **Multiplexed/latched EEPROM DIP switch** — used to select digital information between a set of 5 bits of default hardware inputs and an alternative set of inputs provided by the I<sup>2</sup>C-bus/SMBus interface and stored in the EEPROM. Examples of this type of selection include processor voltage configuration or processor vendor identification (VID). The multiplexed/latched EEPROM can also be used to replace DIP switches or jumpers, since the settings can be easily changed via I<sup>2</sup>C-bus/SMBus without having to power down the equipment to open the cabinet. The non-volatile memory retains the most current setting selected before the power is turned off.
- **8-bit I/O expander** — used to control, monitor or collect remote information or power LEDs. Monitored or collected information can be read through the I<sup>2</sup>C-bus/SMBus or can be stored in the internal EEPROM.
- **2-kbit serial EEPROM** — used to store information such as card identification or revision/maintenance history on every motherboard/line card and can be read or written via I<sup>2</sup>C-bus/SMBus when required.

The PCA9558 has one address pin, allowing up to two devices to be placed on the same I<sup>2</sup>C-bus or SMBus.

## 2. Features and benefits

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- 5-bit 2-to-1 multiplexer, 1-bit latch DIP switch
- 6-bit MUX\_OUTx and NON\_MUXED\_OUT EEPROM programmable and readable via I<sup>2</sup>C-bus
- 5 V tolerant open-drain MUX\_OUTx and NON\_MUXED\_OUT outputs
- Active LOW override input forces all MUX\_OUTx outputs to logic 0
- I<sup>2</sup>C-bus readable MUX\_INx inputs
- 5 V tolerant open-drain IOx pins, power-up default as outputs
- One address pin, allowing up to two devices on the I<sup>2</sup>C-bus
- Active LOW reset input with internal pull-up for the eight I/O pins
- 2048-bit EEPROM programmable and readable via the I<sup>2</sup>C-bus or I/Os
- Operating power supply voltage range of 3.0 V to 3.6 V
- SMBus compliance with fixed 3.3 V levels



- 2.5 V to 5 V tolerant inputs
- ESD protection exceeds 2000 V HBM per JESD22-A114 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA

### 3. Applications

- Board version tracking and configuration
- Board health monitoring and status reporting
- Multi-card systems in telecom, networking and base station infrastructure equipment
- Field recall and troubleshooting functions for installed boards
- General-purpose integrated I/O with DIP switch and memory

### 4. Ordering information

Table 1. Ordering information

Type number	Topside mark	Temperature range	Package		
			Name	Description	Version
PCA9558PW	PCA9558DH	0 °C to 70 °C	TSSOP28	plastic thin shrink small outline package; 28 leads; body width 4.4 mm	SOT361-1

5. Block diagram

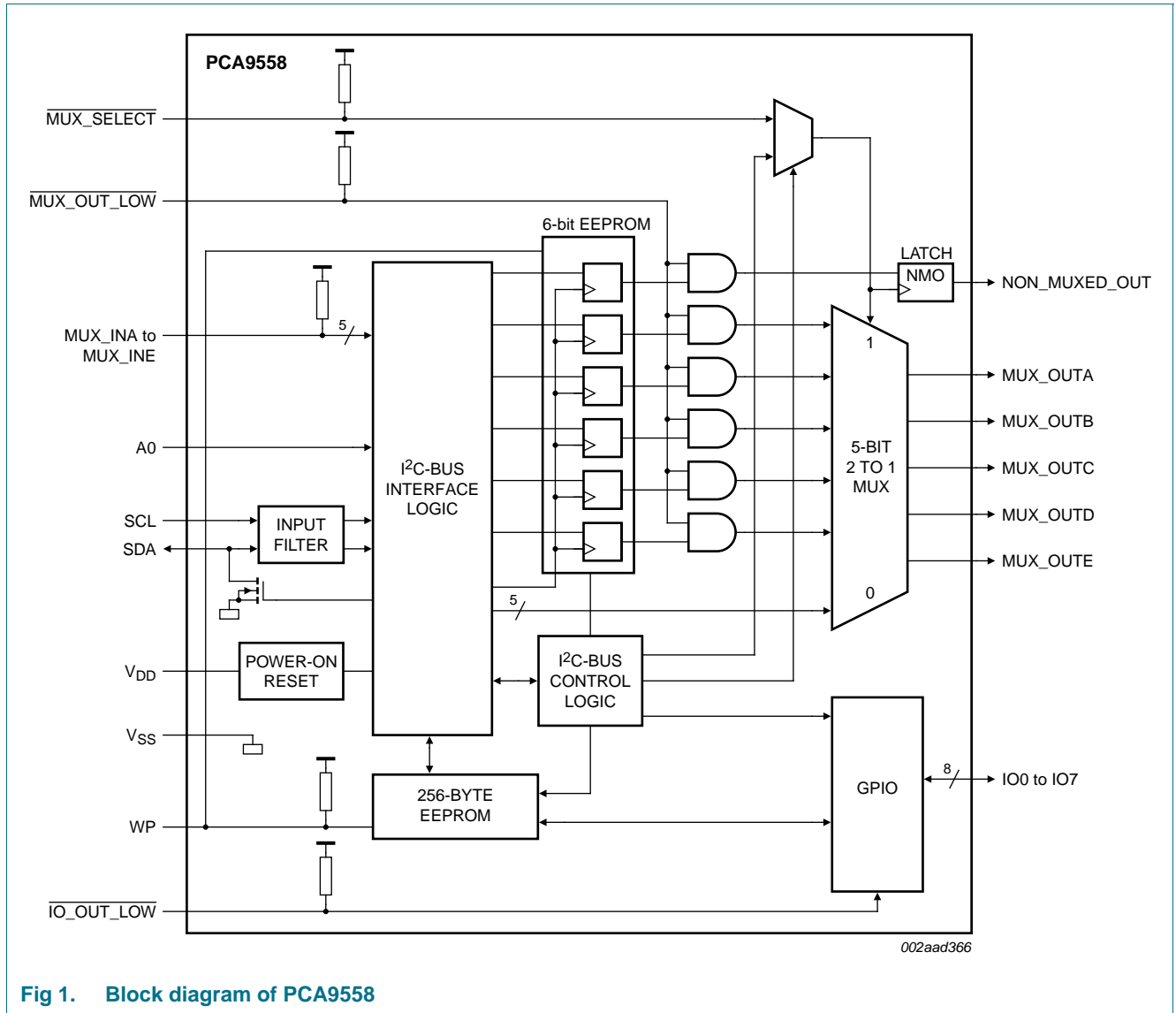


Fig 1. Block diagram of PCA9558

## 6. Pinning information

### 6.1 Pinning

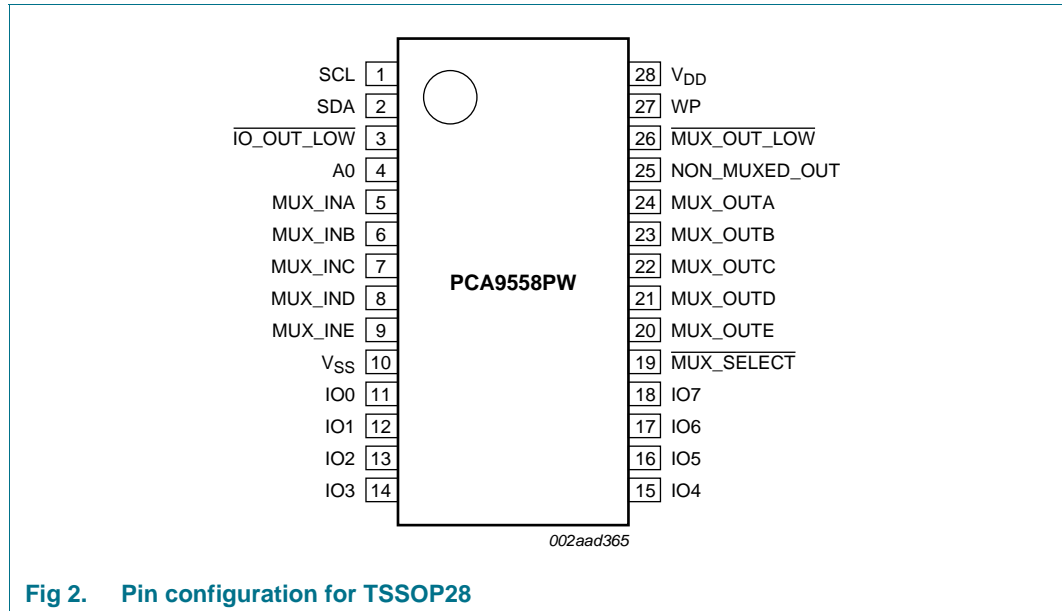


Fig 2. Pin configuration for TSSOP28

### 6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
SCL	1	serial I <sup>2</sup> C-bus clock
SDA	2	serial bidirectional I <sup>2</sup> C-bus data
IO_OUT_LOW	3	active LOW control forces all GPIO to logic 0 outputs
A0	4	A0 address
MUX_INA	5	external input A to multiplexer
MUX_INB	6	external input B to multiplexer
MUX_INC	7	external input C to multiplexer
MUX_IND	8	external input D to multiplexer
MUX_INE	9	external input E to multiplexer
V <sub>SS</sub>	10	ground
IO0	11	general purpose input/output 0 (open-drain output)
IO1	12	general purpose input/output 1 (open-drain output)
IO2	13	general purpose input/output 2 (open-drain output)
IO3	14	general purpose input/output 3 (open-drain output)
IO4	15	general purpose input/output 4 (open-drain output)
IO5	16	general purpose input/output 5 (open-drain output)
IO6	17	general purpose input/output 6 (open-drain output)
IO7	18	general purpose input/output 7 (open-drain output)

Table 2. Pin description ...continued

Symbol	Pin	Description
MUX_SELECT	19	active LOW select of MUX_INx inputs or EEPROM contents for MUX_OUTx outputs
MUX_OUTE	20	open-drain multiplexed output E
MUX_OUTD	21	open-drain multiplexed output D
MUX_OUTC	22	open-drain multiplexed output C
MUX_OUTB	23	open-drain multiplexed output B
MUX_OUTA	24	open-drain multiplexed output A
NON_MUXED_OUT	25	open-drain outputs from non-volatile memory
MUX_OUT_LOW	26	active LOW control forces all MUX outputs to logic 0
WP	27	active HIGH EEPROM write protect
V <sub>DD</sub>	28	power supply (3.0 V to 3.6 V)

## 7. Functional description

Refer to [Figure 1 “Block diagram of PCA9558”](#).

### 7.1 I<sup>2</sup>C-bus interface

Communicating with this device is initiated by sending a valid address on the I<sup>2</sup>C-bus. The address format (see [Figure 3](#)) has 6 fixed bits and one user-programmable bit followed by a 1-bit read/write value which determines the direction of the data transfer.

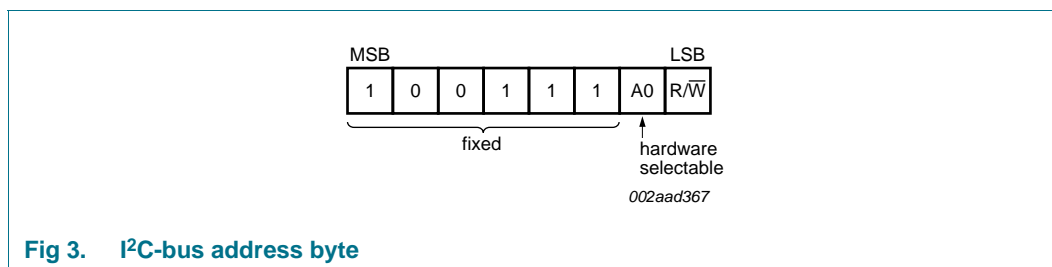


Fig 3. I<sup>2</sup>C-bus address byte

Following the address and acknowledge bit are 8 data bits which, depending on the read/write bit in the address, will read data from or write data to the EEPROM. Data will be written to the register if the read/write bit is logic 0 and the WP input is logic 0. Data will be read from the register if the bit is logic 1. The four high-order bits are latched outputs, while the four low order bits are multiplexed outputs ([Figure 5](#)).

**Remark:** To ensure data integrity, the EEPROM must be internally write protected when V<sub>DD</sub> to the I<sup>2</sup>C-bus is powered down or V<sub>DD</sub> to the component is dropped below normal operating levels.

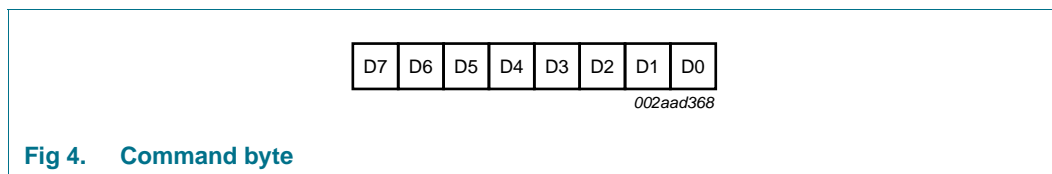
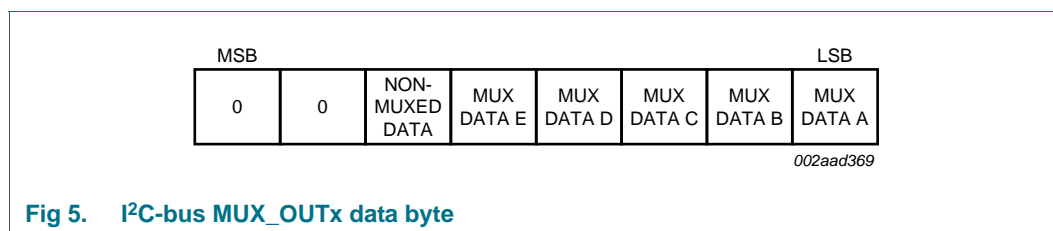


Fig 4. Command byte

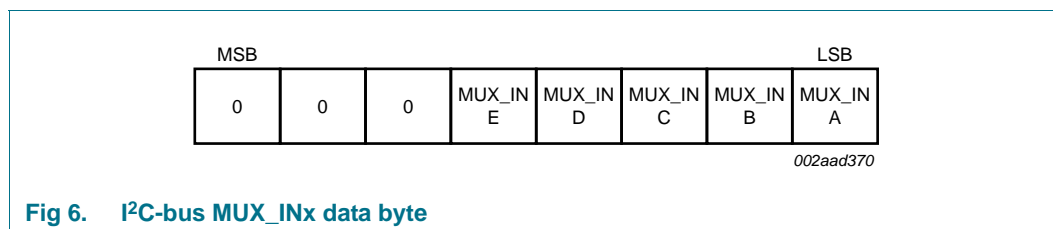
**Table 3. Command byte**

D7	D6	D5	D4	D3	D2	D1	D0	Command
0	0	0	0	0	0	0	1	write to 256-byte EEPROM via I <sup>2</sup> C-bus
0	0	0	0	0	0	1	1	read from 256-byte EEPROM via I <sup>2</sup> C-bus
0	0	0	0	0	1	0	0	write to 6-bit EEPROM via I <sup>2</sup> C-bus
0	0	0	0	0	1	1	0	read from 6-bit EEPROM via I <sup>2</sup> C-bus
0	0	0	0	0	1	1	1	read Input Port (IP) register via I <sup>2</sup> C-bus
0	0	0	0	1	0	0	0	read/write Output Port (OP) register via I <sup>2</sup> C-bus
0	0	0	0	1	0	0	1	read/write Polarity Inversion (PI) register via I <sup>2</sup> C-bus
0	0	0	0	1	0	1	0	read/write Input/Output Configuration (IOC) register via I <sup>2</sup> C-bus
0	0	0	0	1	0	1	1	read/write MUX Control (MUXCNTRL) register via I <sup>2</sup> C-bus
0	0	0	0	1	1	0	0	read MUX_INx values via I <sup>2</sup> C-bus
0	0	0	0	1	1	0	1	reserved
0	0	0	0	1	1	1	0	reserved
0	0	0	0	1	1	1	1	read 256-byte EEPROM and write OP register
0	0	0	1	0	0	0	0	read 256-byte EEPROM and write PI register
0	0	0	1	0	0	0	1	read 256-byte EEPROM and write IOC register
0	0	0	1	0	0	1	0	read IP register and write to 256-byte EEPROM
0	0	0	1	0	0	1	1	reserved
:	:	:	:	:	:	:	:	
1	1	1	1	1	1	1	1	reserved

### 7.1.1 Multiplexer



**Fig 5. I<sup>2</sup>C-bus MUX\_OUTx data byte**



**Fig 6. I<sup>2</sup>C-bus MUX\_INx data byte**

The Multiplexer controls the six open-drain outputs, MUX\_OUTx and NON\_MUXED\_OUT. This control is affected by the input pins MUX\_SELECT (pin 19), MUX\_OUT\_LOW (pin 26), and/or an internal register programmed via the I<sup>2</sup>C-bus.

Upon power-up, the multiplex function is controlled by the MUX\_SELECT and MUX\_OUT\_LOW pins. When the MUX\_SELECT signal is a logic 0, the multiplexer will select the data from the 6-bit EEPROM to drive on the MUX\_OUTx and NON\_MUXED\_OUT pins. When the MUX\_SELECT signal is a logic 1, the multiplexer will select the MUX\_INx pins to drive on the MUX\_OUTx pins.

The NON\_MUXED\_OUT output is latched from the 6-bit EEPROM on a rising edge of the MUX\_SELECT signal. This latch is transparent while the MUX\_SELECT signal is a logic 0. An internal control register, written via the I<sup>2</sup>C-bus, can also control the multiplexer function. When this register is written, the MUX\_SELECT function can change from the external pin to an internal register. In this register a bit will act in a similar fashion to the MUX\_SELECT input, i.e., a logic 1 will cause the multiplexer to select data from the 6-bit EEPROM to drive on the MUX\_OUTx and NON\_MUXED\_OUT pins. In this configuration, the NON\_MUXED\_OUT will latch data when the PCA9558 acknowledges the I<sup>2</sup>C-bus. The MUX\_SELECT pin will have no effect on the MUX\_OUTx or NON\_MUXED\_OUT while in this mode.

When the MUX\_OUT\_LOW signal is a logic 0 and the multiplexer is configured so that the MUX\_OUTx pins are being driven by the 6-bit EEPROM, the MUX\_OUTx pins will be driven to a logic 0. This information is summarized in [Table 4](#).

**Table 4. Multiplexer function table**

Register		Input		Output	
B1 <sup>[1]</sup>	B0 <sup>[1]</sup>	<u>MUX_OUT_LOW</u>	<u>MUX_SELECT</u>	<u>MUX_OUTx</u>	<u>NON_MUXED_OUT</u>
x	0	0	1	<u>MUX_INx</u> inputs	latched from EEPROM <sup>[2]</sup>
x	0	0	0	0	0
x	0	1	1	<u>MUX_INx</u> inputs	latched from EEPROM <sup>[2]</sup>
x	0	1	0	from EEPROM	from EEPROM
0	1	0	x	<u>MUX_INx</u> inputs	latched from EEPROM <sup>[3]</sup>
1	1	0	x	0	0
0	1	1	x	<u>MUX_INx</u> inputs	latched from EEPROM <sup>[3]</sup>
1	1	1	x	from EEPROM	from EEPROM

- [1] These are the 2 LSBs of the MUX Control (MUXCNTRL) register.
- [2] NON\_MUXED\_OUT value will be the value present in the 6-bit EEPROM at the time of the rising edge of the MUX\_SELECT input.
- [3] NON\_MUXED\_OUT value will be the value present in the 6-bit EEPROM at the time of the slave ACK when bit 1 has changed from logic 0 to logic 1.

If the MUX\_OUTx outputs are being driven by the 6-bit EEPROM and this EEPROM is programmed, the outputs will remain stable and change to the new values after the EEPROM program cycle completes.

Examples of read/write for MUX control can be found in [Figure 7](#).

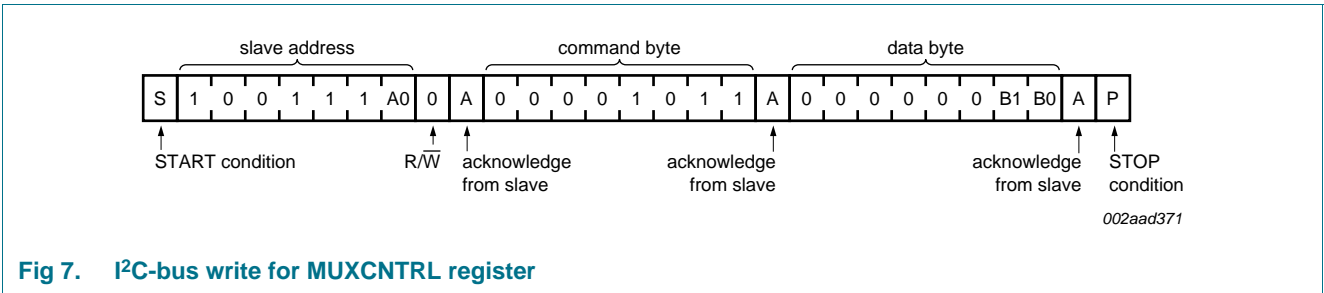


Fig 7. I<sup>2</sup>C-bus write for MUXCNTRL register

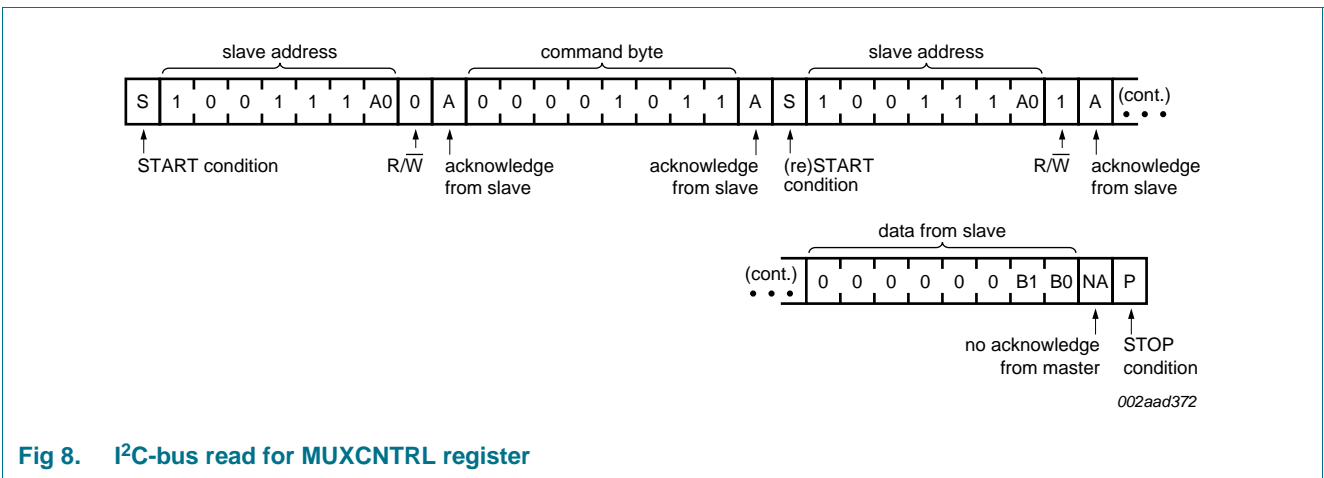


Fig 8. I<sup>2</sup>C-bus read for MUXCNTRL register

### 7.1.2 Registers

The GPIOs are controlled by a set of 4 internal registers: Input Port (IP) register; Output Port (OP) register; Polarity Inversion (PI) register; and the Input/Output Configuration (IOC) register. Each register is read/write via the I<sup>2</sup>C-bus or 256-byte EEPROM, with the exception of the Input Port register, which is read only, one at a time. The read/write takes place on the slave Acknowledge. The control of which register is currently available to the I<sup>2</sup>C-bus is set by bits in the control register. See [Section 7.1.2.1](#) through [Section 7.1.2.4](#) for details.

#### 7.1.2.1 IP - Input Port register

This register is an input-only port. It reflects the logic value present on the GPIO pins regardless of whether they are configured as inputs or outputs (IOC register). Writes to this register have no effect.

Table 5. IP - Input Port register description

Bit	7	6	5	4	3	2	1	0
Symbol	I7	I6	I5	I4	I3	I2	I1	I0
Default	0	0	0	0	0	0	0	0



### 7.1.2.2 OP - Output Port register

This register is an output-only port. It reflects the outgoing logic levels of the GPIO defined as outputs in the IOC register. Bit values in this register have no effect on GPIO defined as inputs. In turn, reads from this register reflect the value stored in the flip-flop controlling the output, **not** the actual output value.

**Table 6. OP - Output Port register description**

Bit	7	6	5	4	3	2	1	0
Symbol	O7	O6	O5	O4	O3	O2	O1	O0
Default	0	0	0	0	0	0	0	0

### 7.1.2.3 PI - Polarity Inversion register

This register enables polarity inversion of GPIO defined as inputs by the IOC register. If a bit in this register is set to a logic 1, the corresponding GPIO input port is inverted. If a bit in this register is set to a logic 0, the corresponding GPIO input port is not inverted.

**Table 7. PI - Polarity Inversion register description**

Bit	7	6	5	4	3	2	1	0
Symbol	P7	P6	P5	P4	P3	P2	P1	P0
Default	1	1	1	1	0	0	0	0

### 7.1.2.4 IOC - Input/Output Configuration register

This register configures the direction of the GPIO pins (IOx). If a bit is set to a logic 1, the corresponding port pin is enabled as an input with a high-impedance output driver. If a bit is set to a logic 0, the corresponding port pin is enabled as an output.

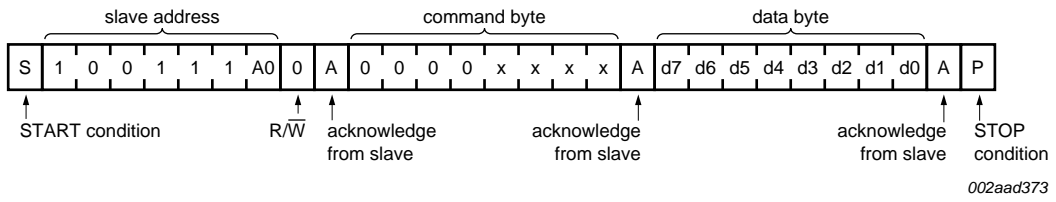
**Table 8. IOC - Input/Output Configuration register description**

Bit	7	6	5	4	3	2	1	0
Symbol	C7	C6	C5	C4	C3	C2	C1	C0
Default	0	0	0	0	0	0	0	0

Examples of read/write to these registers can be found in [Figure 9](#), [Figure 10](#), [Figure 15](#), and [Figure 16](#).

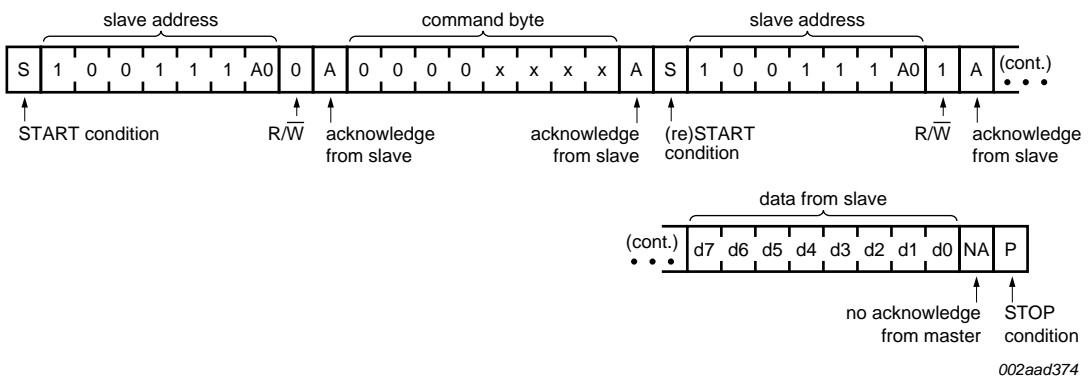
The  $\overline{\text{IO\_OUT\_LOW}}$  input, when held LOW longer than the time  $T_{\text{cy(W)}}$ , will reset the GPIO registers to their default (power-up) values.

A read of the present value of the inputs MUX\_INx can be done via the I<sup>2</sup>C-bus. This is done by addressing the PCA9558 in a write mode and entering the correct command code. The preset value on the MUX\_INx inputs is latched at the command code Acknowledge. A REPEATED START is then sent with the  $\overline{\text{R/W}}$  bit set to a logic 1, read, and this latched data is read out on the I<sup>2</sup>C-bus. See [Figure 11](#).

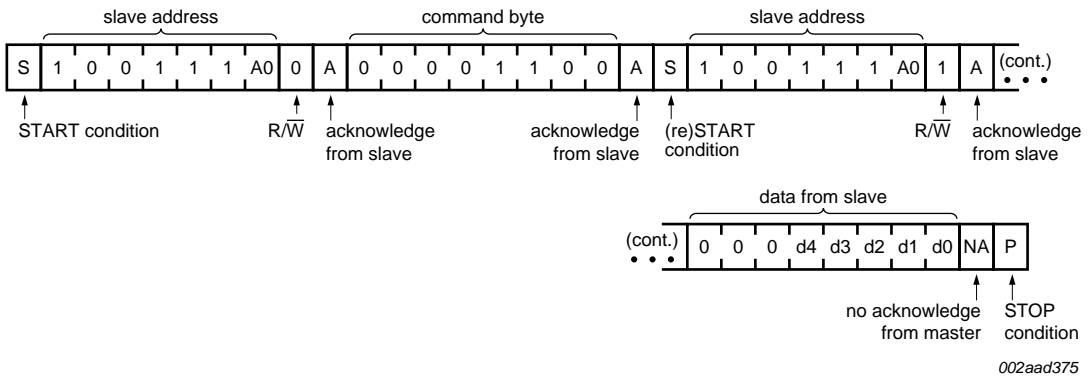


See [Table 3](#) for the proper command byte.

**Fig 9. I<sup>2</sup>C-bus write for GPIO registers**



**Fig 10. I<sup>2</sup>C-bus read for GPIO registers**



**Fig 11. I<sup>2</sup>C-bus read of MUX\_INx inputs**

7.1.3 EEPROM write operation

7.1.3.1 6-bit write operation

A write operation to the 6-bit EEPROM requires that an address byte be written after the command byte. This address points to the 6-bit address space in the EEPROM array. Upon receipt of this address, the PCA9558 waits for the next byte that will be written to the EEPROM. The master then ends the transaction with a STOP condition on the I<sup>2</sup>C-bus. See [Figure 12](#).

After the STOP condition, the E/W cycle starts, and the parts will not respond to any request to access the EEPROM array until the cycle finishes, approximately 4 ms.

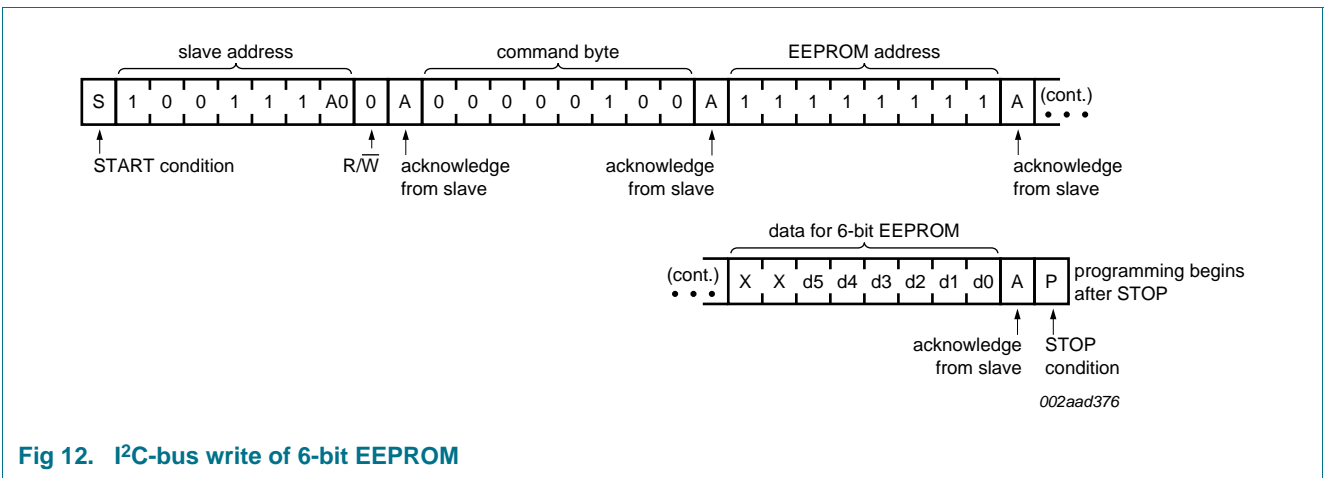


Fig 12. I<sup>2</sup>C-bus write of 6-bit EEPROM

7.1.3.2 6-bit read operation

A read operation is initiated in the same manner as a write operation, with the exception that after the word address has been written a REPEATED START condition is placed on the I<sup>2</sup>C-bus and the direction of communication is reversed (see [Figure 13](#)).

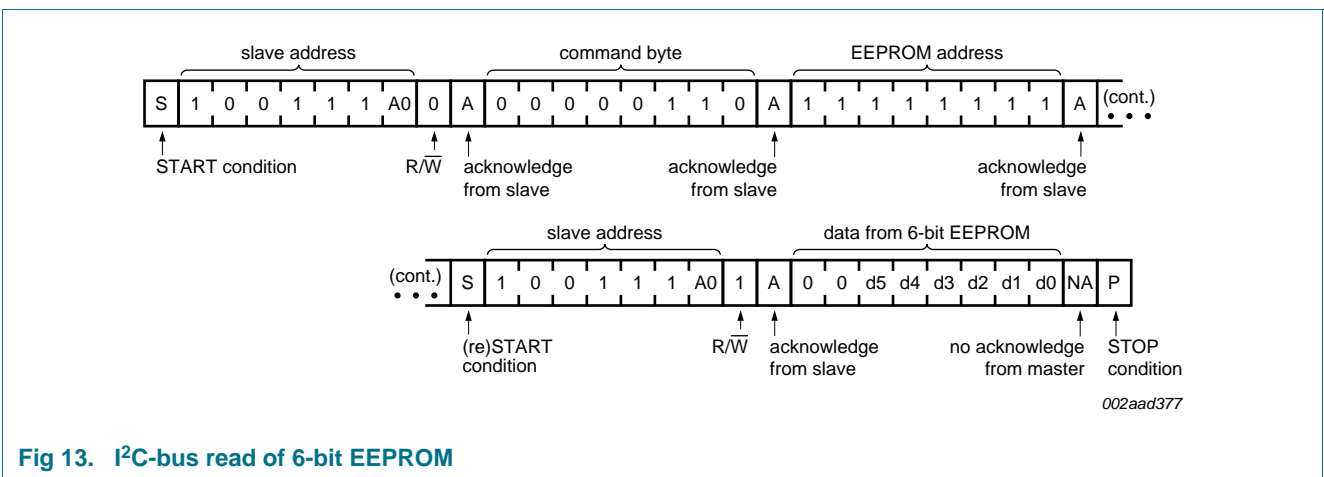
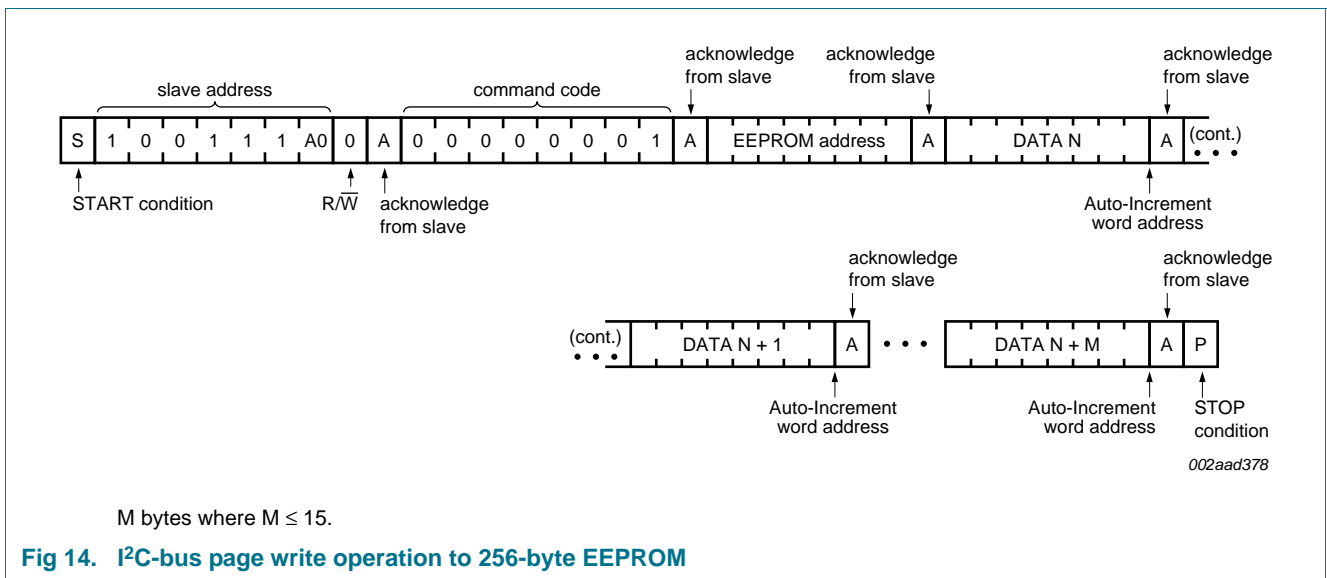


Fig 13. I<sup>2</sup>C-bus read of 6-bit EEPROM

7.1.3.3 256-byte write operation (I<sup>2</sup>C-bus)

A write operation to the 256-byte EEPROM requires that an address byte be written after the command byte. This address points to the starting address in the EEPROM array. The four LSBs of this address select a position on a 16-byte page register, the four MSBs select which page register. The four LSBs will be auto-incremented after receipt of each byte of data; in this manner, the entire page register can be written starting at any point. Up to 16 bytes of data may be sent to the PCA9558, followed by a STOP condition on the I<sup>2</sup>C-bus. If the master sends more than 16 bytes of data prior to generating a STOP condition, data within the address page will be overwritten and unpredictable results may occur. See [Figure 14](#).

After the STOP condition, the E/W cycle starts, and the parts will not respond to any request to access the EEPROM array until the cycle finishes, approximately 4 ms.



7.1.3.4 256-byte read operation (I<sup>2</sup>C-bus)

A read operation is initiated in the same manner as a write operation, with the exception that after the word address has been written, a REPEATED START condition is placed on the I<sup>2</sup>C-bus, and the direction of communication is reversed. For a read operation, the entire address is incremented after the transmission of each byte, meaning that the entire 256-byte EEPROM array can be read at one time. See [Figure 15](#).

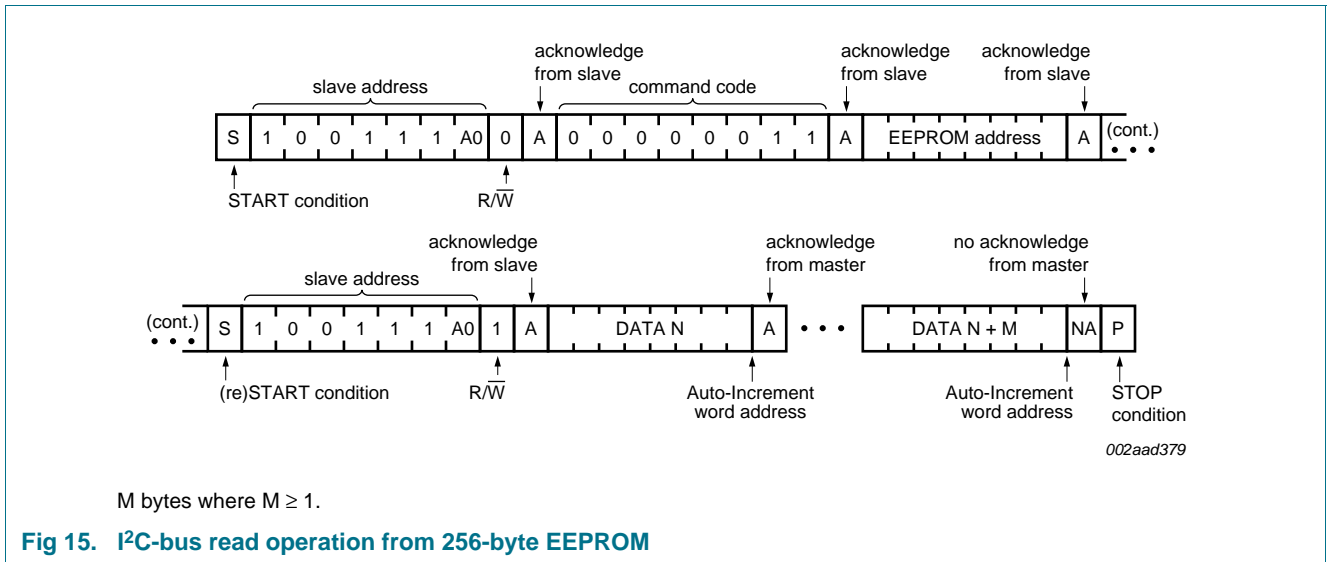


Fig 15. I<sup>2</sup>C-bus read operation from 256-byte EEPROM

7.1.3.5 256-byte EEPROM write to GPIO

A mode is available whereby a byte of data in the 256-byte EEPROM array can be written to the GPIO (OP register). This is initiated by the I<sup>2</sup>C-bus. In this mode, a control word indicating a read from the 256-byte EEPROM and write to the GPIO is sent, followed by the word address of the data within the EEPROM array. Upon Acknowledge from the slave, the data is sent to the GPIO. See [Figure 16](#).

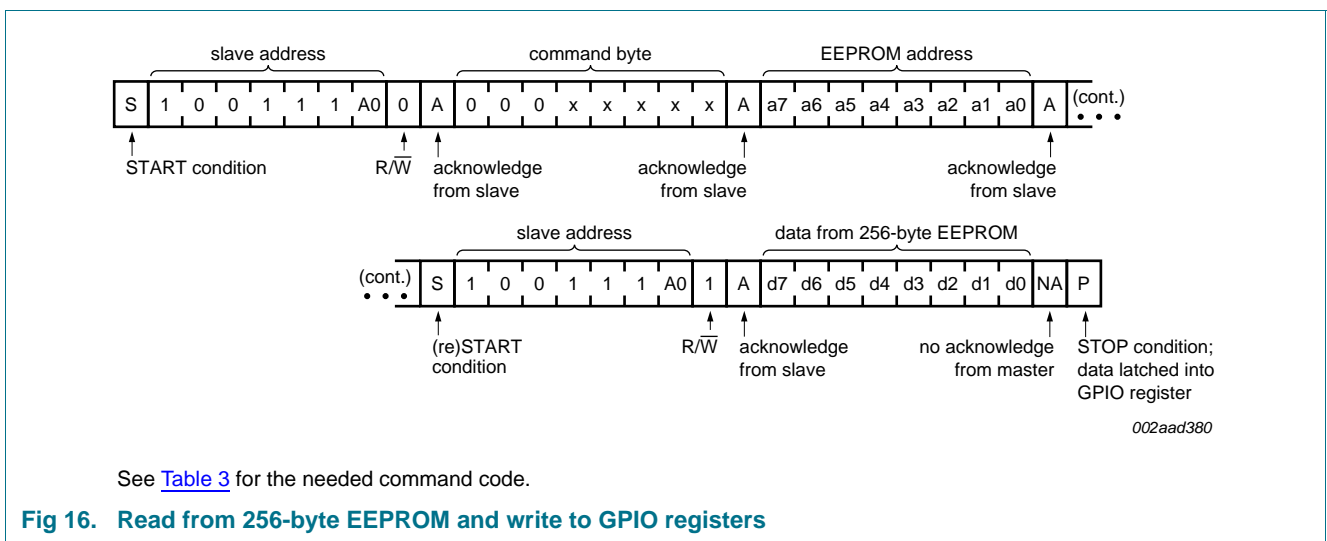


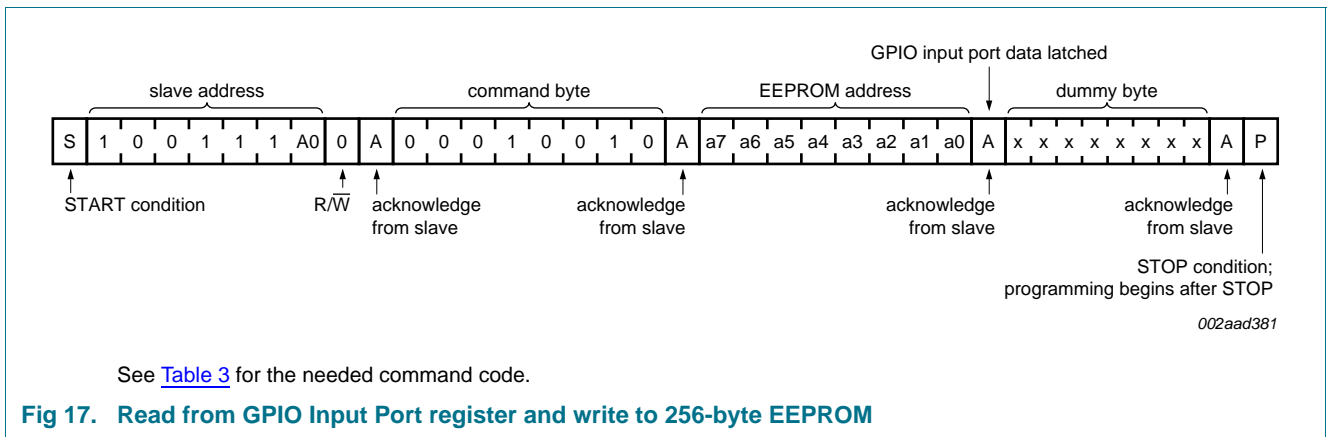
Fig 16. Read from 256-byte EEPROM and write to GPIO registers

**7.1.3.6 256-byte EEPROM write from GPIO**

A mode is available whereby data in the GPIO (IP register) can be written to the 256-byte EEPROM. This is initiated by the I<sup>2</sup>C-bus. In this mode, a control word indicating a read from the GPIO and write to the 256-byte EEPROM is sent, followed by the word address for the data to be written. Once the slave has sent an Acknowledge, the master must send a STOP condition. See [Figure 17](#).

After the STOP condition, the E/W cycle starts, and the parts will not respond to any request to access the EEPROM array until the cycle finishes, approximately 4 ms.

When the Write Protect (WP) input is a logic 0 it allows writes to both EEPROM arrays. When it is a logic 1, it prevents any writes to the EEPROM arrays.



See [Table 3](#) for the needed command code.

**Fig 17. Read from GPIO Input Port register and write to 256-byte EEPROM**

**7.1.4 Reset**

**7.1.4.1 Power-on reset**

When power is applied to V<sub>DD</sub>, an internal Power-On Reset (POR) holds the PCA9558 in a reset state until V<sub>DD</sub> has reached V<sub>POR</sub>. At that point, the reset condition is released and the PCA9558 volatile registers and SMBus state machine will initialize to their default states.

The GPIO outputs (IO<sub>x</sub>) will be selected as outputs.

The DIP switch MUX\_OUT<sub>x</sub> and NON\_MUXED\_OUT pin values depend on:

- The MUX\_OUT\_LOW and MUX\_SELECT logic levels
- The previously stored values in the EEPROM register/current MUX\_IN<sub>x</sub> pin values as shown in [Table 4](#)

**7.1.4.2 External reset**

A reset of the GPIO registers can be accomplished by holding the IO\_OUT\_LOW pin LOW for a minimum of T<sub>cy(W)</sub>. These GPIO registers return to their default states until the IO\_OUT\_LOW input is once again HIGH.

## 7.2 Using the PCA9558 on the SMBus

It is possible to use Intel chip sets to communicate with the PCA9558. There are no limitations when the SMBus controller is communicating with the MUX or the GPIO; however, there are limitations with the 2-kbit serial EEPROM. Because of being able to address any location in the EEPROM block using the second command byte, the designer using the PCA9558 on the SMBus will have to program around it, an easy thing to do. The device designers had to deal with the specifics of addressing the EEPROM and chose the I<sup>2</sup>C-bus specification and use the second command byte to address any location in the EEPROM block.

In order to write to the EEPROM, write the EEPROM address byte in the Data0 byte and the data to be sent should be placed in the Data1 byte. The Intel chip set's Word Data instruction would then send the address, followed by the command register then Data0 (EEPROM address), and then the Data1 (data byte). A read from the EEPROM would be a two-step process. The first step would be to do a 'Write Byte' with the EEPROM address in the Data0 register. The second step would be to do a 'Receive Byte' where the data is stored in the command register.

Other differences from the *SMBus specification*:

- Paragraph 5.5.5 – Read Byte/Word in figure 5-11: The PCA9558 follows this same command code with one exception, the PCA9558 requires 2 bytes of command before the repeated START.
- Paragraph 5.5.6 – Process call in figure 5-15: The PCA9558 read operation is very similar to the SMBus process call. In the PCA9558 read operation you send a START condition – slave address with a write bit – 2 bytes of command code – repeated START – slave address with a read bit – then read data.

## 8. Application design-in information

A central processor/controller typically located on the system main board can use the 400 kHz I<sup>2</sup>C-bus/SMBus to poll the PCA9558 devices located on the system cards for status or version control type of information. The PCA9558 may be programmed at manufacturing to store information regarding board build, firmware version, manufacturer identification, configuration option data, etc. Alternately, these devices can be used as convenient interface for board configuration, thereby utilizing the I<sup>2</sup>C-bus/SMBus as an intra-system communication bus.

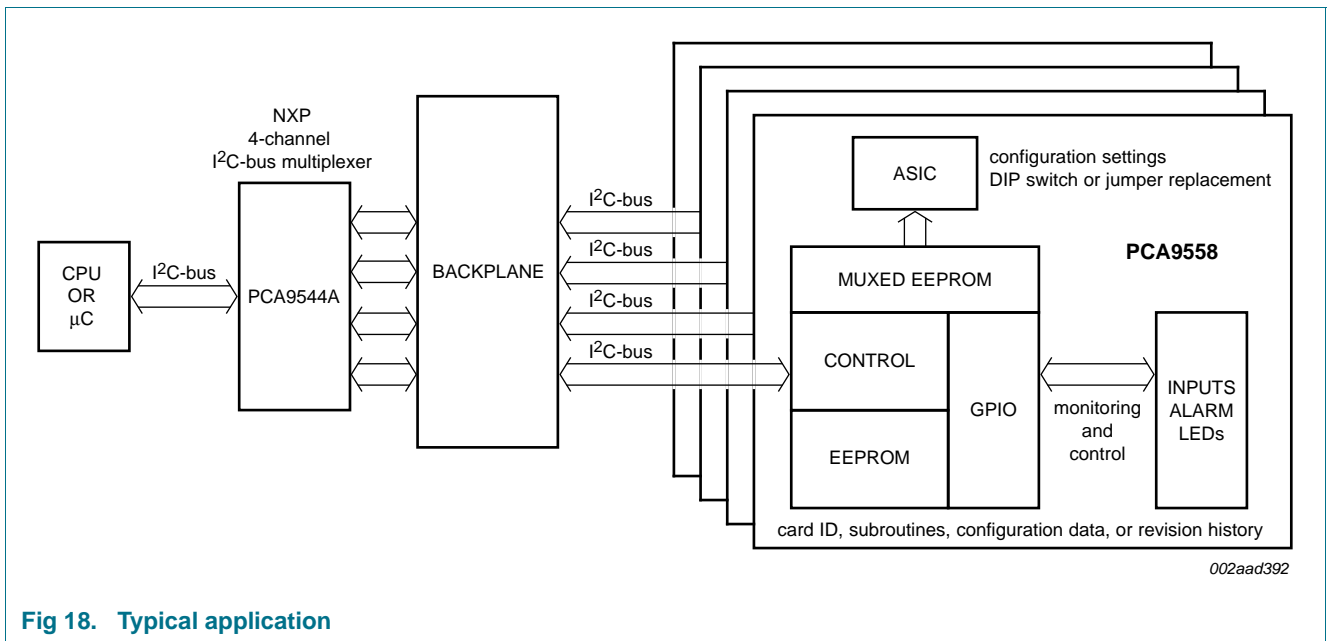


Fig 18. Typical application



## 9. Limiting values

**Table 9. Limiting values**<sup>[1]</sup>

In accordance with the Absolute Maximum Rating System (IEC 60134).  
Voltages are referenced to  $V_{SS}$  (0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD}$	supply voltage		2.5	4.6	V
$V_I$	input voltage		<sup>[2]</sup> -0.5	$V_{DD} + 0.5$	V
$V_O$	output voltage		<sup>[2]</sup> -0.5	$V_{DD} + 0.5$	V
$T_{stg}$	storage temperature		-60	+150	°C

- [1] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.
- [2] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 10. Recommended operating conditions

**Table 10. Operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD}$	supply voltage		3	-	3.6	V
$V_{IL}$	LOW-level input voltage	SCL, SDA; $I_{OL} = 3$ mA	-0.5	-	0.9	V
		$\overline{MUX\_OUT\_LOW}$ , $\overline{MUX\_INx}$ , $\overline{MUX\_SELECT}$	-0.5	-	0.8	V
$V_{IH}$	HIGH-level input voltage	SCL, SDA; $I_{OL} = 3$ mA	2.7	-	4.0	V
		$\overline{MUX\_OUT\_LOW}$ , $\overline{MUX\_INx}$ , $\overline{MUX\_SELECT}$	2.0	-	4.0	V
$V_{OL}$	LOW-level output voltage	SCL, SDA; $I_{OL} = 3$ mA	-	-	0.4	V
		SCL, SDA; $I_{OL} = 6$ mA	-	-	0.6	V
$I_{OL}$	LOW-level output current	$\overline{MUX\_OUTx}$ , $\overline{NON\_MUXED\_OUT}$ ; $V_{OL} = 0.4$ V	-	-	4	mA
$I_{OH}$	HIGH-level output current	$\overline{MUX\_OUTx}$ , $\overline{NON\_MUXED\_OUT}$	-	-	100	μA
$\Delta t/\Delta V$	input transition rise and fall rate		0	-	10	ns/V
$T_{amb}$	ambient temperature	operating	0	-	70	°C

## 11. Static characteristics

Table 11. Static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Supply</b>						
V <sub>DD</sub>	supply voltage		3.0	-	3.6	V
I <sub>CCL</sub>	LOW-level supply current	operating mode; all inputs = 0 V	-	-	10	mA
I <sub>CCH</sub>	HIGH-level supply current	operating mode; all inputs = V <sub>DD</sub>	-	-	10	mA
V <sub>POR</sub>	power-on reset voltage	no load; V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub>	-	2.3	2.6	V
<b>Input SCL; input/output SDA</b>						
V <sub>IL</sub>	LOW-level input voltage		-0.5	-	+0.8	V
V <sub>IH</sub>	HIGH-level input voltage		2	-	V <sub>DD</sub> + 0.5	V
I <sub>OL</sub>	LOW-level output current	V <sub>OL</sub> = 0.4 V	3	-	-	mA
		V <sub>OL</sub> = 0.6 V	6	-	-	mA
I <sub>LH</sub>	HIGH-level leakage current	V <sub>I</sub> = V <sub>DD</sub>	-1	-	+1	μA
I <sub>LL</sub>	LOW-level leakage current	V <sub>I</sub> = V <sub>SS</sub>	-1	-	+1	μA
C <sub>i</sub>	input capacitance		-	-	10	pF
<b>MUX_OUT_LOW, WP, MUX_SELECT</b>						
I <sub>LH</sub>	HIGH-level leakage current	V <sub>I</sub> = V <sub>DD</sub>	-	-	1	μA
I <sub>LL</sub>	LOW-level leakage current	V <sub>I</sub> = V <sub>SS</sub>	-	-	-100	μA
C <sub>i</sub>	input capacitance		-	-	10	pF
<b>MUX_INx</b>						
I <sub>LH</sub>	HIGH-level leakage current	V <sub>I</sub> = V <sub>DD</sub>	-	-	1	μA
I <sub>LL</sub>	LOW-level leakage current	V <sub>I</sub> = V <sub>SS</sub>	-	-	-100	μA
C <sub>i</sub>	input capacitance		-	-	10	pF
<b>A0 input</b>						
I <sub>LH</sub>	HIGH-level leakage current	V <sub>I</sub> = V <sub>DD</sub>	-	-	1	μA
I <sub>LL</sub>	LOW-level leakage current	V <sub>I</sub> = V <sub>SS</sub>	-	-	-100	μA
C <sub>i</sub>	input capacitance		-	-	10	pF
<b>MUX_OUTx</b>						
V <sub>OL</sub>	LOW-level output voltage	I <sub>OL</sub> = 100 μA	-	-	0.4	V
		I <sub>OL</sub> = 4 mA	-	-	0.7	V
I <sub>OH</sub>	HIGH-level output current	V <sub>OH</sub> = V <sub>DD</sub>	-	-	100	μA
<b>NON_MUXED_OUT</b>						
V <sub>OL</sub>	LOW-level output voltage	I <sub>OL</sub> = 100 μA	-	-	0.4	V
		I <sub>OL</sub> = 4 mA	-	-	0.7	V
I <sub>OH</sub>	HIGH-level output current	V <sub>OH</sub> = V <sub>DD</sub>	-	-	100	μA
<b>GPIO (IOx)</b>						
V <sub>OL</sub>	LOW-level output voltage	I <sub>OL</sub> = 100 μA	-	-	0.4	V
		I <sub>OL</sub> = 4 mA	-	-	0.7	V
I <sub>OH</sub>	HIGH-level output current	V <sub>OH</sub> = V <sub>DD</sub>	-	-	100	μA

## 12. Dynamic characteristics

Table 12. Dynamic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>MUX_INx to MUX_OUTx</b>						
t <sub>PLH</sub>	LOW to HIGH propagation delay		-	21	28	ns
t <sub>PHL</sub>	HIGH to LOW propagation delay		-	7	10	ns
<b>MUX_SELECT to MUX_OUTx</b>						
t <sub>PLH</sub>	LOW to HIGH propagation delay		-	20	28	ns
t <sub>PHL</sub>	HIGH to LOW propagation delay		-	8	12	ns
<b>MUX_OUT_LOW to NON_MUXED_OUT</b>						
t <sub>PLH</sub>	LOW to HIGH propagation delay		-	20	26	ns
t <sub>PHL</sub>	HIGH to LOW propagation delay		-	8	15	ns
<b>MUX_OUT_LOW to MUX_OUTx</b>						
t <sub>PLH</sub>	LOW to HIGH propagation delay		-	20	28	ns
t <sub>PHL</sub>	HIGH to LOW propagation delay		-	7.0	15	ns
t <sub>r</sub>	rise time	output	1.0	-	10	ns/V
t <sub>f</sub>	fall time	output	1.0	-	5	ns/V
C <sub>L</sub>	load capacitance	test load on outputs	-	-	10	pF
<b>I<sup>2</sup>C-bus</b>						
f <sub>SCL</sub>	SCL clock frequency		10	-	400	kHz
t <sub>BUF</sub>	bus free time between a STOP and START condition		1.3	-	-	μs
t <sub>HD;STA</sub>	hold time (repeated) START condition		[1] 600	-	-	ns
t <sub>LOW</sub>	LOW period of the SCL clock		1.3	-	-	μs
t <sub>HIGH</sub>	HIGH period of the SCL clock		600	-	-12	ns
t <sub>SU;STA</sub>	set-up time for a repeated START condition		600	-	-32	ns
t <sub>HD;DAT</sub>	data hold time		0	-	10	ns
t <sub>SU;DAT</sub>	data set-up time		100	-	-100	ns
t <sub>SP</sub>	pulse width of spikes that must be suppressed by the input filter		0	-	50	ns
t <sub>SU;STO</sub>	set-up time for STOP condition		600	-	10	ns
t <sub>r</sub>	rise time of both SDA and SCL signals	10 pF to 400 pF bus	20	-	300	ns
t <sub>f</sub>	fall time of both SDA and SCL signals	10 pF to 400 pF bus	20	-	300	ns
C <sub>b</sub>	capacitive load for each bus line		-	-	400	pF
T <sub>cy(W)</sub>	write cycle time		[2] -	15	-	ms

[1] After this period, the first clock pulse is generated.

[2] Write cycle time can only be measured indirectly during the write cycle. During this time, the device will not acknowledge its I<sup>2</sup>C-bus address.

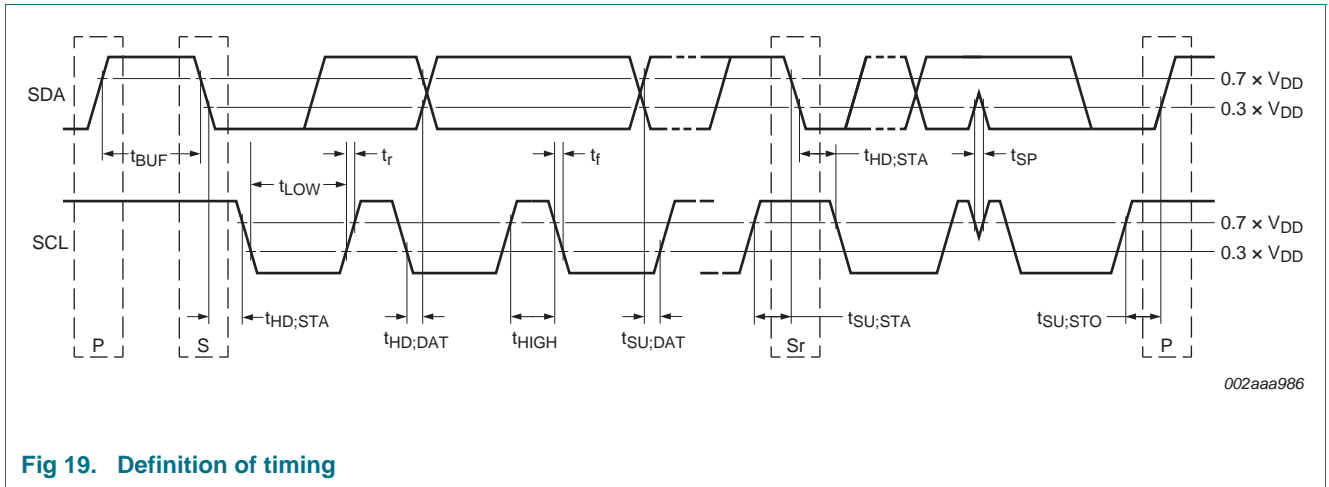


Fig 19. Definition of timing

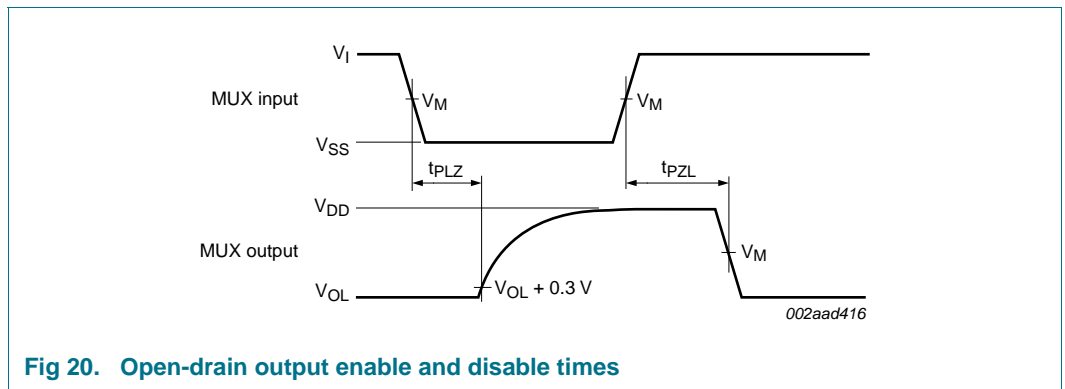


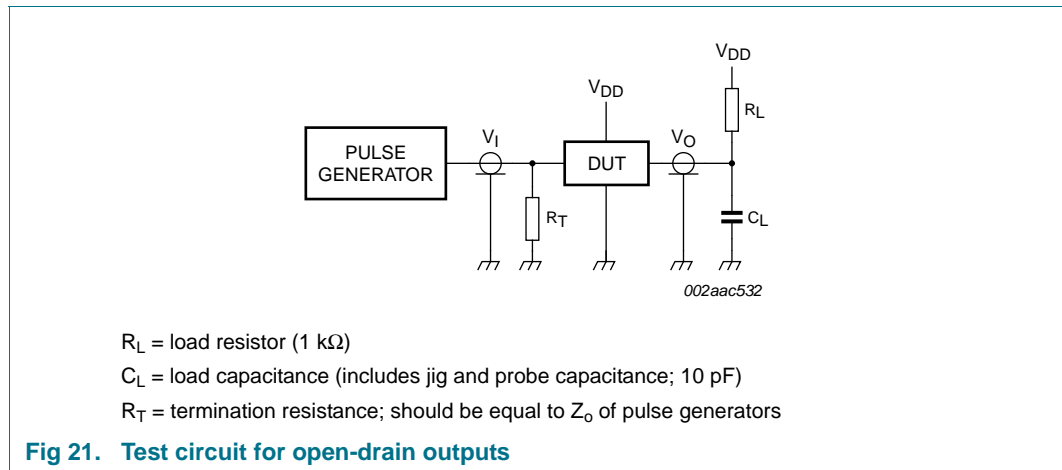
Fig 20. Open-drain output enable and disable times

### 13. Non-volatile storage specifications

Table 13. Non-volatile storage specifications

Parameter	Specification
memory cell data retention	10 years (minimum)
number of memory cell write cycles	100,000 cycles (minimum)

## 14. Test information



### 15. Package outline

TSSOP28: plastic thin shrink small outline package; 28 leads; body width 4.4 mm

SOT361-1

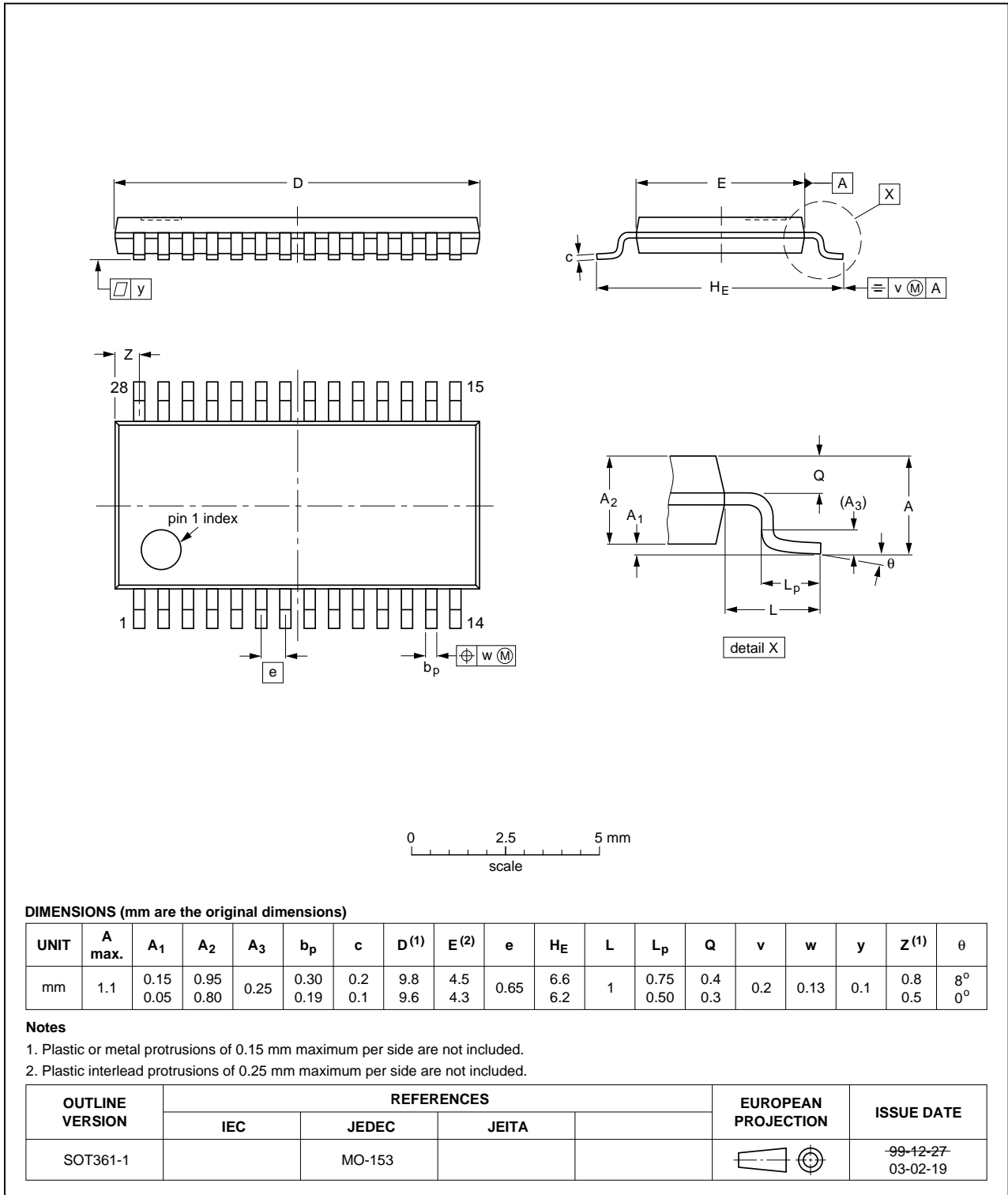


Fig 22. Package outline SOT361-1 (TSSOP28)

## 16. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note AN10365 “Surface mount reflow soldering description”.

### 16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

## 16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 23](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 14](#) and [15](#)

**Table 14. SnPb eutectic process (from J-STD-020C)**

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm <sup>3</sup> )	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

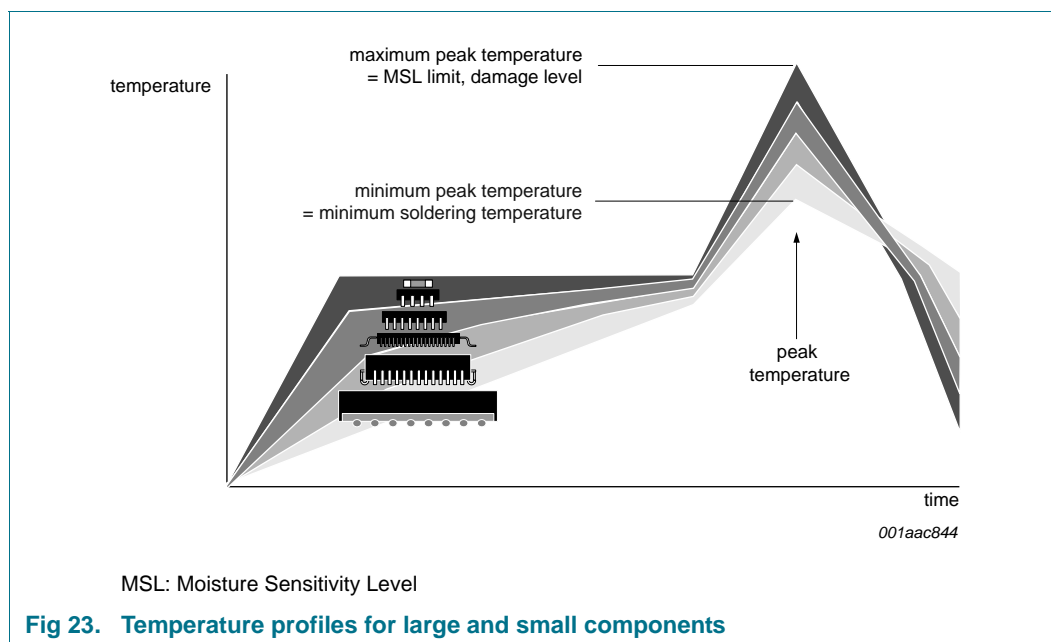
**Table 15. Lead-free process (from J-STD-020C)**

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm <sup>3</sup> )		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 23](#).





For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

## 17. Abbreviations

**Table 16. Abbreviations**

Acronym	Description
ASIC	Application Specific Integrated Circuit
CDM	Charged Device Model
CPU	Central Processing Unit
DIP	Dual In-line Package
DUT	Device Under Test
EEPROM	Electrically-Erasable Programmable Read-Only Memory
ESD	ElectroStatic Discharge
GPIO	General Purpose Input/Output
HBM	Human Body Model
I/O	Input/Output
I <sup>2</sup> C-bus	Inter-Integrated Circuit bus
LED	Light Emitting Diode
LSB	Least Significant Bit
MSB	Most Significant Bit
POR	Power-On Reset
SMBus	System Management Bus
μC	microcontroller

## 18. Revision history

Table 17. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9558 v.5	20120625	Product data sheet	-	PCA9558 v.4
Modifications:	<ul style="list-style-type: none"> <li>• <a href="#">Section 2 "Features and benefits"</a>, 13th bullet: deleted "200 V MM per JESD22-A115"</li> <li>• <a href="#">Table 8 "IOC - Input/Output Configuration register description"</a>: default corrected from "1111 1111" to "0000 0000" (documentation correction only, there is no change in silicon)</li> <li>• <a href="#">Table 16 "Abbreviations"</a>: deleted row "MM, Machine Model"</li> </ul>			
PCA9558 v.4	20090414	Product data sheet	-	PCA9558 v.3
PCA9558 v.3 (9397 750 11674)	20030627	Product data	ECN 853-2235 29936 of 19 May 2003	PCA9558 v.2
PCA9558 v.2 (9397 750 09889)	20020524	Product data	ECN 853-2235 28310 of 24 May 2002	PCA9558 v.1
PCA9558 v.1	20001204	Product specification	-	-

## 19. Legal information

### 19.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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