Advantech

AQD-SD21GN80-SX
Datasheet

Rev. 0.0

2014-9-25

Description

AQD-SD21GN80-SX is 128Mx64 bits DDR2 SDRAM Module, The module is composed of eight 128Mx8 bits CMOS DDR2 SDRAMs in FBGA package and one 2Kbit EEPROM in 8pin TSSOP(TSOP) package on a 200pin glass–epoxy printed circuit board.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operation frequencies, programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

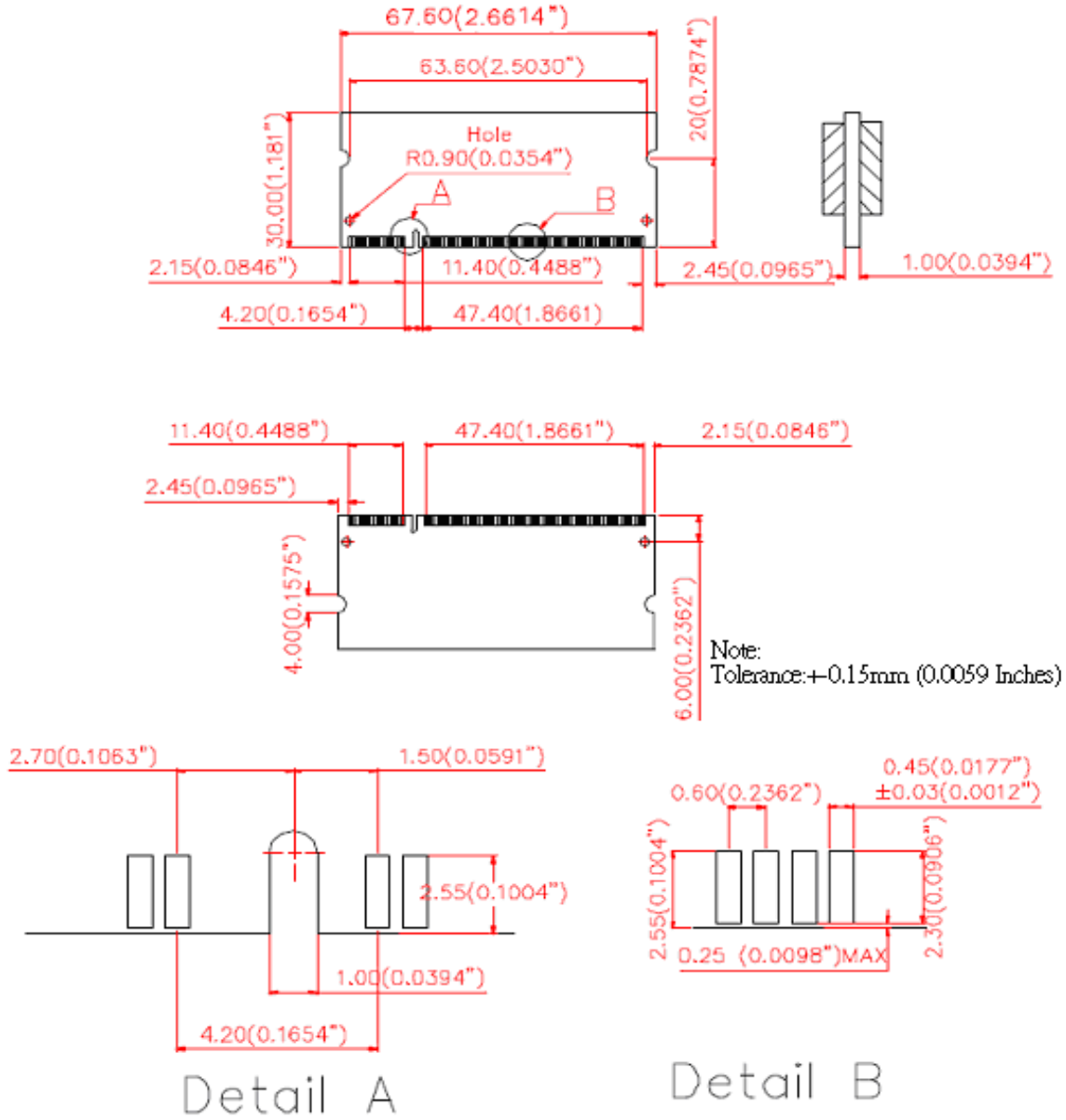
Features

- Power supply (Normal): VDD & VDDQ = 1.8V ± 0.1V
- 1.8V (SSTL_18 compatible) I/O
- MRS Cycle with address key programs
  - CAS Latency (4, 5, 6)
  - Burst Length (4,8)
- Programmable Additive Latency: 0,1,2,3,4,5
- Bi-directional, differential data strobe (DQS and /DQS)
- Differential clock input (CK, /CK) operation
- DLL aligns DQ and DQS transition with CK transition
- Double-data-rate architecture
- Auto refresh and self refresh
- Average Refresh period 7.8 us
- Off-Chip Driver (OCD) Impedance Adjustment
- On Die Termination
- Lead-free and Halogen-free products are RoHS Compliant

Pin Identification

Symbol	Function
A0~A13, BA0~BA2	Address/Bank input
DQ0~DQ63	Bi-direction data bus.
DQS0~DQS7	Data strobes
/DQS0~/DQS7	Differential Data strobes
CK0, /CK0,CK1, /CK1	Clock Input. (Differential pair)
CKE0, CKE1	Clock Enable Input.
ODT0, ODT1	On-die termination control line
/CS0 ,/CS1	DIMM rank select lines.
/RAS	Row address strobe
/CAS	Column address strobe
/WE	Write Enable
DM0~DM7	Data masks/high data strobes
VDD	Core power supply
V_{REF}	Power Supply reference
V_{DD}SPD	SPD EEPROM power supply
SA0~SA1	I2C serial bus address select for EEPROM
SCL	I2C serial bus clock for EEPROM
SDA	I2C serial bus data for EEPROM
VSS	Ground
NC	No Connection

Dimensions (Unit: millimeter)

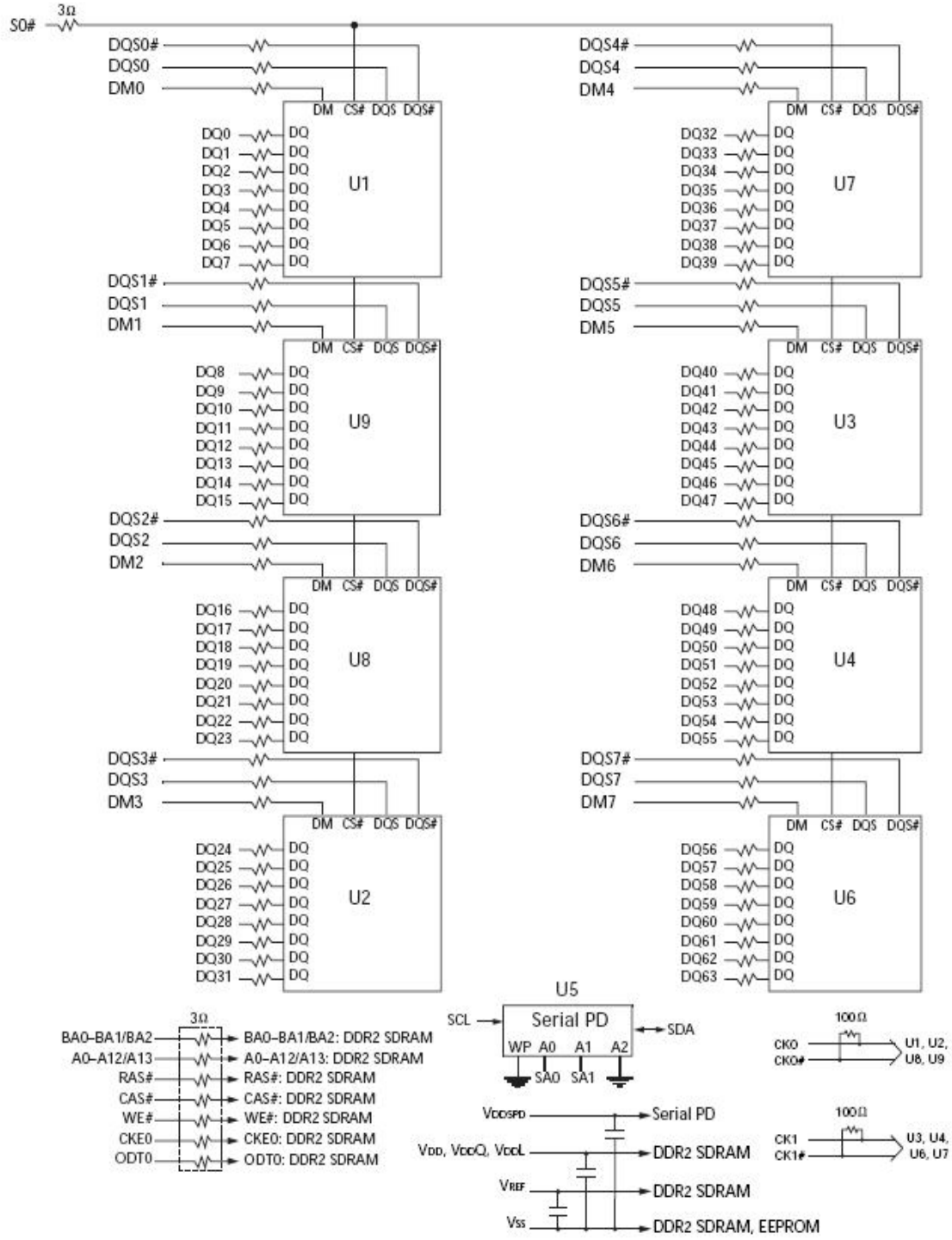


Note:1. Tolerances on all dimensions +/-0.15mm unless otherwise specified.

Pin Assignments

PIN	Name	PIN	Name	PIN	Name	PIN	Name		PIN	Name	PIN	Name	PIN	Name	PIN	Name
1	VREF	51	DQS2	101	A1	151	DQ42		2	VSS	52	DM2	102	A0	152	DQ46
3	VSS	53	VSS	103	VDD	153	DQ43		4	DQ4	54	VSS	104	VDD	154	DQ47
5	DQ0	55	DQ18	105	A10/AP	155	VSS		6	DQ5	56	DQ22	106	BA1	156	VSS
7	DQ1	57	DQ19	107	BA0	157	DQ48		8	VSS	58	DQ23	108	/RAS	158	DQ52
9	VSS	59	VSS	109	/WE	159	DQ49		10	DM0	60	VSS	110	/CS0	160	DQ53
11	/DQS0	61	DQ24	111	VDD	161	VSS		12	VSS	62	DQ28	112	VDD	162	VSS
13	DQS0	63	DQ25	113	/CAS	163	NC		14	DQ6	64	DQ29	114	ODT0	164	CK1
15	VSS	65	VSS	115	/CS1	165	VSS		16	DQ7	66	VSS	116	NC/A13	166	/CK1
17	DQ2	67	DM3	117	VDD	167	/DQS6		18	VSS	68	/DQS3	118	VDD	168	VSS
19	DQ3	69	NC	119	ODT1	169	DQS6		20	DQ12	70	DQS3	120	NC	170	DM6
21	VSS	71	VSS	121	VSS	171	VSS		22	DQ13	72	VSS	122	VSS	172	VSS
23	DQ8	73	DQ26	123	DQ32	173	DQ50		24	VSS	74	DQ30	124	DQ36	174	DQ54
25	DQ9	75	DQ27	125	DQ33	175	DQ51		26	DM1	76	DQ31	126	DQ37	176	DQ55
27	VSS	77	VSS	127	VSS	177	VSS		28	VSS	78	VSS	128	VSS	178	VSS
29	/DQS1	79	CKE0	129	/DQS4	179	DQ56		30	CK0	80	CKE1	130	DM4	180	DQ60
31	DQS1	81	VDD	131	DQS4	181	DQ57		32	/CK0	82	VDD	132	VSS	182	DQ61
33	VSS	83	NC	133	VSS	183	VSS		34	VSS	84	NC	134	DQ38	184	VSS
35	DQ10	85	NC/BA2	135	DQ34	185	DM7		36	DQ14	86	NC	136	DQ39	186	/DQS7
37	DQ11	87	VDD	137	DQ35	187	VSS		38	DQ15	88	VDD	138	VSS	188	DQS7
39	VSS	89	A12	139	VSS	189	DQ58		40	VSS	90	A11	140	DQ44	190	VSS
41	VSS	91	A9	141	DQ40	191	DQ59		42	VSS	92	A7	142	DQ45	192	DQ62
43	DQ16	93	A8	143	DQ41	193	VSS		44	DQ20	94	A6	144	VSS	194	DQ63
45	DQ17	95	VDD	145	VSS	195	SDA		46	DQ21	96	VDD	146	/DQS5	196	VSS
47	VSS	97	A5	147	DM5	197	SCL		48	VSS	98	A4	148	DQS5	198	SA0
49	/DQS2	99	A3	149	VSS	199	VDDSPD		50	NC	100	A2	150	VSS	200	SA1

1GB, 1Gbx8 Module(1 Rank x8)



Operating Temperature Condition

Parameter	Symbol	Rating	Unit	Note
Operating Temperature	TOPER	0 to 95	°C	1,2

Note: Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

Absolute Maximum DC Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on V_{DD} relative to Vss	VDD	-0.5 ~ +2.3	V	1
Voltage on V_{DDQ} pin relative to Vss	VDDQ	-0.5 ~ +2.3	V	1
Voltage on any pin relative to Vss	VIN, VOUT	-0.5 ~ +2.3	V	1
Storage temperature	T_{STG}	-55~+100	°C	1,2

Note:
1. Stress greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

AC & DC Operating Conditions

Recommended DC operating conditions

Parameter	Symbol	Voltage	Rating			Unit	Notes
			Min	Typ.	Max		
Supply voltage	VDD	1.8V	1.7	1.8	1.9	V	1, 2
Supply voltage for Output	VDDQ	1.8V	1.7	1.8	1.9	V	1, 2
I/O Reference Voltage (DQ)	$VREF_{DQ}$(DC)	1.8V	0.49*VDDQ	0.50*VDDQ	0.51*VDDQ	V	3
I/O Reference Voltage (CMD/ADD)	$VREF_{CA}$(DC)	1.8V	0.49*VDDQ	0.50*VDDQ	0.51*VDDQ	V	3
AC Input Logic High	VIH(AC)	1.8V	VREF+0.125	-	-	V	
AC Input Logic Low	VIL(AC)	1.8V	-	-	VREF-0.125	V	
DC Input Logic High	VIH(DC)	1.8V	VREF+0.125	-	VDDQ+0.3	V	
DC Input Logic Low	VIL(DC)	1.8V	-0.3	-	VREF-0.125	V	

Note:
1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD, AC parameters are measured with VDD and VDDQ tied together.
3. Peak to peak AC noise on VREF may not allow deviate from VREF(DC) by more than +/-1% VDD.

IDD Specification parameters Definition - 1GB (1 Rank x8)

Parameter	Symbol	DDR 800 CL6	Unit
Operating One bank Active-Precharge current; tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD); CKE is HIGH, /CS is HIGH between valid commands;Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD0	TBD	mA
Operating One bank Active-read-Precharge current; IOUT = 0mA; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRC = tRC (IDD), tRAS = tRASmin(IDD), tRCD = tRCD(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	IDD1	TBD	mA
Precharge power-down current; All banks idle; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2P	TBD	mA
Precharge quiet standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, /CS is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2Q	TBD	mA
Precharge standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, /CS is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD2N	TBD	mA
Active power - down current; All banks open; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD3P	TBD	mA
Active standby current; All banks open; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD3N	TBD	mA
Operating burst read current; All banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	IDD4R	TBD	mA
Operating burst write current; All banks open, Continuous burst writes; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING IDD4R	IDD4W	TBD	mA
Burst refresh current; tCK = tCK(IDD); Refresh command at every tRFC(IDD) interval; CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD5	TBD	mA
Self refresh current; CK and /CK at 0V; CKE ≒ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	IDD6	TBD	mA
Operating bank interleave read current; All bank interleaving reads, IOUT = 0mA; BL = 8, CL = CL(IDD), AL = tRCD(IDD)-1*tCK(IDD); tCK = tCK(IDD), Trc = tRC(IDD), tRRD = tRRD(IDD), tRCD = 1*tCK(IDD); CKE is HIGH, CS is HIGH between valid commands;Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R;	IDD7	TBD	mA

Note: 1.Module IDD was calculated on the specific brand DRAM(35nm) component IDD and can be differently measured according to DQ loading capacitor.

Timing Parameters & Specifications

Speed		DDR2 800		Unit
Parameter	Symbol	Min	Max	
Average Clock Period	tCK	2500	8000	ps
CK high-level width	tCH	0.48	0.52	tCK
CK low-level width	tCL	0.48	0.52	tCK
DQS, /DQS to DQ skew, per group, per access	tDQSQ	-	200	ps
DQ output hold time from DQS, /DQS	tQH	tHP - tQHS	-	ps
DQ low-impedance time from CK, /CK	tLZ(DQ)	2 x tAC,min	tAC,max	ps
DQ high-impedance time from CK, /CK	tHZ(DQ)	-	tAC,max	ps
Data setup time to DQS, /DQS reference to Vih(ac)Vil(ac) levels	tDS	50	-	ps
Data hold time to DQS, /DQS reference to Vih(ac)Vil(ac) levels	tDH	125		ps
DQ and DM input pulse width for each input	tDIPW	0.35	-	tCK(avg)
DQS, /DQS Read preamble	tRPRE	0.9	1.1	tCK
DQS, /DQS differential Read postamble	tRPST	0.4	0.6	tCK
DQS, /DQS Write preamble	tWPRE	0.35	-	tCK
DQS, /DQS Write postamble	tWPST	0.4	0.6	tCK
DQS, /DQS low-impedance time	tLZ(DQS)	tAC,min	tAC,max	ps
DQS, /DQS high-impedance time	tHZ(DQS)	-	tAC,max	ps
DQS, /DQS differential input low pulse width	tDQSL	0.35	0.55	tCK
DQS, /DQS differential input high pulse width	tDQSH	0.35	0.55	tCK
DQS, /DQS rising edge to CK, /CK rising edge	tDQSS	-0.25	0.25	tCK
DQS, /DQS falling edge setup time to CK, /CK rising edge	tDSS	0.2	-	tCK
DQS, /DQS falling edge hold time to CK, /CK rising edge	tDSH	0.2	-	tCK
Delay from start of Internal write transaction to Internal read command	tWTR	7.5	-	ns
Write recovery time	tWR	15	-	ns
Mode register set command cycle time	tMRD	2	-	nCK
/CAS to /CAS command delay	tCCD	2	-	nCK
Auto precharge write recovery + precharge time	tDAL	WR + tnRP		nCK
Active to active command period for	tRRD	7.5	-	ns

1KB page size				
Speed		**DDR2 800**		**Unit**
Parameter	**Symbol**	**Min**	**Max**	
Active to active command period for 2KB page size	tRRD	10	-	ns
Four Activate Window for 1KB page size	tFAW	35	-	ns
Exit self refresh to commands not requiring a locked DLL	tXSNR	tRFC (MIN) + 10	-	ns
Internal read to precharge command delay	tRTP	7.5	-	ns
Exit power down with DLL to any valid command: Exit Precharge Power Down with DLL	tXP	2	-	tCK
CKE minimum pulse width (high and low pulse width)	tCKE	3	-	tCK
Asynchronous RTT turn-on delay (Power-Down mode)	tAONPD	tAC (MIN) + 2000	2 × tCK + tAC (MAX) + 1000	ps
Asynchronous RTT turn-off delay (Power-Down mode)	tAOFPD	tAC (MIN) + 2000	2.5 × tCK + tAC (MAX) + 1000	ps
ODT turn-on	tAON	tAC (MIN)	tAC (MAX) + 600	ps
ODT turn-off	tAOF	tAC (MIN)	tAC (MAX) + 600	ps

SERIAL PRESENCE DETECT SPECIFICATION

AQD-SD21GN80-SX Serial Presence Detect			
Byte No.	**Function Described**	**Standard Specification**	**Vendor Part**
0	Number of Serial PD Bytes written during module production	128 bytes	80
1	Total number of Bytes in Serial PD device	256 bytes	08
2	Fundamental Memory Type (FPM, EDO, SDRAM, DDR, DDR2…)	DDR2 SDRAM	08
3	Number of Row Addresses on this assembly	14	0E
4	Number of Column Addresses on this assembly	10	0A
5	Number of DIMM Ranks	1 Rank	60
6	Data Width of this assembly	64 bits	40
7	Reserved		00
8	Voltage Interface Level of this assembly	SSTL 1.8V	05
9	SDRAM Cycle time at Maximum Supported CAS Latency (CL), CL=X	2.5ns	25
10	SDRAM Access from Clock	0.4ns	40
11	DIMM configuration type (Non-parity, Parity or ECC)	-	00
12	Refresh Rate/Type	7.8 us	82
13	Primary SDRAM Width	8 bits	08
14	Error Checking SDRAM Width	-	00
15	Reserved	-	00
16	SDRAM Device Attributes: Burst Lengths Supported	4.8	0C
17	SDRAM Device Attributes: Number of Banks on SDRAM Device	8 banks	08
18	SDRAM Device Attributes: CAS Latency	6.5.4	70
19	DIMM Mechanical Characteristics	-	01
20	DIMM Type Information	SO-DIMM	04
21	SDRAM Module Attributes	-	00
22	SDRAM Device Attributes: General	50ohm ODT/Weak Driver	03
23	Minimum Clock Cycle at CLX-1	3 ns	30
24	Maximum Data Access Time (tAC) from Clock at CLX-1	0.45 ns	45
25	Minimum Clock Cycle at CLX-2	3.75 ns	3D
26	Maximum Data Access Time (tAC) from Clock at CLX-2	0.5 ns	50
27	Minimum Row Precharge Time (tRP)	15 ns	3C
28	Minimum Row Active to Row Active delay (tRRD)	7.5 ns	1E
29	Minimum RAS to CAS delay (tRCD)	15 ns	3C
30	Minimum Active to Precharge Time (tRAS)	45 ns	2D
31	Module Rank Density	1GB	01
32	Address and Command Input Setup Time Before Clock (tIS)	0.175 ns	18
33	Address and Command Input Hold Time After Clock (tIH)	0.25 ns	25
34	Data Input Setup Time Before Strobe (tDS)	0.05 ns	05
35	Data Input Hold Time After Strobe (tDH)	0.125 ns	13
36	Write recovery time (tWR)	15 ns	3C
37	Internal write to read command delay (tWTR)	7.5 ns	1E
38	Internal read to precharge command delay (tRTP)	7.5 ns	1E

39	Memory Analysis Probe Characteristics	-		00
40	Extension of Byte 41 tRC and Byte 42 tRFC	0	0.5	06
41	SDRAM Device Minimum Active to Active/Refresh Time (tRC)	60 ns		3C
42	SDRAM Device Minimum Refresh to Active/Refresh Command Period (tRFC)	127.5 ns		7F
43	SDRAM Device Maximum device cycle time (tCKmax)	8 ns		80
44	SDRAM Device maximum skew between DQS and DQ signals (tDQSQ)	0.2 ns		14
45	SDRAM Device Maximum Read Data Hold Skew Factor (tQHS)	0.3 ns		1E
46	PLL Relock Time	-		00
47-61	Superset Information (may be used in future)	-		00
62	62 SPD Revision	1.2		12
63	Checksum for Bytes 0-62	checksum data		E0
64	Manufacturer JEDEC ID code	A-DATA		7F
65				7F
66				7F
67				7F
68				CB
69				00
70				00
71				00
72	Manufacturing location	*Note: 1		-
73-90	Manufacturer Part Number	*Note: 2		-
91-92	Manufacturer Revision Code	Undefined		00
93	Manufacturing Date (Year)	*Note: 3		-
94	Manufacturing Data (week)	*Note: 4		-
95-98	Module Serial Number	*Note: 5		00
99-112	Manufacturer's Specific Data (Working Order Number)	*Note: 6		-
113-124	Manufacturer's Specific Data (SPD Naming Number)	*Note: 7		-
125-127	Manufacturer's Specific Data	Undefined		00
128-255	Open for customer use	*Note: 8		00

***Note :**

1. Byte 72 -- Manufacturing location by manufacturing location (00:Taiwan /01:China)
2. Bytes 73~90 -- Manufacturer Part Number by module part number , Unused digits are coded as ASCII blanks (20h).
3. Byte 93 -- Manufacturing Date by Date Year (YY).
4. Byte 94 -- Manufacturing Date by Date Week (WW).
5. Byte 95~98 -- Module Serial Number by module serial number. ---> In the future. Digits are coded as 00h now.
6. Byte 99~112 -- Manufacturer's Specific Data by working order number. Unused digits are coded as 00h.
7. Byte 113~124 -- Manufacturer's Specific Data by SPD naming number. Unused digits are coded as 00h.
8. Byte 128~255 --These bytes are Undefined and can be used for A-DATA's own purpose.
   Digits are coded as 00h or FFh now.