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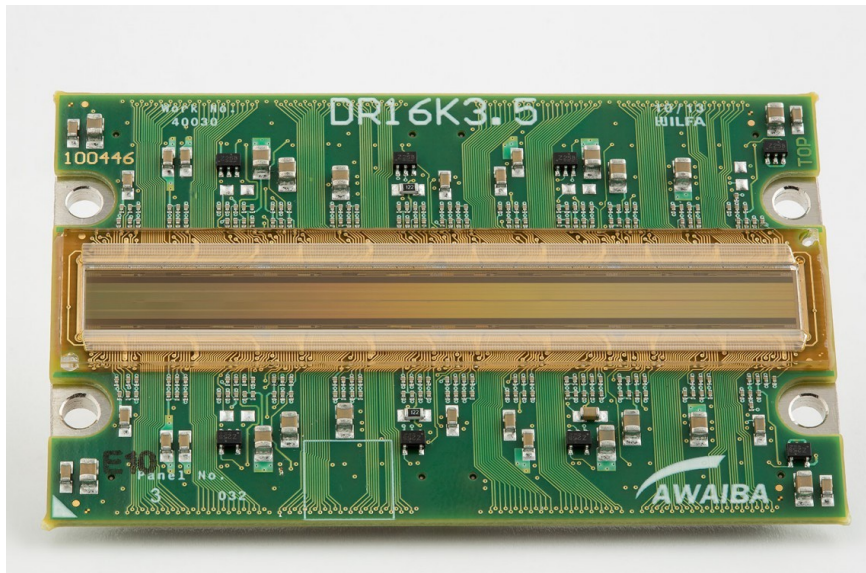
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DRAGSTER

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1 Introduction

DRAGSTER is a platform of a digital line-scan sensors. The sensor family is made using three types of basic elements: a single line element with 2048 pixel resolution and 7μm pixel size and pitch, a dual line element with 2048 pixel resolution and 7μm pixel size and pitch and a 4096 pixels element with 3.5μm pixel size and pitch. Any of the following types can be made, where "1x" means single line and "2x" means dual line:

Line	Resolution
1x	2K
	4K
	6K
	8K
	16K
	24K
2x	2K
	4K
	8K

The chip versions with dual line are optionally available with Bayer Pattern RGB filters placed on the sensors.

For all variations the basic readout and control electronics are identical. Other different variations of pixel aspect ratios can be implemented, please contact AWAIBA if you require customized resolution sensors based on Dragster architecture.

The current specification covers the following device variations:

Part Number	Number of pixels	Pixel size	Package Type
DR-B&W-2K-7-LCC	1x2048	7μm x 7μm	LCC
DR-B&W-2K-7-Invar	1x2048	7μm x 7μm	Invar module
DR-B&W-4K-3.5-LCC	1x4096	3.5μm x 3.5μm	LCC
DR-B&W-4K-3.5-Invar	1x4096	3.5μm x 3.5μm	Invar module
DR-B&W-4K-7-Invar	1x4096	7μm x 7μm	Invar module
DR-B&W-6K-7-Invar	1x6175	7μm x 7μm	Invar module
DR-B&W-8K-3.5-Invar	1x8192	3.5μm x 3.5μm	Invar module
DR-B&W-8K-7-Invar	1x8192	7μm x 7μm	Invar module

DR-B&W-16K-3.5-Invar	1x16384	3.5μm x 3.5μm	Invar module
DR-B&W-24K-3.5-Invar	1x24640	3.5μm x 3.5μm	Invar module
DR-B&W-2x2K-7-LCC DR-RGB-2x2K-7-LCC	2x2048	7μm x 7μm	LCC
DR-B&W-2x2K-7-Invar DR-RGB-2x2K-7-Invar	2x2048	7μm x 7μm	Invar module
DR-B&W-2x4K-7-Invar DR-RGB-2x4K-7-Invar	2x4096	7μm x 7μm	Invar module
DR-B&W-2x8K-7-Invar** DR-RGB-2x8K-7-Invar**	2x8192	7μm x 7μm	Invar module

** sales restrictions may apply to some markets

2 External Components
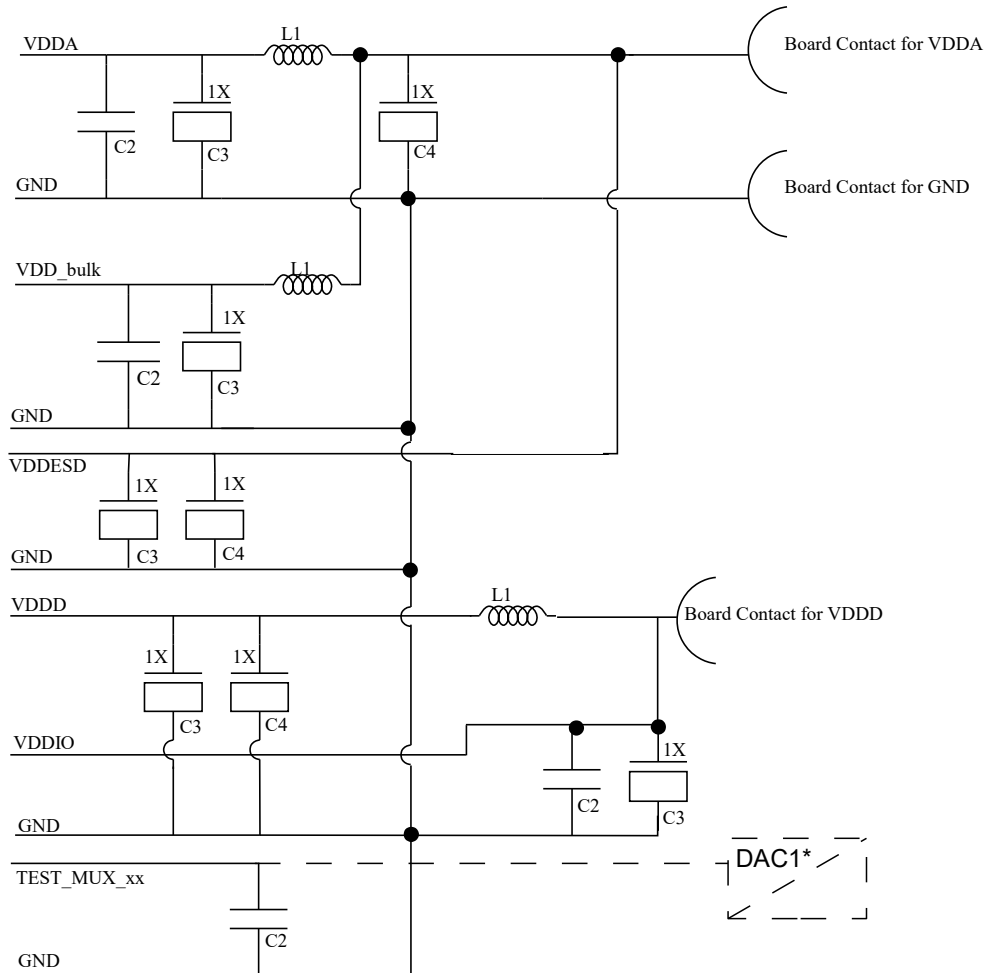
*Fig 1: Recommended power supply strategy for the sensor head board. *The component DAC1 is optional*

Component	Description	Nominal value	Tolerance	Voltage range
C2	Power decoupling capacitor, close to each VDDx connector pin low ESR Ceramic	10nF	+/- 25%	>3.6V
C3	Power decoupling capacitor, placed one time per power supply. Tantal type.	10uF	+/- 25%	>3.6V
C4	Power decoupling capacitor, placed one time per power supply. Tantal type.	100uF	+/- 25%	>3.6V
L1	Power decoupling inductance	10nH	+/- 25%	dimension according power consumption of respective sensor variation
C5	Additional decoupling capacitor on the outputs of TEST_MUX *	10nF	+/- 25%	>3.6V

Table 1: Recommended values for capacitors and inductances

* optional additional components 1) If the "TEST_MUX_XX_#" signals are accessible an additional capacitance should be placed in this signal and then by writing Register 0x0A with the value 0x0F the line by line offset noise is reduced significantly.

3 Electrical Description

The sensor will comply to the specifications listed in this section within the operating ranges listed in the respective section.

An applied signal must not have a deviation from the ideal signal, at the pin of the circuit, such that the circuit or the parameter under test are affected significantly.

Proper decoupling of the circuit according to chapter 2 is required. The following section defines the limits of functional operation and parametric characteristics of the circuit, and reliability. Note that functionality of the circuit outside the operating range as specified in this section is not guaranteed.

3.1 Absolute Maximum Ratings

Stresses above those listed in this clause may cause immediate and permanent device failure. Operation outside the operating conditions for extended periods may affect device reliability. It is not implied that more than one of these conditions can be violated simultaneously.

Total cumulative dwell time above the maximum operating rating for temperature must be less than 100 hours.

Symbol	Description	Min	Max	Unit
VDD	Power supply voltage (digital)	-0.3	3.6	V
VIO	Voltage on any IO	-0.3	VDDIO +0.3 or 3.6	V
IIO	DC forward BIAS current, input or output		-24 (source) +24 (sink)	mA
Tj	Junction temperature	-55	125	°C

Table 2: Absolute maximum ratings

3.2 Electrical overstress immunity

Electrostatic discharges on component level:
The device withstands 1k Volts Human Body Model ESD pulses when tested according to MIL STD 883 method 3015.7

3.3 Latch-up immunity

Static latch-up protection level is 10mA at 25°C when tested according to EIA/JESD78.

3.4 Operating Conditions

Symbol	Description	Min	Typical	Max	Unit
VDDD	Power supply voltage (digital)	3.2	3.3	3.4	V
VDDA	Power supply voltage (analogue)	3.2	3.3	3.4	V
VDDESD	Power supply voltage ESD	3.2	3.3	3.4	V
VDDIO	Power supply voltage IO	2.4*	3.3	3.4	V
GND	Ground supply		0		V
Fclk	Input Clock Frequency	1**		85***	MHz
Duty clk	Input Clock Duty cycle up to 50MHz	45	55	70	%
Duty clk	Input Clock Duty cycle up to >50MHz	55	57	65	%
Jitter clk	Input Clock Jitter			<5% Tclk	% Tclk
Cload	Load capacitance on digital I/O's			10	pF
Tj	Junction temperature	0	27	+80	°C
VnrmsVDDD	RMS Noise on VDD digital			20	mV
VnppVDDD	Peak to Peak Noise on VDD digital			100	mV
VnrmsVDDA	RMS Noise on VDD analogue			5	mV
VnppVDDA	Peak to Peak Noise on VDD analogue			20	mV
VnrmsVDD/IO	RMS Noise on VDD I/O			20	mV
VnppVDD/IO	Peak to Peak Noise on VDD I/O			100	mV
Vil	Low level input voltage	-0.3	0	0.4	V
Vih	High level input voltage	0.8xVDD/IO	VDD/IO	VDD/IO +0.3	V
Tsetup, data in	Setup Time for digital input signals relative to rising edge of Mclk at Mclk pin	3			ns
Thold, data in	Hold Time for digital input signals relative to rising edge of Mclk st Mclk pin	3			ns
Tsetup, MOSI	Setup Time for MOSI input signals relative to rising edge of SCLK	3			ns
Thold, MOSI	Hold Time for MOSI input signals relative to rising edge of SCLK	5			ns

Table 3: Operating conditions

* VDDIO < 3.0V is not recommended for pixel_clock speeds above 40MHz and may not meet the slew rate specifications in all cases.

** Fclk can be lower then 1MHz however the ADC conversion accuracy might be reduced.   *** The ADC can be clocked with up to 100MHz for faster conversion when using clock reduction for readout.

3.5 Electrical characteristics

Current consumptions are for one segment of 2k pixels, multiples apply for higher resolution sensors.

Symbol	Description	Min	Max	Unit
Vol	Low level output voltage		0.5	V
Voh	High level output voltage	VDD/IO-0.6		V
Iil	Low level input leakage (Vi=0)		+/-1	uA
Iih	High level input leakage (Vi=VDD/IO)		+/-1	uA
tslew, rising*	Output slew rate of rising edge		5	ns
tslew, falling*	Output slew rate of falling edge		5	ns
Ptot	Power Consumption per 2k segment		400	mW
I (VDDA)	Current to analog devices per 2k segment		50	mA
I (VDDD)	Current to Digital devices per 2k segment		30	mA
I (VDDIO)	Current for I/O per 2k segment		40	mA

Table 4: Electrical characteristics

* The output swing on signal pixel_clock (if enabled) may be smaller at pixel clock rates above 60MHz

Resulting maximum current consumption for the different chip variations

Sensor	I(VDDA) / mA	I(VDDD) / mA	I(VDDIO) / mA *	Ptot /mW ** (total power consumption)
DR-2k-7-Invar	50	30	40	400
DR-4k-3.5-Invar	100	120	80	800
DR-2x2k-7-Invar	100	120	80	800
DR-4k-7	100	60	80	800
DR-8k-7	260	150	160	1850
DR-8k-3.5	200	120	160	1600
DR-16k-3.5	520	320	160	3500
DR-24K-3.5	680	460	240	5100[1]
DR-2x4k-7	200	120	160	1600
DR-2x8k-7	500	240	320	3500

Table 5: Power consumption for Dragster Invar package

Sensor	I(VDDA) / mA	I(VDDA) / mA	Ptot /mW ** (total power consumption)
DR-2k-7-LCC	75	65	460
DR-4k-3.5-LCC	240	170	920
DR-2x2k-7-LCC	240	170	9200

Table 6: Power consumption for Dragster LCC package

* @ 10pF
** At VDDDIO = 3.3V 46MHz Cload dig 10pF 20% I/O activity

(1) The consumption of the FPGA depends on user programming and is additional to the sensor consumption of 6x the 4k segment. The stated consumption is based on AWAIBA's FPGA sample code implementation.

3.6 Optical characteristics DR-2k-7, DR-4k-7, DR-6k-7, DR-8k-7

Parameter	Min	Typ/ Target	Max	Unit
Pixel size		7 x 7		µm
Pixel pitch in x direction		7		µm
Number of dark pixels in most left segment		32		pixels
Fill Factor		100		%
Quantum efficiency at 630nm	50	60	70	%
Full Well capacity (4)	30	46	65	ke-
Total System Gain K		0.076		DN/e-
DSNU rms (1;5)		4	10	DN/12bit
Responsivity (1)		77		DN/nJ/cm2 (@12bit)
Responsvity analogue gain 4x (6)		310		DN/nJ/cm2 (@12bit)
PRNU rms (1;5)		0.7%	3%	% (full scale)
PRNU pp (1; 5)		4%	8%	% (full scale)
ADC Programmable gain	-6		20	dB
ADC gain resolution		8		bit
Blooming overload tolerance	100x	infinite		
Lag		0	0.01	%
Crosstalk (optical & electrical)		2	5	%
Exposure time range	2		infinite	us
Temporal noise Dark rms (2)*		1.5	4	DN/12bit
Dark noise electrons rms (2)*		22		e-
NEE (noise equivalent energy) unity gain (1)		0.02		nJ/cm2
Temporal noise Dark rms gain 4x (6)*		2.9	5	DN/12bit
Dark noise electrons rms gain 4x (6)*		7		e-
NEE (noise equivalent energy) analogue gain x4 (6)*		0.01		nJ/cm2
Non Linearity (3)		2	5	%
Dark current @27C		3	50	e-/ms
Maximum Line Rate			80	kScan/s
ADC Resolution		12 (13)**		bit
Number of output taps		2 per 2k segment		
Configuration Interface (1 interface / 2k segment)		Serial 4 line		
Integration control		Asynchronous, with 6 digital signals		
Trigger delay			1	us
Integration & Readout		Interleaved		

Table 7: Optical characteristics for DR-2k-7, DR-4k-7, DR-6k-7, DR-8k-7

(1) Tint=10us, Unity gain (CDS_gain = 0 -> x1; Inverse ADC gain = 0x20h)

(2) T=27ºC , Tint=20us, Unity gain (CDS_gain = 0; -> x1 Inverse ADC gain = 0x20h)

(3) Measured in % deviation from full scale signal for the signal range of 5% - 95% (according to EMVA1288 proposal for linearity measurement)

(4) At unity gain (CDS_gain = 0 -> x1; Inverse ADC gain = 0x20h; end counter 128 (4096 ADC levels))

(5) Ramp offset and ramp gain must be adjusted for all segments to match with each other.

(6) T=27ºC , Tint=20us, Unity gain (CDS_gain = 1; -> x4 Inverse ADC gain = 0x20h)

* {info only: temporal noise can further be reduced by subtracting from each line the average value of the dark reference pixels, which will reduce temporal noise components coupled over the supply at frequencies below the line rate. :end info}
*** internal ADC resolution is 13bit.

3.7 Optical characteristics DR-2x2k-7, DR-2x4k-7, DR-2x8k-7

Parameter	Min	Typ/ Target	Max	unit
Pixel size		7 x 7		μm
Pixel pitch in x direction		7		μm
Number of dark pixels in most left segment		2x32		pixels
Fill Factor		100		%
Quantum efficiency at 630nm	50	60	70	%
Full Well capacity(4)	30	46	65	ke-
Total System Gain K		0.076		DN/e-
DSNU rms (1;5)		4	10	DN/12bit
Responsivity (1)		77		DN/nJ/cm2 (@12bit)
Responsvity analogue gain 4x (6)		310		DN/nJ/cm2 (@12bit)
PRNU rms (1;5)		0.7%	3%	% (full scale)
PRNU pp (1; 5)		4%	8%	% (full scale)
ADC Programmable gain	-6		20	dB
ADC gain resolution		8		bit
Blooming overload tolerance	100x	infinite		
Lag		0	0.01	%
Crosstalk (optical & electrical)		2	5	%
Exposure time range	2		infinite	us
Temporal noise Dark rms (2)*		1.5	4	DN/12bit
Dark noise electrons rms (2)*		22		e-
NEE (noise equivalent energy) unity gain (1)		0.02		nJ/cm2
Temporal noise Dark rms gain 4x (6)*		2.9	5	DN/12bit
Dark noise electrons rms gain 4x (6)*		7		e-
NEE (noise equivalent energy) analogue gain x4 (6)*		0.01		nJ/cm2
Non Linearity (3)		2	5	%
Dark current @ 27C		3	50	e-/ms
Maximum Line Rate 2:1 TDI mode			80	kScan/s
Maximum Line Rate dual line mode			160	kScan/s
ADC Resolution		12 (13)***		bit
Number of output taps		4 for each 2x2k pixels segment		
Configuration Interface 1 interface for each line and each 2k segment		Serial 4 line		
Integration control**		Asynchronous, with 6 digital signals		
Trigger delay			1	us
Integration & Readout		Interleaved		

Table 8: Optical Characteristics for DR-2x2k-7, DR-2x4k-7, DR2x8k-7

(1) Tint = 10us, Unity gain (CDS_gain = 0 -> x1; Inverse ADC gain = 0x20h)
(2) T = 27ºC , Tint = 20us, Unity gain (CDS_gain = 0; -> x1 Inverse ADC gain = 0x20h)
(3) Measured in % deviation from full scale signal for the signal range of 5% - 95% (according to EMVA1288 proposal for linearity measurement)
(4) At unity gain (CDS_gain = 0 -> x1; Inverse ADC gain = 0x20h; end counter 128 (4096 ADC levels))
(5) Ramp offset and ramp gain must be adjusted for all segments to match with each other.

(6) T=27ºC , Tint=20us, Unity gain (CDS_gain = 1; -> x4 Inverse ADC gain = 0x20h)

* {info only: temporal noise can further be reduced by subtracting from each line the average value of the dark reference pixels, which will reduce temporal noise components coupled over the supply at frequencies below the line rate. :end info}
** each line can be triggered individually.
*** internal ADC resolution is 13bit.

3.8 Optical characteristics DR-4k-3.5, DR-8k-3.5, DR-16k-3.5, DR-24K-3.5

Parameter	Min	Typ/ Target	Max	unit
Pixel Size (x,y)		3.5x3.5		μm2
Pixel Pitch in x direction		3.5		μm
Number of dark & special pixels in most left segment		64		pixels
Fill Factor		100		%
Quantum efficiency at 630nm	50	56	70	%
Full Well capacity(4)	15	23	35	ke-
DSNU rms (1;5)		4	10	DN/12bit
Responsivity (1)		39		DN/nJ/cm2 (@12bit)
Responsivity CDS gain 4x (6)		155		DN/nJ/cm2 (@12bit)
PRNU rms (1;5)		0.8	3	% (full scale)
PRNU pp (1; 5)		4	10	% (full scale)
ADC Programmable gain	-6		20	dB
ADC gain resolution		8		bit
Blooming overload tolerance	100x	infinite		
Lag		0	0.1	%
Crosstalk (optical & electrical)		2	5	%
Exposure time range	1		infinite	us
Temporal noise Dark rms (2)*		1.6	5	DN/12bit
NEE (noise equivalent energy) unity gain (1)		0.04		nJ/cm2
Temporal noise Dark rms gain 4x (6)*		3.4	6	DN/12bit
NEE (noise equivalent energy) analogue gain x4 (6)		0.02		nJ/cm2
Non Linearity (3)		2	5	%
Maximum Line Rate			80	kScan/s
ADC Resolution		12 (13)**		bit
Number of output taps		4per 4k pixel segment		
Configuration Interface (2 Interfaces for each 4k pixel segment		Serial 4 line		
Integration control		Asynchronous, with 4 digital signals		
Trigger delay			1	us
Integration & Readout		Interleaved		

Table 9: Optical characteristics DR-4k-3.5, DR-8k-3.5, DR-16k-3.5, DR-24K-3.5

(1) Tint=10us, Unity gain (CDS_gain = 0 -> x1; ADC ramp = 29)
(2) T=27ºC , Tint=20us, Unity gain (CDS_gain = 0; -> x1 ADC ramp = 29)
(3) Measured in % deviation from full scale signal for the signal range of 5% - 95% (according to EMVA1288 proposal for linearity measurement)
(4) At unity gain (CDS_gain = 0 -> x1; ADC ramp = 29; end counter 128 (4096 ADC levels))
(5) Ramp offset and ramp gain must be adjusted for all segments to match with each other Placement of pixels

(6) T=27ºC , Tint=20us, Unity gain (CDS_gain = 1; -> x4 ADC ramp = 29)

* {info only: temporal noise can further be reduced by subtracting from each line the average value of the dark reference pixels, which will reduce temporal noise components coupled over the supply at frequencies below the line rate. :end info}
**internal ADC resolution is 13bit.

3.9 Quantum efficiency all B&W versions
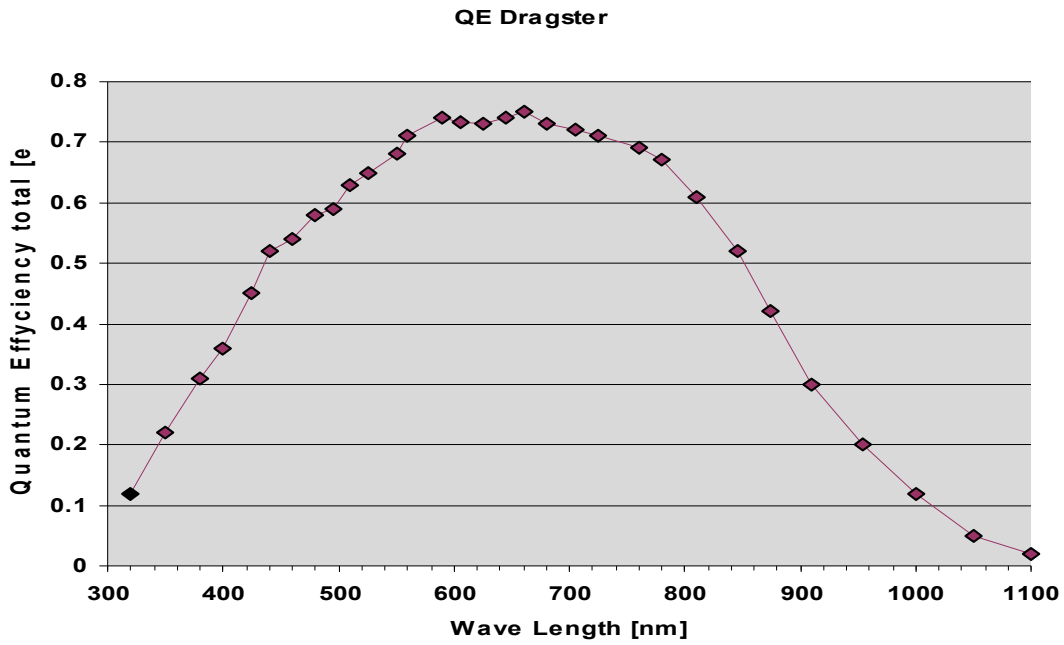
QE Dragster

Fig 2: Quantum efficiency measured according EMVA1288 [detected e-/photon]

3.9.1 Filter transmission for RGB Bayer pattern sensor versions
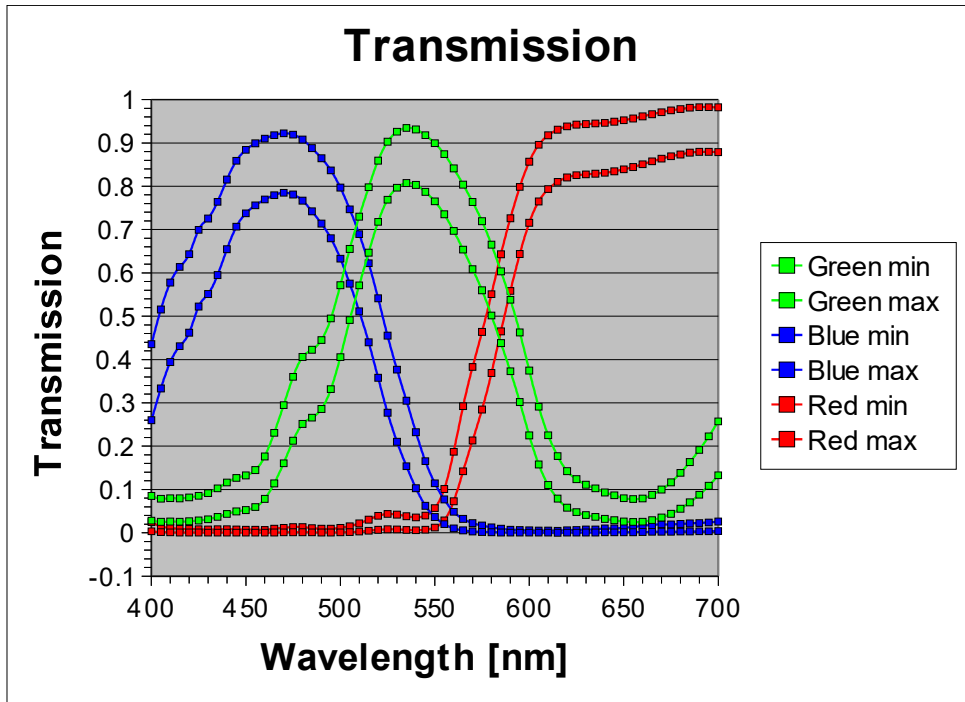
Fig 3: Spectral transmission of colour filters

3.9.2 Color filter arrangement for RGB Dragster versions

On the dual line Dragsters there's the possibility to have RGB filters that are organized in both lines as shown in the next figure.
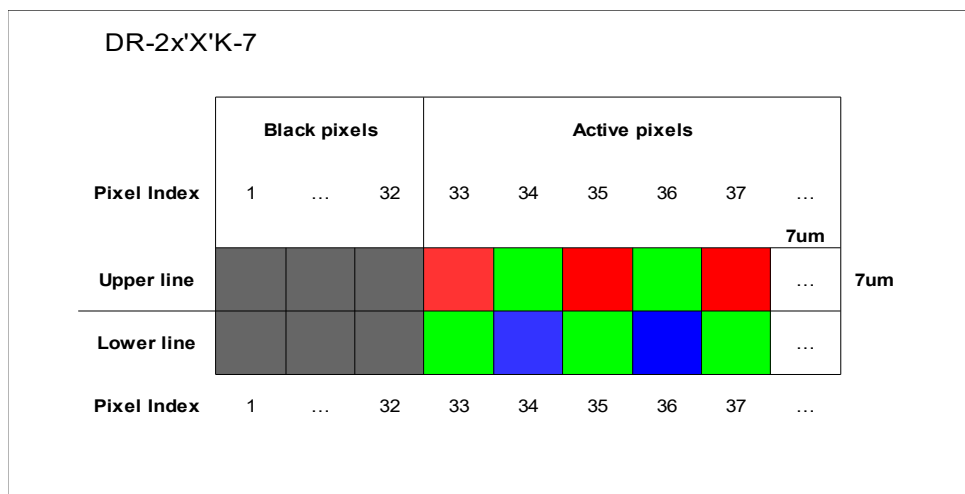
Fig 4: Color filter arrangement on Dragster dual line sensors

3.10 Placement of pixels DR-Xk-7
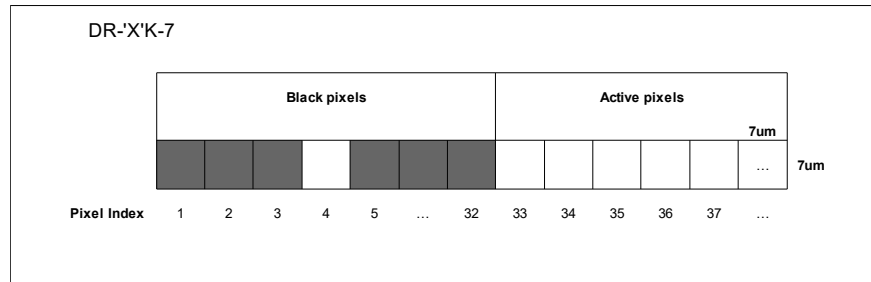
Fig 5: Placement of pixels sensors with 7um pixel pitch

3.10.1 Test & special pixels DR-Xk-7

The first 32 pixels include not only dark pixels but also special pixels like described:

1. The output from the first pixel is directly connected to the pad 1.*

2. The output from the second pixel is directly connected to the pad 2.*

3. The third pixel is a black pixel, electrically fixed to ADC low saturation

4. The fourth pixels is a white pixel, electrically fixed to ADC high saturation

5. The pixels 5 - 24 are normal pixels however the photo diode is covered by a metal light shield. They serve as a dark reference. However at longer wavelengths the metal shield will not completely shield light any more.

6. The pixels 25 -32 are electrical black pixels. In these pixels the photo diode is disconnected electrically from the readout chain. These pixels will follow all analogue and digital offset variations, however not integrate dark current or any photo current. They can be used check the validity of the dark pixels 5 - 24, or to compensate for line by line ADC offset variations.

These pixels are light sensitive. The respective outputs are connected to a test point on the head board for debugging purpose in certain package variations.

3.11 Placement of pixels DR-Xk-3.5
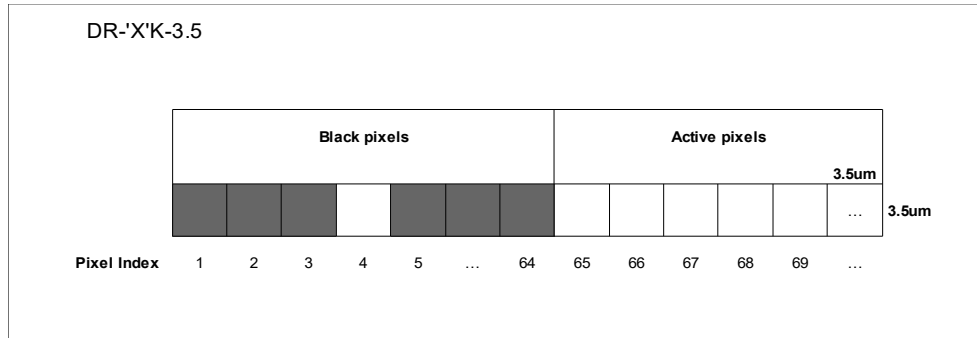
Fig 6: Placement of pixels sensor variations with 3.5μm pixel pitch

3.11.1 Test & special pixels DR-Xk-3.5

The first 64 pixels include not only dark pixels but also special pixels like described:

1. The output from the first & second pixels are directly connected to the pad 1 of the most left segments on top and bottom.*

2. The output from the third and fourth pixels are directly connected to the pad 2of the most left segments on top and bottom.*

3. The fifth and sixth pixels are a black pixel, electrically fixed to ADC low saturation

4. The seventh and eight pixels are white pixel, electrically fixed to ADC high saturation

5. The pixels 9 - 48 are normal pixels however the photo diode is covered by a metal light shield. They serve as a dark reference. However at longer wavelengths the metal shield will not completely shield light any more.

6. The pixels 49 - 64 are electrical black pixels. In these pixels the photo diode is disconnected electrically from the readout chain. These pixels will follow all analogue and digital offset variations, however not integrate dark current or any photo current. They can be used check the validity of the dark pixels 9 - 48, or to compensate for line by line ADC offset variations.

* These pixels are light sensitive. The respective outputs are connected to a test point on the head board for debugging purpose in certain package variations.

4 Functional Description

4.1 General sensor description

Sensors with 3.5μm pixels are structurally identical to sensors with 7μm pixel. However for the sensor with 3.5μm two independent readout blocks are placed, one on tho of the sensor line, which reads out odd pixels and one at the bottom of the sensor line which reads out even pixels. Thus for sensors with 3.5μm pixels two independent segments are alway's placed together to form a segment with double resolution compared to the segment with 7μm pixel. Thus for sensors with 3.5μm pixel all pixel numbers indicated further in this section are double compared to the 7μm sensor variations.

The sensor is built of a line of 2080 pixels. The first 32 pixels counting from the left are designated as Black pixels, and are used to have a reference for dark current and signal offsets, the remaining 2048 are the normal pixels, responsible for the image. For readout each 2k segment is completely independent. This can be exploited to align the readout of th lght sensitive pixels from each segment. To do so, the readout is started in the most left segment 16 Pixel clock cycles earlier than the more right segments. The individual start of readout for different segments can also be exploited to reduce the required signal bandwidth by sequentially addressing the SRAM blocks of different 2k segments and multiplexing the data lines.

The analogue voltage references, especially the references to define the ADC start voltage and the ADC gain are interconnected along the sensor line, however remain individual for odd an even pixels in the case of 3.5μm pixels. However each segment comprises an individual SPI block to configure these voltages. Normally it is recommended to program the registers controlling an interconnected voltage with the same settings. See figure 7 and 8 to illustrate how analogue voltages are interconnected over multiple segments and controlled over the respective SPI interfaces for sensors with 7μm and 3.5μm pixel pitch respectively.
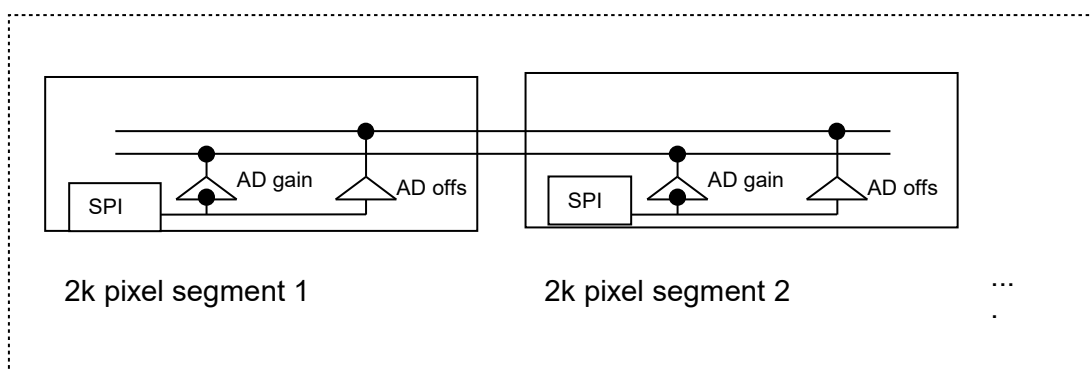
Fig 7: Interconnection of ADC reference voltages in case of 7μm pixel pitch sensors with multiple segments
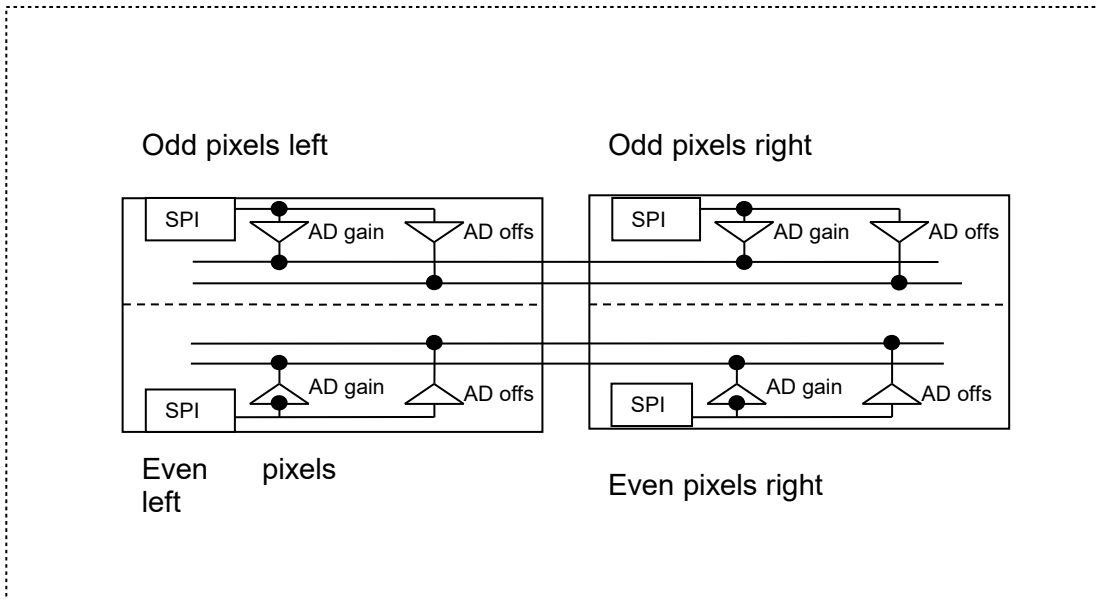
Fig 8: Interconnection of ADC reference voltages in case of 3.5µm pixel pitch sensors with multiple segments

The sensor features a 13 bit ramp ADC with programmable conversion gain and end range stage. The on chip digital control circuit generates all necessary control for conversion and the readout modes. However the readout of a new line can be triggered over an external signal if required. The ADC conversion range (maximum number of bit's can be programmed over the serial interface. Higher conversion range requires longer ADC conversion time.

The sensor enables interleaved integration, A/D conversion and readout, therefor the overall pipeline delay is 2 minimum line times.
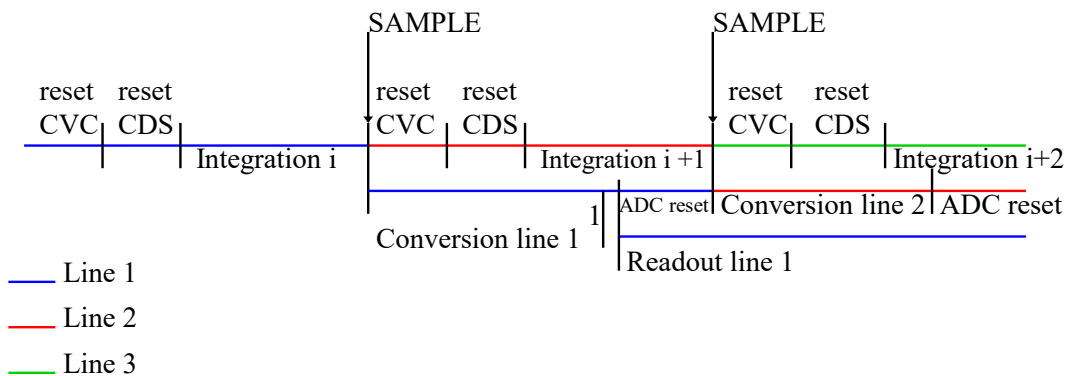
1 - Transfer from Shadow to Readout Register

Fig 9: Overview of pipelined integration ADC and readout sequence

4.2 Serial 4 wire configuration interface

For access to the internal registers of the sensor, a serial interface with 4 wires is implemented. The interface consists in 4 different lines, one clock line (SCLK), one receive (MOSI) and transmit (MISO) line which are synchronous to each other. The fourth line is the chip select (/CS) and must be low to send/receive data trough the lines. The sensor will be always slave in the application. By the use of the /CS signal the master can activate the serial interface of an individual segment or several segments together. The bus frequency range is from DC to 20MHz, but must always be lower then MCLK/2.

The data is sent from LSB to MSB. The command word has a length of 16 bits and contains the data of the register and the register address. It is possible to write multiple registers consecutively, sending data and address each 16 SCLK. After the last write word the SCLK should be sent for minimum 2 extra clocks, (maximum 4 SCLK) while /CS is still low.

The updating to the registers is performed after update request bit is sent at the next rising edge of "RESET_COUNTER" signal. The last word sent to the registers has to be always to register 0x01 and containing the update request bit, otherwise not update is performed.

4.2.1 Writing Operation

The writing operation is performed by sending the word containing the data and the address, no acknowledge signal or indication is given back.

Time 0   Time 16SCLK

LSB .... *MSB*	
<-------------------------------------- 16 bit of serial data ------------------------------------->	
<------------------- Data ------------------->	<-------------- Address ----------------------->
D0 | D1 |..................... .... D6 | D7	A0 | A1 | .... A6 | A7

3 extra clocks before
rising edge of n_CS
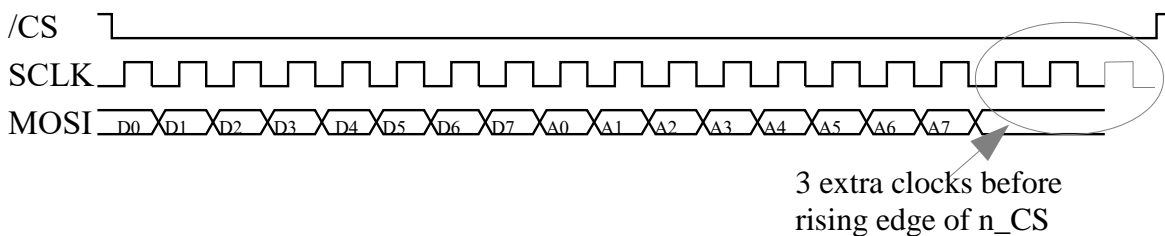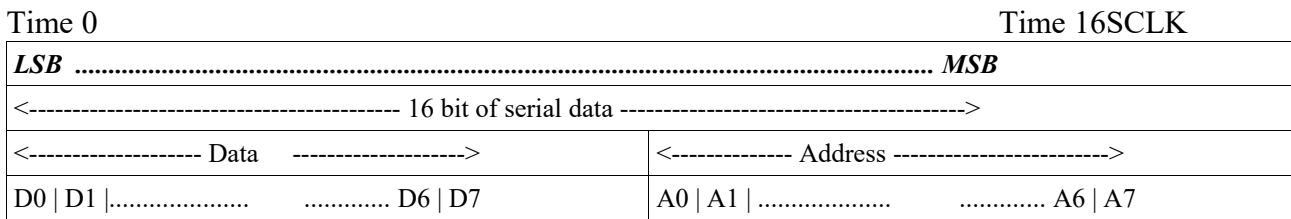
Fig 10: Writing operation

4.2.2 Reading Operation

To perform a read operation, the address for the register to be read, has to be written on register 15 (as data). The output data will be sent over the MISO line, with one leading one, and with 2 SCLK delay to the last bit of the address word (LSB first).

Time 0   Time 16SCLK

LSB ....*MSB*
<------------------------------------ 16 bit of serial data ------------------------------------>

<-------- Data (read address) ------------------>	<------------- Address R15 ------------------->
D0 | D1 |.. D6 | D7	A0 | A1 | .... A6 | A7
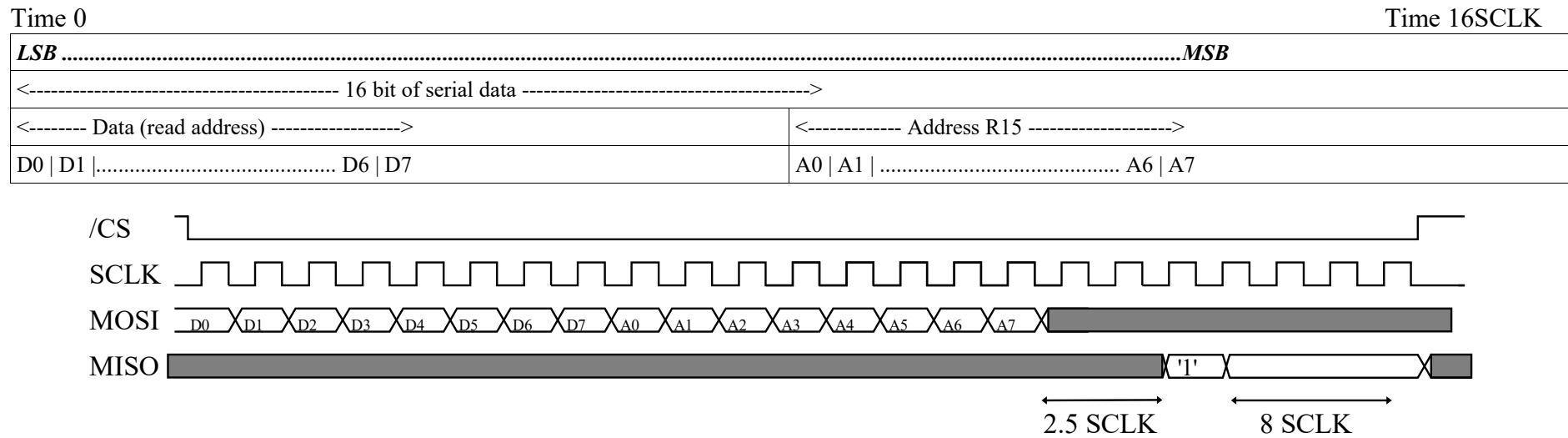
Fig 11: Reading operation

4.3 Timing diagrams

Start of integration
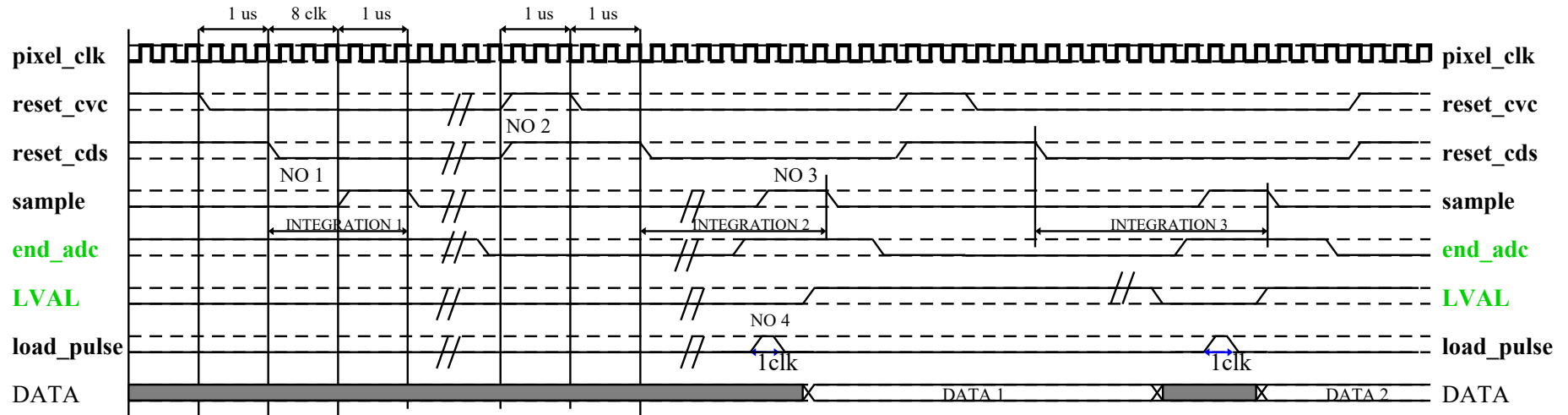
Fig 12: Timing diagram

NO 1 - To start the integration the user should send the falling edge of RST_CVC and with a delay of 1us the falling edge of RST_CDS, only after at least 8clk the user can send the raising edge of SAMPLE. However the rising edge of SAMPLE should never be sent before the end of the active ADC conversion. (END_ADC = HIGH) and SAMPLE should be high for at least 1us.

NO 2 - The user can send the rising edge of RST_CVC and RST_CDS earliest 7clk after falling edge of sample. (Note 6clk after falling edge of sample, END_ADC will have it's falling edge)

NO 3 - The raising edge of SAMPLE should only be sent if END_ADC is HIGH

NO 4 - The load pulse should be sent, with at least 4 clocks delayed to the latest event of falling edge of LVAL or rising edge of END_ADC.

End of readout entering idle
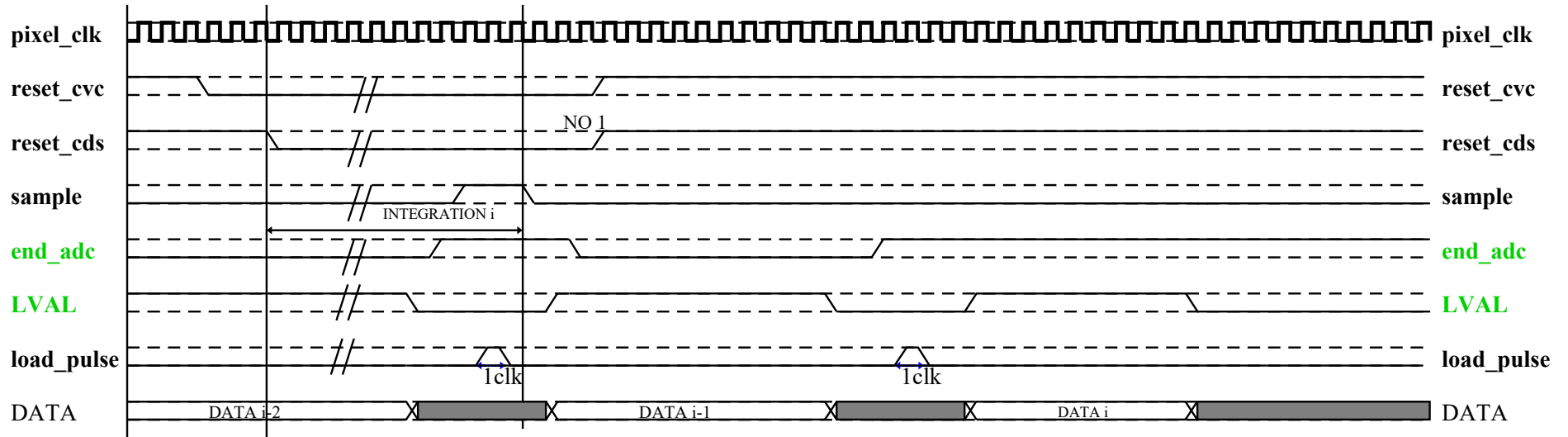
Fig 13: Timing diagram

NO 1 - To put the sensor in idle mode, the user should send the rising edge of RST_CVC and RST CDS, and keep the signal at HIGH Level

Detail end of integration start ADC and readout
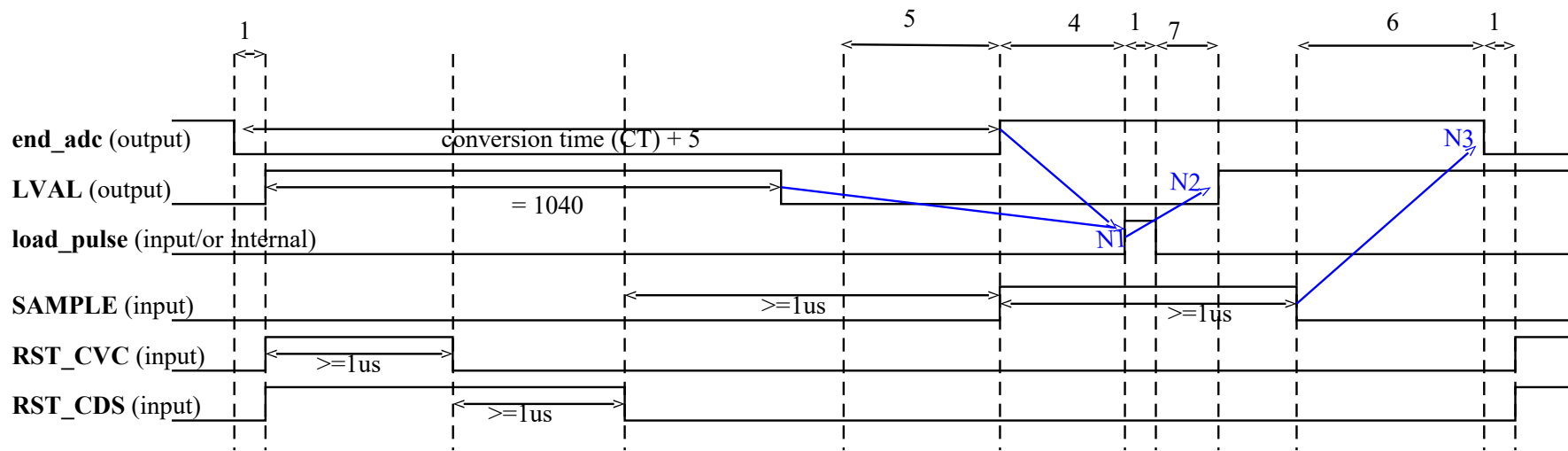
NOTE 1: rising of load = the later of (rising edge end_adc; falling edge LVAL) + 4
NOTE 2: rising of LVAL = rising edge of load_pulse + 8
NOTE 3: falling of end_adc = falling edge of $\overline{\text{SAMPLE}}$ + 6

<u>Conversion time:</u>

if ADC_mode_bit =0)
    CT = end_range*32
else (ADC_mode_bit = 1)
    CT = [thr1+ (thr2-thr1)/2 + (thr3-thr2)/4 + (end_range -thr3)/8]*32

Fig 14: Detail end of integration start ADC and readout

5 Tap organization

5.1.1 Tap organization DR-2k-7, DR-4k-7, DR-8k-7
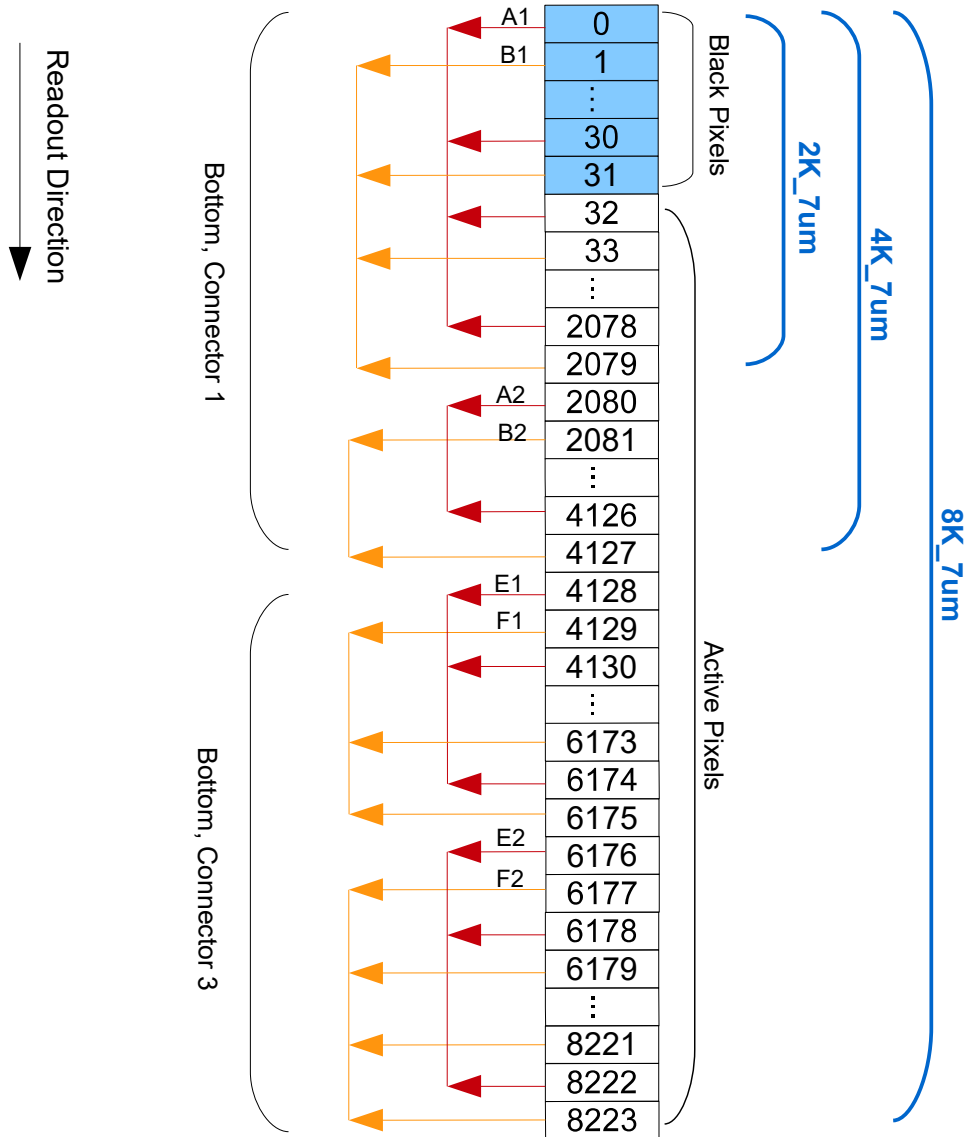
Fig 15: Tap organization DR-2k-7, DR-4k-7, DR-8k-7

5.1.2 Tap organization DR-6k-7
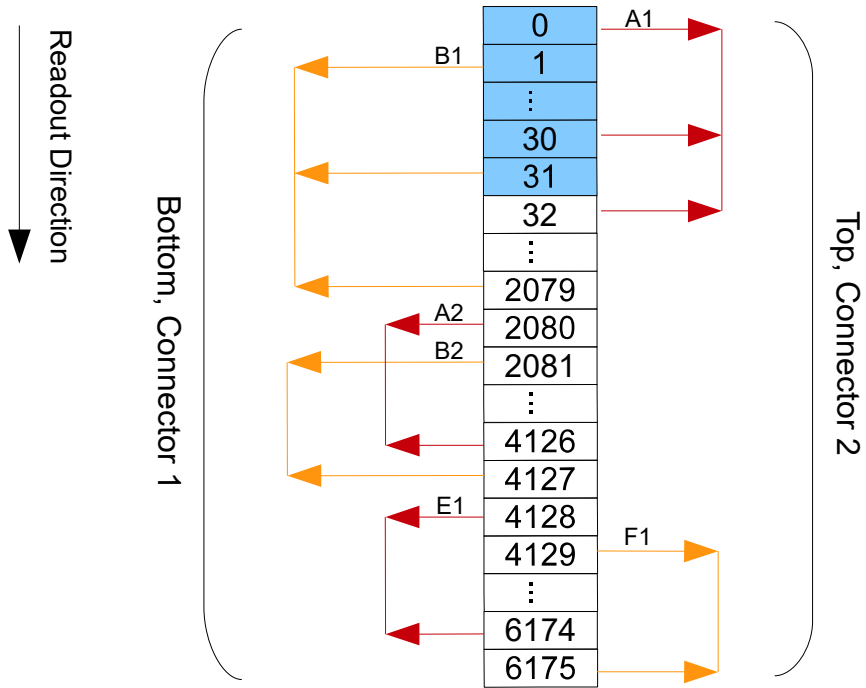
Fig 16: Tap organization DR-6k-7

5.1.3 Tap organization DR-4k-3.5, DR-8k-3.5, DR-16k-3.5
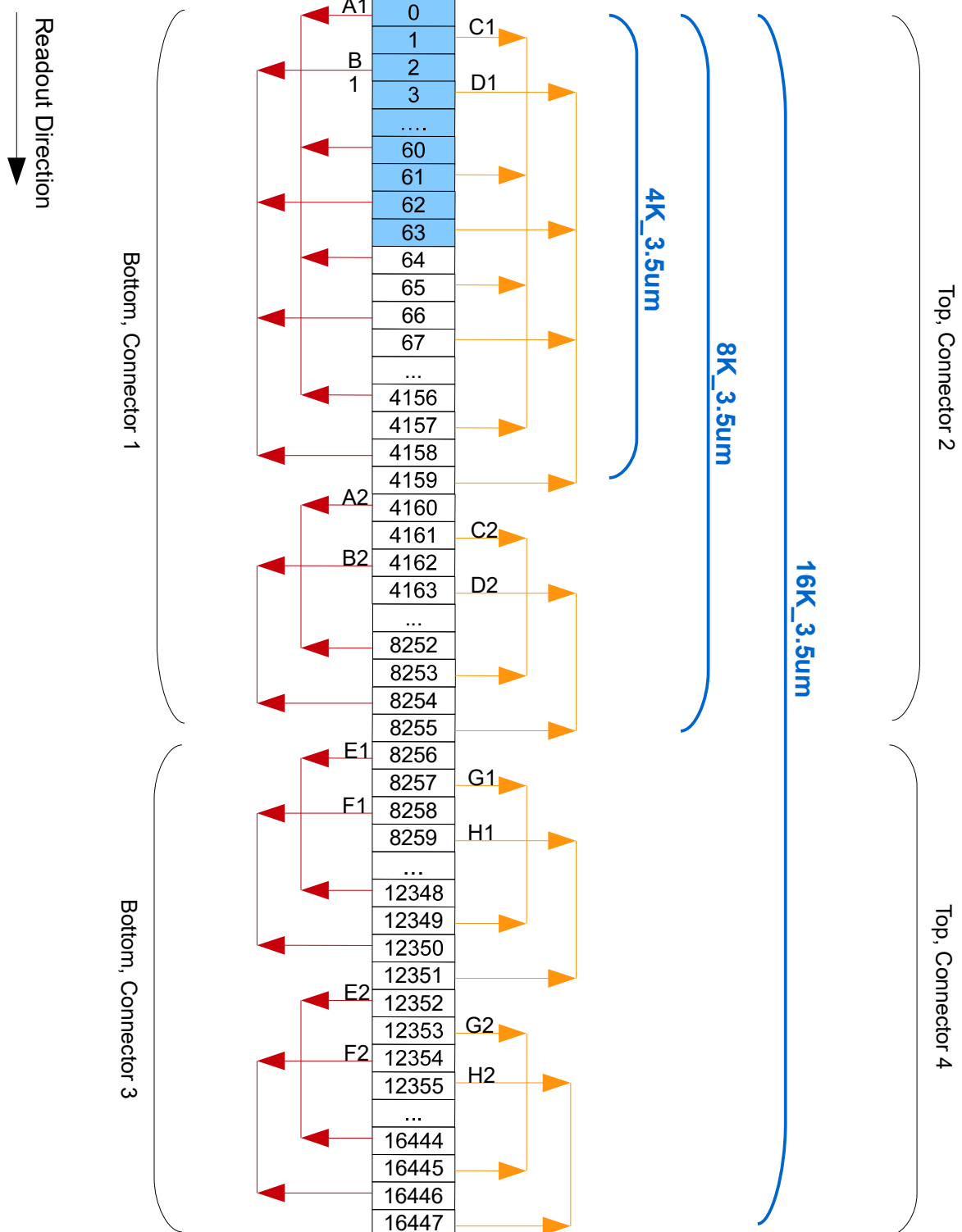
Fig 17: Tap organization DR-4k-3.5, DR-8k-3.5, DR-16k-3.5

5.1.4 Tap organization DR-2x2k-7, DR-2x4k-7, DR-2x8k-7
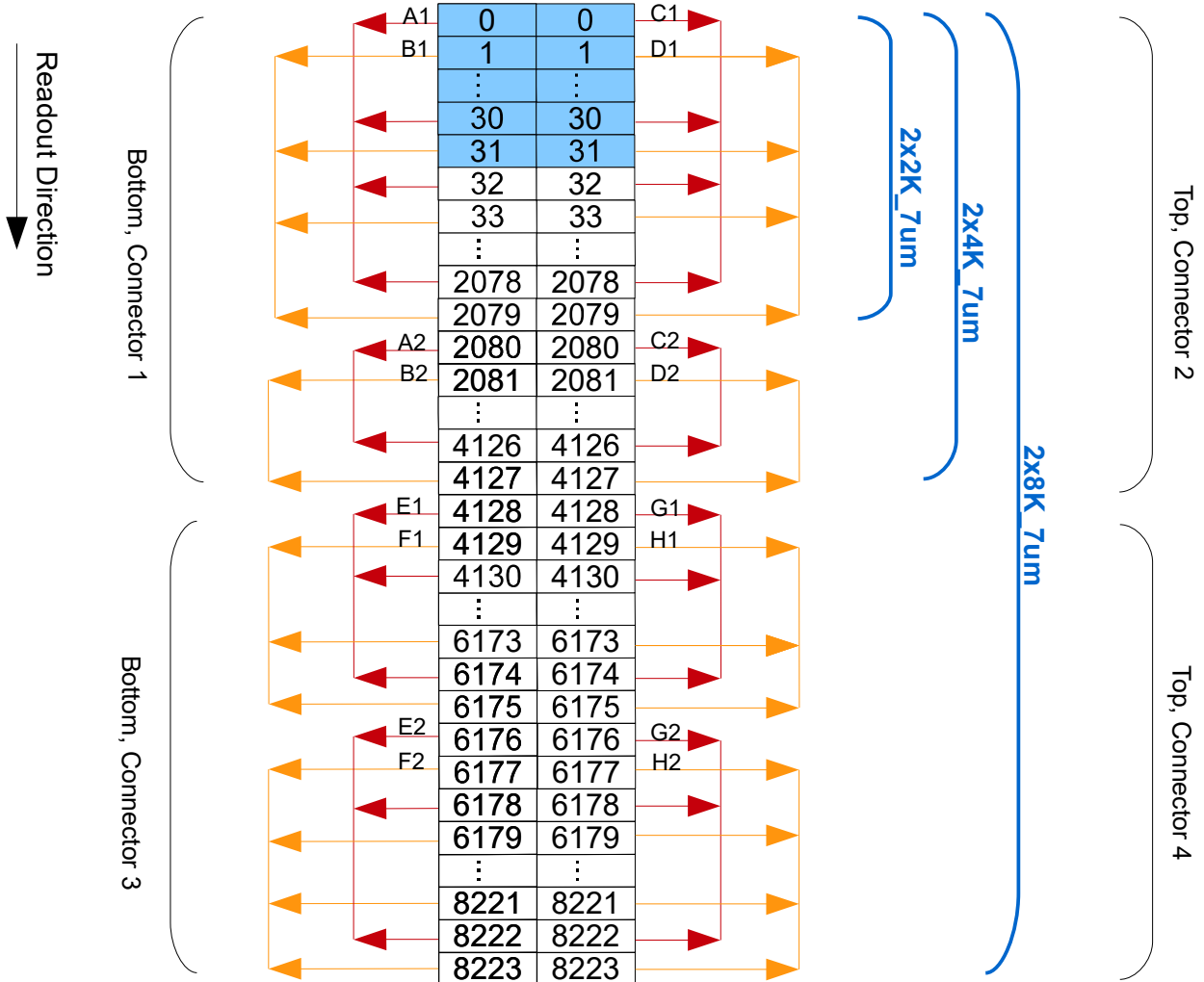
Fig 18: Tap organization DR-2x2k-7, DR-2x4k-7, DR-2x8k-7

5.1.5 Tap organization DR-2x2k-7-RGB, DR-2x4k-7-RGB, DR-2x8k-7-RGB
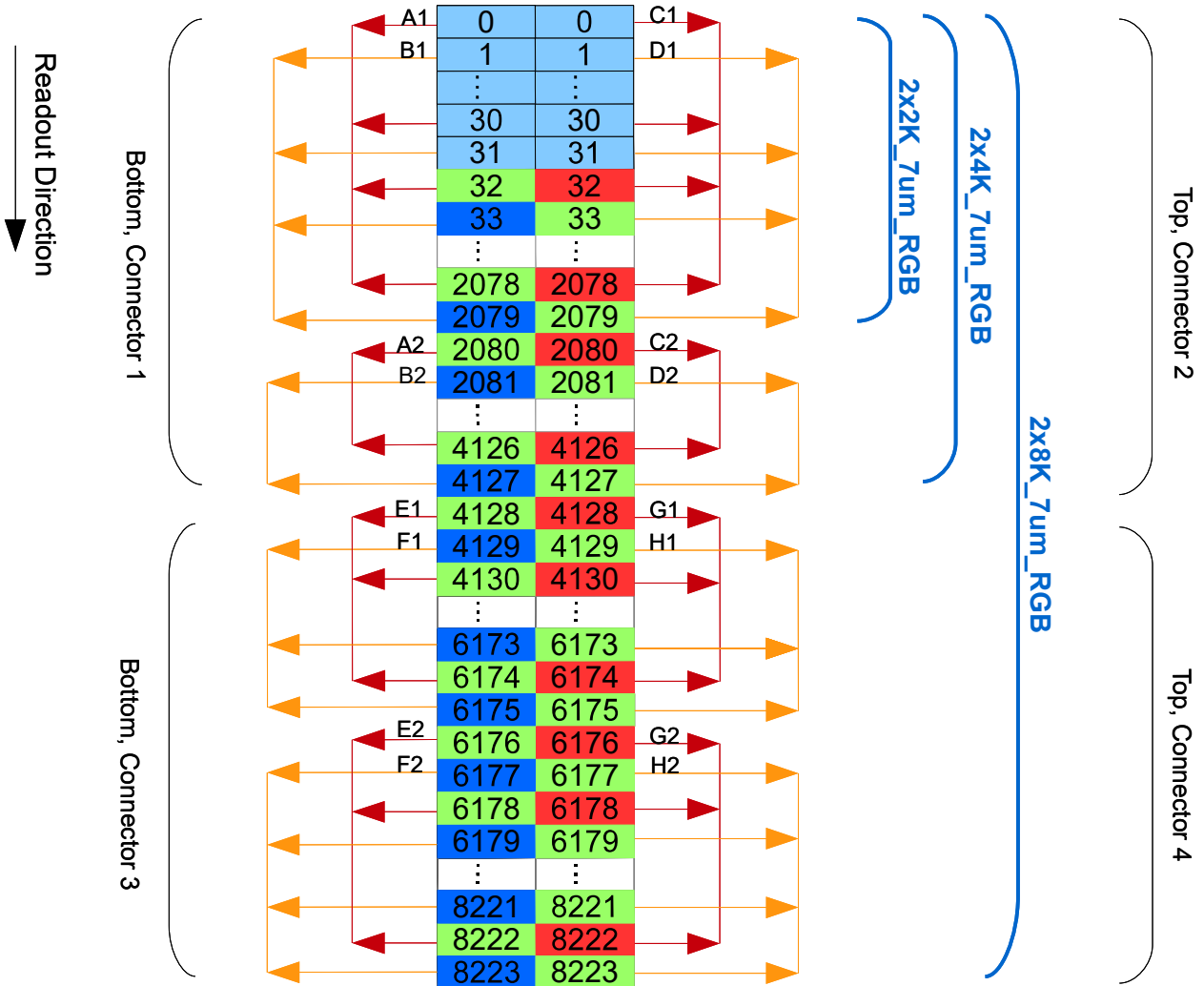
Fig 19: Tag organization DR-2x2k-7-RGB, DR-2x4k-7-RGB, DR-2x8k-7-RGB

5.1.6 Tap organization DR-24k-3.5
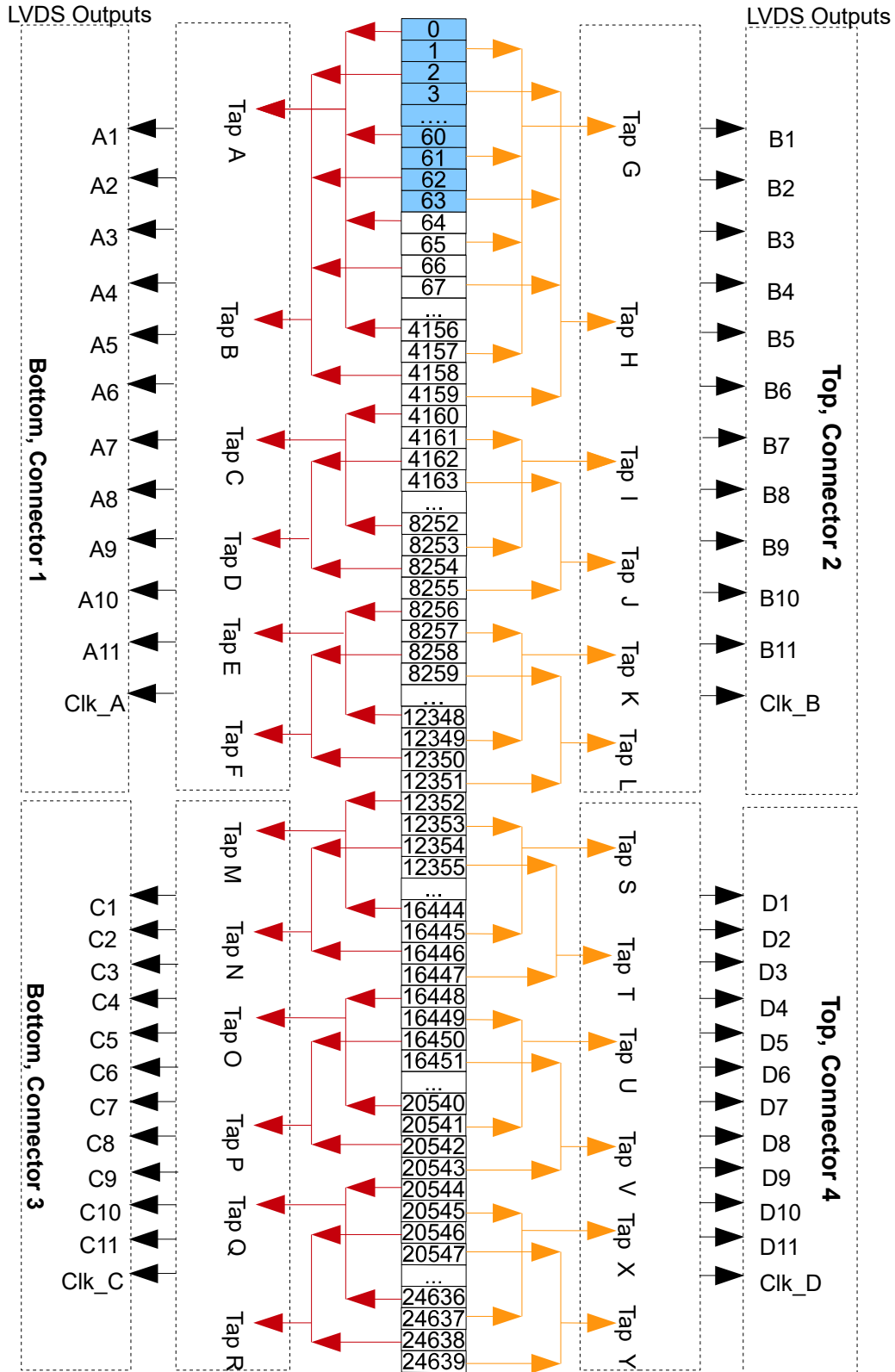
Fig 20: Tap organization DR-24k-3.5
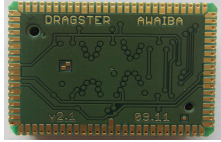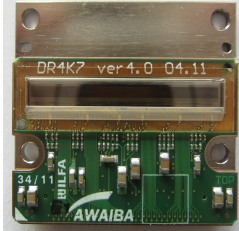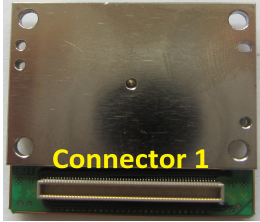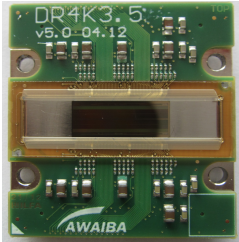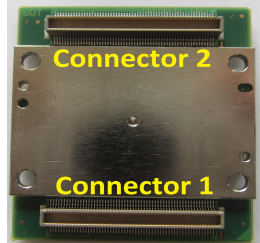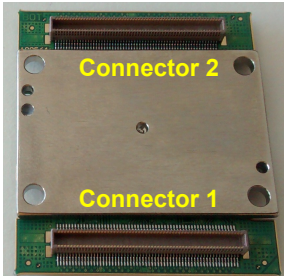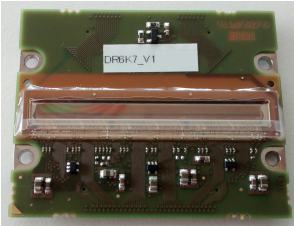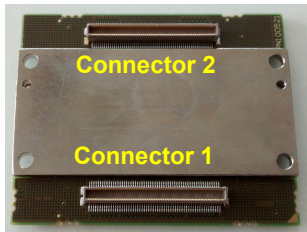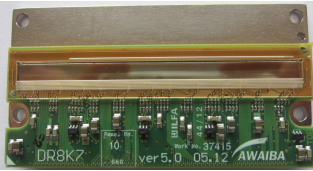
6 Packages overview

DRAGSTER sensors are supplied with specific packages developed at Awaiba that are made to bring serious advantages to camera developers. They include years of close development with Awaiba's customers in the most demanding applications.

The available packages are organized in two main types: LCC and INVAR. The LCC is a no lead package where the silicon's carrier is FR4 while the INVAR package uses a special nickel iron alloy as heat dissipation and mechanical reference. While the LCC package is oriented for size, resolution and cost conscious applications the INVAR type is focused on high performance, where highest speed and high resolutions are the main advantages to the field application. All package types take a cover glass over sensor's silicon to protect from external dust particles. Optionally, the sensor can be delivered without cover glass and a globe top protection of bond wires.

For the customer, one of the most obvious advantage of Dragster packages are the use of commercially available connectors or low cost LCC connections. This makes each camera development fast and easy and brings also other advantages: precise mechanical alignment to the optics by taking INVAR as reference and it's CNC machined features, integrated heat dissipation plate that minimizes sensor stress in Z-axis, maximization of sensor performance in speed and noise and easily customizable package to suit any requirement. Furthermost the LCC can also be mounted as a SMD part.

Other packages are possible, like bare die or CSP, so contact AWAIBA if you require a custom package.

Package	Sensors	Top View	Bottom View
LCC	DR-2K-7 DR-2x2K-7 DR-4K-3.5		
Invar with 1 connector	DR-4K-7		
Invar with 2 connectors	DR-2K-7 DR-2x2K-7 DR-4K-3.5		
	DR-2x4K-7 DR-8K-3.5		
	DR-6K-7		
Invar with 2 connectors in the bottom	DR-8K-7		
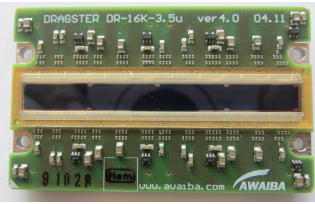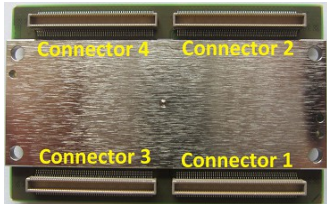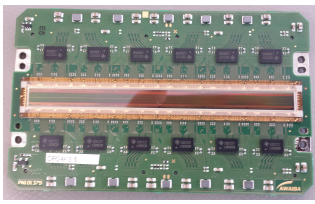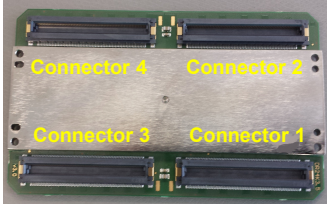
Invar with 4 connectors	DR-2x8K-7 DR-16K-3.5		
	DR-24K-3.5		

Table 10: Package overview

7 Mechanical Drawings

7.1 LCC Package drawings DR2k-7

center point of optical axis
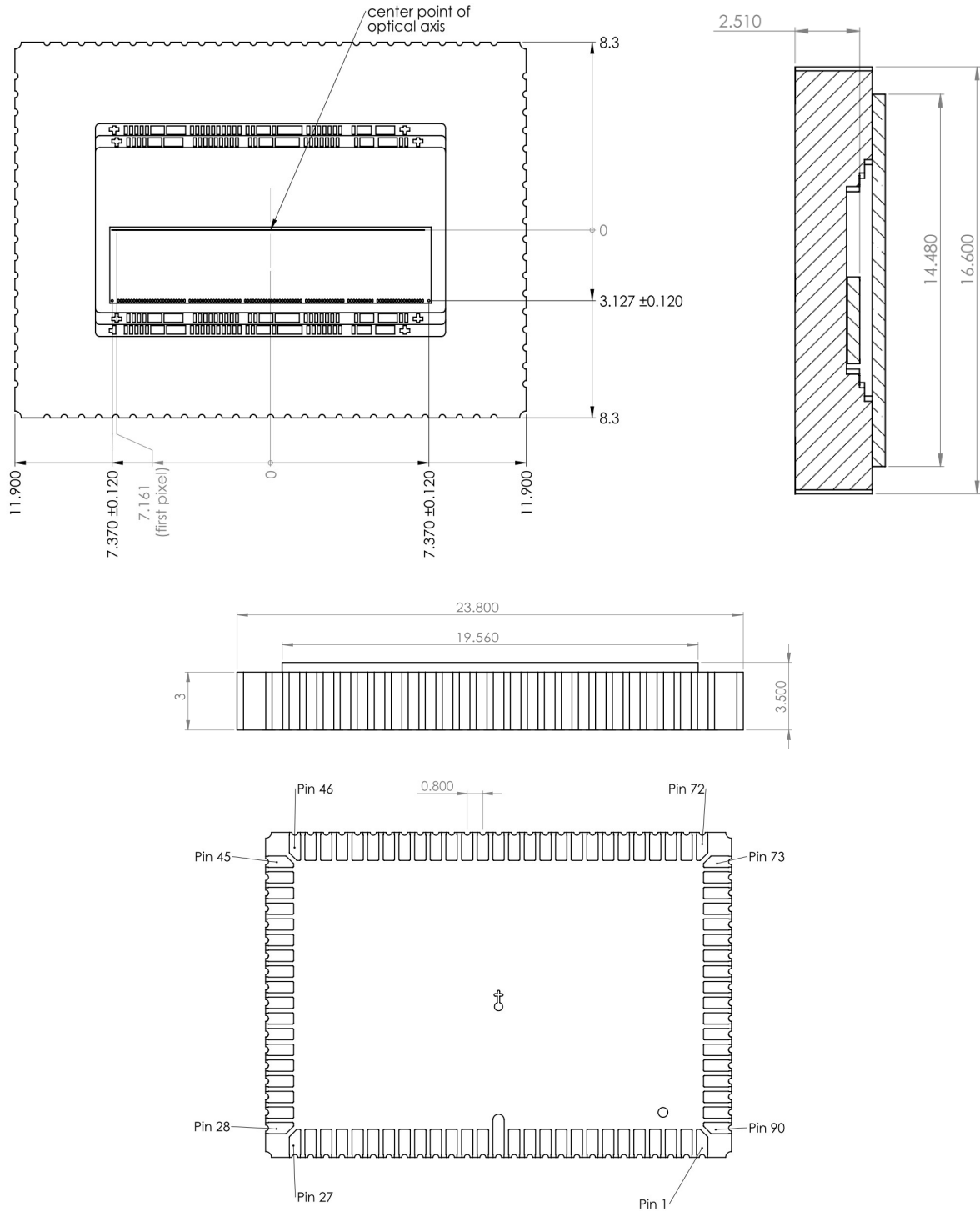
Fig 21: Four Views of LCC Package Drawings for DR2k-7

7.2 LCC package drawings DR2x2k-7, DR4k-3.5
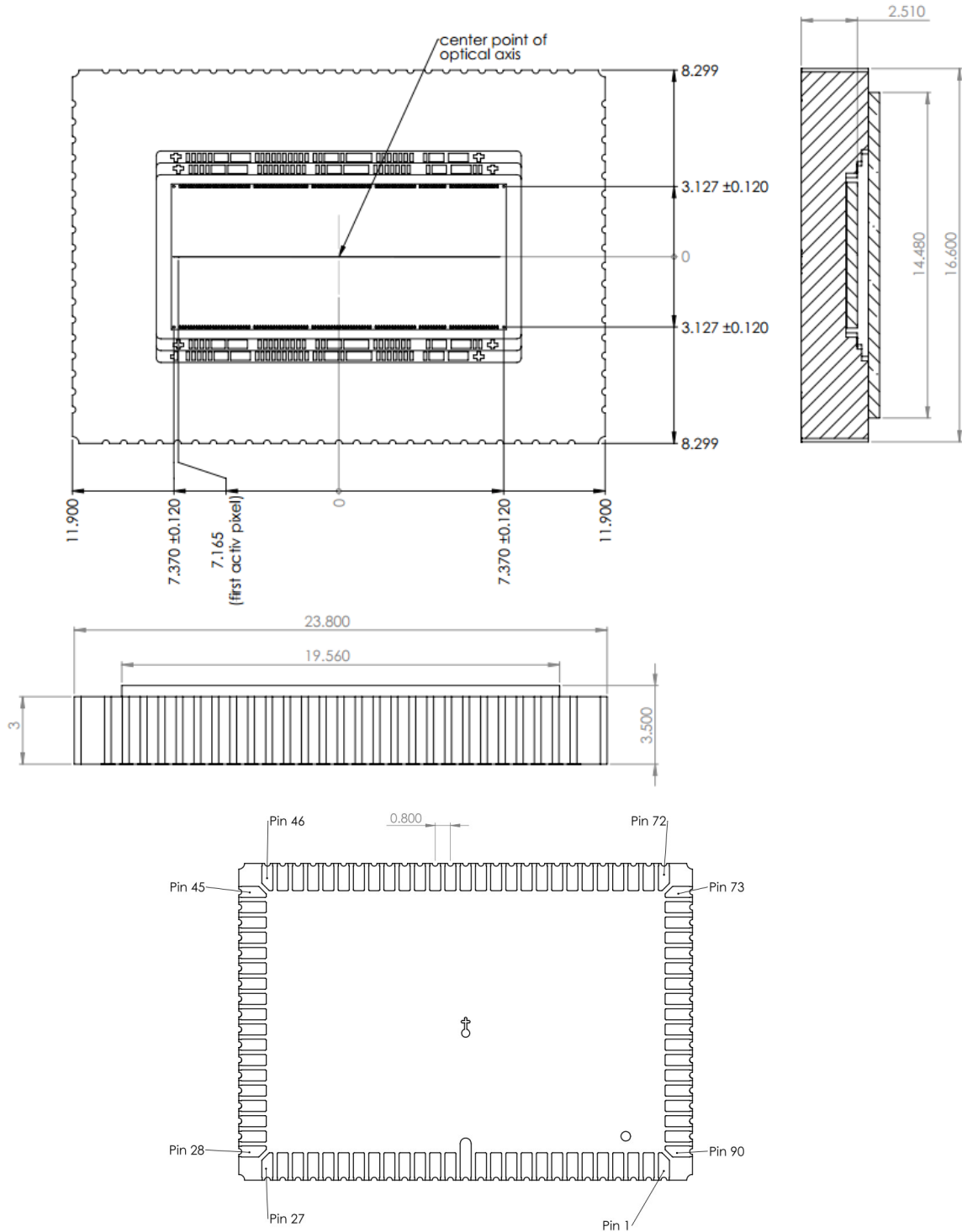
Fig 22: Four Views of LCC Package Drawings for DR2x2k-7 B&W and RGB, DR4k-3.5

7.3 Invar package drawing DR4k-7
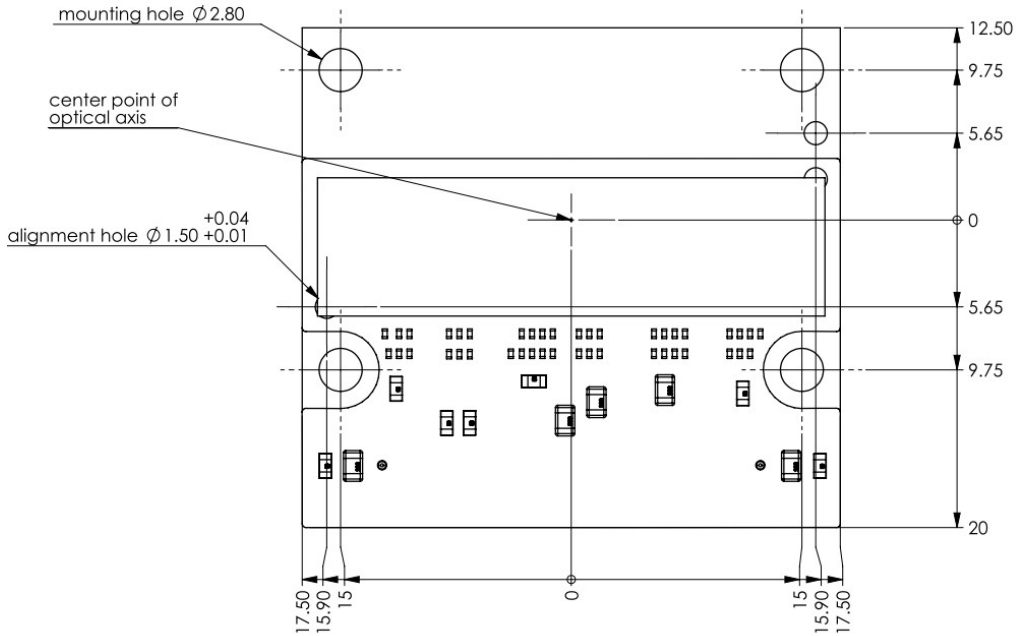
Fig 23: Top view DR-B&W-4k-7-Invar. If not otherwise noted all tolerances are +/- 0.1mm
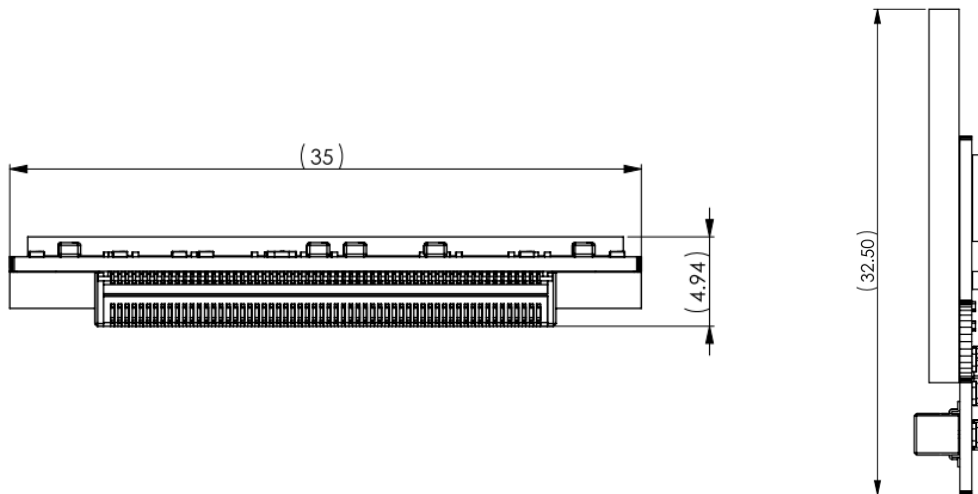
Fig 24: DR-B&W-4k-7-Invar. Tolerance +/- 0.1mm

7.4 Invar package drawing DR-2x4k-7, DR8k-3.5
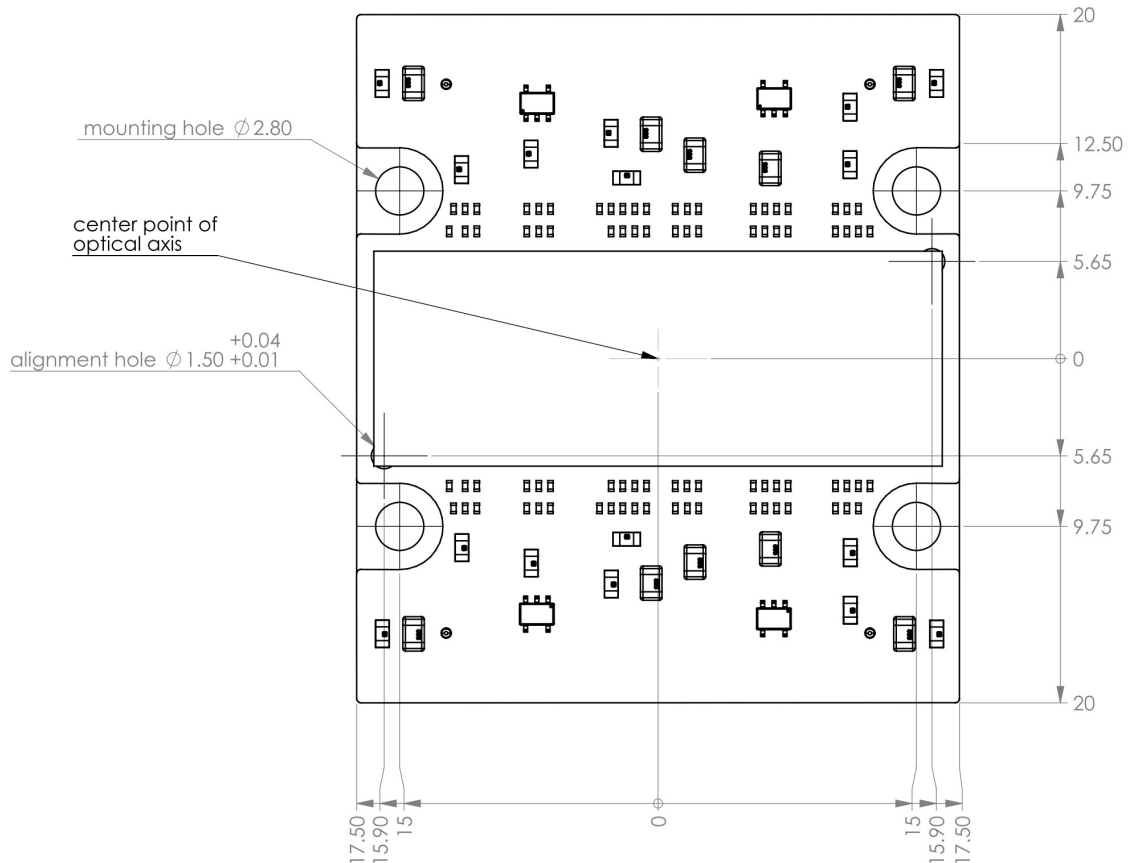
Fig 25: Top view DR-B&W-2x4k-7-Invar and DR-B&W-8K-3.5-Invar. If not otherwise noted all tolerances are +/- 0.1mm
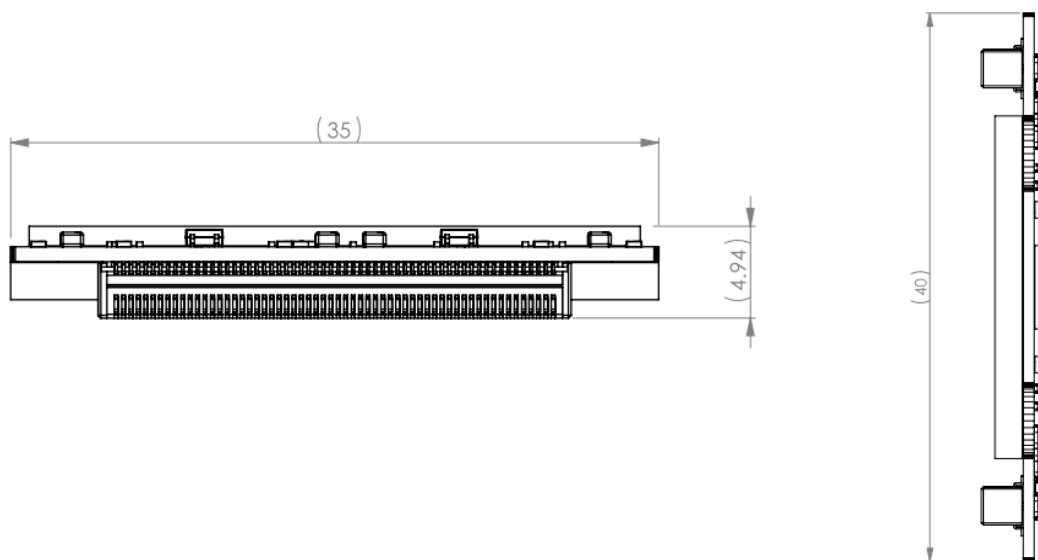
Fig 26: DR-B&W-2x4k-7-Invar, DR-B&W-8K-3.5-Invar. Tolerance +/- 0.1mm

7.5 Invar package drawing DR-2k-7, DR-2x2k-7, DR-4k-3.5
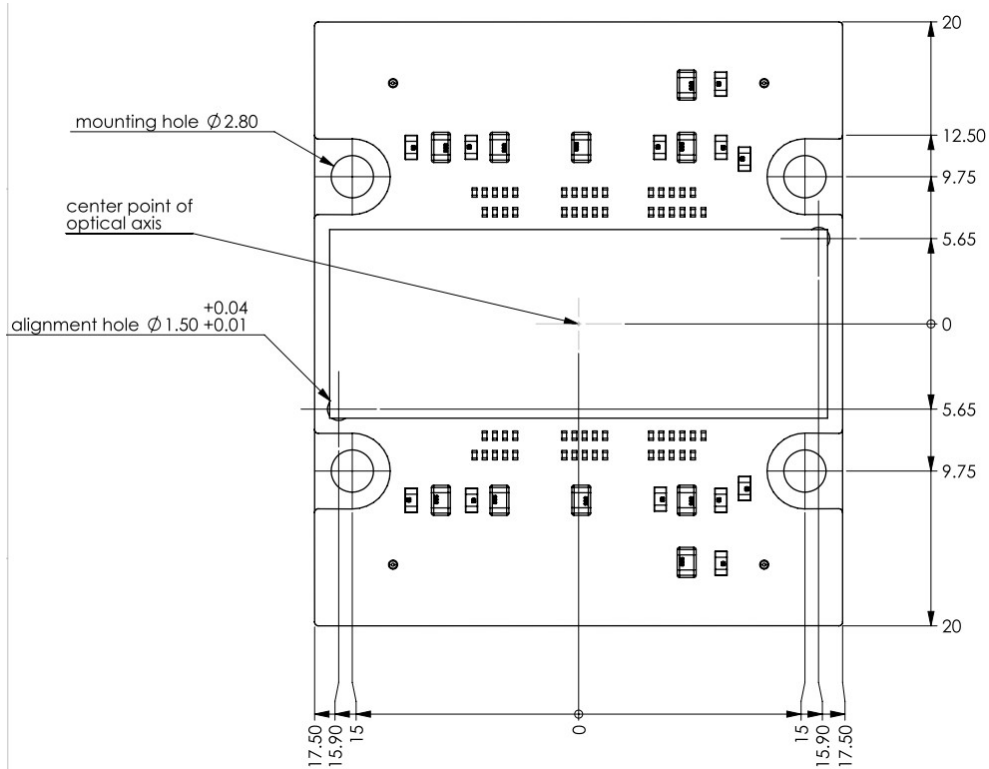
Fig 27: Top view DR-B&W-2k-7-Invar, DR-B&W-2x2k-7-Invar, DR-B&W-4k-3.5-Invar. If not otherwise noted all tolerances are +/- 0.1mm
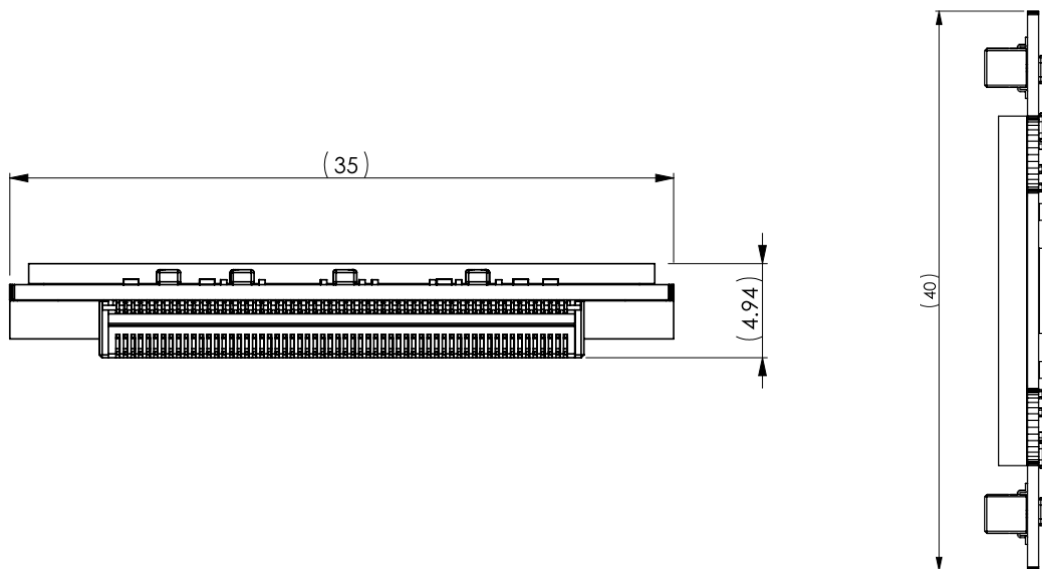
Fig 28: DR-B&W-2k-7-Invar, DR-B&W-2x2k-7-Invar, DR-B&W-4k-3.5-Invar.. Tolerance +/- 0.1mm

7.6 Invar package drawing DR6k-7
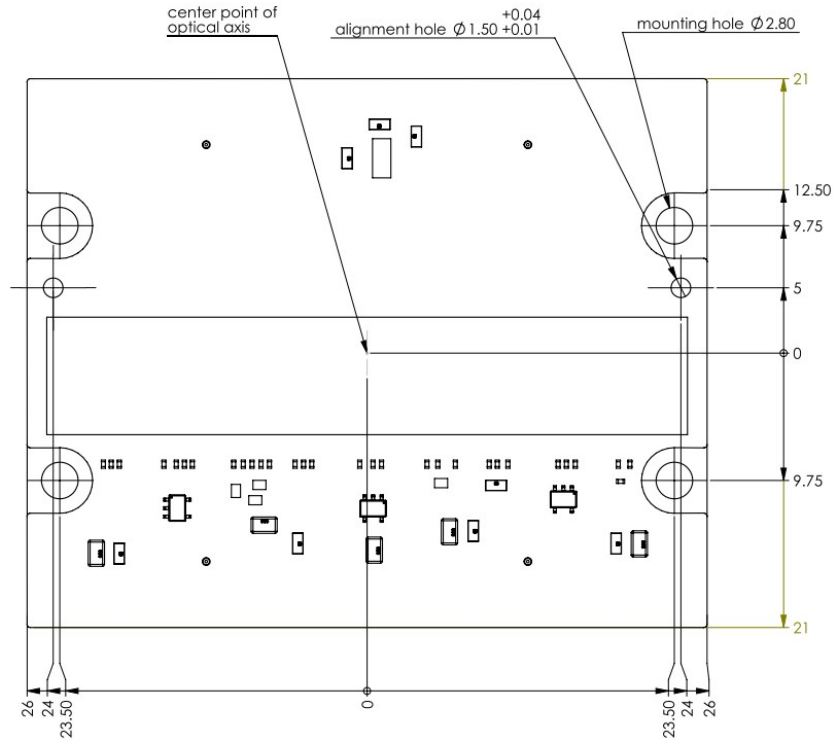
Fig 29: Top view DR-B&W-6k-7-Invar. If not otherwise noted all tolerances are +/- 0.1mm
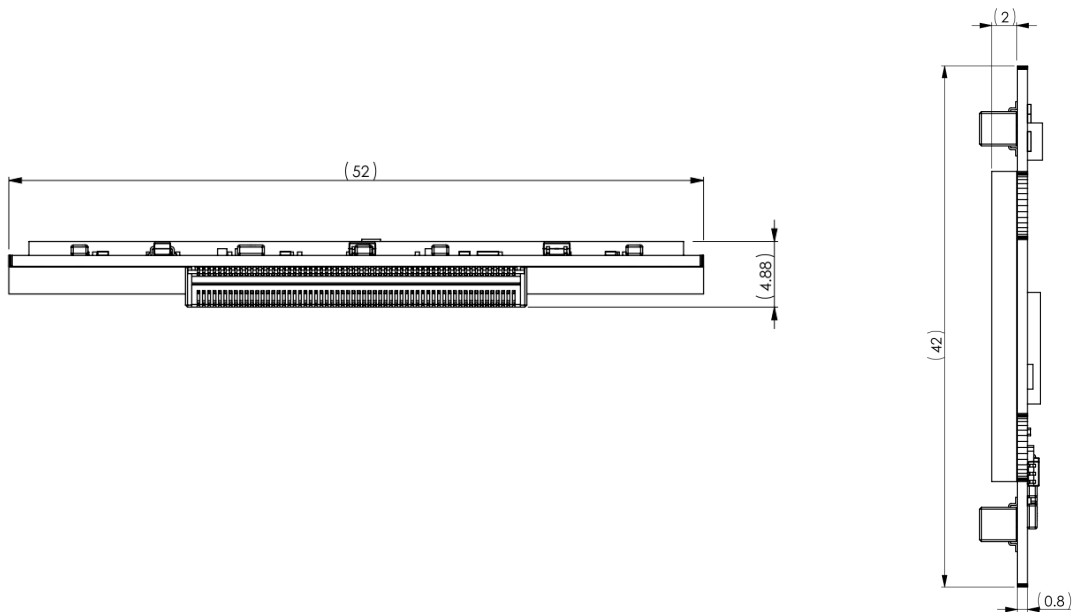
Fig 30: DR-B&W-6k-7-Invar. Tolerance +/- 0.1mm

7.7 Invar package drawing DR8k-7
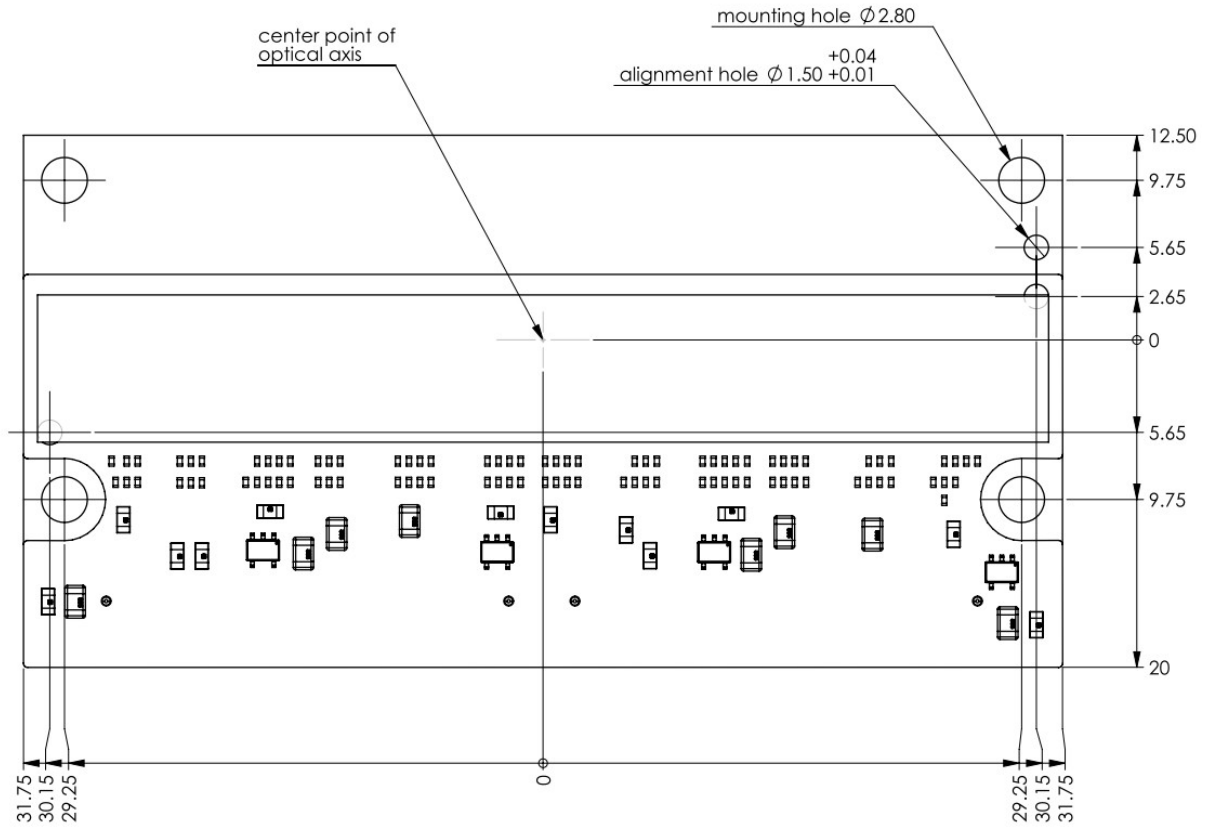
Fig 31: Top view DR-B&W-8k-7-Invar. If not otherwise noted all tolerances are +/- 0.1mm
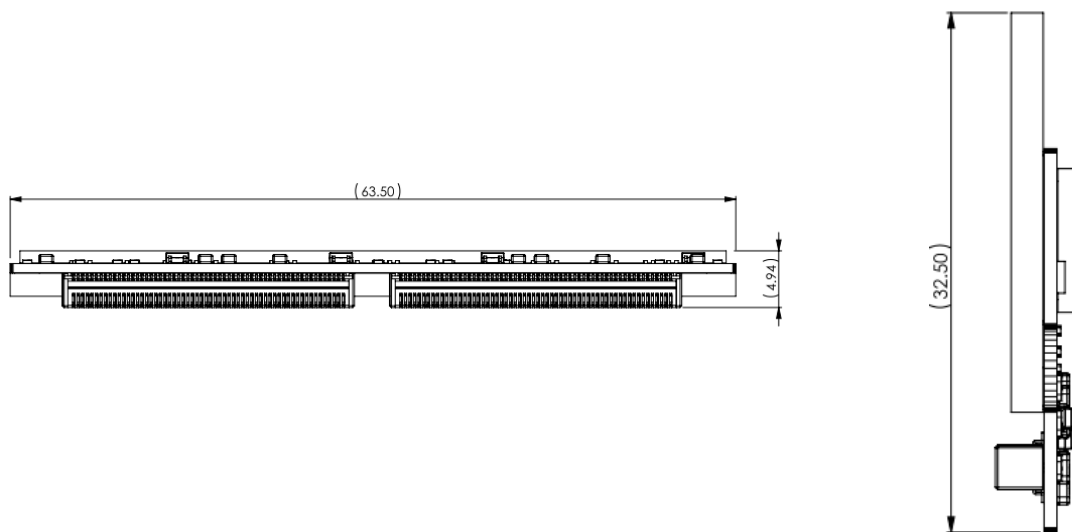
Fig 32: DR-B&W-8k-7-Invar. Tolerance +/- 0.1mm

7.8 Invar package drawing DR-2x8k-7, DR-16k-3.5
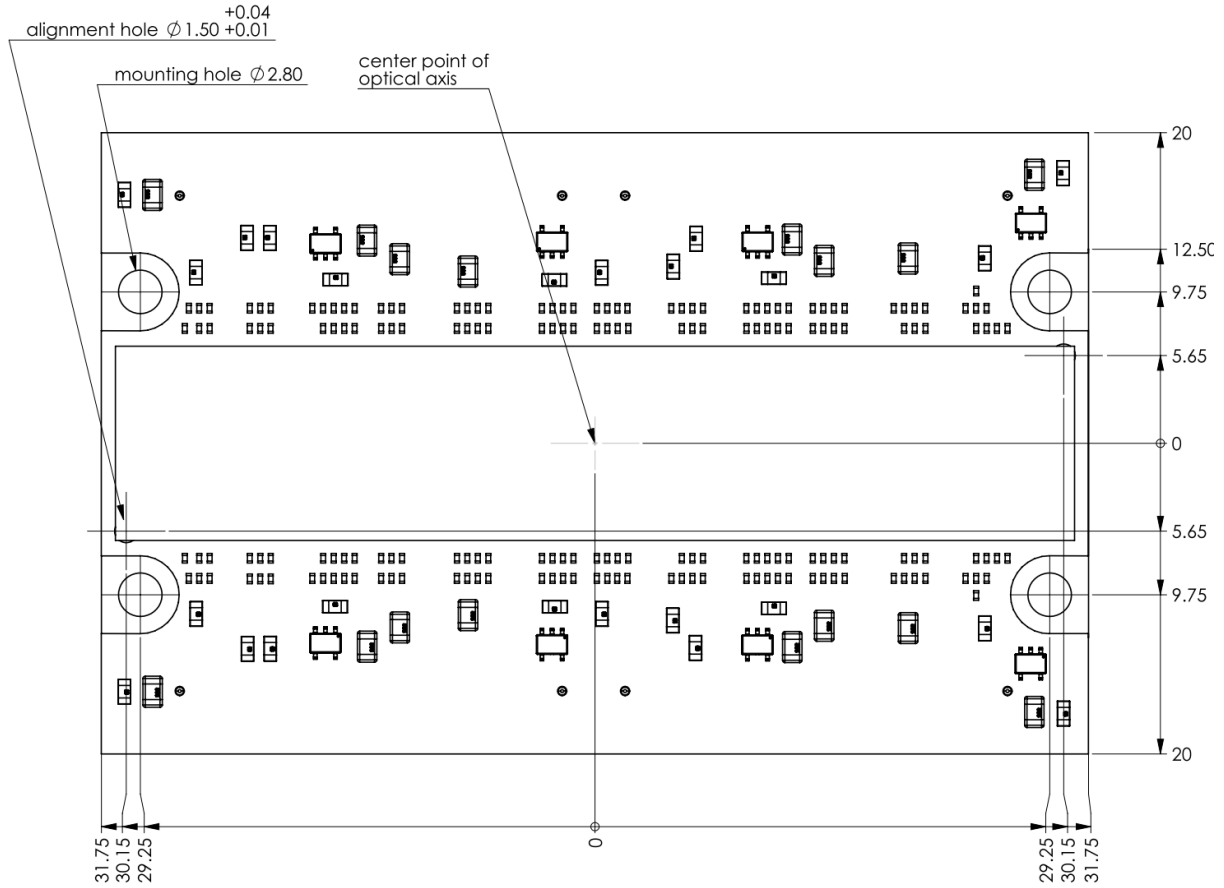
Fig 33: Top view DR-B&W-2x8k-7-Invar and DR-B&W-16k-3.5-Invar. If not otherwise noted all tolerances are +/- 0.1mm
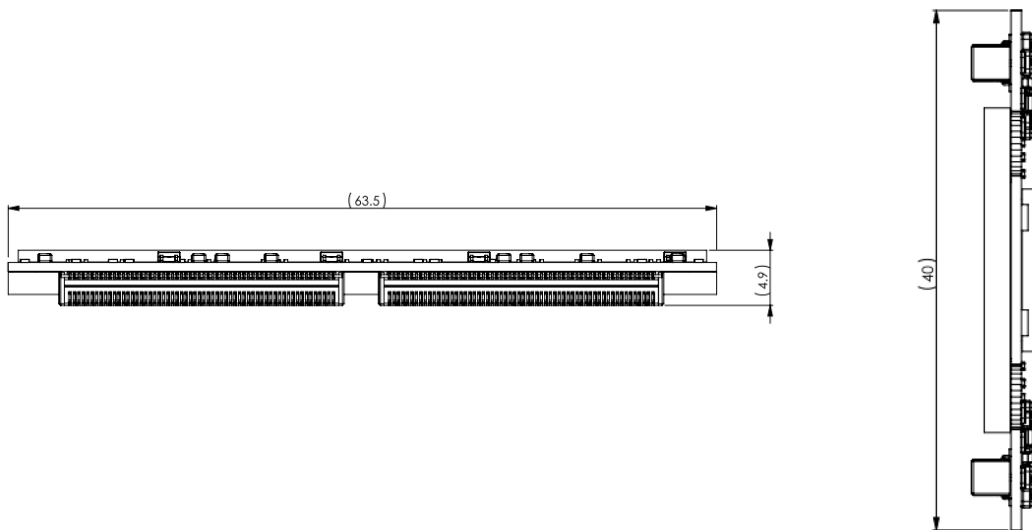
Fig 34: DR-B&W-2x8k-7-Invar, DR-B&W-16k-3.5-Invar. Tolerance +/- 0.1mm

7.9 Invar package drawing DR-24k-3.5
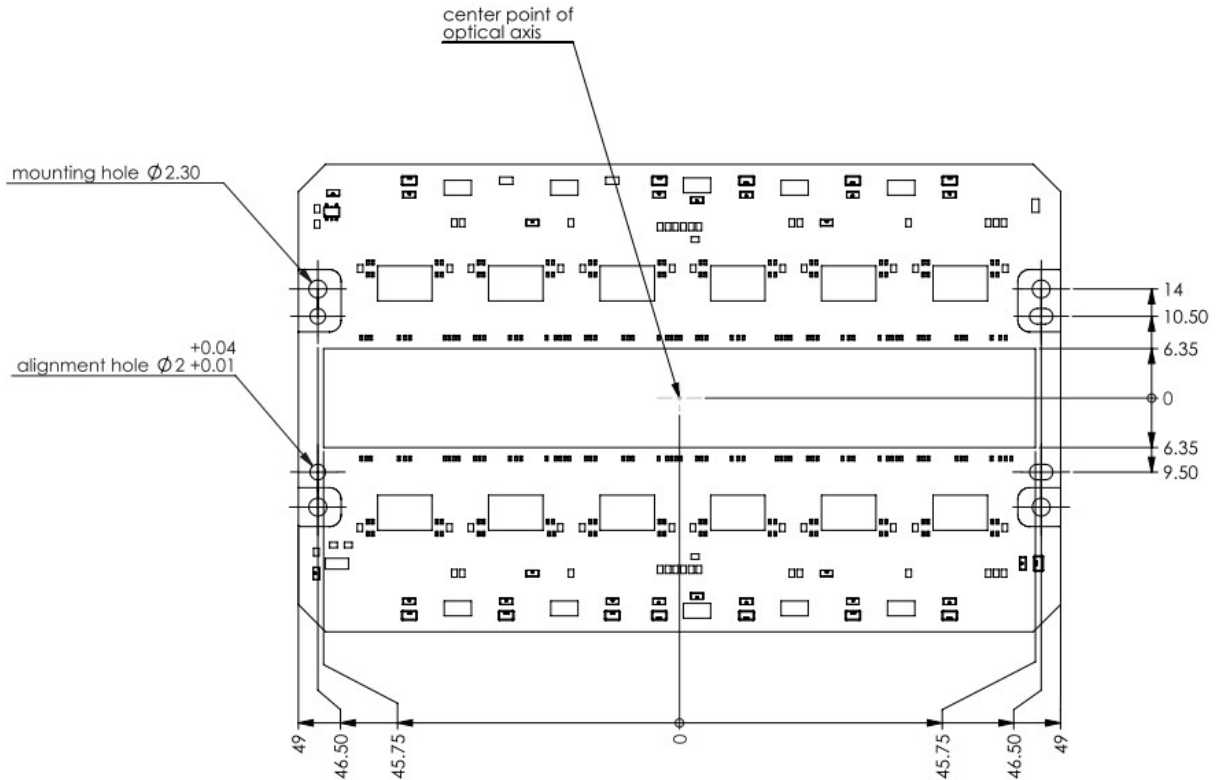
Fig 35: Top view DR-B&W-24k-3.5-Invar. If not otherwise noted all tolerances are +/- 0.1mm
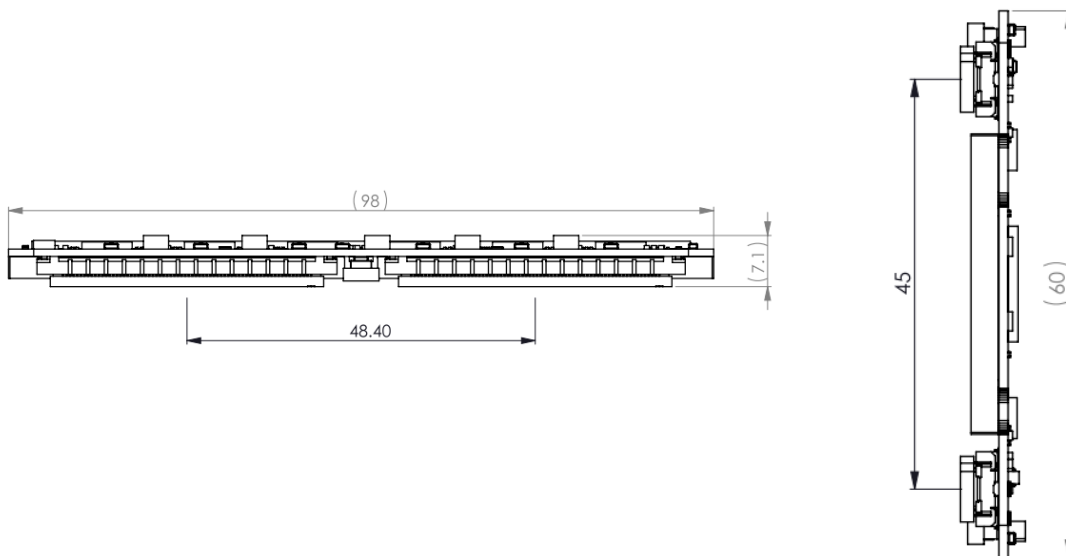
Fig 36: DR-B&W-24k-3.5-Invar. Tolerance +/- 0.1mm

8 Connectors pin outlined

8.1 Pinout DR-2k-7-LCC, DR-2x2k-7-LCC, DR-4k-3.5-LCC

Pin	Signal Name DR-4k-3.5-LCC DR-2x2k-7-LCC	Signal Name DR-2k-7-LCC	Type
1	Tap A1 Bit 11	Tap A1 Bit 11	Digital Output
2	Tap A1 Bit 9	Tap A1 Bit 9	Digital Output
3	Tap A1 Bit 7	Tap A1 Bit 7	Digital Output
4	Tap A1 Bit 5	Tap A1 Bit 5	Digital Output
5	Tap A1 Bit 3	Tap A1 Bit 3	Digital Output
6	Tap A1 Bit 1	Tap A1 Bit 1	Digital Output
7	VSS	VSS	Ground
8	LVAL Tap A1/B1	LVAL Tap A1/B1	Digital Output
9	Tap A1 Bit 12	Tap A1 Bit 12	Digital Output
10	Tap A1 Bit 10	Tap A1 Bit 10	Digital Output
11	Tap A1 Bit 8	Tap A1 Bit 8	Digital Output
12	Tap A1 Bit 6	Tap A1 Bit 6	Digital Output
13	Tap A1 Bit 4	Tap A1 Bit 4	Digital Output
14	Tap A1 Bit 2	Tap A1 Bit 2	Digital Output
14	Tap A1 Bit 0	Tap A1 Bit 0	Digital Output
16	Pixel_CLK_Tap A1/B1	Pixel_CLK_Tap A1/B1	Digital Output
17	END_ADC_TAP A1/B1	END_ADC_TAP A1/B1	Digital Output
18	VSS	VSS	Ground
19	Tap B1 Bit 1	Tap B1 Bit 1	Digital Output
20	Tap B1 Bit 3	Tap B1 Bit 3	Digital Output
21	Tap B1 Bit 5	Tap B1 Bit 5	Digital Output
22	Tap B1 Bit 7	Tap B1 Bit 7	Digital Output
23	Tap B1 Bit 9	Tap B1 Bit 9	Digital Output
24	Tap B1 Bit 11	Tap B1 Bit 11	Digital Output
25	Tap B1 Bit 0	Tap B1 Bit 0	Digital Output
26	Tap B1 Bit 2	Tap B1 Bit 2	Digital Output
27	Tap B1 Bit 4	Tap B1 Bit 4	Digital Output

Pin	Signal Name DR-4k-3.5-LCC DR-2x2k-7-LCC	Signal Name DR-2k-7-LCC	Type
28	VSS	VSS	Ground
29	Tap B1 Bit 6	Tap B1 Bit 6	Digital Output
30	Tap B1 Bit 8	Tap B1 Bit 8	Digital Output
31	Tap B1 Bit 10	Tap B1 Bit 10	Digital Output
32	Tap B1 Bit 12	Tap B1 Bit 12	Digital Output
33	VSS	VSS	Ground
34	VDDA	VDDA	3.3V Analogue
35	VDD	VDD	3.3V supply
36	VDD	VDD	3.3V supply
37	VDD	VDD	3.3V supply
38	VDDA	VDDA	3.3V Analogue
39	N_Reset	N_Reset	Digital Input
40	VSS	Ground	Ground
41	Tap D1 Bit 12	Not connected	Digital Output
42	Tap D1 Bit 10	Not connected	Digital Output
43	Tap D1 Bit 8	Not connected	Digital Output
44	Tap D1 Bit 6	Not connected	Digital Output
45	VSS	VSS	Ground
46	Tap D1 Bit 4	Not connected	Digital Output
47	Tap D1 Bit 2	Not connected	Digital Output
48	Tap D1 Bit 0	Not connected	Digital Output
49	Tap D1 Bit 11	Not connected	Digital Output
50	Tap D1 Bit 9	Not connected	Digital Output
51	Tap D1 Bit 7	Not connected	Digital Output
52	Tap D1 Bit 5	Not connected	Digital Output
53	Tap D1 Bit 3	Not connected	Digital Output
54	Tap D1 Bit 1	Not connected	Digital Output
55	VSS	Ground	Ground
56	END_ADC_TAP C1/D1	Not connected	Digital Output
57	Pixel_CLK_Tap C1/D1	Not connected	Digital Output
58	Tap C1 Bit 0	Not connected	Digital Output

Pin	Signal Name DR-4k-3.5-LCC DR-2x2k-7-LCC	Signal Name DR-2k-7-LCC	Type
59	Tap C1 Bit 2	Not connected	Digital Output
60	Tap C1 Bit 4	Not connected	Digital Output
61	Tap C1 Bit 6	Not connected	Digital Output
62	Tap C1 Bit 8	Not connected	Digital Output
63	Tap C1 Bit 10	Not connected	Digital Output
64	Tap C1 Bit 12	Not connected	Digital Output
65	LVAL Tap C1/D1	Not connected	Digital Output
66	VSS	Ground	Ground
67	MISO C1/D1	Not connected	Digital Output
68	Tap C1 Bit 1	Not connected	Digital Output
69	Tap C1 Bit 3	Not connected	Digital Output
70	Tap C1 Bit 5	Not connected	Digital Output
71	Tap C1 Bit 7	Not connected	Digital Output
72	Tap C1 Bit 9	Not connected	Digital Output
73	VSS	Ground	Ground
74	Tap C1 Bit 11	Not connected	Digital Output
75	RESET_CDS	Digital Input	Digital Input
76	N_CS C1/D1	Not connected	Digital Input
77	MOSI	Digital Input	Digital Input
78	Main_CLK	Digital Input	Digital Input
79	Load_Pulse	Digital Input	Digital Input
80	VSS	Ground	Ground
81	VDD	3.3V	3.3V
82	VDD	3.3V	3.3V
83	VDDA	VDDA	3.3V Analogue
84	VDDA	VDDA	3.3V Analogue
85	N_CS A1/B1	Digital Input	Digital Input
86	SAMPLE	Digital Input	Digital Input
87	RST_CVC	Digital Input	Digital Input
88	SCLK	Digital Input	Digital Input
89	MISO A1/B1	Digital Output	Digital Output

Pin	Signal Name DR-4k-3.5-LCC DR-2x2k-7-LCC	Signal Name DR-2k-7-LCC	Type
90	VSS	Ground	Ground

From LCC version v2.0 there is a separation from chip analogue power to other supplies but without separation on GND pins.

8.2 Connectors for different versions of Invar headboard packages

All Dragster modules, excepting DR-24Kk-3.5, have up to 4 Molex connectors with 120 pin and reference 055339-1208. Dragster 24K-3.5 module uses KELL floating connectors. On the PCB side the matting part is DY01-140S.

The below table indicates which connectors are present for the different chip versions.

Chip version	Present connectors	Connector Reference
DR-2k-7-LCC DR-2x2k-7-LCC DR-4k-3.5-LCC	Not applied	----------------------
DR-4k-7-Invar	Connector 1	Molex 055339-1208
DR-2k-7-Invar DR-2x2k-7-Invar DR-4k-3.5-Invar DR-2x4k-7-Invar DR-6k-7-Invar DR-8k-3.5-Invar	Connector 1 & Connector 2	Molex 055339-1208
DR-8k-7-Invar	Connector 1& Connector 3	Molex 055339-1208
DR-2x8k-7-Invar DR-16k-3.5-Invar	Connector 1 - 4	Molex 055339-1208
DR-24K-3.5-Invar	Connector 1 - 4	KELL DY01-140S

Table 11: Connectors for different chip versions

8.2.1 Connector number identification and pin numbers

60	1
Connector 4	
120	61

60	1
Connector 2	
120	61

60	1
Connector 3	
120	61

60	1
Connector 1	
120	61
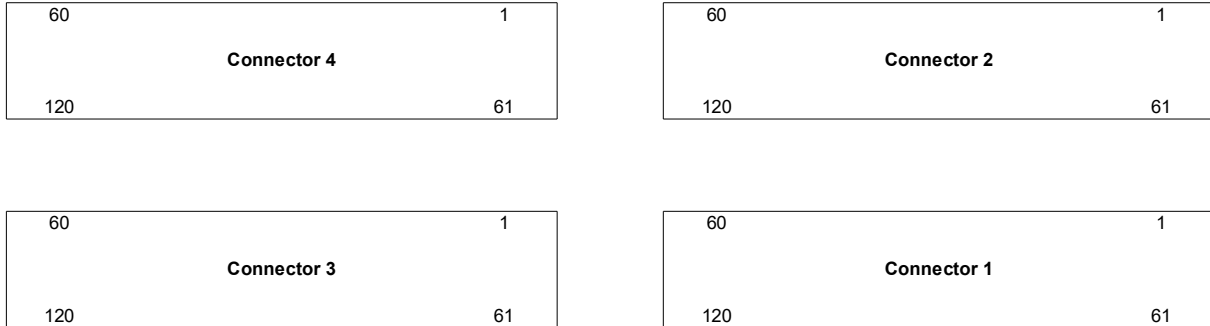
Fig 37: Identification of connector number and pin numbers, DR-16K-3.5 back view

2	140
Connector 4	
1	139

2	140
Connector 2	
1	139

2	140
Connector 3	
1	139

2	140
Connector 1	
1	139
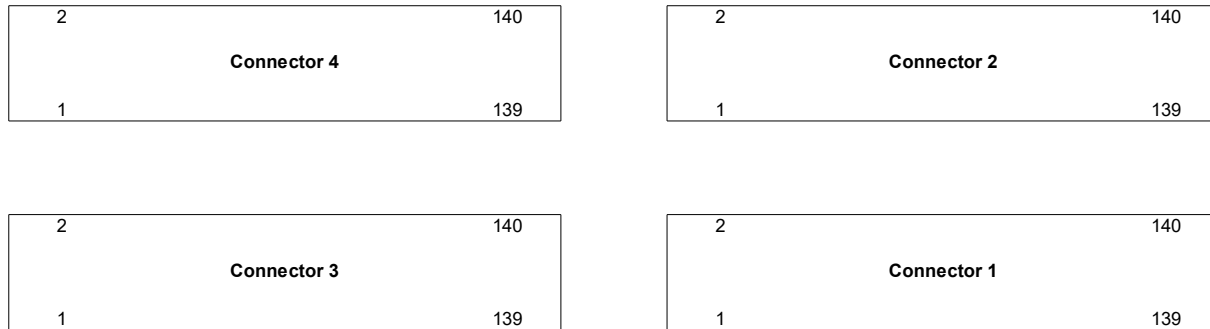
Fig 38: Identification of connector number and pin numbers, DR-24K-3.5 back view

8.3 Connector signal assignment for Invar head board DR-2x2k-7-Invar, DR-4k-3.5-Invar, DR-2k-7-Invar

For DR-2k-7-Invar Connector 2 is present but not required. Only the powers present on the connector are routed to the sensor. Connector 2 can be left completely unconnected for DR-2k-7-Invar.

8.3.1 Connector 1

Pin Number	Signal Name	Signal Type
1	N_CS_AB_1	Dig in
2	MISO_AB_1	Dig out
3	VDDA	VDDA
4	VDDD	VDDD
5	VSSA	GND
6	VSS_BULK	GND
7	VSSD	GND
8	LOAD_PULSE_AB_1	Dig in
9	VDDIO	VDDIO
10	END_ADC_AB_1	Dig out
11	VDDA	VDDA
12	VDD_BULK	VDD_Bulk
13	VDDD	VDDD
14	VDDESD	VDDESD
15	VSSA	GND
16	VSS_BULK	GND
17	VSSD	GND
18	VDDIO	VDDIO
19	TEST_MUX_AB_1	analogue monitor leave n.c.
20	VDDA	VDDA
21	VDDD	VDDD
22	VSSA	GND
23	VSS_BULK	GND
24	VSSD	GND
25	VSSESD/IO	GND
26	PIXEL_CLK_AB_1	Dig_out
27	VCLAMP_AB_1	VDDA
28	SAMPLE_AB	Dig in
29	RST_CDS_AB	Dig in
30	RST_CVC_AB	Dig in
31	Not Connected	
32	SCLK_AB_EF	Dig in
33	MOSI_AB_EF	dig in
34	Not Connected	
35	VDDA	VDDA
36	VDD_BULK	VDD_Bulk

Pin Number	Signal Name	Signal Type
37	VDDD	VDDD
38	VDDESD	VDDESD
39	VSSA	GND
40	VSS_BULK	GND
41	VSSD	GND
42	Not Connected	
43	VDDIO	VDDIO
44	Not Connected	
45	VDDA	VDDA
46	VDDD	VDDD
47	VSSA	GND
48	VSSD	GND
49	VDDIO	VDDIO
50	Not Connected	
51	VDDA	VDDA
52	VDD_BULK	VDD_Bulk
53	VDDD	VDDD
54	VDDESD	VDDESD
55	VSSA	GND
56	VSS_BULK	GND
57	VSSD	GND
58	N_RESET_AB	Dig in
59	Not Connected	
60	Not Connected	
61	VSSESD/IO	GND
62	LVAL_AB_1	Dig out
63	BIT_12_TAP_A1	Dig out
64	BIT_11_TAP_A1	Dig out
65	BIT_10_TAP_A1	Dig out
66	BIT_09_TAP_A1	Dig out
67	BIT_08_TAP_A1	Dig out
68	BIT_07_TAP_A1	Dig out
69	BIT_06_TAP_A1	Dig out
70	BIT_05_TAP_A1	Dig out
71	BIT_04_TAP_A1	Dig out
72	BIT_03_TAP_A1	Dig out
73	BIT_02_TAP_A1	Dig out
74	BIT_01_TAP_A1	Dig out
75	BIT_00_TAP_A1	Dig out
76	VSSESD/IO	GND
77	BIT_00_TAP_B1	Dig out
78	BIT_01_TAP_B1	Dig out
79	BIT_02_TAP_B1	Dig out
80	BIT_03_TAP_B1	Dig out
81	BIT_04_TAP_B1	Dig out
82	BIT_05_TAP_B1	Dig out
83	BIT_06_TAP_B1	Dig out
84	BIT_07_TAP_B1	Dig out
85	BIT_08_TAP_B1	Dig out

Pin Number	Signal Name	Signal Type
86	BIT_09_TAP_B1	Dig out
87	BIT_10_TAP_B1	Dig out
88	BIT_11_TAP_B1	Dig out
89	BIT_12_TAP_B1	Dig out
90	MAIN_CLK	Dig in
91	VSSESD/IO	GND
92	Not Connected	
93	Not Connected	
94	Not Connected	
95	Not Connected	
96	Not Connected	
97	Not Connected	
98	Not Connected	
99	Not Connected	
100	Not Connected	
101	Not Connected	
102	Not Connected	
103	Not Connected	
104	Not Connected	
105	Not Connected	
106	VSSESD/IO	GND
107	Not Connected	
108	Not Connected	
109	Not Connected	
110	Not Connected	
111	Not Connected	
112	Not Connected	
113	Not Connected	
114	Not Connected	
115	Not Connected	
116	Not Connected	
117	Not Connected	
118	Not Connected	
119	Not Connected	
120	VSSESD/IO	GND

Note: SCLK and MOSI are connected between connector 1 and connector 3 in the headboard, resulting names are SCLK_AB_EF and MOSI_AB_EF. User just needs to provide the headboard one pair of this signals to connector 1 or 3 to communicate with the SPI's, taking the advantage that 2 IO lines from the control unit (FPGA or CPLD) are saved. Each SPI can be selected individually by selecting respective negative chip select pin.

8.3.2 Connector 2

Pin Number	Signal Name	Signal Type
1	VSSESD/IO	GND
2	LVAL_CD_1	Dig out
3	BIT_12_TAP_C1	Dig out
4	BIT_11_TAP_C1	Dig out
5	BIT_10_TAP_C1	Dig out
6	BIT_09_TAP_C1	Dig out
7	BIT_08_TAP_C1	Dig out
8	BIT_07_TAP_C1	Dig out
9	BIT_06_TAP_C1	Dig out
10	BIT_05_TAP_C1	Dig out
11	BIT_04_TAP_C1	Dig out
12	BIT_03_TAP_C1	Dig out
13	BIT_02_TAP_C1	Dig out
14	BIT_01_TAP_C1	Dig out
15	BIT_00_TAP_C1	Dig out
16	VSSESD/IO	GND
17	BIT_00_TAP_D1	Dig out
18	BIT_01_TAP_D1	Dig out
19	BIT_02_TAP_D1	Dig out
20	BIT_03_TAP_D1	Dig out
21	BIT_04_TAP_D1	Dig out
22	BIT_05_TAP_D1	Dig out
23	BIT_06_TAP_D1	Dig out
24	BIT_07_TAP_D1	Dig out
25	BIT_08_TAP_D1	Dig out
26	BIT_09_TAP_D1	Dig out
27	BIT_10_TAP_D1	Dig out
28	BIT_11_TAP_D1	Dig out
29	BIT_12_TAP_D1	Dig out
30	Not Connected	
31	VSSESD/IO	GND
32	Not Connected	
33	Not Connected	
34	Not Connected	
35	Not Connected	
36	Not Connected	
37	Not Connected	
38	Not Connected	
39	Not Connected	
40	Not Connected	
41	Not Connected	
42	Not Connected	
43	Not Connected	
44	Not Connected	
45	Not Connected	
46	VSSESD/IO	GND
47	Not Connected	

Pin Number	Signal Name	Signal Type
48	Not Connected	
49	Not Connected	
50	Not Connected	
51	Not Connected	
52	Not Connected	
53	Not Connected	
54	Not Connected	
55	Not Connected	
56	Not Connected	
57	Not Connected	
58	Not Connected	
59	Not Connected	
60	VSSESD/IO	GND
61	N_CS_CD_1	Dig in
62	MISO_CD_1	Dig out
63	VDDA	VDDA
64	VDDD	VDDD
65	VSSA	GND
66	VSS_BULK	GND
67	VSSD	GND
68	LOAD_PULSE_CD_1	Dig in
69	VDDIO	VDDIO
70	END_ADC_CD_1	Dig out
71	VDDA	VDDA
72	VDD_BULK	VDD_Bulk
73	VDDD	VDDD
74	VDDESD	VDDESD
75	VSSA	GND
76	VSS_BULK	GND
77	VSSD	GND
78	VDDIO	VDDIO
79	TEST_MUX_CD_1	analogue monitor leave n.c.
80	VDDA	VDDA
81	VDDD	VDDD
82	VSSA	GND
83	VSS_BULK	GND
84	VSSD	GND
85	VSSESD/IO	GND
86	PIXEL_CLK_CD_1	Dig_out
87	VCLAMP_CD_1	VDDA
88	SAMPLE_CD	Dig in
89	RST_CDS_CD	Dig in
90	RST_CVC_CD	Dig in
91	Not Connected	
92	SCLK_CD_GH	Dig in
93	MOSI_CD_GH	Dig in
94	Not Connected	
95	VDDA	VDDA
96	VDD_BULK	VDD_Bulk

Pin Number	Signal Name	Signal Type
97	VDDD	VDDD
98	VDDESD	VDDESD
99	VSSA	GND
100	VSS_BULK	GND
101	VSSD	GND
102	Not Connected	
103	VDDIO	VDDIO
104	Not Connected	
105	VDDA	VDDA
106	VDDD	VDDD
107	VSSA	GND
108	VSSD	GND
109	VDDIO	VDDIO
110	Not Connected	
111	VDDA	VDDA
112	VDD_BULK	VDD_Bulk
113	VDDD	VDDD
114	VDDESD	VDDESD
115	VSSA	GND
116	VSS_BULK	GND
117	VSSD	GND
118	N_RESET_CD	Dig in
119	Not Connected	
120	Not Connected	

Note: SCLK and MOSI are connected between connector 2 and connector 4 in the headboard, resulting names are SCLK_CD_GH and MOSI_CD_GH. The user just need to provide to the headboard one pair of this signals to connector 2 or 4 to communicate with the SPI's, taking the advantage that 2 IO lines from the control unit (FPGA or CPLD) are saved. Each SPI can be selected individually by selecting respective negative chip select pin.

8.4 Connector signal assignment for Invar head board variations DR-4k-7, DR-8k-7, DR-8k-3.5, DR-16k-3.5, DR-2x4k-7, DR-2x8k-7

The signal assignment for all Invar type headboards is identical, though for smaller chip versions some connectors may not be present. The pin numbers are cyclic, when looking on the connector form the connector side right to left.

8.4.1 Connector 1

Pin Number	Signal Name	Signal Type
1	N_CS_AB_1	Dig in
2	MISO_AB_1	Dig out
3	VDDA	VDDA
4	VDDD	VDDD
5	VSSA	GND
6	VSS_BULK	GND
7	VSSD	GND
8	LOAD_PULSE_AB_1	Dig in
9	VDDIO	VDDIO
10	END_ADC_AB_1	Dig out
11	VDDA	VDDA
12	VDD_BULK	VDD_Bulk
13	VDDD	VDDD
14	VDDESD	VDDESD
15	VSSA	GND
16	VSS_BULK	GND
17	VSSD	GND
18	VDDIO	VDDIO
19	TEST_MUX_AB_1	analogue monitor leave n.c.
20	VDDA	VDDA
21	VDDD	VDDD
22	VSSA	GND
23	VSS_BULK	GND
24	VSSD	GND
25	VSSESD/IO	GND
26	PIXEL_CLK_AB_1	Dig_out
27	VCLAMP_AB_1	VDDA
28	SAMPLE_AB	Dig in
29	RST_CDS_AB	Dig in
30	RST_CVC_AB	Dig in
31	N_CS_AB_2	Dig in
32	SCLK_AB_EF	Dig in
33	MOSI_AB_EF	dig in
34	MISO_AB_2	Dig out
35	VDDA	VDDA
36	VDD_BULK	VDD_Bulk
37	VDDD	VDDD
38	VDDESD	VDDESD

Pin Number	Signal Name	Signal Type
39	VSSA	GND
40	VSS_BULK	GND
41	VSSD	GND
42	LOAD_PULSE_AB_2	Dig in
43	VDDIO	VDDIO
44	END_ADC_AB_2	Dig out
45	VDDA	VDDA
46	VDDD	VDDD
47	VSSA	GND
48	VSSD	GND
49	VDDIO	VDDIO
50	TEST_MUX_AB_2	analogue monitor leave n.c.
51	VDDA	VDDA
52	VDD_BULK	VDD_Bulk
53	VDDD	VDDD
54	VDDESD	VDDESD
55	VSSA	GND
56	VSS_BULK	GND
57	VSSD	GND
58	N_RESET_AB	Dig in
59	PIXEL_CLOCK_AB_2	Dig out
60	VCLAMP_AB_2	VDDA
61	VSSESD/IO	GND
62	LVAL_AB_1	Dig out
63	BIT_12_TAP_A1	Dig out
64	BIT_11_TAP_A1	Dig out
65	BIT_10_TAP_A1	Dig out
66	BIT_09_TAP_A1	Dig out
67	BIT_08_TAP_A1	Dig out
68	BIT_07_TAP_A1	Dig out
69	BIT_06_TAP_A1	Dig out
70	BIT_05_TAP_A1	Dig out
71	BIT_04_TAP_A1	Dig out
72	BIT_03_TAP_A1	Dig out
73	BIT_02_TAP_A1	Dig out
74	BIT_01_TAP_A1	Dig out
75	BIT_00_TAP_A1	Dig out
76	VSSESD/IO	GND
77	BIT_00_TAP_B1	Dig out
78	BIT_01_TAP_B1	Dig out
79	BIT_02_TAP_B1	Dig out
80	BIT_03_TAP_B1	Dig out
81	BIT_04_TAP_B1	Dig out
82	BIT_05_TAP_B1	Dig out
83	BIT_06_TAP_B1	Dig out
84	BIT_07_TAP_B1	Dig out
85	BIT_08_TAP_B1	Dig out
86	BIT_09_TAP_B1	Dig out
87	BIT_10_TAP_B1	Dig out

Pin Number	Signal Name	Signal Type
88	BIT_11_TAP_B1	Dig out
89	BIT_12_TAP_B1	Dig out
90	MAIN_CLK	Dig in
91	VSSESD/IO	GND
92	LVAL_AB_2	Dig out
93	BIT_12_TAP_A2	Dig out
94	BIT_11_TAP_A2	Dig out
95	BIT_10_TAP_A2	Dig out
96	BIT_09_TAP_A2	Dig out
97	BIT_08_TAP_A2	Dig out
98	BIT_07_TAP_A2	Dig out
99	BIT_06_TAP_A2	Dig out
100	BIT_05_TAP_A2	Dig out
101	BIT_04_TAP_A2	Dig out
102	BIT_03_TAP_A2	Dig out
103	BIT_02_TAP_A2	Dig out
104	BIT_01_TAP_A2	Dig out
105	BIT_00_TAP_A2	Dig out
106	VSSESD/IO	GND
107	BIT_00_TAP_B2	Dig out
108	BIT_01_TAP_B2	Dig out
109	BIT_02_TAP_B2	Dig out
110	BIT_03_TAP_B2	Dig out
111	BIT_04_TAP_B2	Dig out
112	BIT_05_TAP_B2	Dig out
113	BIT_06_TAP_B2	Dig out
114	BIT_07_TAP_B2	Dig out
115	BIT_08_TAP_B2	Dig out
116	BIT_09_TAP_B2	Dig out
117	BIT_10_TAP_B2	Dig out
118	BIT_11_TAP_B2	Dig out
119	BIT_12_TAP_B2	Dig out
120	VSSESD/IO	GND

Note: SCLK and MOSI are connected between connector 1 and connector 3 in the headboard, resulting names are SCLK_AB_EF and MOSI_AB_EF. User just need to provide to the headboard one pair of this signals to connector 1 or 3 to communicate with the SPI's, taking the advantage that 2 IO lines from the control unit (FPGA or CPLD) are saved. Each SPI can be selected individually by selecting respective negative chip select pin.

8.4.2 Connector 2

Pin Number	Signal Name	Signal Type
1	VSSESD/IO	GND
2	LVAL_CD_1	Dig out
3	BIT_12_TAP_C1	Dig out
4	BIT_11_TAP_C1	Dig out
5	BIT_10_TAP_C1	Dig out
6	BIT_09_TAP_C1	Dig out
7	BIT_08_TAP_C1	Dig out
8	BIT_07_TAP_C1	Dig out
9	BIT_06_TAP_C1	Dig out
10	BIT_05_TAP_C1	Dig out
11	BIT_04_TAP_C1	Dig out
12	BIT_03_TAP_C1	Dig out
13	BIT_02_TAP_C1	Dig out
14	BIT_01_TAP_C1	Dig out
15	BIT_00_TAP_C1	Dig out
16	VSSESD/IO	GND
17	BIT_00_TAP_D1	Dig out
18	BIT_01_TAP_D1	Dig out
19	BIT_02_TAP_D1	Dig out
20	BIT_03_TAP_D1	Dig out
21	BIT_04_TAP_D1	Dig out
22	BIT_05_TAP_D1	Dig out
23	BIT_06_TAP_D1	Dig out
24	BIT_07_TAP_D1	Dig out
25	BIT_08_TAP_D1	Dig out
26	BIT_09_TAP_D1	Dig out
27	BIT_10_TAP_D1	Dig out
28	BIT_11_TAP_D1	Dig out
29	BIT_12_TAP_D1	Dig out
30	NC	not connected
31	VSSESD/IO	GND
32	LVAL_CD_2	Dig out
33	BIT_12_TAP_C2	Dig out
34	BIT_11_TAP_C2	Dig out
35	BIT_10_TAP_C2	Dig out
36	BIT_09_TAP_C2	Dig out
37	BIT_08_TAP_C2	Dig out
38	BIT_07_TAP_C2	Dig out
39	BIT_06_TAP_C2	Dig out
40	BIT_05_TAP_C2	Dig out
41	BIT_04_TAP_C2	Dig out
42	BIT_03_TAP_C2	Dig out
43	BIT_02_TAP_C2	Dig out
44	BIT_01_TAP_C2	Dig out
45	BIT_00_TAP_C2	Dig out
46	VSSESD/IO	GND

Pin Number	Signal Name	Signal Type
47	BIT_00_TAP_D2	Dig out
48	BIT_01_TAP_D2	Dig out
49	BIT_02_TAP_D2	Dig out
50	BIT_03_TAP_D2	Dig out
51	BIT_04_TAP_D2	Dig out
52	BIT_05_TAP_D2	Dig out
53	BIT_06_TAP_D2	Dig out
54	BIT_07_TAP_D2	Dig out
55	BIT_08_TAP_D2	Dig out
56	BIT_09_TAP_D2	Dig out
57	BIT_10_TAP_D2	Dig out
58	BIT_11_TAP_D2	Dig out
59	BIT_12_TAP_D2	Dig out
60	VSSESD/IO	GND
61	N_CS_CD_1	Dig in
62	MISO_CD_1	Dig out
63	VDDA	VDDA
64	VDDD	VDDD
65	VSSA	GND
66	VSS_BULK	GND
67	VSSD	GND
68	LOAD_PULSE_CD_1	Dig in
69	VDDIO	VDDIO
70	END_ADC_CD_1	Dig out
71	VDDA	VDDA
72	VDD_BULK	VDD_Bulk
73	VDDD	VDDD
74	VDDESD	VDDESD
75	VSSA	GND
76	VSS_BULK	GND
77	VSSD	GND
78	VDDIO	VDDIO
79	TEST_MUX_CD_1	analogue monitor leave n.c.
80	VDDA	VDDA
81	VDDD	VDDD
82	VSSA	GND
83	VSS_BULK	GND
84	VSSD	GND
85	VSSESD/IO	GND
86	PIXEL_CLK_CD_1	Dig_out
87	VCLAMP_CD_1	VDDA
88	SAMPLE_CD	Dig in
89	RST_CDS_CD	Dig in
90	RST_CVC_CD	Dig in
91	N_CS_CD_2	Dig in
92	SCLK_CD_GH	Dig in
93	MOSI_CD_GH	Dig in
94	MISO_CD_2	Dig out
95	VDDA	VDDA

Pin Number	Signal Name	Signal Type
96	VDD_BULK	VDD_Bulk
97	VDDD	VDDD
98	VDDESD	VDDESD
99	VSSA	GND
100	VSS_BULK	GND
101	VSSD	GND
102	LOAD_PULSE_CD_2	Dig in
103	VDDIO	VDDIO
104	END_ADC_CD_2	Dig out
105	VDDA	VDDA
106	VDDD	VDDD
107	VSSA	GND
108	VSSD	GND
109	VDDIO	VDDIO
110	TEST_MUX_CD_2	analogue monitor leave n.c.
111	VDDA	VDDA
112	VDD_BULK	VDD_Bulk
113	VDDD	VDDD
114	VDDESD	VDDESD
115	VSSA	GND
116	VSS_BULK	GND
117	VSSD	GND
118	N_RESET_CD	Dig in
119	PIXEL_CLK_CD_2	Dig_out
120	VCLAMP_CD_2	VDDA

Note: SCLK and MOSI are connected between connector 2 and connector 4 in the headboard, resulting names are SCLK_CD_GH and MOSI_CD_GH. The user just need to provide to the headboard one pair of this signals to connector 2 or 4 to communicate with the SPI's, taking the advantage that 2 IO lines from the control unit (FPGA or CPLD) are saved. Each SPI can be selected individually by selecting respective negative chip select pin.

8.4.3 Connector 3

Pin Number	Signal Name	Signal Type
1	N_CS_EF_1	Dig in
2	MISO_EF_1	Dig out
3	VDDA	VDDA
4	VDDD	VDDD
5	VSSA	GND
6	VSS_BULK	GND
7	VSSD	GND
8	LOAD_PULSE_EF_1	Dig in
9	VDDIO	VDDIO
10	END_ADC_EF_1	Dig out
11	VDDA	VDDA
12	VDD_BULK	VDD_Bulk
13	VDDD	VDDD
14	VDDESD	VDDESD
15	VSSA	GND
16	VSS_BULK	GND
17	VSSD	GND
18	VDDIO	VDDIO
19	TEST_MUX_EF_1	analogue monitor leave n.c.
20	VDDA	VDDA
21	VDDD	VDDD
22	VSSA	GND
23	VSS_BULK	GND
24	VSSD	GND
25	VSSESD/IO	GND
26	PIXEL_CLK_EF_1	Dig_out
27	VCLAMP_EF_1	VDDA
28	SAMPLE_EF	Dig in
29	RST_CDS_EF	Dig in
30	RST_CVC_EF	Dig in
31	N_CS_EF_2	Dig in
32	SCLK_AB_EF	Dig in
33	MOSI_AB_EF	dig in
34	MISO_EF_2	Dig out
35	VDDA	VDDA
36	VDD_BULK	VDD_Bulk
37	VDDD	VDDD
38	VDDESD	VDDESD
39	VSSA	GND
40	VSS_BULK	GND
41	VSSD	GND
42	LOAD_PULSE_EF_2	Dig in
43	VDDIO	VDDIO
44	END_ADC_EF_2	Dig out
45	VDDA	VDDA
46	VDDD	VDDD
47	VSSA	GND

Pin Number	Signal Name	Signal Type
48	VSSD	GND
49	VDDIO	VDDIO
50	TEST_MUX_EF_2	analogue monitor leave n.c.
51	VDDA	VDDA
52	VDD_BULK	VDD_Bulk
53	VDDD	VDDD
54	VDDESD	VDDESD
55	VSSA	GND
56	VSS_BULK	GND
57	VSSD	GND
58	N_RESET_EF	Dig in
59	PIXEL_CLOCK_EF_2	Dig out
60	VCLAMP_EF_2	VDDA
61	VSSESD/IO	GND
62	LVAL_EF_1	Dig out
63	BIT_12_TAP_E1	Dig out
64	BIT_11_TAP_E1	Dig out
65	BIT_10_TAP_E1	Dig out
66	BIT_09_TAP_E1	Dig out
67	BIT_08_TAP_E1	Dig out
68	BIT_07_TAP_E1	Dig out
69	BIT_06_TAP_E1	Dig out
70	BIT_05_TAP_E1	Dig out
71	BIT_04_TAP_E1	Dig out
72	BIT_03_TAP_E1	Dig out
73	BIT_02_TAP_E1	Dig out
74	BIT_01_TAP_E1	Dig out
75	BIT_00_TAP_E1	Dig out
76	VSSESD/IO	GND
77	BIT_00_TAP_F1	Dig out
78	BIT_01_TAP_F1	Dig out
79	BIT_02_TAP_F1	Dig out
80	BIT_03_TAP_F1	Dig out
81	BIT_04_TAP_F1	Dig out
82	BIT_05_TAP_F1	Dig out
83	BIT_06_TAP_F1	Dig out
84	BIT_07_TAP_F1	Dig out
85	BIT_08_TAP_F1	Dig out
86	BIT_09_TAP_F1	Dig out
87	BIT_10_TAP_F1	Dig out
88	BIT_11_TAP_F1	Dig out
89	BIT_12_TAP_F1	Dig out
90	MAIN_CLK	Dig in
91	VSSESD/IO	GND
92	LVAL_EF_2	Dig out
93	BIT_12_TAP_E2	Dig out
94	BIT_11_TAP_E2	Dig out
95	BIT_10_TAP_E2	Dig out
96	BIT_09_TAP_E2	Dig out

Pin Number	Signal Name	Signal Type
97	BIT_08_TAP_E2	Dig out
98	BIT_07_TAP_E2	Dig out
99	BIT_06_TAP_E2	Dig out
100	BIT_05_TAP_E2	Dig out
101	BIT_04_TAP_E2	Dig out
102	BIT_03_TAP_E2	Dig out
103	BIT_02_TAP_E2	Dig out
104	BIT_01_TAP_E2	Dig out
105	BIT_00_TAP_E2	Dig out
106	VSSESD/IO	GND
107	BIT_00_TAP_F2	Dig out
108	BIT_01_TAP_F2	Dig out
109	BIT_02_TAP_F2	Dig out
110	BIT_03_TAP_F2	Dig out
111	BIT_04_TAP_F2	Dig out
112	BIT_05_TAP_F2	Dig out
113	BIT_06_TAP_F2	Dig out
114	BIT_07_TAP_F2	Dig out
115	BIT_08_TAP_F2	Dig out
116	BIT_09_TAP_F2	Dig out
117	BIT_10_TAP_F2	Dig out
118	BIT_11_TAP_F2	Dig out
119	BIT_12_TAP_F2	Dig out
120	VSSESD/IO	GND

8.4.4 Connector 4

Pin Number	Signal Name	Signal Type
1	VSSESD/IO	GND
2	LVAL_GH_1	Dig out
3	BIT_12_TAP_G1	Dig out
4	BIT_11_TAP_G1	Dig out
5	BIT_10_TAP_G1	Dig out
6	BIT_09_TAP_G1	Dig out
7	BIT_08_TAP_G1	Dig out
8	BIT_07_TAP_G1	Dig out
9	BIT_06_TAP_G1	Dig out
10	BIT_05_TAP_G1	Dig out
11	BIT_04_TAP_G1	Dig out
12	BIT_03_TAP_G1	Dig out
13	BIT_02_TAP_G1	Dig out
14	BIT_01_TAP_G1	Dig out
15	BIT_00_TAP_G1	Dig out
16	VSSESD/IO	GND
17	BIT_00_TAP_H1	Dig out
18	BIT_01_TAP_H1	Dig out
19	BIT_02_TAP_H1	Dig out
20	BIT_03_TAP_H1	Dig out
21	BIT_04_TAP_H1	Dig out
22	BIT_05_TAP_H1	Dig out
23	BIT_06_TAP_H1	Dig out
24	BIT_07_TAP_H1	Dig out
25	BIT_08_TAP_H1	Dig out
26	BIT_09_TAP_H1	Dig out
27	BIT_10_TAP_H1	Dig out
28	BIT_11_TAP_H1	Dig out
29	BIT_12_TAP_H1	Dig out
30	NC	not connected
31	VSSESD/IO	GND
32	LVAL_GH_2	Dig out
33	BIT_12_TAP_G2	Dig out
34	BIT_11_TAP_G2	Dig out
35	BIT_10_TAP_G2	Dig out
36	BIT_09_TAP_G2	Dig out
37	BIT_08_TAP_G2	Dig out
38	BIT_07_TAP_G2	Dig out
39	BIT_06_TAP_G2	Dig out
40	BIT_05_TAP_G2	Dig out
41	BIT_04_TAP_G2	Dig out
42	BIT_03_TAP_G2	Dig out
43	BIT_02_TAP_G2	Dig out
44	BIT_01_TAP_G2	Dig out
45	BIT_00_TAP_G2	Dig out
46	VSSESD/IO	GND
47	BIT_00_TAP_H2	Dig out

Pin Number	Signal Name	Signal Type
48	BIT_01_TAP_H2	Dig out
49	BIT_02_TAP_H2	Dig out
50	BIT_03_TAP_H2	Dig out
51	BIT_04_TAP_H2	Dig out
52	BIT_05_TAP_H2	Dig out
53	BIT_06_TAP_H2	Dig out
54	BIT_07_TAP_H2	Dig out
55	BIT_08_TAP_H2	Dig out
56	BIT_09_TAP_H2	Dig out
57	BIT_10_TAP_H2	Dig out
58	BIT_11_TAP_H2	Dig out
59	BIT_12_TAP_H2	Dig out
60	VSSESD/IO	GND
61	N_CS_GH_1	Dig in
62	MISO_GH_1	Dig out
63	VDDA	VDDA
64	VDDD	VDDD
65	VSSA	GND
66	VSS_BULK	GND
67	VSSD	GND
68	LOAD_PULSE_GH_1	Dig in
69	VDDIO	VDDIO
70	END_ADC_GH_1	Dig out
71	VDDA	VDDA
72	VDD_BULK	VDD_Bulk
73	VDDD	VDDD
74	VDDESD	VDDESD
75	VSSA	GND
76	VSS_BULK	GND
77	VSSD	GND
78	VDDIO	VDDIO
79	TEST_MUX_GH_1	analogue monitor leave n.c.
80	VDDA	VDDA
81	VDDD	VDDD
82	VSSA	GND
83	VSS_BULK	GND
84	VSSD	GND
85	VSSESD/IO	GND
86	PIXEL_CLK_GH_1	Dig_out
87	VCLAMP_GH_1	VDDA
88	SAMPLE_GH	Dig in
89	RST_CDS_GH	Dig in
90	RST_CVC_GH	Dig in
91	N_CS_GH_2	Dig in
92	SCLK_CD_GH	Dig in
93	MOSI_CD_GH	Dig in
94	MISO_GH_2	Dig out
95	VDDA	VDDA
96	VDD_BULK	VDD_Bulk

Pin Number	Signal Name	Signal Type
97	VDDD	VDDD
98	VDDESD	VDDESD
99	VSSA	GND
100	VSS_BULK	GND
101	VSSD	GND
102	LOAD_PULSE_GH_2	Dig in
103	VDDIO	VDDIO
104	END_ADC_GH_2	Dig out
105	VDDA	VDDA
106	VDDD	VDDD
107	VSSA	GND
108	VSSD	GND
109	VDDIO	VDDIO
110	TEST_MUX_GH_2	analogue monitor leave n.c.
111	VDDA	VDDA
112	VDD_BULK	VDD_Bulk
113	VDDD	VDDD
114	VDDESD	VDDESD
115	VSSA	GND
116	VSS_BULK	GND
117	VSSD	GND
118	N_RESET_GH	Dig in
119	PIXEL_CLK_GH_2	Dig_out
120	VCLAMP_GH_2	VDDA

8.5 Connector signal assignment for Invar head board DR-6K-7

Pin Number	Signal Name	
	Bottom, Connector 1	**Top, Connector 2**
1	N_CS_AB_1	GND_D
2	MISO_AB_1	LVAL_EF_1
3	VDDA	Not connected
4	VDDD	BIT_11_TAP_A1
5	GND_D	BIT_10_TAP_A1
6	GND_D	BIT_09_TAP_A1
7	GND_A	BIT_08_TAP_A1
8	Load_Pulse_AB_1	BIT_07_TAP_A1
9	VDDIO	BIT_06_TAP_A1
10	End_ADC_AB_1	BIT_05_TAP_A1
11	VDDA	BIT_04_TAP_A1
12	VDD_Bulk	BIT_03_TAP_A1
13	VDDD	BIT_02_TAP_A1
14	VDDESD	BIT_01_TAP_A1
15	GND_D	BIT_00_TAP_A1
16	GND_D	GND_D
17	GND_A	Not connected
18	VDDIO	Not connected
19	Test_Mux	Not connected
20	VDDA	Not connected
21	VDDD	Not connected
22	GND_D	Not connected
23	GND_D	Not connected
24	GND_D	Not connected
25	GND_A	Not connected
26	Pixel_Clk_AB_1	Not connected
27	Not connected	Not connected
28	Sample_AB	Not connected
29	RST_CDS_AB	Not connected
30	RST_CVC_AB	Not connected
31	N_CS_AB_2	GND_D

Pin Number	Bottom, Connector 1	Top, Connector 2
32	SCLK_AB_EF	Not connected
33	MOSI_AB_EF	Not connected
34	MISO_AB_2	Not connected
35	VDDA	Not connected
36	VDD_BULK	Not connected
37	VDDD	Not connected
38	VDDESD	Not connected
39	GND_D	Not connected
40	GND_D	Not connected
41	GND_A	Not connected
42	Load_Pulse_AB_2	Not connected
43	VDDIO	Not connected
44	End_ADC_AB_2	Not connected
45	VDDA	Not connected
46	VDDD	GND_D
47	GND_D	BIT_00_TAP_F1
48	GND_A	BIT_01_TAP_F1
49	VDDIO	BIT_02_TAP_F1
50	Not connected	BIT_03_TAP_F1
51	VDDA	BIT_04_TAP_F1
52	VDD_Bulk	BIT_05_TAP_F1
53	VDDD	BIT_06_TAP_F1
54	VDDESD	BIT_07_TAP_F1
55	GND_D	BIT_08_TAP_F1
56	GND_D	BIT_09_TAP_F1
57	GND_A	BIT_10_TAP_F1
58	N_Reset_AB	BIT_11_TAP_F1
59	Pixel_Clk_AB_2	Not connected
60	Not connected	GND_D
61	GND_D	N_CS_EF_1
62	LVAL_AB_1	MISO_EF_1
63	Not connected	Not connected
64	BIT_00_TAP_B1	Not connected

Pin Number	Bottom, Connector 1	Top, Connector 2
65	BIT_01_TAP_B1	GND_D
66	BIT_02_TAP_B1	GND_D
67	BIT_03_TAP_B1	GND_A
68	BIT_04_TAP_B1	Load_Pulse_EF_1
69	BIT_05_TAP_B1	Not connected
70	BIT_06_TAP_B1	End_ADC_EF_1
71	BIT_07_TAP_B1	Not connected
72	BIT_08_TAP_B1	Not connected
73	BIT_09_TAP_B1	Not connected
74	BIT_10_TAP_B1	Not connected
75	BIT_11_TAP_B1	GND_D
76	GND_D	GND_D
77	BIT_11_TAP_A2	GND_A
78	BIT_10_TAP_A2	Not connected
79	BIT_09_TAP_A2	Not connected
80	BIT_08_TAP_A2	Not connected
81	BIT_07_TAP_A2	Not connected
82	BIT_06_TAP_A2	GND_D
83	BIT_05_TAP_A2	GND_D
84	BIT_04_TAP_A2	GND_D
85	BIT_03_TAP_A2	GND_A
86	BIT_02_TAP_A2	Pixel_Clk_EF_1
87	BIT_01_TAP_A2	Not connected
88	BIT_00_TAP_A2	Sample_EF
89	Not connected	RST_CDS_EF
90	Main_Clk	RST_CVC_EF
91	GND_D	ID_Chip
92	LVAL_AB_2	Not connected
93	Not connected	Not connected
94	BIT_00_TAP_B2	Not connected
95	BIT_01_TAP_B2	Not connected
96	BIT_02_TAP_B2	Not connected
97	BIT_03_TAP_B2	Not connected

Pin Number	Bottom, Connector 1	Top, Connector 2
98	BIT_04_TAP_B2	Not connected
99	BIT_05_TAP_B2	GND_D
100	BIT_06_TAP_B2	GND_D
101	BIT_07_TAP_B2	GND_A
102	BIT_08_TAP_B2	Not connected
103	BIT_09_TAP_B2	Not connected
104	BIT_10_TAP_B2	Not connected
105	BIT_11_TAP_B2	Not connected
106	GND_D	3.3V_Digital
107	BIT_11_TAP_E1	GND_D
108	BIT_10_TAP_E1	GND_A
109	BIT_09_TAP_E1	Not connected
110	BIT_08_TAP_E1	Not connected
111	BIT_07_TAP_E1	Not connected
112	BIT_06_TAP_E1	Not connected
113	BIT_05_TAP_E1	Not connected
114	BIT_04_TAP_E1	3.3V_Digital
115	BIT_03_TAP_E1	GND_D
116	BIT_02_TAP_E1	GND_D
117	BIT_01_TAP_E1	GND_A
118	BIT_00_TAP_E1	N_Reset_EF
119	Not connected	Not connected
120	GND_D	Not connected

8.6 Connector signal assignment for Invar head board DR-24K-3.5

8.6.1 Connector 1

Name	Pin No	Pin No	Name
RESET_CDS_C	1	2	SAMPLE_C
RESET_CVC_C	3	4	LOAD_PULSE_A2
SENSORDATA_A8_N	5	6	SENSORDATA_A8_P
N_CS_C1	7	8	
SENSORDATA_A9_N	9	10	SENSORDATA_A9_P
END_ADC_C1	11	12	
SENSORDATA_A10_N	13	14	SENSORDATA_A10_P
LOAD_PULSE_C1	15	16	
SENSORCLK_A3_N	17	18	SENSORCLK_A3_P
GND	19	20	GND
SENSORDATA_A11_N	21	22	SENSORDATA_A11_P
	23	24	
	25	26	
GND	27	28	GND
	29	30	
3V3_VDDESD	31	32	3V3_VDDESD
	33	34	
GND	35	36	GND
	37	38	
GND	39	40	N_CS_A3
GIO_1	41	42	
GIO_2	43	44	SHTDN_N_TX_BOT_EXT
3.3V_VDDESD	45	46	MCLK_SENSOR_A
	47	48	
GND	49	50	GND
	51	52	
GND	53	54	GND
	55	56	
3.3V_VDDESD	57	58	3.3V_VDDESD
	59	60	
GND	61	62	GND
SENSORDATA_A4_N	63	64	SENSORDATA_A4_P
	65	66	
SENSORDATA_A5_N	67	68	SENSORDATA_A5_P
GND	69	70	GND
SENSORDATA_A6_N	71	72	SENSORDATA_A6_P
	73	74	
SENSORCLK_A2_N	75	76	SENSORCLK_A2_P
GND	77	78	GND
SENSORDATA_A7_N	79	80	SENSORDATA_A7_P
P3V3A	81	82	P3V3A
P3V3A	83	84	P3V3A
P3V3A	85	86	P3V3A
P3V3A	87	88	N_CS_A2
P3V3A	89	90	N_RESET_LOGIC_A
	91	92	
GND	93	94	GND
SENSORDATA_A0_N	95	96	SENSORDATA_A0_P
	97	98	
SENSORDATA_A1_N	99	100	SENSORDATA_A1_P
GND	101	102	GND
SENSORDATA_A2_N	103	104	SENSORDATA_A2_P
	105	106	
SENSORCLK_A1_N	107	108	SENSORCLK_A1_P
GND	109	110	GND
SENSORDATA_A3_N	111	112	SENSORDATA_A3_P
	113	114	
	115	116	
GND	117	118	GND
	119	120	
3.3V_VDDESD	121	122	3.3V_VDDESD
	123	124	
GND	125	126	GND
TEST_MUX_AC	127	128	LOAD_PULSE_A1
END_ADC_A1	129	130	MISO_A
N_CS_A1	131	132	MOSI_A
SAMPLE_A	133	134	SCLK_A
P3V3A	135	136	RESET_CVC_A
P3V3A	137	138	RESET_CDS_A
P3V3A	139	140	ID-CHIP

8.6.2 Connector 2

Name	Pin No	Pin No	Name
SAMPLE_D	1	2	RESET_CDS_D
LOAD_PULSE_B2	3	4	RESET_CVC_D
SENSORDATA_B11_P	5	6	SENSORDATA_B11_N
	7	8	N_CS_D1
SENSORCLK_B3_P	9	10	SENSORCLK_B3_N
	11	12	END_ADC_D1
SENSORDATA_B10_P	13	14	SENSORDATA_B10_N
	15	16	LOAD_PULSE_D1
SENSORDATA_B9_P	17	18	SENSORDATA_B9_N
GND	19	20	GND
SENSORDATA_B8_P	21	22	SENSORDATA_B8_N
	23	24	P1V8
	25	26	
GND	27	28	GND
	29	30	
3V3_VDDESD	31	32	3V3_VDDESD
	33	34	
GND	35	36	GND
	37	38	
N_CS_B3	39	40	GND
GIO_3	41	42	
GIO_4	43	44	SHTDN_N_TX_TOP_EXT
MCLK_SENSOR_B	45	46	3.3V_VDDESD
	47	48	
GND	49	50	GND
	51	52	
GND	53	54	GND
	55	56	
3.3V_VDDESD	57	58	3.3V_VDDESD
	59	60	
GND	61	62	GND
SENSORDATA_B7_P	63	64	SENSORDATA_B7_N
	65	66	
SENSORCLK_B2_P	67	68	SENSORCLK_B2_N
GND	69	70	GND
SENSORDATA_B6_P	71	72	SENSORDATA_B6_N
	73	74	
SENSORDATA_B5_P	75	76	SENSORDATA_B5_N
GND	77	78	GND
SENSORDATA_B4_P	79	80	SENSORDATA_B4_N
P3V3A	81	82	P3V3A
P3V3A	83	84	P3V3A
P3V3A	85	86	P3V3A
N_CS_B2	87	88	P3V3A
N_RESET_LOGIC_B	89	90	P3V3A
	91	92	
GND	93	94	GND
SENSORDATA_B3_P	95	96	SENSORDATA_B3_N
	97	98	
SENSORCLK_B1_P	99	100	SENSORCLK_B1_N
GND	101	102	GND
SENSORDATA_B2_P	103	104	SENSORDATA_B2_N
	105	106	
SENSORDATA_B1_P	107	108	SENSORDATA_B1_N
GND	109	110	GND
SENSORDATA_B0_P	111	112	SENSORDATA_B0_N
	113	114	
	115	116	
GND	117	118	GND
	119	120	
3.3V_VDDESD	121	122	3.3V_VDDESD
	123	124	
GND	125	126	GND
LOAD_PULSE_B1	127	128	TEST_MUX_BD
MISO_B	129	130	END_ADC_B1
MOSI_B	131	132	N_CS_B1
SCLK_B	133	134	SAMPLE_B
RESET_CVC_B	135	136	P3V3A
RESET_CDS_B	137	138	P3V3A
TEMP	139	140	P3V3A

8.6.3 Connector 3

Name	Pin No	Pin No	Name
N_RESET_LOGIC_C	1	2	TDI
TCK	3	4	TDO
GIO_5	5	6	TMS
GIO_6	7	8	TRST
SCLK_C	9	10	MISO_C
P3V3A	11	12	MOSI_C
P3V3A	13	14	P3V3A
P3V3A	15	16	P3V3A
	17	18	
GND	19	20	GND
	21	22	
GND	23	24	GND
SENSORDATA_C8_N	25	26	SENSORDATA_C8_P
3.3V_VDDESD	27	28	3.3V_VDDESD
SENSORDATA_C9_N	29	30	SENSORDATA_C9_P
	31	32	
SENSORDATA_C10_N	33	34	SENSORDATA_C10_P
GND	35	36	GND
SENSORCLK_C3_N	37	38	SENSORCLK_C3_P
GND	39	40	GND
SENSORDATA_C11_N	41	42	SENSORDATA_C11_P
	43	44	
	45	46	
3.3V_VDDESD	47	48	3.3V_VDDESD
	49	50	
GND	51	52	GND
N_CS_C3	53	54	MCLK_SENSOR_C
GND	55	56	GND
SENSORDATA_C4_N	57	58	SENSORDATA_C4_P
GND	59	60	GND
SENSORDATA_C5_N	61	62	SENSORDATA_C5_P
	63	64	
SENSORDATA_C6_N	65	66	SENSORDATA_C6_P
	67	68	
SENSORCLK_C2_N	69	70	SENSORCLK_C2_P
	71	72	
SENSORDATA_C7_N	73	74	SENSORDATA_C7_P
GND	75	76	GND
	77	78	
GND	79	80	GND
	81	82	
GND	83	84	GND
	85	86	
GND	87	88	GND
	89	90	
P3V3A	91	92	P3V3A
P3V3A	93	94	P3V3A
P3V3A	95	96	LOAD_PULSE_C2
P3V3A	97	98	N_CS_C2
	99	100	
GND	101	102	GND
	103	104	
3.3V_VDDESD	105	106	3.3V_VDDESD
No Net	107	108	
GND	109	110	GND
	111	112	
	113	114	
SENSORDATA_C0_N	115	116	SENSORDATA_C0_P
GND	117	118	GND
SENSORDATA_C1_N	119	120	SENSORDATA_C1_P
	121	122	
SENSORDATA_C2_N	123	124	SENSORDATA_C2_P
GND	125	126	GND
SENSORCLK_C1_N	127	128	SENSORCLK_C1_P
	129	130	
SENSORDATA_C3_N	131	132	SENSORDATA_C3_P
GND	133	134	GIO_7
P3V3A	135	136	GIO_8
P3V3A	137	138	GIO_9
P3V3A	139	140	GIO_10

8.6.4 Connector 4

Name	Pin No	Pin No	Name
GIO_11	1	2	N_RESET_LOGIC_D
GIO_12	3	4	GIO_15
GIO_13	5	6	GIO_16
GIO_14	7	8	GIO_17
MISO_D	9	10	SCLK_D
MOSI_D	11	12	P3V3A
P3V3A	13	14	P3V3A
P3V3A	15	16	P3V3A
	17	18	
GND	19	20	GND
	21	22	
GND	23	24	GND
SENSORDATA_D11_P	25	26	SENSORDATA_D11_N
3.3V_VDDESD	27	28	3.3V_VDDESD
SENSORCLK_D3_P	29	30	SENSORCLK_D3_N
	31	32	
SENSORDATA_D10_P	33	34	SENSORDATA_D10_N
GND	35	36	GND
SENSORDATA_D9_P	37	38	SENSORDATA_D9_N
GND	39	40	GND
SENSORDATA_D8_P	41	42	SENSORDATA_D8_N
	43	44	
	45	46	
3.3V_VDDESD	47	48	3.3V_VDDESD
	49	50	
GND	51	52	GND
MCLK_SENSOR_D	53	54	N_CS_D3
GND	55	56	GND
SENSORDATA_D7_P	57	58	SENSORDATA_D7_N
GND	59	60	GND
SENSORCLK_D2_P	61	62	SENSORCLK_D2_N
	63	64	
SENSORDATA_D6_P	65	66	SENSORDATA_D6_N
	67	68	
SENSORDATA_D5_P	69	70	SENSORDATA_D5_N
	71	72	
SENSORDATA_D4_P	73	74	SENSORDATA_D4_N
GND	75	76	GND
	77	78	
GND	79	80	GND
	81	82	
GND	83	84	GND
	85	86	
GND	87	88	GND
	89	90	
P3V3A	91	92	P3V3A
P3V3A	93	94	P3V3A
LOAD_PULSE_D2	95	96	P3V3A
N_CS_D2	97	98	P3V3A
	99	100	
GND	101	102	GND
	103	104	
3.3V_VDDESD	105	106	3.3V_VDDESD
	107	108	
GND	109	110	GND
	111	112	
	113	114	
SENSORDATA_D3_P	115	116	SENSORDATA_D3_N
GND	117	118	GND
SENSORCLK_D1_P	119	120	SENSORCLK_D1_N
	121	122	
SENSORDATA_D2_P	123	124	SENSORDATA_D2_N
GND	125	126	GND
SENSORDATA_D1_P	127	128	SENSORDATA_D1_N
	129	130	
SENSORDATA_D0_P	131	132	SENSORDATA_D0_N
GIO_18	133	134	GND
GIO_19	135	136	P3V3A
GIO_20	137	138	P3V3A
GIO_21	139	140	P3V3A

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