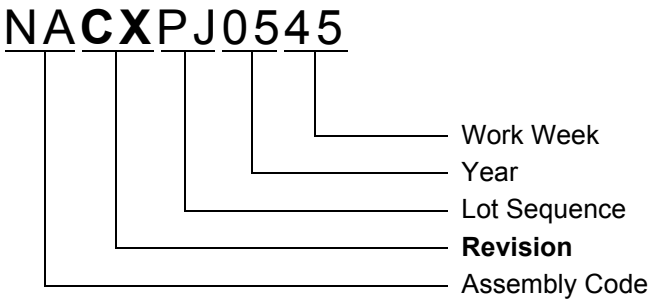
Errata: CS5466 - Silicon revision: C

Reference CS5466 Data Sheet revision DS659F1 dated AUG 2005.

Determining the Silicon Revision of the Integrated Circuit

On the front of the integrated circuit, directly under the part number, is an alpha-numeric line. For this device only, characters 3 and 4 in this line represent the silicon revision of the chip. For example, the following line indicates that the chip is a “C” revision device:



This Errata is applicable only to revision C of the chip.

Default State of FOUT

Description (revision B3)

Upon power-on the default state of the FOUT pin is high. The inactive state of FOUT is low. Therefore, after applying power, the FOUT pin would go high then go low (inactive state) after chip initialization.

Correction (revision C)

Upon power-on, FOUT pin is low and remains low after initialization is complete.

High Pass Filters (HPF)

Description (revision B3)

Input pin $\overline{\text{HPF}}$ defines the three options:

- High-pass Filter (HPF) is disabled when pin $\overline{\text{HPF}}$ is connected high.
- HPF is enabled in the voltage channel when pin $\overline{\text{HPF}}$ is connected low.
- HPF is enabled in the current channel when pin $\overline{\text{HPF}}$ is connected to pin FOUT.

Change (revision C)

High-pass Filter (HPF) is always enabled in the voltage channel.

Input pin $\overline{\text{HPF}}$ defines the two options:

- High-pass Filter (HPF) is disabled in the current channel when pin $\overline{\text{HPF}}$ is connected high.
- HPF is enabled in the current channel when pin $\overline{\text{HPF}}$ is connected low or when connected to FOUT.

Suppress False Indication on NEG Pin

Description (revision B3)

The NEG pin will toggle in the presence of AC line noise, falsely indicating negative active power.

Correction (revision C)

A threshold of +0.045% of full scale has been added to the NEG pin in order to suppress false negative active power indications caused by noise on the AC line.

Selecting Frequency of E1 and E2

Description (revision B3)

Frequency of Pulse out is determined as described in data sheet.

Change (revision C)

Frequency of Pulse out is determined as follows:

Frequency Select			Maximum Frequency for a Sine Wave *(Notes 1, 2)*			
FREQ2	**FREQ1**	**FREQ0**	**$\overline{E1}$ or $\overline{E2}$**	**$\overline{E1}$+$\overline{E2}$**	**FOUT**	
0	0	0	0.125 Hz	0.25 Hz	64x($\overline{E1}$+$\overline{E2}$)	16 Hz
0	0	1	0.25 Hz	0.5 Hz	32x($\overline{E1}$+$\overline{E2}$)	16 Hz
0	1	0	0.5Hz	1.0 Hz	16x($\overline{E1}$+$\overline{E2}$)	16 Hz
0	1	1	1.0 Hz	2.0 Hz	2048x($\overline{E1}$+$\overline{E2}$)	4,096 Hz
1	0	0	1.0 Hz	2.0 Hz	8x($\overline{E1}$+$\overline{E2}$)	16 Hz
1	0	1	0.25 Hz	0.5 Hz	64x($\overline{E1}$+$\overline{E2}$)	32 Hz
1	1	0	0.5 Hz	1.0 Hz	32x($\overline{E1}$+$\overline{E2}$)	32 Hz
1	1	1	1.0 Hz	2.0 Hz	16x($\overline{E1}$+$\overline{E2}$)	32 Hz

Notes: 1 A pure sinusoidal input with zero phase shift is applied to the voltage and current channel.
2 MCLK = 4.096 MHz

Table 1. Maximum Frequency for $\overline{E1}$, $\overline{E2}$, and FOUT

Frequency Select			Absolute Maximum Frequency *(Note 1)*	
FREQ2	**FREQ1**	**FREQ0**	**$\overline{E1}$ or $\overline{E2}$**	**$\overline{E1}$+$\overline{E2}$**
0	0	0	0.25 Hz	0.5 Hz
0	0	1	0.5Hz	1.0 Hz
0	1	0	1.0 Hz	2.0 Hz
0	1	1	2.0 Hz	4.0 Hz
1	0	0	2.0 Hz	4.0 Hz
1	0	1	0.5Hz	1.0 Hz
1	1	0	1.0 Hz	2.0 Hz
1	1	1	2.0 Hz	4.0 Hz

Notes: 1. MCLK = 4.096 MHz

Table 2. Absolute Maximum Frequency for $\overline{E1}$ and $\overline{E2}$