

# SPECIFICATION

SPEC. No. A-ESD-b

D A T E : 2014 May.

To

**Non-Controlled Copy**

CUSTOMER'S PRODUCT NAME

TDK PRODUCT NAME

MULTILAYER CERAMIC CHIP CAPACITORS

CGA Series / Automotive Grade

ESD Protection CGA3EA Series

Please return this specification to TDK representatives.

If orders are placed without returned specification, please allow us to judge that specification is accepted by your side.

## RECEIPT CONFIRMATION

DATE: \_\_\_\_\_ YEAR \_\_\_\_\_ MONTH \_\_\_\_\_ DAY \_\_\_\_\_

TDK Corporation  
Sales  
Electronic Components  
Sales & Marketing Group

TDK-EPC Corporation  
Engineering  
Ceramic Capacitors Business Group

APPROVED	Person in charge

APPROVED	CHECKED	Person in charge

1. SCOPE

This specification is applicable to chip type multilayer ceramic capacitors with a priority over the other relevant specifications.

Production places defined in this specification shall be TDK-EPC Corporation Japan, TDK (Suzhou) Co., Ltd and TDK Components U.S.A. Inc.

EXPLANATORY NOTE:

This specification warrants the quality of the ceramic chip capacitor. The chips should be evaluated or confirmed a state of mounted on your product.

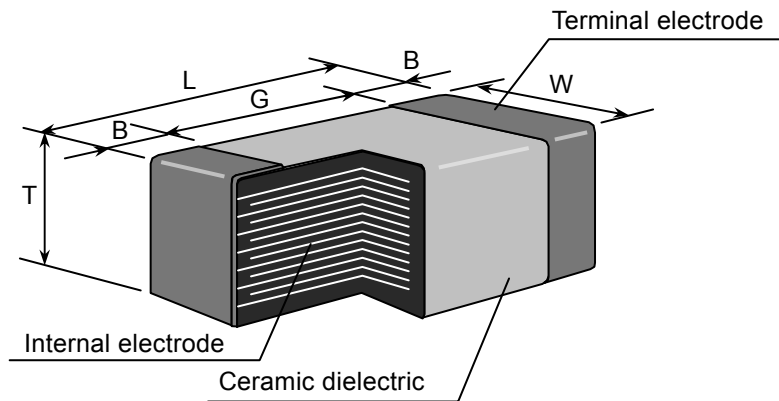
If the use of the chips go beyond the bounds of this specification, we can not afford to guarantee.

2. CODE CONSTRUCTION

(Example)

Catalog Number :	<u>CGA3</u>	<u>E</u>	<u>A</u>	<u>C0G</u>	<u>2 A</u>	<u>103</u>	<u>J</u>	<u>080</u>	<u>A</u>	<u>C</u>
(Web)	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)	(9)	(10)
Item Description :	<u>CGA3</u>	<u>E</u>	<u>A</u>	<u>C0G</u>	<u>2 A</u>	<u>103</u>	<u>J</u>	<u>T</u>	<u>xxxx</u>	
	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(11)	(12)	

(1) Type



Please refer to product list for the dimension of each product.

(2) Thickness

\* As for dimension tolerance, please contact with our sales representative.

Thickness	Dimension (mm)
E	0.80

(3) Identification for ESD capacitor

(Details are shown in table 1 No.16 at page 6)

Symbol	Identification
A	ESD Capacitor

(4) Temperature Characteristics (Details are shown in table 1 No.6 at page 3)

(5) Rated Voltage

Symbol	Rated Voltage
2 A	DC 100 V

(6) Rated Capacitance

Stated in three digits and in units of pico farads (pF).

The first and Second digits identify the first and second significant figures of the capacitance, the third digit identifies the multiplier.

Example 103 → 10,000pF

(7) Capacitance tolerance

Symbol	Tolerance
J	± 5 %

(8) Thickness code (Only Catalog Number)

(9) Package code (Only Catalog Number)

(10) Special code (Only Catalog Number)

(11) Packaging (Only Item Description)

(Bulk is not applicable for CGA1 and CGA2 type.)

Symbol	Packaging
B	Bulk
T	Taping

(12) Internal code (Only Item Description)

### 3. OPERATING TEMPERATURE RANGE

T.C.	Min. operating Temperature	Max. operating Temperature	Reference Temperature
C0G	-55°C	125°C	25°C
NP0	-55°C	150°C	25°C

### 4. STORING CONDITION AND TERM

5 to 40°C at 20 to 70%RH

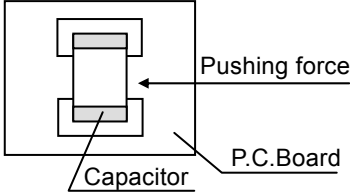
6 months Max.

### 5. INDUSTRIAL WASTE DISPOSAL

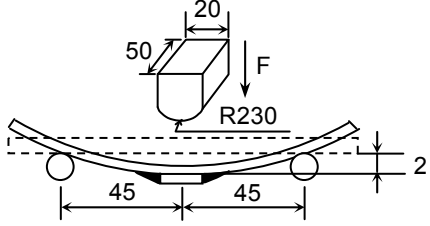
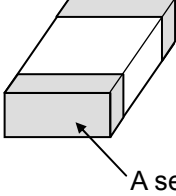
Dispose this product as industrial waste in accordance with the Industrial Waste Law.

6. PERFORMANCE

table 1

No.	Item	Performance	Test or inspection method								
1	External Appearance	No defects which may affect performance.	Inspect with magnifying glass (3×).								
2	Insulation Resistance	10,000MΩ min.	Apply rated voltage for 60s.								
3	Voltage Proof	Withstand test voltage without insulation breakdown or other damage.	3 times of rated voltage Above DC voltage shall be applied for 1 to 5s. Charge / discharge current shall not exceed 50mA.								
4	Capacitance	Within the specified tolerance.	<table border="1"> <thead> <tr> <th>Capacitance</th> <th>Measuring frequency</th> <th>Measuring voltage</th> </tr> </thead> <tbody> <tr> <td>1000pF and under</td> <td>1MHz±10%</td> <td rowspan="2">0.5-5Vrms.</td> </tr> <tr> <td>Over 1000pF</td> <td>1kHz±10%</td> </tr> </tbody> </table> <p>For information which product has which measuring voltage, please contact with our sales representative.</p>	Capacitance	Measuring frequency	Measuring voltage	1000pF and under	1MHz±10%	0.5-5Vrms.	Over 1000pF	1kHz±10%
Capacitance	Measuring frequency	Measuring voltage									
1000pF and under	1MHz±10%	0.5-5Vrms.									
Over 1000pF	1kHz±10%										
5	Q (Class1)	1,000 min.	See No.4 in this table for measuring condition.								
6	Temperature Characteristics of Capacitance (Class1)	<table border="1"> <thead> <tr> <th>T.C.</th> <th>Temperature Coefficient</th> </tr> </thead> <tbody> <tr> <td>C0G</td> <td>0 ± 30 (ppm/°C)</td> </tr> <tr> <td>NP0</td> <td>0 ± 30 (ppm/°C)</td> </tr> </tbody> </table> <p>Capacitance drift within ± 0.2% or ± 0.05pF, whichever larger.</p>	T.C.	Temperature Coefficient	C0G	0 ± 30 (ppm/°C)	NP0	0 ± 30 (ppm/°C)	<p>Temperature coefficient shall be calculated based on values at 25°C and 85°C temperature.</p> <p>Measuring temperature below 20°C shall be -10°C and -25°C.</p>		
T.C.	Temperature Coefficient										
C0G	0 ± 30 (ppm/°C)										
NP0	0 ± 30 (ppm/°C)										
7	Robustness of Terminations	No sign of termination coming off, breakage of ceramic, or other abnormal signs.	<p>Reflow solder the capacitors on a P.C.Board shown in Appendix 1a or Appendix 1b and apply a pushing force of 17.7N with 10±1s.</p>  <p>The diagram illustrates a capacitor mounted on a P.C. Board. A rectangular box represents the capacitor, with a smaller rectangle inside representing the ceramic core. An arrow labeled 'Pushing force' points to the right, indicating the direction of the applied force. The label 'P.C.Board' points to the board, and 'Capacitor' points to the capacitor assembly.</p>								

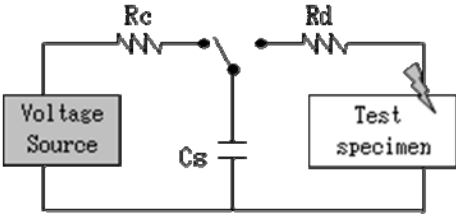
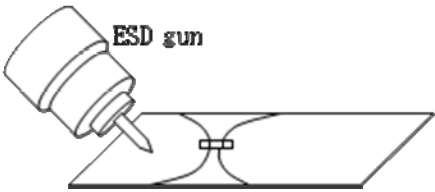
(continued)

No.	Item	Performance	Test or inspection method														
8	Bending	No mechanical damage.	Reflow solder the capacitors on a P.C.Board shown in Appendix 2a or Appendix 2b and bend it for 2mm.  <p style="text-align: right;">(Unit : mm)</p>														
9	Solderability	New solder to cover over 75% of termination. 25% may have pin holes or rough spots but not concentrated in one spot. Ceramic surface of A sections shall not be exposed due to melting or shifting of termination material.  <p style="text-align: center;">A section</p>	Completely soak both terminations in solder at $235\pm 5^{\circ}\text{C}$ for $2\pm 0.5\text{s}$ .  Solder : H63A (JIS Z 3282)  Flux : Isopropyl alcohol (JIS K 8839) Rosin (JIS K 5902) 25% solid solution.														
10	Resistance to solder heat	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td data-bbox="344 1115 518 1218">External appearance</td> <td data-bbox="518 1115 954 1218">No cracks are allowed and terminations shall be covered at least 60% with new solder.</td> </tr> <tr> <td data-bbox="344 1218 518 1420">Capacitance</td> <td data-bbox="518 1218 954 1420"> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th data-bbox="549 1256 719 1323">Characteristics</th> <th data-bbox="719 1256 954 1323">Change from the value before test</th> </tr> </thead> <tbody> <tr> <td data-bbox="549 1323 719 1384">COG NPO</td> <td data-bbox="719 1323 954 1384" style="text-align: center;"><math>\pm 2.5\%</math></td> </tr> </tbody> </table> </td> </tr> <tr> <td data-bbox="344 1420 518 1503">Q (Class1)</td> <td data-bbox="518 1420 954 1503">1,000 min.</td> </tr> <tr> <td data-bbox="344 1503 518 1585">Insulation Resistance</td> <td data-bbox="518 1503 954 1585">Meet the initial spec.</td> </tr> <tr> <td data-bbox="344 1585 518 1673">Voltage proof</td> <td data-bbox="518 1585 954 1673">No insulation breakdown or other damage.</td> </tr> </table>	External appearance	No cracks are allowed and terminations shall be covered at least 60% with new solder.	Capacitance	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th data-bbox="549 1256 719 1323">Characteristics</th> <th data-bbox="719 1256 954 1323">Change from the value before test</th> </tr> </thead> <tbody> <tr> <td data-bbox="549 1323 719 1384">COG NPO</td> <td data-bbox="719 1323 954 1384" style="text-align: center;"><math>\pm 2.5\%</math></td> </tr> </tbody> </table>	Characteristics	Change from the value before test	COG NPO	$\pm 2.5\%$	Q (Class1)	1,000 min.	Insulation Resistance	Meet the initial spec.	Voltage proof	No insulation breakdown or other damage.	Completely soak both terminations in solder at $260\pm 5^{\circ}\text{C}$ for $5\pm 1\text{s}$ .  Preheating condition Temp. : $150\pm 10^{\circ}\text{C}$ Time : 1 to 2min.  Flux : Isopropyl alcohol (JIS K 8839) Rosin (JIS K 5902) 25% solid solution.  Solder : H63A (JIS Z 3282)  Leave the capacitors in ambient condition for 6 to 24h (Class1) before measurement.
External appearance	No cracks are allowed and terminations shall be covered at least 60% with new solder.																
Capacitance	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th data-bbox="549 1256 719 1323">Characteristics</th> <th data-bbox="719 1256 954 1323">Change from the value before test</th> </tr> </thead> <tbody> <tr> <td data-bbox="549 1323 719 1384">COG NPO</td> <td data-bbox="719 1323 954 1384" style="text-align: center;"><math>\pm 2.5\%</math></td> </tr> </tbody> </table>	Characteristics	Change from the value before test	COG NPO	$\pm 2.5\%$												
Characteristics	Change from the value before test																
COG NPO	$\pm 2.5\%$																
Q (Class1)	1,000 min.																
Insulation Resistance	Meet the initial spec.																
Voltage proof	No insulation breakdown or other damage.																

(continued)

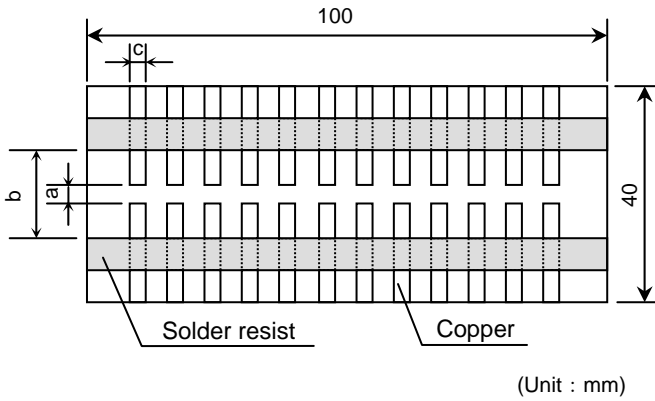
No.	Item	Performance	Test or inspection method																
11	Vibration	External appearance	No mechanical damage.																
		Capacitance	Characteristics	Change from the value before test															
			COG NPO	± 2.5%															
		Q (Class1)	1,000 min.	<p>Reflow solder the capacitors on a P.C.Board shown in Appendix1 before testing.</p> <p>Vibrate the capacitor with following conditions.</p> <p>Applied force : 5G max. Frequency : 10-2000Hz Duration : 20 min. Cycle : 12 cycles in each 3 mutually perpendicular directions.</p>															
12	Temperature cycle	External appearance	No mechanical damage.																
		Capacitance	Characteristics	Change from the value before test															
			COG NPO	± 2.5%															
		Q (Class1)	1,000 min.	<p>Reflow solder the capacitors on a P.C.Board shown in Appendix 1a or Appendix 1b before testing.</p> <p>Expose the capacitors in the condition step1 through step 4 and repeat 1,000 times consecutively.</p> <p>Leave the capacitors in ambient condition for 6 to 24h (Class 1) before measurement.</p>															
		Insulation Resistance	Meet the initial spec.	<table border="1"> <thead> <tr> <th>Step</th> <th>Temperature(°C)</th> <th>Time (min.)</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>Min. operating temp. ±3</td> <td>30 ± 3</td> </tr> <tr> <td>2</td> <td>Reference Temp. ±2</td> <td>2 - 5</td> </tr> <tr> <td>3</td> <td>Max. operating temp. ±2</td> <td>30 ± 2</td> </tr> <tr> <td>4</td> <td>Reference Temp. ±2</td> <td>2 - 5</td> </tr> </tbody> </table>	Step	Temperature(°C)	Time (min.)	1	Min. operating temp. ±3	30 ± 3	2	Reference Temp. ±2	2 - 5	3	Max. operating temp. ±2	30 ± 2	4	Reference Temp. ±2	2 - 5
		Step	Temperature(°C)	Time (min.)															
1	Min. operating temp. ±3	30 ± 3																	
2	Reference Temp. ±2	2 - 5																	
3	Max. operating temp. ±2	30 ± 2																	
4	Reference Temp. ±2	2 - 5																	
Voltage proof	No insulation breakdown or other damage.																		
13	Moisture Resistance (Steady State)	External appearance	No mechanical damage.																
		Capacitance	Characteristics	Change from the value before test															
			COG NPO	± 7.5%															
		Q (Class1)	350 min.	<p>Reflow solder the capacitors on a P.C.Board shown in Appendix 1a or Appendix 1b before testing.</p> <p>Leave at temperature 40±2°C, 90 to 95%RH for 500 +24,0h.</p> <p>Leave the capacitors in ambient condition for 6 to 24h (Class1) before measurement.</p>															
Insulation Resistance	1,000MΩ min.																		

(continued)

No.	Item	Performance	Test or inspection method							
14	Moisture Resistance	<p>No mechanical damage.</p> <table border="1" data-bbox="555 293 940 479"> <tr> <td data-bbox="555 331 730 398">Characteristics</td> <td data-bbox="730 331 940 398">Change from the value before test</td> </tr> <tr> <td data-bbox="555 398 730 479">COG NPO</td> <td data-bbox="730 398 940 479">± 7.5%</td> </tr> </table> <p>Q (Class1) 200 min.</p> <p>Insulation Resistance 500MΩ min.</p>	Characteristics	Change from the value before test	COG NPO	± 7.5%	<p>Reflow solder the capacitors on a P.C.Board shown in Appendix 1a or Appendix 1b before testing.</p> <p>Apply the rated voltage at temperature 85°C and 85%RH for 1000 +24,0h.</p> <p>Charge/discharge current shall not exceed 50mA.</p> <p>Leave the capacitors in ambient condition for 6 to 24h (Class1) before measurement</p>			
Characteristics	Change from the value before test									
COG NPO	± 7.5%									
15	Life	<p>No mechanical damage.</p> <table border="1" data-bbox="555 750 940 913"> <tr> <td data-bbox="555 788 730 855">Characteristics</td> <td data-bbox="730 788 940 855">Change from the value before test</td> </tr> <tr> <td data-bbox="555 855 730 913">COG NPO</td> <td data-bbox="730 855 940 913">± 7.5%</td> </tr> </table> <p>Q (Class1) 350 min.</p> <p>Insulation Resistance 1,000MΩ min.</p>	Characteristics	Change from the value before test	COG NPO	± 7.5%	<p>Reflow solder the capacitors on a P.C.Board shown in Appendix 1a or Appendix 1b before testing.</p> <p>Below the voltage shall be applied at maximum operating temperature ±2°C for 1,000 +48, 0h.</p> <table border="1" data-bbox="1042 913 1442 1048"> <tr> <td data-bbox="1042 913 1442 965">Applied voltage</td> </tr> <tr> <td data-bbox="1042 965 1442 1016">Rated voltage x2</td> </tr> <tr> <td data-bbox="1042 1016 1442 1048">Rated voltage x1</td> </tr> </table> <p>For information which product has which applied voltage, please contact with our sales representative.</p> <p>Charge/discharge current shall not exceed 50mA.</p> <p>Leave the capacitors in ambient condition for 6 to 24h (Class1) before measurement.</p>	Applied voltage	Rated voltage x2	Rated voltage x1
Characteristics	Change from the value before test									
COG NPO	± 7.5%									
Applied voltage										
Rated voltage x2										
Rated voltage x1										
16	ESD	<p>Withstand ESD voltage without insulation breakdown.</p>  <p>Rc : Charge current limit resistor Rd : Discharge resistor Cs : Energy storage capacitor</p> 	<p>Solder the capacitors on a P.C.Board shown in Appendix3 before testing.</p> <p>Circuit condition : IEC 61000-4-2 ( Cs : 150pF / Rd : 330Ω )</p> <p>Test method : Direct contact Number of ESD pulse : ± 10 times</p> <p>As for applied ESD level, please refer to the table A in the end of the specification.</p> <p>After each ESD pulse, dissipation of residual charge shall be done with applying 1MΩ resistance for 1 sec min.</p>							

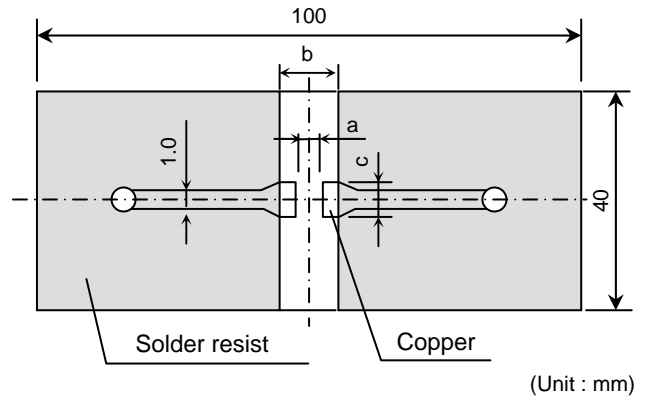
### Appendix - 1

#### P.C. Board for reliability test



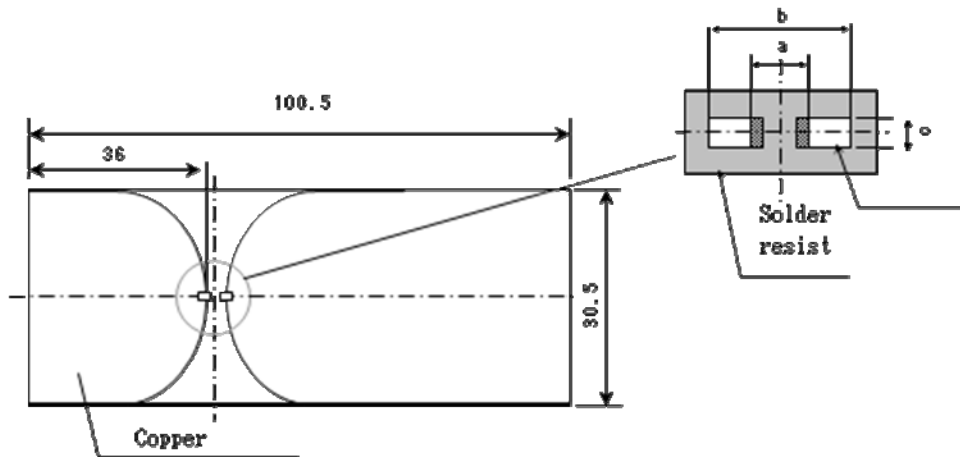
### Appendix - 2

#### P.C. Board for bending test



### Appendix - 3

#### P.C. Board for ESD test



Material : Glass Epoxy ( As per JIS C6484 GE4 )

P.C. Board thickness : Appendix-1, 2, 3 1.6mm

- Copper ( thickness 0.035mm )
- Solder resist

#### Appendix 1, 2

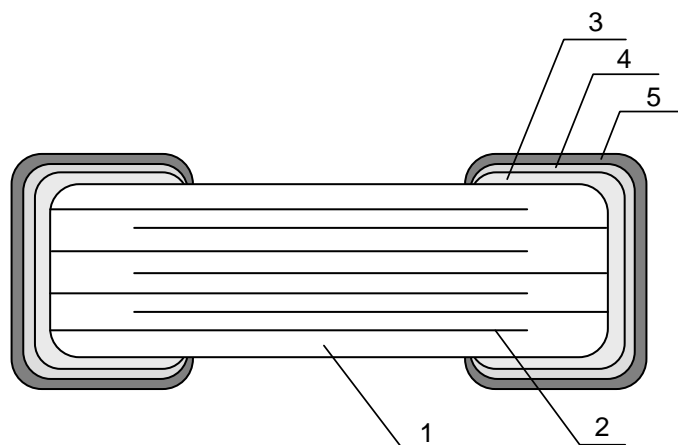
TDK (EIA style)	Dimensions (mm)		
	a	b	c
CGA3 (CC0603)	1.0	3.0	1.2

#### Appendix 3

TDK (EIA style)	Dimensions (mm)		
	a	b	c
CGA3 (CC0603)	1.0	3.0	0.75

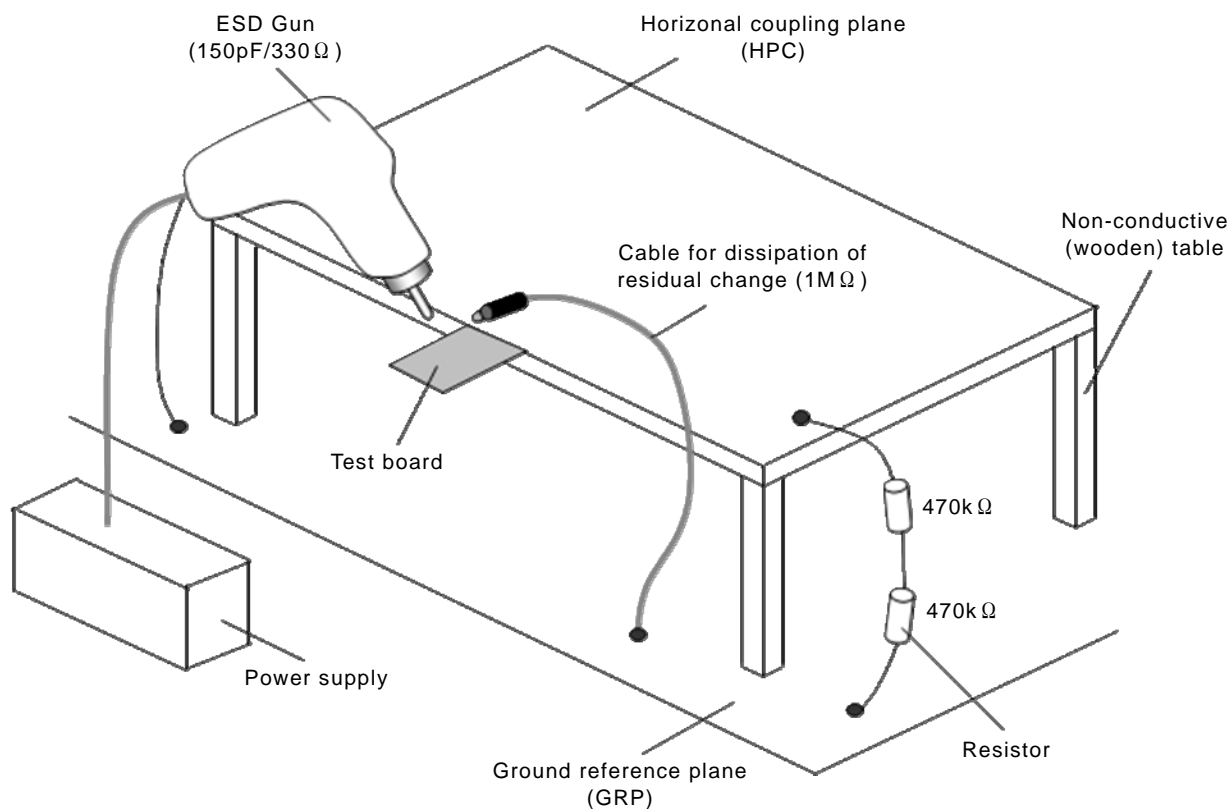


## 7. INSIDE STRUCTURE AND MATERIAL

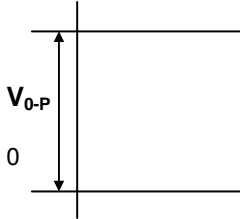
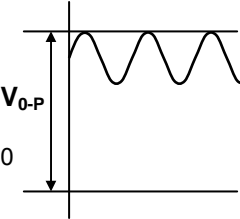
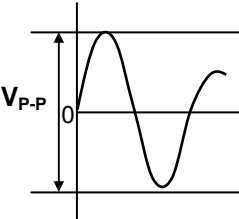
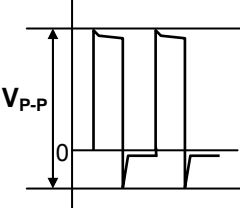
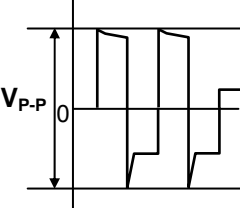
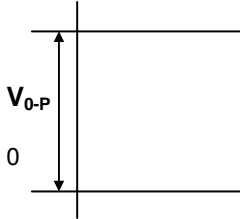
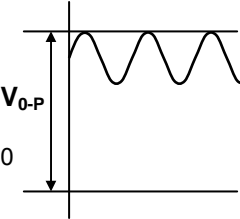
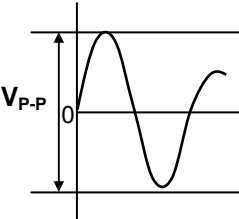
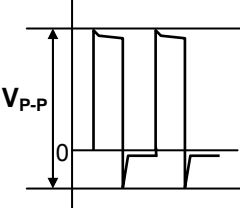
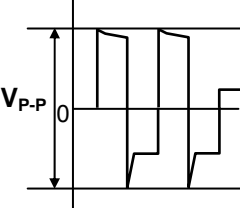
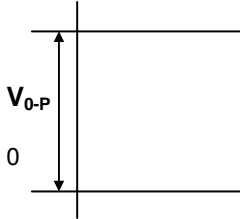
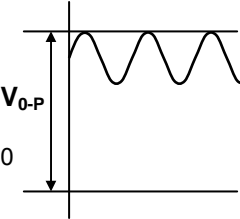
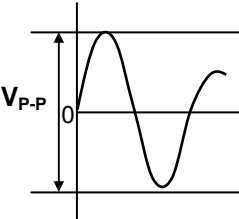
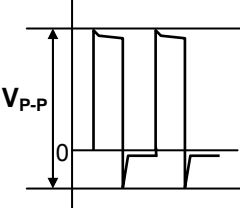
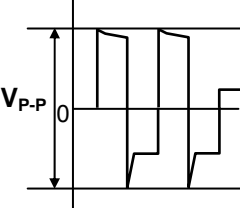


No.	NAME	MATERIAL
1	Dielectric	CaZrO <sub>3</sub>
2	Electrode	Nickel (Ni)
3	Termination	Copper (Cu)
4		Nickel (Ni)
5		Tin (Sn)

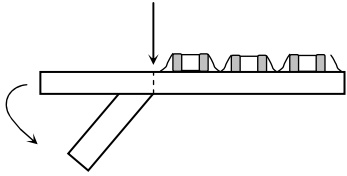
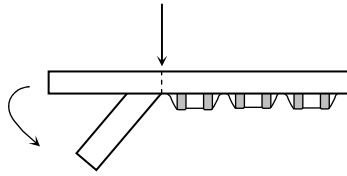
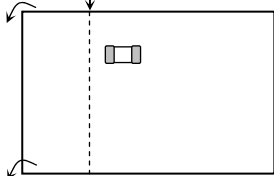
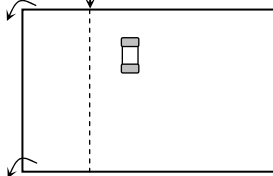
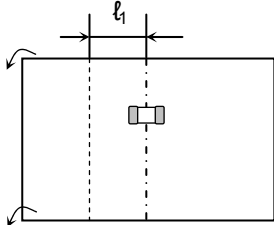
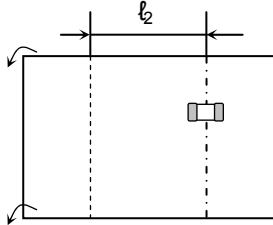
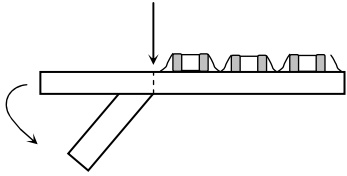
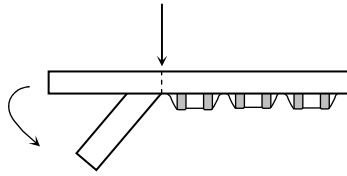
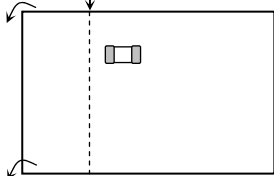
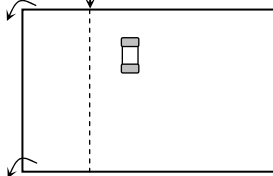
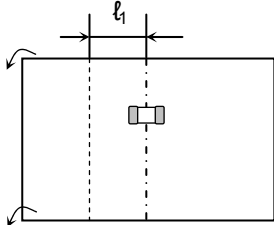
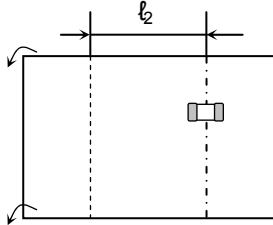
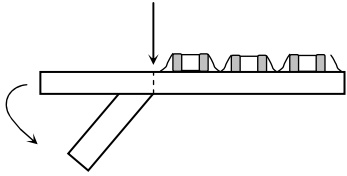
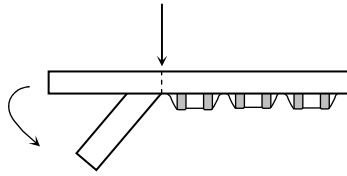
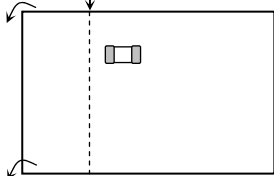
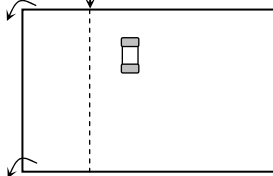
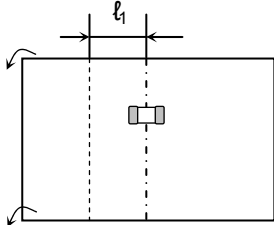
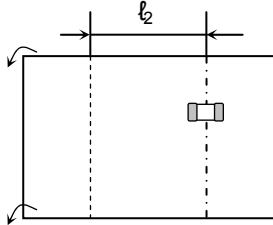
## 8. Setting up for ESD test

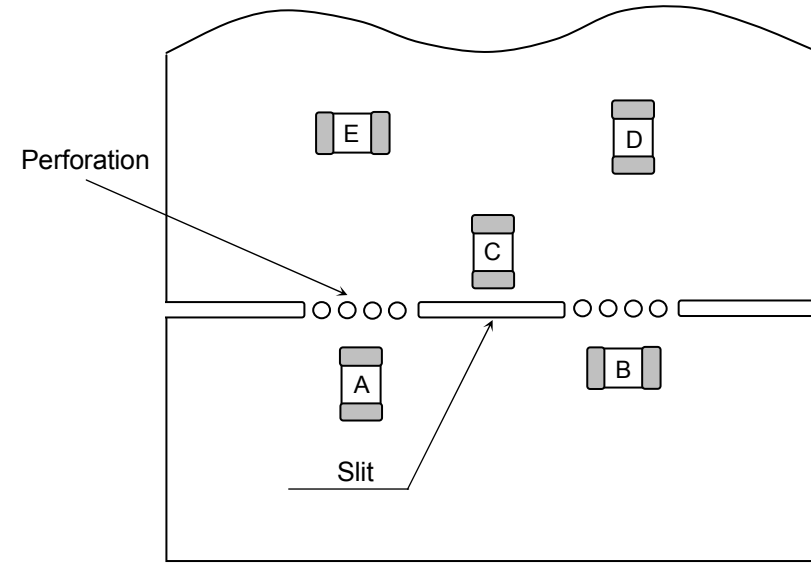
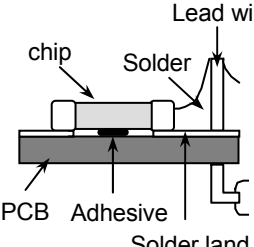
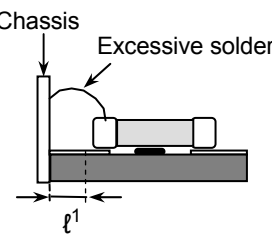
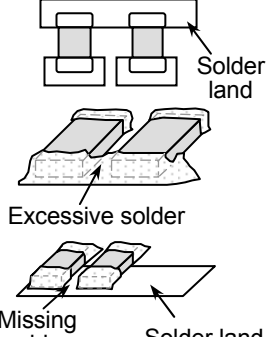
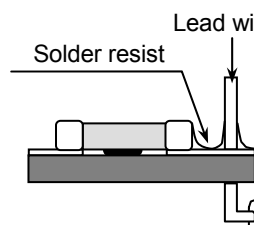
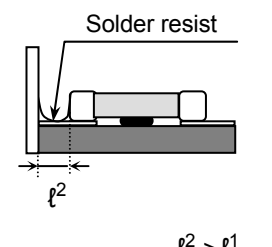
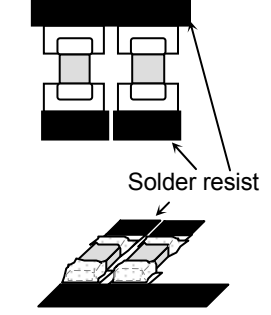
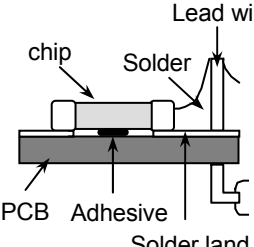
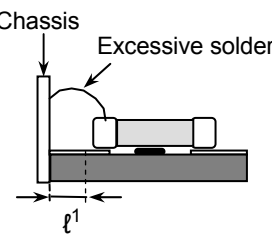
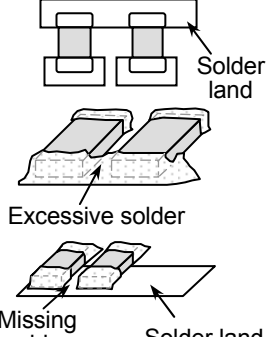
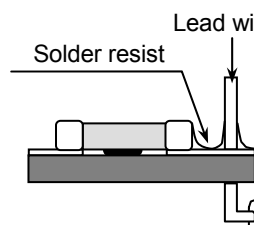
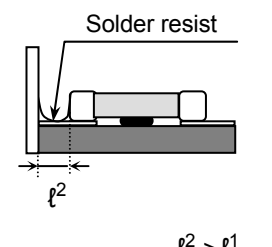
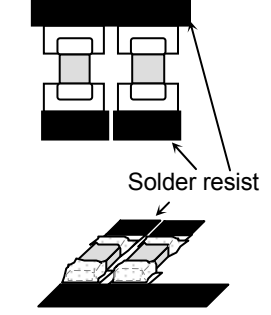
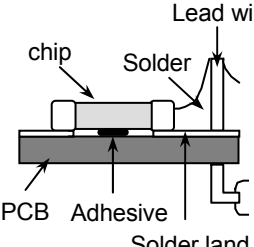
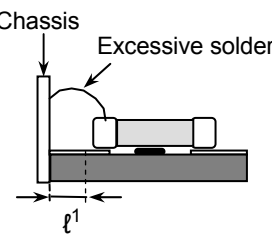
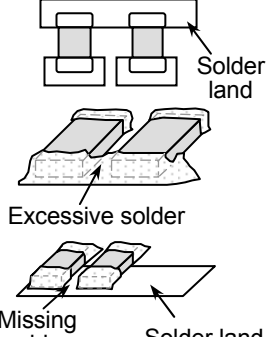
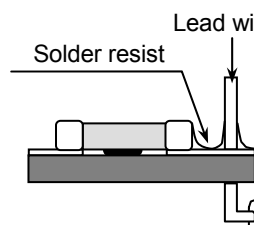
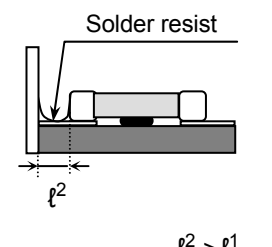
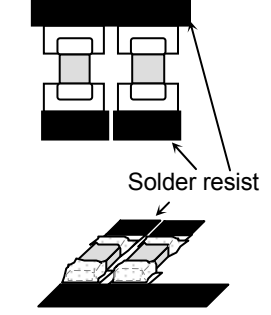


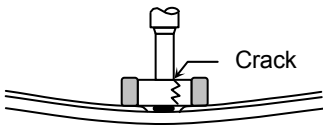
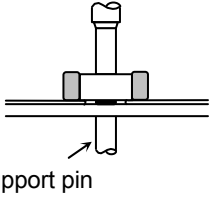
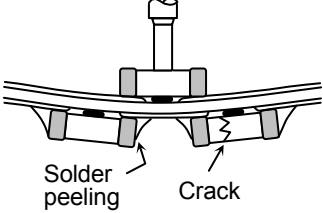
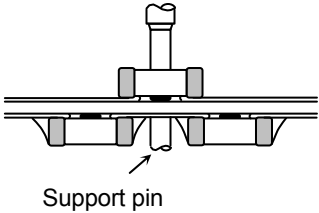
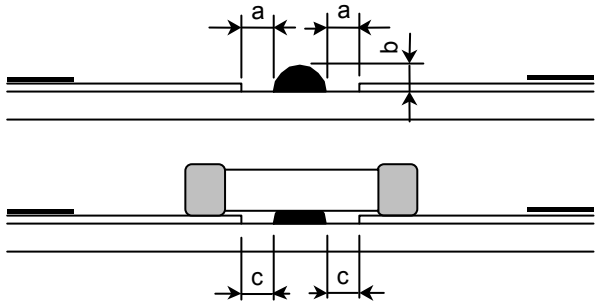
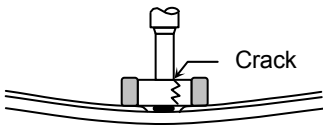
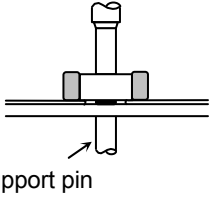
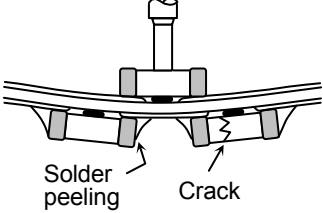
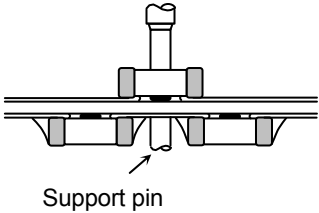
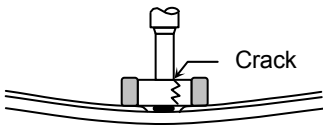
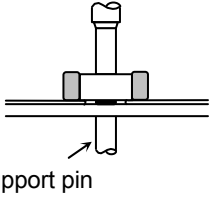
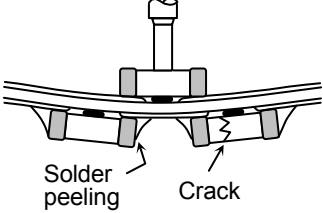
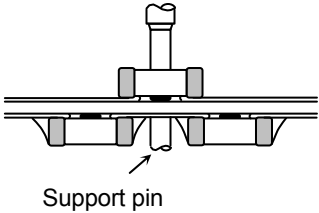
## 9. Caution

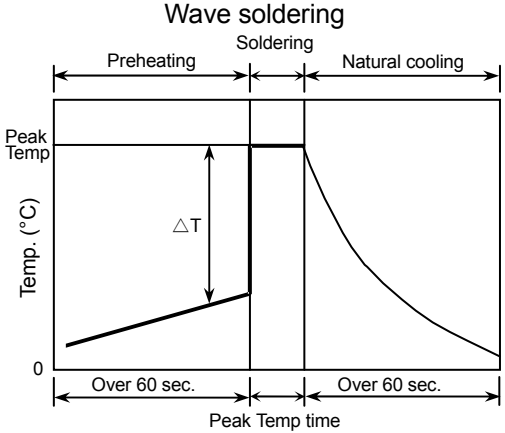
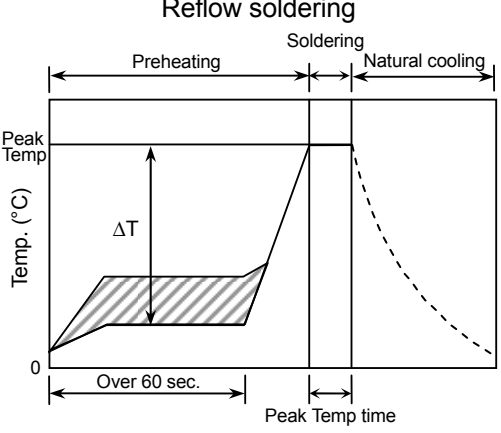
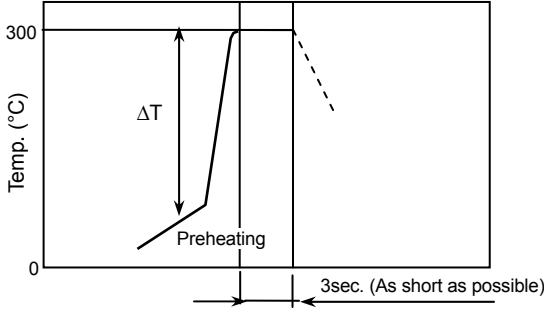
No.	Process	Condition														
1	Operating Condition (Storage, Transportation)	<p>1-1. Storage</p> <ol style="list-style-type: none"> <li>1) The capacitors must be stored in an ambient temperature of 5 to 40°C with a relative humidity of 20 to 70%RH. The products should be used within 6 months upon receipt.</li> <li>2) The capacitors must be operated and stored in an environment free of dew condensation and these gases such as Hydrogen Sulphide, Hydrogen Sulphate, Chlorine, Ammonia and sulfur.</li> <li>3) Avoid storing in sun light and falling of dew.</li> <li>4) Do not use capacitors under high humidity and high and low atmospheric pressure which may affect capacitors reliability.</li> <li>5) Capacitors should be tested for the solderability when they are stored for long time.</li> </ol> <p>1-2. Handling in transportation</p> <p>In case of the transportation of the capacitors, the performance of the capacitors may be deteriorated depending on the transportation condition. (Refer to JEITA RCR-2335B 9.2 Handling in transportation)</p>														
2	Circuit design ⚠ Caution	<p>2-1. Operating temperature</p> <p>Operating temperature should be followed strictly within this specification, especially be careful with maximum temperature.</p> <ol style="list-style-type: none"> <li>1) Do not use capacitors above the maximum allowable operating temperature.</li> <li>2) Surface temperature including self heating should be below maximum operating temperature. (Due to dielectric loss, capacitors will heat itself when AC is applied. Especially at high frequencies around its SRF, the heat might be so extreme that it may damage itself or the product mounted on. Please design the circuit so that the maximum temperature of the capacitors including the self heating to be below the maximum allowable operating temperature. Temperature rise at capacitor surface shall be below 20°C)</li> <li>3) The electrical characteristics of the capacitors will vary depending on the temperature. The capacitors should be selected and designed in taking the temperature into consideration.</li> </ol> <p>2-2. Operating voltage</p> <ol style="list-style-type: none"> <li>1) Operating voltage across the terminals should be below the rated voltage. When AC and DC are super imposed, <math>V_{0-P}</math> must be below the rated voltage. _____ (1) and (2) AC or pulse with overshooting, <math>V_{P-P}</math> must be below the rated voltage. _____ (3), (4) and (5) When the voltage is started to apply to the circuit or it is stopped applying, the irregular voltage may be generated for a transit period because of resonance or switching. Be sure to use the capacitors within rated voltage containing these Irregular voltage.</li> </ol> <table border="1" data-bbox="472 1451 1445 1727"> <thead> <tr> <th data-bbox="472 1451 660 1496">Voltage</th> <th data-bbox="660 1451 922 1496">(1) DC voltage</th> <th data-bbox="922 1451 1184 1496">(2) DC+AC voltage</th> <th data-bbox="1184 1451 1445 1496">(3) AC voltage</th> </tr> </thead> <tbody> <tr> <td data-bbox="472 1496 660 1727">Positional Measurement (Rated voltage)</td> <td data-bbox="660 1496 922 1727">  </td> <td data-bbox="922 1496 1184 1727">  </td> <td data-bbox="1184 1496 1445 1727">  </td> </tr> </tbody> </table> <table border="1" data-bbox="472 1753 1445 2018"> <thead> <tr> <th data-bbox="472 1753 660 1798">Voltage</th> <th data-bbox="660 1753 922 1798">(4) Pulse voltage (A)</th> <th data-bbox="922 1753 1445 1798">(5) Pulse voltage (B)</th> </tr> </thead> <tbody> <tr> <td data-bbox="472 1798 660 2018">Positional Measurement (Rated voltage)</td> <td data-bbox="660 1798 922 2018">  </td> <td data-bbox="922 1798 1445 2018">  </td> </tr> </tbody> </table>	Voltage	(1) DC voltage	(2) DC+AC voltage	(3) AC voltage	Positional Measurement (Rated voltage)				Voltage	(4) Pulse voltage (A)	(5) Pulse voltage (B)	Positional Measurement (Rated voltage)		
Voltage	(1) DC voltage	(2) DC+AC voltage	(3) AC voltage													
Positional Measurement (Rated voltage)																
Voltage	(4) Pulse voltage (A)	(5) Pulse voltage (B)														
Positional Measurement (Rated voltage)																

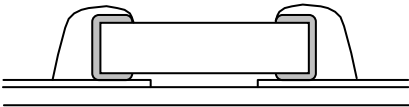

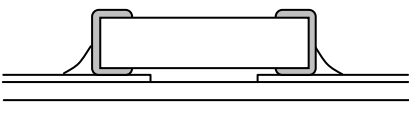
No.	Process	Condition																
2	Circuit design ⚠ Caution	<p>2) Even below the rated voltage, if repetitive high frequency AC or pulse is applied, the reliability of the capacitors may be reduced.</p> <p>3) The effective capacitance will vary depending on applied DC and AC voltages. The capacitors should be selected and designed in taking the voltages into consideration.</p> <p>2-3. Frequency When the capacitors (Class 2) are used in AC and/or pulse voltages, the capacitors may vibrate themselves and generate audible sound.</p>																
3	Designing P.C.board	<p>The amount of solder at the terminations has a direct effect on the reliability of the capacitors.</p> <p>1) The greater the amount of solder, the higher the stress on the chip capacitors, and the more likely that it will break. When designing a P.C.board, determine the shape and size of the solder lands to have proper amount of solder on the terminations.</p> <p>2) Avoid using common solder land for multiple terminations and provide individual solder land for each terminations.</p> <p>3) Size and recommended land dimensions.</p> <div data-bbox="667 846 1380 1131" data-label="Diagram"> <p>The diagram shows a cross-section of a chip capacitor mounted on a PCB. Dimension A is the length of the capacitor body. Dimension B is the length of the solder land on the capacitor side. Dimension C is the height of the solder land. Labels include 'Chip capacitors', 'Solder land', and 'Solder resist'.</p> </div> <table border="1" data-bbox="497 1182 1045 1438"> <caption>Flow soldering (mm)</caption> <thead> <tr> <th>Type</th> <th>CGA3 (CC0603)</th> </tr> </thead> <tbody> <tr> <td>A</td> <td>0.7 - 1.0</td> </tr> <tr> <td>B</td> <td>0.8 - 1.0</td> </tr> <tr> <td>C</td> <td>0.6 - 0.8</td> </tr> </tbody> </table> <table border="1" data-bbox="497 1482 1045 1729"> <caption>Reflow soldering (mm)</caption> <thead> <tr> <th>Type</th> <th>CGA3 (CC0603)</th> </tr> </thead> <tbody> <tr> <td>A</td> <td>0.6 - 0.8</td> </tr> <tr> <td>B</td> <td>0.6 - 0.8</td> </tr> <tr> <td>C</td> <td>0.6 - 0.8</td> </tr> </tbody> </table>	Type	CGA3 (CC0603)	A	0.7 - 1.0	B	0.8 - 1.0	C	0.6 - 0.8	Type	CGA3 (CC0603)	A	0.6 - 0.8	B	0.6 - 0.8	C	0.6 - 0.8
Type	CGA3 (CC0603)																	
A	0.7 - 1.0																	
B	0.8 - 1.0																	
C	0.6 - 0.8																	
Type	CGA3 (CC0603)																	
A	0.6 - 0.8																	
B	0.6 - 0.8																	
C	0.6 - 0.8																	

No.	Process	Condition												
3	Designing P.C.board	<p data-bbox="437 192 1098 226">4) Recommended chip capacitors layout is as following.</p> <table border="1" data-bbox="475 259 1430 1682"> <thead> <tr> <th data-bbox="475 259 660 342"></th> <th data-bbox="660 259 1043 342">Disadvantage against bending stress</th> <th data-bbox="1043 259 1430 342">Advantage against bending stress</th> </tr> </thead> <tbody> <tr> <td data-bbox="475 342 660 757">Mounting face</td> <td data-bbox="660 342 1043 757"> <p data-bbox="751 387 954 421">Perforation or slit</p>  <p data-bbox="699 645 948 712">Break P.C.board with mounted side up.</p> </td> <td data-bbox="1043 342 1430 757"> <p data-bbox="1134 387 1337 421">Perforation or slit</p>  <p data-bbox="1091 645 1340 712">Break P.C.board with mounted side down.</p> </td> </tr> <tr> <td data-bbox="475 757 660 1205">Chip arrangement (Direction)</td> <td data-bbox="660 757 1043 1205"> <p data-bbox="751 880 954 913">Perforation or slit</p>  </td> <td data-bbox="1043 757 1430 1205"> <p data-bbox="1134 880 1337 913">Perforation or slit</p>  </td> </tr> <tr> <td data-bbox="475 1205 660 1682">Distance from slit</td> <td data-bbox="660 1205 1043 1682"> <p data-bbox="671 1216 1007 1249">Closer to slit is higher stress</p>  <p data-bbox="922 1585 1007 1619"><math>(l_1 &lt; l_2)</math></p> </td> <td data-bbox="1043 1205 1430 1682"> <p data-bbox="1054 1216 1390 1249">Away from slit is less stress</p>  <p data-bbox="1310 1585 1394 1619"><math>(l_1 &lt; l_2)</math></p> </td> </tr> </tbody> </table>		Disadvantage against bending stress	Advantage against bending stress	Mounting face	<p data-bbox="751 387 954 421">Perforation or slit</p>  <p data-bbox="699 645 948 712">Break P.C.board with mounted side up.</p>	<p data-bbox="1134 387 1337 421">Perforation or slit</p>  <p data-bbox="1091 645 1340 712">Break P.C.board with mounted side down.</p>	Chip arrangement (Direction)	<p data-bbox="751 880 954 913">Perforation or slit</p> 	<p data-bbox="1134 880 1337 913">Perforation or slit</p> 	Distance from slit	<p data-bbox="671 1216 1007 1249">Closer to slit is higher stress</p>  <p data-bbox="922 1585 1007 1619"><math>(l_1 &lt; l_2)</math></p>	<p data-bbox="1054 1216 1390 1249">Away from slit is less stress</p>  <p data-bbox="1310 1585 1394 1619"><math>(l_1 &lt; l_2)</math></p>
	Disadvantage against bending stress	Advantage against bending stress												
Mounting face	<p data-bbox="751 387 954 421">Perforation or slit</p>  <p data-bbox="699 645 948 712">Break P.C.board with mounted side up.</p>	<p data-bbox="1134 387 1337 421">Perforation or slit</p>  <p data-bbox="1091 645 1340 712">Break P.C.board with mounted side down.</p>												
Chip arrangement (Direction)	<p data-bbox="751 880 954 913">Perforation or slit</p> 	<p data-bbox="1134 880 1337 913">Perforation or slit</p> 												
Distance from slit	<p data-bbox="671 1216 1007 1249">Closer to slit is higher stress</p>  <p data-bbox="922 1585 1007 1619"><math>(l_1 &lt; l_2)</math></p>	<p data-bbox="1054 1216 1390 1249">Away from slit is less stress</p>  <p data-bbox="1310 1585 1394 1619"><math>(l_1 &lt; l_2)</math></p>												

No.	Process	Condition												
3	Designing P.C.board	<p>5) Mechanical stress varies according to location of chip capacitors on the P.C.board.</p>  <p>The stress in capacitors is in the following order.  <math>A &gt; B = C &gt; D &gt; E</math></p> <p>6) Layout recommendation</p> <table border="1" data-bbox="379 1008 1481 1921"> <thead> <tr> <th data-bbox="379 1008 539 1124">Example</th> <th data-bbox="539 1008 842 1124">Use of common solder land</th> <th data-bbox="842 1008 1152 1124">Soldering with chassis</th> <th data-bbox="1152 1008 1481 1124">Use of common solder land with other SMD</th> </tr> </thead> <tbody> <tr> <td data-bbox="379 1124 539 1505">Need to avoid</td> <td data-bbox="539 1124 842 1505">  </td> <td data-bbox="842 1124 1152 1505">  </td> <td data-bbox="1152 1124 1481 1505">  </td> </tr> <tr> <td data-bbox="379 1505 539 1921">Recommendation</td> <td data-bbox="539 1505 842 1921">  </td> <td data-bbox="842 1505 1152 1921">  </td> <td data-bbox="1152 1505 1481 1921">  </td> </tr> </tbody> </table>	Example	Use of common solder land	Soldering with chassis	Use of common solder land with other SMD	Need to avoid				Recommendation			
Example	Use of common solder land	Soldering with chassis	Use of common solder land with other SMD											
Need to avoid														
Recommendation														


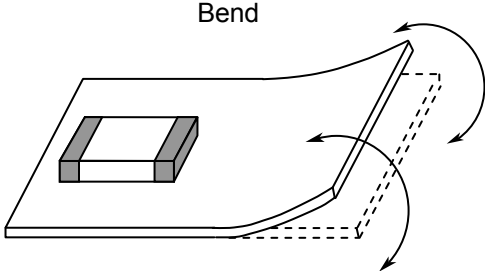
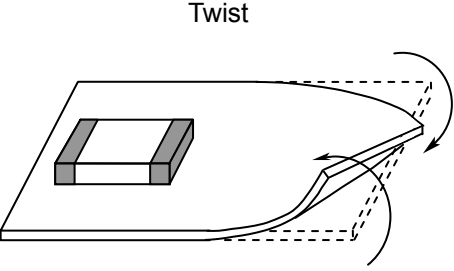
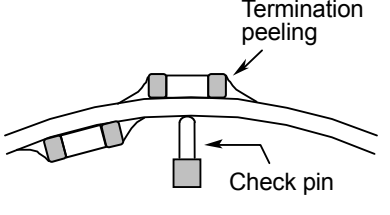
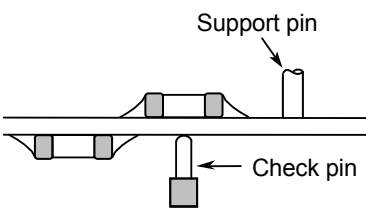
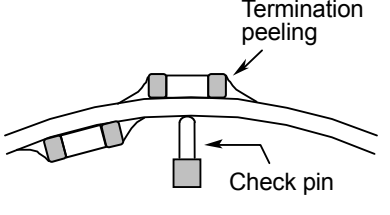
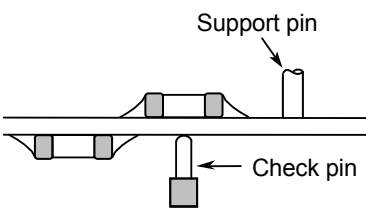
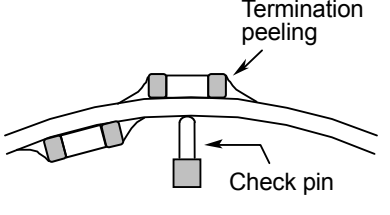
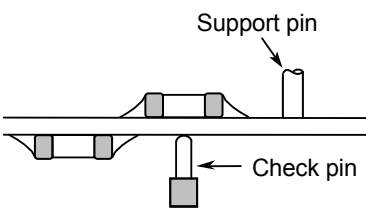
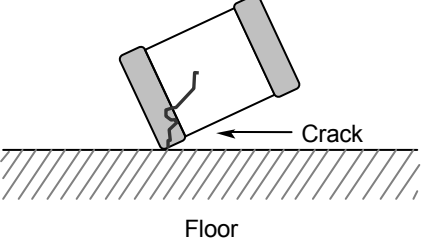
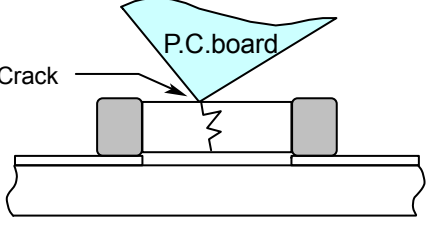
No.	Process	Condition									
4	Mounting	<p>4-1. Stress from mounting head</p> <p>If the mounting head is adjusted too low, it may induce excessive stress in the chip capacitors to result in cracking. Please take following precautions.</p> <ol style="list-style-type: none"> <li>1) Adjust the bottom dead center of the mounting head to reach on the P.C.board surface and not press it.</li> <li>2) Adjust the mounting head pressure to be 1 to 3N of static weight.</li> <li>3) To minimize the impact energy from mounting head, it is important to provide support from the bottom side of the P.C.board.</li> </ol> <p>See following examples.</p> <table border="1" data-bbox="480 600 1433 1173"> <thead> <tr> <th></th> <th data-bbox="667 600 1059 647">Not recommended</th> <th data-bbox="1059 600 1433 647">Recommended</th> </tr> </thead> <tbody> <tr> <td data-bbox="480 647 667 896">Single sided mounting</td> <td data-bbox="667 647 1059 896">  </td> <td data-bbox="1059 647 1433 896">  </td> </tr> <tr> <td data-bbox="480 896 667 1173">Double-sides mounting</td> <td data-bbox="667 896 1059 1173">  </td> <td data-bbox="1059 896 1433 1173">  </td> </tr> </tbody> </table> <p>When the centering jaw is worn out, it may give mechanical impact on the capacitors to cause crack. Please control the close up dimension of the centering jaw and provide sufficient preventive maintenance and replacement of it.</p> <p>4-2. Amount of adhesive</p> 		Not recommended	Recommended	Single sided mounting			Double-sides mounting		
	Not recommended	Recommended									
Single sided mounting											
Double-sides mounting											


No.	Process	Condition																								
5	Soldering	<p>5-1. Flux selection</p> <p>Although highly-activated flux gives better solderability, substances which increase activity may also degrade the insulation of the chip capacitors. To avoid such degradation, it is recommended following.</p> <ol style="list-style-type: none"> <li>1) It is recommended to use a mildly activated rosin flux (less than 0.1wt% chlorine). Strong flux is not recommended.</li> <li>2) Excessive flux must be avoided. Please provide proper amount of flux.</li> <li>3) When water-soluble flux is used, enough washing is necessary.</li> </ol> <p>5-2. Recommended soldering profile by various methods</p> <div style="display: flex; justify-content: space-around;"> <div style="text-align: center;"> <p>Wave soldering</p>  </div> <div style="text-align: center;"> <p>Reflow soldering</p>  </div> </div> <div style="text-align: center; margin-top: 20px;"> <p>Manual soldering (Solder iron)</p>  </div> <p>5-3. Recommended soldering peak temp and peak temp duration</p> <table border="1" style="width: 100%; border-collapse: collapse; text-align: center;"> <thead> <tr> <th rowspan="2" style="text-align: left;">Temp./Duration</th> <th colspan="2">Wave soldering</th> <th colspan="2">Reflow soldering</th> </tr> <tr> <th>Peak temp(°C)</th> <th>Duration(sec.)</th> <th>Peak temp(°C)</th> <th>Duration(sec.)</th> </tr> </thead> <tbody> <tr> <td style="text-align: left;">Solder</td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td style="text-align: left;">Pb-Sn Solder</td> <td>250 max.</td> <td>3 max.</td> <td>230 max.</td> <td>20 max.</td> </tr> <tr> <td style="text-align: left;">Lead Free Solder</td> <td>260 max.</td> <td>5 max.</td> <td>260 max.</td> <td>10 max.</td> </tr> </tbody> </table> <p>Recommended solder compositions  Sn-37Pb (Pb-Sn solder)  Sn-3.0Ag-0.5Cu (Lead Free Solder)</p>	Temp./Duration	Wave soldering		Reflow soldering		Peak temp(°C)	Duration(sec.)	Peak temp(°C)	Duration(sec.)	Solder					Pb-Sn Solder	250 max.	3 max.	230 max.	20 max.	Lead Free Solder	260 max.	5 max.	260 max.	10 max.
Temp./Duration	Wave soldering			Reflow soldering																						
	Peak temp(°C)	Duration(sec.)	Peak temp(°C)	Duration(sec.)																						
Solder																										
Pb-Sn Solder	250 max.	3 max.	230 max.	20 max.																						
Lead Free Solder	260 max.	5 max.	260 max.	10 max.																						

No.	Process	Condition												
5	Soldering	<p>5-4. Avoiding thermal shock</p> <p>1) Preheating condition</p> <table border="1" data-bbox="555 264 1428 434"> <thead> <tr> <th data-bbox="555 264 826 309">Soldering</th> <th data-bbox="826 264 1169 309">Type</th> <th data-bbox="1169 264 1428 309">Temp. (°C)</th> </tr> </thead> <tbody> <tr> <td data-bbox="555 309 826 344">Wave soldering</td> <td data-bbox="826 309 1169 344">CGA3(CC0603)</td> <td data-bbox="1169 309 1428 344"><math>\Delta T \leq 150</math></td> </tr> <tr> <td data-bbox="555 344 826 383">Reflow soldering</td> <td data-bbox="826 344 1169 383">CGA3(CC0603)</td> <td data-bbox="1169 344 1428 383"><math>\Delta T \leq 150</math></td> </tr> <tr> <td data-bbox="555 383 826 434">Manual soldering</td> <td data-bbox="826 383 1169 434">CGA3(CC0603)</td> <td data-bbox="1169 383 1428 434"><math>\Delta T \leq 150</math></td> </tr> </tbody> </table> <p>2) Cooling condition Natural cooling using air is recommended. If the chips are dipped into a solvent for cleaning, the temperature difference (<math>\Delta T</math>) must be less than 100°C.</p> <p>5-5. Amount of solder</p> <p>Excessive solder will induce higher tensile force in chip capacitors when temperature changes and it may result in chip cracking. In sufficient solder may detach the capacitors from the P.C.board.</p> <div data-bbox="507 846 1428 952"> <p>Excessive solder  Higher tensile force in chip capacitors to cause crack</p> </div> <hr/> <div data-bbox="507 1008 1276 1120"> <p>Adequate  Maximum amount Minimum amount</p> </div> <hr/> <div data-bbox="507 1176 1428 1310"> <p>Insufficient solder  Low robustness may cause contact failure or chip capacitors come off the P.C.board.</p> </div> <hr/> <p>5-6. Solder repair by solder iron</p> <p>1) Selection of the soldering iron tip Tip temperature of solder iron varies by its type, P.C.board material and solder land size. The higher the tip temperature, the quicker the operation. However, heat shock may cause a crack in the chip capacitors. Please make sure the tip temp. before soldering and keep the peak temp and time in accordance with following recommended condition. (Please preheat the chip capacitors with the condition in 5-4 to avoid the thermal shock.)</p>	Soldering	Type	Temp. (°C)	Wave soldering	CGA3(CC0603)	$\Delta T \leq 150$	Reflow soldering	CGA3(CC0603)	$\Delta T \leq 150$	Manual soldering	CGA3(CC0603)	$\Delta T \leq 150$
Soldering	Type	Temp. (°C)												
Wave soldering	CGA3(CC0603)	$\Delta T \leq 150$												
Reflow soldering	CGA3(CC0603)	$\Delta T \leq 150$												
Manual soldering	CGA3(CC0603)	$\Delta T \leq 150$												



No.	Process	Condition								
5	Soldering	<p style="text-align: center;">Recommended solder iron condition (Pb-Sn Solder and Lead Free Solder)</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th data-bbox="555 241 762 297">Temp. (°C)</th> <th data-bbox="762 241 970 297">Duration (sec.)</th> <th data-bbox="970 241 1177 297">Wattage (W)</th> <th data-bbox="1177 241 1385 297">Shape (mm)</th> </tr> </thead> <tbody> <tr> <td data-bbox="555 297 762 365">300 max.</td> <td data-bbox="762 297 970 365">3 max.</td> <td data-bbox="970 297 1177 365">20 max.</td> <td data-bbox="1177 297 1385 365">Ø 3.0 max.</td> </tr> </tbody> </table> <p>2) Direct contact of the soldering iron with ceramic dielectric of chip capacitors may cause crack. Do not touch the ceramic dielectric and the terminations by solder iron.</p> <p>5-7. Sn-Zn solder Sn-Zn solder affects product reliability. Please contact TDK in advance when utilize Sn-Zn solder.</p> <p>5-8. Countermeasure for tombstone The misalignment between the mounted positions of the capacitors and the land patterns should be minimized. The tombstone phenomenon may occur especially the capacitors are mounted (in longitudinal direction) in the same direction of the reflow soldering. (Refer to JEITA RCR-2335B Annex A (Informative) Recommendations to prevent the tombstone phenomenon)</p>	Temp. (°C)	Duration (sec.)	Wattage (W)	Shape (mm)	300 max.	3 max.	20 max.	Ø 3.0 max.
Temp. (°C)	Duration (sec.)	Wattage (W)	Shape (mm)							
300 max.	3 max.	20 max.	Ø 3.0 max.							
6	Cleaning	<p>1) If an unsuitable cleaning fluid is used, flux residue or some foreign articles may stick to chip capacitors surface to deteriorate especially the insulation resistance.</p> <p>2) If cleaning condition is not suitable, it may damage the chip capacitors.</p> <p>2)-1. Insufficient washing</p> <p>(1) Terminal electrodes may corrode by Halogen in the flux.</p> <p>(2) Halogen in the flux may adhere on the surface of capacitors, and lower the insulation resistance.</p> <p>(3) Water soluble flux has higher tendency to have above mentioned problems (1) and (2).</p> <p>2)-2. Excessive washing</p> <p>When ultrasonic cleaning is used, excessively high ultrasonic energy output can affect the connection between the ceramic chip capacitor's body and the terminal electrode. To avoid this, following is the recommended condition.</p> <p style="text-align: center;">Power : 20 W/l max. Frequency : 40 kHz max. Washing time : 5 minutes max.</p> <p>2)-3. If the cleaning fluid is contaminated, density of Halogen increases, and it may bring the same result as insufficient cleaning.</p>								

No.	Process	Condition						
7	Coating and molding of the P.C.board	1) When the P.C.board is coated, please verify the quality influence on the product. 2) Please verify carefully that there is no harmful decomposing or reaction gas emission during curing which may damage the chip capacitors. 3) Please verify the curing temperature.						
8	Handling after chip mounted  Caution	1) Please pay attention not to bend or distort the P.C.board after soldering in handling otherwise the chip capacitors may crack. <div style="display: flex; justify-content: space-around; align-items: center;"> <div style="text-align: center;">  <p>Bend</p> </div> <div style="text-align: center;">  <p>Twist</p> </div> </div> 2) When functional check of the P.C.board is performed, check pin pressure tends to be adjusted higher for fear of loose contact. But if the pressure is excessive and bend the P.C.board, it may crack the chip capacitors or peel the terminations off. Please adjust the check pins not to bend the P.C.board. <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th data-bbox="491 981 627 1037">Item</th> <th data-bbox="627 981 1050 1037">Not recommended</th> <th data-bbox="1050 981 1449 1037">Recommended</th> </tr> </thead> <tbody> <tr> <td data-bbox="491 1037 627 1294" style="text-align: center; vertical-align: middle;">Board bending</td> <td data-bbox="627 1037 1050 1294" style="text-align: center;">  <p>Termination peeling</p> <p>Check pin</p> </td> <td data-bbox="1050 1037 1449 1294" style="text-align: center;">  <p>Support pin</p> <p>Check pin</p> </td> </tr> </tbody> </table>	Item	Not recommended	Recommended	Board bending	 <p>Termination peeling</p> <p>Check pin</p>	 <p>Support pin</p> <p>Check pin</p>
Item	Not recommended	Recommended						
Board bending	 <p>Termination peeling</p> <p>Check pin</p>	 <p>Support pin</p> <p>Check pin</p>						
9	Handling of loose chip capacitors	1) If dropped the chip capacitors may crack. Once dropped do not use it. Especially, the large case sized chip capacitors are tendency to have cracks easily, so please handle with care. <div style="text-align: center;">  <p>Crack</p> <p>Floor</p> </div> 2) Piling the P.C.board after mounting for storage or handling, the corner of the P.C. board may hit the chip capacitors of another board to cause crack. <div style="text-align: center;">  <p>Crack</p> <p>P.C.board</p> </div>						

No.	Process	Condition
10	Estimated life and estimated failure rate of capacitors	<p>As per the estimated life and the estimated failure rate depend on the temperature and the voltage. This can be calculated by the equation described in JEITA RCR-2335B Annex 6 (Informative) Calculation of the estimated lifetime and the estimated failure rate ( Voltage acceleration coefficient : 3 multiplication rule, Temperature acceleration coefficient : 10°C rule)</p> <p>The failure rate can be decreased by reducing the temperature and the voltage but they will not be guaranteed.</p>
11	<p>Others</p> <p> Caution</p>	<p>The products listed on this specification sheet are intended for use in general electronic equipment (AV equipment, telecommunications equipment, home appliances, amusement equipment, computer equipment, personal equipment, office equipment, measurement equipment, industrial robots) under a normal operation and use condition.</p> <p>The products are not designed or warranted to meet the requirements of the applications listed below, whose performance and/or quality require a more stringent level of safety or reliability, or whose failure, malfunction or trouble could cause serious damage to society, person or property. Please understand that we are not responsible for any damage or liability caused by use of the products in any of the applications below or for any other use exceeding the range or conditions set forth in this specification sheet. If you intend to use the products in the applications listed below or if you have special requirements exceeding the range or conditions set forth in this specification, please contact us.</p> <p>(1) Aerospace/Aviation equipment  (2) Transportation equipment (electric trains, ships, etc.)  (3) Medical equipment  (4) Power-generation control equipment  (5) Atomic energy-related equipment  (6) Seabed equipment  (7) Transportation control equipment  (8) Public information-processing equipment  (9) Military equipment  (10) Electric heating apparatus, burning equipment  (11) Disaster prevention/crime prevention equipment  (12) Safety equipment  (13) Other applications that are not considered general-purpose applications</p> <p>When designing your equipment even for general-purpose applications, you are kindly requested to take into consideration securing protection circuit/device or providing backup circuits in your equipment.</p>

## 10. PACKAGING LABEL

Packaging shall be done to protect the components from the damage during transportation and storing, and a label which has the following information shall be attached.

- 1) Inspection No.
- 2) TDK P/N
- 3) Customer's P/N
- 4) Quantity

\*Composition of Inspection No.

Example     F 2 A - 00 - 000  
                  (a) (b) (c)     (d)        (e)

- a) Line code
- b) Last digit of the year
- c) Month and A for January and B for February and so on. (Skip I)
- d) Inspection Date of the month.
- e) Serial No. of the day

## 11. BULK PACKAGING QUANTITY

Total number of components in a plastic bag for bulk packaging : 1,000pcs.

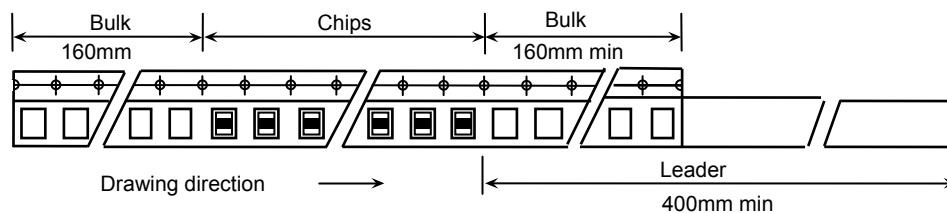
## 12. TAPE PACKAGING SPECIFICATION

### 1. CONSTRUCTION AND DIMENSION OF TAPING

#### 1-1. Dimensions of carrier tape

Dimensions of paper tape shall be according to Appendix 4.

#### 1-2. Bulk part and leader of taping

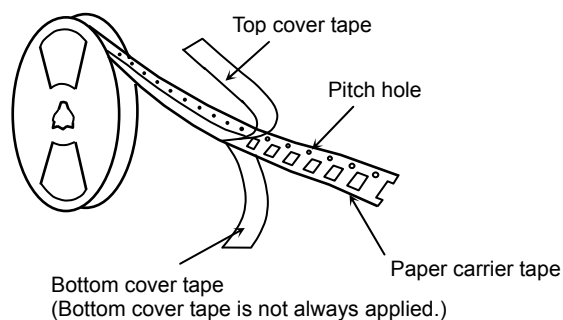


#### 1-3. Dimensions of reel

Dimensions of Ø178 reel shall be according to Appendix 5.

Dimensions of Ø330 reel shall be according to Appendix 6.

#### 1-4. Structure of taping



## 2. CHIP QUANTITY

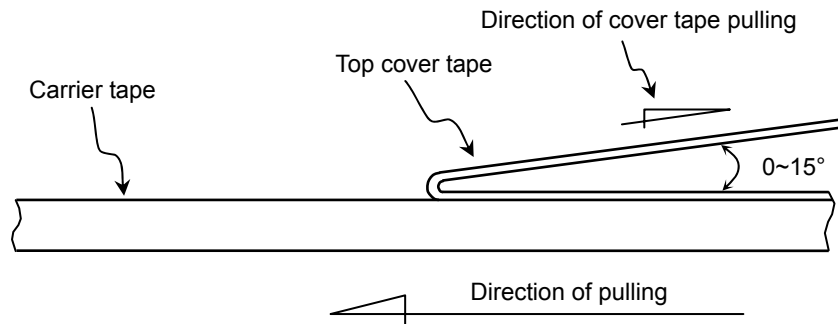
Type	Thickness of chip	Taping Material	Chip quantity(pcs.)	
			Ø 178mm reel	Ø 330mm reel
CGA3(CC0603)	0.80 mm	Paper	4,000	10,000

### 3. PERFORMANCE SPECIFICATIONS

3-1. Fixing peeling strength (top tape)

0.05-0.7N. (See the following figure.)

TYPE 1 (Paper)



3-2. Carrier tape shall be flexible enough to be wound around a minimum radius of 30mm with components in tape.

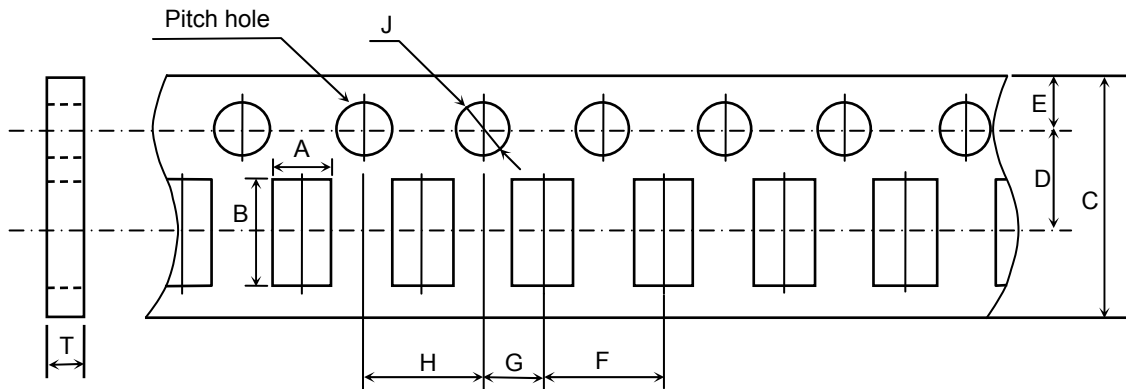
3-3. The missing of components shall be less than 0.1%

3-4. Components shall not stick to fixing tape.

3-5. The fixing tapes shall not protrude beyond the edges of the carrier tape not shall cover the sprocket holes.

## Appendix 4

### Paper Tape



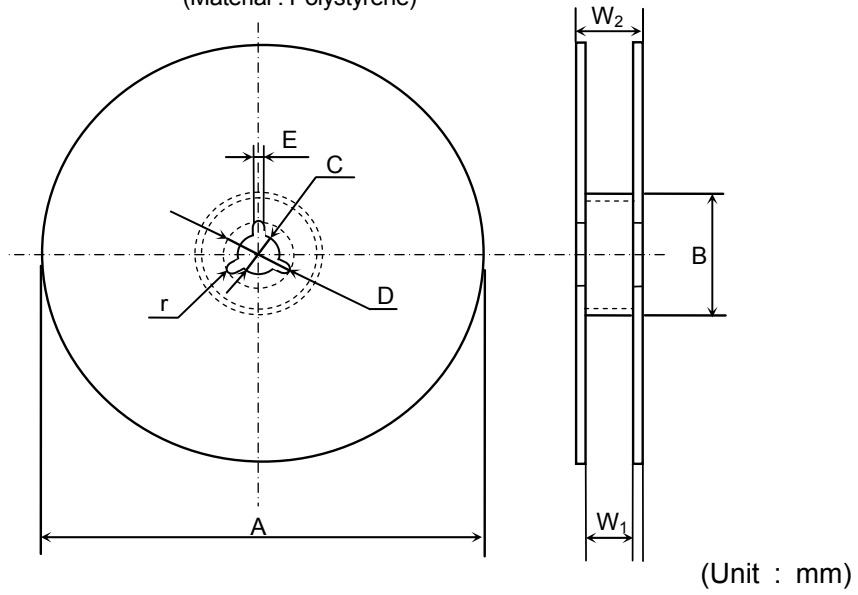
(Unit : mm)

Symbol Type	A	B	C	D	E	F
CGA3 (CC0603)	( 1.10 )	( 1.90 )	$8.00 \pm 0.30$	$3.50 \pm 0.05$	$1.75 \pm 0.10$	$4.00 \pm 0.10$
Symbol Type	G	H	J	T		
CGA3 (CC0603)	$2.00 \pm 0.05$	$4.00 \pm 0.10$	$\varnothing 1.5 \begin{smallmatrix} +0.10 \\ 0 \end{smallmatrix}$	1.20 max.		

\* The values in the parentheses ( ) are for reference.

## Appendix 5

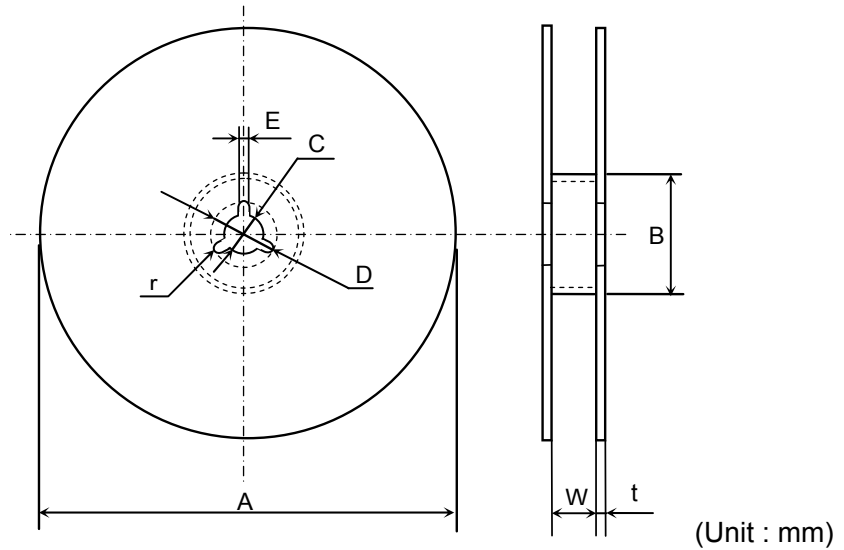
(Material : Polystyrene)



Symbol	A	B	C	D	E	W <sub>1</sub>
Dimension	Ø178 ± 2.0	Ø60 ± 2.0	Ø13 ± 0.5	Ø21 ± 0.8	2.0 ± 0.5	9.0 ± 0.3
Symbol	W <sub>2</sub>	r				
Dimension	13.0 ± 1.4	1.0				

## Appendix 6

(Material : Polystyrene)



Symbol	A	B	C	D	E	W
Dimension	Ø382 max. (Nominal Ø330)	Ø50 min.	Ø13 ± 0.5	Ø21 ± 0.8	2.0 ± 0.5	10.0 ± 1.5
Symbol	t	r				
Dimension	2.0 ± 0.5	1.0				