PI90LVB179/PI90LVB180/ PI90LVB050/PI90LVB051

3.3V Bus LVDS High-Speed Differential Line Drivers and Receivers

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Features

- Signaling Rates >660 Mbps (330 MHz)
- Single 3.3V Power Supply Design
- Driver:
  - — ±350mV Differential Swing into a 50-ohm load
  - — Propogation Delay of 1.5ns Typ.
  - — Low Voltage TTL (LVTTL) Inputs are 5V Tolerant
  - — Driver is High Impedance when Disabled or V_{CC} < 1.5V
- Receiver:
  - — Accepts ±50mV (min.) Differential Swing with up to 2.0V ground potential difference
  - — Propagation Delay of 2ns Typ.
  - — Low Voltage TTL (LVTTL) Outputs
  - — Open, Short, and Terminated Fail Safe
- Industrial Temperature Operating Range: –40°C to 85°C
- Bus-Terminal ESD≥12kV
- Packaging (Pb-free & Green avalible):
  - PI90LVB179: 8-pin SOIC (W) & 8-pin MSOP (U)
  - PI90LVB180: 14-pin TSSOP (L) & 14-pin SOIC (W)
  - PI90LVB050: 16-pin TSSOP (L) & 16-pin SOIC (W)
  - PI90LVB051: 16-pin TSSOP (L) & 16-pin SOIC (W)

Description

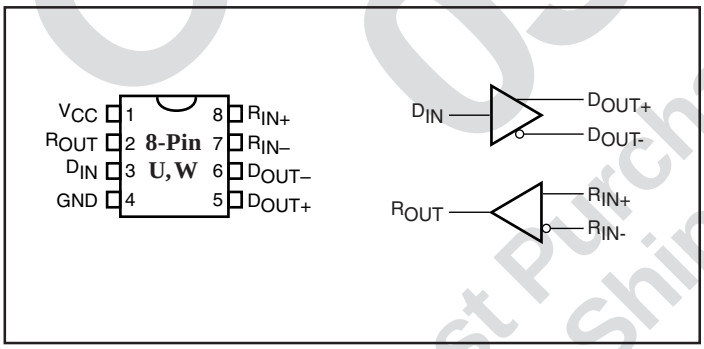
The PI90LVB179, PI90LVB180, PI90LVB050, and PI90LVB051 are differential line drivers and receivers (transceivers) that are similar to the IEEE 1596.3 SCI and ANSI/TIA/EIA-644 LVDS standards (the difference is that the driver output current is doubled). This modification enables true half-duplex operation with more than one LVDS driver or with two line transmission resistors over a 50-ohm differential transmission line. These devices use low-voltage differential signaling (LVDS) to achieve data rates in excess of 660 Mbps while being less susceptible to noise than single-ended transmission.

The drivers translate a low-voltage TTL/CMOS input into a low-voltage (350mV typical) differential output signal into a 50-ohm load. The receivers translate a differential 350mV input signal to a 3V CMOS output level. Driver section can be independently set to a power-down & high-impedance output mode with the D_{EN} pin (active HIGH). Receiver section is controlled by the R_{EN*} pin (active LOW).

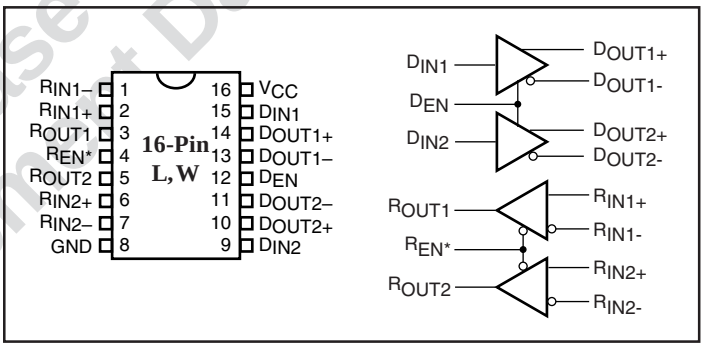
Applications

Applications include point-to-point and multidrop baseband data transmission over a controlled impedance media of approximately 50-ohms. These include intra-system connections via printed circuit board traces or cables, hubs and routers for data communications; PBXs, switches, repeaters & base stations for telecommunications and other applications such as digital cameras, printers and copiers.

PI90LVB179



PI90LVB050



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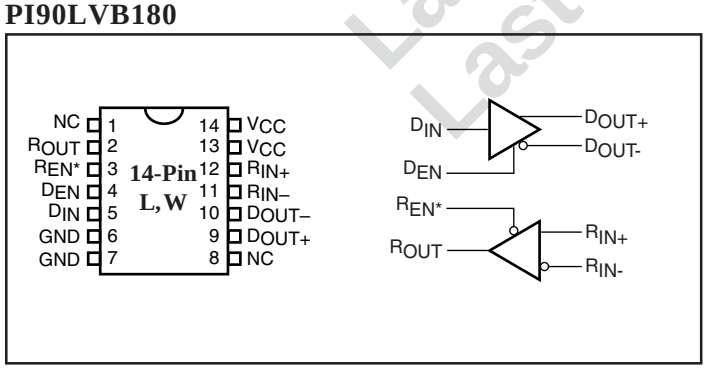
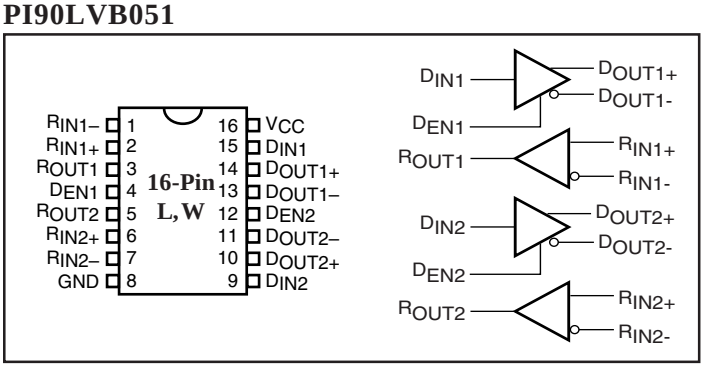


PI90LVB051



Function Tables

PI90LVB179 Receiver

Inputs	Output
$V_{ID} = V_{RIN+} - V_{RIN-}$	R_{OUT}
$V_{ID} \geq 50mV$	H
$-50mV < V_{ID} < 50mV$	?
$V_{ID} \leq -50mV$	L
open	H

PI90LVB179 Driver

Input	Output	
D_{IN}	D_{OUT+}	D_{OUT-}
L	L	H
H	H	L
open	L	H

PI90LVB180/ PI90LVB050/PI90LVB051 Receivers

Inputs		Output
$V_{ID} = V_{RIN+} - V_{RIN-}$	R_{EN*}	R_{OUT}
$V_{ID} \geq 50mV$	L	H
$-50mV < V_{ID} < 50mV$	L	?
$V_{ID} \leq -50mV$	L	L
open	L	H
X	H	Z

PI90LVB180/PI90LVB050/PI90LVB051 Drivers

Inputs		Output	
D_{IN}	D_{EN}	D_{OUT+}	D_{OUT-}
L	H	L	H
H	H	H	L
open	H	L	H
X	L	Z	Z

Notes:
H = High Level, L = Low Level, ? = Indeterminate,
Z = High-Impedance, X = Don't Care

Pin Descriptions

Name	Description
D_{IN}	TTL/CMOS driver input pins
D_{OUT+}	Non-inverting driver output pins
D_{OUT+}	Inverting driver output pins
R_{OUT}	TTL/CMOS receiver output pins
$R_{IN}+$	Non-inverting receiver input pins
R_{IN-}	Inverting receiver input pins
V_{ID}	Input Differential Signal Voltage
GND	Ground pin
V_{CC}	Positive power supply pin, +3.3V ±10%

Absolute Maximum Ratings

Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
Driver
Input Voltage (D_{IN}) ..... –0.3V to (Vcc + 0.3V)
Output Voltage (D_{OUT+}, D_{OUT-}) ..... –0.3V to +3.9V
Short Circuit Duration (D_{OUT+}, D_{OUT-}) ..... Continuous
Enable Input Voltage (D_{EN}) ..... –0.3V to (V_{CC} + 0.3V)
Receiver
Input Voltage (R_{IN+}, R_{IN-}) ..... –0.3V to +3.9V)
Output Voltage (R_{OUT}) ..... –0.3V to (V_{CC} + 0.3V)
Enable Input Voltage (R_{EN*}) ..... –0.3V to (V_{CC} + 0.3V)
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature Range Soldering (4s) ..... +260°C
Maximum Junction Temperature ..... +150°C
ESD Rating ..... >12kV

Recommended Operating Conditions

	Min.	Typ.	Max.	Units
Supply Voltage (V_{CC})	3	3.3	3.6	V
High Level Input Voltage, V_{IH}	2			
Low Level Input Voltage, V_{IL}			0.8	
Magnitude of Differential Input Voltage V_{ID}	0.1		0.6	
Common-mode Input Voltage, V_{IC} (Fig 5)	$\|V_{ID}\|/2$		$2.4 - \|V_{ID}\|/2$	
			$V_{CC} - 0.8$	
Operating Free Air Temperature T_A	–40		85	°C

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Electrical Characteristics (Over recommended operating conditions unless otherwise noted).

Parameter		Test Condition	Min.	Typ.†	Max.	Units
I_{CC}* Supply Current	PI90LVB179	No receiver load, Driver R_L = 50-ohms		14	19.5	mA
	PI90LVB180	Driver and receiver enabled. No receiver load, Driver R_L = 50-ohms		12.5	16.4	
		Driver enabled, Receiver disabled, R_L = 50 ohms		10.2	14	
		Driver disabled, Receiver enabled, No load		3.4	5	
		Disabled		0.8	1.5	
	PI90LVB050	Driver and receivers enabled. No receiver loads, Driver R_L = 50-ohms		25	30	
		Drivers enabled, Receivers disabled, R_L = 50-ohms		14.8	20	
		Drivers disabled, Receivers enabled, No loads		6	8	
		Disabled		0.8	1.3	
	PI90LVB051	Drivers enabled, No receiver loads, Driver R_L = 50-ohms		27	33	
		Drivers disabled, No loads		6.5	8.8	

†All typical values are at 25°C with a 3.3V supply
*I_{CC} measured with all TTL input. $V_{IN} = V_{CC}$ or GND.

Driver Electrical Characteristics (Over recommended operating conditions unless otherwise noted).

Parameter			Test Conditions	Min.	Typ.	Max.	Units
$\lvert V_{OD} \rvert$	Differential output voltage magnitude		R_L = 50-ohms See Figures 1 and 2	247	380	475	mV
$\Delta\lvert V_{OD} \rvert$	Change in differential output voltage magnitude between logic states			–50		50	
$V_{OC(SS)}$	Steady-state common-mode output voltage		See Figure 3	1.125	1.25	1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states			–50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage				50	150	
I_{IH}	High-level input current	DE	V_{IH} = 5V		–0.5	–20	µA
		D_{IN}			2	20	
I_{IL}	Low-level input current	DE	V_{IL} = 0.8V		–0.5	–10	
		D_{IN}			2	10	
I_{OS}	Short-circuit output current		V_{OY} or V_{OZ} = 0V		–11	–15	mA
			V_{OD} = 0V		–12	–15	
I_{OZ}	High-impedance output current		V_{OD} = 600mV			±1	µA
			V_O - 0V or V_{CC}			±1	
$I_{O(OFF)}$	Power-off output current		V_{CC} = 0V, V_O = 3.6V			±1	
C_{IN}	Input capacitance				7		pF

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Receiver Electrical Characteristics (Over recommended operating conditions unless otherwise noted).

Parameter		Test Conditions	Min.	Typ.	Max.	Units
V_{ITH+}	Positive-going differential input voltage threshold	See Figures 5 & Table 1			50	mV
V_{ITH-}	Negative-going differential input voltage threshold		–50			
V_{OH}	High-level output voltage	I_{OH} = –8mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8mA			0.4	V
I_I	Input current (R_{IN+} or R_{IN-})	V_I = 0	–2	–11	–20	µA
		V_I = 2.4V	–1.2	–3		
$I_{I\ (OFF)}$	Power-off input current (R_{IN+} or R_{IN-})	V_{CC} = 0			±20	
I_H	High-level input current (enables)	V_{IH} = 2V			±10	
I_L	Low-level input current (enables)	V_{IL} = 0.8V			±10	
I_{OZ}	High-impedance output current	V_O = 0 or 5V			±10	
C_I	Input capacitance			6.6		pF

†All typical values are at 25°C with a 3.3V supply

Driver Switching Characteristics (Over recommended operating conditions unless otherwise noted).

Parameter		Test Conditions	Min.	Typ.†	Max.	Units
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 50-ohms C_L = 10pF See Figure 2		1.7	2.6	ns
t_{PHL}	Propagation delay time, high-to-low-level output			1.7	2.6	
t_r	Differential output signal rise time			0.4	0.8	
t_f	Differential output signal fall time			0.4	0.8	
$t_{sk(p)}$	Pulse skew ($t_{PHL} - t_{PLH}$)			250	360	ps
$t_{sk(o)}$	Channel-to-channel output skew‡			90	160	
$t_{sk(pp)}$	Part-part-part skew**				0.9	ns
t_{PZH}	ENABLE TIME, High Impedance to High Level output	See Figure 4		3	5	
t_{PZL}	ENABLE TIME, High Impedance to Low Level output			3	5	
t_{PHZ}	DISABLE TIME, High Level to High Impedance output			3	5	
t_{PLZ}	DISABLE TIME, Low Level to High Impedance output			3	5	

† All typical values are at 25°C with a 3.3V supply
‡ $t_{sk(o)}$: the maximum delay time difference between drivers on the same device.
** $t_{sk(pp)}$: magnitude of difference in propagation delay times between any specific terminals of two devices (all things being equal)

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Receiving Switching Characteristics (Over recommended operating conditions unless otherwise noted).

Parameter		Test Conditions	Min.	Typ.†	Max.	Units
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 10pF See Figure 6		2	3.0	ns
t_{PHL}	Propagation delay time, high-to-low-level output			2.1	3.0	
$t_{sk(pp)}$**	Part-part-part skew**				1.0	
$t_{sk(p)}$	Pulse skew ($t_{PHL} - t_{PLH}$)			300	750	ps
$t_{sk(o)}$	Channel-to-channel skew			60		
t_r	Output signal rise time			1.0	1.5	ns
t_f	Output signal fall time			1.2	1.8	
t_{PZH}	ENABLE TIME, High Impedance to High Level output	See Figure 7		1.7	2.3	
t_{PZL}	ENABLE TIME, High Impedance to Low Level output			4.5	5.7	
t_{PHZ}	DISABLE TIME, High Level to High Impedance output			2.5	3.2	
t_{PLZ}	DISABLE TIME, Low Level to High Impedance output			6.0	7.8	

† All typical values are at 25°C with a 3.3V supply.
** $t_{sk(pp)}$ is magnitude of difference in propagation delay times between any specific terminals of two devices (all things being equal).

Parameter Measurement Information

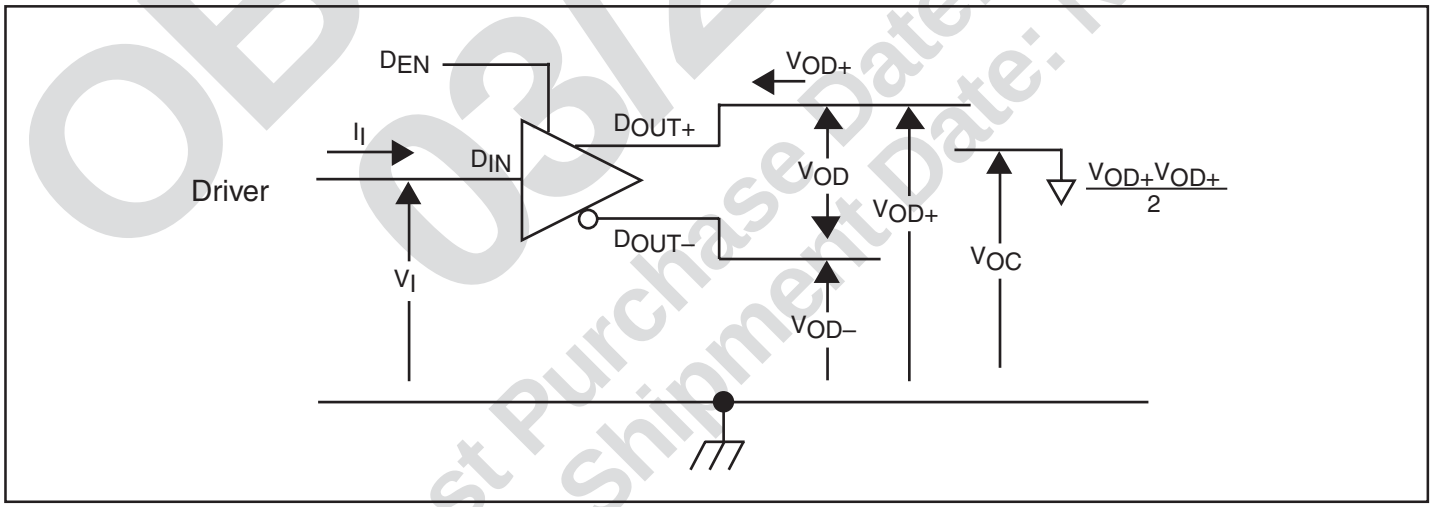

Figure 1. Driver Voltage and Current Definitions

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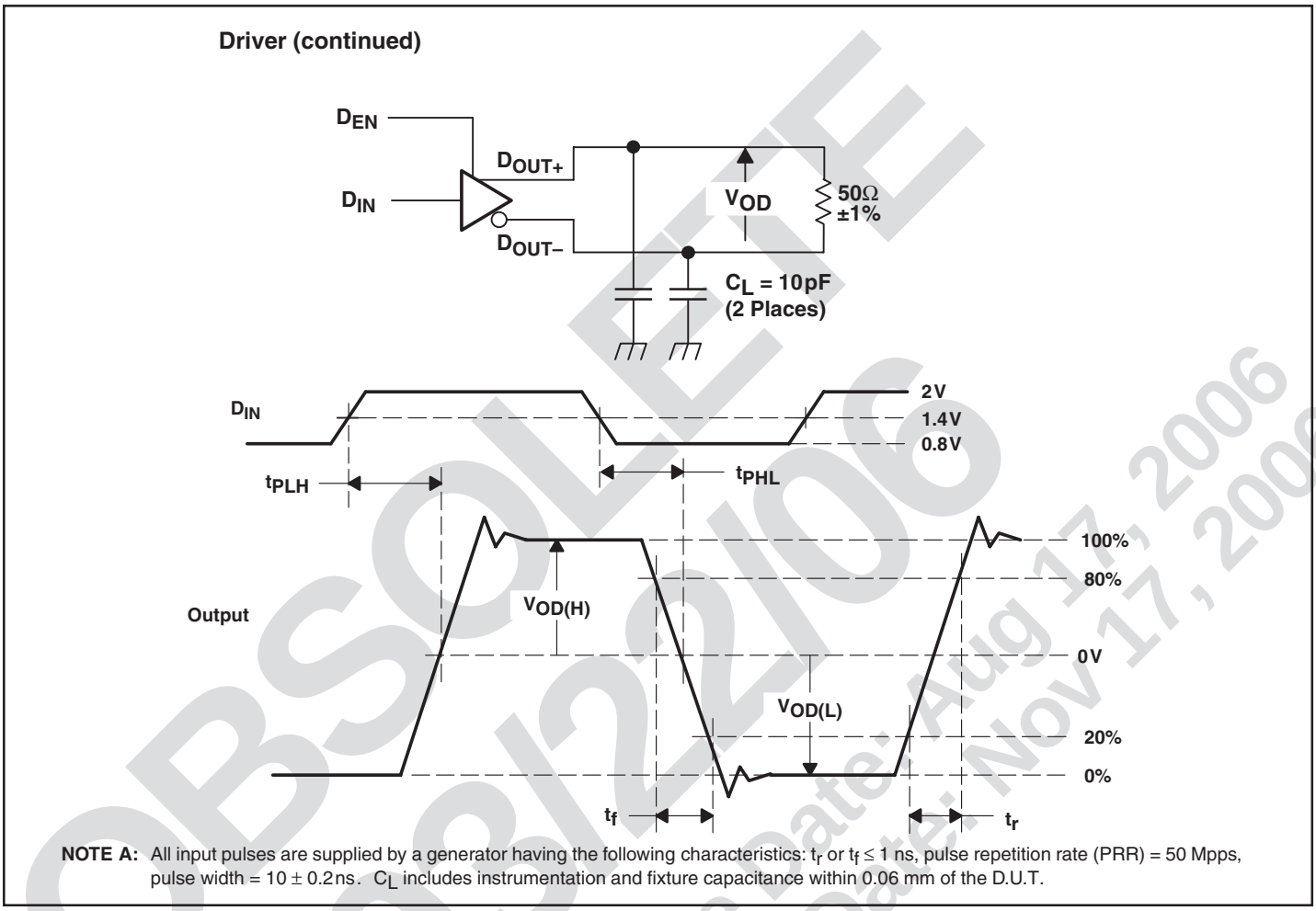
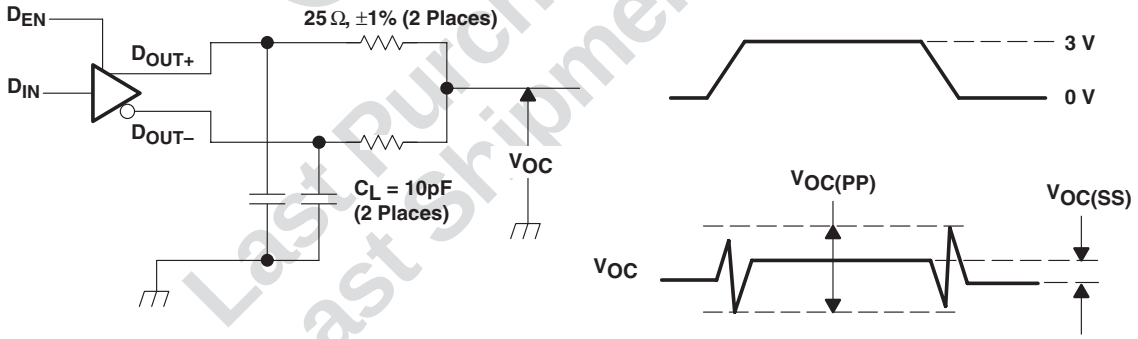
Parameter Measurement Information



NOTE A: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns. C_L includes instrumentation and fixture capacitance within 0.06 mm of the D.U.T.

Figure 2. Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal



NOTE A: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns. C_L includes instrumentation and fixture capacitance within 0.06 mm of the D.U.T The measurement of $V_{OC(PP)}$ is made on test equipment with a –3 dB bandwidth of at least 300 MHz.

Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

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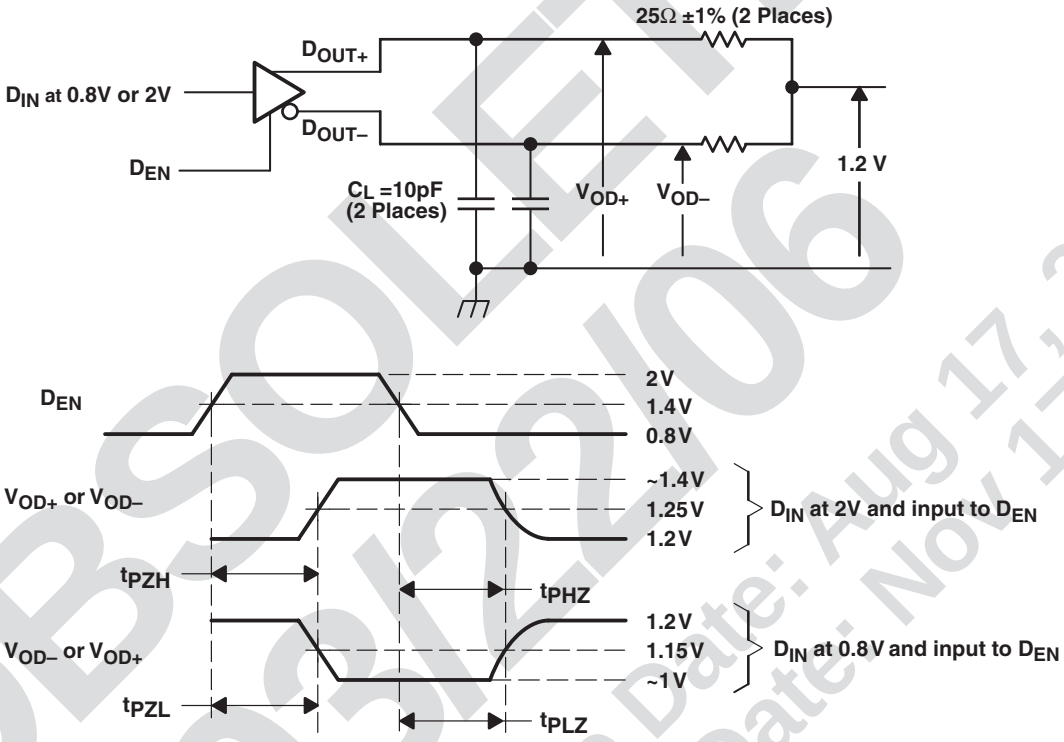
Parameter Measurement Information (continued)

Driver (continued)



NOTE A: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0.06mm of the D.U.T.

Figure 4. Enable and Disable Timing Circuit and Definitions

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Parameter Measurement Information (continued)

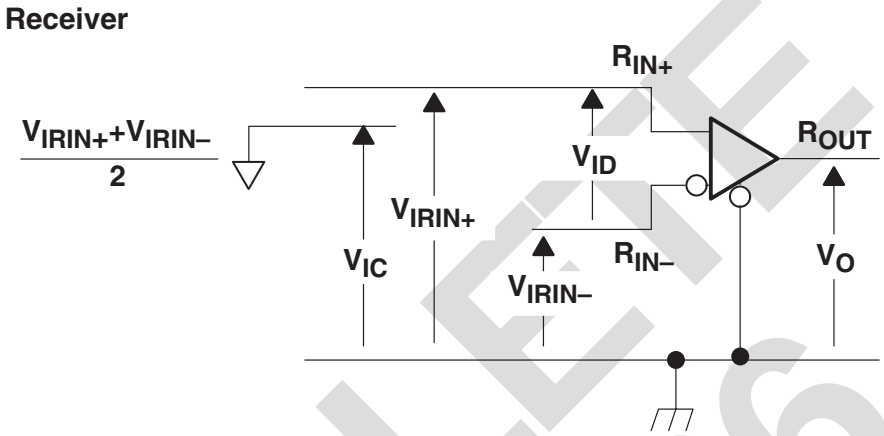

Figure 5. Receiver Voltage Definitions

Table 1. Receiver Minimum and Maximum Input Threshold Test Voltages

APPLIED VOLTAGES (V)		RESULTING DIFFERENTIAL INPUT VOLTAGE (mV)	RESULTING COMMON-MODE INPUT VOLTAGE (V)
V_{IRIN+}	V_{IRIN-}	V_{ID}	V_{IC}
1.225	1.175	50	1.2
1.175	1.225	–50	1.2
2.375	2.325	50	2.35
2.325	2.375	–50	2.35
0.1	0	50	0.05
0	0.05	–50	0.05
1.5	0.9	600	1.2
0.9	1.5	–600	1.2
2.4	1.8	600	2.1
1.8	2.4	–600	2.1
0.6	0	600	0.3
0	0.6	–600	0.3

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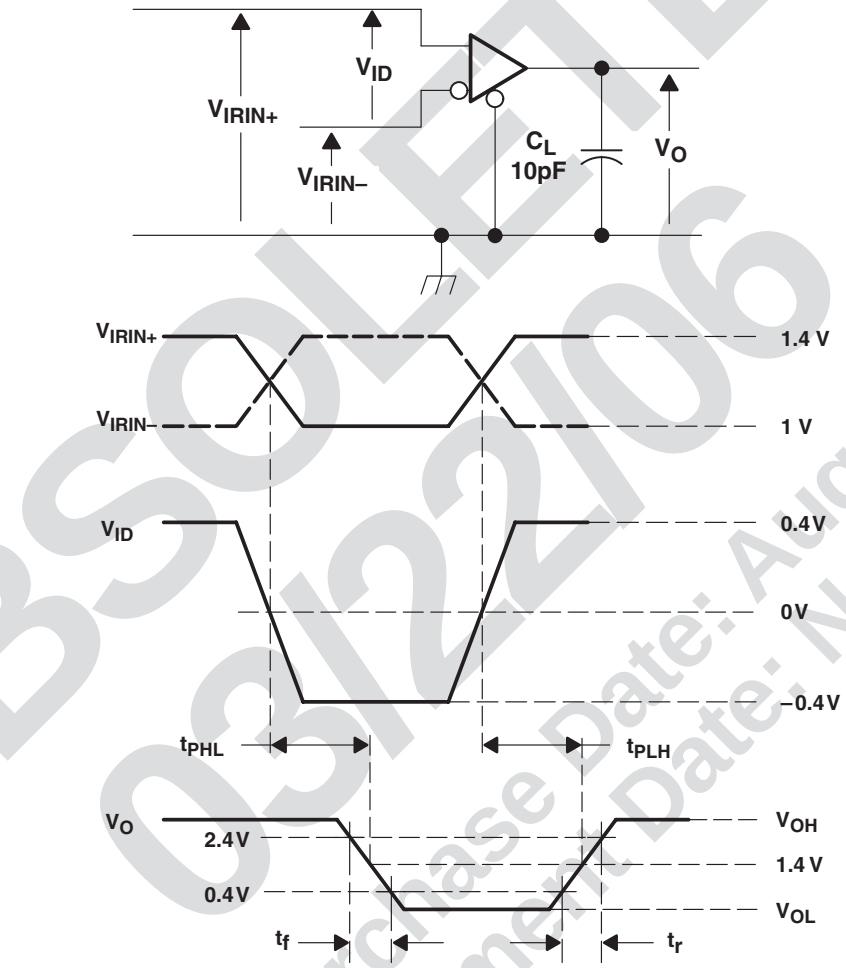
Parameter Measurement Information (continued)

Receiver (continued)



NOTE A: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns. C_L includes instrumentation and fixture capacitance within 0.06 m of the D.U.T.

Figure 6. Timing Test Circuit and Waveforms

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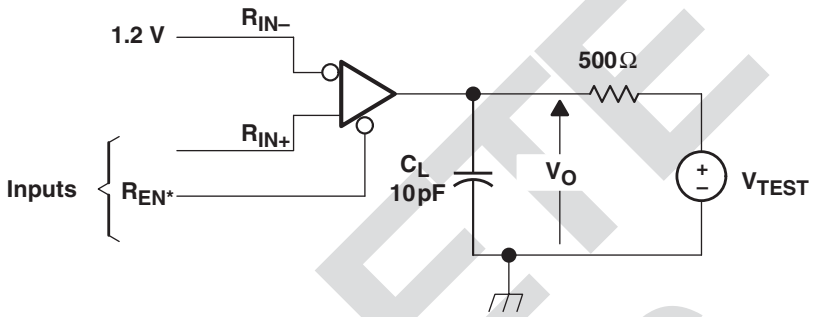
Parameter Measurement Information (continued)

Receiver (continued)



NOTE A: All input pulses are supplied by a genertor having the following characteristics: tr or tf ≤ 1ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse wide = 500 ±10ns. CL includes instrumentation and fixture capacitance within 0.06m of the D.U.T.

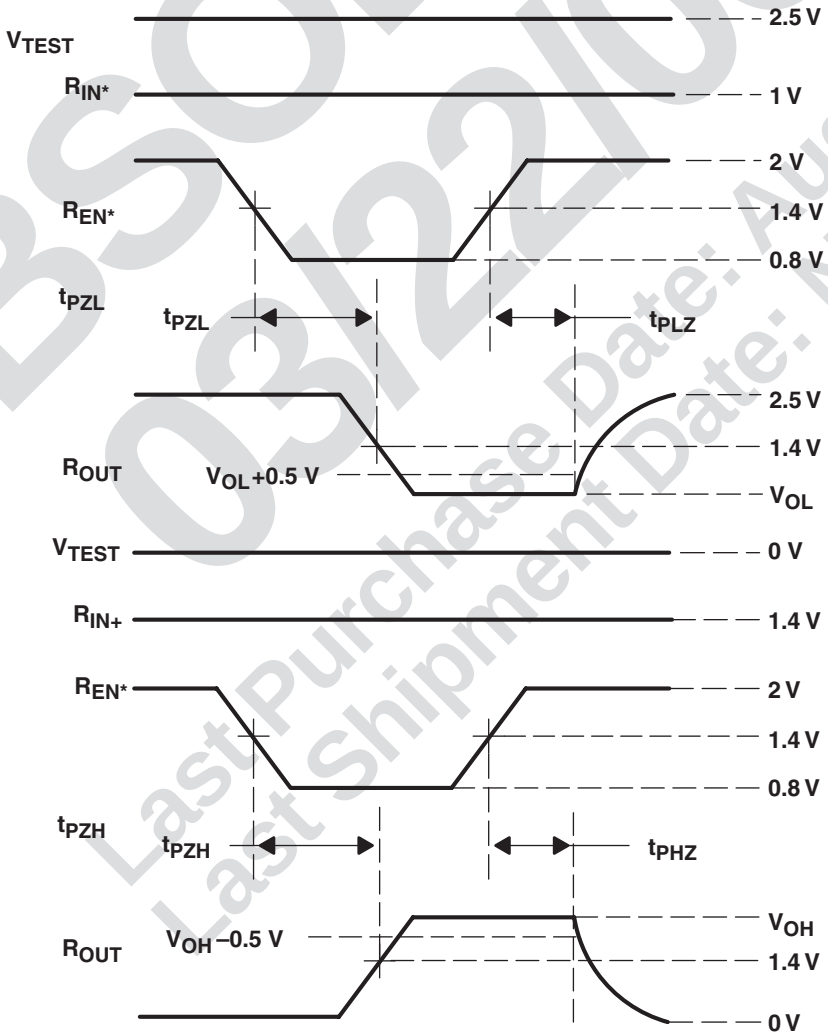


Figure 7. Enable/Disable Time Test Circuit and Waveforms

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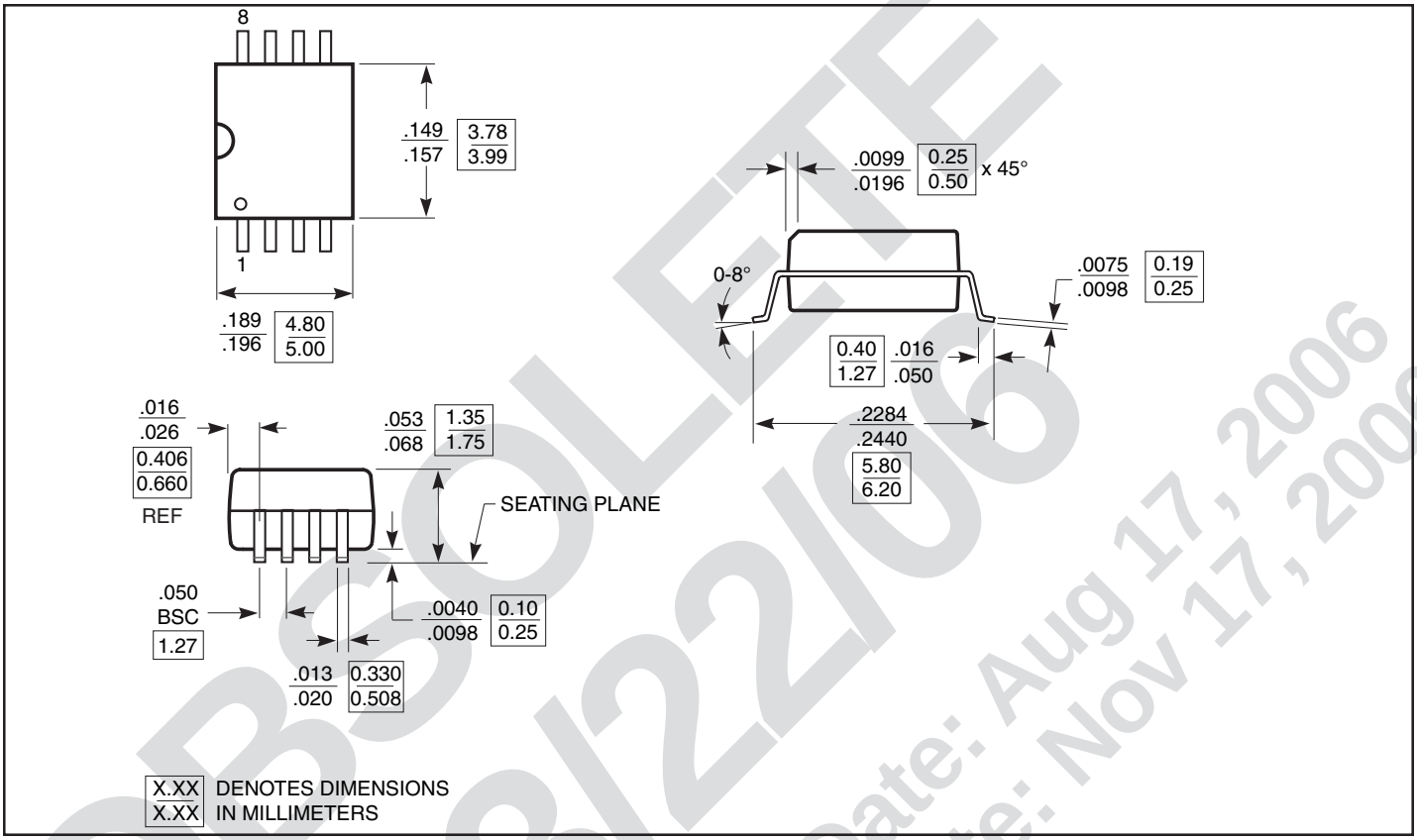
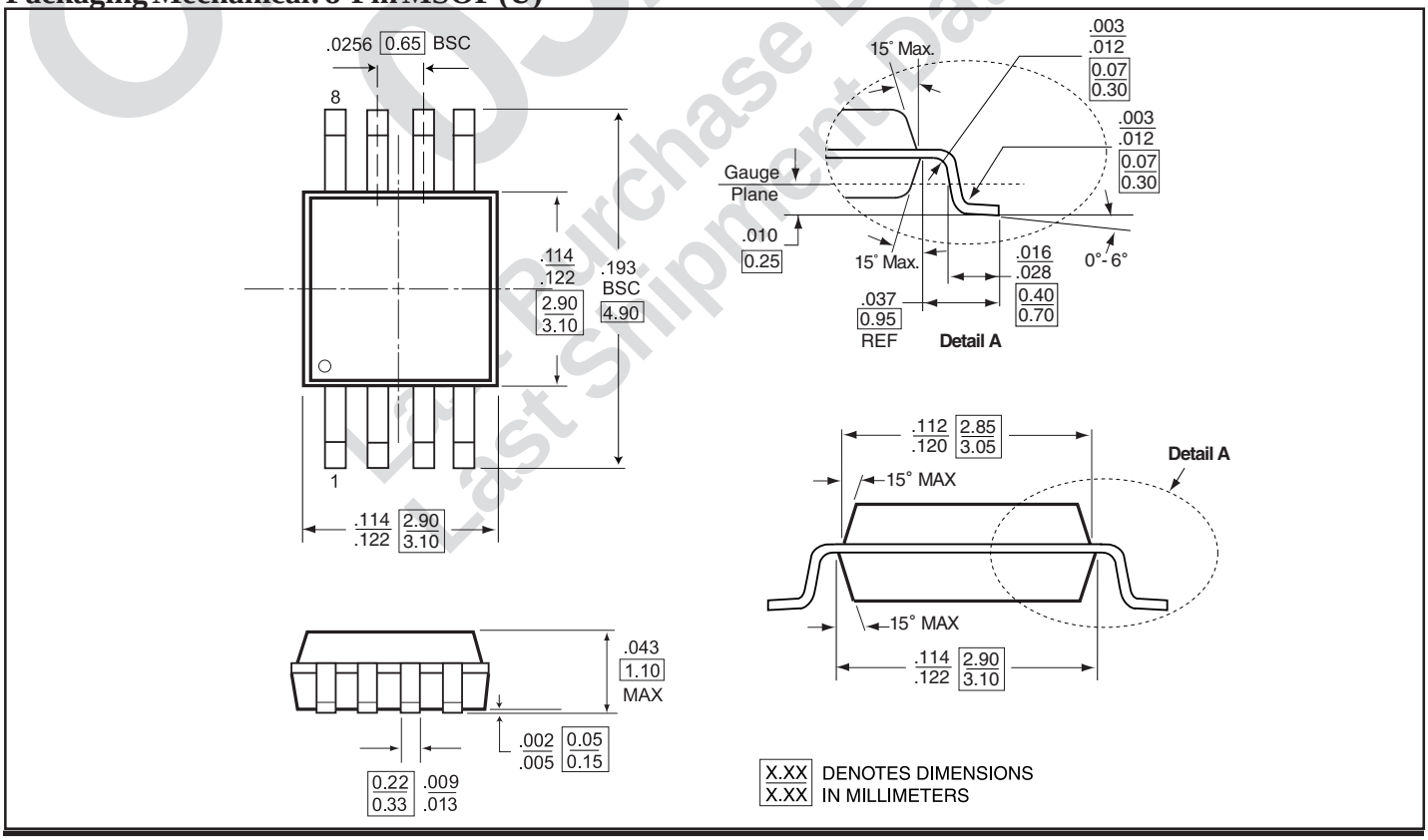
Packaging Mechanical: 8-Pin SOIC (W)



Packaging Mechanical: 8-Pin MSOP (U)



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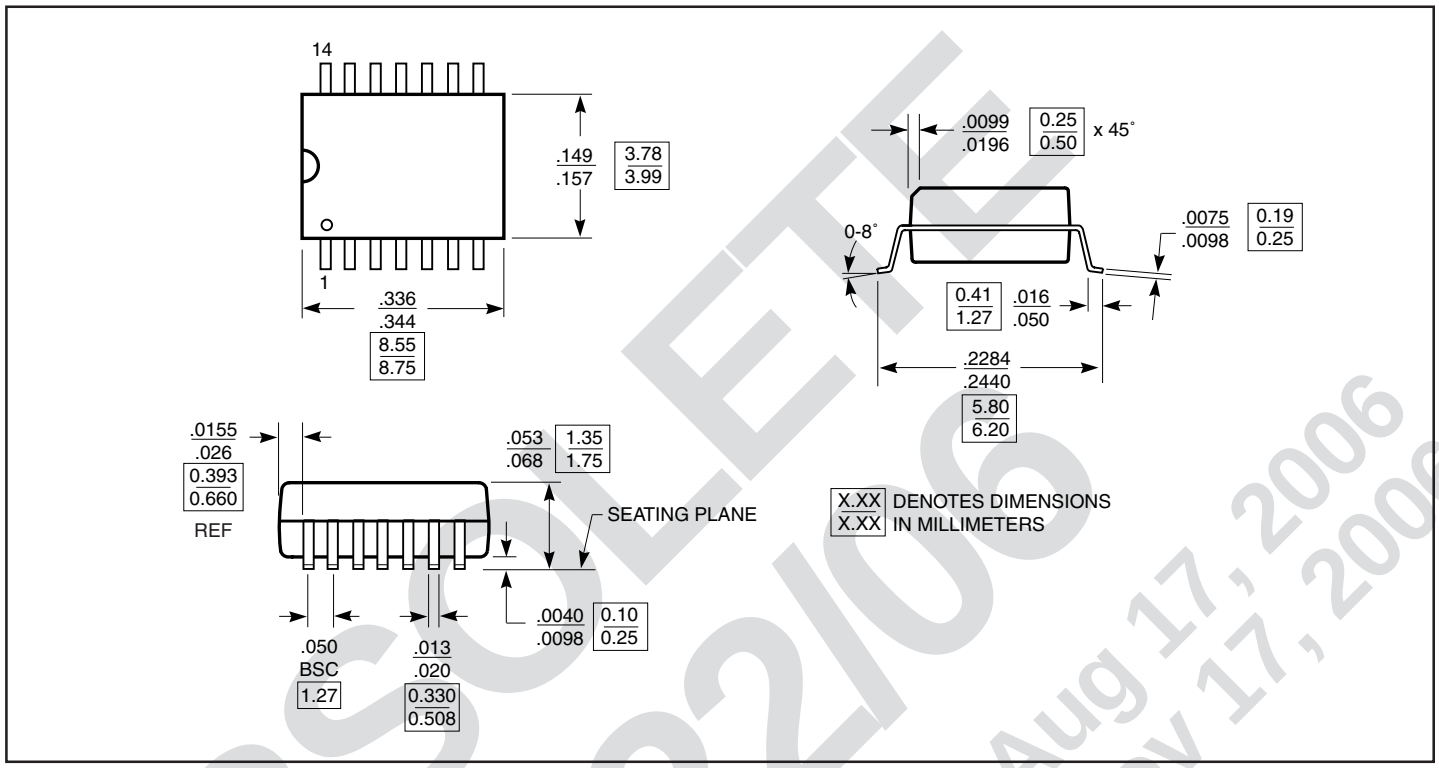
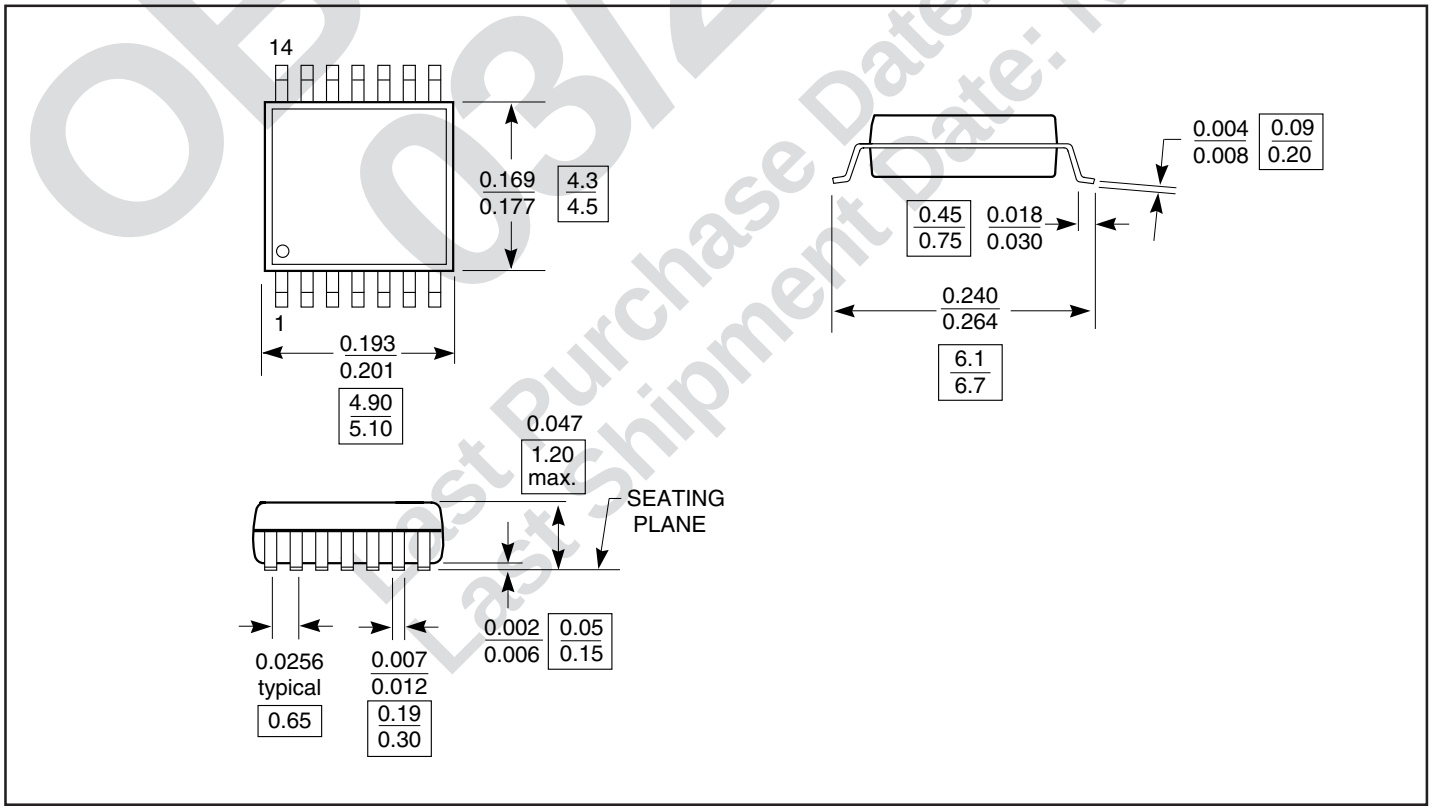
Packaging Mechanical: 14-Pin SOIC(W)



Packaging Mechanical: 14-Pin TSSOP(L)



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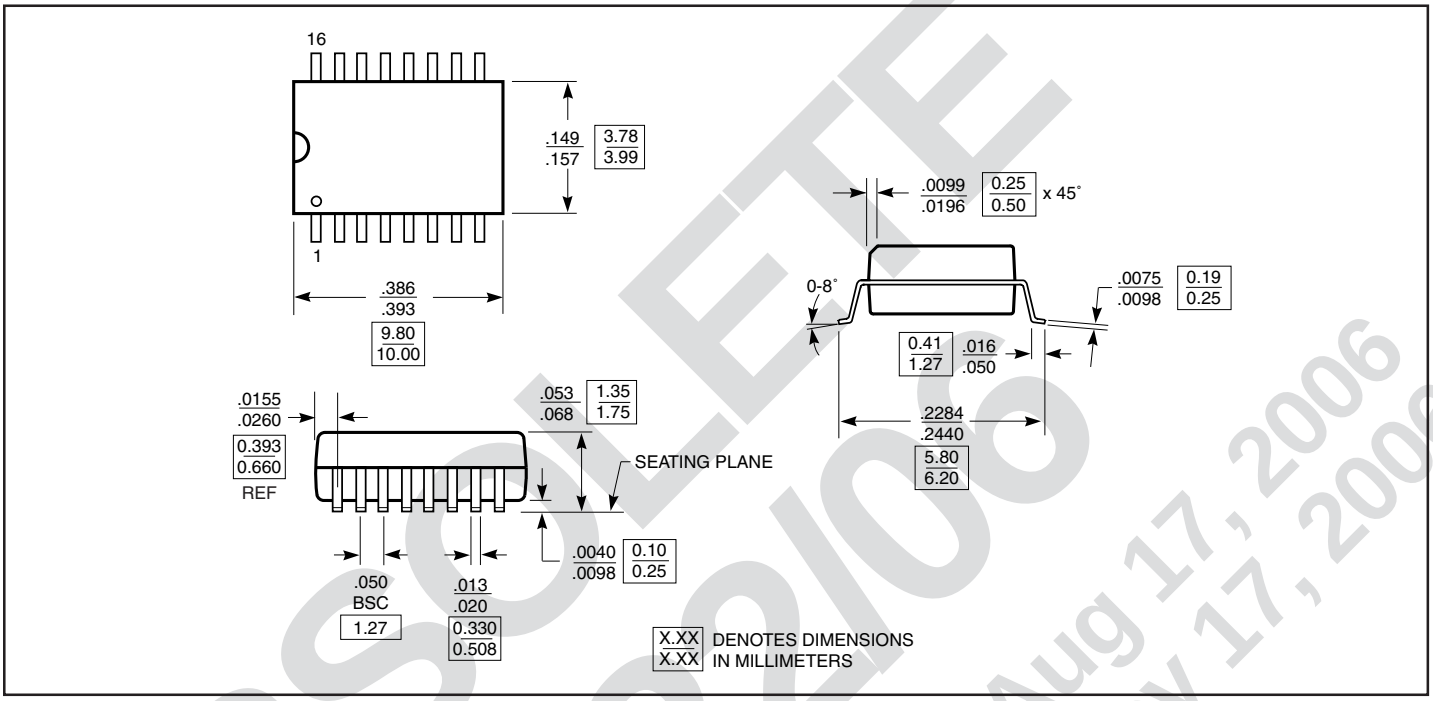
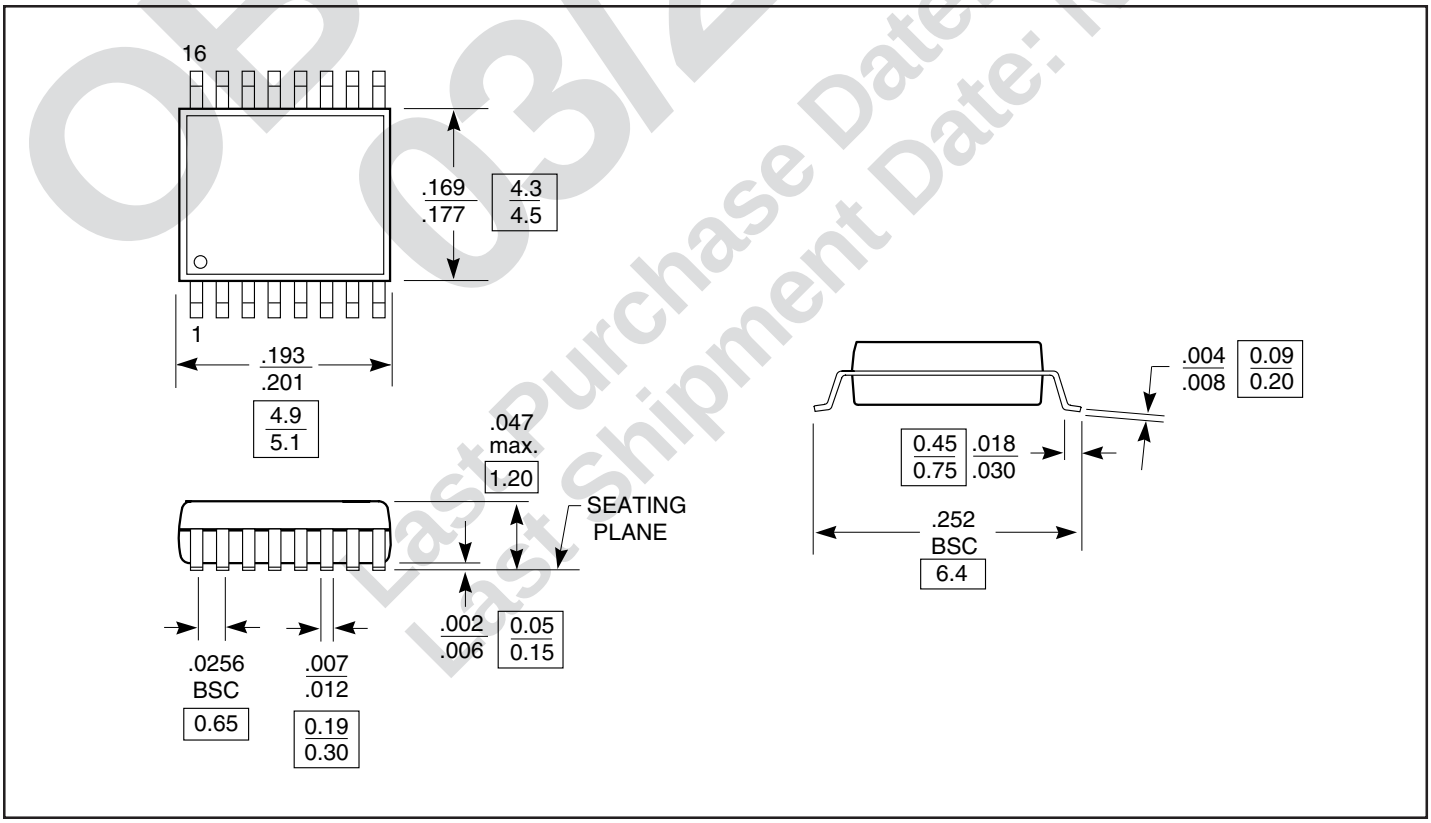
Packaging Mechanical: 16-Pin SOIC (W)



Packaging Mechanical: 16-Pin TSSOP (L)



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Ordering Information

Ordering Code	Package Code	Package Type
PI90LVB179U	U	8-pin MSOP
PI90LVB179UE	U	Pb-free & Green, 8-pin MSOP
PI90LVB179W	W	8-pin SOIC
PI90LVB179WE	W	Pb-free & Green, 8-pin SOIC
PI90LVB180L	L	14-pin TSSOP
PI90LVB180LE	L	Pb-free & Green, 14-pin TSSOP
PI90LVB180W	W	14-pin SOIC
PI90LVB180WE	W	Pb-free & Green, 14-pin SOIC
PI90LVB050L	L	16-pin TSSOP
PI90LVB050LE	L	Pb-free & Green, 16-pin TSSOP
PI90LVB050W	W	16-pin SOIC
PI90LVB050WE	W	Pb-free & Green, 16-pin SOIC
PI90LVB051L	L	16-pin TSSOP
PI90LVB051LE	L	Pb-free & Green, 16-pin TSSOP
PI90LVB051W	W	16-pin SOIC
PI90LVB051WE	W	Pb-free & Green, 16-pin SOIC

Notes:
1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/

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