

## Dual N-Channel 25 V (D-S) MOSFET

PRODUCT SUMMARY			
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A)	Q <sub>g</sub> (Typ.)
25	0.025 at V <sub>GS</sub> = 10 V	8 <sup>a</sup>	3.6 nC
	0.030 at V <sub>GS</sub> = 4.5 V	7.9	

### FEATURES

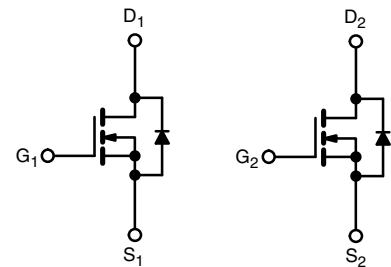
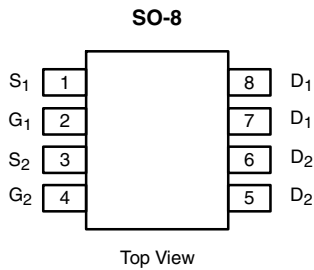
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET<sup>®</sup> Gen III Power MOSFET
- Compliant to RoHS Directive 2002/95/EC



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

### APPLICATIONS

- DC/DC Converter
  - Game Console
  - Notebook System Power



N-Channel MOSFET

N-Channel MOSFET

Ordering Information: Si4200DY-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C, unless otherwise noted)				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V <sub>DS</sub>	25	V	
Gate-Source Voltage	V <sub>GS</sub>	± 16		
Continuous Drain Current (T <sub>J</sub> = 150 °C)	I <sub>D</sub>	T <sub>C</sub> = 25 °C	8 <sup>a</sup>	A
		T <sub>C</sub> = 70 °C	6.9	
		T <sub>A</sub> = 25 °C	7.3 <sup>b, c</sup>	
		T <sub>A</sub> = 70 °C	5.8 <sup>b, c</sup>	
Pulsed Drain Current (t = 300 μs)	I <sub>DM</sub>	30		
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	2.3	
		T <sub>A</sub> = 25 °C	1.7 <sup>b, c</sup>	
Single Pulse Avalanche Current	I <sub>AS</sub>	12		
Single Pulse Avalanche Energy	E <sub>AS</sub>	7.2	mJ	
Maximum Power Dissipation	P <sub>D</sub>	T <sub>C</sub> = 25 °C	2.8	W
		T <sub>C</sub> = 70 °C	1.8	
		T <sub>A</sub> = 25 °C	2.0 <sup>b, c</sup>	
		T <sub>A</sub> = 70 °C	1.3 <sup>b, c</sup>	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>b, d</sup>	R <sub>thJA</sub>	58	62.5	°C/W
Maximum Junction-to-Foot (Drain)	R <sub>thJF</sub>	38	45	

Notes:

- Package limited.
- Surface mounted on 1" x 1" FR4 board.
- t = 10 s.
- Maximum under steady state conditions is 110 °C/W.

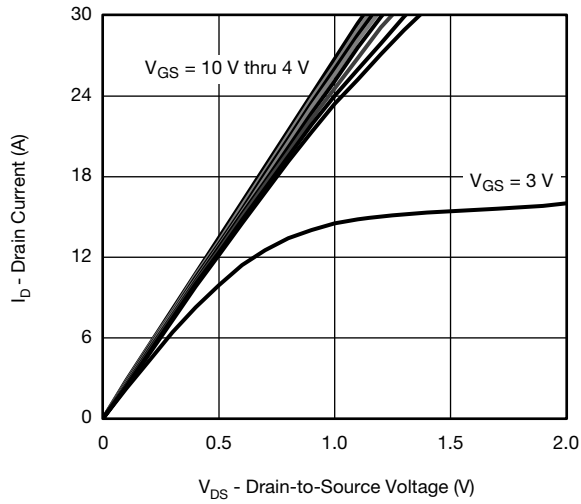
SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	25			V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		25		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$		-4.4			
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.0		2.2	V
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 16\text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
		$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			10	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	20			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 7.3\text{ A}$		0.020	0.025	$\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 6.7\text{ A}$		0.024	0.030	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 10\text{ V}, I_D = 7.3\text{ A}$		20		S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	$C_{ISS}$	$V_{DS} = 13\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		415		pF
Output Capacitance	$C_{OSS}$		96			
Reverse Transfer Capacitance	$C_{RSS}$		37			
Total Gate Charge	$Q_g$	$V_{DS} = 13\text{ V}, V_{GS} = 10\text{ V}, I_D = 7.3\text{ A}$		7.6	12	nC
		$V_{DS} = 13\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 7.3\text{ A}$		3.6	6	
Gate-Source Charge	$Q_{gs}$		1.3			
Gate-Drain Charge	$Q_{gd}$		0.9			
Gate Resistance	$R_g$	$f = 1\text{ MHz}$	0.8	4.1	8.2	$\Omega$
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 13\text{ V}, R_L = 2.2\text{ }\Omega$ $I_D \cong 5.8\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$		9	18	ns
Rise Time	$t_r$		10	20		
Turn-Off Delay Time	$t_{d(off)}$		9	18		
Fall Time	$t_f$		8	16		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 13\text{ V}, R_L = 2.2\text{ }\Omega$ $I_D \cong 5.8\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		3	6	
Rise Time	$t_r$		10	20		
Turn-Off Delay Time	$t_{d(off)}$		11	20		
Fall Time	$t_f$		8	16		
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$			2.3	A
Pulse Diode Forward Current	$I_{SM}$				30	
Body Diode Voltage	$V_{SD}$	$I_S = 5.8\text{ A}, V_{GS} = 0\text{ V}$		0.8	1.2	V
Body Diode Reverse Recovery Time	$t_{rr}$	$I_F = 5.8\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		17	26	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$		7	14	nC	
Reverse Recovery Fall Time	$t_a$		10		ns	
Reverse Recovery Rise Time	$t_b$		7			

Notes:

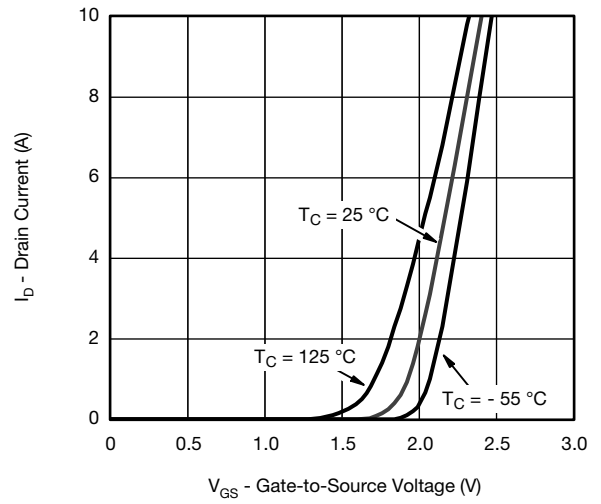
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .  
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

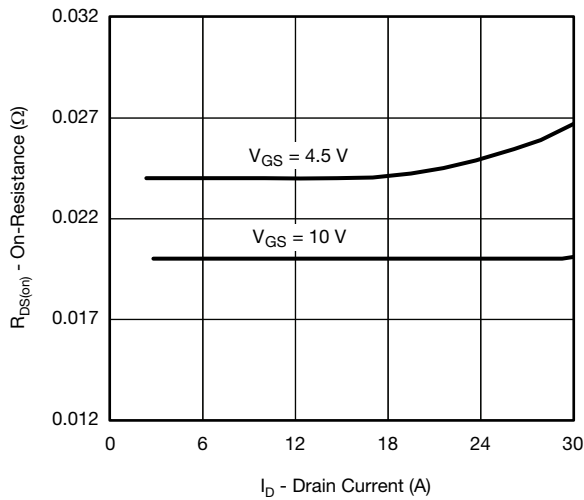
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



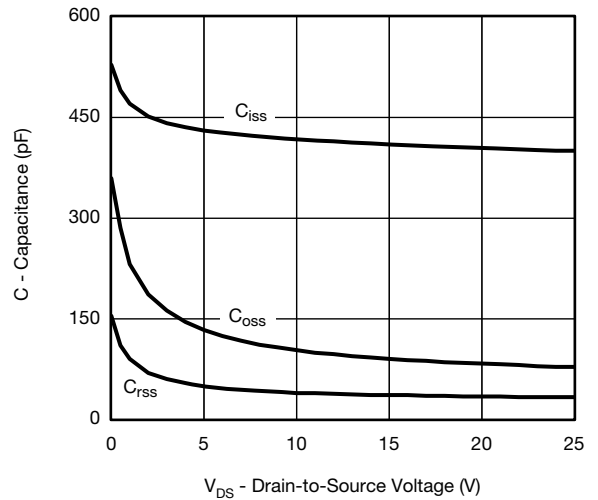
$V_{DS}$  - Drain-to-Source Voltage (V)  
**Output Characteristics**



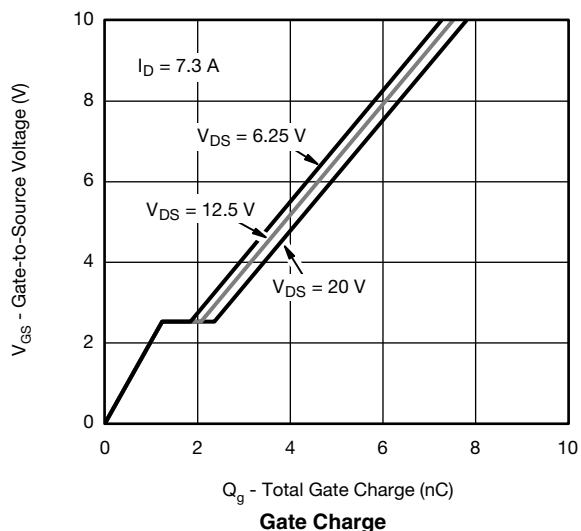
$V_{GS}$  - Gate-to-Source Voltage (V)  
**Transfer Characteristics**



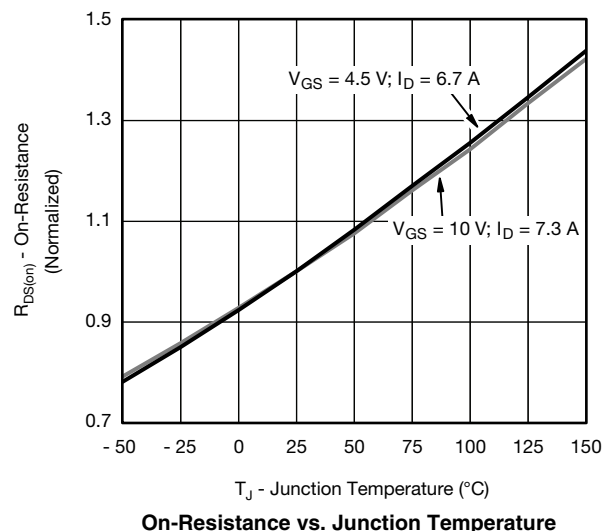
$I_D$  - Drain Current (A)  
**On-Resistance vs. Drain Current**



$V_{DS}$  - Drain-to-Source Voltage (V)  
**Capacitance**

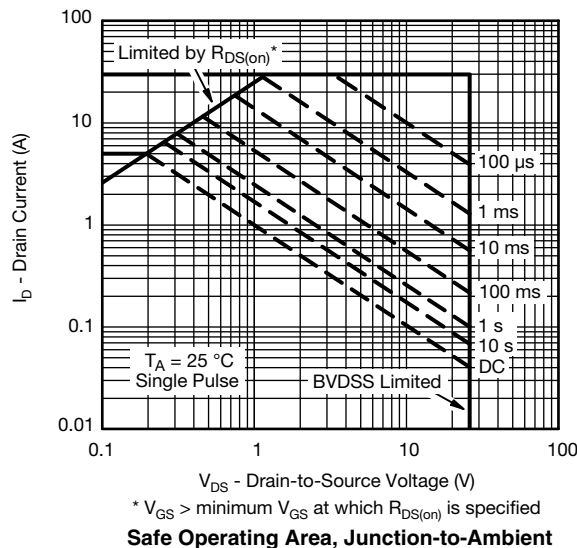
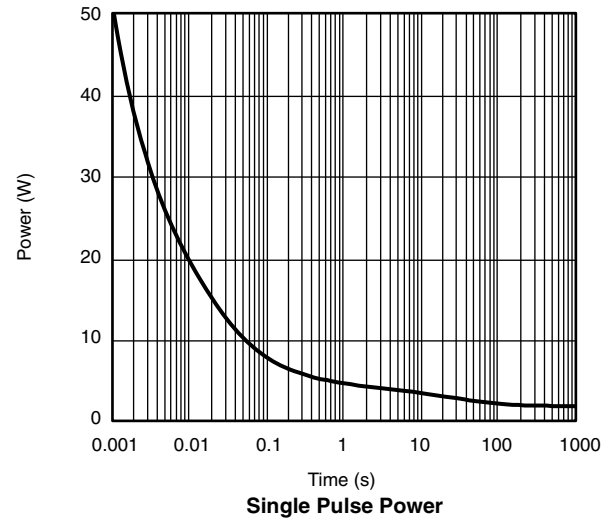
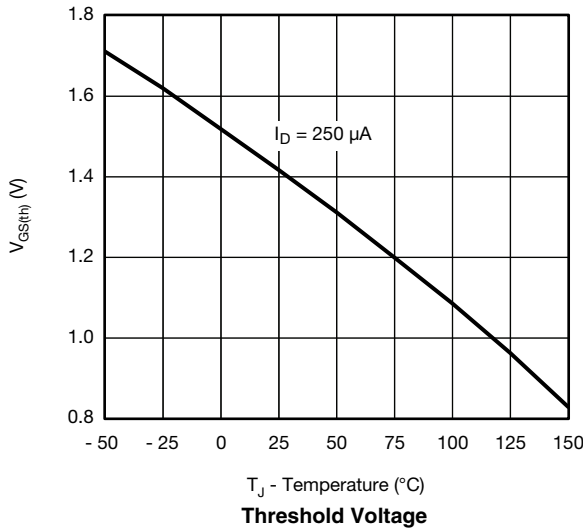
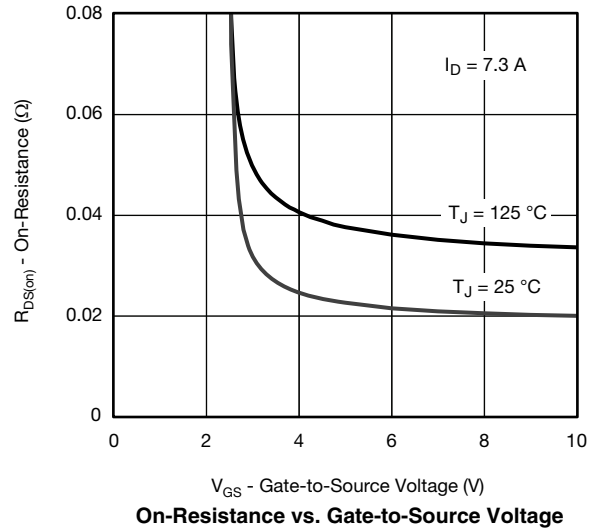
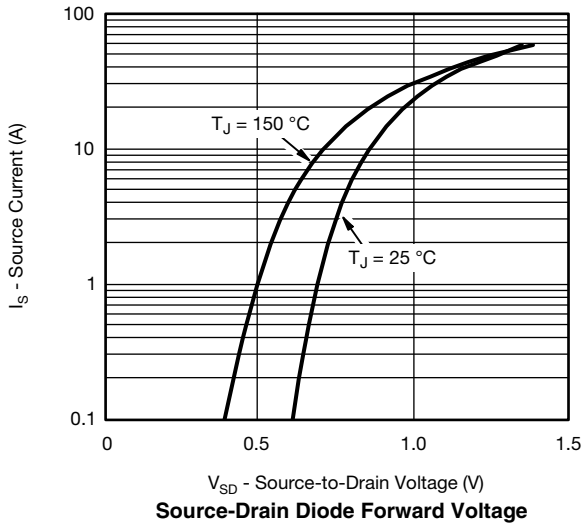


$Q_g$  - Total Gate Charge (nC)  
**Gate Charge**

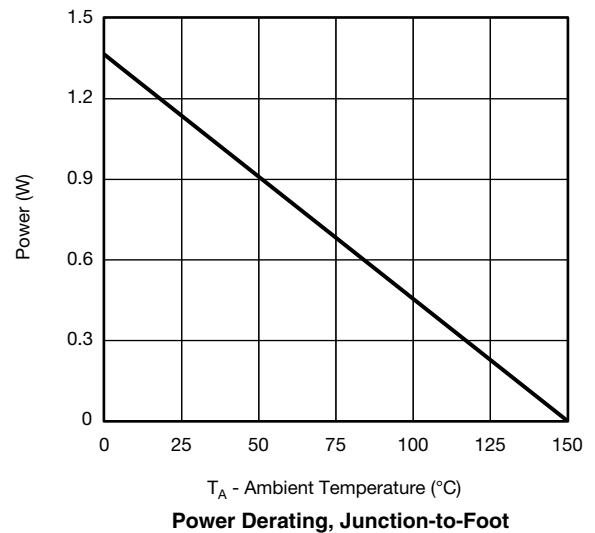
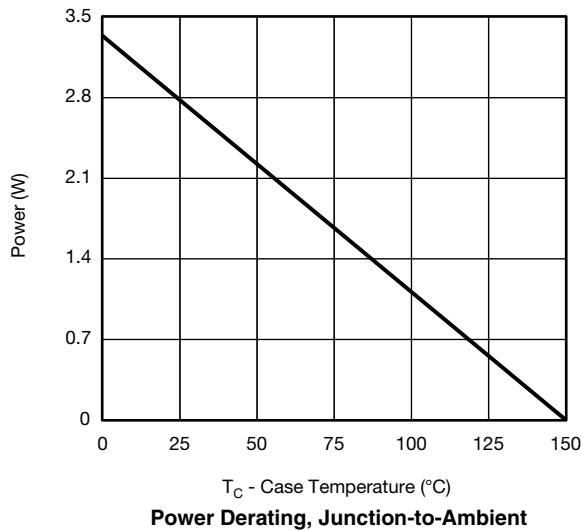
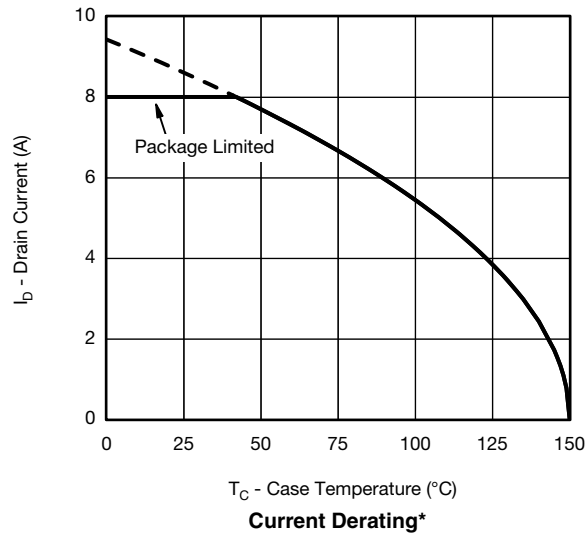


$T_J$  - Junction Temperature ( $^{\circ}\text{C}$ )  
**On-Resistance vs. Junction Temperature**

## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

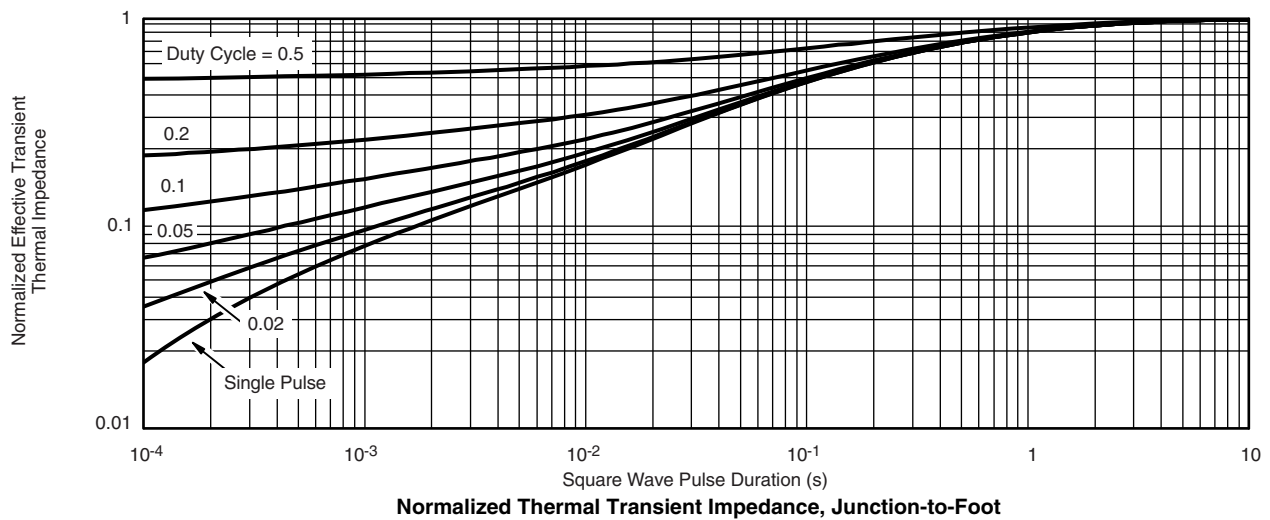
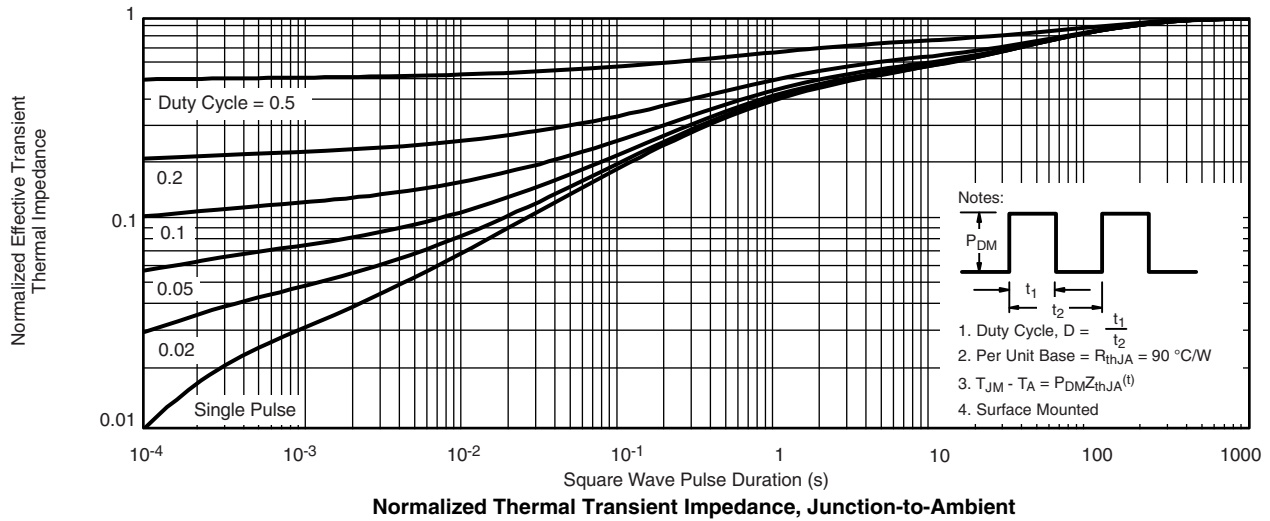


**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?66825](http://www.vishay.com/ppg?66825).

## SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A <sub>1</sub>	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				

## RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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