

BATTERY MONITORING IC FOR 1-CELL PACK

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Rev.1.0_02

The S-8259A Series is an IC including high-accuracy voltage detection circuits and delay circuits.

The S-8259A Series is suitable for monitoring overcharge and overdischarge for 1-cell lithium-ion / lithium polymer rechargeable battery packs.

■ Features

- High-accuracy voltage detection circuit

Overcharge detection voltage	3.5 V to 4.6 V (5 mV step)	Accuracy ±20 mV
Overcharge release voltage	3.1 V to 4.6 V* ¹	Accuracy ±50 mV
Overdischarge detection voltage	2.0 V to 3.4 V (10 mV step)	Accuracy ±50 mV
Overdischarge release voltage	2.0 V to 3.4 V* ²	Accuracy ±100 mV
- Detection delay times are generated only by an internal circuit (external capacitors are unnecessary).
- Wide operation temperature range: Ta = -40°C to +85°C
- Low current consumption

During operation:	1.5 μA typ., 3.0 μA max. (Ta = +25°C)
During overdischarge:	2.0 μA max. (Ta = +25°C)
- Lead-free (Sn 100%), halogen-free

*1. Overcharge release voltage = Overcharge detection voltage – Overcharge hysteresis voltage
(Overcharge hysteresis voltage can be selected from a range of 0 V to 0.4 V in 50 mV step.)

*2. Overdischarge release voltage = Overdischarge detection voltage + Overdischarge hysteresis voltage
(Overdischarge hysteresis voltage can be selected from a range of 0.1 V to 0.7 V in 100 mV step.)

■ Applications

- Lithium-ion rechargeable battery pack
- Lithium polymer rechargeable battery pack

■ Package

- SOT-23-6

■ **Block Diagram**

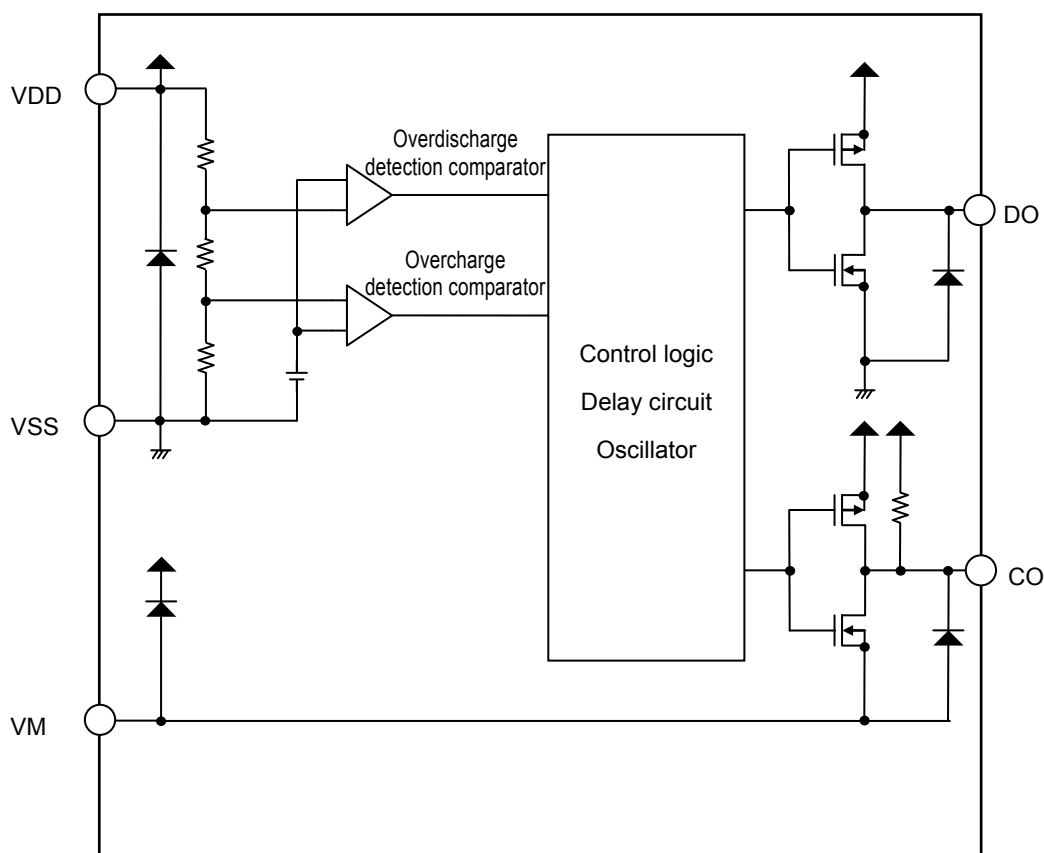
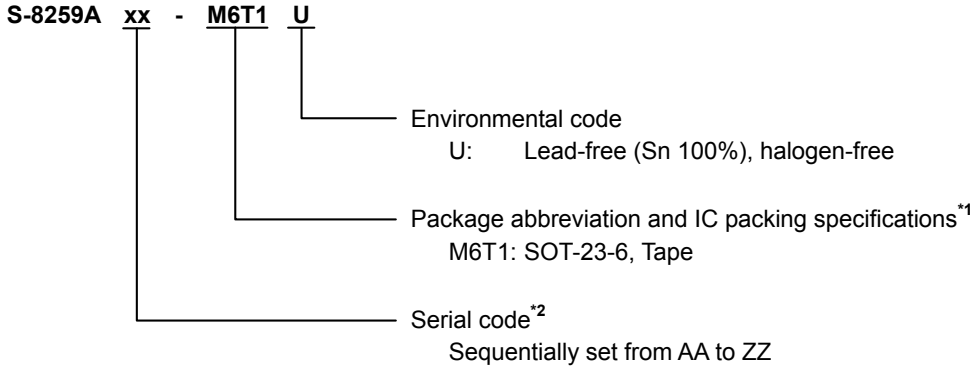


Figure 1

■ Product Name Structure

1. Product name



- *1. Refer to the tape drawing.
- *2. Refer to "3. Product name list".

2. Package

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel
SOT-23-6	MP006-A-P-SD	MP006-A-C-SD	MP006-A-R-SD

3. Product name list

Table 2

Product Name	Overcharge Detection Voltage [V _{cu}]	Overcharge Release Voltage [V _{cl}]	Overdischarge Detection Voltage [V _{dl}]	Overdischarge Release Voltage [V _{du}]	Overcharge Detection Delay Time [t _{cu}]	Overcharge Release Delay Time [t _{cl}]	Overdischarge Detection Delay Time [t _{dl}]
S-8259AAA-M6T1U	4.275 V	4.175 V	2.300 V	2.600 V	1.0 s	32 ms	128 ms
S-8259AAB-M6T1U	4.250 V	4.100 V	2.500 V	3.000 V	1.0 s	128 ms	256 ms
S-8259AAC-M6T1U	3.900 V	3.800 V	2.000 V	2.300 V	1.0 s	32 ms	128 ms
S-8259AAD-M6T1U	4.200 V	4.100 V	2.500 V	3.000 V	256 ms	2.0 s	32 ms
S-8259AAE-M6T1U	4.200 V	4.200 V	2.800 V	3.000 V	1.0 s	4.0 s	256 ms

- Remark 1.** Please contact our sales office for the products with detection voltage value other than those specified above.
- 2.** The delay times can be changed within the range listed in **Table 3**. For details, please contact our sales office.

Table 3

Delay Time	Symbol	Selection Range						Remark
Overcharge detection delay time	t _{cu}	128 ms	256 ms	512 ms	1.0 s	2.0 s	4.0 s	Select a value from the left.
Overcharge release delay time	t _{cl}	32 ms	64 ms	128 ms	1.0 s	2.0 s	4.0 s	Select a value from the left.
overdischarge detection delay time	t _{dl}	32 ms	64 ms	128 ms	256 ms	–	–	Select a value from the left.

■ **Pin Configuration**

1. SOT-23-6

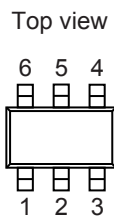


Figure 2

Table 4

Pin No.	Symbol	Description
1	DO	Output pin for overdischarge detection (CMOS output)
2	VM	Negative power supply input pin for CO pin
3	CO	Output pin for overcharge detection (CMOS output)
4	NC*1	No connection
5	VDD	Input pin for positive power supply
6	VSS	Input pin for negative power supply

*1. The NC pin is electrically open.
 The NC pin can be connected to VDD pin or VSS pin.

■ Absolute Maximum Ratings

Table 5

(Ta = +25°C unless otherwise specified)

Item	Symbol	Applied Pin	Absolute Maximum Rating	Unit
Input voltage between VDD pin and VSS pin	V _{DS}	VDD	V _{SS} - 0.3 to V _{SS} + 6	V
VM pin input voltage	V _{VM}	VM	V _{DD} - 28 to V _{DD} + 0.3	V
DO pin output voltage	V _{DO}	DO	V _{SS} - 0.3 to V _{DD} + 0.3	V
CO pin output voltage	V _{CO}	CO	V _{VM} - 0.3 to V _{DD} + 0.3	V
Power dissipation	P _D	—	650*1	mW
Operation ambient temperature	T _{opr}	—	-40 to +85	°C
Storage temperature	T _{stg}	—	-55 to +125	°C

*1. When mounted on board
[Mounted board]

- (1) Board size: 114.3 mm × 76.2 mm × t1.6 mm
- (2) Board name: JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

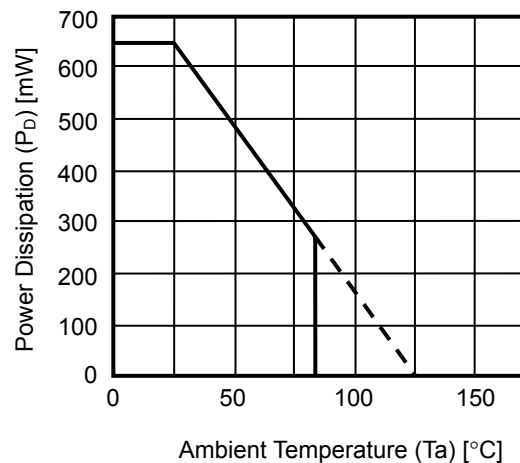


Figure 3 Power Dissipation of Package (When Mounted on Board)

■ **Electrical Characteristics**

1. **Ta = +25°C**

Table 6

(Ta = +25°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Detection Voltage							
Overcharge detection voltage	V _{CU}	–	V _{CU} – 0.020	V _{CU}	V _{CU} + 0.020	V	1
		Ta = –10°C ~ +60°C*1	V _{CU} – 0.025	V _{CU}	V _{CU} + 0.025	V	1
Overcharge release voltage	V _{CL}	V _{CL} ≠ V _{CU}	V _{CL} – 0.050	V _{CL}	V _{CL} + 0.050	V	1
		V _{CL} = V _{CU}	V _{CL} – 0.025	V _{CL}	V _{CL} + 0.020	V	1
Overdischarge detection voltage	V _{DL}	–	V _{DL} – 0.050	V _{DL}	V _{DL} + 0.050	V	2
Overdischarge release voltage	V _{DU}	V _{DL} ≠ V _{DU}	V _{DU} – 0.100	V _{DU}	V _{DU} + 0.100	V	2
Input Voltage							
Operation voltage between VDD pin and VSS pin	V _{DSOP}	–	1.5	–	6.0	V	–
Input Current							
Current consumption during operation	I _{OPE}	V _{DD} = 3.4 V, V _{VM} = 0 V	–	1.5	3.0	μA	3
Current consumption during overdischarge	I _{OPED}	V _{DD} = 1.5 V, V _{VM} = 0 V	–	–	2.0	μA	3
Output Resistance							
CO pin resistance "H" 1	R _{COH1}	–	5	10	20	kΩ	4
CO pin resistance "L"	R _{COL}	–	5	10	20	kΩ	4
DO pin resistance "H"	R _{DOH}	–	5	10	20	kΩ	4
DO pin resistance "L"	R _{DOL}	–	5	10	20	kΩ	4
CO pin resistance "H" 2	R _{COH2}	–	1	4	–	MΩ	4
Delay Time							
Overcharge detection delay time	t _{CU}	–	t _{CU} × 0.7	t _{CU}	t _{CU} × 1.3	–	5
Overcharge release delay time	t _{CL}	–	t _{CL} × 0.7	t _{CL}	t _{CL} × 1.3	–	5
Overdischarge detection delay time	t _{DL}	–	t _{DL} × 0.7	t _{DL}	t _{DL} × 1.3	–	5

*1. Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

BATTERY MONITORING IC FOR 1-CELL PACK
S-8259A Series

Rev.1.0_02

2. Ta = -40°C to +85°C*1

Table 7

(Ta = -40°C to +85°C*1 unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Detection Voltage							
Overcharge detection voltage	V _{CU}	–	V _{CU} – 0.045	V _{CU}	V _{CU} + 0.030	V	1
Overcharge release voltage	V _{CL}	V _{CL} ≠ V _{CU}	V _{CL} – 0.080	V _{CL}	V _{CL} + 0.060	V	1
		V _{CL} = V _{CU}	V _{CL} – 0.050	V _{CL}	V _{CL} + 0.030	V	1
Overdischarge detection voltage	V _{DL}	–	V _{DL} – 0.080	V _{DL}	V _{DL} + 0.060	V	2
Overdischarge release voltage	V _{DU}	V _{DL} ≠ V _{DU}	V _{DU} – 0.130	V _{DU}	V _{DU} + 0.110	V	2
Input Voltage							
Operation voltage between VDD pin and VSS pin	V _{D SOP}	–	1.5	–	6.0	V	–
Input Current							
Current consumption during operation	I _{OP E}	V _{DD} = 3.4 V, V _{VM} = 0 V	–	1.5	4.0	μA	3
Current consumption during overdischarge	I _{OP ED}	V _{DD} = V _{VM} = 1.5 V	–	–	3.0	μA	3
Output Resistance							
CO pin resistance "H" 1	R _{COH1}	–	2.5	10	30	kΩ	4
CO pin resistance "L"	R _{COL}	–	2.5	10	30	kΩ	4
DO pin resistance "H"	R _{DOH}	–	2.5	10	30	kΩ	4
DO pin resistance "L"	R _{DOL}	–	2.5	10	30	kΩ	4
CO pin resistance "H" 2	R _{COH2}	–	0.5	4	–	MΩ	4
Delay Time							
Overcharge detection delay time	t _{CU}	–	t _{CU} × 0.5	t _{CU}	t _{CU} × 2.5	–	5
Overcharge release delay time	t _{CL}	–	t _{CL} × 0.5	t _{CL}	t _{CL} × 2.5	–	5
Overdischarge detection delay time	t _{DL}	–	t _{DL} × 0.5	t _{DL}	t _{DL} × 2.5	–	5

*1. Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

■ Test Circuits

Caution Unless otherwise specified, the output voltage levels "H" and "L" at CO pin (V_{CO}) are judged by $V_{VM} + 1.0$ V, and the output voltage levels "H" and "L" at DO pin (V_{DO}) are judged by $V_{SS} + 1.0$ V. Judge the CO pin level with respect to V_{VM} and the DO pin level with respect to V_{SS} .

1. Overcharge detection voltage, overcharge release voltage (Test circuit 1)

Overcharge detection voltage (V_{CU}) is defined as the voltage V_1 at which V_{CO} goes from "H" to "L" when the voltage V_1 is gradually increased from the starting condition of $V_1 = 3.4$ V. Overcharge release voltage (V_{CL}) is defined as the voltage V_1 at which V_{CO} goes from "L" to "H" when the voltage V_1 is then gradually decreased. Overcharge hysteresis voltage (V_{HC}) is defined as the difference between V_{CU} and V_{CL} .

2. Overdischarge detection voltage, overdischarge release voltage (Test circuit 2)

Overdischarge detection voltage (V_{DL}) is defined as the voltage V_1 at which V_{DO} goes from "H" to "L" when the voltage V_1 is gradually decreased from the starting condition of $V_1 = 3.4$ V. Overdischarge release voltage (V_{DU}) is defined as the voltage V_1 at which V_{DO} goes from "L" to "H" when the voltage V_1 is then gradually increased. Overdischarge hysteresis voltage (V_{HD}) is defined as the difference between V_{DU} and V_{DL} .

3. Current consumption during operation (Test circuit 3)

The current consumption during operation (I_{OPE}) is the current that flows through VDD pin (I_{DD}) under the set condition of $V_1 = 3.4$ V.

4. Current consumption during overdischarge (Test circuit 3)

The current consumption during overdischarge (I_{OPE_D}) is I_{DD} under the set condition of $V_1 = 1.5$ V.

5. CO pin resistance "H" 1 (Test circuit 4)

The CO pin resistance "H" 1 (R_{COH1}) is the resistance between VDD pin and CO pin under the set conditions of $V_1 = 3.4$ V, $V_3 = 3.0$ V.

6. CO pin resistance "L" (Test circuit 4)

The CO pin resistance "L" (R_{COL}) is the resistance between VM pin and CO pin under the set conditions of $V_1 = 4.7$ V, $V_3 = 0.4$ V.

7. DO pin resistance "H" (Test circuit 4)

The DO pin resistance "H" (R_{DOH}) is the resistance between VDD pin and DO pin under the set conditions of $V_1 = 3.4$ V, $V_4 = 3.0$ V.

8. DO pin resistance "L" (Test circuit 4)

The DO pin resistance "L" (R_{DOL}) is the resistance between VSS pin and DO pin under the set conditions of $V_1 = 1.8$ V, $V_4 = 0.4$ V.

9. CO pin resistance "H" 2 (Test circuit 4)

The CO pin resistance "H" 2 (R_{COH2}) is the resistance between VDD pin and CO pin under the set conditions of $V_1 = 4.7$ V, $V_3 = 0$ V.

**10. Overcharge detection delay time
(Test circuit 5)**

The overcharge detection delay time (t_{CU}) is the time needed for V_{CO} to go to "L" just after the voltage $V1$ increases and exceeds V_{CU} under the set condition of $V1 = 3.4$ V.

**11. Overcharge release delay time
(Test circuit 5)**

The overcharge release delay time (t_{CL}) is the time needed for V_{CO} to go to "H" just after the voltage $V1$ decreases and falls below V_{CL} under the set condition of $V1 = 4.7$ V.

**12. Overdischarge detection delay time
(Test circuit 5)**

The overdischarge detection delay time (t_{DL}) is the time needed for V_{DO} to go to "L" after the voltage $V1$ decreases and falls below V_{DL} under the set condition of $V1 = 3.4$ V.

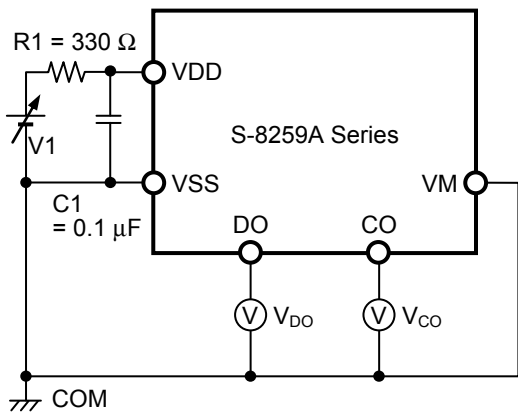


Figure 4 Test Circuit 1

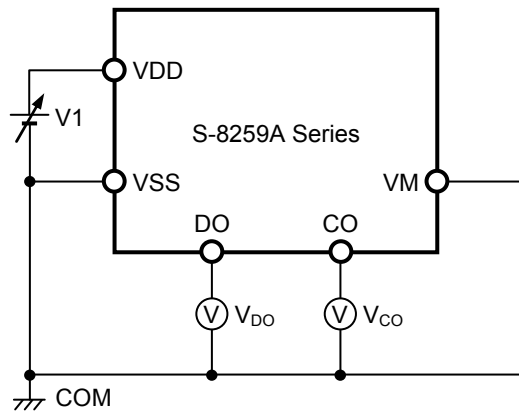


Figure 5 Test Circuit 2

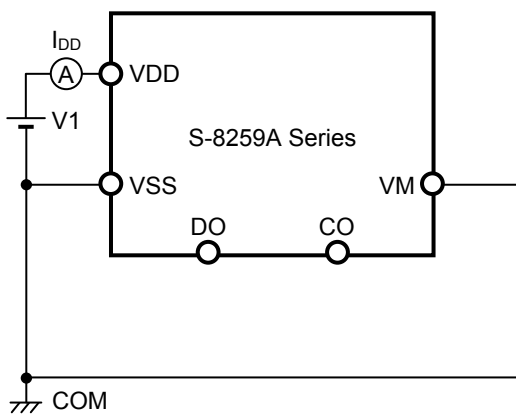


Figure 6 Test Circuit 3

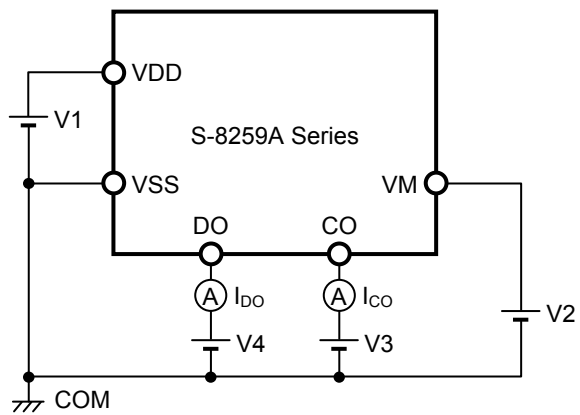


Figure 7 Test Circuit 4

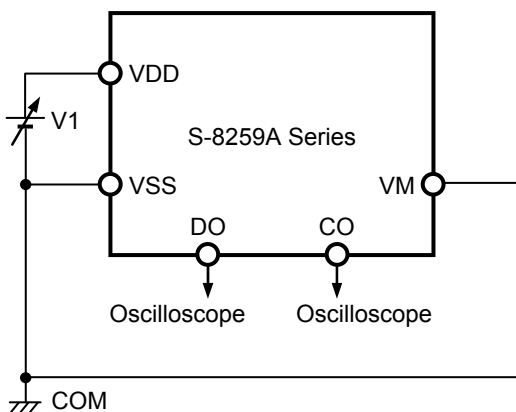


Figure 8 Test Circuit 5

■ Operation

Remark Refer to "■ Connection Example".

1. Normal status

The S-8259A Series monitors the voltage of the battery connected between VDD pin and VSS pin to control charging and discharging. When the battery voltage is in the range from overdischarge detection voltage (V_{DL}) to overcharge detection voltage (V_{CU}), CO pin and DO pin both output the VDD pin level. This condition is called the normal status.

2. Overcharge status

When the battery voltage becomes higher than V_{CU} during charging in the normal status and the condition continues for the overcharge detection delay time (t_{CU}) or longer, CO pin outputs the VM pin level. This condition is called the overcharge status.

When the battery voltage falls below the overcharge release voltage (V_{CL}) and the condition continues for the overcharge release delay time (t_{CL}) or longer, the S-8259A Series releases the overcharge status.

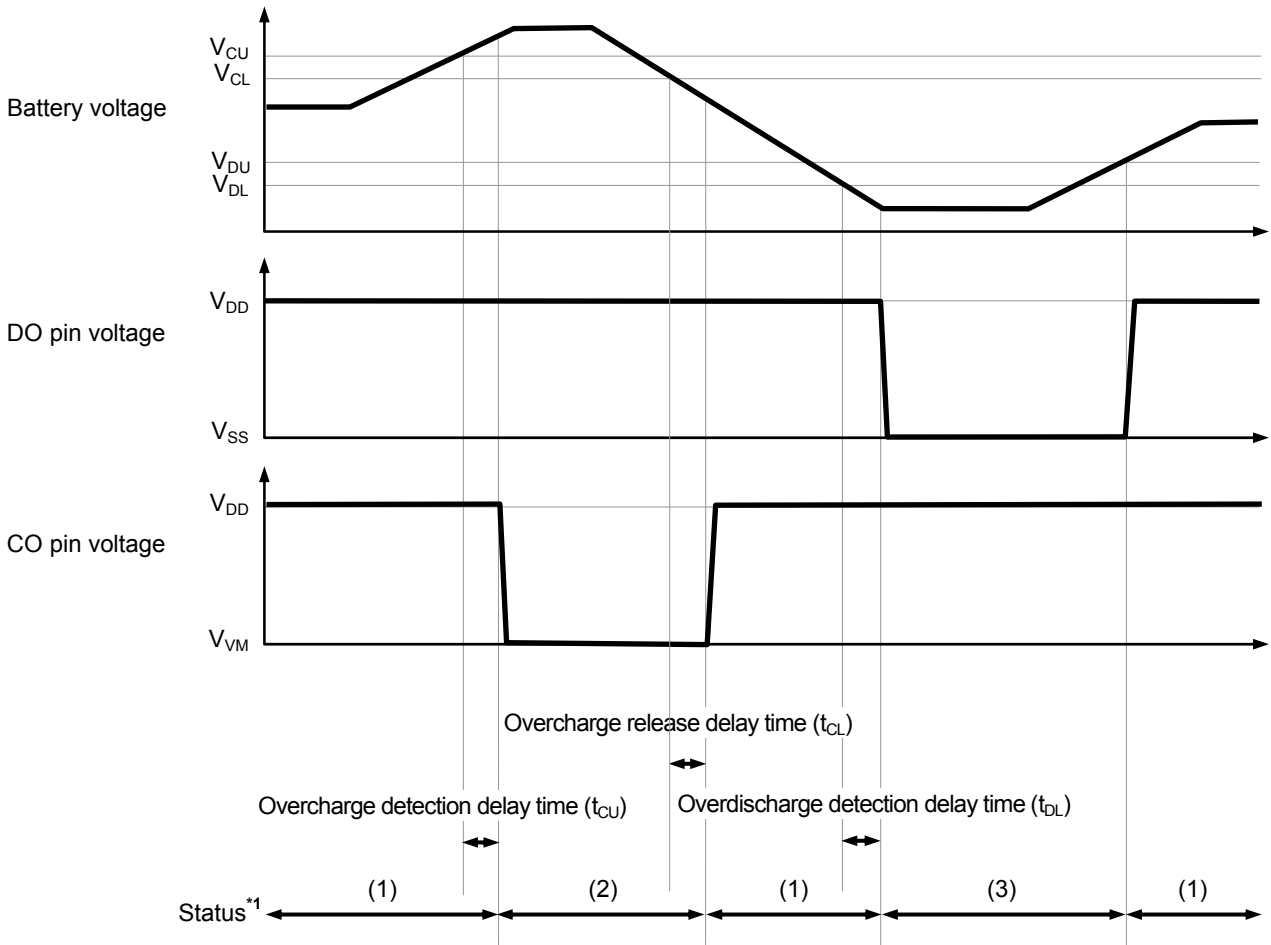
3. Overdischarge status

When the battery voltage falls below V_{DL} during discharging in the normal status and the condition continues for the overdischarge detection delay time (t_{DL}) or longer, DO pin outputs the VSS pin level. This condition is called the overdischarge status.

When the battery voltage exceeds the overdischarge release voltage (V_{DU}), the S-8259A Series releases the overdischarge status.

■ **Timing Chart**

1. **Overcharge detection, overdischarge detection**



- *1. (1): Normal status
- (2): Overcharge status
- (3): Overdischarge status

Figure 9

■ Connection Example

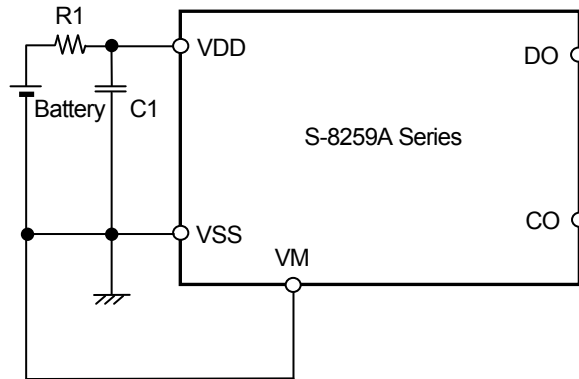


Figure 10

Table 8 Constants for External Components

Symbol	Part	Purpose	Min.	Typ.	Max.	Remark
R1	Resistor	ESD protection, For power fluctuation	150 Ω	330 Ω	1 k Ω	–
C1	Capacitor	For power fluctuation	0.068 μF	0.1 μF	1.0 μF	–

Caution 1. The above constants may be changed without notice.

2. It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection. In addition, the example of connection shown above and the constant do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constant.

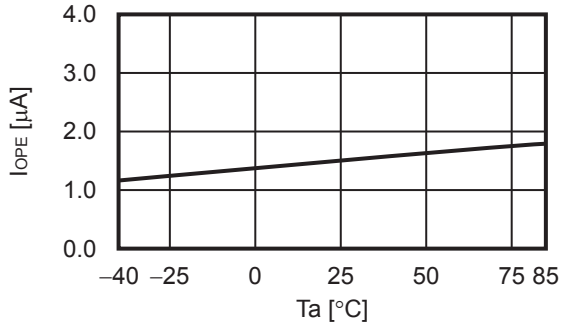
■ **Precautions**

- The application conditions for the input voltage, output voltage, and load current should not exceed the package power dissipation.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- SII Semiconductor Corporation claims no responsibility for any and all disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

■ Characteristics (Typical Data)

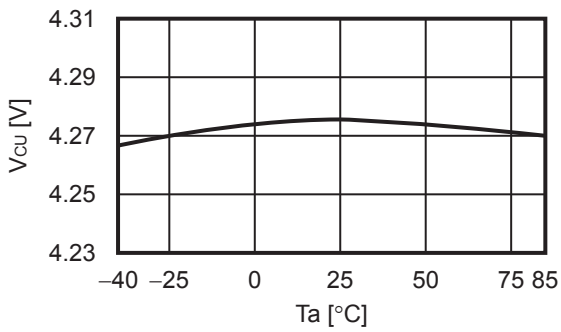
1. Current consumption

1.1 I_{OPE} vs. T_a

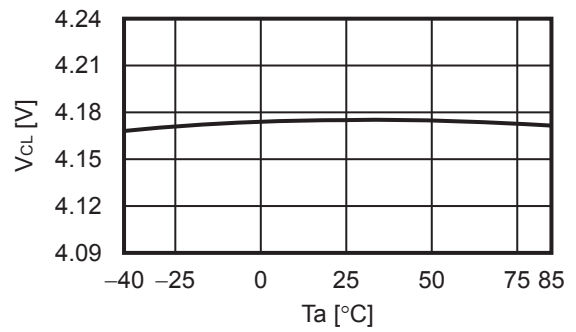


2. Detection voltage

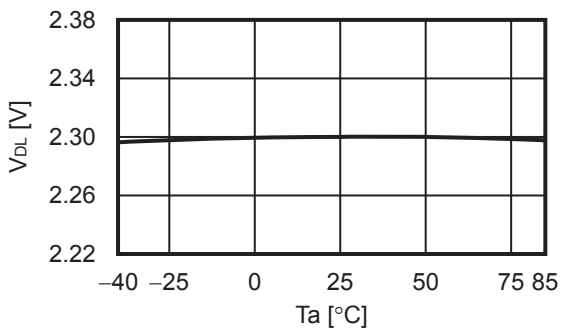
2.1 V_{CU} vs. T_a



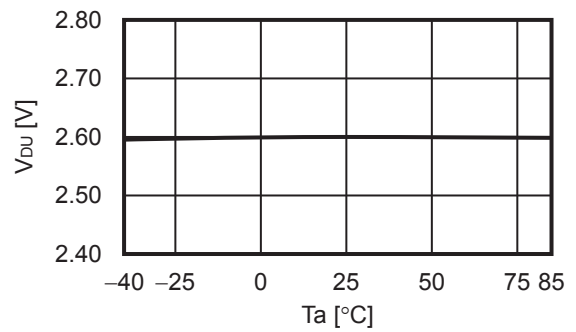
2.2 V_{CL} vs. T_a



2.3 V_{DL} vs. T_a

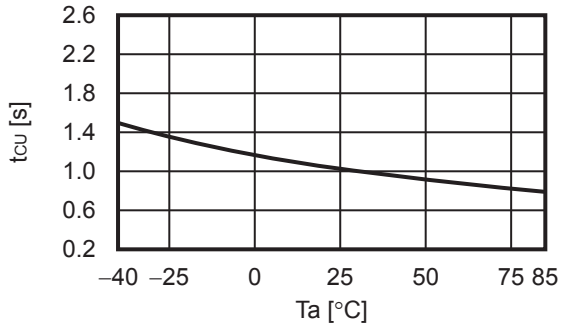


2.4 V_{DU} vs. T_a

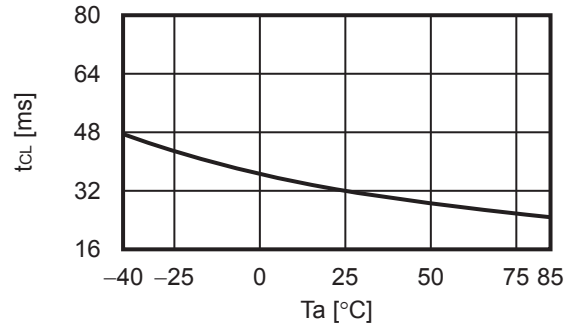


3. Delay time

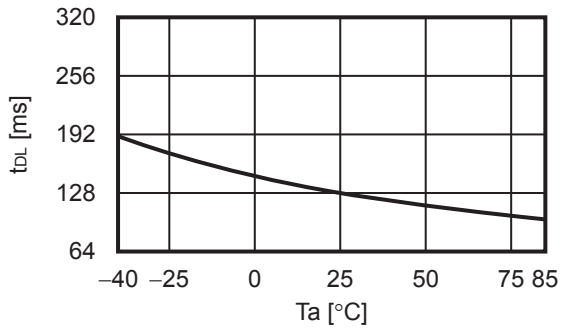
3.1 t_{CU} vs. T_a



3.2 t_{CL} vs. T_a

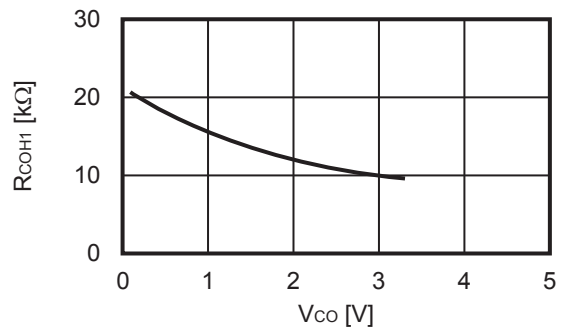


3.3 t_{DL} vs. T_a

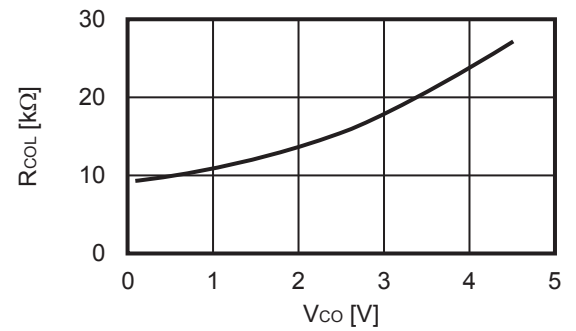


4. Output resistance

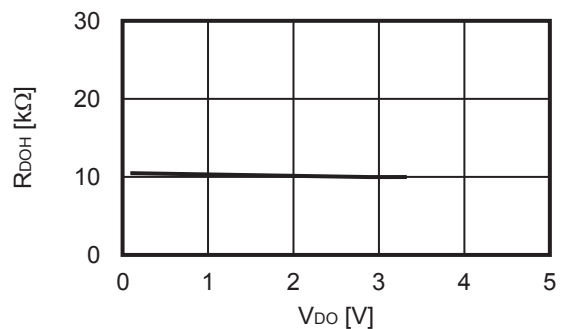
4.1 R_{COH1} vs. V_{CO}



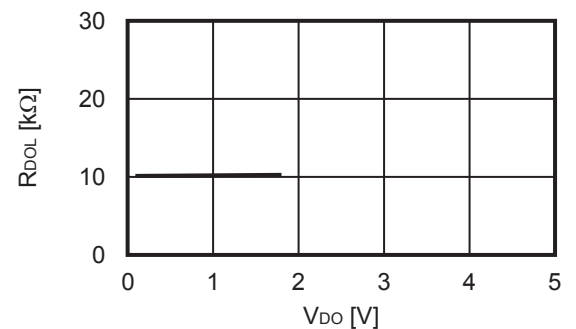
4.2 R_{COL} vs. V_{CO}



4.3 R_{DOH} vs. V_{DO}

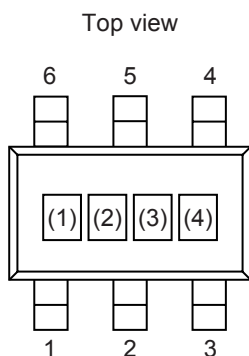


4.4 R_{DOL} vs. V_{DO}



■ Marking Specifications

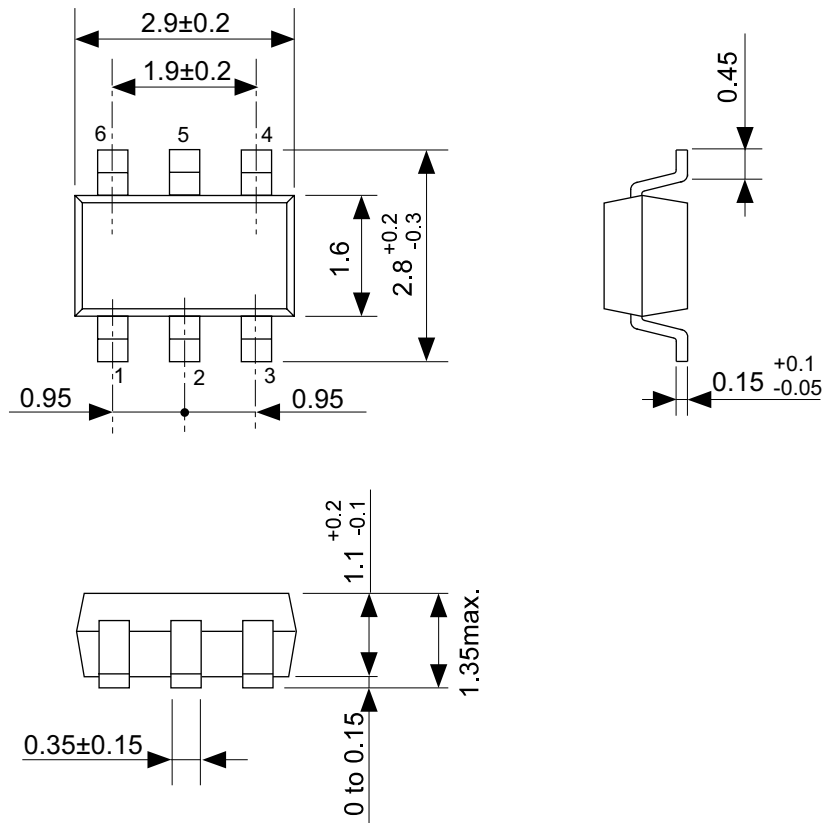
1. SOT-23-6



(1) to (3): Product code (refer to **Product name vs. Product code**)
(4): Lot number

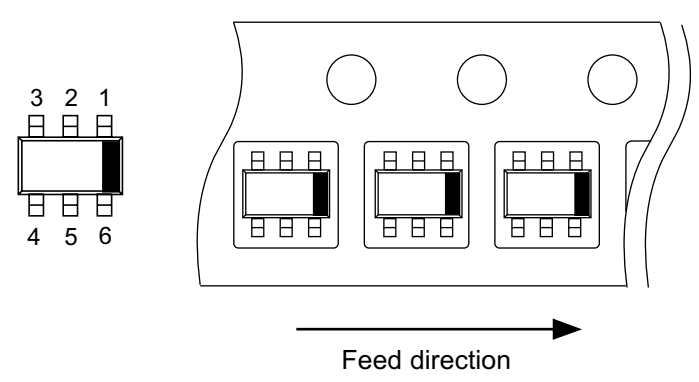
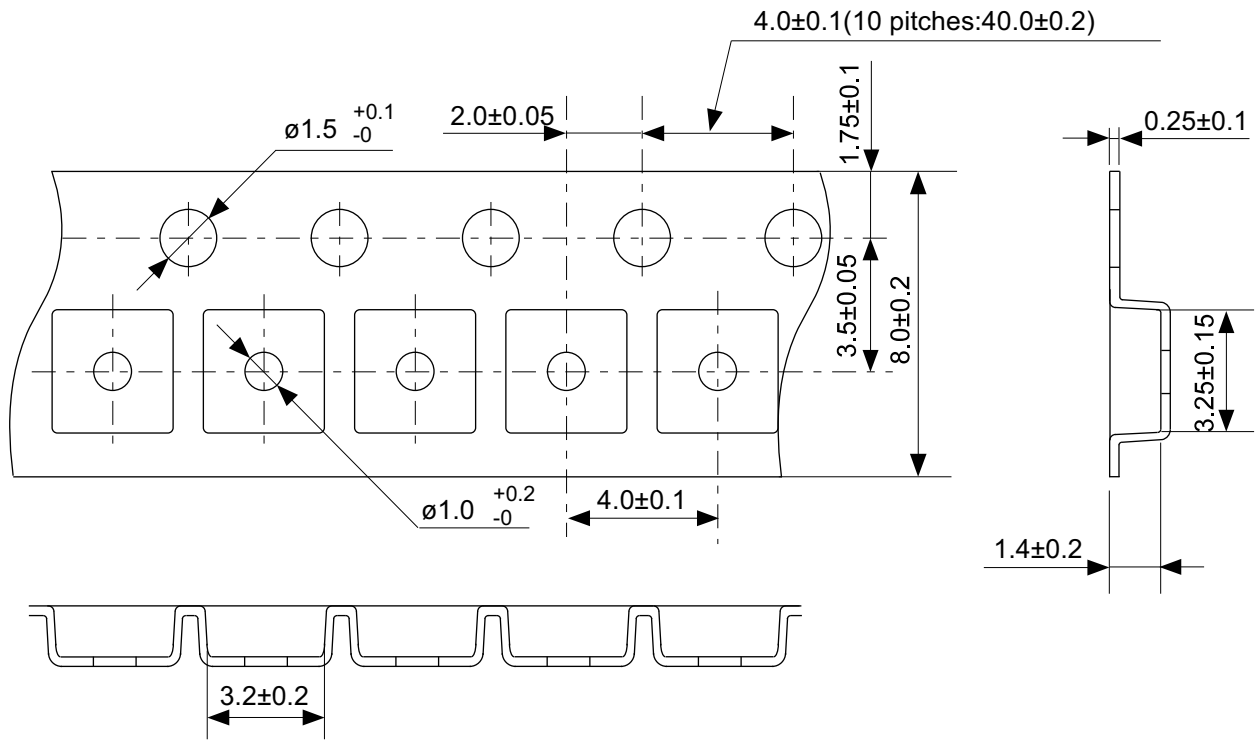
Product name vs. Product code

Product Name	Product Code		
	(1)	(2)	(3)
S-8259AAA-M6T1U	H	5	A
S-8259AAB-M6T1U	H	5	B
S-8259AAC-M6T1U	H	5	C
S-8259AAD-M6T1U	H	5	D
S-8259AAE-M6T1U	H	5	E



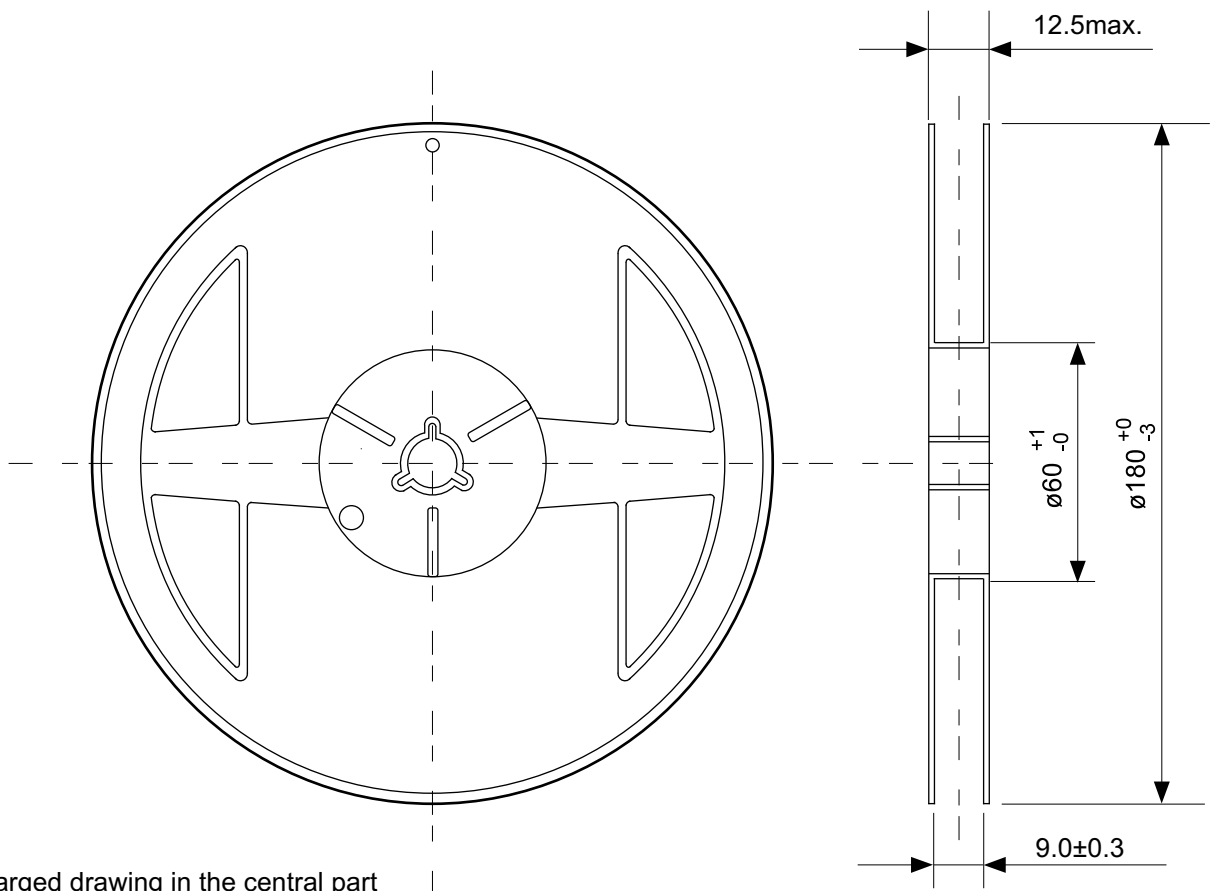
No. MP006-A-P-SD-2.0

TITLE	SOT236-A-PKG Dimensions
No.	MP006-A-P-SD-2.0
SCALE	
UNIT	mm
SII Semiconductor Corporation	

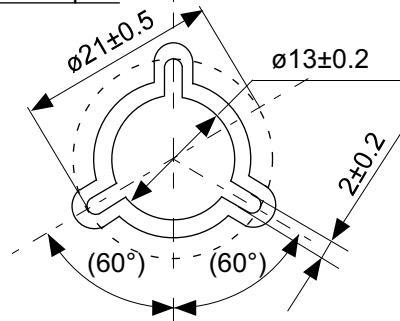


No. MP006-A-C-SD-3.1

TITLE	SOT236-A-Carrier Tape
No.	MP006-A-C-SD-3.1
SCALE	
UNIT	mm
SII Semiconductor Corporation	



Enlarged drawing in the central part



No. MP006-A-R-SD-2.1

TITLE	SOT236-A-Reel		
No.	MP006-A-R-SD-2.1		
SCALE		QTY	3,000
UNIT	mm		
SII Semiconductor Corporation			

Disclaimers (Handling Precautions)

1. All the information described herein (product data, specifications, figures, tables, programs, algorithms and application circuit examples, etc.) is current as of publishing date of this document and is subject to change without notice.
2. The circuit examples and the usages described herein are for reference only, and do not guarantee the success of any specific mass-production design.
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4. Take care to use the products described herein within their specified ranges. Pay special attention to the absolute maximum ratings, operation voltage range and electrical characteristics, etc.
SII Semiconductor Corporation is not responsible for damages caused by failures and/or accidents, etc. that occur due to the use of products outside their specified ranges.
5. When using the products described herein, confirm their applications, and the laws and regulations of the region or country where they are used and verify suitability, safety and other factors for the intended use.
6. When exporting the products described herein, comply with the Foreign Exchange and Foreign Trade Act and all other export-related laws, and follow the required procedures.
7. The products described herein must not be used or provided (exported) for the purposes of the development of weapons of mass destruction or military use. SII Semiconductor Corporation is not responsible for any provision (export) to those whose purpose is to develop, manufacture, use or store nuclear, biological or chemical weapons, missiles, or other military use.
8. The products described herein are not designed to be used as part of any device or equipment that may affect the human body, human life, or assets (such as medical equipment, disaster prevention systems, security systems, combustion control systems, infrastructure control systems, vehicle equipment, traffic systems, in-vehicle equipment, aviation equipment, aerospace equipment, and nuclear-related equipment), excluding when specified for in-vehicle use or other uses. Do not use those products without the prior written permission of SII Semiconductor Corporation. Especially, the products described herein cannot be used for life support devices, devices implanted in the human body and devices that directly affect human life, etc.
Prior consultation with our sales office is required when considering the above uses.
SII Semiconductor Corporation is not responsible for damages caused by unauthorized or unspecified use of our products.
9. Semiconductor products may fail or malfunction with some probability.
The user of these products should therefore take responsibility to give thorough consideration to safety design including redundancy, fire spread prevention measures, and malfunction prevention to prevent accidents causing injury or death, fires and social damage, etc. that may ensue from the products' failure or malfunction.
The entire system must be sufficiently evaluated and applied on customer's own responsibility.
10. The products described herein are not designed to be radiation-proof. The necessary radiation measures should be taken in the product design by the customer depending on the intended use.
11. The products described herein do not affect human health under normal use. However, they contain chemical substances and heavy metals and should therefore not be put in the mouth. The fracture surfaces of wafers and chips may be sharp. Take care when handling these with the bare hands to prevent injuries, etc.
12. When disposing of the products described herein, comply with the laws and ordinances of the country or region where they are used.
13. The information described herein contains copyright information and know-how of SII Semiconductor Corporation.
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14. For more details on the information described herein, contact our sales office.

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