



QorIQ™ P1021/P1012 Modular Development System (MDS)

The P1021/P1012 Modular Development System is designed for hardware and software developers using the P1021/P1012 QorIQ™ processor family to accelerate development and testing, and improve time to market. The P1021/P1012 MDS enables:

- Silicon bring-up/verification
- Software/application development and support
- Performance benchmarking
- Processor evaluation

The P1021/P1012 MDS consists of multiple boards that provide a comprehensive development system—a P1021/P1012 processor board, a platform I/O board and several expansion modules which add support for TDM and ATM.

P1021/P1012 Processor Board

The P1021/P1012 processor board includes a P1021 (dual-core) or P1012 (single-core) processor running up to 800 MHz, along with circuitry to utilize the following:

- 3x Gigabit Ethernet (GbE) and dual asynchronous receiver/transmitter (DUART)
- PCI Express® interconnect
- Serial RapidIO® technology
- USB 2.0
- Double data rate (DDR3 or optional DDR2) memory
- NAND flash memory
- SD/MMC card interface
- Real-time clock (RTC)
- Dual I²C interface
- Serial electrically erasable programmable read-only memory (EEPROM)
- Control switches and LED indicators
- Digital/analog regulated core voltage power supply (PS)
- Fully controlled onboard power supply subsystem

- Programmable reconfiguration through on-board CPLD mapped Board Configuration Registers Set (BCSR)
- JTAG interface to host PC

The P1021/P1012 MDS processor board's onboard resources and debugging devices allow developers to upload and run code, set breakpoints, display memory and register and connect proprietary hardware. It can also be used as a demonstration tool for the developer since the developer's application software may be programmed into the flash memory.

The P1021/P1012 processor board can be inserted into a PC as a PCI Express end point device. A 4-pin connector is provided to connect to the PC power supply. The PC power supply is not necessary. Other external connections are the same as in the stand-alone configuration.



PMC Expansion Modules

- PQ-MDS-T1—Supports E1/T1, DS3, T3 I/F with an option of two POTS analog telephone lines
- PQ-MDS-QOC3—Supports up to 4x 155 Mbps optical transceivers for evaluating the UTOPIA L2 /POS bus
- PQ-MDS-PCI—Single-slot PMC to PCI agent connector to enable additional PCI-based boards for evaluation (actual for MDSs with legacy PCI I/F functionality)
- PQ-MDS-PCI Express—Expansion module supporting multiple PCI Express agents

P1021/P1012 MDS Processor Board Features

- Supports both the P1021/P1012, running up to 800 MHz at 0.95V core voltage in a 689-pin TeBGA 1 mm pitch package
- DDR3 SODIMM @ 800 MHz, 512 MB with ECC support
- PCI Express adapter to provide root complex mode
- Dual 10/100 Mbps Ethernet ports for QUICC Engine™ module
- Three additional 10/100/1000 Mbps Ethernet ports from the platform
- Dual RS232 transceiver connected to DUART
- 2x LYNXx1 modules provide dual Serial RapidIO interface
- 4x LYNX connected to PCI Express adapter through PCI Express mux to support host or agent modes:
 - 4x PCI Express edge connector can be plugged in a PC
 - PCI Express adapter slot connector for root complex mode accepts standard (off-the-shelf) PCI Express, up to x4 cards
- Local bus I/F
 - Address latch, data (8-bit width) and control buffers to support slow devices on the PMC boards
 - 8-bit 32 MB NAND flash in a socket
 - CPLD BCSR
- Debug port access via JTAG/COP connector
- 16 MB flash on eSPI interface
- Two I²C buses
 - Bus for 256 KB boot EEPROM, 1 KB board related info EEPROM, RTC, SODIMM SPD EEPROM, core voltage POT and UEM configuration
- Two operation modes
 - Stand-alone mode
 - PCI Express end point mode—plugged into a PC as standard PC card
- QUICC Engine functions supported
 - All QUICC Engine signals are available on PMC0 and PMC1
 - 4x TDM port with the PQ-MDS-T1 card on the MDS (on PMC0 only)
 - 1x DS3 port with the PQ-MDS-T1 card on the MDS (on PMC0 only)
 - 1x UTOPIA/POS Level 2, 8-bit, multi-PHY multi device with PQ-MDS-QOC3 cards on the MDS (on PMC1 only)
 - 2x 10/100 Mbps RMII Ethernet ports
- 3x 1000 Mbps RGMII/RTBI (2x SGMII) Ethernet ports on the PB
- RoHS compliant
- FCC compliant
- CE compliant

P1021/P1012 Processor Board

Characteristics	Specifications
• Power requirements	◦ 5V @ 8A external DC power supply
• P1021/P1012 processor	◦ Internal clock runs up to 800 MHz @ 0.95V
• Memory	◦ 512 MB (with ECC support) SODIMM ◦ DDR3 at up to 800 MHz data rate
• Local bus: flash memory	◦ 8-bit 32 MB NAND flash in a socket
• Dimensions	◦ Length 312 mm, width 111 mm, height 50 mm max

CodeWarrior® Development Support

- Development Tools Linux® OS 2.6, supporting DUART, local bus, DDR, flash, TSEC, I²C, PCI Express (root complex and end point) and SPI

Typical Applications for the QorIQ P1021/P1012 Processors

- Access Gateway (IPv4 forwarding/security)
- SMB/SME applications
- Multi-service routers
- Industrial networking

About the QorIQ P1021/P1012 Processor

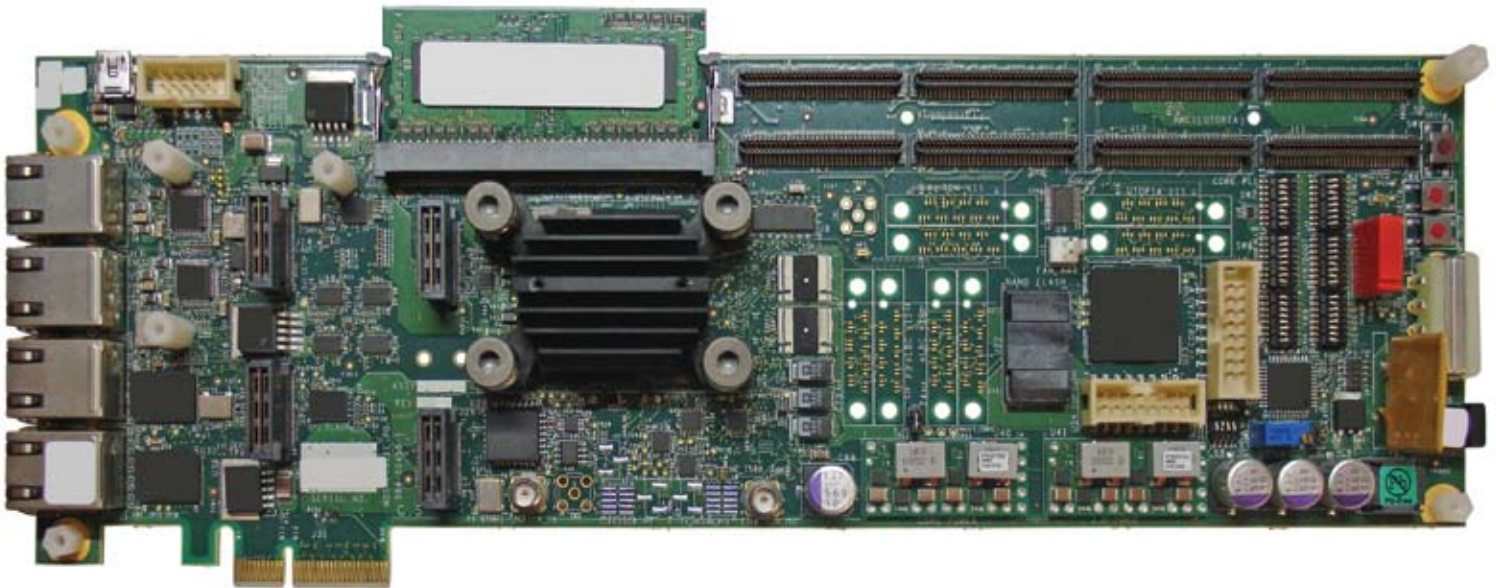
Freescale QorIQ communications platforms are the next-generation evolution of our leading PowerQUICC® communications processors. Built using high-performance cores built on Power Architecture® technology, QorIQ platforms enable a new era of networking innovation where the reliability, security and quality of service for every connection matters.

The QorIQ P1 platform series, which includes the P1021 and P1012 communications processors, offers the value of extensive integration and extreme power intelligence for a wide variety of applications in the networking, telecom, defense and industrial markets. Based on 45 nm technology for low-power implementation, the P1012 and

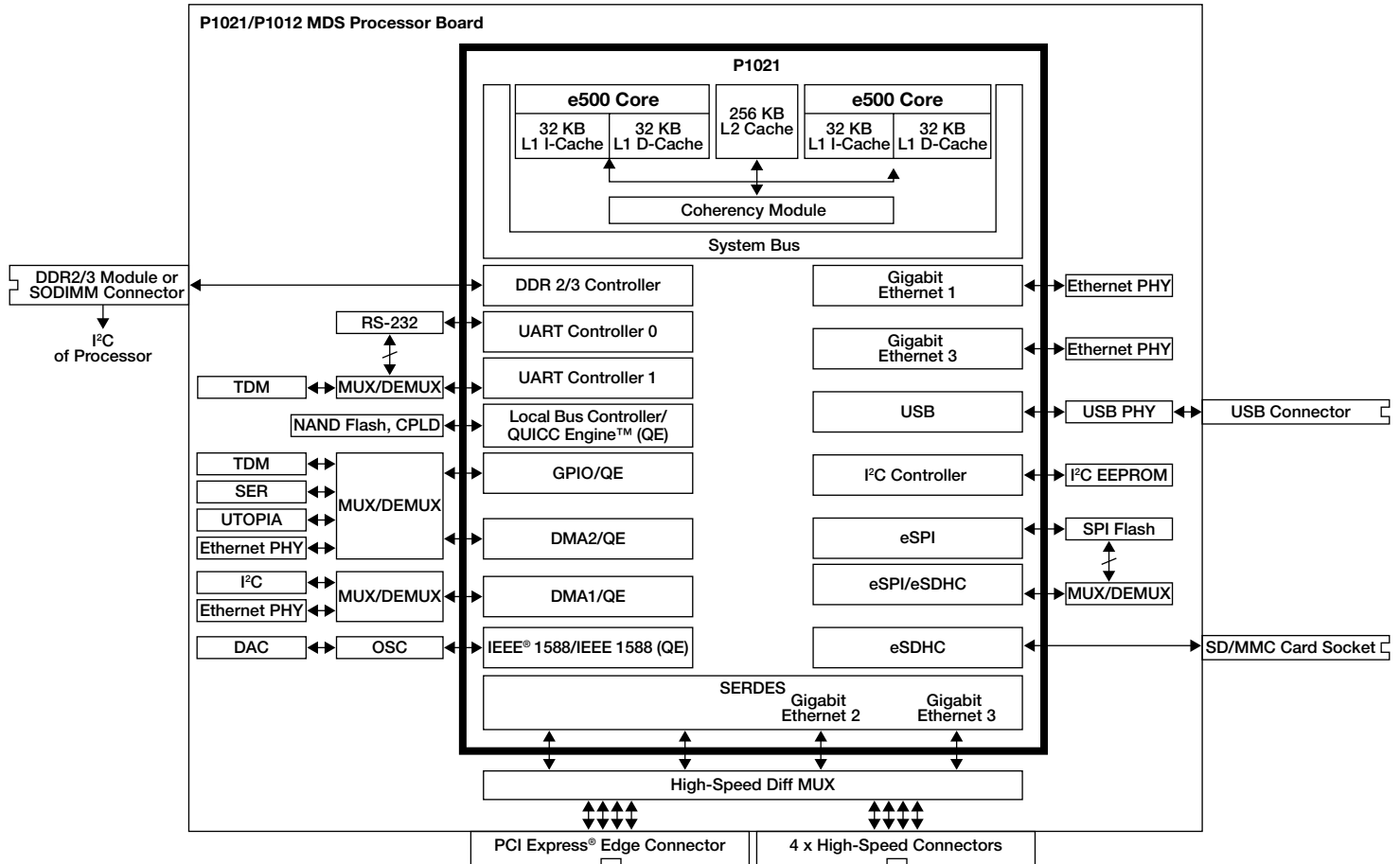
P1021 processors provide single- and dual-core solutions for the 533 MHz to 800 MHz performance range, along with advanced security and a rich set of interfaces.

The P1012 and P1021 processors are perfectly suited for multi-service gateways, Ethernet switch controllers, wireless LAN access points and high-performance general purpose control processor applications with tight thermal constraints.

The QorIQ P1012 and P1021 processors are pin-compatible with the QorIQ P2 platform products, offering a four-chip range of cost-effective solutions. Scaling from a single core at 533 MHz (P1011) to a dual core at 1.2 GHz per core (P2020), the two QorIQ platforms deliver an impressive 4.5x aggregate frequency range.



P1021/P1012 MDS Block Diagram



■ Freescale Technology

The devices in these two platforms are software compatible, sharing the e500 Power Architecture core and peripherals, as well as being fully software compatible with the existing PowerQUICC processors. This enables you to create a product with multiple performance points from a single board design. The QorIQ P1020 dual-core processor supports symmetric and asymmetric processing, enabling you to

further integrate your design with the same applications running on each core or serialize your application using the cores for different processing tasks.

The P1012 and P1021 processors have an advanced set of features for ease of use. The 256 KB L2 cache offers incremental configuration to partition the cache between the two cores or to configure it as SRAM or

stashing memory. The integrated security engine supports the cryptographic algorithms commonly used in IPsec, SSL, 3GPP and other networking and wireless security protocols. The memory controller offers future-proofing against memory technology migration with support for both DDR2 and DDR3. It also supports error correction codes, a baseline requirement for any high-reliability system.

Learn More:

For current information about Freescale products and documentation, please visit www.freescale.com/QorIQ.



Freescale and the Freescale logo are trademarks or registered trademarks of Freescale Semiconductor, Inc. in the U.S. and other countries. All other product or service names are the property of their respective owners. The Power Architecture and Power.org word marks and the Power and Power.org logos and related marks are trademarks and service marks licensed by Power.org. © Freescale Semiconductor, Inc. 2009.

Document Number: P1021MDSFS
REV 0

