PIC12F529T48A/T39A

PIC12F529T48A/T39A Memory Programming Specification

This document includes the programming specifications for the following devices:

- PIC12F529T48A
- PIC12F529T39A

1.0 PROGRAMMING THE PIC12F529T48A AND PIC12F529T39A

The PIC12F529T48A and PIC12F529T39A are programmed using a serial method. The Serial mode will allow the PIC12F529T48A and PIC12F529T39A to be programmed while in the user's system. This allows for increased design flexibility. This programming specification applies to the PIC12F529T48A and PIC12F529T39A devices in all packages.

1.1 Hardware Requirements

The PIC12F529T48A and PIC12F529T39A require one power supply for VDD (3.3V) and one for VPP (12.5V).

1.2 Program/Verify Mode

The Program/Verify mode for the PIC12F529T48A and PIC12F529T39A allows programming of user program memory, user ID locations, backup OSCCAL location and the Configuration Word.

FIGURE 1-1: 14-PIN DIAGRAM, PIC12F529T48A/PIC12F529T39A

TSSOP

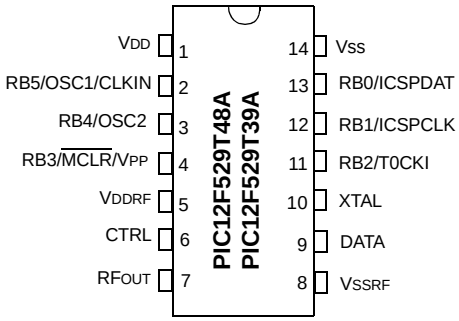


TABLE 1-1: PIN DESCRIPTIONS DURING PROGRAMMING

Pin Name	During Programming		
	Function	Pin Type	Pin Description
RB1	ICSPCLK	I	Clock input – Schmitt Trigger input
RB0	ICSPDAT	I/O	Data input/output – Schmitt Trigger input
$\overline{MCLR}$/VPP/RB3	Program/Verify mode	P(1)	Programming Power
VDD	VDD	P	Power Supply
VSS	VSS	P	Ground
VDDRF	VDDRF	P	Power Supply
VSSRF	VSSRF	P	Ground

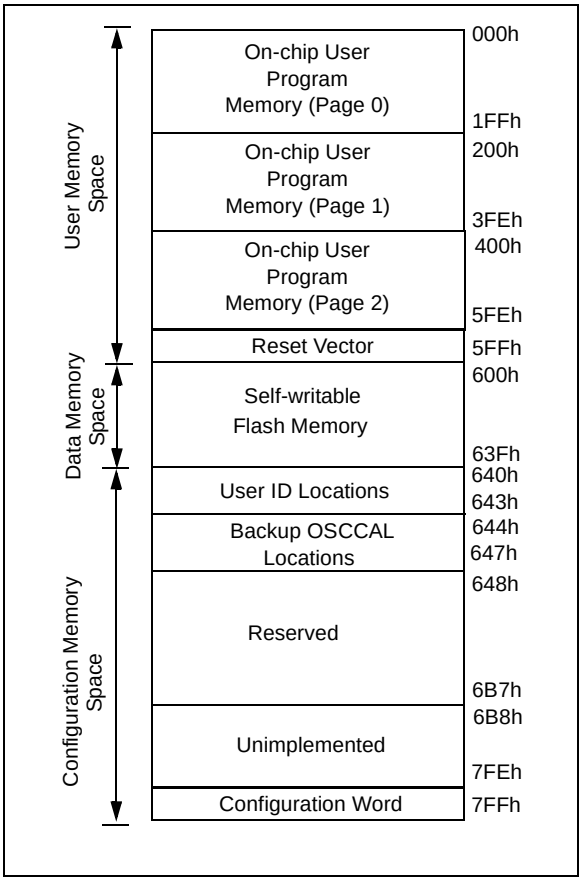
Legend: I = Input, O = Output, P = Power

Note 1: In the PIC12F529T48A and PIC12F529T39A, the programming high voltage is internally generated. To activate the Program/Verify mode, high voltage of IIHH current capability (see Table 6-1) needs to be applied to the $\overline{MCLR}$ input.

2.0 MEMORY MAPPING

The Program Memory map of the PIC12F529T48A and PIC12F529T39A devices is shown in Figure 2-1. In Program/Verify mode, the program memory extends from 0x000 to 0x7FF.

FIGURE 2-1: MEMORY MAP



2.1 User Memory

The user memory space is the on-chip user program memory. As shown in Figure 2-1, it extends from 0x000 to 0x5FF and partitions into pages, including Reset vector at address 0x3FF. Note that the PC will increment from (0x000-0x5FF) then to 0x0, (not to 0x600).

2.2 Data Memory

The data memory space is the Flash data memory block and is located at addresses PC = 600h-63Fh. All Program mode commands that work on the normal Flash memory work on the Flash data memory block. This includes Bulk Erase, Load and Read data commands.

2.3 Configuration Memory

The configuration memory space extends from 0x640 to 0x7FF. Locations from 0x648 through 0x6B7 are reserved. The user ID locations extend from 0x640 through 0x643. The Configuration Word is physically located at 0x7FF, and the backup OSCCAL locations extend from 0x644 through 0x647.

2.3.1 USER ID LOCATIONS

A user may store identification information (ID) in four user ID locations. The user ID locations are mapped in [0x640:0x643]. Each user ID location is 12 bits. The contents of user ID locations are used in the calculation of the device checksum when Code Protection is enabled. The four Least Significant bits (LSbs) of each location are concatenated into a 2-byte value, the “User ID”, and used in the checksum calculation. This 2-byte “User ID” is displayed by MPLAB® IDE. Table 2-1 illustrates the relationship between the user ID locations and the “User ID” value used in the checksum computations (see Table 5-2).

TABLE 2-1: “USER ID” VALUE AND LOCATION

User ID Memory	User ID Location – 12-bit value		“User ID” Values
	Binary	Hex	
0x640	0000 0000 1001b	009h	**9**xxxh
0x641	1100 0001 1000b	C18h	x**8**xxh
0x642	0111 0010 0100b	724h	xx**4**xh
0x643	0110 0011 0101b	635h	xxx**5**h

“User ID” composite value displayed in MPLAB® IDE = 9845h

Although 12 bits are available in each location, previous devices only implemented the lower four bits of each location. As a result, these additional bits may not have support in the language and programming tools. For this reason, it is recommended that the user only use the four LSBs of each user ID location.

2.3.2 CONFIGURATION WORD

The Configuration Word is physically located at 0x7FF. It is only available upon Program mode entry. Once an Increment Address command is issued, the Configuration Word is no longer accessible, regardless of the address of the program counter.

Note:	By convention, the Configuration Word is stored at the logical address location of 0xFFF within the hex file generated for the PIC12F529T48A and PIC12F529T39A. This logical address location may not reflect the actual physical address for the part itself. It is the responsibility of the programming software to retrieve the Configuration Word from the logical address within the hex file and granulate the address to the proper physical location when programming.

2.3.3 BACKUP OSCCAL VALUE

The backup OSCCAL locations 0x644+0x647 are the locations where the OSCCAL values are stored during testing of the INTOSC. This location is not erased during a standard Bulk Erase, but is erased if the PC is moved into configuration memory prior to invoking a Bulk Erase. If this value is erased, it is the user's responsibility to rewrite it back to this location for future use.

2.4 Oscillator Calibration Bits

The oscillator Calibration bits are stored at the Reset vector as the operand of a `MOVLW` instruction. Programming interfaces must allow users to program the Calibration bits themselves for custom trimming of the INTOSC. Capability for programming the Calibration bits when programming the entire memory array must also be maintained for backwards compatibility.

3.0 PROGRAM/VERIFY MODE

In Program/Verify mode, the program memory and the configuration memory can be accessed and programmed in serial fashion. ICSPDAT and ICSPCLK are used for the data and the clock, respectively. All commands and data words are transmitted LSb first. Data changes on the rising edge of the ICSPCLK and is latched on the falling edge. In Program/Verify mode, both the ICSPDAT and ICSPCLK are Schmitt Trigger inputs. The sequence that enters the device into Program/Verify mode places all other logic into the Reset state. Upon entering Program/Verify mode, all I/Os are automatically configured as high-impedance inputs and the address is cleared.

3.1 High-Voltage Program/Verify Mode Entry and Exit

There are two different methods of entering Program/Verify mode via high-voltage:

- VDD-First entry mode

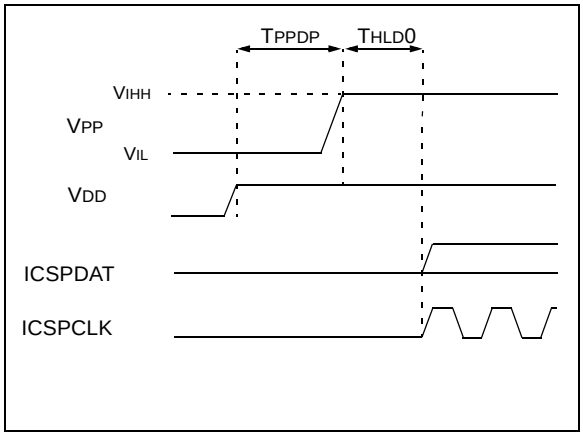
3.1.1 VDD-FIRST ENTRY MODE

To enter Program/verify mode via the VDD-first method, please follow the sequence below:

1. Hold ICSPCLK and ICSPDAT low;
2. Raise the voltage on VDD from 0V to the desired operating voltage (VIL to VDD);
3. Raise the voltage on $\overline{\text{MCLR}}$/VPP from VDD or below, to VIHH.

The VDD-first method is useful when programming the device when VDD is already applied, for it is not necessary to disconnect VDD to enter Program/Verify mode. See the timing diagram in Figure 3-1.

FIGURE 3-1: PROGRAMMING MODE ENTRY – VDD FIRST



3.1.2 PROGRAM/VERIFY MODE EXIT

To exit Program/Verify mode take $\overline{\text{MCLR}}$ to VDD or lower (VIL). See Figure 3-2 and Figure 3-3.

FIGURE 3-2: PROGRAMMING MODE EXIT – VPP LAST

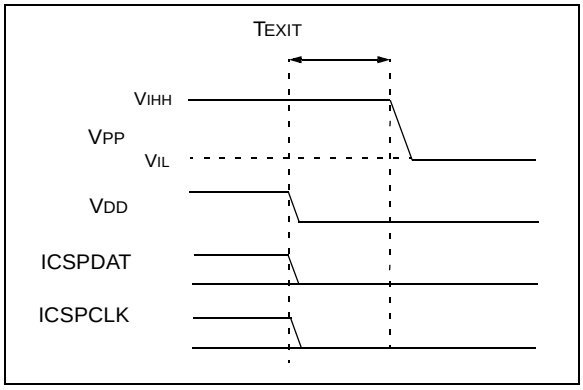
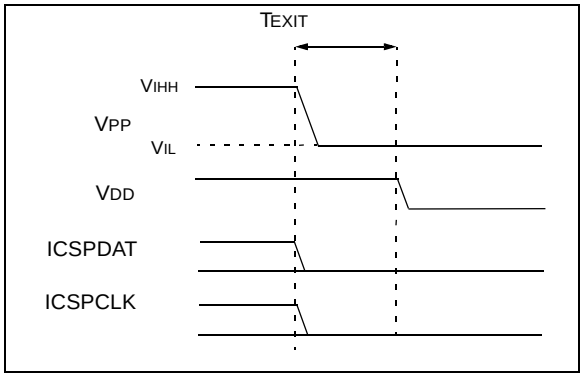


FIGURE 3-3: PROGRAMMING MODE EXIT – VDD LAST



3.1.3 SERIAL PROGRAM/VERIFY OPERATION

The RB1 pin is used as a clock input pin, and the RB0 pin is used for entering command bits and data input/output during serial operation. To input a command, the clock pin (RB1) is cycled six times. Each command bit is latched on the falling edge of the clock with the Least Significant bit (LSb) of the command being input first. The data on pin RB0 is required to have a minimum setup and hold time of 100 ns with respect to the falling edge of the clock. Commands that have data associated with them (Read and Load) are specified to have a minimum delay of 1 µs between the command and the data. After this delay the clock pin is cycled 16 times with the first cycle being a Start bit and the last cycle being a Stop bit. Data is also input and output LSb first, with data input being latched on the falling edge of the clock and data output being driven on the rising edge of the clock. Therefore, during a read operation the LSb will be transmitted onto pin RB0 on the rising edge of the second cycle, and during a Load operation the LSb will be latched on the falling edge of the second cycle. A minimum 1 µs delay is also specified between consecutive commands; except the “End Programming” command which requires a 100 µs delay. Because this

is a 12-bit core, the two MSbs of the data word are ignored. The commands that are available are described in Table 3-1.

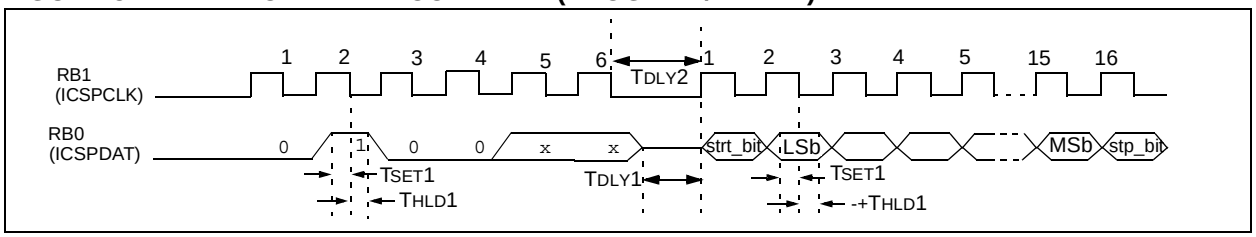
TABLE 3-1: COMMAND MAPPING LOAD DATA

Command	Mapping (MSb ... LSb)	Hex Value	Data
Load Data	xx0010	2	start_bit, data (14), stop_bit
Read Data	xx0100	4	start_bit, data (14), stop_bit
Increment Address	xx0110	6	
Begin Programming	xx1000	8	
End Programming	xx1110	E	
Bulk Erase Program Memory	xx1001	9	

3.1.3.1 Load Data

After receiving this command, the device will clock in 14 bits as a “data word” when 16 cycles are applied, as described previously. Because this is a 12-bit core, the two MSbs of the data word are ignored. A timing diagram for the Load Data command is shown in Figure 3-4.

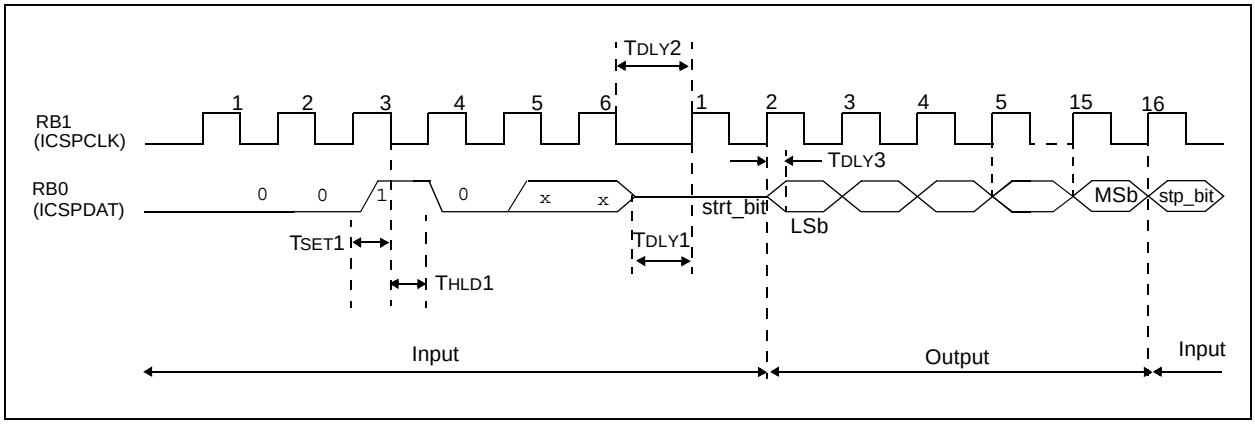
FIGURE 3-4: LOAD DATA COMMAND (PROGRAM/VERIFY)



3.1.3.2 Read Data

After receiving this command, the chip will transmit data bits out of the memory currently accessed starting with the second rising edge of the clock input. The RB0 pin will go into Output mode on the second rising clock edge and it will revert back to Input mode (high-impedance) after the 16th rising edge. Because this is a 12-bit core, the two MSbs will read as ‘1’. A timing diagram of this command is shown in Figure 3-5.

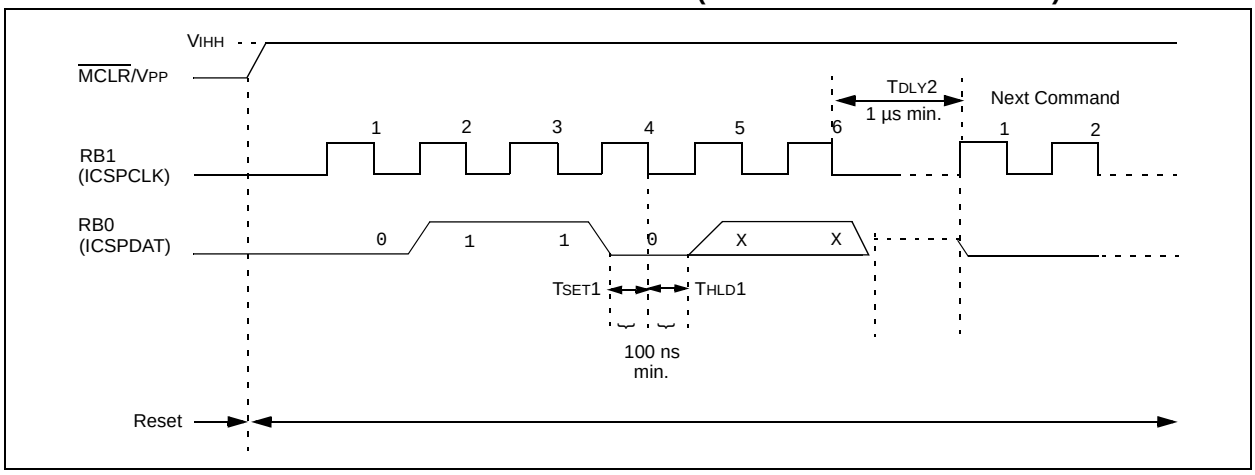
FIGURE 3-5: READ DATA FROM PROGRAM MEMORY COMMAND



3.1.3.3 Increment Address

The PC is incremented when this command is received.

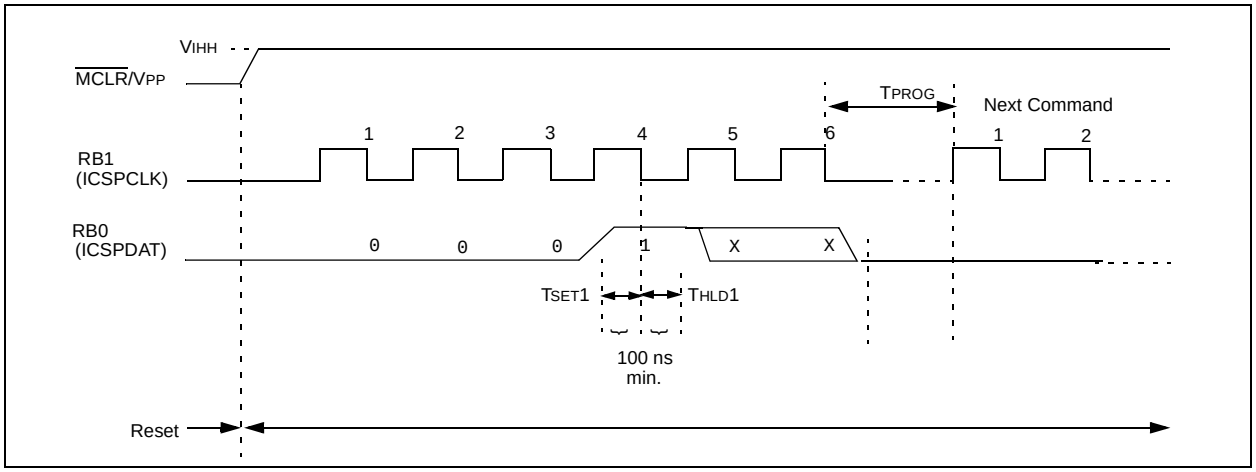
FIGURE 3-6: INCREMENT ADDRESS COMMAND (SERIAL PROGRAM/VERIFY)



3.1.3.4 Begin Programming

A Load command (Load Data) must be given before every Begin Programming command. Programming of the appropriate memory (User Program Memory, Flash Data Memory or Test Program Memory) will begin after this command is received and decoded.

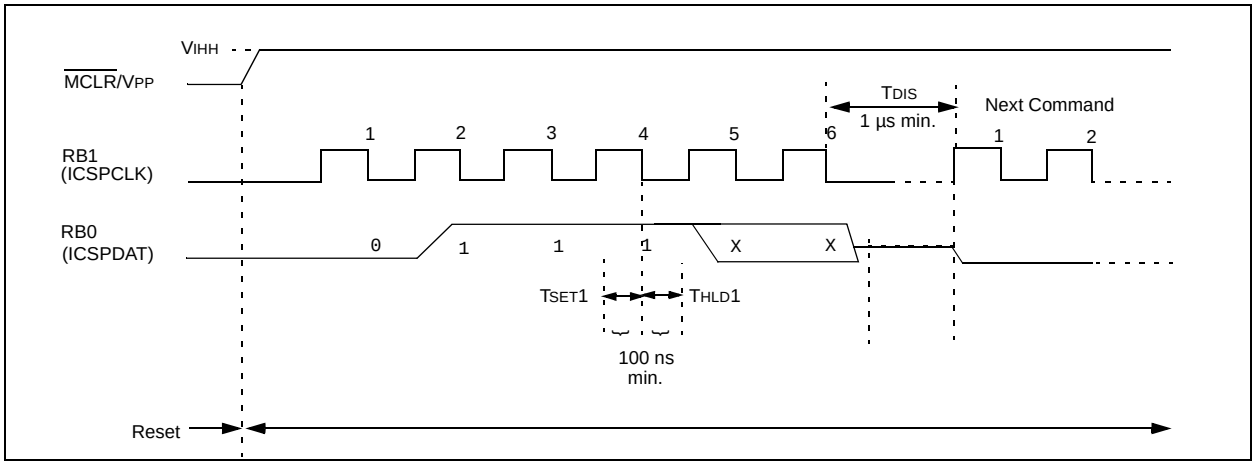
FIGURE 3-7: BEGIN PROGRAMMING COMMAND



3.1.3.5 End Programming

After receiving this command, the chip stops programming the memory (User Program Memory, Flash Data Memory or Test Program Memory) it was programming at the time.

FIGURE 3-8: END PROGRAMMING COMMAND



3.1.3.6 Bulk Erase Program Memory

After this command is performed, the specific section of program memory and Configuration Word is erased. See Table 3-2 for details.

Note 1: A fully erased part will read '1's in every Program Memory location.

2: The oscillator Calibration bits are erased if a Bulk Erase is invoked. They must be read and saved prior to erasing the device and restored during the programming operation. Oscillator Calibration bits are stored at the Reset vector as the operand of a `MOVLW` instruction.

3: PIC12F529T48A and PIC12F529T39A require three full Bulk Erases before code protection is disabled.

FIGURE 3-9: BULK ERASE PROGRAM MEMORY COMMAND

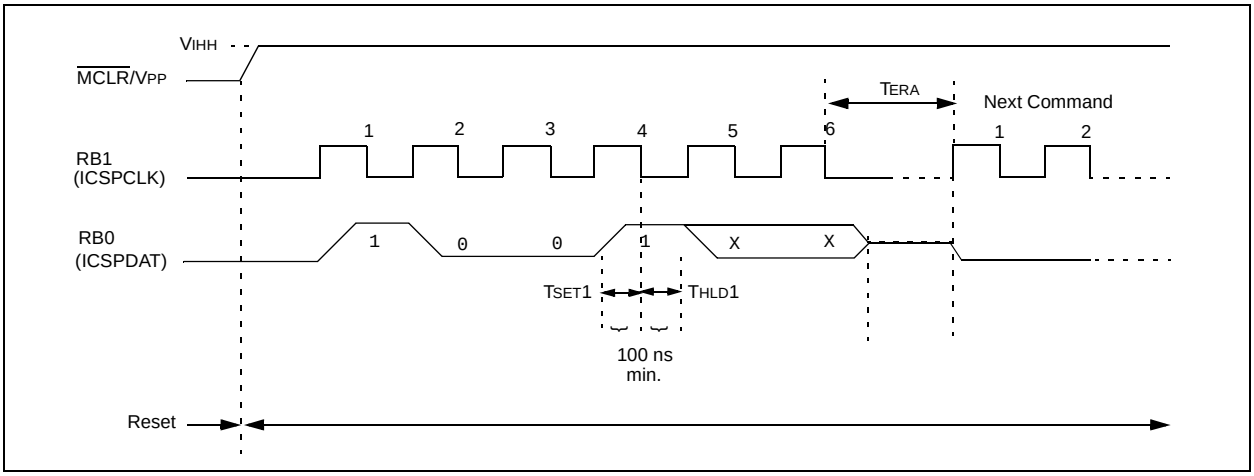


TABLE 3-2: BULK ERASE MEMORY PORTIONS

PC	Config. Word (Fuses)	User Program Memory Erased	Flash Data Memory Erased	User ID Memory Erased
Configuration Word (Fuses)	Yes	Yes	$\overline{CPDF}$ = 0 – Yes $\overline{CPDF}$ = 1 – No	No
000h-5FFh (User Memory)	Yes	Yes	$\overline{CPDF}$ = 0 – Yes $\overline{CPDF}$ = 1 – No	No
600h-63Fh (Data Memory)	No	No	$\overline{CPDF}$ = 0 – No $\overline{CPDF}$ = 1 – Yes	No
640h-647h (Configuration Memory)	No	No	No	Yes

Note: Yes = erase
No = unchanged

FIGURE 3-10: READING AND TEMPORARY SAVING OF THE OSCCAL CALIBRATION BITS

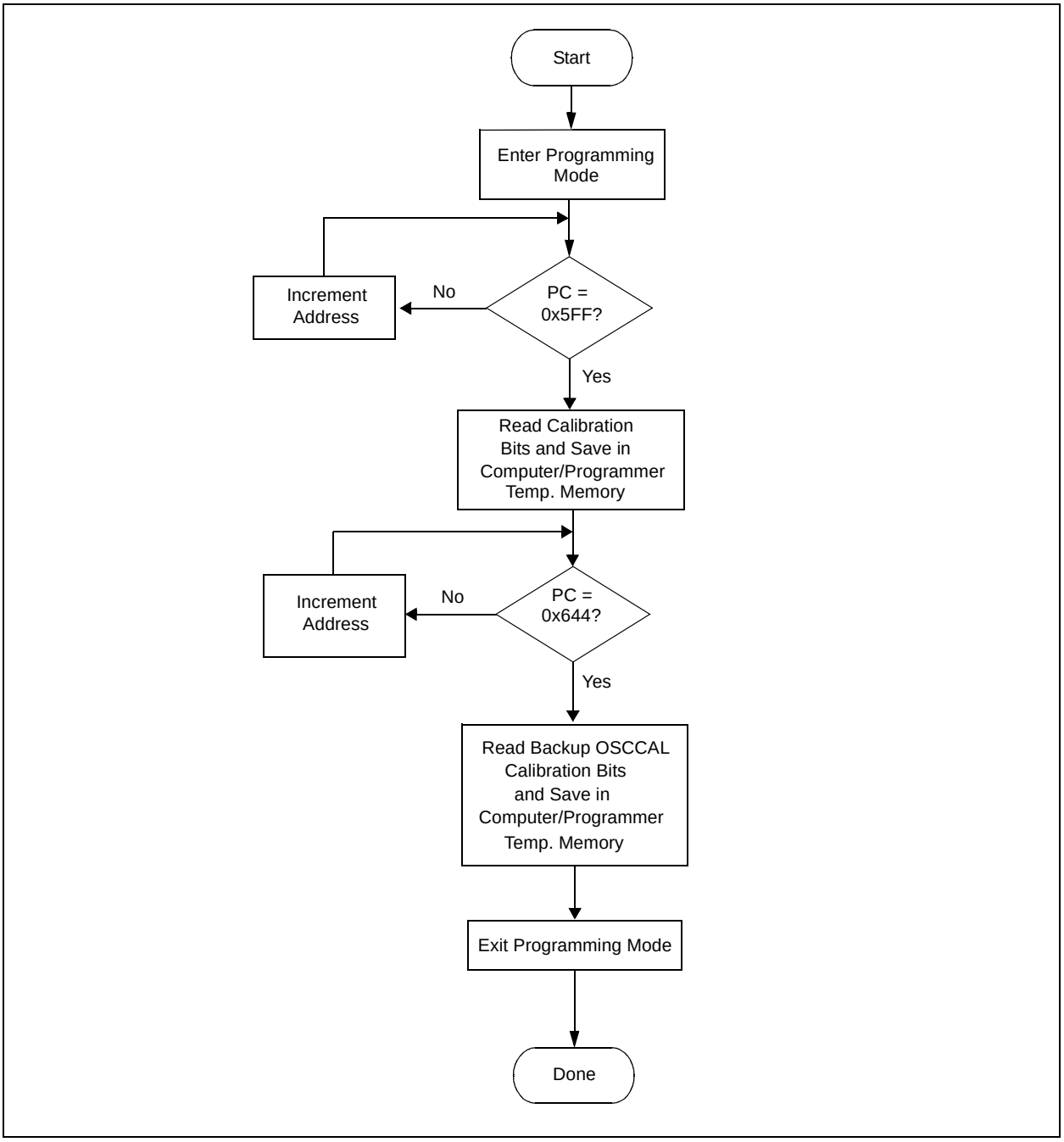


FIGURE 3-11: RESTORING/PROGRAMMING THE OSCCAL CALIBRATION BITS

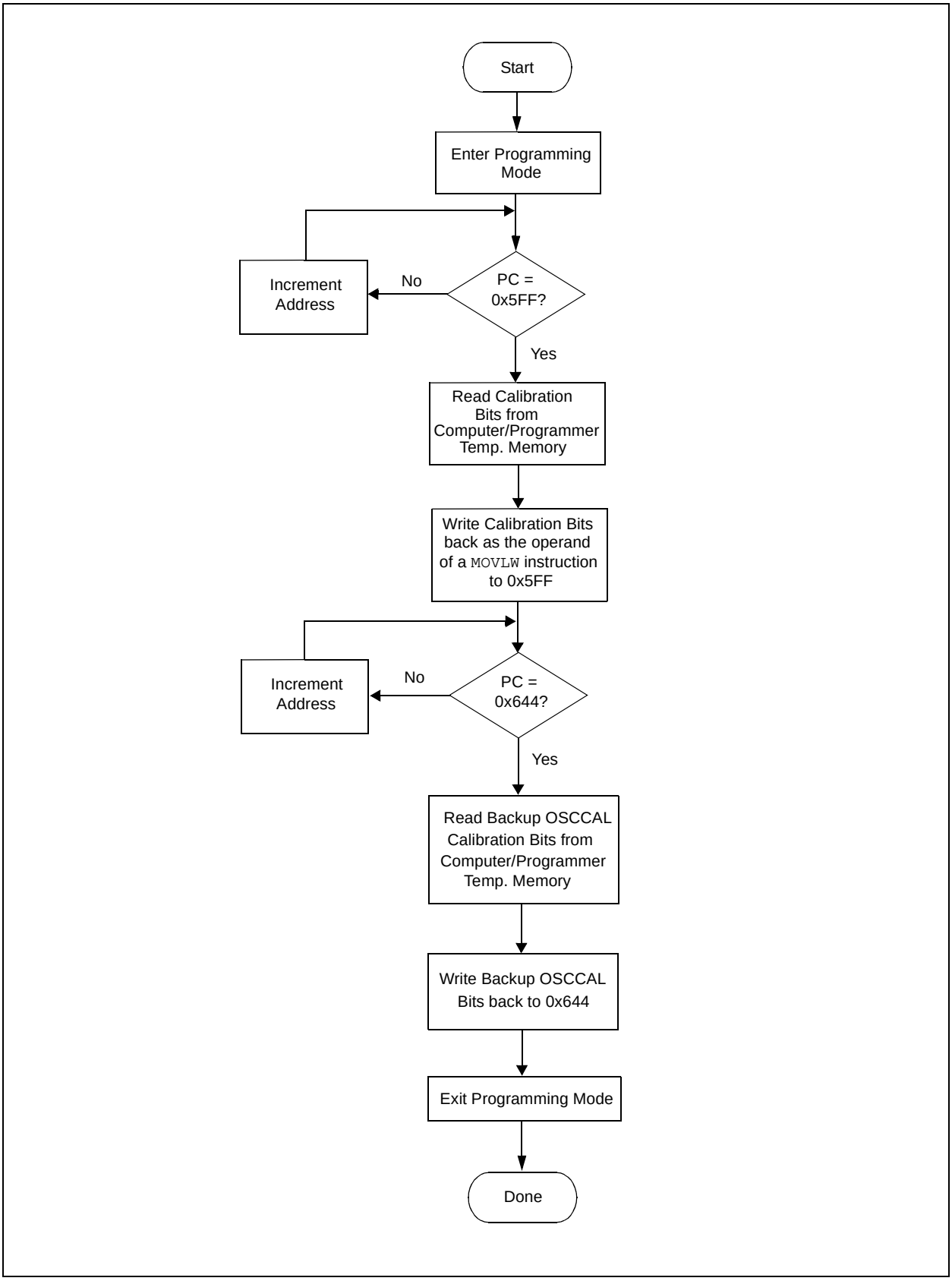


FIGURE 3-12: PROGRAM FLOWCHART – USER MEMORY

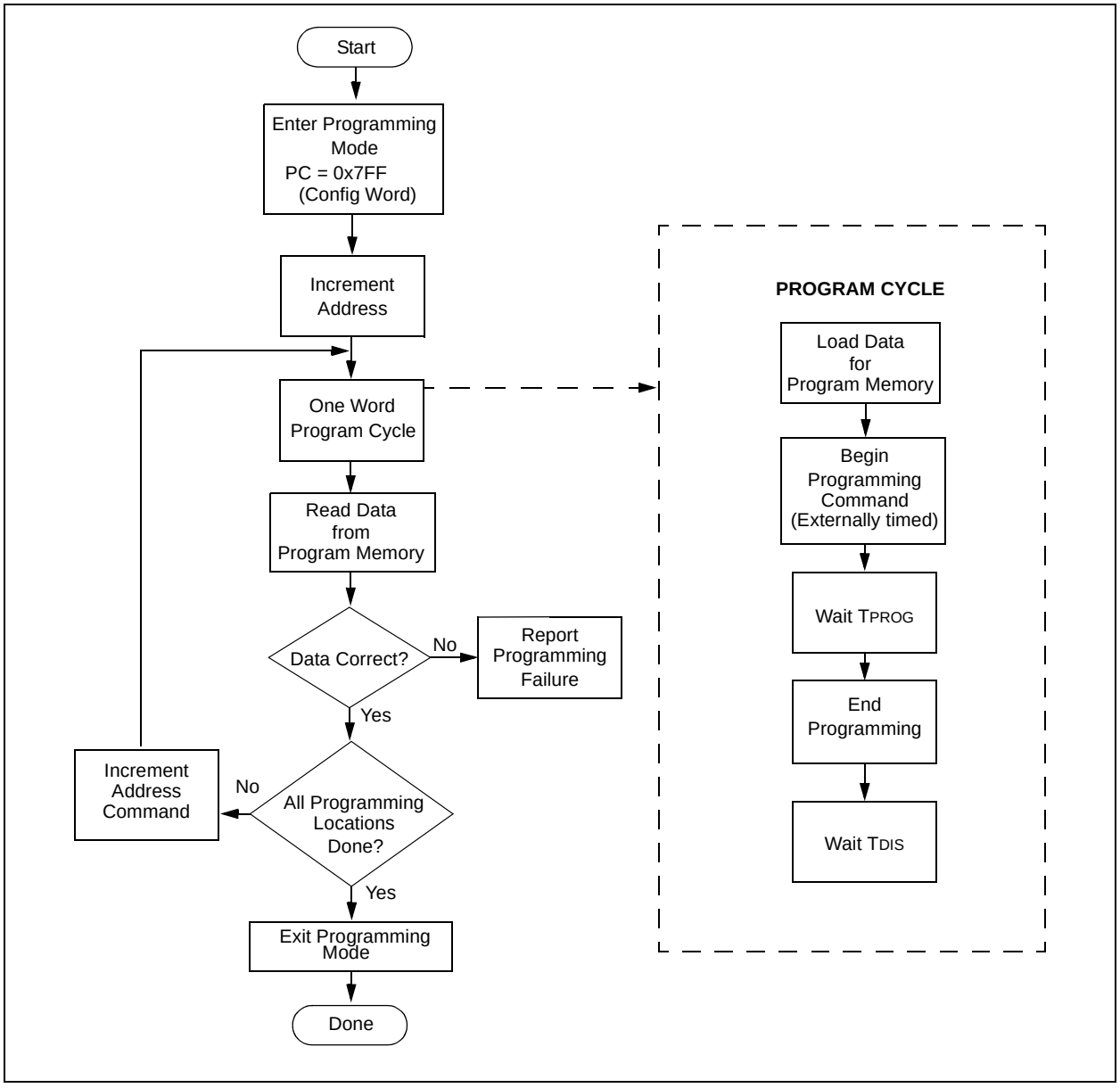


FIGURE 3-13: PROGRAM FLOWCHART – FLASH DATA MEMORY

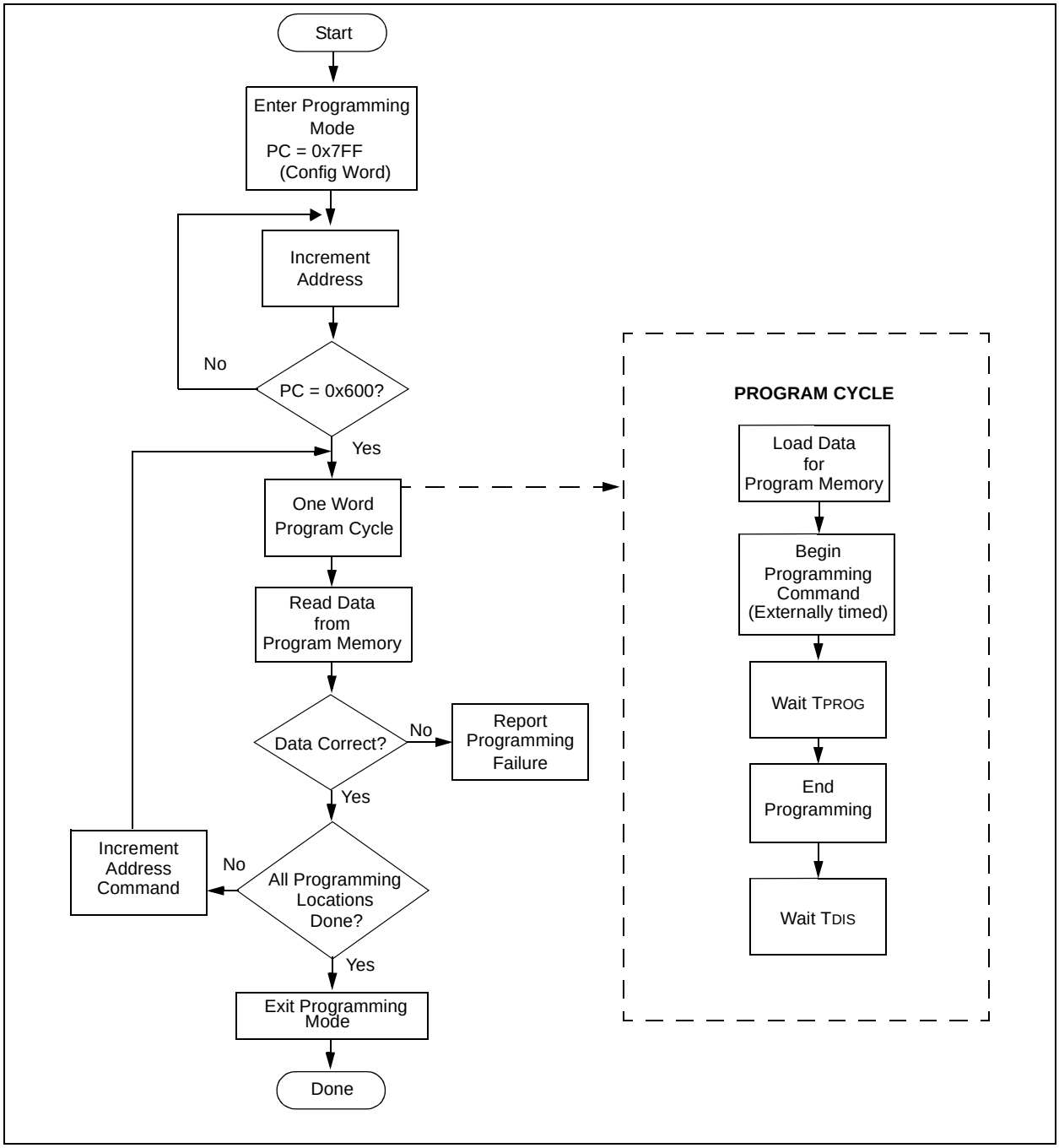


FIGURE 3-14: PROGRAM FLOWCHART – CONFIGURATION MEMORY

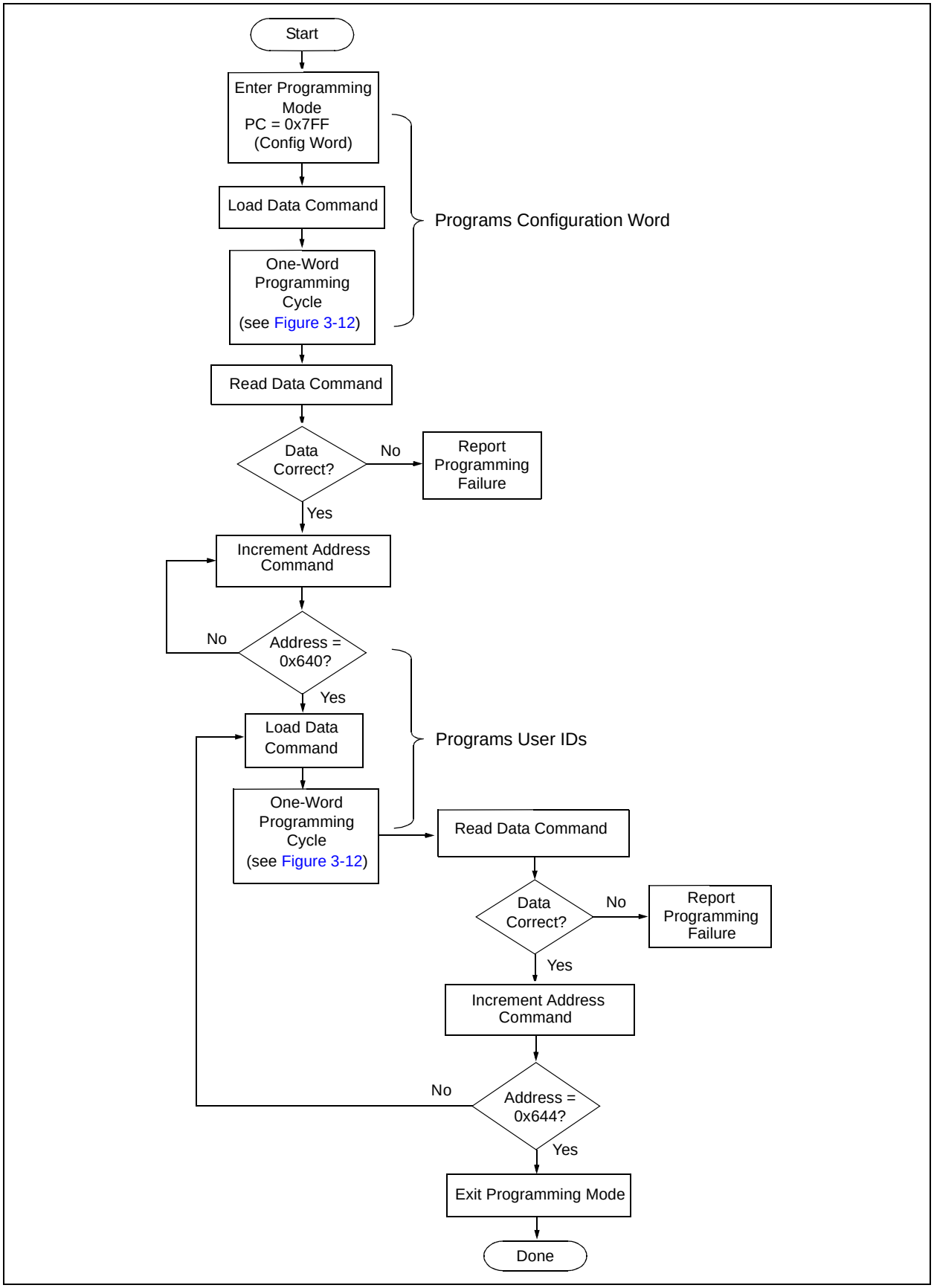
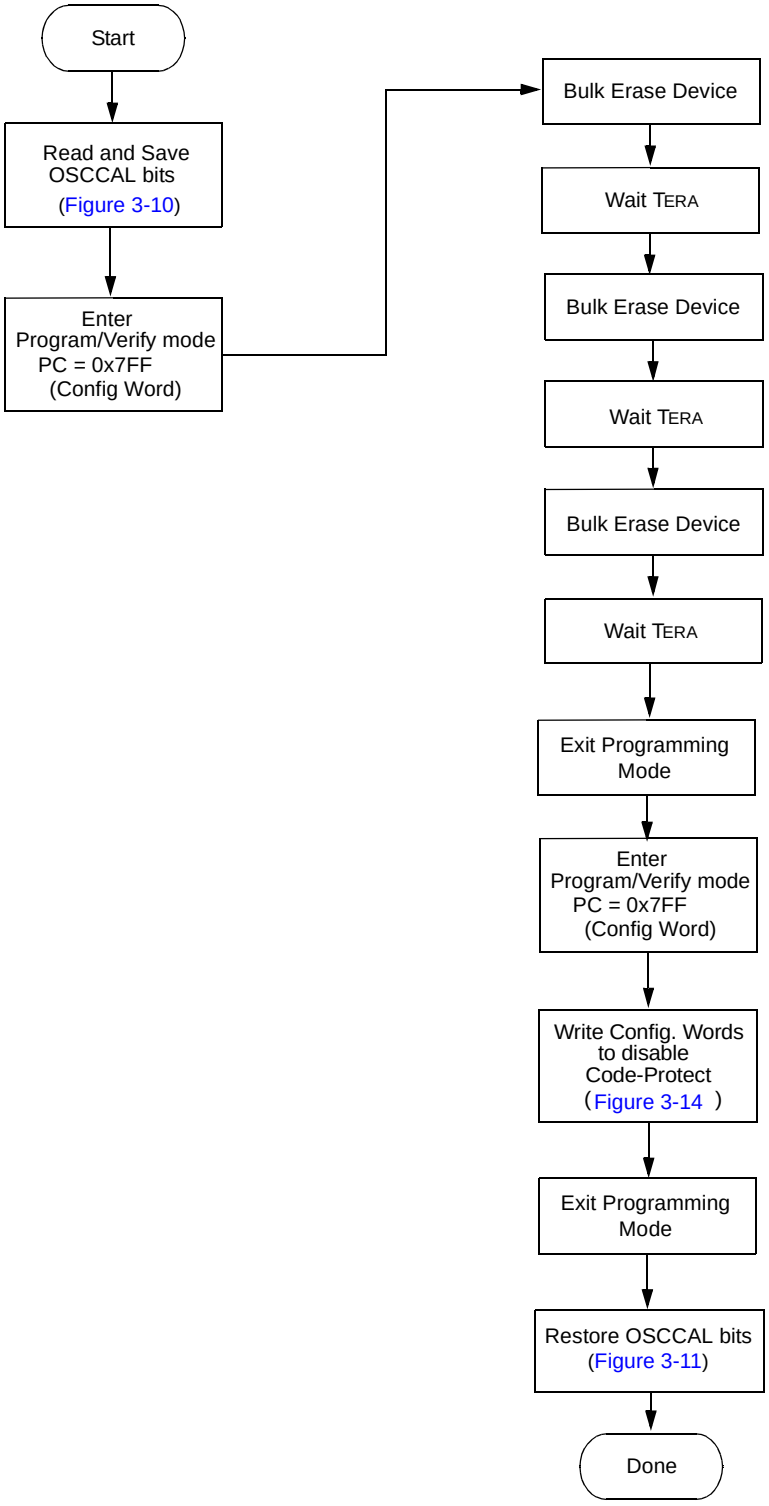
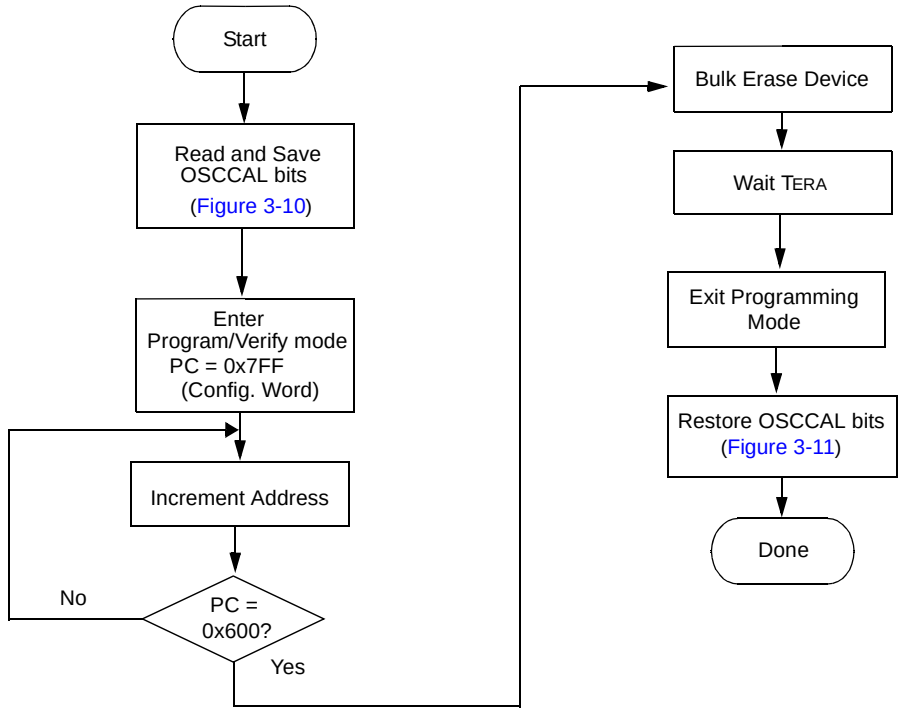


FIGURE 3-15: PROGRAM FLOWCHART – ERASE PROGRAM MEMORY, CONFIGURATION WORD



Note: Flash Data Memory block will also be erased if $\overline{\text{CPDF}}$ = 0 (see Table 3-2 for more information).

FIGURE 3-16: PROGRAM FLOWCHART – ERASE FLASH DATA MEMORY



Note 1: This operation requires that $\overline{\text{CPDF}}$ = 1.

FIGURE 3-17: PROGRAM FLOWCHART – ERASE USER ID

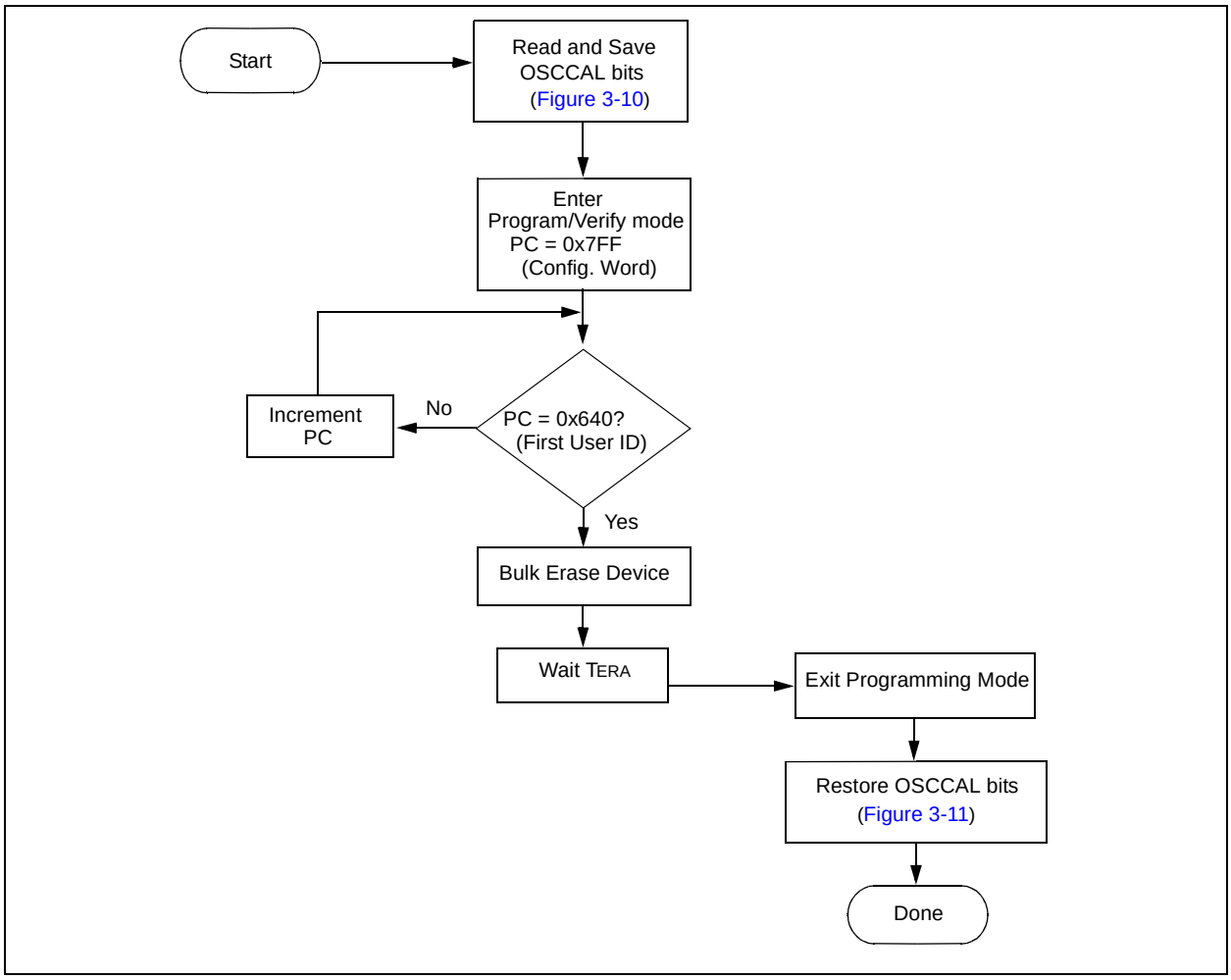


FIGURE 3-18: PROGRAM FLOWCHART – HIGH-LEVEL FULL DEVICE PROGRAM

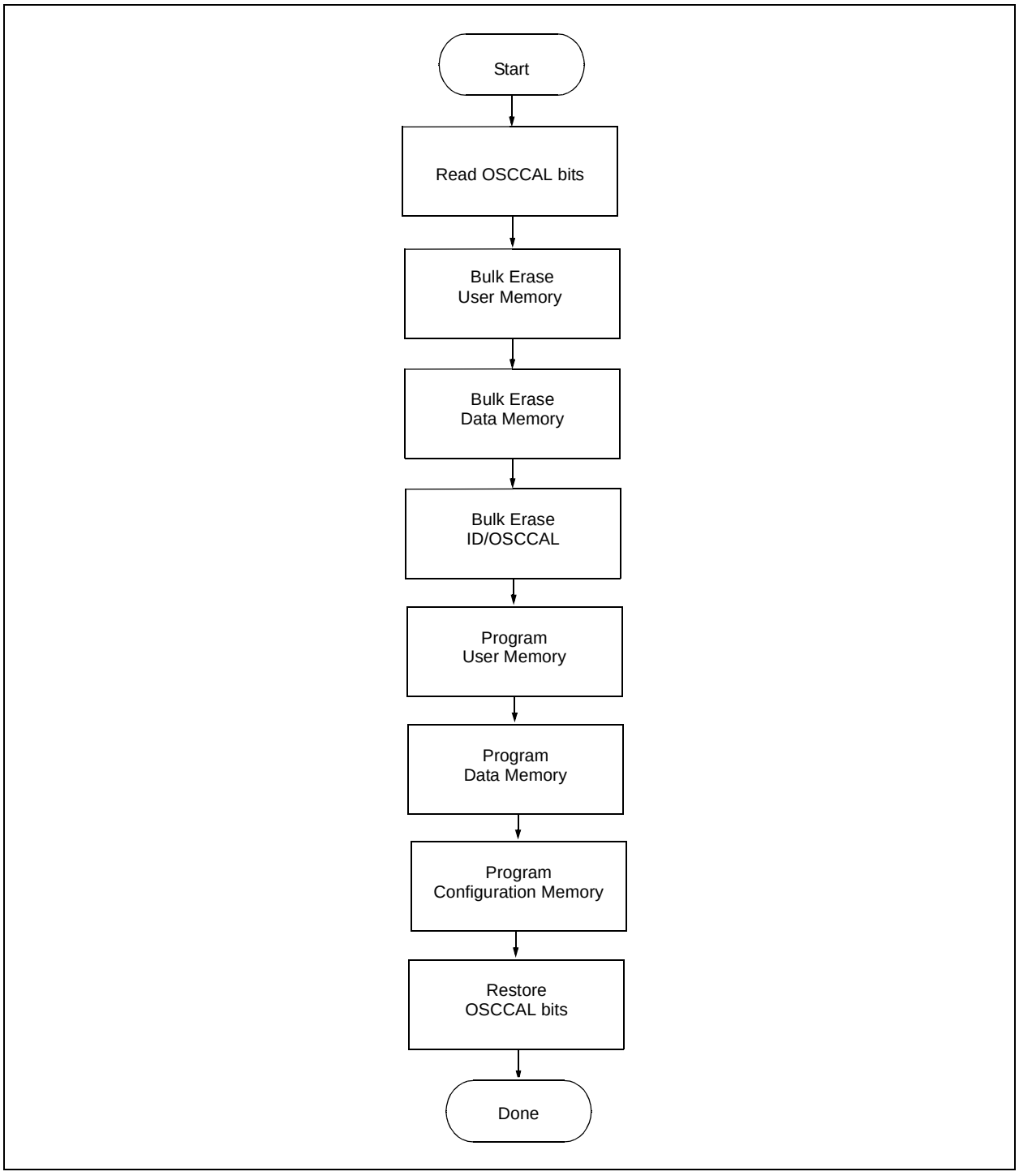
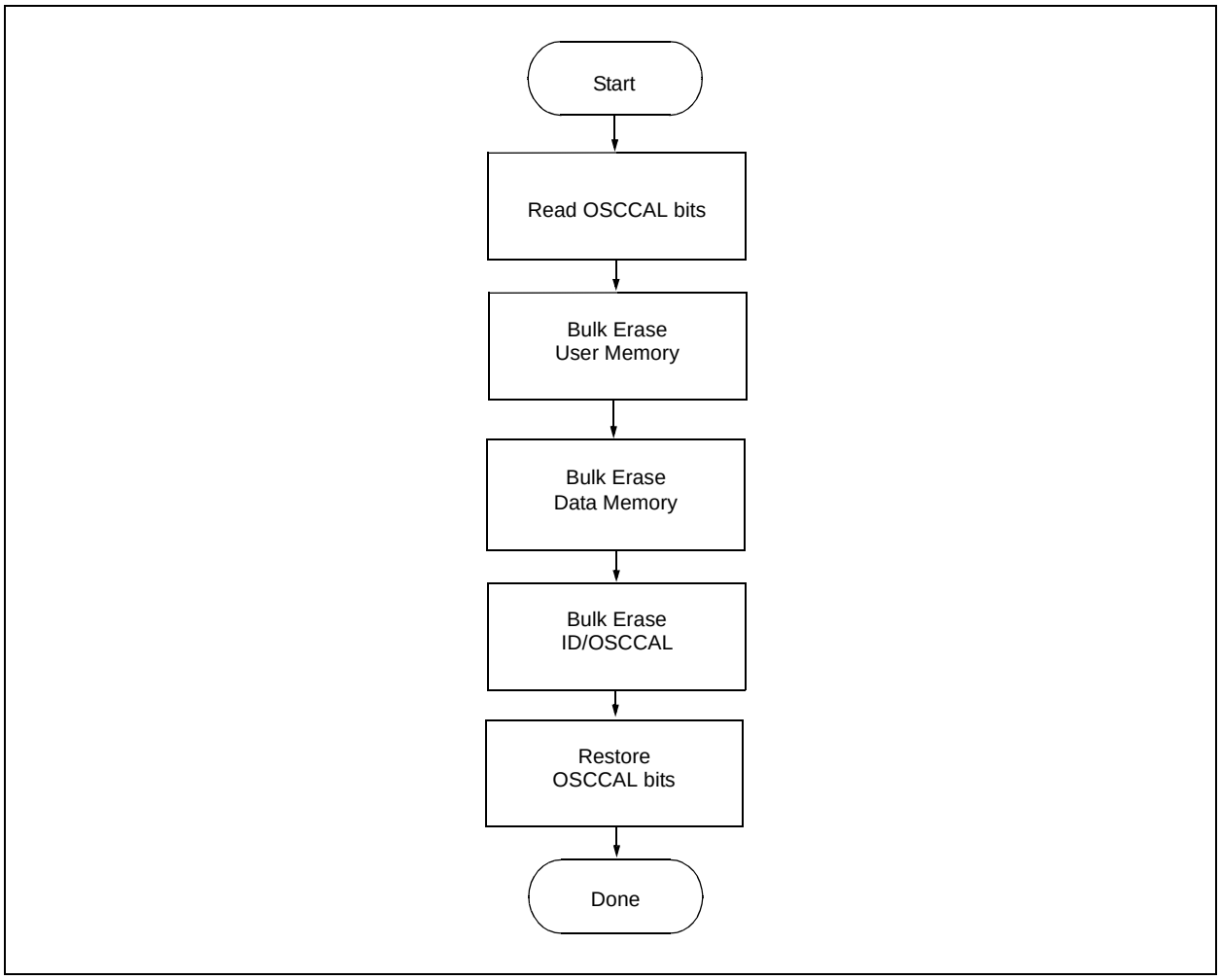


FIGURE 3-19: PROGRAM FLOWCHART – HIGH-LEVEL FULL DEVICE ERASE



4.0 CONFIGURATION WORD

The implemented Configuration bits can be programmed at their default values, or they are not programmed.

See Register 4-1 below for details.

REGISTER 4-1: CONFIGURATION WORD

U-1	P-1	P-1	P-1	P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
—	CP3	CP2	CP1	CP0	$\overline{\text{CPDF}}$	IOSCFS	MCLRE	PAR	WDTE	FOSC1	FOSC0
bit 11											bit 0

Legend:	**P = Programmable**	U = Unimplemented bit, read as '1'
R = Readable bit	W = Writable bit	'0' = Bit is cleared
-n = Blank/Bulk Erased Value	'1' = Bit is set	

bit 11 **Unimplemented:** Read as '1'

bit 10-7 **CP<3:0>:** Enhanced Code Protect bits
1011 = Program memory code protection disabled
0010 = Program memory code protection enabled
All others = Memory access disabled

bit 6 **$\overline{\text{CPDF}}$:** Code Protection bit – Flash Data Memory
1 = Code protection off
0 = Code protection on

bit 5 **IOSCFS:** Internal Oscillator Frequency Select bit
1 = 8 MHz INTOSC speed
0 = 4 MHz INTOSC speed

bit 4 **MCLRE:** Master Clear Enable bit
1 = $\overline{\text{MCLR}}$ pin functions as $\overline{\text{MCLR}}$
0 = $\overline{\text{MCLR}}$ pin functions as "input-only", $\overline{\text{MCLR}}$ internally tied to V_{DD}

bit 3 **PAR:** Code Protection Parity bit(2)
1 = Parity bit set
0 = Parity bit clear

bit 2 **WDTE:** Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 1-0 **FOSC1:FOSC0:** Oscillator Selection bits
00 = LP oscillator with 18 ms DRT
01 = XT oscillator with 18 ms DRT
10 = INTRC with 1 ms DRT(1)
11 = EXTRC with 1 ms DRT(1)

Note 1: It is the responsibility of the application designer to ensure the use of the 1 ms DRT will result in acceptable operation. Refer to Electrical Specifications for V_{DD} rise time and stability requirements for this mode of operation.

2: Set or clear to create odd parity with Configuration Word excluding CP<3:0>.

5.0 CODE PROTECTION

For the PIC12F529T48A and PIC12F529T39A, once code protection is enabled, all program memory locations 0x0-0x5FE, read all '0's. Program memory location 0x5FF is always unprotected. The user ID locations, backup OSCCAL location and the Configuration Word read out in an unprotected fashion. It is possible to program the user ID locations, backup OSCCAL location and the Configuration Word after code-protect is enabled.

Program memory code protection is controlled by four Configuration bits: CP3, CP2, CP1, CP0. These bits must be configured in a certain pattern for correct operation in both protected and unprotected states. See Table 5-1 for a description of these states. They do not affect Flash data memory protection.

TABLE 5-1: CPx CONFIGURATION BIT SETTINGS

CPx Configuration Bit settings				
CP3	**CP2**	**CP1**	**CP0**	
1	1	1	1	Erased
1	0	1	1	Code protection disabled
0	0	1	0	Code protection enabled

All other combinations are reserved and should not be used.

The device is initially in the Erased state anytime the configuration fuses are erased. The device code protection must be disabled before attempting to program Flash memory.

The PAR bit should be used to create an odd parity with the Configuration Word, excluding the CP<3:0> bits.

The code protection of the Flash data memory is dependant on the $\overline{\text{CPDF}}$ bit. If the $\overline{\text{CPDF}}$ bit is set, only the Flash data memory block is code-protected. See Table 3-2 for erase conditions involving the $\overline{\text{CPDF}}$ bit.

5.1 Disabling Code Protection

It is recommended that the following procedure be performed before any other programming is attempted. It is also possible to turn code protection off using this procedure. However, ***all data within the program memory will be erased when this procedure is executed, and thus, the security of the code is not compromised.*** See Table 3-2 for more information on Flash data memory.

To disable code-protect:

a) Enter Program mode
b) Execute Bulk Erase Program Memory command (001001).
c) Wait TERA
d) Repeat steps b and c for a total of three erase cycles.

Note: To allow portability of code, the programmer is required to read the Configuration Word and user ID locations from the hex file when loading the hex file. If Configuration Word information was not present in the hex file, then a simple warning message may be issued. Similarly, while saving a hex file, Configuration Word and user ID information must be included. An option to not include this information may be provided.

Microchip Technology Incorporated feels strongly that this feature is important for the benefit of the end customer.

Note: The device code protection must be disabled before attempting to program Flash memory.

5.2 Checksum Computation

5.2.1 CHECKSUM

Checksum is calculated by reading the contents of the PIC12F529T48A and PIC12F529T39A memory locations and adding up the opcodes up to the maximum user addressable location. Any Carry bits exceeding 16 bits are neglected. Finally, the Configuration Word (appropriately masked) is added to the checksum. The checksum computation for the PIC12F529T48A and PIC12F529T39A is shown in Table 5-2.

The checksum is calculated by summing the following:

- The contents of all program memory locations
- The Configuration Word, appropriately masked
- Masked user ID locations (when applicable)

The Least Significant 16 bits of this sum is the checksum.

The following table describes how to calculate the checksum for each PIC12F529T48A and PIC12F529T39A.

Note:	The checksum calculation differs depending on the code-protect setting. The Configuration Word and user ID locations can always be read regardless of the code-protect settings.

Note:	Data memory does not affect the checksum.

TABLE 5-2: CHECKSUM COMPUTATIONS(1)

Device	Program Code-Protect	Checksum*	Blank Value	0x723 at 0 and Max. Address
PIC12F529T48A PIC12F529T39A	OFF	SUM[0x000:0x5FE] + CFGW & 0x07F	0xEA80	0xD8C8
	ON	CFGW & 0x07F + SUM_ID(1)	0xEAFF(2)	0xD947

Legend: CFGW = Configuration Word
SUM[a:b] = [Sum of locations a to b inclusive]
SUM_ID = User ID locations masked by 0x00F then made into a 16-bit value with ID0 as the Most Significant nibble. For example, ID0 = 0x1, ID1 = 0x2, ID2 = 0x3, ID3 = 0x4, then SUM_ID = 0x1234.
*Checksum = [Sum of all the individual expressions] & [0x0FFFF]
+ = Addition
& = Bitwise AND

Note 1: Checksum shown assumes that SUM_ID contains the unprotected checksum.

2: Data protect is disabled in this example. The Parity bit is set as is appropriate for this Configuration Word.

6.0 PROGRAM/VERIFY MODE ELECTRICAL CHARACTERISTICS

TABLE 6-1: AC/DC TIMING REQUIREMENTS

AC TARGETS						
Sym.	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
General						
VIHH	VPP high voltage on $\overline{\text{MCLR}}$ for Program/Verify mode entry	12.5	—	13.5	V	
VIHL	Voltage on $\overline{\text{MCLR}}$ to be in Normal mode	VSS	—	VDD + 1.0	V	
TVHHR	$\overline{\text{MCLR}}$ rise time (VSS to VHH) for Test mode entry	—	—	1.0	µs	
VIH1	Clock (RB1) and Data (RB0) input high level	0.85*VDD	—		V	
VIL1	Clock (RB1) and Data (RB0) input low level	—	—	0.15*VDD	V	
VDDOK	Minimum VDD to perform Bulk Erase	2.7	—	—	V	
VPROG	High voltage on $\overline{\text{MCLR}}$ for programming	12.5	13.0	13.5	V	
IDDPROG	IDD level for programming operations, program memory	—	—	1.8	mA	
IDDERA	IDD level for Bulk Erase operations, program memory	—	—	1.8	mA	
IPP	$\overline{\text{MCLR}}$ pin current during Program/Verify mode	—	—	0.4	mA	
TPROG	Programming time	1000	—	2000	µs	
TPPDP	Hold time after VPP↑	5	—	—	µs	
TEXIT	Time delay when exiting Program/Verify mode	1	—	—	µs	
THLD0	ISPCLK, ISPDATA hold time after $\overline{\text{MCLR}}$↑ (Program/Verify mode selection pattern setup time)	5	—	—	µs	
Serial Program/Verify						
TSET1	Data in setup time before clock↓	100	—	—	ns	
THLD1	Data in hold time after clock↓	100	—	—	ns	
TDLY1	Data input not driven to next clock input (delay required between command/data or command/command)	1.0	—	—	µs	
TDLY2	Delay between clock↓ to clock↑ of next command or data	1.0	—	—	µs	
TDLY3	Clock↑ to data out valid (during Read Data)	80	—	—	ns	
TERA	Bulk Erase Time	4	—	10	ms	Total time to perform both stages of Bulk Erase and accept the next command.
TDIS	High Voltage Discharge Time	100	—	—	µs	Time to discharge high voltage.

APPENDIX A: REVISION HISTORY

Revision A (02/2012)

Initial release of this document.

Revision B (03/2012)

Added the PIC12F529T39A device.

Revision C (06/2012)

Corrected and clarified the checksum example (Table 5-2); Other minor corrections.

Note the following details of the code protection feature on Microchip devices:

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