Automotive Grade 2 SmartFusion2 SoC FPGAs Product Brief

Microsemi® SmartFusion®2 System-on-Chip (SoC) field programmable gate array (FPGA) integrate fourth generation flash-based FPGA fabric, an ARM® Cortex®-M3 processor, and high-performance communications interfaces on a single chip. The SmartFusion2 family is the industry's lowest power, most reliable and highest security programmable logic solution. SmartFusion2 FPGAs offer up to 3.6X the gate density, up to 2X the performance of previous flash-based FPGA families, and includes multiple memory blocks and multiply accumulate blocks for DSP processing. The 133 MHz ARM Cortex-M3 processor is enhanced with an embedded trace macrocell (ETM), memory protection unit (MPU), 8 Kbyte instruction cache, and additional peripherals, including controller area network (CAN), Gigabit Ethernet, and high speed universal serial bus (USB). High speed serial interfaces include PCI EXPRESS® (PCIe®), while DDR2/DDR3 memory controllers provide high speed memory interfaces.

Microsemi's automotive grade SmartFusion2 SoC FPGA offers automotive designers the advantages of best-in-class security, high reliability and low-power flash FPGAs. Automotive grade SmartFusion2 is offered in grade 2 (-40°C to 125°C T_J) temperature range and is ideally suited for on-body or in-cabin applications. SmartFusion2 provides a broad product roadmap with multiple I/O and fabric density options to allow users to select a device that fits their requirements.

SmartFusion2 Family

Reliability

- Extended Temperature AEC-Q100 Qualified Devices
  - Grade T2: -40°C to 125°C T_J
- Single Event Upset (SEU) Immune
  - Zero FIT FPGA Configuration Cells
- Single Error Correct Double Error Detect (SECDED) Protection on the Following:
  - Ethernet Buffers
  - CAN Message Buffers
  - Cortex-M3 Embedded Scratch Pad Memory (eSRAMs)
  - USB Buffers
  - PCIe Buffer
  - DDR Memory Controllers with Optional SECDED Modes
- Buffers Implemented with SEU Resistant Latches on the Following:
  - DDR Bridges (MSS, MDDR)
  - Instruction Cache
  - MMUART FIFOs
  - Serial Peripheral Interface (SPI) FIFOs
- NVM Integrity Check at Power-Up and On-Demand
- No External Configuration Memory Required—Instant-On, Retains Configuration When Powered Off

Security

- Design Security Features (Available on all Devices)
  - Intellectual Property (IP) Protection Through Unique Security Features and Use Models New to the PLD Industry
  - Encrypted User Key and Bitstream Loading, Enabling Programming in Less-Trusted Locations
  - Supply-Chain Assurance Device Certificate
  - Enhanced Anti-Tamper Features
  - Zeroization
- Data Security Features
  - Non-Deterministic Random Bit Generator (NRBG)
  - User Cryptographic Services (AES-256, SHA-256, Elliptical Curve Cryptographic (ECC) Engine)
  - User Physically Unclonable Function (PUF) Key Enrollment and Regeneration
  - CRI Pass-Through DPA Patent Portfolio License
  - Hardware Firewalls Protecting Microcontroller Subsystem (MSS) Memories

Low Power

- Low Static and Dynamic Power
  - Flash*Freeze Mode for Fabric
- Power as low as 13 mW/Gbps per lane for SERDES devices
- Up to 50% lower total power than competing SoC devices

High Performance FPGA

- Efficient 4-Input LUTs with Carry Chains for High-Performance and Low Power
- Up to 109 Blocks of Dual-Port 18 Kbit SRAM (Large SRAM) with 400 MHz Synchronous Performance (512 x 36, 512 x 32, 1 Kbit x 18, 1 Kbit x 16, 2 Kbit x 9, 2 Kbit x 8, 4 Kbit x 4, 8 Kbit x 2, or 16 Kbit x 1)
- Up to 112 Blocks of Three-Port 1 Kbit SRAM with 2 Read Ports and 1 Write Port (micro SRAM)

- High-Performance DSP Signal Processing
  - Up to 84 Fast Mathblocks with 18 x 18 Signed Multiplication, 17 x 17 Unsigned Multiplication and 44-Bit Accumulator.

Microcontroller Subsystem (MSS)

- Hard 133 MHz 32-Bit ARM Cortex-M3 Processor
  - 1.25 DMIPS/MHz
  - 8 Kbyte Instruction Cache
  - Embedded Trace Macrocell (ETM)
  - Memory Protection Unit (MPU)
  - Single Cycle Multiplication, Hardware Divide
  - JTAG Debug (4 wires), Serial Wire Debug (SWD, 2 wires), and Serial Wire Viewer (SWV) Interfaces
- 64 Kb Embedded SRAM (eSRAM)
- Up to 512 Kb Embedded Nonvolatile Memory (eNVM)
- Triple Speed Ethernet (TSE) 10/100/1000 Mbps MAC
- USB 2.0 High Speed On-The-Go (OTG) Controller with ULPI Interface
- CAN Controller, 2.0B Compliant, Conforms to ISO11898-1, 32 Transmit and 32 Receive Buffers
- Two Each: SPI, I^2C, Multi-Mode UARTs (MMUART) Peripherals
- Hardware Based Watchdog Timer
- 1 General Purpose 64-Bit (or two 32-bit) Timer(s)
- Real-Time Calendar/Counter (RTC)
- DDR Bridge (4-Port Data R/W Buffering Bridge to DDR Memory) with 64-Bit AXI Interface
- Non-Blocking, Multi-Layer AHB Bus Matrix Allowing Multi-Master Scheme Supporting 10 Masters and 7 Slaves
- Two AHB-Lite/APB3 Interfaces to FPGA Fabric (Master/Slave Capable)
- Two DMA Controllers to Offload Data Transactions from the Cortex-M3 Processor
  - 8-channel Peripheral DMA (PDMA) for Data Transfer Between MSS Peripherals and Memory
  - High-Performance DMA (HPDMA) for Data Transfer Between eSRAM and DDR Memories

Clocking Resources

- Clock Sources
  - Up to Two High Precision 32 KHz to 20 MHz Main Crystal Oscillator
  - 1 MHz Embedded RC Oscillator
  - 50 MHz Embedded RC Oscillator
- Up to 6 Clock Conditioning Circuits (CCCs) with Up to 6 Integrated Analog PLLs
  - Output Clock with 6 Output Phases and 45° Phase Difference (Multiply/Divide, and Delay Capabilities)
  - Frequency: Input 1 MHz to 200 MHz, Output 20 MHz to 400 MHz

High Speed Serial Interfaces

- Up to 4 SERDES Lanes, Each Supporting:
  - Native SERDES Interface Facilitates Implementation of Serial RapidIO in Fabric or an SGMII Interface to the Ethernet MAC in MSS
  - PCI Express (PCIe) Endpoint Controller
    - x1, x2, x4 Lane PCI Express Core
    - Up to 2 Kbytes Maximum Payload Size
    - 64-Bit/32-Bit AXI and 64-Bit/32-Bit AHB Master and Slave Interfaces to the Application Layer

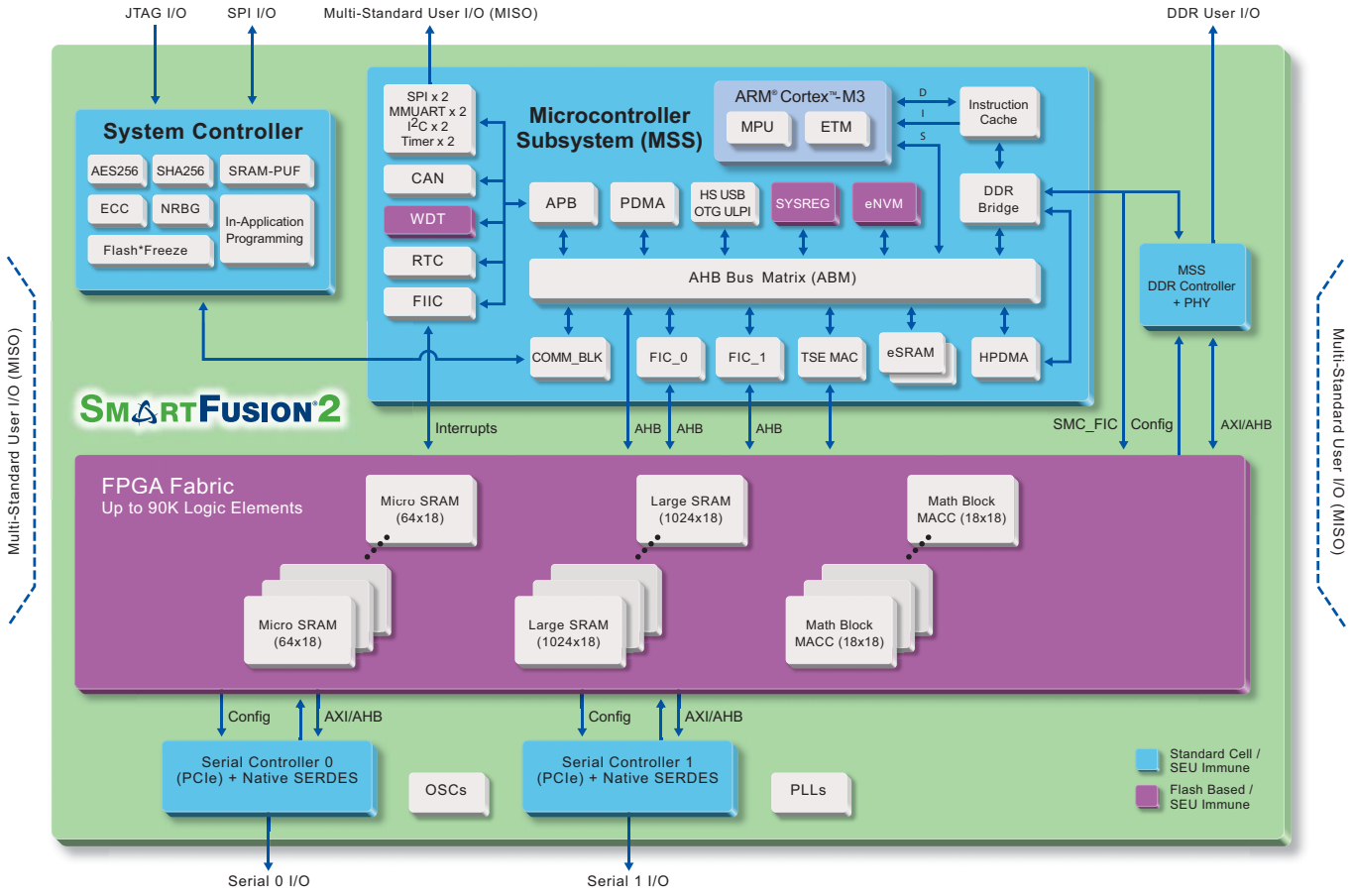
High Speed Memory Interfaces

- High Speed DDRx Memory Controllers
  - MSS DDR (MDDR) Controllers
  - Supports LPDDR/DDR2/DDR3
  - Maximum 333 MHz DDR Clock Rate
  - SECDED Enable/Disable Feature
  - Supports Various DRAM Bus Width Modes, x8, x9, x16, x18
  - Supports Command Reordering to Optimize Memory Efficiency
  - Supports Data Reordering, Returning Critical Word First for Each Command
- SDRAM Support through the SMC_FIC and Additional Soft SDRAM Memory Controller

Operating Voltage and I/Os

- 1.2 V Core Voltage
- Multi-Standard User I/Os (MSIO/MSIOD)
  - LVTTL/LVCMOS 3.3 V (MSIO Only)
  - LVCMOS 1.2 V, 1.5 V, 1.8 V, 2.5 V
  - DDR (SSTL2_1, SSTL2_2)
  - LVDS, MLVDS, Mini-LVDS, RSDS Differential Standards
  - PCI
  - LVPECL (receiver only)
- DDR I/Os (DDRIO)
  - DDR2, DDR3, LPDDR, SSTL2, SSTL18, HSTL
  - LVCMOS 1.2 V, 1.5 V, 1.8 V, 2.5 V

SmartFusion2 SoC FPGA Block Diagram



Acronyms

AES	Advanced Encryption Standard
AHB	Advanced High-Performance Bus
APB	Advanced Peripheral Bus
AXI	Advanced eXtensible Interface
COMM_BLK	Communication Block
DDR	Double Data Rate
DPA	Differential Power Analysis
ECC	Elliptic Curve Cryptography
EDAC	Error Detection and Correction
ETM	Embedded Trace Macrocell
FIC	Fabric Interface Controller
FIIC	Fabric Interface Interrupt Controller
HS USB OTG	High Speed USB 2.0 On-The-Go
IAP	In-Application Programming
MACC	Multiply-Accumulate
MDDR	DDR2/3 Controller in MSS
MMUART	Multi-Mode UART
MPU	Memory Protection Unit
MSIO	Multi-Standard I/O
MSS	Microcontroller Subsystem
PUF	Physically Unclonable Function
SECDED	Single Error Correct Double Error Detect
SEU	Single Event Upset
SHA	Secure Hashing Algorithm
SMC_FIC	Soft Memory Controller
TSE	Triple Speed Ethernet (10/100/1000 Mbps)
ULPI	UTMI + Low Pin Interface
UTMI	USB 2.0 Transceiver Macrocell Interface
WDT	Watchdog Timer

Table 1 • SmartFusion2 SoC FPGA Product Family [2]

	Features	M2S005S	M2S010TS	M2S025TS	M2S060TS	M2S090TS
Logic/DSP	Maximum Logic Elements (4LUT + DFF)[1]	6,060	12,084	27,696	56,520	86,184
	Math Blocks (18x18)	11	22	34	72	84
	Fabric Interface Controllers (FICs)	1			1	
	PLLs and CCCs	2		6		
	Data Security	AES256, SHA256, RNG			AES256, SHA256, RNG, ECC, PUF	
MSS	Cortex-M3 + Instruction cache	Yes				
	eNVM (K Bytes)	128	256			512
	eSRAM (K Bytes)	64				
	eSRAM (K Bytes) Non SECDED	80				
	CAN, 10/100/1000 Ethernet, HS USB	1 each				
	Multi-Mode UART, SPI, I2C, Timer	2 each				
Fabric Memory	LSRAM 18 K Blocks	10	21	31	69	109
	uSRAM1 K Blocks	11	22	34	72	112
	Total RAM (K bits)	191	400	592	1314	2074
High Speed	DDR Controllers (Count x Width)	1x18			1x18	
	SERDES Lanes (T)	0	4			
	PCIe End Points	0	1		2	
User I/Os	MSIO (3.3 V)	119	123	157	271	309
	MSIOD (2.5 V)	28	40	40	40	40
	DDRIO (2.5 V)	66	70	70	76	76
	Total User I/O	209	233	267	387	425

Note:

1. *Total logic may vary based on utilization of DSP and memories in the design. See the UG0445: IGLOO2 and SmartFusion2 Fabric User Guide for details.*
2. *Feature availability is package dependent.*

I/Os Per Package

Table 2 • I/Os per Package and Package Options

Package Options								
Type	**VFG256***		**VFG400***		**FGG484***		**FGG676***	
Pitch (mm)	0.8		0.8		1.0		1.0	
Length x Width (mm)	14x14		17x17		23x23		27x27	
Device	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes
M2S005S	161	-	171	-	209	-		
M2S010TS	138	2	195	4	233	4		
M2S025TS	138	2	207	4	267	4		
M2S060TS			207	4	267	4	387	4
M2S090TS					267	4	425	4

*Note: *All Automotive packages are RoHS compliant and available in lead free options only.*

Shade indicates that device packages have vertical migration capability

Table 3 • Features per Device/Package Combination

Package	Devices	MDDR	Crystal Oscillators	3.125 Gbps SERDES Lanes	PCIe Endpoints	ULPI	UTMI	MSIO (3.3 V max)[3]	MSIOD (2.5 V max)[4]	DDRIO (2.5 V max)	Total User I/O
VFG256[5]	M2S005S	-	2	-	-	1	1	119	12	30	161
	M2S010TS	x18[1]	2	2	1	1	1	66	8	64	138
	M2S025TS	x18[1]	2	2	1	1	1	66	8	64	138
VFG400[5]	M2S005S	x18[1]	2	-	-	1	1	79	28	64	171
	M2S010TS	x18[1]	2	4	1	1	1	99	32	64	195
	M2S025TS	x18[1]	2	4	1	1	1	111	32	64	207
	M2S060TS	x18[1]	2	4	2	1	1	111	32	64	207
FGG484[5]	M2S005S	x18[1]	2	-	-	1	1	115	28	66	209
	M2S010TS	x18[1]	2	4	1	1	1	123	40	70	233
	M2S025TS	x18[1]	2	4	1	1	1	157	40	70	267
	M2S060TS	x18[1]	2	4	2	1	1	157	40	70	267
	M2S090TS	x18[1]	2	4	2	1	1	157	40	70	267
FGG676[5]	M2S060TS	x18[1]	2	4	2	1	1	271	40	76	387
	M2S090TS	x18[1]	2	4	2	1	1	309	40	76	425

Notes:

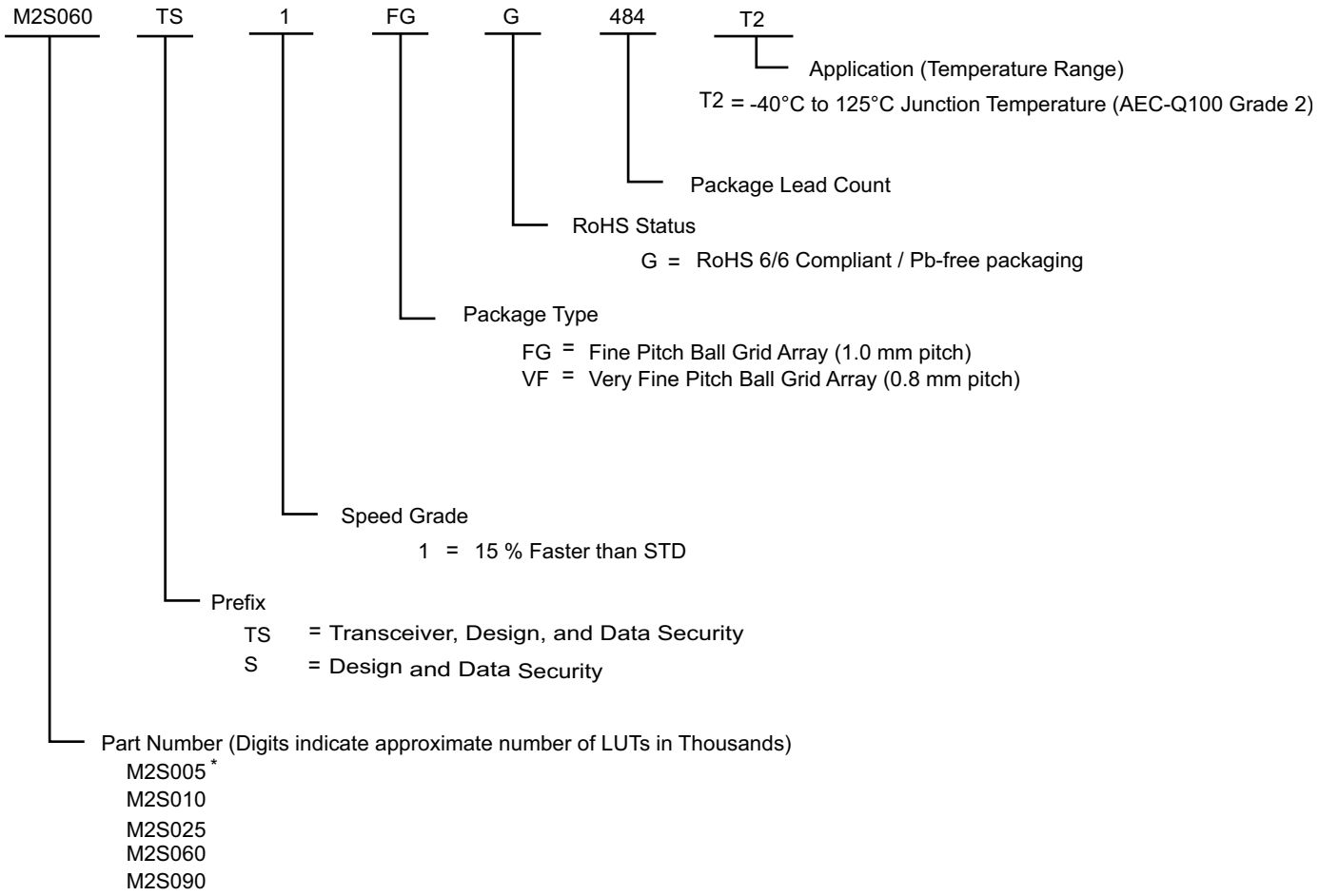
1. *DDR supports x18, x16, x9, and x8 modes.*
2. *DDR supports x18 and x16 modes.*
3. *Number of differential MSIO is Number of MSIOs/2 for even and (Number of MSIOs-1)/2 for odd MSIO supports LVDS 3.3/2.5 standard.*
4. *Number of differential MSIOD is Number of MSIODs/2 for even and (Number of MSIODs-1)/2 for odd MSIOD supports only LVDS 2.5 standard.*
5. *All Automotive packages are RoHS compliant and available in lead free options only.*

Table 4 • Available Programming Interfaces

Package	Devices	JTAG	SPI_0	Flash_GOLDEN_N	System Controller SPI Port
VFG256*	M2S005S	Yes	Yes	Yes	Yes
	M2S010TS	Yes	Yes	Yes	No
	M2S025TS	Yes	Yes	Yes	No
VFG400*	M2S005S	Yes	Yes	Yes	Yes
	M2S010TS	Yes	Yes	Yes	Yes
	M2S025TS	Yes	Yes	Yes	Yes
	M2S060TS	Yes	Yes	Yes	Yes
FGG484*	M2S005S	Yes	Yes	Yes	Yes
	M2S010TS	Yes	Yes	Yes	Yes
	M2S025TS	Yes	Yes	Yes	Yes
	M2S060TS	Yes	Yes	Yes	Yes
	M2S090TS	Yes	Yes	Yes	Yes
FGG676*	M2S060TS	Yes	Yes	Yes	Yes
	M2S090TS	Yes	Yes	Yes	Yes

*Note: *All Automotive packages are RoHS compliant and available in lead free options only.*

SmartFusion2 Ordering Information



Note: *M2S005 devices are not available with Transceivers.

SmartFusion2 Device Status

Refer to the *DS0134: SmartFusion2 SoC and IGLOO2 FPGA Automotive Grade 2* for device status.

SmartFusion2 Datasheet and Pin Descriptions

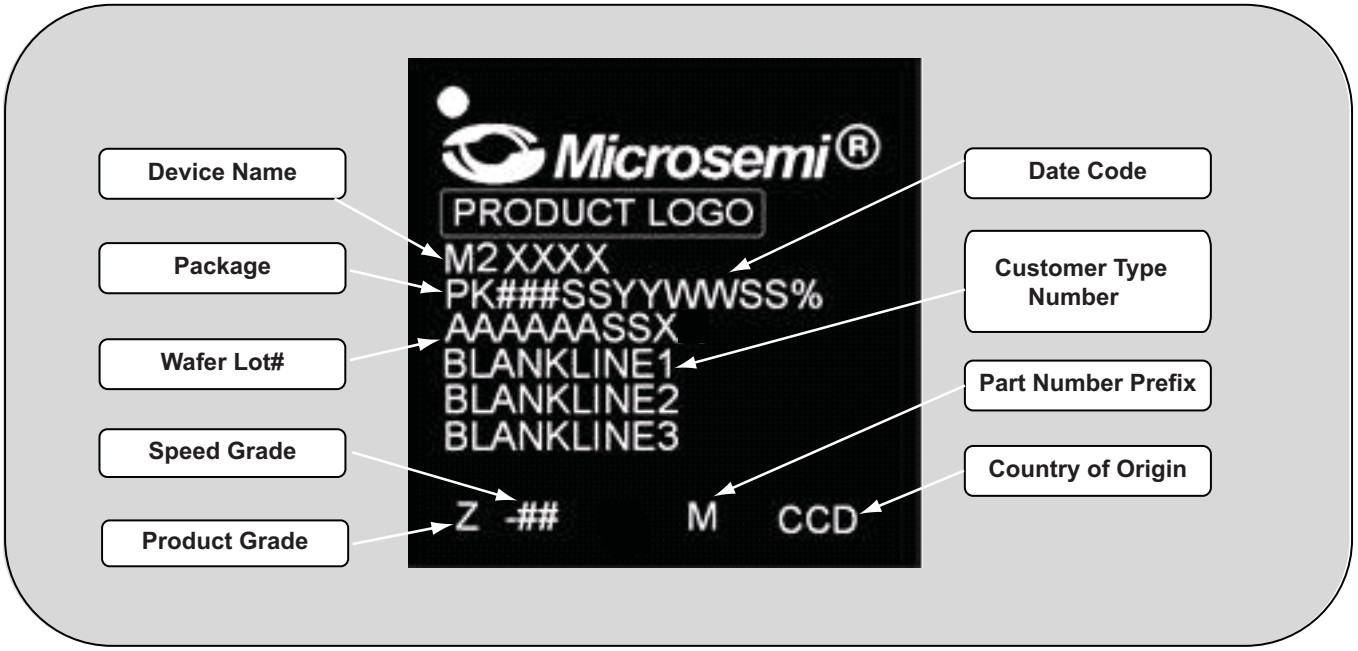
The datasheet and pin descriptions are published separately:

DS0134: SmartFusion2 SoC and IGLOO2 FPGA Automotive Grade 2

SmartFusion2 Pin Descriptions

Marking Specification Details

Microsemi normally topside marks the full ordering part number on each device. The figure below provides the details for each character code present on Microsemi's SmartFusion2 SoC FPGA devices.



Description

- Device Name (M2XXXX): M2S for SmartFusion2 Devices
  Example: M2S060TS
- Package (PK###): Available Package as below
  PK: Package code†:
  FGG: Fine Pitch BGA, 1.00 mm pitch
  VFG: Very Fine Pitch BGA, 0.8 mm pitch
  ###: Number of Pins: Can be three or four digits. For example,256
- Wafer Lot (AAAAAASSX): Microsemi Wafer lot #
  AAAAAA: Wafer lot number

† All Automotive packages are RoHS compliant and available in lead free options only.

X: One digit die revision code
SS: Two Blank Spaces

- Speed Grade (-##): Speed Binning Number
  Blank: Standard speed grade
  -1: -1 Speed grade
- Product grade (Z): Product Grade; assigned as follows
  Blank/C: Commercial
  ES: Engineering Samples
  I: Industrial
  M: Military Temperature
  PP: Pre Production
  T2: Automotive temperature Grade 2
- Date Code (YYWWSS%): Assembly Date Code
  YY: Last two digits for seal year
  WW: Work week the part was sealed
  SS: Two blank spaces
  %: Can be digital number or character for new product
- Customer Type Number: As specified on lot traveler
  GW: Gold Wire bond
- Part number Prefix: Part number prefix, assigned as below
  Blank: Design Security
  S: Design and Data Security
  TS: Transceiver, Design, and Data Security
- Country of Origin (CCD): Assembly house country location
  Country name: Country Code
  China: CHN
  Hong Kong: HKG
  Japan: JPN
  Korea, South: KOR
  Philippines: PHL
  Taiwan: TWN
  Singapore: SGP
  United States: USA
  Malaysia: MYS

1 – SmartFusion2 Device Family Overview

Microsemi's SmartFusion2 SoC FPGAs integrate fourth generation flash-based FPGA fabric, an ARM Cortex-M3 processor, and high-performance communications interfaces on a single chip. The SmartFusion2 FPGA is the industry's lowest power, the most secure, and has the highest reliability of any programmable logic solution.

SmartFusion2 FPGAs offer up to 3.6X the gate density and up to 2X the performance of previous flash-based FPGA families and includes multiple memory blocks and multiply accumulate blocks for DSP processing. The 133 MHz ARM Cortex-M3 processor is enhanced with ETM and 8 Kbyte instruction cache, and additional peripherals including CAN, Gigabit Ethernet, and high speed USB. High speed serial interfaces enable PCIe, while DDR2/DDR3 memory controllers provide high speed memory interfaces.

SmartFusion2 Chip Layout

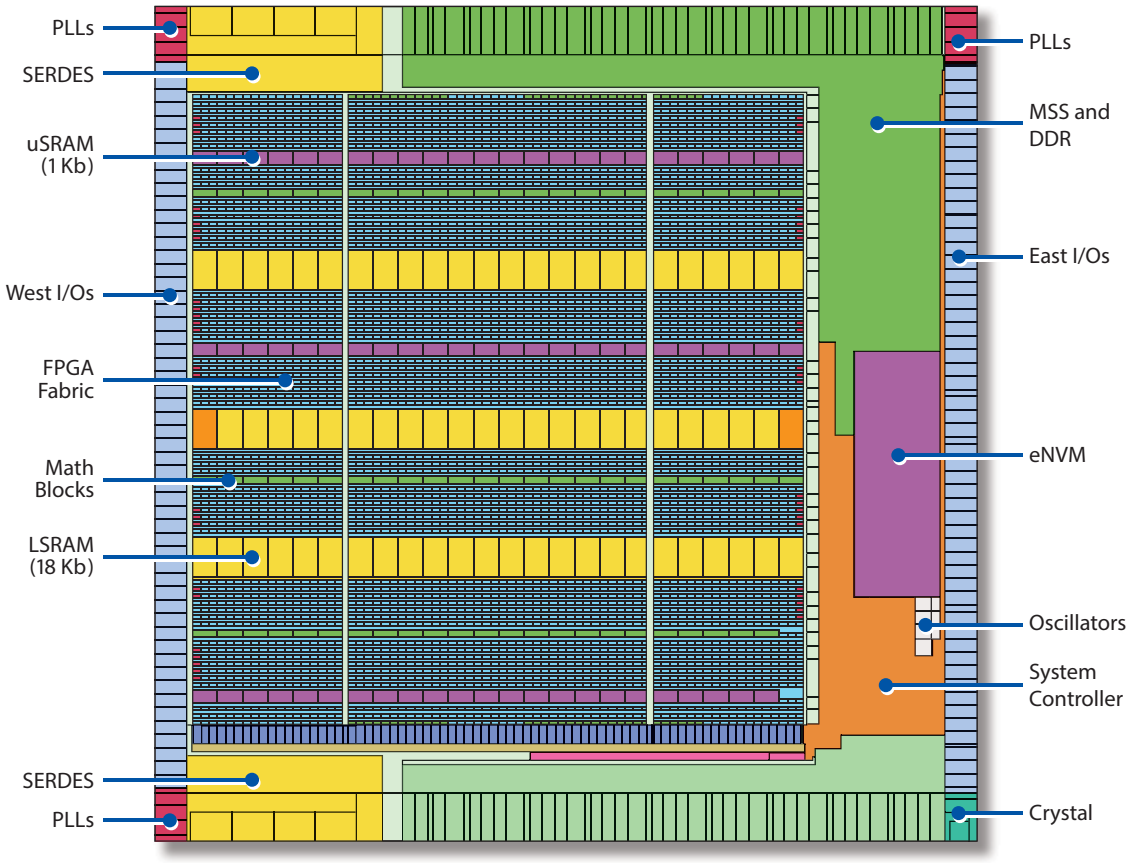


Figure 1-1 • **SmartFusion2 Chip Layout**

Reliability

SmartFusion2 flash-based fabric has zero FIT configuration rate due to its single event upset (SEU) immunity, which is critical in reliability applications. The flash fabric also has the advantage that no external configuration memory is required, making the device instant-on; it retains configuration when powered off. To complement this unique FPGA capability, SmartFusion2 devices add reliability to many other aspects of the device. Single Error Correct Double Error Detect (SECDED) protection is implemented on the Cortex-M3 embedded scratch pad memory, Ethernet, CAN and USB buffers, and is optional on the DDR memory controllers. This means that if a one-bit error is detected, it will be corrected. Errors of more than one bit are detected only and not corrected. SECDED error signals are brought to the FPGA fabric to allow the user to monitor the status of these protected internal memories. Other areas of the architecture are implemented with latches, which are more resistant to SEUs. Therefore, no correction is needed in these locations: DDR bridges (MSS, MDDR), instruction cache and MMUART, SPI, and PCIe FIFOs.

Highest Security Devices

Building further on the intrinsic security benefits of flash nonvolatile memory technology, the SmartFusion2 family incorporates essentially all the legacy security features that made the original SmartFusion®, Fusion®, IGLOO, and ProASIC®3 third-generation flash FPGAs and cSoCs the gold standard for secure devices in the PLD industry. In addition, the fourth-generation flash-based SmartFusion2 SoC FPGAs add many unique design and data security features and use models new to the PLD industry.

Design Security vs. Data Security

When classifying security attributes of programmable logic devices (PLDs), a useful distinction is made between design security and data security.

Design Security

Design security is protecting the intent of the owner of the design, such as keeping the design and associated bitstream keys confidential, preventing design changes (for example, insertion of Trojan Horses), and controlling the number of copies made throughout the device life cycle. Design security may also be known as intellectual property (IP) protection. It is one aspect of anti-tamper (AT) protection. Design security applies to the device from initial production, includes any updates such as in-the-field upgrades, and can include decommissioning of the device at the end of its life, if desired. Good design security is a prerequisite for good data security.

The following are the main design security features supported.

Table 1-1 • **Design Security Features**

Features	**M2S005S**	**M2S060TS**
	M2S010TS	**M2S090TS**
	M2S025TS	
Software Memory Protection Unit (MPU)	x	x
FlashLock™ Passcode Security (256-bit)	x	x
Flexible security settings using flash lock-bits	x	x
Encrypted/Authenticated Design Key Loading	x	x
Symmetric Key Design Security (256-bit)	x	x
Design Key Verification Protocol	x	x
Encrypted/Authenticated Configuration Loading	x	x
Certificate-of-Conformance (C-of-C)	x	x
Back-Tracking Prevention (also known as, Versioning)	x	x
Device Certificate(s) (Anti-Counterfeiting)	x	x
Support for Configuration Variations	x	x
Fabric NVM and eNVM Integrity Tests	x	x
Information Services (S/N, Cert., USERCODE, and others)	x	x
Tamper Detection	x	x
Tamper Response (includes Zeroization)	x	x
ECC Public Key Design Security (384-bit)		x
Hardware Intrinsic Design Key (SRAM-PUF)		x

Data Security

Data security is protecting the information the FPGA is storing, processing, or communicating in its role in the end application. If, for example, the configured design is implementing the key management and encryption portion of a secure military radio, data security could entail encrypting and authenticating the radio traffic, and protecting the associated application-level cryptographic keys. Data security is closely related to the terms information assurance (IA) and information security. All SmartFusion2 devices incorporate enhanced design security, making them the most secure programmable logic devices ever made. Select SmartFusion2 models also include an advanced set of on-chip data security features that make designing secure information assurance applications easier and better than ever before.

Table 1-2 • **Data Security Features**

Features	**M2S005S**	**M2S060TS**
	M2S010TS	**M2S090TS**
	M2S025TS	
CRI Pass-through DPA Patent License	x	x
Hardware Firewalls protecting access to memories	x	x
Non-Deterministic Random Bit Generator Service	x	x
AES-128/256 Service (ECB, OFB, CTR, CBC modes)	x	x
SHA-256 Service	x	x
HMAC-SHA-256 Service	x	x
Key Tree Service	x	x
PUF Emulation (Pseudo-PUF)	x	
PUF Emulation (SRAM-PUF)		x
ECC Point-Multiplication Service		x
ECC Point-Addition Service		x
User SRAM-PUF Enrollment Service		x
User SRAM-PUF Activation Code Export Service		x
SRAM-PUF Intrinsic Key Gen. & Enrollment Service		x
SRAM-PUF Key Import & Enrollment Service		x
SRAM-PUF Key Regeneration Service		x

Low Power

Microsemi's flash-based FPGA fabric results in extremely low power design implementation with static power as low as 7.5 mW (for 6,060 LE device). Flash*Freeze (F*F) technology provides an ultra-low power static mode (Flash*Freeze mode) for SmartFusion2 devices, with power less than 6.12 mW for the largest device (86,184 LE device). F*F mode entry retains all the SRAM and register information and the exit from F*F mode achieves rapid recovery to active mode.

High-Performance FPGA Fabric

Built on 65 nm process technology, the SmartFusion2 FPGA fabric is composed of 4 building blocks: the logic module, the large SRAM, the micro SRAM and the mathblock. The logic module is the basic logic element and has advanced features:

- A fully permutable 4-input LUT (look-up table) optimized for lowest power
- A dedicated carry chain based on carry look-ahead technique
- A separate flip-flop which can be used independently from the LUT

The 4-input look-up table can be configured either to implement any 4-input combinatorial function or to implement an arithmetic function where the LUT output is XORed with carry input to generate the sum output.

Dual-Port Large SRAM (LSRAM)

Large SRAM (RAM1Kx18) is targeted for storing large memory for use with various operations. Each LSRAM block can store up to 18,432 bits. Each RAM1Kx18 block contains two independent data ports: Port A and Port B. The LSRAM is synchronous for both Read and Write operations. Operations are triggered on the rising edge of the clock. The data output ports of the LSRAM have pipeline registers which have control signals that are independent of the SRAM's control signals.

Three-Port Micro SRAM (uSRAM)

Micro SRAM (RAM64x18) is the second type of SRAM which is embedded in the fabric of SmartFusion2 devices. RAM64x18 uSRAM is a 3-port SRAM; it has two read ports (Port A and Port B) and one write port (Port C). The two read ports are independent of each other and can perform Read operations in both synchronous and asynchronous modes. The write port is always synchronous. The uSRAM block is approximately 1 KB (1,152 bits) in size. These uSRAM blocks are primarily targeted for building embedded FIFOs to be used by any embedded fabric masters.

Mathblocks for DSP Applications

The fundamental building block in any digital signal processing algorithm is the multiply-accumulate function. SmartFusion2 FPGAs implement a custom 18x18 Multiply-Accumulate (18x18 MACC) block for efficient implementation of complex DSP algorithms such as finite impulse response (FIR) filters, infinite impulse response (IIR) filters, and fast Fourier transform (FFT) for filtering and image processing applications.

Each mathblock has the following capabilities:

- Supports 18x18 signed multiplications natively (A[17:0] x B[17:0])
- Supports dot product; the multiplier computes:

  $(A[8:0] \times B[17:9] + A[17:9] \times B[8:0]) \times 2^9$
- Built-in addition, subtraction, and accumulation units to combine multiplication results efficiently

In addition to the basic MACC function, DSP algorithms typically need small amounts of RAM for coefficients and larger RAMs for data storage. SmartFusion2 micro RAMs are ideally suited to serve the needs of coefficient storage while the large RAMs are used for data storage.

Microcontroller Subsystem (MSS)

The microcontroller subsystem (MSS) contains a high-performance integrated Cortex-M3 processor, running at up to 133 MHz. The MSS contains an 8 Kbyte instruction cache to provide low latency access to internal eNVM and external DDR memory. The MSS provides multiple interfacing options to the FPGA fabric in order to facilitate tight integration between the MSS and user logic in the fabric.

ARM Cortex-M3 Processor

The MSS uses the latest revision (r2p1) of the ARM Cortex-M3 processor. Microsemi's implementation includes the optional embedded trace macrocell (ETM) features for easier development and debug and the memory protection unit (MPU) for real-time operating system support.

Cache Controller

In order to minimize latency for instruction fetches when executing firmware out of off-chip DDR or on-chip eNVM, an 8 Kbyte, 4-way set associative instruction cache is implemented. This provides zero wait state access for cache hits and is shared by both I and D code buses of the Cortex-M3 processor. In the event of cache misses, cache lines are filled, replacing existing cache entries based on a least recently used (LRU) algorithm.

There is a configurable option available to operate the cache in a locked mode, whereby a fixed segment of code from either the DDR or eNVM is copied into the cache and locked there, so that it is not replaced when cache misses occur. This would be used for performance-critical code.

It is also possible to disable the cache altogether, which is desirable in systems requiring very deterministic execution times.The cache is implemented with SEU tolerant latches.

DDR Bridge

The DDR bridge is a data bridge between four AHB bus masters and a single AXI bus slave. The DDR bridge accumulates AHB writes into write combining buffers prior to bursting out to external DDR memory. The DDR bridge also includes read combining buffers, allowing AHB masters to efficiently read data from the external DDR memory from a local buffer. The DDR bridge optimizes reads and writes from multiple masters to a single external DDR memory. Data coherency rules between the four masters and the external DDR memory are implemented in hardware. The DDR bridge contains three write combining / read buffers and one read buffer. All buffers within the DDR bridge are implemented with SEU tolerant latches and are not subject to the single event upsets (SEUs) that SRAM exhibits. SmartFusion2 devices implement two DDR bridges in the MSS, and MDDR subsystems.

AHB Bus Matrix (ABM)

The AHB bus matrix (ABM) is a non-blocking, AHB-Lite multi-layer switch, supporting 10 master interfaces and 7 slave interfaces. The switch decodes access attempts by masters to various slaves, according to the memory map and security configurations. When multiple masters are attempting to access a particular slave simultaneously, an arbiter associated with that slave decides which master gains access, according to a configurable set of arbitration rules. These rules can be configured by the user to provide different usage patterns to each slave. For example, a number of consecutive access opportunities to the slave can be allocated to one particular master, to increase the likelihood of same type accesses (all reads or all writes), which makes more efficient usage of the bandwidth to the slave.

System Registers

The MSS System registers are implemented as an AHB slave on the AHB bus matrix. This means the Cortex-M3 processor or a soft master in the FPGA fabric may access the registers and therefore control the MSS. The System registers can be initialized by user-defined flash configuration bits on power-up. Each register also has a flash bit to enable write protecting the contents of the registers. This allows the MSS system configuration to be reliably fixed for a given application.

Fabric Interface Controller (FIC)

The FIC block provides two separate interfaces between the MSS and the FPGA fabric: the MSS master (MM) and fabric master (FM). Each of these interfaces can be configured to operate as AHB-Lite or APB3. Depending on device density, there are up to two FIC blocks present in the MSS (FIC_0 and FIC_1).

Embedded SRAM (eSRAM)

The MSS contains two blocks of 32 KB eSRAM, giving a total of 64 KB. Having the eSRAM arranged as two separate blocks allows the user to take advantage of the Harvard architecture of the Cortex-M3 processor. For example, code could be located in one eSRAM, while data, such as the stack, could be located in the other.

The eSRAM is designed for Single Error Correct Double Error Detect (SECDED) protection. When SECDED is disabled, the SRAM usually used to store SECDED data may be reused as an extra 16 KB of eSRAM.

Embedded NVM (eNVM)

The MSS contains up to 512 KB of eNVM (64 bits wide). Accesses to the eNVM from the Cortex-M3 processor are cacheable.

DMA Engines

Two DMA engines are present in the MSS: high-performance DMA and peripheral DMA.

HPDMA

HPDMA engine provides efficient memory to memory data transfers between an external DDR memory and internal eSRAM. This engine has two separate AHB-Lite interfaces—one to the MDDR bridge and the other to the AHB bus matrix. All transfers by the HPDMA are full word transfers.

PDMA

The PDMA engine is tuned for offloading byte-intensive operations, involving MSS peripherals, to and from the internal eSRAMs. Data transfers can also be targeted to user logic/RAM in the FPGA fabric.

APB Configuration Bus

On every SmartFusion2 device, an APB configuration bus is present to allow the user to initialize the SERDES ASIC blocks, the fabric DDR memory controller, and user instantiated peripherals in the FPGA fabric.

Peripherals

A large number of communications and general purpose peripherals are implemented in the MSS.

USB Controller

The MSS contains a high speed USB 2.0 On-The-Go (OTG) controller with the following features:

- Operates either as the function controller of a high-speed / full-speed USB peripheral or as the host/peripheral in point-to-point or multi-point communications with other USB functions.
- Complies with the USB 2.0 standard for high-speed functions and with the *On-The-Go* supplement to the USB 2.0 specification.
- Supports OTG communications with one or more high-speed, full-speed, or low-speed devices.

TSE Ethernet MAC

The triple speed Ethernet (TSE) MAC supports IEEE 802.3 10/100/1000 Mbps Ethernet operation. The following PHY interfaces are directly supported by the MAC:

- GMII
- MII
- TBI

The Ethernet MAC hardware implements the following functions:

- 4 KB internal transmit FIFO and 8 KB internal receive FIFO
- IEEE 802.3X full-duplex flow control
- DMA of Ethernet frames between internal FIFOs and system memory (such as eSRAM or DDR)
- Cut-through operation
- SECDED protection on internal buffers

SGMII PHY Interface

SGMII mode is implemented by means of configuring the MAC for 10-bit interface (TBI) operation, allocating one of the high-speed serial channels to SGMII, and by implementing custom logic in the fabric.

Communication Block (COMM_BLK)

The COMM block provides a UART-like communications channel between the MSS and the system controller. System services are initiated through the COMM block.

SPI

The SPI controller is compliant with the Motorola SPI, Texas Instruments synchronous serial, and National Semiconductor MICROWIRE™ formats. In addition, the SPI supports interfacing to large SPI flash and EEPROM devices by way of the slave protocol engine. The SPI controller supports both Master and Slave modes of operation.

The SPI controller embeds two 4×32 (depth × width) FIFOs for receive and transmit. These FIFOs are accessible through Rx data and Tx data registers. Writing to the Tx data register causes the data to be written to the transmit FIFO. This is emptied by transmit logic. Similarly, reading from the Rx data register causes data to be read from the receive FIFO.

Multi-Mode UART (MMUART)

SmartFusion2 devices contain two identical multi-mode universal asynchronous/synchronous receiver/transmitter (MMUART) peripherals that provide software compatibility with the popular 16550 device. They perform serial-to-parallel conversion on data originating from modems or other serial devices, and perform parallel-to-serial conversion on data from the Cortex-M3 processor to these devices.

The following are the main features supported:

- Fractional baud rate capability
- Asynchronous and synchronous operation
- Full programmable serial interface characteristics
  - Data width is programmable to 5, 6, 7, or 8 bits
  - Even, odd, or no-parity bit generation/detection
  - 1,1½, and 2 stop bit generation
- 9-bit address flag capability used for multidrop addressing topologies

I^2C

SmartFusion2 devices contain two identical master/slave I^2C peripherals that perform serial to-parallel conversion on data originating from serial devices, and perform parallel-to-serial conversion on data from the ARM Cortex-M3 processor, or any other bus master, to these devices. The following are the main features supported:

- I^2C v2.1
  - 100 Kbps
  - 400 Kbps
- Dual-slave addressing
- SMBus v2.0
- PMBus v1.1

Clock Sources: On-Chip Oscillators, PLLs, and CCCs

SmartFusion2 devices have two on-chip RC oscillators—a 1 MHz RC oscillator and a 50 MHz RC oscillator—and up to two main crystal oscillators (32 kHz–20 MHz). These are available to the user for generating clocks to the on-chip resources and the logic built on the FPGA fabric array. The second crystal oscillator available on the SmartFusion2 devices is dedicated for RTC clocking. These oscillators (except the RTC crystal oscillator) can be used in conjunction with the integrated user phase-locked loops (PLLs) and fabric clock conditioning circuits (FAB_CCC) to generate clocks of varying frequency and phase. In addition to being available to the user, these oscillators are also used by the system controller, power-on reset circuitry, MSS during Flash*Freeze mode, and the RTC.

SmartFusion2 devices have up to six fabric CCC (FAB_CCC) blocks and a dedicated PLL associated with each CCC to provide flexible clocking to the FPGA fabric portion of the device. The user has the freedom to use any of the six PLLs and CCCs to generate the fabric clocks and the internal MSS clock from the base fabric clock (CLK_BASE). There is also a dedicated CCC block for the MSS (MSS_CCC) and an associated PLL (MPLL) for MSS clocking and de-skewing the CLK_BASE clock. The fabric alignment clock controller (FACC), part of the MSS CCC, is responsible for generating various aligned clocks required by the MSS for correct operation of the MSS blocks and synchronous communication with the user logic in the FPGA fabric.

High Speed Serial Interfaces

SERDES Interface

SmartFusion2 has up to four 3.125 Gbps SERDES transceivers, each supporting the following:

- 4 SERDES lanes
- The native SERDES interface facilitates implementation of Serial RapidIO (SRIO) in fabric or an SGMII interface for the Ethernet MAC in MSS

PCIe

PCIe is a high speed, packet-based, point-to-point, low pin count, serial interconnect bus. The SmartFusion2 family has two hard high-speed serial interface blocks. Each SERDES block contains a PCIe system block. The PCIe system is connected to the SERDES block and following are the main features supported:

- Supports x1, x2, and x4 lane configuration
- Endpoint configuration only
- PCI Express Base Specification Revision 2.0
- 2.5 Gbps compliant
- Embedded receive (2 KB), transmit (1 KB) and retry (1 KB) buffer dual-port RAM implementation
- Up to 2 Kbytes maximum payload size
- 64-bit AXI or 32-bit AHB-Lite Master and Slave interface to the application layer
- 32-bit APB interface to access configuration and status registers of PCIe system
- Up to 3 x 64 bit base address registers
- 1 virtual channel (VC)

High Speed Memory Interfaces: DDRx Memory Controllers

There are up to three DDR subsystems, MDDR (MSS DDR) present in SmartFusion2 devices. Each subsystem consists of a DDR controller, PHY, and a wrapper. The MDDR has an interface from the MSS and fabric.

The following are the main features supported by MDDR:

- Support for LPDDR, DDR2, and DDR3 memories
- Simplified DDR command interface to standard AMBA AXI/AHB interface
- Up to 667 Mbps (333 MHz double data rate) performance
- Supports 1, 2, or 4 ranks of memory
- Supports different DRAM bus width modes: x8, x9, x16, and x18
- Supports DRAM burst length of 2, 4, or 8 in full bus-width mode; supports DRAM burst length of 2, 4, 8, or 16 in half bus-width mode
- Supports memory densities up to 4 GB
- Supports a maximum of 8 memory banks
- SECDED enable/disable feature
- Embedded physical interface (PHY)
- Read and Write buffers in fully associative CAMs, configurable in powers of 2, up to 64 Reads plus 64 Writes
- Support for dynamically changing clock frequency while in self-refresh
- Supports command reordering to optimize memory efficiency
- Supports data reordering, returning critical word first for each command

MDDR Subsystem

The MDDR subsystem has two interfaces to the DDR. One is an AXI 64-bit bus from the DDR bridge within the MSS. The other is a multiplexed interface from the FPGA fabric, which can be configured as either a single AXI 64-bit bus or two 32-bit AHB-Lite buses. There is also a 16-bit APB configuration bus, which is used to initialize the majority of the internal registers within the MDDR subsystem after reset. This APB configuration bus can be mastered by the MSS directly or by a master in the FPGA fabric. Support for 3.3 V Single Data Rate DRAMs (SDRAM) can be obtained by using the SMC_FIC interface in the MDDR subsystem. Users would then instantiate a soft AHB or AXI SDRAM memory controller in the FPGA fabric and connect I/O ports to 3.3 V MSIO.

SmartFusion2 Development Tools

Design Software

Microsemi's Libero® System-on-Chip (SoC) is a comprehensive software toolset to design applications using the SmartFusion2 device. Libero SoC manages the entire design flow from design entry, synthesis and simulation, place and route, timing and power analysis, with enhanced integration of the embedded design flow.
System designers can leverage the easy-to-use Libero SoC that includes the following features:

- System Builder for creation of system level architecture
- Synthesis, DSP and debug support from Synopsys
- Simulation from Mentor Graphics
- Push-button design flow with power analysis and timing analysis
- SmartDebug for access to non-invasive probes within the SmartFusion2 devices
- Integrated firmware flows for SoftConsole (GNU/Eclipse), IAR®, and Keil™
- Operating system support includes uClinux™ from Emcraft Systems, FreeRTOS™, SAFERTOS® and uc/OS-III™ from Micrium

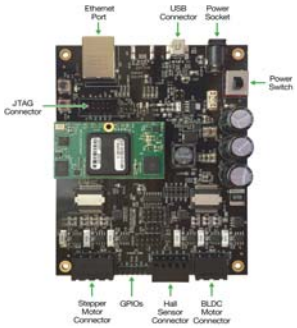
For more information refer to *Libero SoC*.

Design Hardware

Several SmartFusion2 kits are available for quick evaluation of the device features and prototyping. The Demo designs ensure faster learning for the users. For more information on kits, refer to *SmartFusion2 Kits*.

Table 1-3 lists the available SmartFusion2 kits.

***Table 1-3* • SmartFusion2 Kits**

SmartFusion2 Starter Kit The SmartFusion2 Starter Kit provides a cost effective platform for evaluation and development of a SmartFusion2 SoC FPGA based solution. The kit utilizes a miniature mezzanine form factor system-on-module, which integrates the SmartFusion2 device with 64 MB LPDDR, 16 MB SPI flash, and Ethernet PHY. The baseboard provides easy to use benchtop access to the SmartFusion2 SoC and interfaces.	
SmartFusion2 Security Evaluation Kit The SmartFusion2 Security Evaluation Kit is a low cost platform to evaluate the security, low power consumption, reliability and high integration capabilities of the SmartFusion2 device. This kit has a 90K LE device that allows a larger system to be implemented on the kit. The board contains 512 Mb LPDDR, 64 Mb SPI flash, X1 PCIe Edge connector, 4-SMA connectors, 10/100/1000 Ethernet and GPIO connector.	
SmartFusion2 Motor Control Kit The SmartFusion2 Motor Control Kit is used for quick evaluation of the motor control solution using the SmartFusion2 device. This kit supports two axis motor control (one BLDC motor and one stepper motor).	

IP Cores

SmartFusion2 SoC FPGAs contain an ARM Cortex-M3 processor and multiple peripherals hardcoded into the device. In addition to these, Microsemi offers many soft peripherals that can be placed in the FPGA fabric of the device. These include Core429, Core1553, CoreJESD204BRX/TX, CoreFRI, CoreFFT, and many other DirectCores. Refer to *IP Cores* for more information.

2 – Product Brief Information

List of Changes

The following table shows important changes made in this document for each revision.

Revision	Changes	Page
Revision 4 (October 2015)	Updated Table 1 (SAR 71997). Updated "SmartFusion2 Ordering Information" Diagram (SAR 71997). Updated "Marking Specification Details" content and diagram (SAR 71997). Updated "Low Power" content (SAR 71997). Updated Table 1-3 (SAR 71997).	1-IV 1-VII 1-VIII 1-4 1-12
Revision 3 (June 2015)	Removed 5G SERDES and instances of XAUI support (SAR 68715).	NA
	Updated "SERDES Interface" (SAR 68715).	1-9
Revision 2 (June 2015)	Changed the Document Title from “Automotive Grade SmartFusion2 SoC FPGAs Product Brief” to “Automotive Grade 2 SmartFusion2 SoC FPGAs Product Brief” (SAR 68572).	1-I
	Changed Microprocessor Subsystem Cortex-M3 processor range from 166 MHz to 133 MHz (SAR 68572).	1-I,1-II,1-1, and 1-6
Revision 1 (June 2015)	Initial release	NA

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device, as highlighted in the "SmartFusion2 Device Status" table on page VIII, is designated as either “Product Brief,” “Advance,” “Preliminary,” or “Production.” The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Production

This version contains information that is considered to be final.

Export Administration Regulations (EAR)

The products described in this document are subject to the Export Administration Regulations (EAR). They could require an approved export license prior to export from the United States. An export includes release of product or disclosure of technology to a foreign national inside or outside the United States.

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