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Kind regards,

Team Nexperia



# BUK764R0-75C

N-channel TrenchMOS standard level FET

Rev. 2 — 26 April 2011

Product data sheet

## 1. Product profile

### 1.1 General description

Standard level gate drive N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using advanced TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in high performance automotive applications.

### 1.2 Features and benefits

- AEC-Q101 compliant
- Avalanche robust
- Suitable for standard level gate drive
- Suitable for thermally demanding environment due to 175 °C rating

### 1.3 Applications

- 12 V Motor, lamp and solenoid loads
- High performance automotive power systems
- High performance Pulse Width Modulation (PWM) applications

### 1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	-	75	V
$I_D$	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C};$ see <a href="#">Figure 1</a> ; see <a href="#">Figure 4</a>	[1][2]	-	100	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C};$ see <a href="#">Figure 2</a>	-	-	333	W



**Table 1. Quick reference data ...continued**

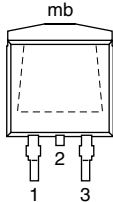
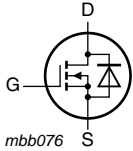
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ }^\circ\text{C};$ see <a href="#">Figure 7</a> ; see <a href="#">Figure 8</a>	-	3.4	4	mΩ
$I_{GSS}$	gate leakage current	$V_{DS} = 0\text{ V}; V_{GS} = 20\text{ V}; T_j = 25\text{ }^\circ\text{C}$	-	2	100	nA
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 100\text{ A}; V_{sup} \leq 75\text{ V}; R_{GS} = 50\text{ }\Omega; V_{GS} = 10\text{ V}; T_{j(init)} = 25\text{ }^\circ\text{C};$ unclamped	-	-	630	mJ

[1] Refer to document 9397 750 12572 for further information.

[2] Continuous current is limited by package.

## 2. Pinning information

**Table 2. Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain <sup>[1]</sup>		
3	S	source		
mb	D	mounting base; connected to drain		

**SOT404 (D2PAK)**

[1] It is not possible to make a connection to pin 2 of the SOT404 package.

## 3. Ordering information

**Table 3. Ordering information**

Type number	Package		Version
	Name	Description	
BUK764R0-75C	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

## 4. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$	-	75	V	
$V_{DGR}$	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	75	V	
$V_{GS}$	gate-source voltage		-20	20	V	
$I_D$	drain current	$T_{mb} = 25\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 1</a> ; see <a href="#">Figure 4</a>	<a href="#">[1][2]</a>	-	100	A
			<a href="#">[1][3]</a>	-	199	A
		$T_{mb} = 100\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 1</a>	<a href="#">[1][2]</a>	-	100	A
$I_{DM}$	peak drain current	$T_{mb} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; see <a href="#">Figure 4</a>	-	797	A	
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	-	333	W	
$T_{stg}$	storage temperature		-55	175	°C	
$T_j$	junction temperature		-55	175	°C	
<b>Source-drain diode</b>						
$I_S$	source current	$T_{mb} = 25\text{ °C}$	<a href="#">[3][1]</a>	-	199	A
			<a href="#">[3][2]</a>	-	100	A
$I_{SM}$	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$	-	797	A	
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 100\text{ A}$ ; $V_{sup} \leq 75\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; $V_{GS} = 10\text{ V}$ ; $T_{j(init)} = 25\text{ °C}$ ; unclamped	-	630	mJ	
$E_{DS(AL)R}$	repetitive drain-source avalanche energy	see <a href="#">Figure 3</a>	<a href="#">[4][5]</a>	-	-	J
			<a href="#">[6][7]</a>	-	-	J

[1] Refer to document 9397 750 12572 for further information.

[2] Continuous current is limited by package.

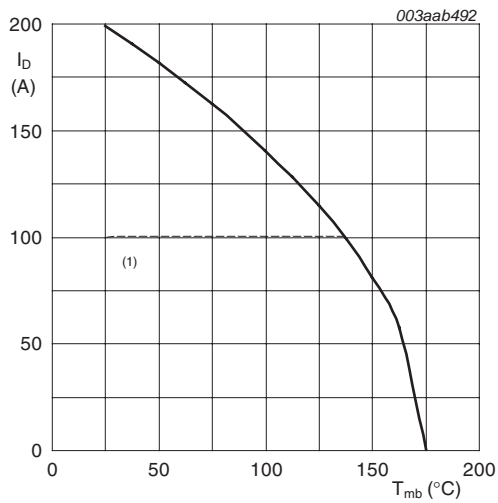
[3] Current is limited by power dissipation chip rating.

[4] Maximum value not quoted. Repetitive rating defined in avalanche rating figure.

[5] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.

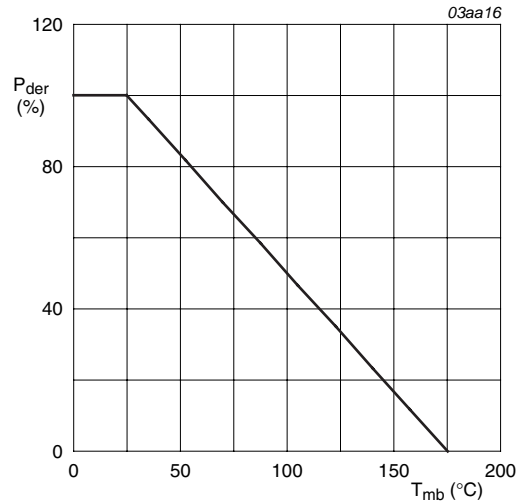
[6] Repetitive avalanche rating limited by an average junction temperature of 170 °C.

[7] Refer to application note AN10273 for further information.



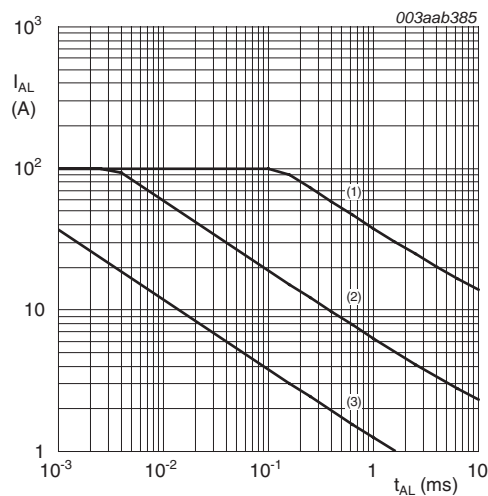
$V_{GS} \geq 10\text{ V}$   
 (1) Capped at 100 A due to package.

**Fig 1. Normalized continuous drain current as a function of mounting base temperature**

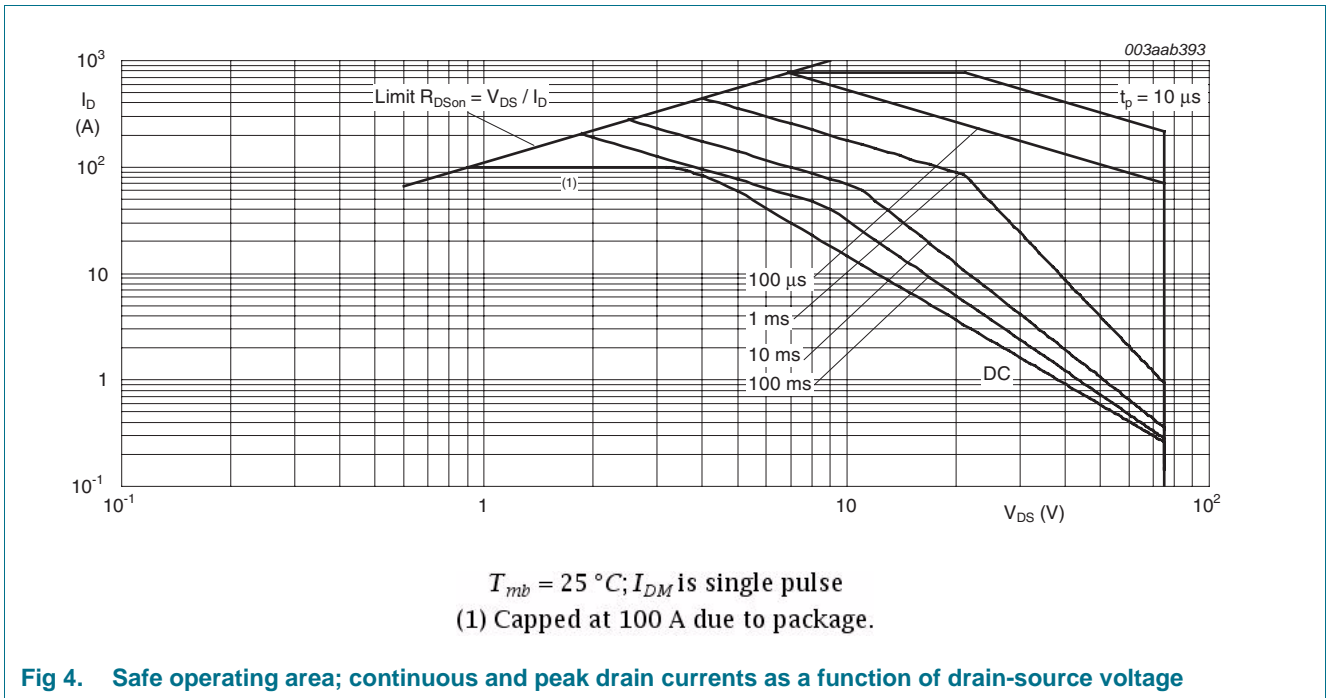


$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

**Fig 2. Normalized total power dissipation as a function of mounting base temperature**



**Fig 3. Single-pulse and repetitive avalanche rating; avalanche current as a function of avalanche time.**



## 5. Thermal characteristics

**Table 5. Thermal characteristics**

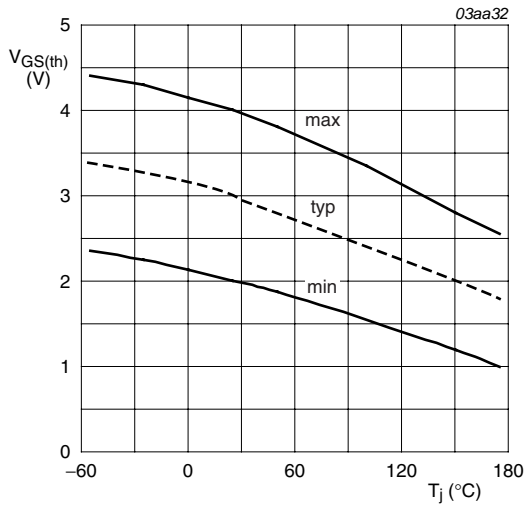
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base		-	-	0.45	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint	[1] -	50	-	K/W

[1] Mounted on a printed-circuit board; vertical in still air.

## 6. Characteristics

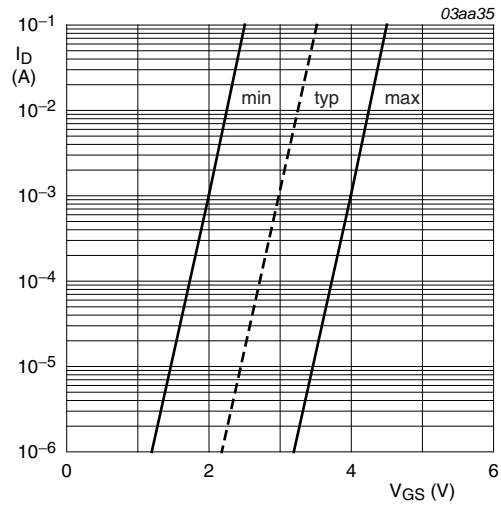
Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	70	-	-	V
		$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	75	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 5</a> ; see <a href="#">Figure 6</a>	2	3	4	V
$V_{GSth}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ\text{C};$ see <a href="#">Figure 5</a> ; see <a href="#">Figure 6</a>	1	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ see <a href="#">Figure 5</a> ; see <a href="#">Figure 6</a>	-	-	4.4	V
$I_{DSS}$	drain leakage current	$V_{DS} = 75 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.02	1	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ\text{C};$ see <a href="#">Figure 7</a> ; see <a href="#">Figure 8</a>	-	-	8.4	m $\Omega$
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 7</a> ; see <a href="#">Figure 8</a>	-	3.4	4	m $\Omega$
$I_{DSS}$	drain leakage current	$V_{DS} = 75 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ\text{C}$	-	-	500	$\mu\text{A}$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 60 \text{ V}; V_{GS} = 10 \text{ V};$ see <a href="#">Figure 9</a>	-	142	-	nC
$Q_{GS}$	gate-source charge		-	36	-	nC
$Q_{GD}$	gate-drain charge		-	67	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25 \text{ A}; V_{DS} = 60 \text{ V};$ see <a href="#">Figure 9</a>	-	5	-	V
$C_{iss}$	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 10</a>	-	8744	11659	pF
$C_{oss}$	output capacitance		-	923	1108	pF
$C_{rss}$	reverse transfer capacitance		-	579	793	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30 \text{ V}; R_L = 1.2 \text{ } \Omega; V_{GS} = 10 \text{ V};$ $R_{G(ext)} = 10 \text{ } \Omega$	-	65	-	ns
$t_r$	rise time		-	133	-	ns
$t_{d(off)}$	turn-off delay time		-	146	-	ns
$t_f$	fall time		-	119	-	ns
$L_D$	internal drain inductance	from upper edge of drain mounting base to centre of die	-	2.5	-	nH
$L_S$	internal source inductance	from source lead to source bonding pad	-	7.5	-	nH
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 11</a>	-	0.85	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 20 \text{ A}; dI_S/dt = -100 \text{ A}/\mu\text{s}; V_{GS} = 0 \text{ V};$ $V_{DS} = 25 \text{ V}$	-	83	-	ns
$Q_r$	recovered charge		-	155	-	nC



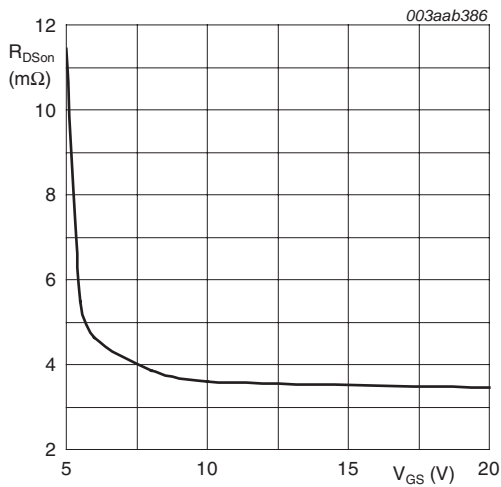
$$I_D = 1\text{mA}; V_{DS} = V_{GS}$$

**Fig 5. Gate-source threshold voltage as a function of junction temperature**



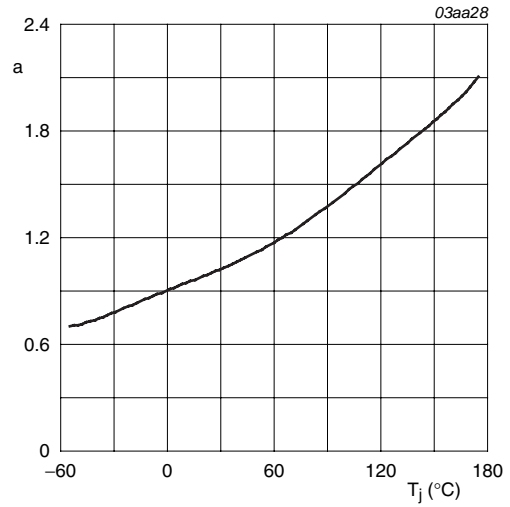
$$T_j = 25\text{ }^\circ\text{C}; V_{DS} = 5\text{V}$$

**Fig 6. Sub-threshold drain current as a function of gate-source voltage**



$$T_j = 25\text{ }^\circ\text{C}; I_D = 25\text{ A}$$

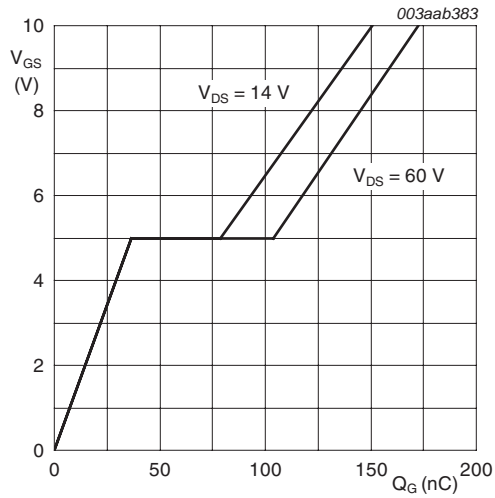
**Fig 7. Drain-source on-state resistance as a function of gate-source voltage; typical values**



$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

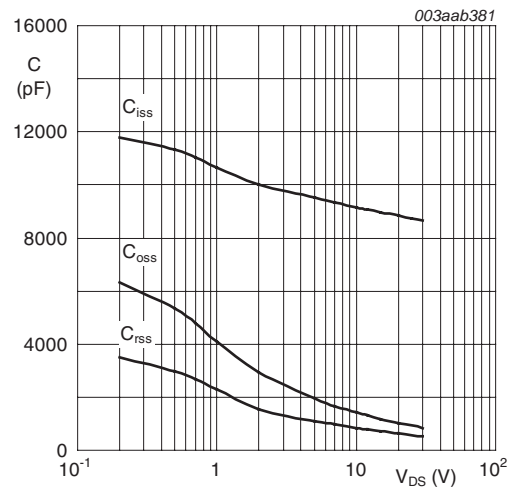
**Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature**





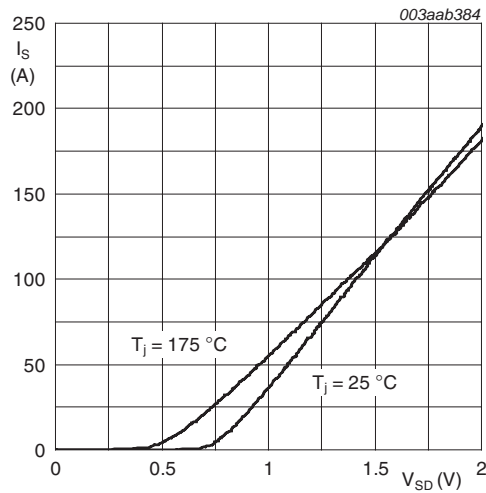
$T_j = 25\text{ }^\circ\text{C}; I_D = 25\text{A}$

**Fig 9. Gate-source voltage as a function of gate charge; typical values**



$V_{GS} = 0\text{V}; f = 1\text{MHz}$

**Fig 10. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



$V_{GS} = 0\text{V}$

**Fig 11. Source current as a function of source-drain diode; typical values**

**7. Package outline**

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

**SOT404**



**Fig 12. Package outline SOT404 (D2PAK)**

## 8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK764R0-75C v.2	20110426	Product data sheet	-	BUK764R0-75C_1
Modifications:	<ul style="list-style-type: none"><li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>• Legal texts have been adapted to the new company name where appropriate.</li></ul>			
BUK764R0-75C_1	20060817	Product specification	-	-

## 9. Legal information

### 9.1 Data sheet status

Document status <a href="#">[1]</a> <a href="#">[2]</a>	Product status <a href="#">[3]</a>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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