USB Audio 2.0 Reference Design, XS1-L2 Edition Hardware Manual

REV 1.6

If you intend to produce hardware designs based on the information provided in this document, you should always check the datasheet of the xCORE device. In the case where the reference design and datasheet conflict, the datasheet presides.

XMOS datasheets contain additional hardware design requirements and guidelines that are not covered in this document, which users of XMOS hardware reference designs must ensure are followed.

The presence of a third party device in an XMOS hardware reference design does not make any statement about its general availability. You must make your own arrangements to ensure that all components can be sourced in the required volumes.

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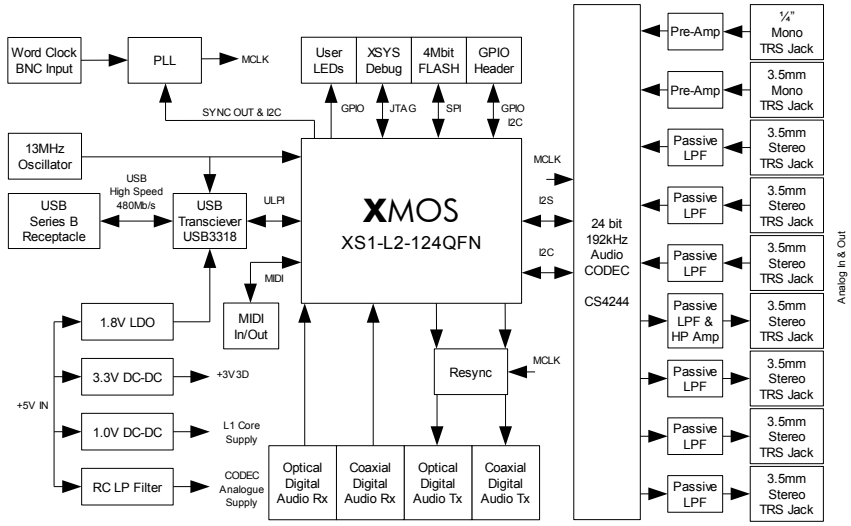
1 Introduction

The USB Audio 2.0 Reference Design, XS1-L2 Edition (hereafter "the board") is a hardware reference design for a multi-channel USB audio interface using the XMOS XS1-L2 dual-core event-driven processor. It contains a single XS1-L2 device enabling implementation of a complete USB 2.0 high-speed device compliant with release 2.0 of the USB Audio Class specification.

A block diagram of the design is shown below:



The XS1-L2 event-driven processor communicates with the USB host via a ULPI USB transceiver at the 480Mb/s high-speed rate. The XS1-L2 controls the streaming of audio data over the USB connection and direct I^2S interface to the audio CODEC, digital streams and MIDI communications. Multiple additional functions (e.g. Mixers/DSP etc.) can be implemented by modifications to the standard software.

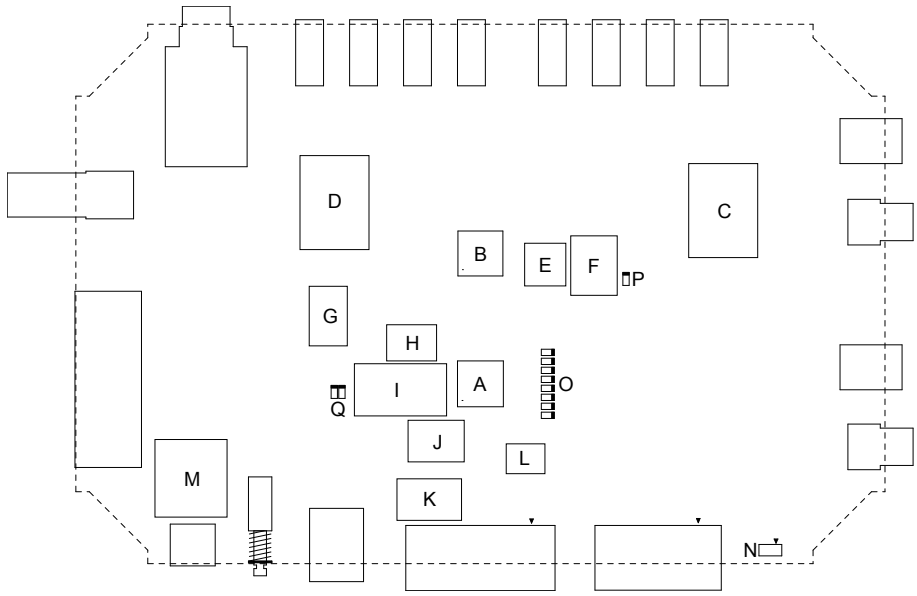
1.1 Feature Overview

Key features of the board are as follows:

- Support for standard sample rates - 32kHz, 44.1kHz, 48kHz, 88.2kHz, 96kHz, 176.4kHz, 192kHz
- Six channels of analogue line level input
- Eight channels of analogue line level output
- Optical and coaxial digital audio input (S/PDIF or ADAT)
- Optical and coaxial digital audio output (S/PDIF or ADAT)
- MIDI input and output
- Word (house) clock input to allow synchronization to an external clock
- Integrated instrument and microphone pre-amplifier
- Integrated headphone amplifier on analogue outputs 1/2
- Powered via USB bus or external 5V source
- XMOS XSYS debug header for easy programming/debug from the host using the XMOS XTAG2 debug adapter
- Eight LEDs for programmable use
- Expansion header with I^2C and twelve general purpose IOs for programmable use
- Multiple test-points to allow connection of custom ADC/DAC hardware etc

1.2 Board Components

The diagram below shows the layout of the main components of the board:

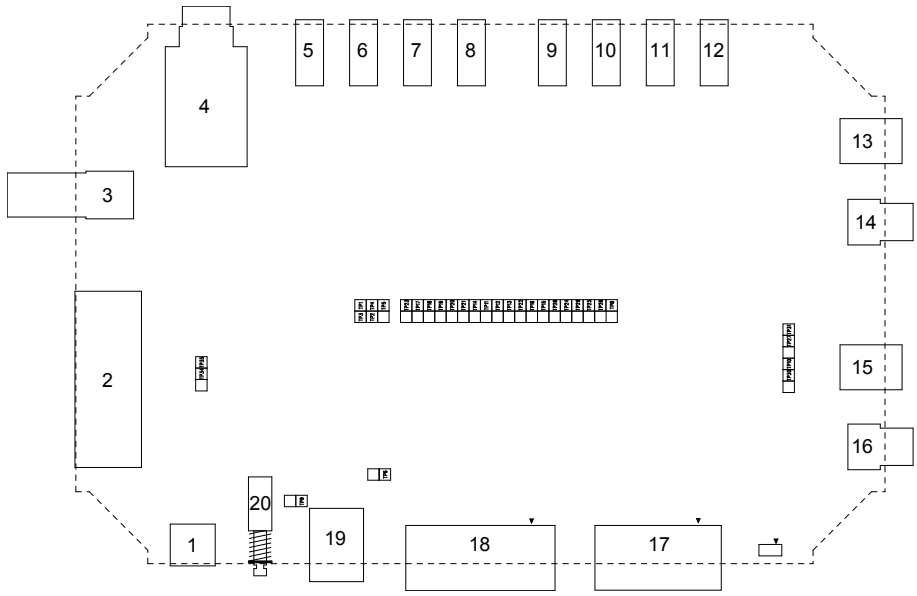


A	XS1-L2 Device	**J**	1V0 Core Supply
B	Audio CODEC	**K**	13MHz Oscillator
C	Headphone Pre-Amp	**L**	4Mb SPI FLASH
D	Instrument & Mic Pre-Amp	**M**	Power Supply Protection & Fuse
E	Audio CODEC Clock Buffers	**N**	Case LED Power Connector
F	PLL & Clock Distribution	**O**	8 x User Programmable LEDs
G	4V1 Analogue Supply	**P**	PLL Auxiliary Output LED
H	3V3 Digital Supply	**Q**	USB & Power On LEDs
I	USB Transceiver		

The rest of this document provides a detailed description of each of the main board components.

1.3 Connectors

The diagram below shows the layout of the connectors on the board:



1	5V DC Power In
2	MIDI Input & Output (Via Gameport)
3	75Ω BNC Word Clock Input
4	Instrument IN (Mono 1/4" Jack)
5	Microphone IN (Mono 3.5mm Jack)
6	Analogue 1/2 IN (Stereo 3.5mm Jack)
7	Analogue 3/4 IN (Stereo 3.5mm Jack)
8	Analogue 5/6 IN (Stereo 3.5mm Jack)
9	Analogue 1/2 OUT (Stereo 3.5mm Jack)
10	Analogue 3/4 OUT (Stereo 3.5mm Jack)
11	Analogue 5/6 OUT (Stereo 3.5mm Jack)
12	Analogue 7/8 OUT (Stereo 3.5mm Jack)
13	Optical Digital Output
14	Coaxial Digital Output
15	Optical Digital Input
16	Coaxial Digital Input
17	Expansion Header
18	XSYS Debug Interface
19	USB B Connector
20	Push Button Power Switch

2 XS1-L2 Device [A]

The board is based on a single XS1-L2 device in a 124 pin QFN package.

The XS1-L2 consists of a two XCore processors. Each XCore comprises an event-driven multi-threaded processor with tightly integrated general purpose I/O pins, 64 KBytes of on-chip RAM and 8 KBytes of OTP (One Time Programmable) memory.

XCore processors have time-aware ports that are directly connected to the I/O pins. Examples of how to write software that interfaces over these ports are provided in *Programming XC on XMOS Devices* available from `www.xmos.com`.

2.1 Clocking [K]

A discrete 13MHz pierce oscillator is used to feed the XS1-L2 reference clock input and also the USB3318 USB transceiver. The L2 has MODE1 and MODE0 pins wired to ground which sets the internal XS1-L2 PLL multiplication factor to 30.75. This results in a default core clock frequency of 399.75MHz and an I/O reference clock frequency of 99.9375MHz.

2.2 Reset

A supply voltage supervisor connected to the 1V0 core supply is used to provide a reset to the L2. This ensures the device is reset at power on and also provides predictable behaviour under brownout conditions. The device can also be reset over the XSYS debug interface.

2.3 Boot

The boot mode of the XS1-L2 is set by the MODE3 and MODE2 pins which are connected together on the board.

With MODE3 and MODE2 both high (default), the device will boot from the 4Mb SPI FLASH on the board. With MODE3 and MODE2 both low, the device will not boot from SPI FLASH, thus instead allowing boot via JTAG using the XSYS debug link.

To allow automatic boot mode selection based on debug hardware presence the MODE2 and MODE3 pins are connected to the TRST_N of the debug connector.

Without debug hardware connected to the XSYS interface, the board will boot from SPI FLASH. With the XTAG2 connected to the XSYS interface, the host can control the boot mode of the device by way of the TRST_N line. This functionality is provided purely for developer convenience. A typical production board might use a jumper or switch for manual boot mode selection if JTAG boot is required.

The MODE4 pin is held low on the board. This causes the second XCore to boot from a link connected to first XCore, rather than its own SPI FLASH.

3 USB Connector and Transceiver [19 & I]

The board uses a standard USB series B receptacle for USB connectivity.

The high-speed USB signals are connected to an SMSC® USB3318 USB transceiver which provides a ULPI connection to XCore 0 of the XS1-L2.

On power-up, a pulldown resistor holds the transceiver in reset until the XS1-L2 is ready to begin USB activity. The USB transceiver reset pin is connected to port X0P1M of the XS1-L2 in order that it can be controlled by software.

The transceiver uses the 13MHz clock provided by a discrete oscillator which doubles as the reference clock for the XS1-L2.

4 Audio CODEC [C]

The board is equiped with a 24 bit, 192kHz multi-channel audio CODEC (Cirrus Logic® CS42448).

The CODEC is configured via an I^2C serial configuration interface with slave address 0x48.

The CODEC can be configured to provide audio clocks (master mode) or with all clocks being inputs (slave mode).

The CODEC has seperate LRCLK and SCLK I/Os for ADC and DAC. These are both connected to a single I/O pin on the XCore. Clock buffers are provided for SCLK and LRCLK I/Os to remove any potential contention issues.

The control pin (CODEC_MODE) for the buffers is mapped to bit 1 of port X1P4A on the XS1-L2.

CODEC_MODE	Clock Mode
0	Clocks Connected
1	Clocks Disconnected

When using the codec in slave mode the clocks should be connected together.

The CODEC has three internal modes depending on the sampling rate used. These change the oversampling ratio used internally in the CODEC. The three modes are shown below:

CODEC mode	CODEC sample rate range
Single speed	4-50kHz
Double speed	50-100kHz
Quad speed	100-200kHz

The reset input to the CODEC is mapped to bit 3 of port X1P4A on the XS1-L2.

The interrupt output from the CODEC is mapped to bit 3 of port X1P4B on the XS1-L2.

4.1 Analogue Audio I/O [4 - 12]

3.5mm Tip Ring Sleeve (TRS) audio jacks are provided for stereo audio inputs and outputs. The layout of the audio jacks is shown in the connector diagram of the board.

A simple passive AC-coupling and low pass filter circuit is used on input and output. The circuit is configured such that the audio output will produce approximately 0.94V_{RMS} (-0.54dBV) for a digital full scale signal. Due to the output coupling capacitors, the output impedance falls with frequency and is approximately 1kΩ @ 35Hz falling to 576Ω @ 1kHz.

The input circuit contains an attenuator such that a 1.62V_{RMS} (+4.2dBV) signal will produce a full scale digital output. The input impedance is approximately 9kΩ.

The CODEC microphone and instrument inputs are AC-coupled to low noise op-amp pre-amplifiers before being AC-coupled onto the CODEC inputs. These are set with gains of -1 and -10 for the instrument and microphone inputs respectively.

A 3.5mm Tip Ring Sleeve (TRS) audio jack is provided for the stereo headphone out, which is powered by a 75mW TI TPA152 stereo headphone amplifier. This is the a capable of driving a minimum load of 32Ω. It is configured with a gain of -1.

5 Digital Audio Output [13 & 14]

Optical and coaxial digital audio transmitters are used to provide digital audio output in formats such as IEC60958 consumer mode (S/PDIF) and ADAT. The signals are generated from two 1-bit ports on the XS1-L2 as defined in the port map.

The data streams from the XS1-L2 are re-clocked using the external master clock to synchronise the data into the audio clock domain. This is achieved using simple external D-type flip-flops.

The optical output uses a TOSLINK optical connector with an integrated LED and differential driving circuit. The coaxial output uses an RCA connector and is isolated via a transformer.

6 Digital Audio Input [15 & 16]

Digital audio input is provided to allow formats such as IEC60958 consumer mode (S/PDIF) or ADAT to be connected to the device via either optical or coaxial mediums.

The optical input uses a TOSLINK optical connector with an integrated photodiode and receiver circuit. The coaxial input uses an RCA connector and is AC-coupled into a 75Ω terminator.

This gives a signal level of 0.5V_{p-p}, which is fed into a differential line receiver.

The input signals are fed into two 1-bit ports on the processor as defined in the port map.

7 MIDI I/O [2]

Musical Instrument Digital Interface input and output is provided on the board via a standard Gameport connector. The signals are buffered using 5V line drivers and are then connected to 1-bit ports on the XS1-L2, via a 5V to 3.3V buffer.

10KΩ pull ups are placed on the MIDI IN signal from the connector and on the MIDI OUT signal from the XCore. These stop glitches on startup and when no MIDI devices are connected to the board.

The MIDI input and output signals are connected to the XS1-L2 as follows:

Port	Signal
X1P1P	MIDI_IN
X1P1O	MIDI_OUT

Standard MIDI devices (using DIN 5/180° connectors) are attached using a Gameport to dual DIN MIDI cable. This is not included in the kit, but are easily purchased from other suppliers.

8 Audio Clocking [3 & K]

In order to accommodate a multitude of clocking options, the low-jitter master clock (e.g. 256 x fs), is generated locally using a fractional-N frequency multiplier PLL chip.

The source for the PLL is either the SYNC_OUT signal from the XS1-L2 or the word clock input as controlled by the SYNC_SEL signal.

The SYNC_SEL signal is mapped to bit 0 of port X1P4A on the XS1-L2 as shown in the port map.

The behaviour of this select signal is as follows:

SYNC_SEL	PLL clock source
0	XS1-L2 SYNC_OUT
1	Word Clock Input

The Cirrus Logic CS2300-CP PLL chip generates a low-jitter output of between 6-75MHz from any 50Hz-30MHz input clock.

A variety of clock sources can be used, including:

- Local crystal oscillator, via XCore clock block (which divides 13MHz down to the SYNC_OUT signal).
- S/PDIF software recovered clock (which then drives the SYNC_OUT signal).
- Word clock input.

The SYNC_OUT signal is connected to both cores of the XS1-L2, but a DNF resistor (R102) normally only allows XCore 1 to output the signal. Fit a 0R 0603 resistor to enable XCore 0 to output the signal.

The audio master clock is connected to both cores of the XS1-L2 on ports X0P1L and X1P1L, to allow the audio output streams on that XCore to be synchronized.

The CS2300-CP is configured over the I^2C bus (shared with the CODEC) at slave address 0x47.

The CS2300-CP auxiliary output drives an LED to indicate the state of the signal. For example, this could show if the PLL is locked or not.

A 75Ω terminated BNC input is provided for an external word clock ("house clock") input. The input accepts a 0-5V ($5V_{p-p}$, 2.5V offset) signal, which is low-pass filtered to remove high frequency components, and schmitt triggered to remove problems with noise and non-monotonic edges.

This signal is also fed to a 1-bit port on the XS1-L2. This allows the application code to detect if a word clock input signal is present.

9 SPI Flash Memory [L]

A 4Mbit FLASH memory device is provided, connected via a standard Serial Peripheral Interface (SPI).

The FLASH is connected to four 1-bit ports as shown in the table below. These are the standard ports the processor will try to boot from in SPI boot mode.

Port	SPI Signal
X0P1A	MISO
X0P1B	SS
X0P1C	CLK
X0P1D	MOSI

The XMOS development tools include the XFLASH utility for programming compiled programs into the flash memory via the XS1-L2. Software may also access the FLASH memory at run-time by interfacing with the above ports.

10 XSYS Interface [18]

A standard XMOS XSYS interface is provided to allow host debug of the board via JTAG.

An XTAG2 USB debug adapter can be plugged into this port to allow running/debugging code, programming the FLASH memory via the XS1-L2 and selection of boot mode. It is not recommended to use an original (FTDI based) XTAG with the L2 device, as this is not as fast as the XTAG2 and can have signal drive strength issues.

A 20-way IDC header is used as the physical connector and the pinout of this is shown below:

Signal	Pin	Description
TRST_N	3	JTAG Test Reset. Active low
TMS	7	JTAG Test Mode Select
TCK	9	JTAG Test Clock
TD1	5	JTAG Test Data. From debug adapter to XS1-L2
TD2	13	JTAG Test Data. From XS1-L2 to debug adapter
SRST_N	15	System Reset. Active low. Resets XS1-L2 device
DEBUG	11	XS1-L2 DEBUG Interrupt line
XMOS-LINK	6, 10, 14, 18	This is a 2-wire XMOS-Link for advanced debug
GND	4, 8, 12, 16, 20	Ground
NC	1, 2, 17, 19	These pins are not connected

As discussed in the Boot section the XS1-L2 MODE2 and MODE3 pins are connected to the TRST_N signal.

11 User LEDs [I]

The board provides eight user LEDs that can be driven by software. These are marked on the board as LED 0 though to LED 7. The LEDs are connected to port X1P8B, the bit mapping is shown in the table below:

Port	LED
X1P8B0	LED 0
X1P8B1	LED 1
X1P8B2	LED 2
X1P8B3	LED 3
X1P8B4	LED 4
X1P8B5	LED 5
X1P8B6	LED 6
X1P8B7	LED 7

The LED connections are also shown in the port map. Setting the relevant bit high will turn the LED on.

12 Expansion Header [17]

The board provides a general purpose input/output expansion header to allow interfacing to custom boards. For example, this could be an I^2C display, eight LEDs and four buttons to make a user interface.

The header contains the following:

- +3V3 power pin.
- Ground pin.
- I^2C bus (as used to configure the PLL and CODEC).
- One 4-bit GPIO port (X1P4F).
- One 8-bit GPIO port, which is also shared with the LED outputs (X1P8B).

A 16-way IDC header is used as the physical connector and the pinout of this is shown below:

Pin	Port	Signal
1	NA	+3V3
2	X1P8B7	LED_7
3	NA	GND
4	X1P8B6	LED_6
5	X1P1C0	I2C_SDA
6	X1P8B5	LED_5
7	X1P1D0	I2C_SCL
8	X1P8B4	LED_4
9	X1P4F0	GPIO_0
10	X1P8B3	LED_3
11	X1P4F1	GPIO_1
12	X1P8B2	LED_2
13	X1P4F2	GPIO_2
14	X1P8B1	LED_1
15	X1P4F3	GPIO_3
16	X1P8B0	LED_0

Each IO pin can source or sink a maximum of 4mA.

13 Power [1, G, H, J, M & Q]

The board is powered from the onboard +5V DC power connector or from the USB bus. Note that the board has not been designed as a bus-powered device due to pre-enumeration current limits.

The two different power supplies are "ORd" together using Schottky diodes with a maximum voltage drop of 0.34V. A 750mA resettable polyfuse and reverse polarity protection, via a bidirectional zener diode, is provided. Ferrite beads are used on the +5V VBus and +5V DC power input to prevent switching noise propagating down the USB and power cables.

A latching push-button power switch is fitted to the board that activates a p-channel MOSFET (which has an Rds(on) of approximately 80mΩ). A soft start circuit is included to limit the inrush current.

When powered from the USB bus all the power used by the board is derived from the nominally +5V VBus supply from the USB connector. The board will use approximately 300mA when fully configured and operating.

The required core and IO voltages for the XS1-L2 are derived from 5V as follows:

- A low cost 1.5A buck switching regulator is used to generate the 1.0V core supply for the XS1-L2.
- A low cost 600mA buck switching regulator is used to generate the global 3.3V supply.

Switching regulators are used on these power supplies due to their high efficiency.

The power supplies are sequenced using a 3.0V voltage supervisor on the 3.3V supply output, to drive the enable input on the 1.0V supply. This makes sure that the 3.3V supply is up and stable, before the 1.0V supply comes up and also provides predictable behaviour under brownout conditions, by causing a reset if the supplies droop significantly.

A simple low drop out (LDO) linear regulator is used to generate the 1.8V supply required by the USB3318 USB transceiver.

A low noise LDO regulator is used to generate the analogue supply for the Audio CODEC. The CODEC offers higher audio performance at higher supply voltages so the voltage for this supply is set at 4.1V. This allows some headroom between the 4.5V minimum VBus voltage and the approx 350mV dropout of the LDO + RC pre-filter.

When the board is correctly connected to a USB source the USB VBUS Power LED is illuminated.

When the board is powered on the Power LED is illuminated.

14 Printed Circuit Board

The PCB is a 1.6mm four layer design in a XMOS XS1-G Development Kit form factor with dimensions of 180 x 120mm. It is made from FR4 (εr = 4.5) material and finished in immersion gold. The mounting holes are 3.2mm in diameter.

Signal stack up is as follows:

- Top signal
- Ground plane
- Power plane
- Bottom signal

15 Test Points

15.1 Test Points by ID

Test Point	Port	Signal
TP1	NA	+5V
TP2	NA	+4V1A
TP3	NA	+3V3
TP4	NA	+1V8
TP5	NA	+1V0
TP6	NA	OSC_13M
TP8	NA	PLL_WCLK
TP9	NA	VBUS
TP10	X0P1J0	OPTICAL_RX
TP11	X1P1N0	DAC_SD4
TP12	X1P1H0	DAC_SD3
TP13	X1P1F0	DAC_SD2
TP14	X1P1M0	DAC_SD1
TP15	X1P1I0	CODEC_SCLK
TP16	X1P1E0	CODEC_LRCK
TP17	X1P1D0	I2C_SCL
TP18	X1P1C0	I2C_SDA
TP19	X1P4A3	CODEC_RSTN
TP20	X1P1B0	ADC_SD3
TP21	X1P1A0	ADC_SD2
TP22	X1P1G0	ADC_SD1
TP23	X1P4B3	CODEC_INT
TP24	X0P1L0 & X1P1L0	XCORE_MCLK
TP25	X0P1C0 & X1P4E0	SYNC_OUT
TP26	X1P4A0	SYNC_SEL
TP27	X1P1K0	COAXIAL_TX
TP28	X1P4A1	CODEC_MODE
TP29	X1P4B1	PLL_LOCK
TP30	X0P1K0	COAXIAL_RX
TP31	X1P1J0	OPTICAL_TX
TP34	X1P1O0	MIDI_OUT
TP35	X1P1P0	MIDI_IN

15.2 Test Points by Signal

15.2.1 Power

Signal	Port	Test Point
+1V0	NA	TP5
+1V8	NA	TP4
+3V3	NA	TP3
+4V1A	NA	TP2
+5V	NA	TP1
VBUS	NA	TP9

15.2.2 XS1-L2 System

Signal	Port	Test Point
OSC_13M	NA	TP6
PLL_LOCK	X1P4B1	TP29

15.2.3 Audio Clocking

Signal	Port	Test Point
SYNC_SEL	X1P4A0	TP26
PLL_WCLK	NA	TP8
SYNC_OUT	X0P1C0 * & X1P4E0	TP25
XCORE_MCLK	X0P1L0 & X1P1L0	TP24

* Enabled via DNF resistor R102.

15.2.4 Codec Audio

Signal	Port	Test Point
ADC_SD1	X1P1G0	TP22
ADC_SD2	X1P1A0	TP21
ADC_SD3	X1P1B0	TP20
DAC_SD1	X1P1M0	TP14
DAC_SD2	X1P1F0	TP13
DAC_SD3	X1P1H0	TP12
DAC_SD4	X1P1N0	TP11
CODEC_LRCLK	X1P1E0	TP16
CODEC_SCLK	X1P1I0	TP15

15.2.5 Codec Config/Status

Signal	Port	Test Point
CODEC_INT	X1P4B3	TP23
CODEC_MODE	X1P4A1	TP28
CODEC_RST	X1P4A3	TP19
I2C_SCL	X1P1D0	TP17
I2C_SDA	X1P1C0	TP18

15.2.6 Digital Audio

Signal	Port	Test Point
OPTICAL_RX	X0P1J0	TP10
OPTICAL_TX	X1P1J0	TP31
COAXIAL_RX	X0P1K0	TP30
COAXIAL_TX	X1P1K0	TP27

15.2.7 MIDI

Signal	Port	Test Point
MIDI_OUT	X1P1O0	TP34
MIDI_IN	X1P1P0	TP35

Unmarked test points are connected to ground.

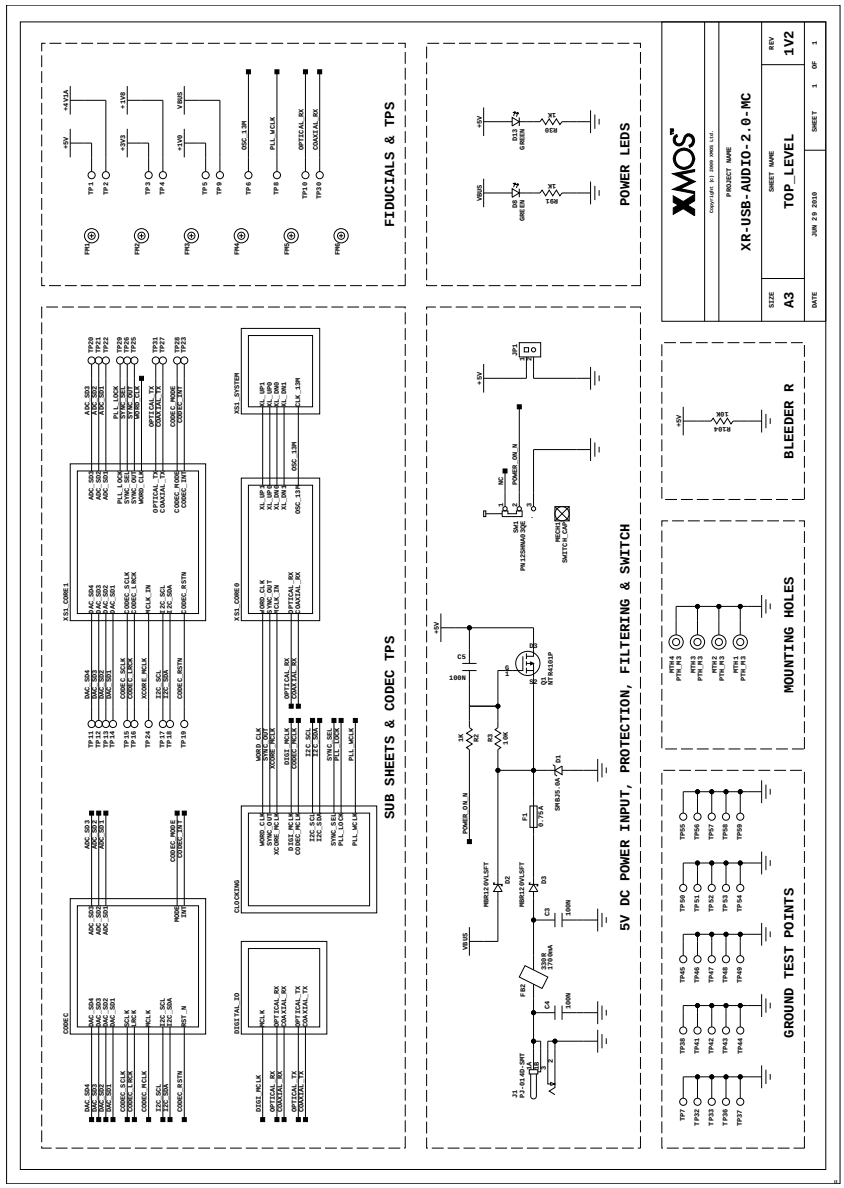
16 Port Map

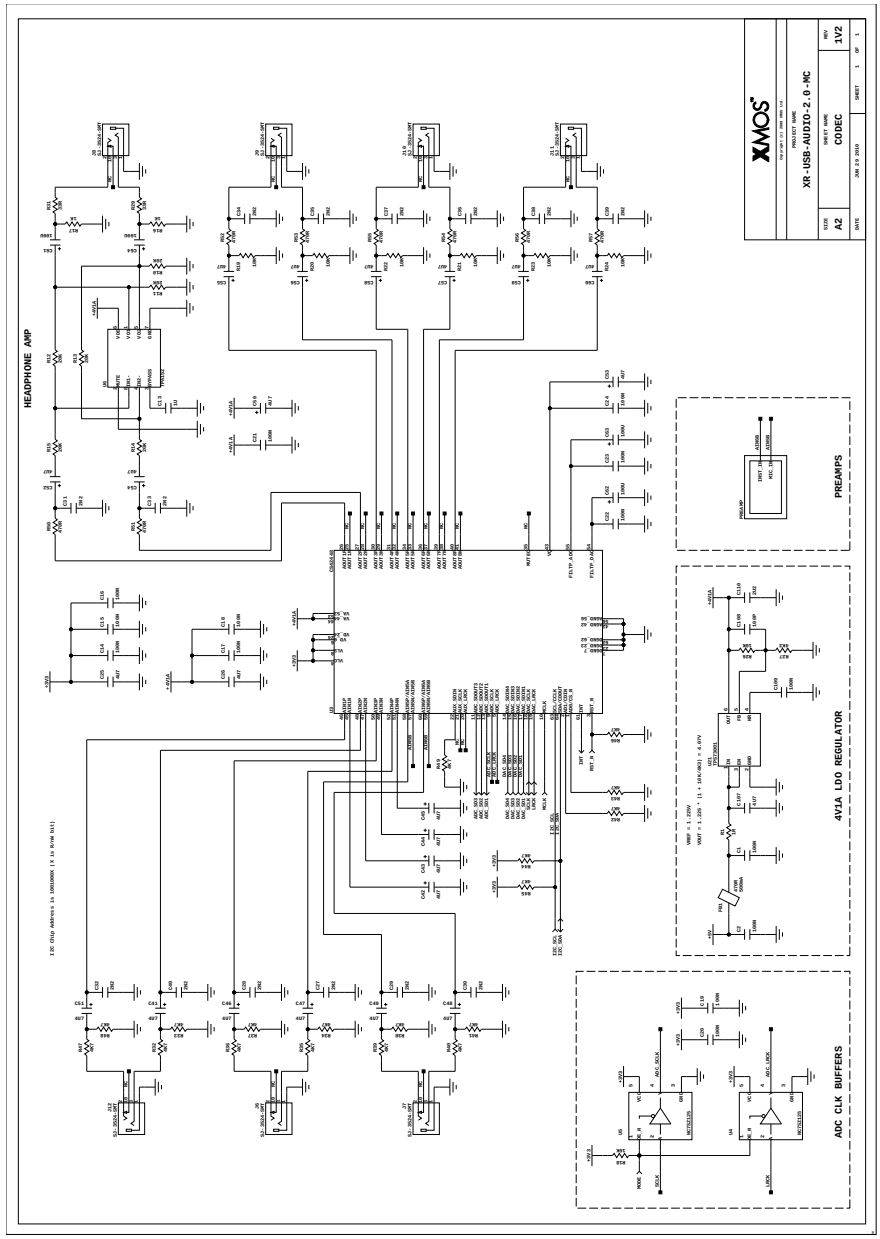
The table below provides a full description of the port to signal mappings used on the board.

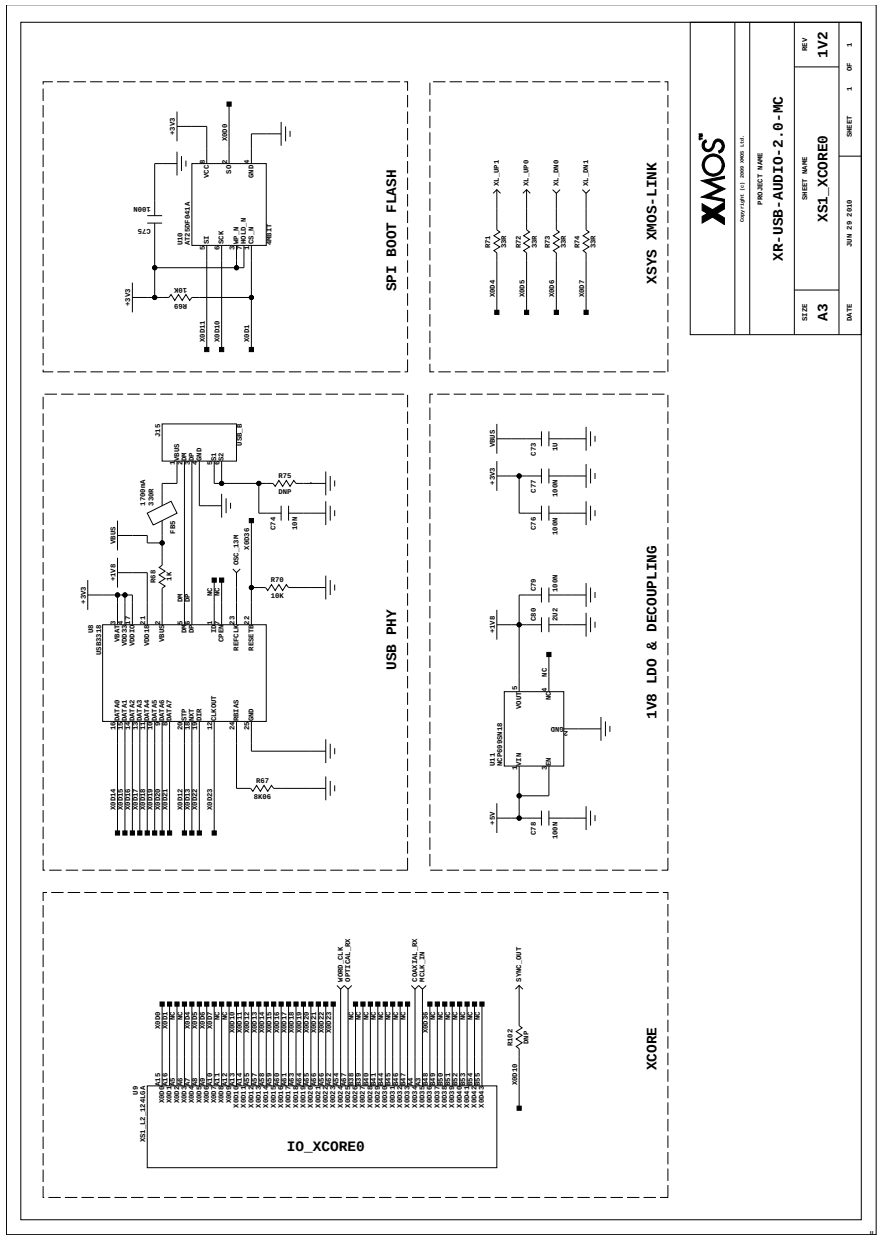
Pin	Port				XCore	
	1b	4b	8b	16b	0	1
XD0	P1A0				SPI_MISO	ADC_SD2
XD1	P1B0				SPI_SS	ADC_SD3
XD2		P4A0	P8A0	P16A0	NA	SYNC_SEL
XD3		P4A1	P8A1	P16A1		CODEC_MODE
XD4		P4B0	P8A2	P16A2	XSYS Link	NA
XD5		P4B1	P8A3	P16A3		PLL_LOCK
XD6		P4B2	P8A4	P16A4		WORD_CLK
XD7		P4B3	P8A5	P16A5		CODEC_INT
XD8		P4A2	P8A6	P16A6	NA	NA
XD9		P4A3	P8A7	P16A7		CODEC_RST_N
XD10	P1C0				SPI_CLK / SYNC_OUT *	I2C_SDA
XD11	P1D0				SPI_MOSI	I2C_SCL
XD12	P1E0				ULPI_STP	CODEC_LRCK
XD13	P1F0				ULPI_NXT	DAC_SD2
XD14		P4C0	P8B0	P16A8	ULPI_DATA[0:7]	LEDS[0:7]
XD15		P4C1	P8B1	P16A9		
XD16		P4D0	P8B2	P16A10		
XD17		P4D1	P8B3	P16A11		
XD18		P4D2	P8B4	P16A12		
XD19		P4D3	P8B5	P16A13		
XD20		P4C2	P8B6	P16A14		
XD21		P4C3	P8B7	P16A15		
XD22	P1G0				ULPI_DIR	ADC_SD1
XD23	P1H0				ULPI_CLK	DAC_SD3
XD24	P1I0				WORD_CLK	CODEC_SCLK
XD25	P1J0				OPTICAL_RX	OPTICAL_TX
XD26		P4E0	P8C0	P16B0	NA	SYNC_OUT
XD27		P4E1	P8C1	P16B1		NA
XD28		P4F0	P8C2	P16B2		GPIO[0:3]
XD29		P4F1	P8C3	P16B3		
XD30		P4F2	P8C4	P16B4		
XD31		P4F3	P8C5	P16B5		
XD32		P4E2	P8C6	P16B6		NA
XD33		P4E3	P8C7	P16B7		
XD34	P1K0				COAXIAL_RX	COAXIAL_TX
XD35	P1L0				MCLK_IN	MCLK_IN
XD36	P1M0		P8D0	P16B8	ULPI_RST	DAC_SD1
XD37	P1N0		P8D1	P16B9	NA	DAC_SD4
XD38	P1O0		P8D2	P16B10		MIDI_OUT
XD39	P1P0		P8D3	P16B11		MIDI_IN
XD40			P8D4	P16B12		NA
XD41			P8D5	P16B13		
XD42			P8D6	P16B14		
XD43			P8D7	P16B15		

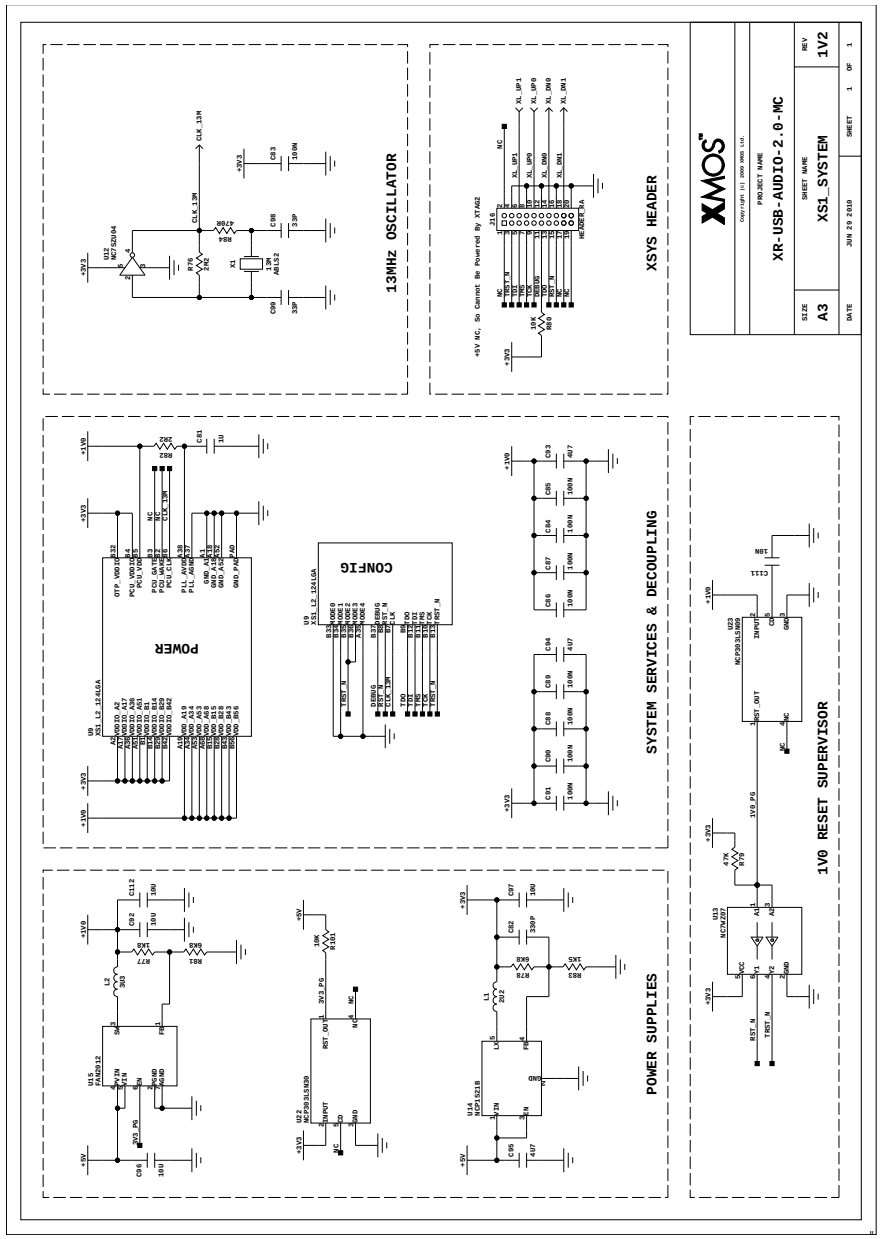
* Enabled via DNF resistor R102.

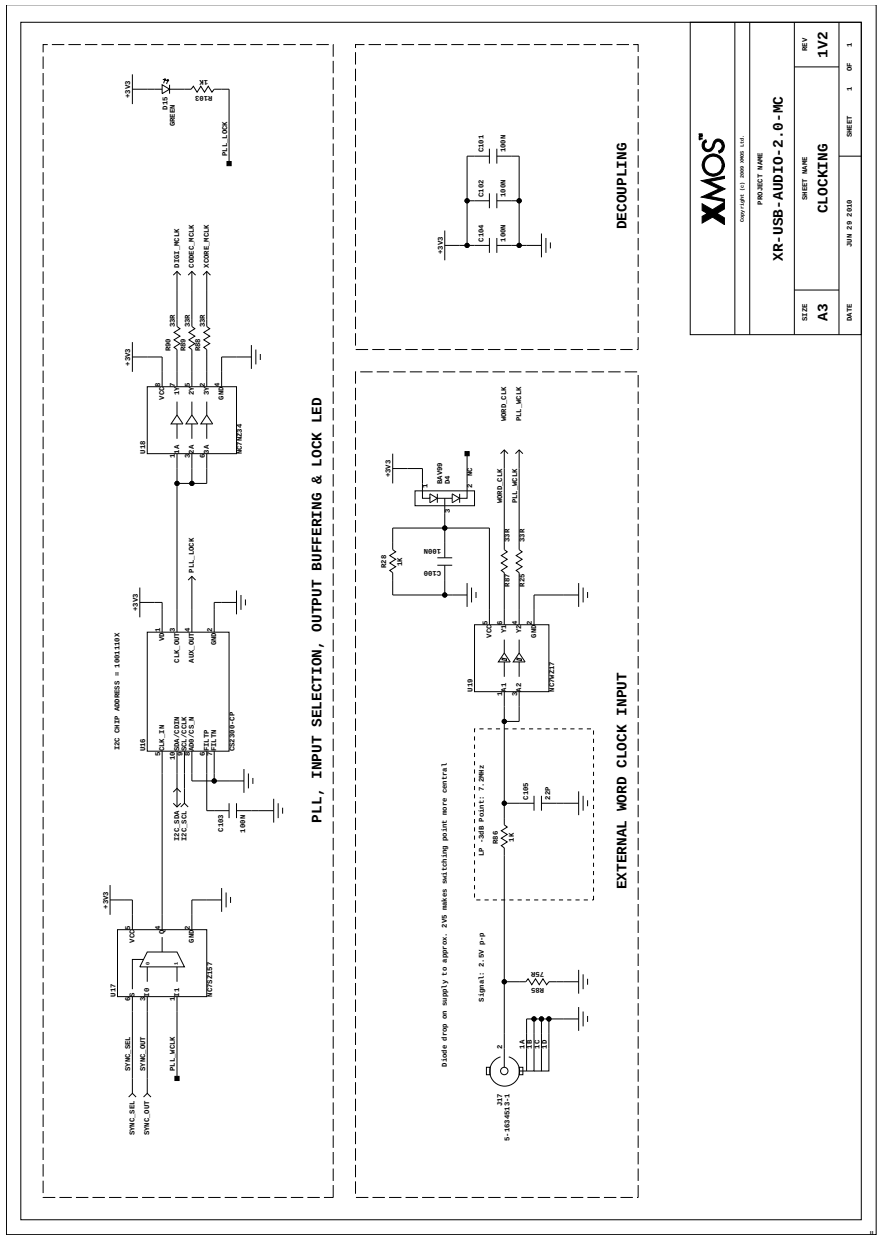
17 Schematics

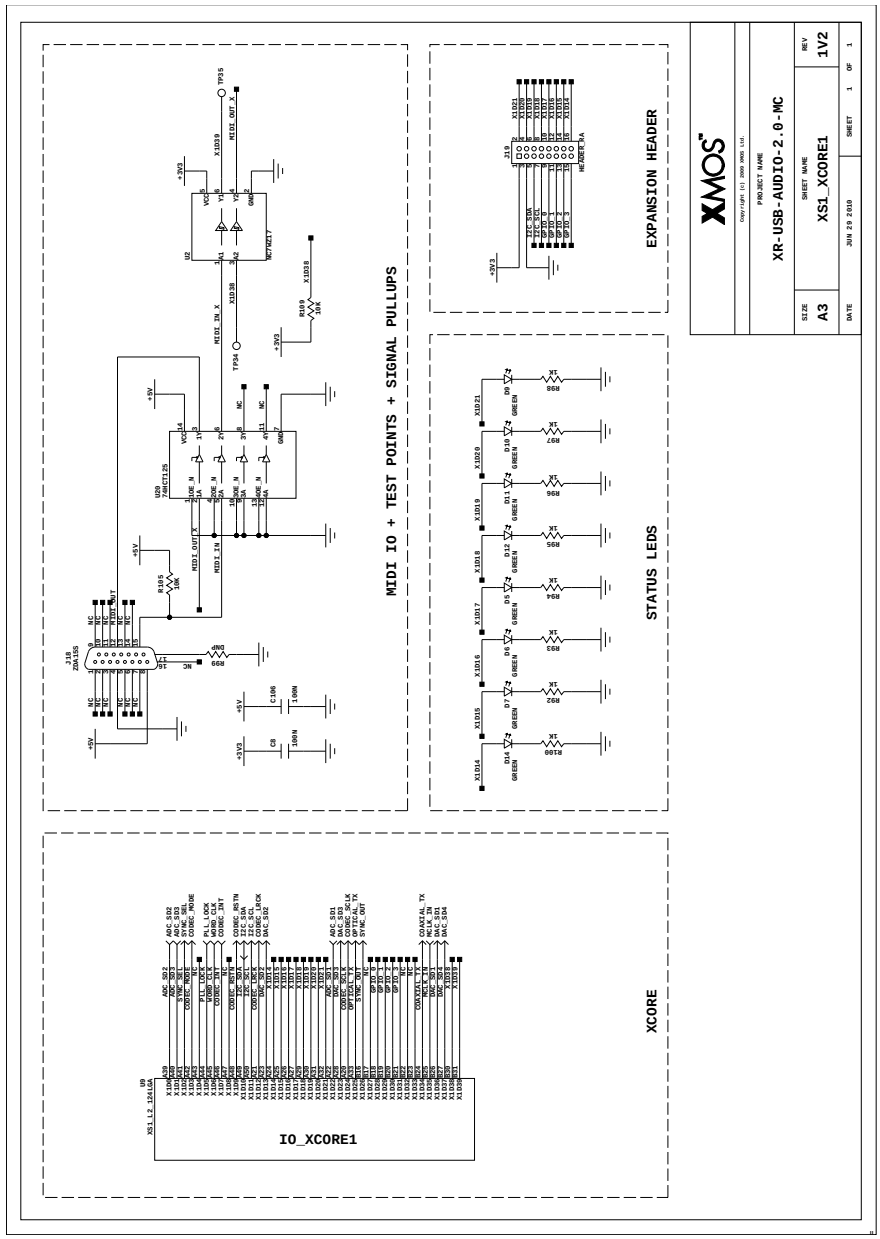


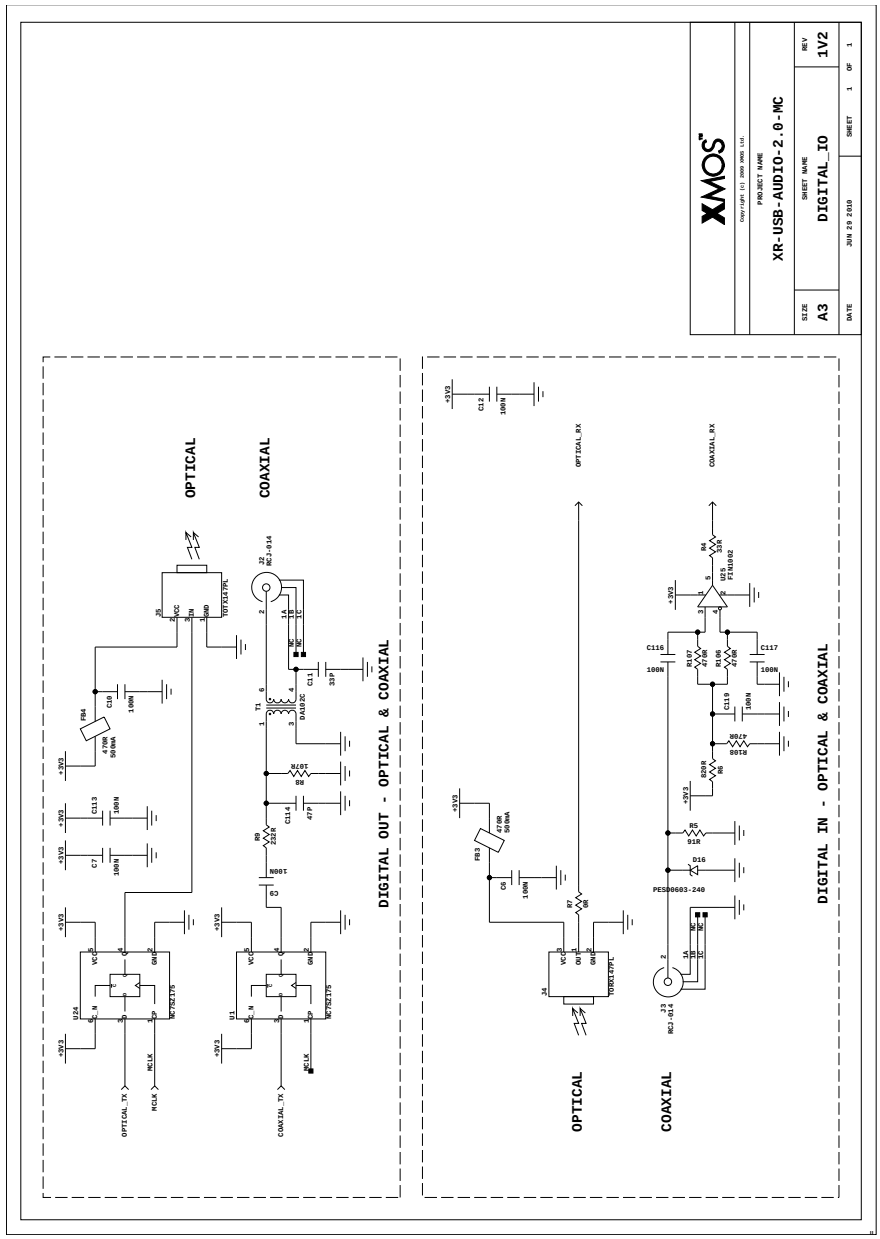

XMOS
XR-USB-AUDIO-2.0-MC
CODEC
A2
JAN 23 2013
1V2
HEADPHONE AMP
PREAMPS
4V1A LDO REGULATOR
ADC CLK BUFFERS

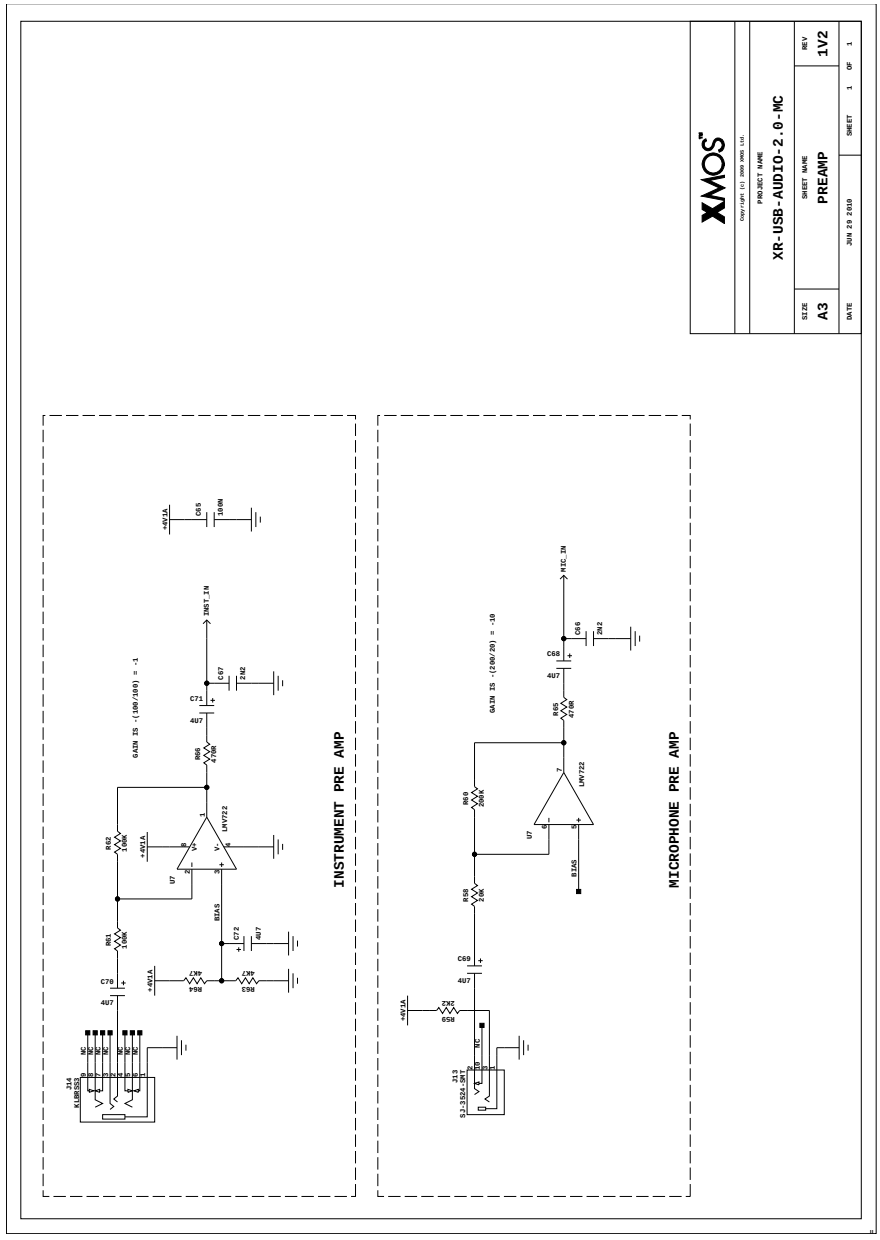

SPI BOOT FLASH
XSYS XMOS-LINK
USB PHY
1V8 LDO & DECOUPLING
XCORE
IO_XCORE0
XMOS
XR-USB-AUDIO-2.0-MC
XS1_XCORE0
1V2
A3
JUN 29 2010


13MHz OSCILLATOR
XSYS HEADER
SYSTEM SERVICES & DECOUPLING
POWER SUPPLIES
1V0 RESET SUPERVISOR
POWER
CONFIG
XMOS
XR-USB-AUDIO-2.0-MC
XS1_SYSTEM
1V2
A3
JAN 29 2010


PLL, INPUT SELECTION, OUTPUT BUFFERING & LOCK LED
DECOUPLING
EXTERNAL WORD CLOCK INPUT
XMOS
XR-USB-AUDIO-2.0-MC
CLOCKING
A3
1V2
JUN 29 2010


XCORE
IO_XCORE1
MIDI IO + TEST POINTS + SIGNAL PULLUPS
STATUS LEDS
EXPANSION HEADER
XMOS
XR-USB-AUDIO-2.0-MC
XS1_XCORE1
1V2
A3
JUN 29 2010


XMOS
XR-USB-AUDIO-2.0-MC
DIGITAL_IO
1V2
A3
DIGITAL OUT - OPTICAL & COAXIAL
DIGITAL IN - OPTICAL & COAXIAL
OPTICAL
COAXIAL
OPTICAL_TX
COAXIAL_TX
OPTICAL_RX
COAXIAL_RX
MCLK


XMOS
XR-USB-AUDIO-2.0-MC
PREAMP
1V2
A3
INSTRUMENT PRE AMP
MICROPHONE PRE AMP
INST_IN
MIC_IN
LMV722
BIAS
GAIN IS -(100/100) = -1
GAIN IS -(200/20) = -10

18 Board Revision Changes

This sections lists the changes between revisions of the PCB.

18.1 Changes From 1V0 To 1V1

- Swapped R62 and R66 silkscreen labels to correct error.
- Removed GPIO test points and added GPIO connector
- Split digital I/O to use seperate ports, rather than outputs being identical and the input being selected by a switch.
- Added testpoints for new digital I/O signals.
- Added PLL AUX LED.
- Added power sequencing to power supplies.
- Moved R75, C75 and 13M oscillator to add power sequencing.
- Changed layout of 1V0 SMPS.
- Changed L2 footprint to improve solderability.
- General tidy up and minor track changes.

18.2 Changes From 1V1 To 1V2

- Added buffer for MIDI I/O to correct 5V going into XS1-L2 I/Os.
- Added pull ups on MIDI signals to stop startup glitches.
- Added 47pf cap to slow coax output and tidied up digital out layout.
- Redesigned coaxial input for better performance and reduced cost.
- Moved the optical input track away from the 1V0 SMPS inductor.
- Moved bulk 1V0 decoupler (C93) across to far corner of L2.
- Changed most 0402 decouplers to 0603.
- Changed layout of the 13M oscillator.
- Added 5 more ground test points (next to CLK, VBUS, MIDI, DIGITAL IN and DIGITAL OUT).
- Added silkscreen labels to all test points, apart from the codec signals in the middle of the board.
- Added silkscreen labels for 5V DC, POWER SW, USB, XSYS and GPIO.
- Moved around R19, R52 and C34 to make it in line with other analogue outputs.
- Tidied up teardrops and changed them to curved shape.

19 Related Documents

The following documents provide more information on designing with XMOS technology:

- *Programming XC on XMOS Devices*: Explains how to program XMOS event-driven processor devices using the XC language.
- *XCore XS1 Architecture Tutorial*: Provides an overview of the XS1 instruction set architecture.
- *XS1 XSystem-L*: Provides an introduction on how to boot the XS1-L devices.
- *XMOS Tools User Guide*: Explains how to use the XMOS Tools to program XMOS event-driven processor devices.

For the most up-to-date information including schematics and product datasheets, is please visit:

- `http://www.xmos.com/usbaudio2/`

20 Release History

Date	Version	Description
28/01/10	1.0	Initial version
05/02/10	1.1	Revisions following interval review
24/02/10	1.2	Revisions for power supply sequencing
02/03/10	1.3	Revisions for board release 1V1
27/04/10	1.4	Revisions for R102
28/05/10	1.5	Revisions for MIDI, PLL & XTAG2
29/06/10	1.6	Revisions for board release 1V2

XMOS

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