# 42V, 2.5A Synchronous Step-Down Regulator with No-Loss Input PowerPath

## FEATURES

- **Seamless, Automatic Transition Between Two Input Power Sources**
- **Wide Input Voltage Range: 2.4V to 42V**
- **Wide Output Voltage Range: 0.818V to $V_{IN}$**
- **Up to 2.5A Continuous Output Current**
- **Pin-Selectable Priority and Ideal Diode-OR Modes**
- **Burst Mode® Operation, $I_Q$ = 2µA**
- 95% Efficiency at 1A, $V_{IN}$ = 12V, $V_{OUT}$ = 5V
- 1µA Current in Shutdown
- Programmable Input UVLO Thresholds
- Input Valid, Priority Channel and PGOOD Indicators
- 200kHz to 2.2MHz Fixed Frequency PWM
- Synchronizable to an External Clock
- Current Mode Control with 60ns Minimum On-Time
- Minimal External Components
- Thermally Enhanced 28-Lead 4mm × 5mm QFN and 28-Lead TSSOP Packages

## APPLICATIONS

- Portable Industrial/Communications Test Equipment
- Battery and Supercapacitor Backup Power
- Automotive Power with Battery Backup
- Uninterruptible Power Supplies

## DESCRIPTION

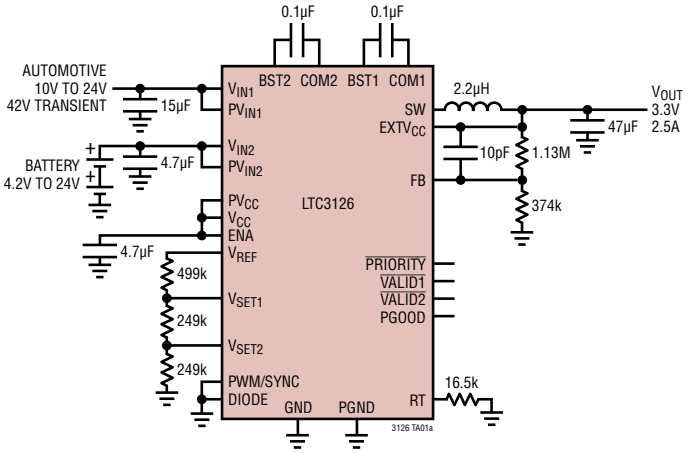
The LTC®3126 is a high efficiency synchronous buck converter with an internal no-loss PowerPath™ supporting seamless operation from two separate input power sources. Pin-selectable ideal diode-OR and priority input modes with user programmable undervoltage lockout thresholds provide full control over the transition between the input power sources. The fast, automatic switchover provided by the internal PowerPath eliminates the need for hold-up capacitors and minimizes disturbances on the output rail. An active input channel indicator and independent input and output power good signals provide complete feedback of the power system status.

A wide 2.4V to 42V input voltage range, 2.5A output current capability and 2µA Burst Mode operation quiescent current facilitate use of the LTC3126 with a wide variety of power sources including supercapacitors, automotive batteries, unregulated wall adapters and single to multicell stacks of most battery chemistries. Additional features include 1µA current in shutdown, internal soft-start and thermal protection. The LTC3126 is available in thermally enhanced 28-lead 4mm × 5mm QFN and 28-lead TSSOP packages.

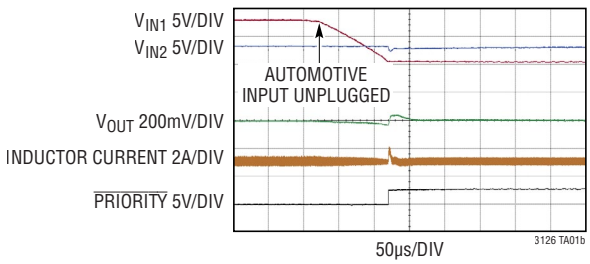


## TYPICAL APPLICATION

**2MHz, 3.3V/2.5A Supply from Automotive and Battery Inputs**



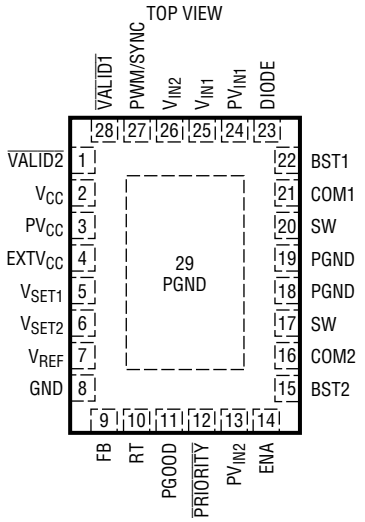

**Switchover to Battery Power, 2.5A Load**



## ABSOLUTE MAXIMUM RATINGS (Note 1)

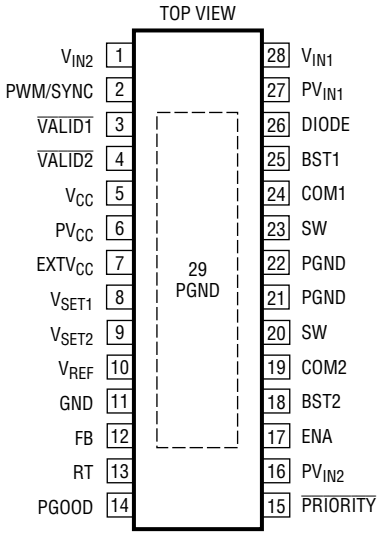
$PV_{IN1}$, $PV_{IN2}$, $V_{IN1}$, $V_{IN2}$ ..... 42V
$EXTV_{CC}$ ..... 42V
$V_{CC}$, $PV_{CC}$ ..... 6V
$V_{REF}$, $V_{SET1}$, $V_{SET2}$, FB, RT ..... 6V
PWM/SYNC, DIODE, ENA ..... 6V
$\overline{VALID1}$, $\overline{VALID2}$, PGOOD, $\overline{PRIORITY}$ ..... 6V
BST1 Pin Above COM1 ..... 6V
BST2 Pin Above COM2 ..... 6V
Operating Junction Temperature Range
(Notes 2, 4) ..... –40°C to 150°C
Storage Temperature ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
TSSOP ..... 300°C

## PIN CONFIGURATION




UFD PACKAGE
28-LEAD (4mm × 5mm) PLASTIC QFN

$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 34°C/W
EXPOSED PAD (PIN 29) IS PGND, MUST BE SOLDERED TO PCB




FE PACKAGE
28-LEAD PLASTIC TSSOP

$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 30°C/W
EXPOSED PAD (PIN 29) IS PGND, MUST BE SOLDERED TO PCB

## ORDER INFORMATION http://www.linear.com/product/LTC3126#orderinfo

| LEAD FREE FINISH | TAPE AND REEL | PART MARKING* | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|---|---|---|---|---|
| LTC3126EUFD#PBF | LTC3126EUFD#TRPBF | 3126 | 28-Lead (4mm × 5mm) Plastic QFN | –40°C to 125°C |
| LTC3126IUFD#PBF | LTC3126IUFD#TRPBF | 3126 | 28-Lead (4mm × 5mm) Plastic QFN | –40°C to 125°C |
| LTC3126EFE#PBF | LTC3126EFE#TRPBF | LTC3126FE | 28-Lead Plastic TSSOP (4.4mm) | –40°C to 125°C |
| LTC3126IFE#PBF | LTC3126IFE#TRPBF | LTC3126FE | 28-Lead Plastic TSSOP (4.4mm) | –40°C to 125°C |
| LTC3126HFE#PBF | LTC3126HFE#TRPBF | LTC3126FE | 28-Lead Plastic TSSOP (4.4mm) | –40°C to 150°C |
| LTC3126MPFE#PBF | LTC3126MPFE#TRPBF | LTC3126FE | 28-Lead Plastic TSSOP (4.4mm) | –55°C to 150°C |

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at $T_A$ = 25°C (Note 2). $PV_{IN1}$ = $V_{IN1}$ = 24V, $PV_{IN2}$ = $V_{IN2}$ = 12V, $V_{SET1}$ = $V_{SET2}$ = GND, unless otherwise noted.**

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Input Operating Voltage | After Start-Up | ● | 2.4 | | 42 | V |
| $V_{IN1}$, $V_{IN2}$ UVLO Threshold | $V_{IN1}$/$V_{IN2}$ Rising<br>$V_{IN1}$/$V_{IN2}$ Falling | ●<br>● | | 2.50<br>2.34 | 2.6<br>2.4 | V<br>V |
| $V_{CC}$ UVLO Threshold | $V_{CC}$ Rising<br>$V_{CC}$ Falling | ● | | 2.3<br>2.2 | 2.4<br>2.3 | V<br>V |
| $V_{IN1}$ Current in Disable | ENA Low, $V_{IN1}$ = 24V, $V_{IN2}$ = 12V<br>ENA Low, $V_{IN1}$ = 12V, $V_{IN2}$ = 24V | | | 1.35<br>0.55 | | µA<br>µA |
| $V_{IN2}$ Current in Disable | ENA Low, $V_{IN2}$ = 24V, $V_{IN1}$ = 12V<br>ENA Low, $V_{IN2}$ = 12V, $V_{IN1}$ = 24V | | | 1.35<br>0.55 | | µA<br>µA |
| $V_{IN1}$ Current in Standby | ENA High, Buck in UVLO, $V_{IN1}$ = 24V, $V_{IN2}$ = 12V<br>ENA High, Buck in UVLO, $V_{IN1}$ = 12V, $V_{IN2}$ = 24V | | | 1.65<br>0.55 | | µA<br>µA |
| $V_{IN2}$ Current in Standby | ENA High, Buck in UVLO, $V_{IN2}$ = 24V, $V_{IN1}$ = 12V<br>ENA High, Buck in UVLO, $V_{IN2}$ = 12V, $V_{IN1}$ = 24V | | | 1.65<br>0.55 | | µA<br>µA |
| $V_{IN1}$ Current, Operating from $V_{IN2}$ | ENA High, Buck Operating, $V_{IN1}$ = 24V, $V_{IN2}$ = 27V | | | 1.2 | | µA |
| $V_{IN2}$ Current, Operating from $V_{IN1}$ | ENA High, Buck Operating, $V_{IN2}$ = 24V, $V_{IN1}$ = 27V | | | 1.2 | | µA |
| Burst Mode Operation Quiescent Current from $V_{IN}$ | Not Switching, $V_{FB}$ = 0.850V | | | 5.5 | | µA |
| Oscillator Frequency | Programmable Frequency<br>$R_T$ Resistor = 33.2k | ●<br>● | 200<br>900 | <br>1000 | 2200<br>1100 | kHz<br>kHz |
| PWM/SYNC Applied Clock Frequency | | ● | 200 | | 2200 | kHz |
| PWM/SYNC High Pulse Width | | | 100 | | | ns |
| PWM/SYNC Low Pulse Width | | | 150 | | | ns |
| Logic Input Threshold (ENA, DIODE, PWM/SYNC) | | ● | 0.3 | 0.8 | 1.1 | V |
| Feedback Voltage | | <br>● | 812<br>804 | 818<br>818 | 824<br>832 | mV<br>mV |
| Feedback Voltage Line Regulation | $V_{IN1}$, $V_{IN2}$ = 2.4V to 42V | | | 0.2 | | % |
| Feedback Pin Current | | | –20 | 1 | 20 | nA |
| Feedback Pin Overvoltage Comparator Threshold | FB Rising, as a Percentage of the Feedback Voltage | | 7.4 | 9.8 | 12 | % |
| Feedback Pin Overvoltage Comparator Hysteresis | | | | 1.1 | | % |
| Soft-Start Duration | | | | 7.5 | | ms |
| PGOOD Threshold | FB Falling, as a Percentage of the Feedback Voltage | ● | –10.7 | –8.7 | –6.6 | % |
| PGOOD Threshold Hysteresis | | | | 1 | | % |
| PGOOD Delay | FB Falling | | | 200 | | µs |
| $V_{REF}$ Voltage | | <br>● | 0.995<br>0.982 | 1.000<br>1.000 | 1.005<br>1.018 | V<br>V |
| $V_{REF}$ Output Current | | | | | 1 | mA |
| $V_{REF}$ Current Limit | | | | 13 | | mA |
| $V_{BEST}$ Comparator Threshold | $V_{IN1}$ Rising, $V_{IN2}$ = 24V<br>$V_{IN1}$ Falling, $V_{IN2}$ = 24V | | | 24.18<br>23.83 | | V<br>V |
| $V_{BEST}$ Comparator Hysteresis | | | 280 | 365 | 450 | mV |
| $V_{BEST}$ Comparator Delay | $V_{IN1}$ Falling, $V_{IN2}$ = 24V<br>$V_{IN2}$ Falling, $V_{IN1}$ = 24V | | | 11<br>40 | | µs<br>µs |
| $V_{IN1}$, $V_{IN2}$ Input Valid Threshold, Rising | $V_{SET1}$ = $V_{SET2}$ = 1000mV<br>$V_{SET1}$ = $V_{SET2}$ = 500mV<br>$V_{SET1}$ = $V_{SET2}$ = 250mV<br>$V_{SET1}$ = $V_{SET2}$ = 150mV | ●<br>●<br>●<br>● | 19.8<br>9.9<br>4.9<br>2.91 | 20.0<br>10.0<br>5.0<br>3.0 | 20.2<br>10.1<br>5.1<br>3.09 | V<br>V<br>V<br>V |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at $T_A$ = 25°C (Note 2). $PV_{IN1}$, = $V_{IN1}$ = 24V, $PV_{IN2}$ = $V_{IN2}$ = 12V, $V_{SET1}$ = $V_{SET2}$ = GND, unless otherwise noted.**

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| $V_{IN1}$, $V_{IN2}$ Input Valid Threshold, Falling | $V_{SET1}$ = $V_{SET2}$ = 1000mV<br>$V_{SET1}$ = $V_{SET2}$ = 500mV<br>$V_{SET1}$ = $V_{SET2}$ = 250mV<br>$V_{SET1}$ = $V_{SET2}$ = 150mV | | 17.57<br>8.77<br>4.34<br>2.57 | 17.75<br>8.86<br>4.43<br>2.65 | 17.93<br>8.95<br>4.52<br>2.73 | V<br>V<br>V<br>V |
| $V_{IN1}$, $V_{IN2}$ Input Valid Threshold Hysteresis | As a Percentage of the Rising Threshold | | | 11 | | % |
| $V_{IN1}$, $V_{IN2}$ Input Valid Comparator Delay | $V_{IN1}$/$V_{IN2}$ Falling, 2V/µs, $V_{SET1}$/$V_{SET2}$ = 1V<br>$V_{IN1}$/$V_{IN2}$ Rising, 2V/µs, $V_{SET1}$/$V_{SET2}$ = 1V | | | 60<br>120 | | µs<br>µs |
| Open-Drain Output Voltage | PGOOD, $\overline{\text{PRIORITY}}$, $\overline{\text{VALID1}}$, $\overline{\text{VALID2}}$ | | | | 5.5 | V |
| Open-Drain Pull-Down Resistance | PGOOD, $\overline{\text{PRIORITY}}$, $\overline{\text{VALID1}}$, $\overline{\text{VALID2}}$ | | | 70 | | Ω |
| Open-Drain Leakage | PGOOD, $\overline{\text{PRIORITY}}$, $\overline{\text{VALID1}}$, $\overline{\text{VALID2}}$ | | | | 1 | µA |
| Low Side Switch Resistance | | | | 70 | | mΩ |
| High Side Switch Resistance | | | | 200 | | mΩ |
| Dropout Voltage | 1A Load, $V_{OUT}$ = 3.3V | | | 310 | | mV |
| High Side Switch Current Limit | (Note 3) | | 3.0 | 3.9 | 4.8 | A |
| Low Side Switch Current Limit | (Note 3) | | 3.8 | 5.2 | 6.8 | A |
| Zero Cross Threshold | PWM/SYNC = Low (Note 3)<br>PWM/SYNC = High or Clocked (Note 3) | | | 220<br>0 | | mA<br>mA |
| SW Leakage Current | $V_{IN1}$ = $V_{IN2}$ = $PV_{IN1}$ = $PV_{IN2}$ = 42V, $V_{SW}$ = 0V, 42V | | –3 | | 3 | µA |
| $V_{CC}$ Voltage | $I_{VCC}$ = 1mA | | 4.12 | 4.22 | 4.32 | V |
| $V_{CC}$ Current Limit | $V_{CC}$ = 3.5V | | 35 | 67 | | mA |
| $V_{CC}$ Drop-Out Voltage | Powered from $V_{IN1}$ or $V_{IN2}$, $V_{IN}$ = 2.4V, $I_{LOAD}$ = 5mA<br>Powered from $EXTV_{CC}$, $V_{EXTVCC}$ = 3.3V, $I_{LOAD}$ = 5mA | | | 70<br>100 | | mV<br>mV |
| $V_{CC}$ Load Regulation | $I_{LOAD}$ = 1mA to 15mA | | | 1.1 | | % |
| $EXTV_{CC}$ Applied Voltage | | | 3.15 | | 42 | V |
| $EXTV_{CC}$ Valid, Rising Threshold | | ● | 2.95 | 3.05 | 3.15 | V |
| $EXTV_{CC}$ Valid, Hysteresis | | | | 167 | | mV |
| $EXTV_{CC}$ Current in Shutdown | $EXTV_{CC}$ = 3.3V, ENA = Low | | | 0.2 | | µA |
| $EXTV_{CC}$ Current | Switching, $f_{SW}$ = 1MHz | | | 8.8 | | mA |
| Frequency Foldback Threshold on FB | | | | 200 | | mV |
| SW Minimum On-Time | $V_{IN}$ = 24V, 1A Load, $EXTV_{CC}$ = OPEN | | | 46 | | ns |
| SW Minimum Low-Time | | | | 100 | | ns |
| SW Frequency Foldback Factor | $V_{FB}$ < 0.2V | | | 16 | | |
| SW Frequency Divider in Drop-Out | | | | 8 | | |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LTC3126 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3126E is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specification over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3126I specifications are guaranteed over the –40°C to 125°C operating junction temperature range. The LTC3126H specifications are guaranteed over the –40°C to 150°C operating junction temperature range. The LTC3126MP specifications are guaranteed and tested over the –55°C to 150°C operating junction temperature range. High temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C.

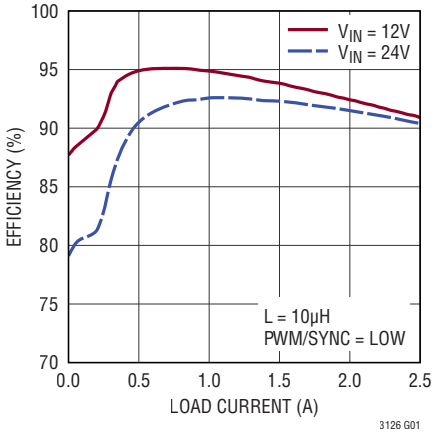
**Note 3:** Current measurements are performed when the LTC3126 is not switching. The current limit values measured in operation will be somewhat higher due to the propagation delay of the comparators.

**Note 4:** This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

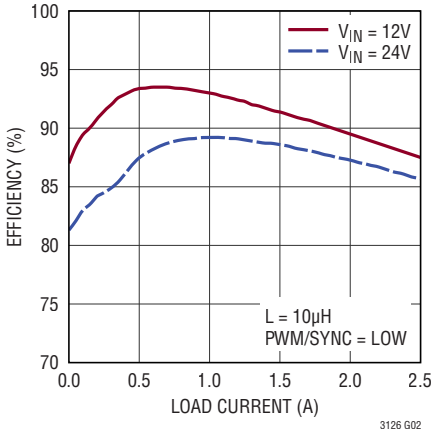
## TYPICAL PERFORMANCE CHARACTERISTICS

$T_A$ = 25°C, unless otherwise noted.

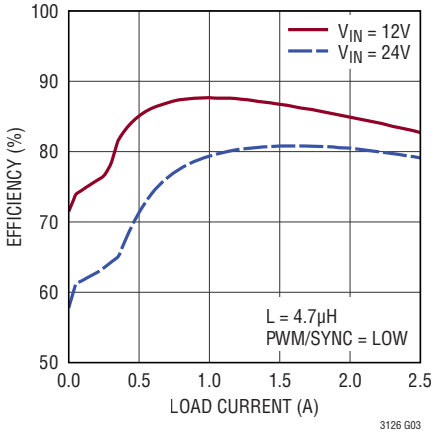
**Efficiency, $V_{OUT}$ = 5V, $f_{SW}$ = 700KHz**



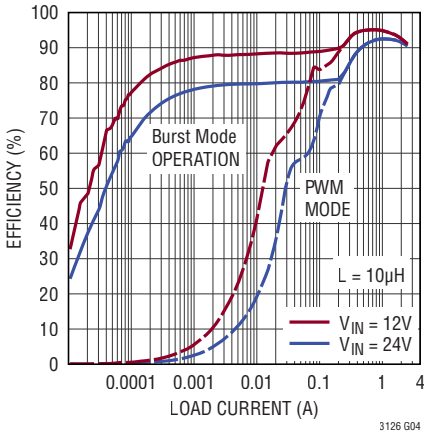

**Efficiency, $V_{OUT}$ = 3.3V, $f_{SW}$ = 700KHz**



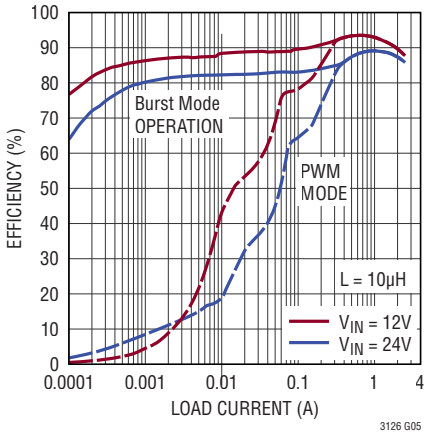

**Efficiency, $V_{OUT}$ = 1.8V, $f_{SW}$ = 700KHz**



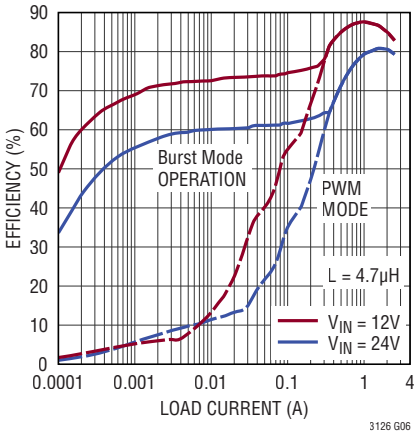

**Efficiency, $V_{OUT}$ = 5V, $f_{SW}$ = 700KHz**



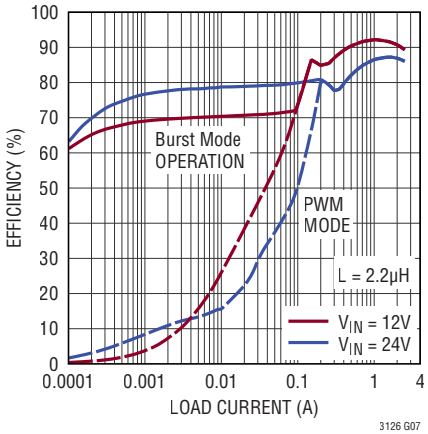

**Efficiency, $V_{OUT}$ = 3.3V, $f_{SW}$ = 700KHz**



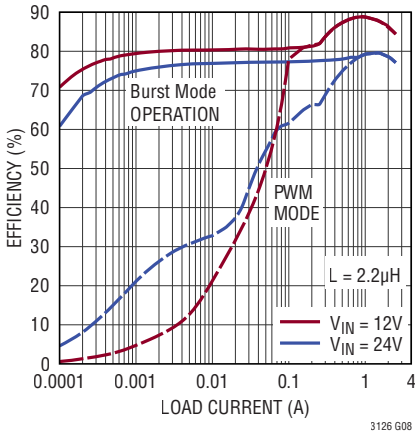

**Efficiency, $V_{OUT}$ = 1.8V, $f_{SW}$ = 700KHz**



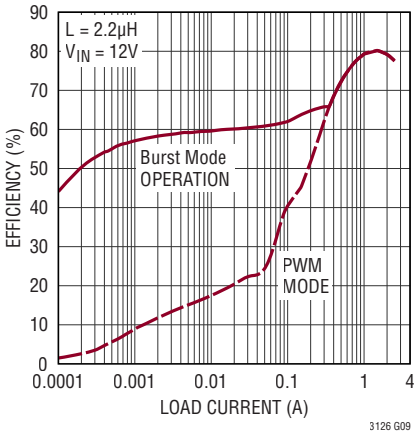

**Efficiency, $V_{OUT}$ = 5V, $f_{SW}$ = 2MHz**




**Efficiency, $V_{OUT}$ = 3.3V, $f_{SW}$ = 2MHz**



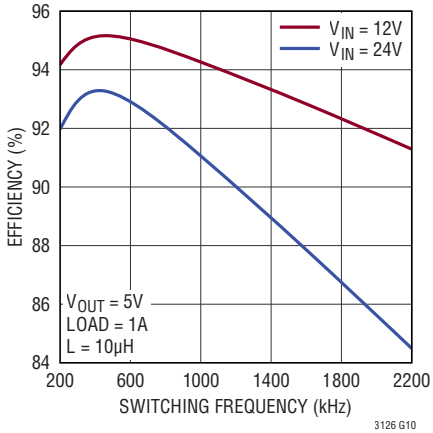

**Efficiency, $V_{OUT}$ = 1.8V, $f_{SW}$ = 2MHz**



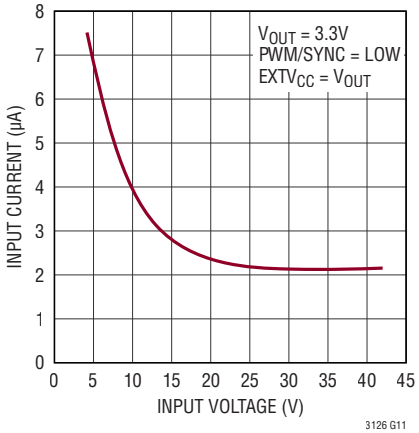
## TYPICAL PERFORMANCE CHARACTERISTICS

$T_A$ = 25°C, unless otherwise noted.

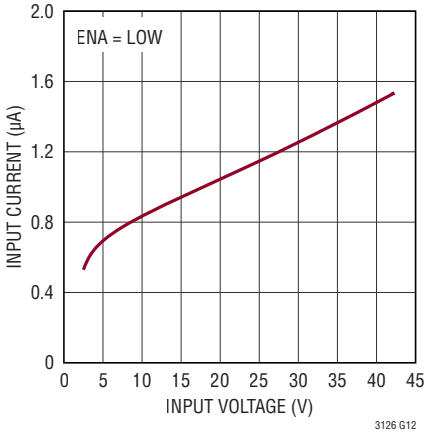
### Efficiency vs Switching Frequency



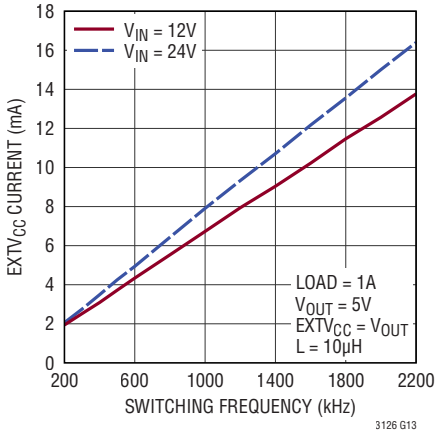

### No-Load Input Current



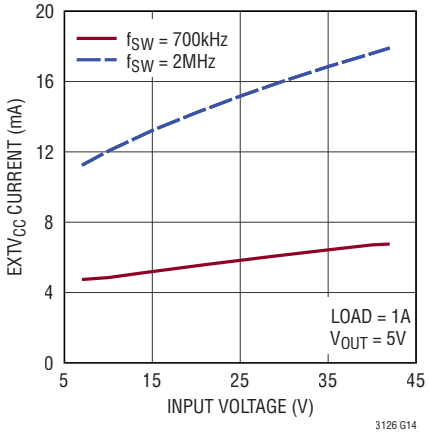

### Shutdown Current vs $V_{IN}$



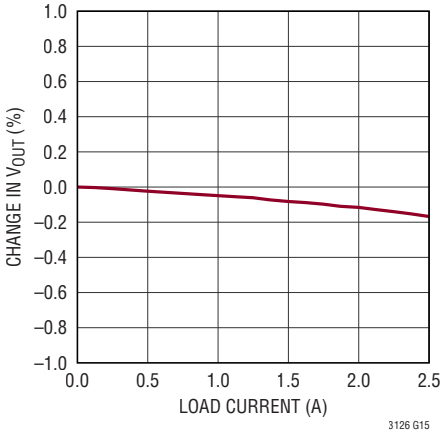

### $EXTV_{CC}$ Current vs Switching Frequency



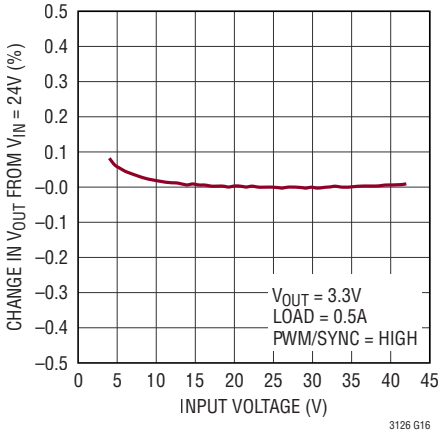

### $EXTV_{CC}$ Current vs Input Voltage



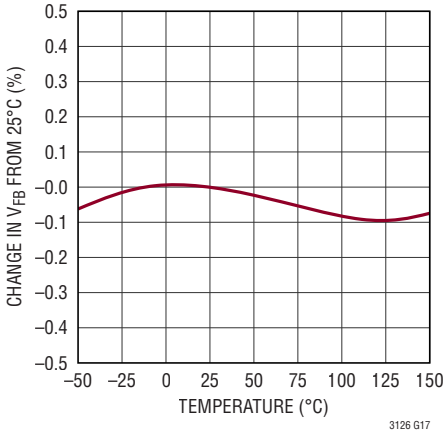

### Load Regulation



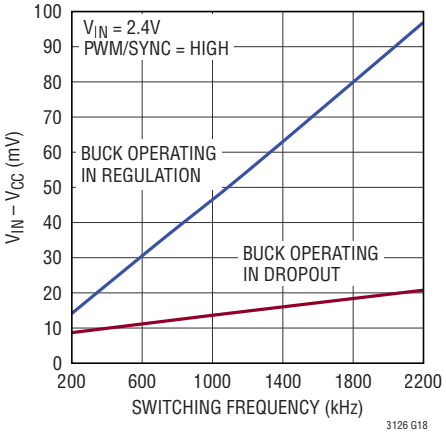

### Line Regulation




### FB Voltage vs Temperature



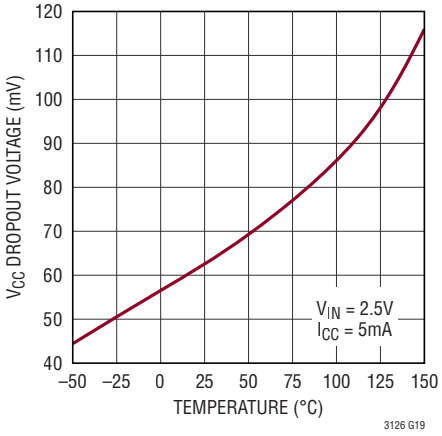

### $V_{CC}$ LDO Voltage Drop vs Switching Frequency



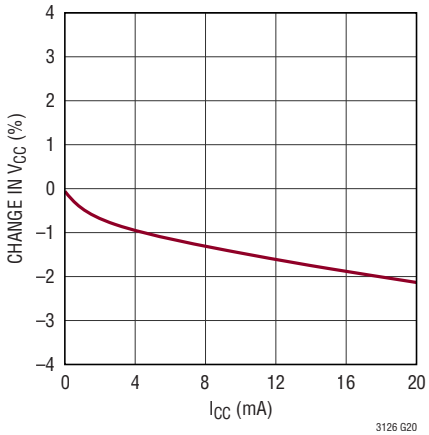
## TYPICAL PERFORMANCE CHARACTERISTICS

$T_A$ = 25°C, unless otherwise noted.

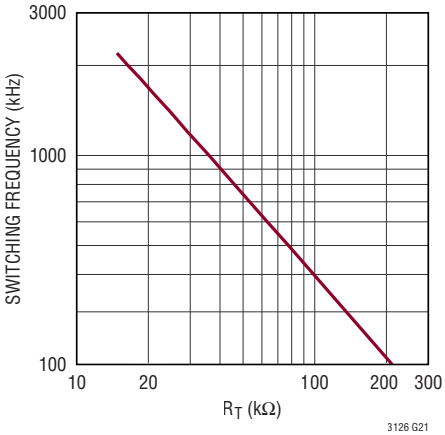
### $V_{CC}$ Dropout Voltage vs Temperature



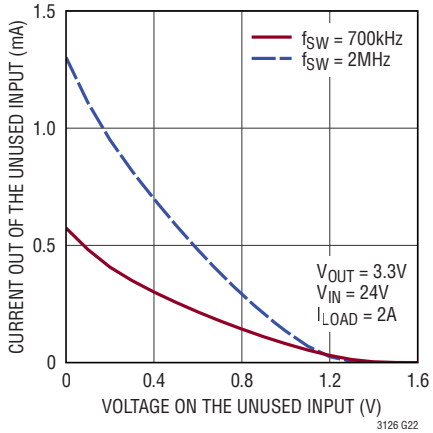

### $V_{CC}$ Load Regulation



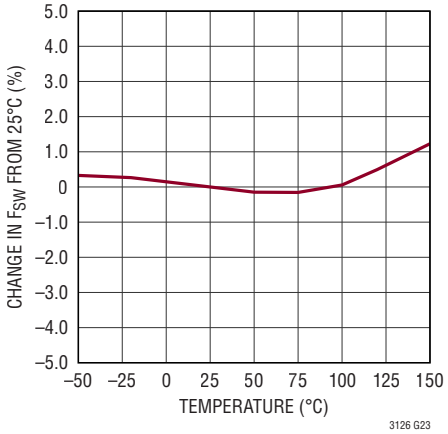

### Switching Frequency vs $R_T$



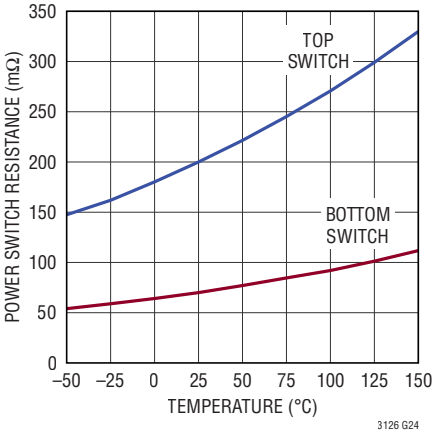

### Reverse Current Out of the Unused Input ($V_{IN1}$ or $V_{IN2}$)



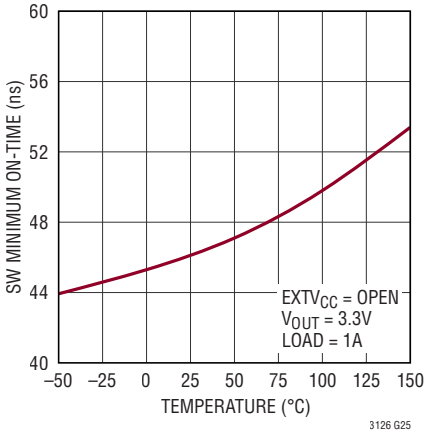

### Switching Frequency vs Temperature



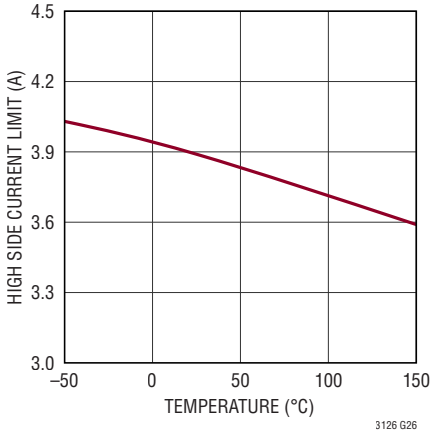

### Power Switch Resistance vs Temperature



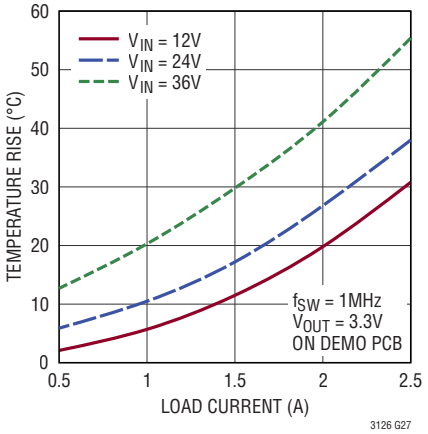

### Minimum On-Time vs Temperature




### High Side Current Limit Threshold vs Temperature



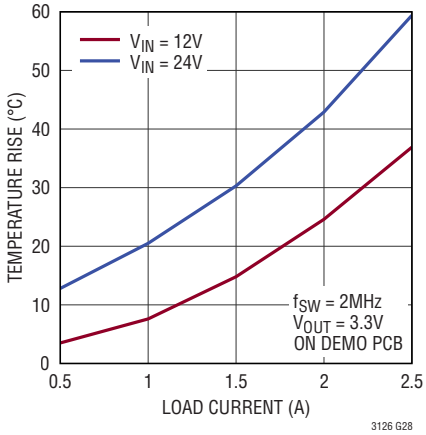

### Temperature Rise vs Load Current



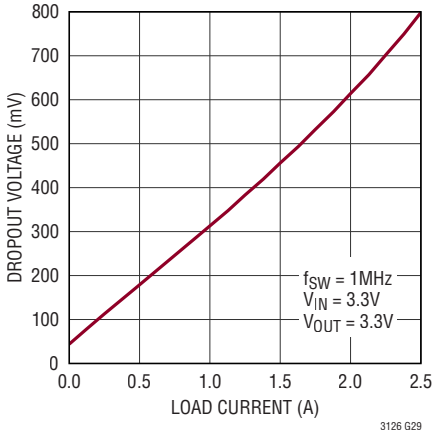
## TYPICAL PERFORMANCE CHARACTERISTICS

$T_A$ = 25°C, unless otherwise noted.

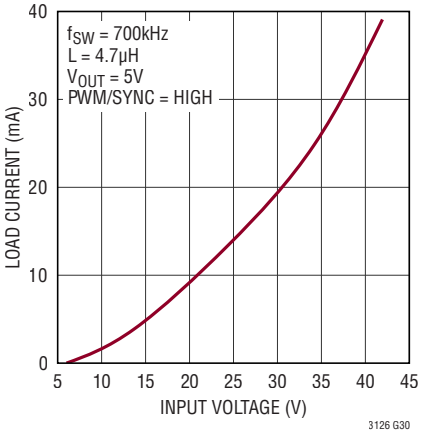
### Temperature Rise vs Load Current



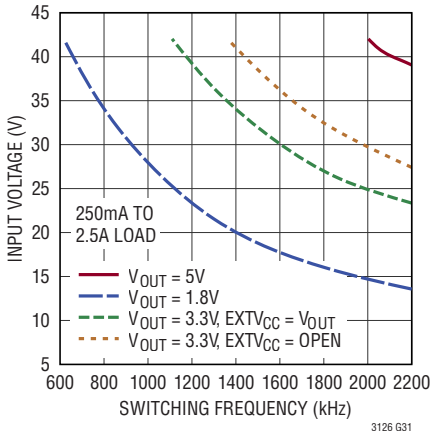

### Dropout Voltage vs Load Current



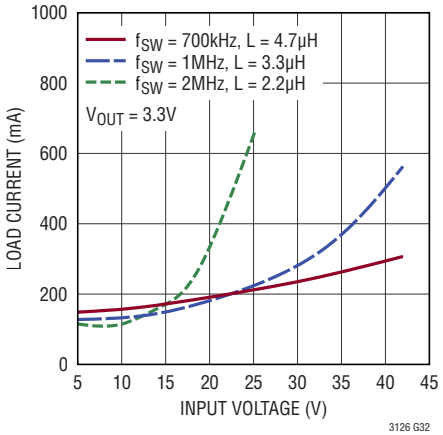

### Minimum Load for Full Frequency Switching (No Pulse Skipping)



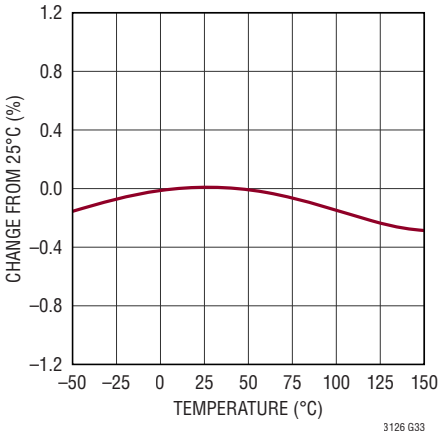

### Maximum Input Voltage without Pulse Skipping



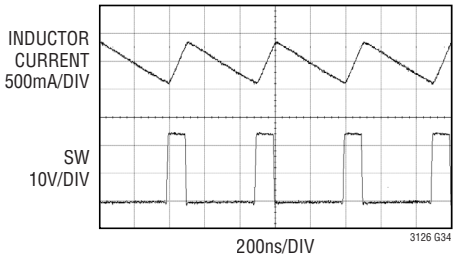

### Burst Mode Operation Threshold vs Input Voltage




### $V_{REF}$ vs Temperature

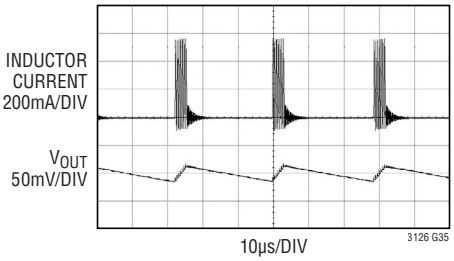



### Switching Waveforms, PWM Mode



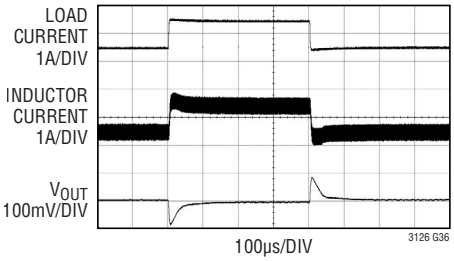

24V TO 5V AT 1A
L = 2.2µH
$f_{SW}$ = 2MHz

### Switching Waveforms, Burst Mode Operation




24V TO 5V AT 25mA
L = 2.2µH
$f_{SW}$ = 2MHz
$C_{OUT}$ = 47µF

### Load Step, 0.5A to 1.5A

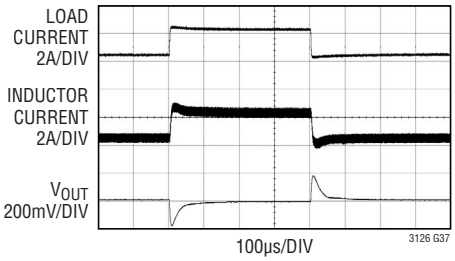



FRONT PAGE APPLICATION

## TYPICAL PERFORMANCE CHARACTERISTICS

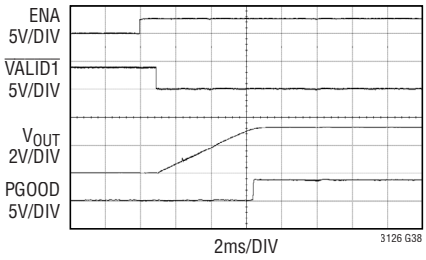
**$T_A$ = 25°C, unless otherwise noted.**

### Load Step, 0.5A to 2.5A



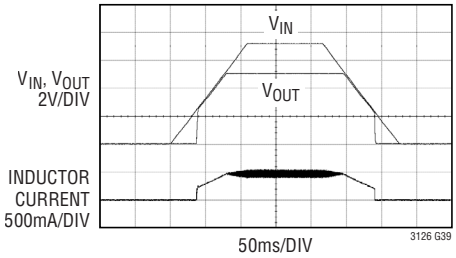

FRONT PAGE APPLICATION

### Start-Up Waveforms



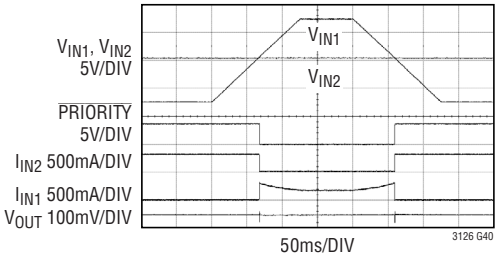

FRONT PAGE APPLICATION

### Start-Up Dropout Performance



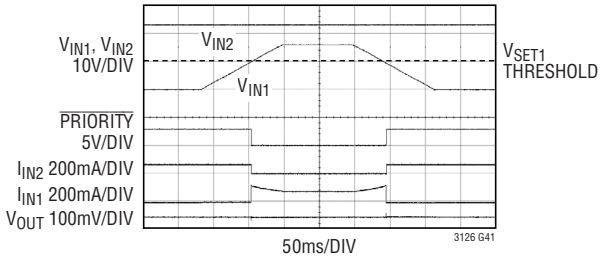

10Ω LOAD
$V_{OUT}$ = 5V

### Ideal Diode Mode Transition



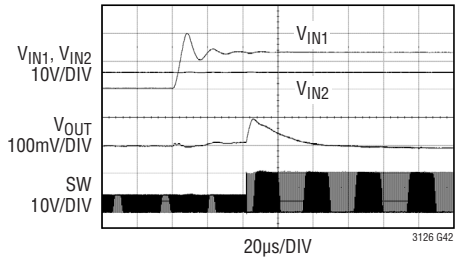

10Ω LOAD
$V_{OUT}$ = 5V

### Priority Mode Transition




10Ω LOAD
$V_{IN2}$ = 10V
$V_{OUT}$ = 3.3V

### Hot Plug of Automotive Input, $V_{IN1}$




FRONT PAGE APPLICATION
1A LOAD
$V_{IN1}$ = 13.8V
$V_{IN2}$ = 6V

## PIN FUNCTIONS (QFN/TSSOP)

**$V_{CC}$, $PV_{CC}$ (Pins 2, 3/Pins 5, 6):** Internal Linear Regulator Output and Power Supply for the Low Voltage Control Circuitry in the IC. Internal linear regulators generate a regulated voltage on these pins from either $V_{IN1}$, $V_{IN2}$ or $EXTV_{CC}$. $V_{CC}$ and $PV_{CC}$ must be connected together in the application. A 4.7µF or larger bypass capacitor must be connected between these pins and ground. The $V_{CC}$ rail remains powered in shutdown and can be used to supply up to 1mA to external loads.

**$EXTV_{CC}$ (Pin 4/Pin 7):** $V_{CC}$ Regulator Bootstrapping Pin. If this pin is forced to 3.15V or greater then $EXTV_{CC}$ will be used to power the internal $V_{CC}$ rail. Typically, the $EXTV_{CC}$ input is connected to the buck converter output voltage. Bootstrapping the internal $V_{CC}$ rail in this fashion provides a significant efficiency advantage and reduced quiescent current especially in applications with high input voltage and low output voltage. If the $EXTV_{CC}$ pin is left open then the $V_{CC}$ rail will be powered from the $V_{IN1}$ and $V_{IN2}$ pins.

**$V_{SET1}$, $V_{SET2}$ (Pins 5, 6/Pins 8, 9):** Programming Pins for the UVLO Thresholds on $V_{IN1}$ and $V_{IN2}$. The voltage on the $V_{SET1}$ and $V_{SET2}$ pins programs the UVLO threshold for the power source inputs $V_{IN1}$ and $V_{IN2}$, respectively. A voltage between zero and 1V programs a corresponding UVLO threshold between zero and 20V. However, there is also a fixed internal UVLO threshold (typically 2.34V) on each input which is always in effect. The voltage on $V_{SET1,2}$ can be set using a resistor divider from the accurate reference output, $V_{REF}$. Grounding $V_{SET1,2}$ will allow the respective input $V_{IN1,2}$ to be used down to the fixed, internal UVLO threshold.

**$V_{REF}$ (Pin 7/Pin 10):** Voltage Reference Output for Powering Resistor Dividers to Set the $V_{SET1}$ and $V_{SET2}$ Inputs. The voltage at this pin is regulated by the IC to maintain a high precision, temperature stable 1.0V output. Resistive dividers from the $V_{REF}$ pin can be used to set the voltage at the $V_{SET1}$ and $V_{SET2}$ pins and thereby program the UVLO threshold for each input. The $V_{REF}$ output may also be used as a general purpose voltage reference in the application, providing a temperature stable reference for comparators, DACs or other functions. The total current drawn from this pin must be limited to 1mA and the total capacitive load should be limited to 470pF. If this pin is not used in the application (i.e., if there is no resistor from $V_{REF}$ to ground) then the $V_{REF}$ pin must be connected to $V_{CC}$.

**GND (Pin 8/Pin 11):** Signal Ground. This pin is the ground connection for the control circuitry of the IC and must be tied to ground.

**FB (Pin 9/Pin 12):** Feedback Voltage Input. A resistor divider connected to this pin establishes the output voltage of the buck converter. Care should be taken in the routing of connections to this pin in order to minimize stray coupling to the SW, BST1, BST2, COM1 and COM2 pins.

**RT (Pin 10/Pin 13):** Switching Frequency Programming Pin. A resistor placed from this pin to ground sets the switching frequency of the buck converter.

**PGOOD (Pin 11/Pin 14):** Open-Drain Power Good Indicator for the Buck Converter Output Voltage. This output is driven low if the buck converter output voltage is more than 8.7% below the regulation voltage or more than 9.8% above the regulation voltage. The PGOOD pin is also driven low whenever the buck converter is disabled. The maximum voltage that can be applied to the PGOOD pin is 5.5V.

**$\overline{\text{PRIORITY}}$ (Pin 12/Pin 15):** Open-Drain Output Indicating That the Priority Input ($V_{IN1}$) Is Being Utilized. The $\overline{\text{PRIORITY}}$ pin is driven low if the part is enabled and the buck converter is operating from the priority input, $V_{IN1}$. In disable (ENA low) the $\overline{\text{PRIORITY}}$ pull-down is disabled, allowing the pin to float. The maximum voltage that can be applied to the $\overline{\text{PRIORITY}}$ pin is 5.5V.

**$PV_{IN2}$ (Pin 13/Pin 16):** Secondary Power Source Input for the Buck Converter. In priority mode (DIODE pin low) the buck converter will only operate from this input if the priority input power source is under voltage. This pin must be bypassed with a 4.7µF or larger ceramic capacitor to ground. If the $PV_{IN2}$ input will be subjected to inductive shorts to ground, then a power Schottky diode must be added from ground to $PV_{IN2}$ to prevent this pin from being driven below ground.

**ENA (Pin 14/Pin 17):** Enable Input. Forcing the ENA pin low disables the input voltage comparators, the $V_{REF}$ pin driver and the buck converter. The $V_{CC}$ rail remains powered in disable and therefore ENA can be connected to $V_{CC}$ to

## PIN FUNCTIONS (QFN/TSSOP)

continuously enable the part. The maximum voltage that can be applied to the ENA pin is 5.5V.

**PGND (Pins 18, 19, Exposed Pad Pin 29/Pins 21, 22, Exposed Pad Pin 29):** Power Ground Connections. These pins must be connected to ground in the application.

For optimal thermal performance, the backpad should be soldered to the PC board and the PC board should be designed with the maximum possible number of vias connecting the backpad to the ground plane.

**SW (Pins 17, 20/Pins 20, 23):** Power Switch Inductor Connections. This pin should be connected to one side of the buck converter inductor.

**COM1, COM2 (Pins 16, 21/Pins 19, 24):** Negative Termination for Charge Pump Capacitors. External 0.1µF capacitors (with 5V rating or greater) must be connected between BST1 and COM1 and between BST2 and COM2.

**BST1, BST2 (Pins 15, 22/Pins 18, 25):** High Side Gate Driver Supply Rails. External 0.1µF capacitors (with 5V rating or greater) must be connected between BST1 and COM1 and between BST2 and COM2. These pins are used to generate a gate drive rail for the high side power devices.

**DIODE (Pin 23/Pin 26):** Logic Input Used to Select Between Ideal Diode-OR and Priority Modes. The integrated power path allows operation from either of two input power sources, $V_{IN1}$ or $V_{IN2}$. An input is considered valid for use only if its voltage is above the UVLO threshold for that input as programmed by the respective voltage at the $V_{SET1}$ or $V_{SET2}$ pin. If DIODE is high then the part operates in ideal-diode mode and the buck converter will operate from the highest voltage valid input ($V_{IN1}$ or $V_{IN2}$). If DIODE is low then the part operates in priority mode and the buck converter will operate from $V_{IN1}$ whenever it is valid and will switch to $V_{IN2}$ only if $V_{IN1}$ becomes invalid. In either mode, if both inputs are under voltage then the buck converter will be disabled.

**$PV_{IN1}$ (Pin 24/Pin 27):** Priority Power Source Input for the Buck Converter. In priority mode (DIODE pin low) the buck converter will preferentially operate from this input if both input power sources are valid (above their respective UVLO thresholds). This pin must be bypassed with a 4.7µF or larger ceramic capacitor to ground. If the $PV_{IN1}$ input will be subjected to inductive shorts to ground, then a power Schottky diode must be added from ground to $PV_{IN1}$ to prevent this pin from being driven below ground.

**$V_{IN1}$ (Pin 25/Pin 28):** Priority Power Source Kelvin Connection. This pin must be bypassed with a 0.1µF ceramic capacitor to ground. The $V_{IN1}$ pin must be connected to $PV_{IN1}$ in the application.

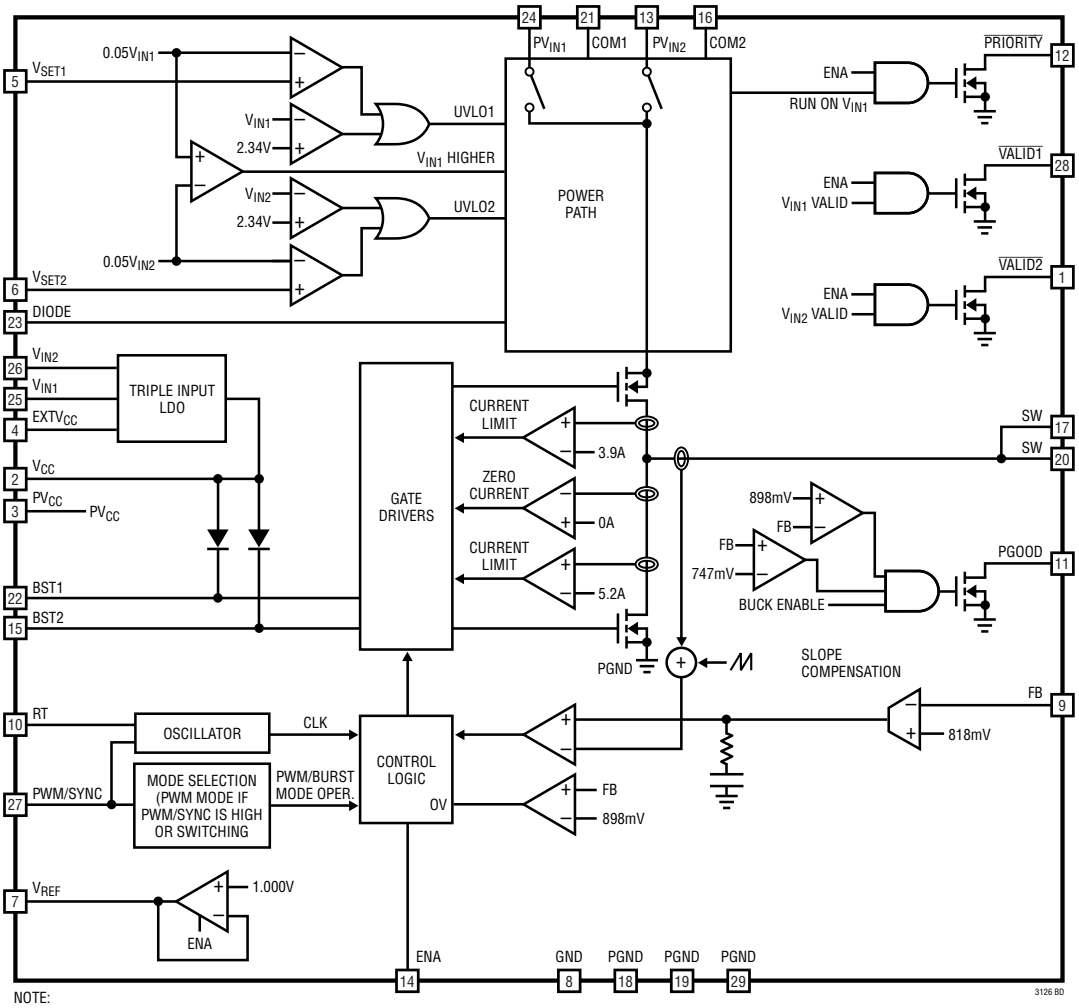
**$V_{IN2}$ (Pin 26/ Pin 1):** Secondary Power Source Kelvin Connection. This pin must be bypassed with a 0.1µF ceramic capacitor to ground. The $V_{IN2}$ pin must be connected to $PV_{IN2}$ in the application.

**PWM/SYNC (Pin 27/Pin 2):** PWM/Burst Mode Operation Control and External Synchronization Clock Input. Forcing this pin high causes the buck converter to operate in PWM mode. In PWM mode, the converter maintains fixed frequency operation over the widest range of load currents possible, leaving fixed frequency operation only at extremely light loads where the converter skips pulses to maintain regulation. Forcing the PWM/SYNC pin low causes the IC to utilize Burst Mode operation at light loads and automatically transition to PWM mode at higher load current. Burst Mode operation improves light load efficiency and significantly reduces no-load input quiescent current at the expense of modestly increased output voltage ripple. In addition, an external clock can be applied to the PWM/SYNC pin for synchronization purposes. When synchronized to an external clock the buck converter operates in PWM mode (Burst Mode operation is disabled).

**$\overline{VALID1}$, $\overline{VALID2}$ (Pins 1, 28/Pins 3, 4):** Open-Drain Outputs Indicating Whether the $V_{IN1}$ and $V_{IN2}$ Inputs Are Valid. When the part is enabled (ENA is high) $\overline{VALID1}$ and $\overline{VALID2}$ are driven low if the voltage at the $V_{IN1}$ or $V_{IN2}$ input is above the UVLO threshold set by the respective $V_{SET1}$ or $V_{SET2}$ pin. When the part is disabled (ENA is low) the $\overline{VALID1}$ and $\overline{VALID2}$ pull-downs are disabled allowing the pins to float. The maximum voltage that can be applied to the $\overline{VALID1}$ and $\overline{VALID2}$ pins is 5.5V.

## BLOCK DIAGRAM

**Pin numbers shown for QFN package**




NOTE:
$PV_{IN1}$ AND $V_{IN1}$ MUST BE CONNECTED TOGETHER IN THE APPLICATION
$PV_{IN2}$ AND $V_{IN2}$ MUST BE CONNECTED TOGETHER IN THE APPLICATION
$V_{CC}$ AND $PV_{CC}$ MUST BE CONNECTED TOGETHER IN THE APPLICATION

## QUICK REFERENCE

This section of the data sheet contains all of the equations necessary for external component selection as well as key part usage notes all compiled into one location for ease of use.

### Switching Frequency

The buck converter switching frequency, $f_{SW}$, is set by the value of $R_T$ resistor connected between the RT pin and ground according to the following equation:

$$R_T = \frac{33.2MHz}{f_{SW}}\ k\Omega$$

**Table 1. $R_T$ Value for Common Switching Frequencies**

| $f_{SW}$ | $R_T$ |
|---|---|
| 300kHz | 110kΩ |
| 500kHz | 66.5kΩ |
| 750kHz | 44.2kΩ |
| 1.0MHz | 33.2kΩ |
| 1.2MHz | 27.4kΩ |
| 1.5MHz | 22.1kΩ |
| 2.0MHz | 16.5kΩ |

# QUICK REFERENCE

## Output Voltage

The buck converter output voltage is set via a resistor divider connected to the FB pin as shown in Figure 1.

In most applications, choosing $R_{TOP}$ equal to 1MΩ represents a good trade-off between quiescent current and robustness against PCB leakage. $R_{BOT}$ can be determined by the following equation where $V_{OUT}$ is the desired output voltage:

$$R_{BOT} = \frac{R_{TOP}}{\left(\frac{V_{OUT}}{0.818V} - 1\right)}$$

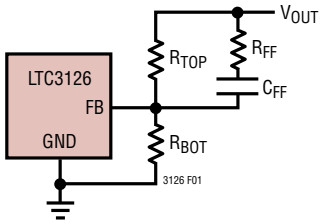



**Figure 1. FB Resistor Divider**

## Inductor Value

If the buck converter will be operated at duty cycles greater than 50% (i.e., $V_{IN} < 2V_{OUT}$) then the inductor value must be equal or greater than $L_{MIN}$ as defined by the following equation:

$$L_{MIN} = \frac{MHz}{f_{SW}} \bullet \frac{V_{OUT}}{2V}\ \mu H$$

**Table 2. Recommended Minimum Inductor Values**

| $f_{SW}$ = 750kHz | |
|---|---|
| $V_{OUT}$ | MINIMUM INDUCTOR VALUE |
| 12V | 8.0µH |
| 5V | 3.3µH |
| 3.3V | 2.2µH |
| 1.8V | 1.2µH |

| $f_{SW}$ = 1MHz | |
|---|---|
| $V_{OUT}$ | MINIMUM INDUCTOR VALUE |
| 12V | 6.0µH |
| 5V | 2.5µH |
| 3.3V | 1.8µH |
| 1.8V | 1.0µH |

| $f_{SW}$ = 2MHz | |
|---|---|
| $V_{OUT}$ | MINIMUM INDUCTOR VALUE |
| 12V | 3.3µH |
| 5V | 1.5µH |
| 3.3V | 1.0µH |
| 1.8V | 1.0µH |

The peak-to-peak inductor ripple, $\Delta I_L$, is given by the following equation.

$$\Delta I_L = \frac{V_{OUT}}{f_{SW} \bullet L}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

## Output Capacitor

The recommended minimum output capacitor, $C_{MIN}$, is given below as a function of output voltage:

$$C_{MIN} = \frac{1V}{V_{OUT}} 150\mu F$$

**Table 3. Minimum Output Capacitor vs $V_{OUT}$**

| $V_{OUT}$ | MINIMUM $C_{OUT}$ |
|---|---|
| 24V | 10µF |
| 12V | 22µF |
| 5V | 33µF |
| 3.3V | 47µF |
| 1.8V | 100µF |
| 1.2V | 150µF |

## QUICK REFERENCE

### $V_{IN1}$, $V_{IN2}$ UVLO Thresholds

The $V_{IN1}$ and $V_{IN2}$ UVLO thresholds are set by the voltage on the $V_{SET1}$ and $V_{SET2}$ pins respectively. Each UVLO threshold can be set from a maximum of 20V down to the internal fixed UVLO threshold of 2.34V using a resistor divider from the $V_{REF}$ output as shown in Figure 2. The rising UVLO threshold is given by the following equation:

$$V_{UVLO1,2} = 20V_{SET1,2} = 20V\frac{R2}{R1+R2}$$

Grounding the $V_{SET1,2}$ pin will define the respective input as valid down to the fixed internal UVLO threshold of 2.34V.

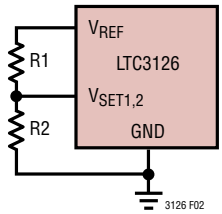



**Figure 2. Input UVLO Threshold Divider**

### External Synchronization Clock Frequency

The buck converter can be synchronized to an external clock applied to the PWM/SYNC pin. The frequency of the external clock must be higher than the internal oscillator frequency as set by the RT pin. In order to accommodate the ±10% possible variation in the oscillator frequency, the $R_T$ resistor should be chosen to set the internal oscillator frequency at least 10% below the lowest synchronization frequency. For example, to synchronize to an external 1MHz clock, $R_T$ should be picked to set the internal oscillator at 900kHz or lower.

### Feedforward Capacitor

The feedforward capacitor, $C_{FF}$, as shown in Figure 1 improves the noise robustness of the FB pin and adds a zero to the loop at the frequency $f_{ZERO}$ given below:

$$f_{ZERO} = \frac{1}{2\pi \bullet R_{TOP} \bullet C_{FF}}$$

In most applications performance will be optimized if the zero frequency is set at approximately 16kHz. In applications with large output capacitance, a larger feedforward capacitor can be utilized to reduce the zero frequency and improve the transient response and phase margin. As shown in Figure 1, a 10k feedforward resistor, $R_{FF}$, can be added to improve noise immunity in applications with high output voltage ripple or a long distance between the resistor divider and $V_{OUT}$.

### Open-Drain Outputs

The open-drain outputs (PGOOD, $\overline{\text{PRIORITY}}$, $\overline{\text{VALID1}}$ and $\overline{\text{VALID2}}$) are low voltage pins and cannot be pulled up to a voltage higher than 5.5V. PGOOD is forced low in disable.

### Logic Inputs

The logic input pins (DIODE, ENA, PWM/SYNC) are low voltage pins and cannot be forced above 5.5V. To force any of these pins continuously high, the pin can be connected to $V_{CC}$.

### Important Usage Notes

1. $PV_{IN1}$ and $V_{IN1}$ must be connected together in the application. $PV_{IN2}$ and $V_{IN2}$ must be connected together in the application. $PV_{IN1}$ and $PV_{IN2}$ must each have a 4.7µF or larger bypass capacitor installed and placed as close to the pin as possible. In addition, $V_{IN1}$ and $V_{IN2}$ should have a separate 0.1µF bypass capacitor installed as close to the pin as possible.
2. The two SW pins must be connected together in the application.
3. $V_{CC}$ and $PV_{CC}$ must be connected together in the application and should be bypassed with a 4.7µF or larger capacitor.
4. If the $V_{REF}$ pin is not used in the application (i.e., there is no resistor from $V_{REF}$ to GND) then the $V_{REF}$ pin must be connected to $V_{CC}$.
5. If $PV_{IN1}$ or $PV_{IN2}$ can be driven below ground in the application, for example due to large inductive ringing at the input, then Schottky diodes must be installed from ground to $PV_{IN1}$/$PV_{IN2}$ to protect the LTC3126.

## OPERATION

The LTC3126 is a dual-input synchronous monolithic buck converter featuring the ability to operate from two different input power sources with voltage ranges from 2.4V to 40V. An integrated lossless power path eliminates the need for an external diode-OR circuit or another type of external power path enabling a complete multi-input power supply solution with higher efficiency, fewer components, lower quiescent current and reduced drop-out voltage. The LTC3126 integrates all of the control circuitry required to automatically transition between two input power sources based on user programmable UVLO thresholds and selectable ideal-diode and priority modes. These features allow the LTC3126 to serve as a complete single chip power supply solution from a variety of different power sources including automotive, wall adapter, USB/Firewire and a wide range of battery chemistries. In addition, the LTC3126 is ideally suited for capacitor backup supplies with its ability to automatically transition to a capacitive backup rail when primary power is interrupted. A low 1µA quiescent current in disable and 2µA operating current make the LTC3126 ideally suited for battery powered and automotive applications.

### PowerPath Operation

The power path controls whether the buck converter operates from the $V_{IN1}$ or $V_{IN2}$ input based on programmable undervoltage lockout thresholds for each input. The UVLO architecture used by the LTC3126 eliminates the need to connect external resistor dividers directly to the input voltages thereby providing a substantial reduction in quiescent current.

The $V_{SET1}$ and $V_{SET2}$ pins are used to set the undervoltage lockout thresholds for the two power source inputs $V_{IN1}$ and $V_{IN2}$ respectively. The UVLO threshold for each input can be independently set to any voltage from 20V down to the internal fixed UVLO threshold of 2.34V using an external resistor divider as shown in Figure 3. The $V_{REF}$ pin is regulated to a fixed, temperature stable 1.0V. An external resistor divider from the $V_{REF}$ pin is used to establish the voltage at the $V_{SET1}$ and $V_{SET2}$ pins. The programmed voltage at the $V_{SET1,2}$ pin is compared to the respective input voltage ($V_{IN1}$ or $V_{IN2}$) scaled down through an internal resistor divider with a ratio of 20:1 to determine if that input is undervoltage. As a result, a voltage

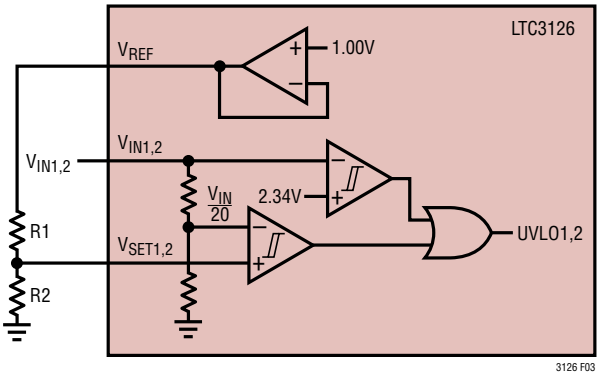



**Figure 3. Programming the UVLO Thresholds on $V_{IN1}$ and $V_{IN2}$**

range of zero to 1V on the $V_{SET1,2}$ corresponds to a UVLO threshold of zero to 20V on $V_{IN1,2}$. In addition, there is a fixed internal minimum UVLO threshold of 2.34V which is always enforced independent of the programmed voltage on the $V_{SET1}$ and $V_{SET2}$ pins. To enable a channel down to this minimum UVLO threshold, the respective $V_{SET1,2}$ pin can be simply connected to ground.

The LTC3126 power path has two operational modes as determined by the state of the DIODE logic input. With DIODE high, the part utilizes ideal diode-OR mode and operates from the input that has the higher voltage (assuming both inputs are above their respective UVLO thresholds). If one input is in UVLO then the other input will be utilized. If both inputs are in UVLO then the buck converter will be disabled. With the DIODE input low, the part operates in priority mode whereby $V_{IN1}$ is always given priority and is utilized as long as it is above its UVLO threshold. If $V_{IN1}$ is in UVLO then $V_{IN2}$ is utilized as long as it is not in UVLO. If both $V_{IN1}$ and $V_{IN2}$ are in UVLO then the buck converter is disabled.

All current drawn from the $V_{REF}$ pin is supplied by one of the inputs, $V_{IN1}$ or $V_{IN2}$. If neither input is above its respective UVLO threshold, then this current will be drawn from the input with the higher voltage. Otherwise, this current will be drawn by the active channel as determined by the power path. The $V_{REF}$ pin current will be supplied by the $EXTV_{CC}$ pin if that pin is utilized and has a valid voltage present.

The $\overline{\text{PRIORITY}}$, $\overline{\text{VALID1}}$ and $\overline{\text{VALID2}}$ open-drain outputs provide feedback on the state of the power path. The $\overline{\text{VALID1}}$ and $\overline{\text{VALID2}}$ outputs indicate that the respective input is present and above its UVLO threshold. Specifically,

## OPERATION

the $\overline{\text{VALID1}}$ pin is driven low if the part is enabled (ENA is high) and $V_{IN1}$ is above its UVLO threshold. The $\overline{\text{VALID2}}$ pin is driven low if the part is enabled and $V_{IN2}$ is above its UVLO threshold. The $\overline{\text{PRIORITY}}$ pin is driven low if the part is enabled and the buck converter is operating from the priority channel, $V_{IN1}$. The $\overline{\text{PRIORITY}}$ pin provides the ability to determine which input is being utilized in ideal-diode mode when both inputs are valid.

The $V_{CC}$ rail stays powered even when the LTC3126 is disabled (ENA is low) as long as either $V_{IN1}$ or $V_{IN2}$ is powered. In this disabled state, the $V_{CC}$ output is powered from whichever input ($V_{IN1}$ or $V_{IN2}$) is higher in voltage independent of the state of the DIODE pin. Given that the $V_{CC}$ output remains powered in shutdown, the ENA pin can be connected to $V_{CC}$ to continuously enable the part.

### Buck Converter Operation

The LTC3126 buck converter utilizes constant frequency switching with peak current mode control to provide low noise operation. The switching frequency can be set from 200kHz to 2.2MHz by appropriate choice of the RT pin resistor. In addition, the buck converter can be synchronized to an external clock applied to the PWM/SYNC pin.

The buck converter always operates from a single input power source ($V_{IN1}$ or $V_{IN2}$) at any time. The input that is used is determined by the state of the DIODE input, the programmed UVLO thresholds and the voltage of each input as described in the PowerPath Operation section. Each switching cycle begins with the high side switch of the active input turning on. The high side switch remains on until the inductor current reaches the current level set by the output of the internally compensated error amplifier. At that point, the low side synchronous rectifier turns on and remains on for the remainder of the cycle or until the inductor current falls to zero. The error amplifier continuously adjusts the commanded current level to maintain regulation of the FB pin voltage.

If PWM/SYNC is forced high or has an external clock applied, then the buck converter will operate in PWM mode. In PWM mode operation, the buck converter will maintain fixed frequency switching at all possible load currents, switching to pulse skipping only at very light load currents when the minimum on-time of the SW is reached. PWM mode provides low noise, fixed frequency operation and low output voltage ripple over the widest possible range of load currents and should be used when it is necessary to maintain the lowest possible noise levels. With PWM/SYNC forced low, the converter will automatically transition to Burst Mode operation at light loads to increase efficiency and reduce no-load quiescent current.

The LTC3126 buck converter is current limit protected to prevent damage to the IC during output overload and short-circuit conditions. If the inductor current exceeds the high side switch current limit threshold then the high side switch is turned off for the remainder of the cycle. If the inductor current exceeds the low side current limit threshold, then the high side switch will remain off during the next cycle to prevent increasing the inductor current further during the high side switch minimum on-time. In addition, the switching frequency is reduced by a factor of 16 if the FB voltage is below 200mV to ensure control of the inductor current is maintained during output overcurrent conditions.

The internal circuitry of the buck converter including the gate drivers is powered from $V_{CC}$. Internal LDOs generate the $V_{CC}$ rail from the active input, $V_{IN1}$ or $V_{IN2}$. In applications where the buck converter output is 3.3V or greater, the $V_{CC}$ rail can be bootstrapped by connecting the $EXTV_{CC}$ pin to the buck converter output. This allows a third LDO to generate the $V_{CC}$ rail directly from $EXTV_{CC}$. Given that the buck converter has much greater efficiency than the LDOs, bootstrapping via the $EXTV_{CC}$ pin increases the efficiency of the converter and reduces its quiescent current. This is particularly the case for applications with high input voltage, low output voltage and high switching frequencies.

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### Input UVLO Thresholds on $V_{IN1}$, $V_{IN2}$

The undervoltage lockout threshold for each input, $V_{IN1}$ and $V_{IN2}$, is set by the voltage on the $V_{SET1}$ and $V_{SET2}$ pins respectively. A voltage between 0V and 1V on $V_{SET1,2}$ linearly programs a corresponding UVLO threshold of zero to 20V. There is also an additional internal minimum undervoltage lockout threshold of 2.34V on each input which is always in effect independent of the voltage at the $V_{SET1,2}$ pins. To allow an input to operate fully down to the internal minimum UVLO threshold, the respective $V_{SET1,2}$ pin can be connected to ground.

In most applications, the voltage at the $V_{SET1}$ and $V_{SET2}$ pin is established using a resistor divider from the $V_{REF}$ pin as shown in Figure 4. The corresponding rising UVLO threshold is given by the following equation:

$$V_{UVLO1,2} = 20V_{SET1,2} = 20V\frac{R2}{R1+R2}$$

When neither input is valid (above its respective UVLO threshold), the current drawn from the $V_{REF}$ pin will add directly to the quiescent current of the higher voltage input ($V_{IN1}$ or $V_{IN2}$). Therefore, use of large value resistors in the $V_{SET1,2}$ divider string will reduce the quiescent current. However, larger value resistors also result in lower immunity to noise and leakage currents. A reasonable compromise in most applications is to utilize a total resistor string impedance of 1MΩ.

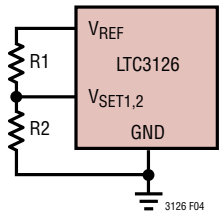


**Figure 4. Setting the Input UVLO Thresholds**

To minimize quiescent current and eliminate an external resistor it is also possible to set both UVLO thresholds via a single resistor string as shown in Figure 5. The upper resistor divider tap is connected to whichever pin, $V_{SET1}$ or $V_{SET2}$, requires the higher UVLO threshold.

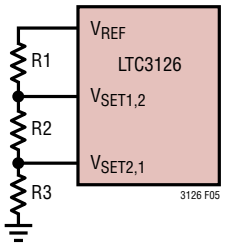


**Figure 5. Setting Both Input UVLO Thresholds Using a Single Resistor String**

Resistor R3 can be chosen independently and selecting R3 equal to 200k is a reasonable starting choice for most applications. The value of R2 and R1 can then be determined from the following equations where $V_{UVLOH}$ is the undervoltage lockout threshold on the higher voltage channel and $V_{ULVOL}$ is the UVLO threshold on the lower voltage channel:

$$R2 = R3\left(\frac{V_{UVLOH}}{V_{UVLOL}} - 1\right)$$

$$R1 = (R2+R3)\left(\frac{20}{V_{UVLOH}} - 1\right)$$

If the resulting total resistance through the resistor chain (R1 + R2 + R3) is larger or smaller then desired, the choice of R3 can be adjusted in the appropriate direction and the calculation for R2 and R1 can be repeated.

### Input Hold-Up Capacitance

The LTC3126 features internal micropower UVLO comparators which minimize the quiescent current required by the application. However, due to their low operating current, the UVLO comparators exhibit a significant delay when responding to an undervoltage condition. Sufficient input hold-up capacitance must be provided to ensure the voltage on the utilized channel remains sufficient to power the buck converter until the transition to the secondary channel is completed.

Consider the example illustrated in Figure 6 where the LTC3126 is being powered by the priority input ($V_{IN1}$) at 12.8V and the UVLO threshold on the $V_{IN1}$ channel is

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programmed to 10V. At time $t_1$, the priority input is unplugged and the buck converter begins discharging the input capacitor. At time $t_2$, the UVLO threshold is reached but the buck converter remains operating from the priority channel due to the comparator delay. At time $t_3$, after comparator delay $t_{DELAY}$, the buck converter switches over to the secondary input ($V_{IN2}$) and the input capacitor on $V_{IN1}$ maintains its voltage since there is no longer any current being drawn on that channel. In this example, the input capacitor on $V_{IN1}$ must be large enough that $V_{IN1}$ remains at sufficient voltage to maintain the output voltage in regulation until time $t_3$. If $V_{IN1}$ is allowed to drop lower than the regulated output voltage then the buck converter output will temporarily lose regulation during the transition.

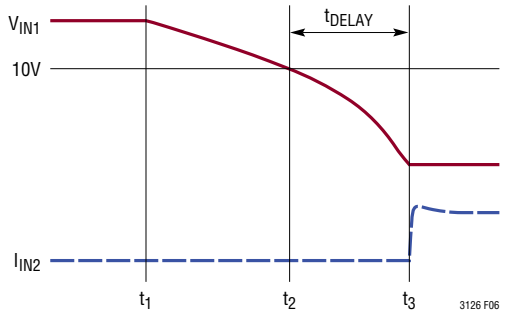


**Figure 6. Waveforms During Transition from $V_{IN1}$ to $V_{IN2}$**

The required value of hold-up capacitance, $C_{IN}$, can be estimated from the following equation where $V_{OUT}$ is the buck converter regulated output voltage, $I_{LOAD}$ is the buck converter load current, $\eta$ is the buck converter efficiency, $V_{UVLO}$ is the falling UVLO threshold of the active channel and $V_{MIN}$ is the minimum required input voltage needed for the buck converter to maintain regulation.

$$C_{IN} = \frac{2V_{OUT} \bullet I_{LOAD} \bullet t_{DELAY}}{\eta\left(V_{UVLO}^2 - V_{MIN}^2\right)}$$

In the example from Figure 6, the UVLO threshold, $V_{UVLO}$, is 10V. The typical comparator delay of $t_{DELAY}$ = 60µs is specified in the Electrical Characteristics section of this data sheet. For the sake of this example, consider a buck converter output voltage of 3.3V with a 2.5A load. The buck converter dropout voltage at 2.5A is approximately 700mV. Therefore, the minimum buck converter input voltage, $V_{MIN}$, required to maintain regulation is 3.3V + 700mV = 4V. Finally, assuming an efficiency of 80%, the minimum required input hold-up capacitance on the priority channel can be calculated as:

$$C_{IN} = \frac{2(3.3V)(2.5A)(60\mu s)}{0.80[(10V)^2 - (4V)^2]}$$

$$= 14.7\frac{\mu s \bullet A}{V} = 14.7\mu F$$

Therefore, in this example a minimum capacitor value of 15µF or greater must be utilized on $V_{IN1}$ to maintain regulation of the buck converter output throughout the transition to the secondary channel. In practice, an additional guardband should be included to account for variations in component tolerances and delays.

### Soft-Start

The LTC3126 incorporates an internal soft-start circuit with a nominal duration of 7.5ms. The soft-start is implemented by a linearly increasing ramp of the error amplifier reference voltage during the soft-start duration. As a result, the duration of the soft-start period is largely unaffected by the size of the output capacitor or the output regulation voltage. Given the closed-loop nature of the soft-start implementation, the converter is able to respond to load transients that occur during the soft-start interval. The soft-start period is reset by thermal shutdown, when the buck converter is disabled via the ENA pin and when both inputs are in UVLO.

### $V_{REF}$ Output

The $V_{REF}$ output is a regulated, temperature stable 1.00V voltage reference. It is intended primarily to be used to establish the $V_{SET1}$ and $V_{SET2}$ pin voltages. However, it can also be used for other functions as long as the total current drawn from the pin is limited to 1mA or less. In addition to that restriction, there is also a maximum amount of capacitance that can be placed on the $V_{REF}$ pin in order to maintain suitable phase margin in the internal pin driver. The maximum recommended capacitance on the $V_{REF}$ pin is 470pF or less. If the $V_{REF}$ pin is not being used in the application (i.e., there is no resistor from $V_{REF}$ to GND) then the $V_{REF}$ pin should be connected to $V_{CC}$. The $V_{REF}$ pin cannot be left floating. The $V_{REF}$ pin is only powered when the part is enabled (ENA is high).

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### Buck Converter Switching Frequency

The LTC3126 buck converter utilizes fixed-frequency PWM to achieve low output ripple and low noise operation. The switching frequency can be set from 200kHz to 2.2MHz by appropriate selection of the $R_T$ resistor placed between the RT pin and ground. See the Quick Reference section for details on selecting the value for $R_T$.

Higher switching frequencies facilitate the use of smaller inductors as well as smaller input and output capacitors which results in a smaller solution size and reduced component height. However, higher switching frequencies also generally reduce conversion efficiency due to increased switching losses.

The on-time of the buck converter SW pin decreases as the step-down ratio from $V_{IN}$ to $V_{OUT}$ increases and as the switching frequency is increased. The minimum switch on-time, $t_{ON(MIN)}$, is the smallest duration on-time that the SW pin can generate. If the required on-time is shorter than the minimum on-time then the part will pulse skip to maintain regulation. Although regulation of the output will be maintained, pulse skipping results in lower frequency switching and increased output voltage ripple. In order to avoid pulse-skipping operation, the switching frequency should be selected to be less than $f_{SW(MAX)}$ as given by the following equation where $t_{ON(MIN)}$ is the minimum SW pin on time with a typical value of 60ns:

$$f_{SW(MAX)} = \frac{V_{OUT}}{V_{IN} \bullet t_{ON(MIN)}}$$

The SW minimum on-time is a function of load current and temperature as shown in the Typical Performance Characteristics section.

### Input Capacitors

To ensure proper functioning of the buck converter, minimize EMI and reduce input ripple, the $PV_{IN1}$ and $PV_{IN2}$ pins must each be connected to a low ESR bypass capacitor with a value of at least 4.7µF. Ceramic capacitors with X5R or X7R dielectric are recommended. Each bypass capacitor must be located as close as possible to the respective pin and should connect to the ground plane via the shortest route possible.

When powered through an inductive connection such as a long cable, the inductance of the power source and the input bypass capacitor form a High-Q resonant LC filter. In such applications, hot-plugging into a powered source can lead to a significant voltage overshoot, even up to twice the nominal input source voltage. Care must be taken in such situations to ensure that the absolute maximum input voltage rating of the LTC3126 is not violated. See Linear Technology Application Note 88 for solutions to increase damping in the input filter and minimize this voltage overshoot.

The $V_{IN1}$ and $V_{IN2}$ pins provide power to the $V_{CC}$ regulator and other internal circuitry. Each of these pins should be connected to a 0.1µF bypass capacitor located as close to the pin as possible.

### Buck Output Capacitor

A low ESR capacitor should be utilized at the output of the buck converter in order to minimize output voltage ripple. For most applications, a ceramic capacitor with X5R or X7R dielectric is the optimal choice. There is also a minimum required output capacitor value as specified in the Quick Reference section. The crossover frequency of the voltage control loop increases with lower output capacitance and therefore a minimum capacitance value is required to limit the bandwidth and ensure stability of the voltage feedback loop. Given that the loop gain is dependent on the voltage divider ratio, the minimum required output capacitor is a function of the output voltage as well. At lower output voltages, the loop gain is higher and a larger output capacitor is required to maintain a fixed loop crossover frequency. The larger recommended output capacitance at low output voltages also helps to reduce the magnitude of voltage steps on load transients in proportion to the reduced output voltage rail in order to maintain a constant percentage deviation.

Increasing the value of the buck converter output capacitor will decrease the bandwidth of the feedback loop. If the output capacitor gets too large, the crossover frequency may decrease too far below the compensation zero leading to degraded phase margin and underdamped transient response. In such cases, the phase margin and transient performance can be improved by increasing the size

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of the feedforward capacitor in parallel with the upper resistor divider resistor to restore the full bandwidth of the feedback loop.

### Feedforward Resistor

In applications where there is a long connection between the feedback resistor divider and the point at which the output voltage is sensed, it is recommended that a 10k feedforward resistor ($R_{FF}$) be added in series with the feedforward capacitor as shown in Figure 7 below. The feedforward resistor prevents high frequency noise on the $V_{OUT}$ trace from coupling into the sensitive FB node. The addition of a 10k feedforward resistor will have little impact on the frequency response of the control loop since the divider pole location is dominated by the values of resistors $R_{TOP}$ and $R_{BOT}$.

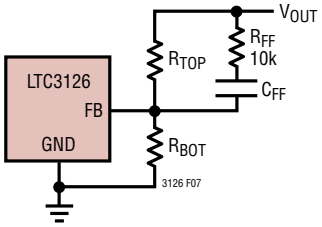


**Figure 7. Feedforward Resistor ($R_{FF}$) for Improved Noise Robustness**

### Inductor Selection

The choice of inductor value influences both the efficiency and the magnitude of the output voltage ripple. Larger inductance values will reduce inductor current ripple and will therefore lead to lower output voltage ripple. For a fixed DC resistance, a larger value inductor will yield higher efficiency via reduced RMS and core losses. However, a larger inductor within a given inductor family will generally have a greater series resistance, thereby counteracting this efficiency advantage. The peak-to-peak current ripple, $\Delta I_L$, given by the following equation will be largest at the highest input voltage experienced in the application.

$$\Delta I_L = \frac{V_{OUT}}{f_{SW} \bullet L}\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

A reasonable choice for ripple current is $\Delta I_L$ = 1A which represents 33% of the minimum current limit. The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current in order to prevent core saturation and loss of efficiency during operation. To optimize efficiency the inductor should have a low DC resistance. As a general guideline, the inductor resistance (ESR) should be approximately equal to the low side switch resistance (70mΩ) or less.

High values of inductor ripple current will reduce the output current capability of the converter since higher ripple increases the peak switch current and will therefore trip the current limit at a lighter load current. The maximum output current is equal to the current limit minus half the peak-to-peak ripple current as shown in the following equation where $I_{LIMIT}$ is the threshold of the high side switch current limit:

$$I_{OUT(MAX)} = I_{LIMIT} - \frac{\Delta I_L}{2}$$

In addition, there is a minimum inductor value required to maintain stability of the current loop as determined by the fixed internal slope compensation. Specifically, if the buck converter is going to be utilized at duty cycles over 50%, the inductance value must be at least equal to $L_{MIN}$ as given by the following equation:

$$L_{MIN} = \frac{MHz}{f_{SW}} \bullet \frac{V_{OUT}}{2V}\ \mu H$$

To ensure sufficient slope compensation if the external synchronization feature is being used, the inductor must be sized for the lowest possible switching frequency the part will experience which is determined by the internal oscillator frequency.

### PGOOD Output

The open-drain PGOOD output is driven low whenever FB is more than +9.8%/–8.7% (typical) from the FB reference voltage. The PGOOD output is also driven low whenever the buck converter is disabled. The maximum voltage that can be applied to the PGOOD output is 5.5V. The PGOOD comparator has a deglitching delay of approximately 200µs.

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### $V_{CC}$ Regulators and Bootstrapping with $EXTV_{CC}$

The $V_{CC}$ rail powers the internal control circuitry and power device gate drivers of the LTC3126. Two internal low dropout linear regulators provide the ability to generate this rail from either $V_{IN1}$ or $V_{IN2}$. When the IC is disabled (ENA low) the $V_{CC}$ rail is powered by the higher voltage input, $V_{IN1}$ or $V_{IN2}$, regardless of the state of the $V_{SET1}$, $V_{SET2}$ and DIODE pins. When the IC is enabled, the input voltage comparators on the $V_{SET1}$ and $V_{SET2}$ pins become active and the $V_{CC}$ rail will be powered by the active channel. In ideal diode mode (DIODE high) the active channel is the valid input with the higher voltage. In priority mode (DIODE low) the active channel is $V_{IN1}$ if $V_{IN1}$ is valid or $V_{IN2}$ otherwise (assuming it is valid). If both $V_{IN1}$ and $V_{IN2}$ are in UVLO then the higher voltage input will be utilized to power the $V_{CC}$ rail.

A third linear regulator allows the $V_{CC}$ rail to be powered via the $EXTV_{CC}$ pin which can be connected to the buck converter output or an auxiliary rail with a voltage above 3.15V. When operating at high input voltages, the losses in the $V_{CC}$ regulator powered from the input voltage can become a significant factor in conversion efficiency and can even become a substantial source of power dissipation. A significant performance improvement can be obtained by connecting the $EXTV_{CC}$ input to the buck converter output so that the gate drive current is provided through the high efficiency buck converter rather than the less efficient linear regulator. This is of particular benefit at higher input voltages, lower output voltages and higher switching frequencies. The $EXTV_{CC}$ pin is only utilized to power the $V_{CC}$ rail when the buck converter is operating.

### Thermal Considerations

The LTC3126 is designed to operate continuously up to its full rated 2.5A output current. However, when operating at high current levels there will be significant heat generated within the IC. In addition, in many applications the $V_{CC}$ regulator is operated with large input-to-output voltage differential resulting in significant levels of power dissipation in its pass element which can add significantly to the total power dissipated within the IC. To ensure full output current capability and optimal efficiency, careful consideration must be given to the thermal environment of the IC. This is even more important in applications that function over an extended ambient temperature range.

Specifically, the exposed die attach pad of both the QFN and TSSOP packages must be soldered to the PC board and the PC board should be designed to maximize the conduction of heat out of the IC package. This can be accomplished by utilizing multiple vias from the die attach pad connection to other PCB layers containing a large area of exposed copper.

If the die temperature exceeds approximately 170°C, the IC will enter overtemperature shutdown and all switching will be inhibited. The part will remain disabled until the die cools by approximately 10°C. The soft-start circuit is re-initialized in overtemperature shutdown to provide a smooth recovery when the fault condition is removed.

### PCB Layout Guidelines

The LTC3126 buck converter switches large currents at high frequencies. Special attention must be paid to the PC board layout to ensure a stable, noise-free and efficient application circuit. Figures 6 and 7 show representative PC board layouts for each package option to outline some of the primary considerations. A few key guidelines are listed below.

1. The parasitic inductance and resistance of all circulating high current paths should be minimized. This can be accomplished by keeping the routes to the inductor, output capacitor and $PV_{IN1/2}$ bypass capacitors as short and as wide as possible. Capacitor ground connections should via down to the ground plane by way of the shortest route possible. The bypass capacitors on $PV_{IN1}$, $PV_{IN2}$ and $V_{CC}$ should be placed as close to the IC as possible and should have the shortest possible return paths to ground.
2. The exposed pad in both packages provides one of the primary paths for heat generated within the package. The IC must be soldered down to the backpad and the backpad area should be filled with vias connecting it to the ground plane.

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3. There should be an uninterrupted ground plane under the entire converter in order to minimize the cross-sectional area of the high frequency current loops. This minimizes EMI and reduces the inductive drops in these loops thereby minimizing SW pin overshoot and ringing.

4. Connections to the $PV_{IN1}$, $PV_{IN2}$ and SW pins should be made as wide as possible to reduce the series impedance. This will improve efficiency and reduce the thermal resistance.

5. To prevent large circulating currents in the ground plane from disrupting operation of the part, all small-signal grounds should either return directly to the small-signal ground pin (GND) or via down to the ground plane close to the GND pin and not near the power stage components. This includes the ground connections for the $R_T$ resistor, the FB resistor divider and the $V_{SET1}$ and $V_{SET2}$ resistor dividers.

6. Keep the routes connecting to the high impedance noise sensitive inputs (FB, RT, $V_{SET1}$, $V_{SET2}$) as short as possible to minimize noise pickup.

7. The BST1/BST2 pins transition at the switching frequency to the full input voltage. To minimize radiated noise and coupling, keep the routes connecting to the boost capacitors as short as possible and keep these routes away from all sensitive circuitry and pins (FB, RT, $V_{SET1}$, $V_{SET2}$).

8. The connection to the $V_{IN1}$ pin (Pin 25) should be separate from the connection to the $PV_{IN1}$ (Pin 24) and should have a separate 0.1µF bypass capacitor. This will prevent noise from the $PV_{IN1}$ trace from being coupled into the sensitive $V_{IN1}$ pin.

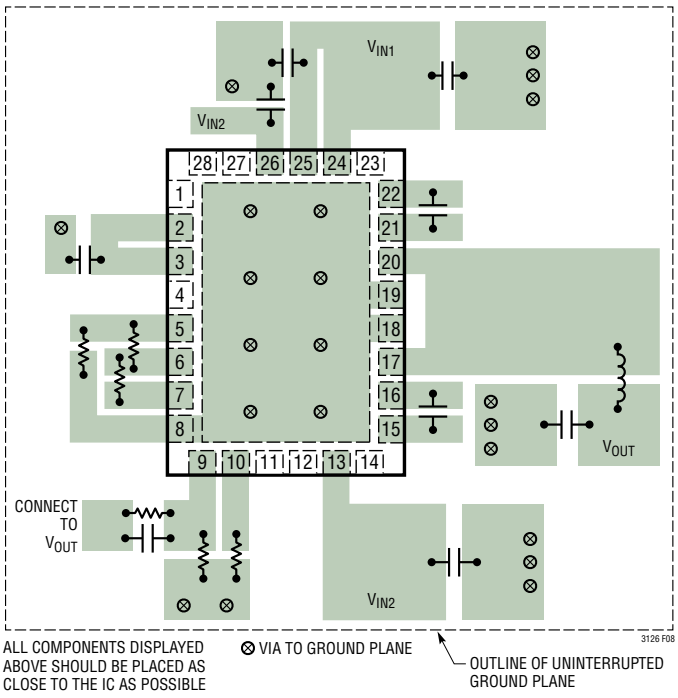



**Figure 8. Recommended PC Board Layout for QFN Package**

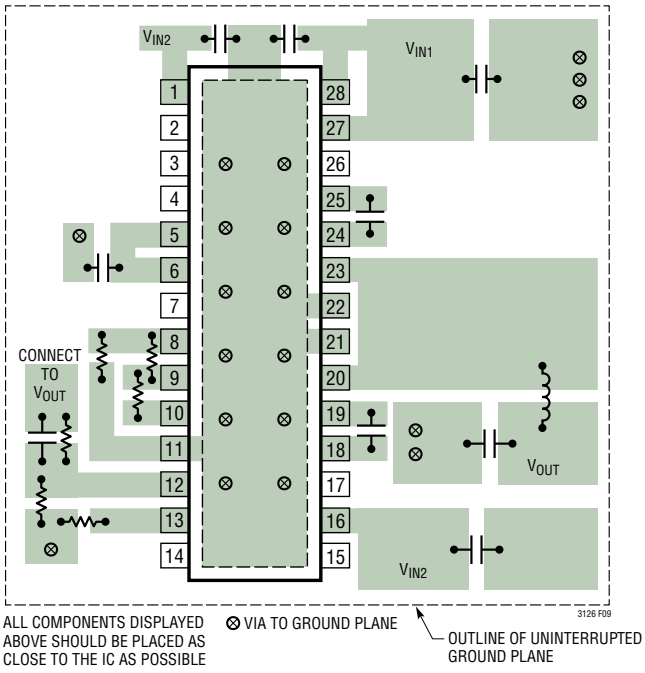
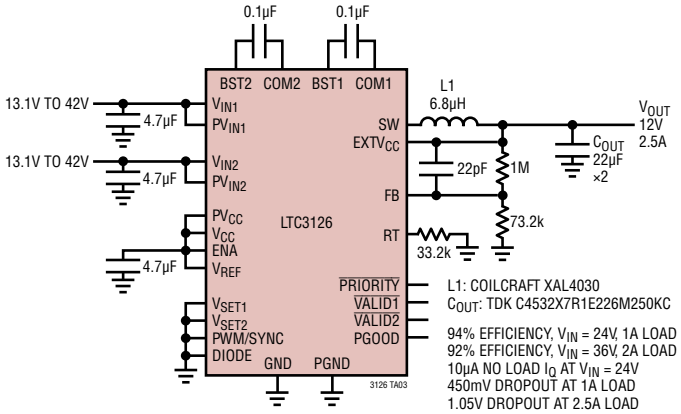


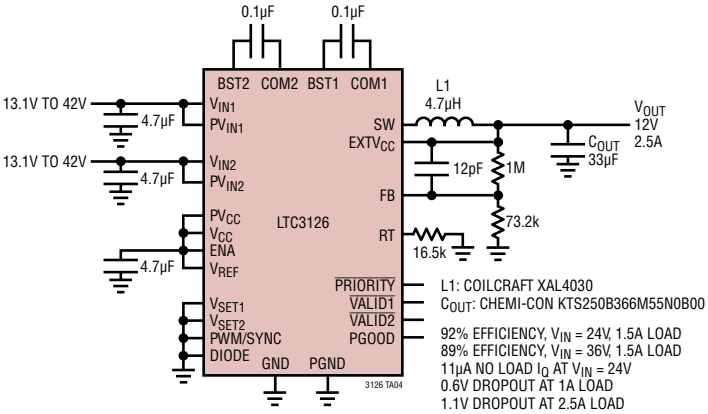

**Figure 9. Recommended PC Board Layout for TSSOP Package**

# TYPICAL APPLICATIONS

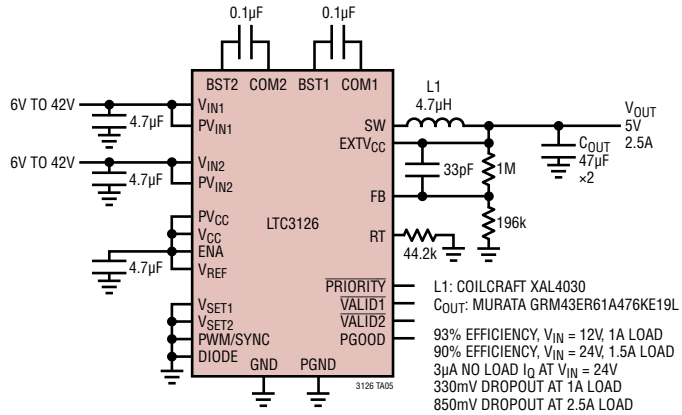
### 12V, 1MHz Step-Down Converter with Dual Inputs



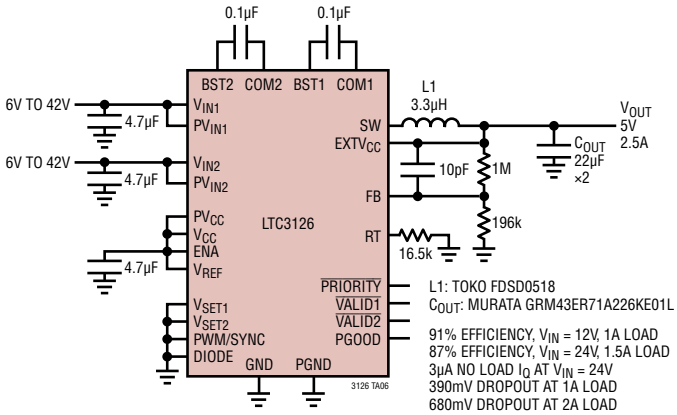

### 12V, 2MHz Step-Down Converter with Dual Inputs




### 5V, 750kHz Step-Down Converter with Dual Inputs

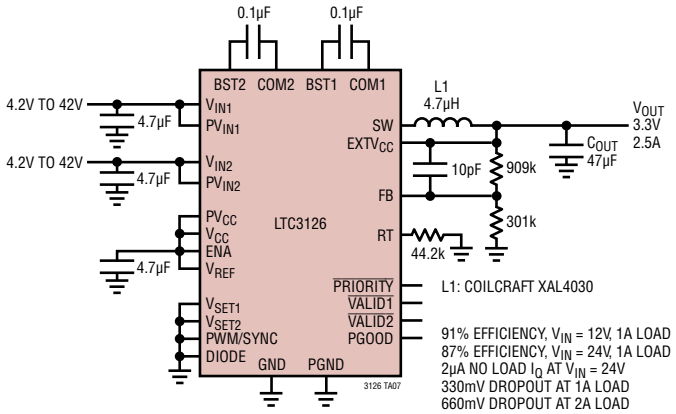



### 5V, 2MHz Step-Down Converter with Dual Inputs

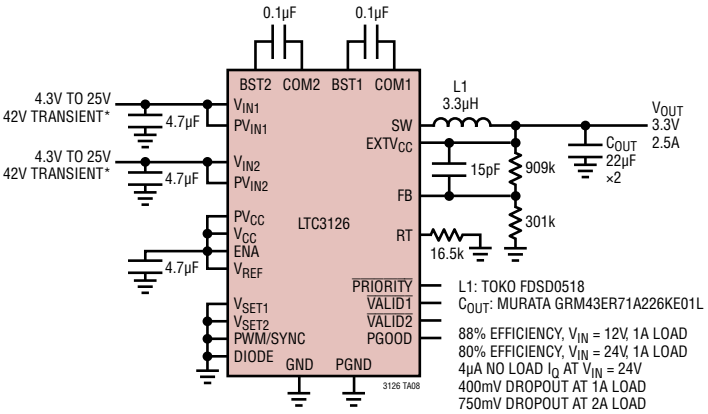


# TYPICAL APPLICATIONS

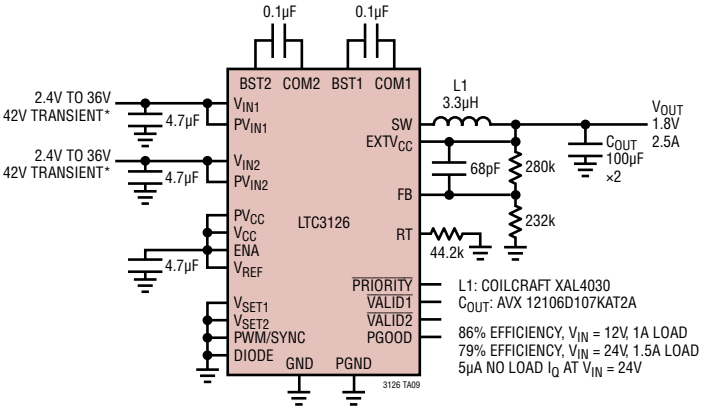
### 3.3V, 750kHz Step-Down Converter with Dual Inputs



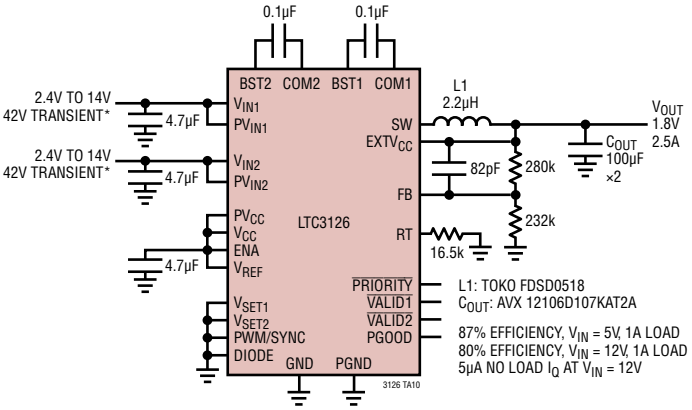

### 3.3V, 2MHz Step-Down Converter with Dual Inputs




### 1.8V, 750kHz Step-Down Converter with Dual Inputs



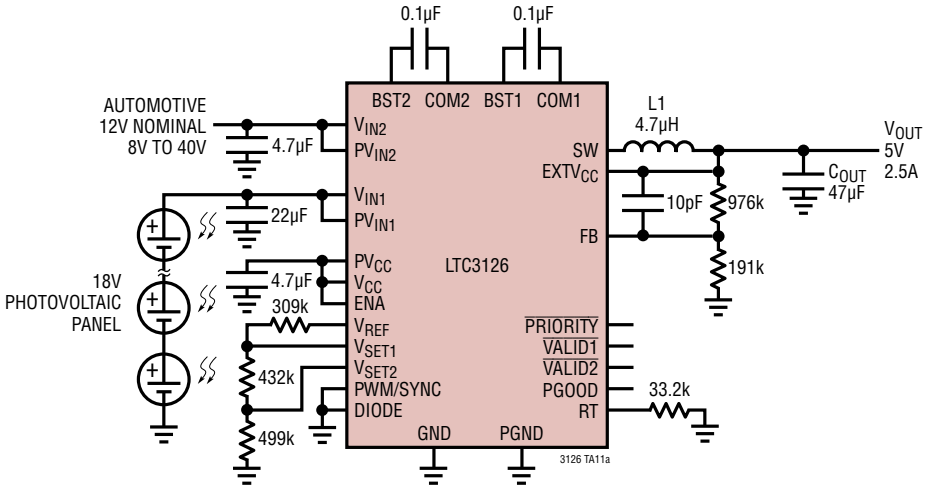

### 1.8V, 2MHz Step-Down Converter with Dual Inputs




*The step-down converter can operate over the specified input voltage range without any pulse skipping for loads from 250mA to 2.5A. However, in all applications, the converter can operate from an input voltage as high as 42V, but pulse skipping may occur if operated above the specified voltage range. Pulse skipping is not detrimental to the IC, but can result in significant output voltage ripple and is therefore generally avoided while in nominal operating conditions.

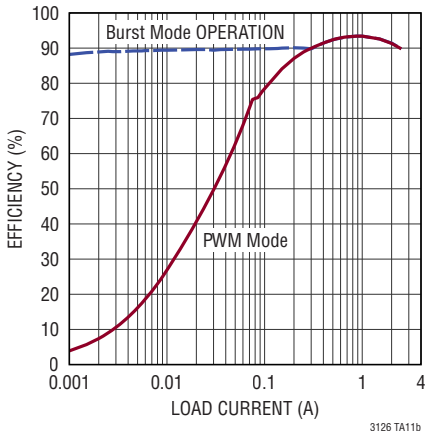
# TYPICAL APPLICATIONS

### Automotive and Photovoltaic Powered 5V USB Supply

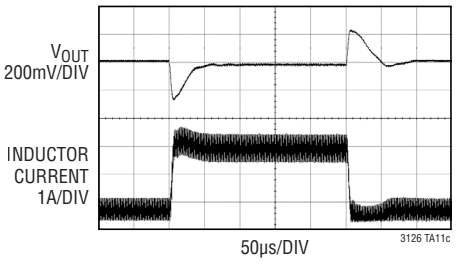



$f_{SW}$ = 1MHz
$V_{IN1}$ UVLO THRESHOLD = 15V
$V_{IN2}$ UVLO THRESHOLD = 8V
L1: COILCRAFT XAL4030

### Efficiency, $V_{IN}$ = 12V

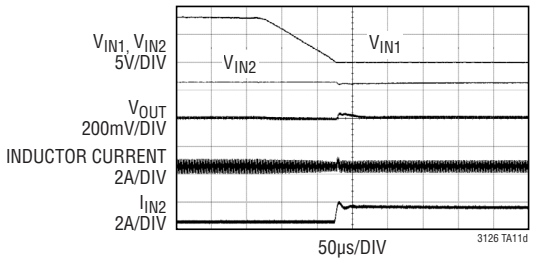



### Load Step, 250mA to 2.5A




$V_{IN}$ = 18V

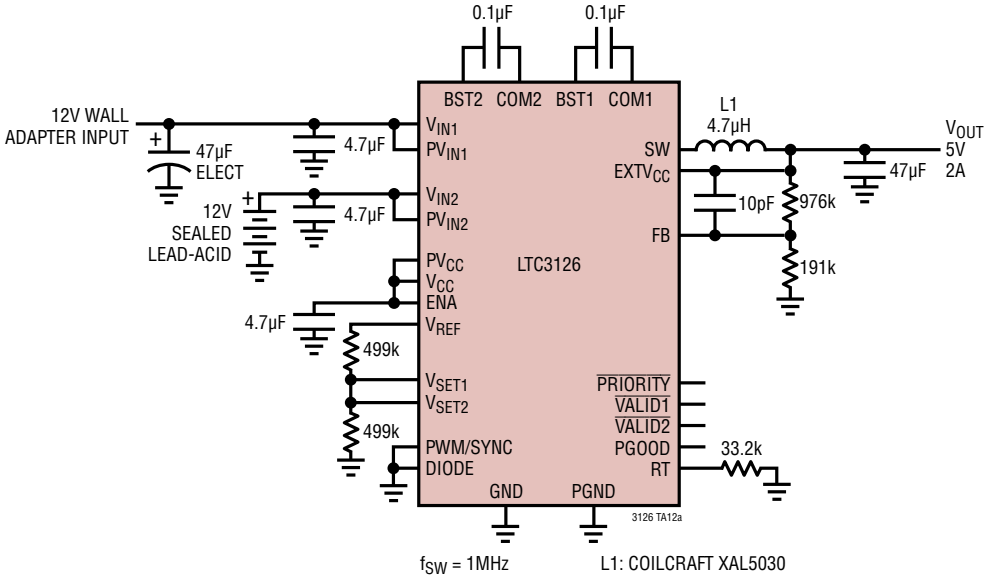
### Photovoltaic Panel Disconnect (Switch to Automotive Input)



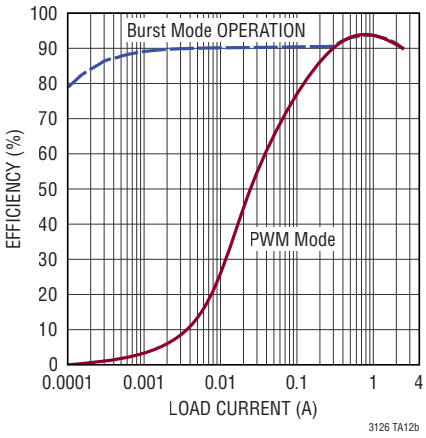

$V_{IN1}$ = 18V
$V_{IN2}$ = 12.8V
2.5A LOAD

# TYPICAL APPLICATIONS

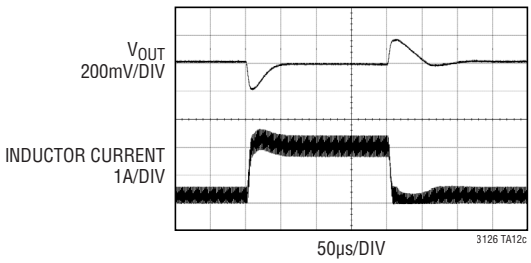
### 5V, 2A Supply from Wall Adapter and Lead-Acid Backup Battery




### Efficiency, $V_{IN}$ = 12V

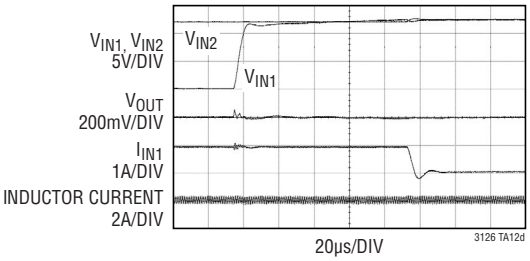



### Load Step, 200mA to 2A



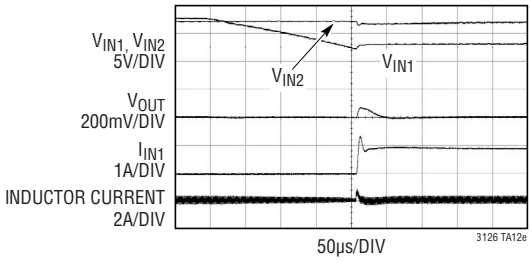

$V_{IN1}$ = 12V

### Wall Adapter Plug-In Transient




2A LOAD

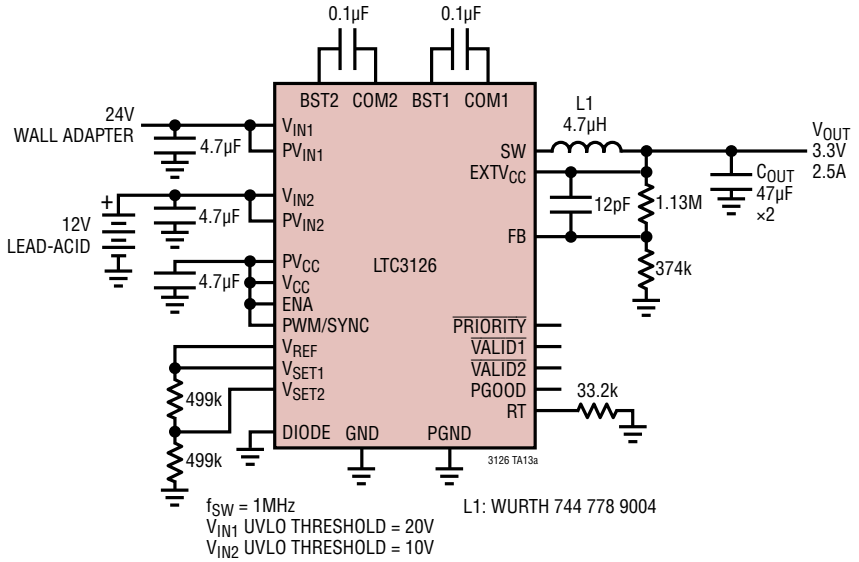
### Wall Adapter Disconnect Transient



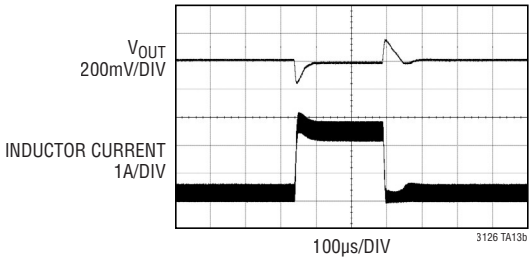

2A LOAD

# TYPICAL APPLICATIONS

### 3.3V/2.5A Supply from 24V Wall Adapter and Lead-Acid Battery

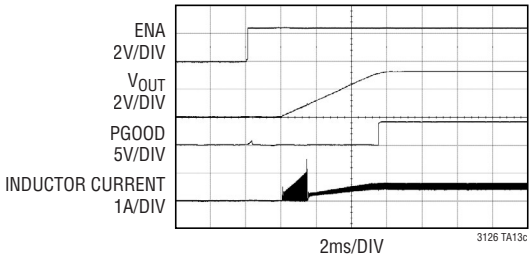



### Load Step, 250mA to 2.5A

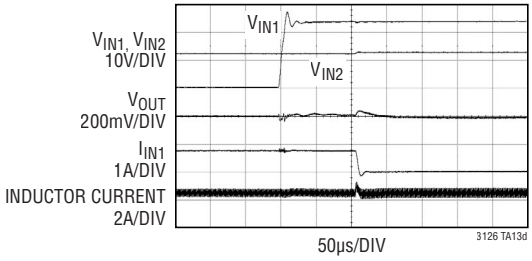



$V_{IN}$ = 24V

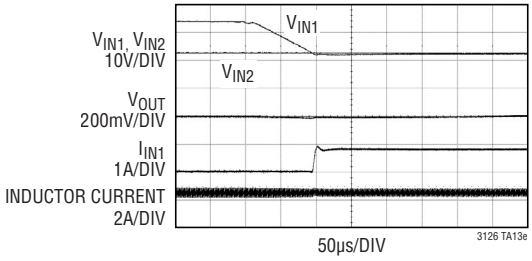
### Soft-Start




### Wall Adapter Plug-In Transient



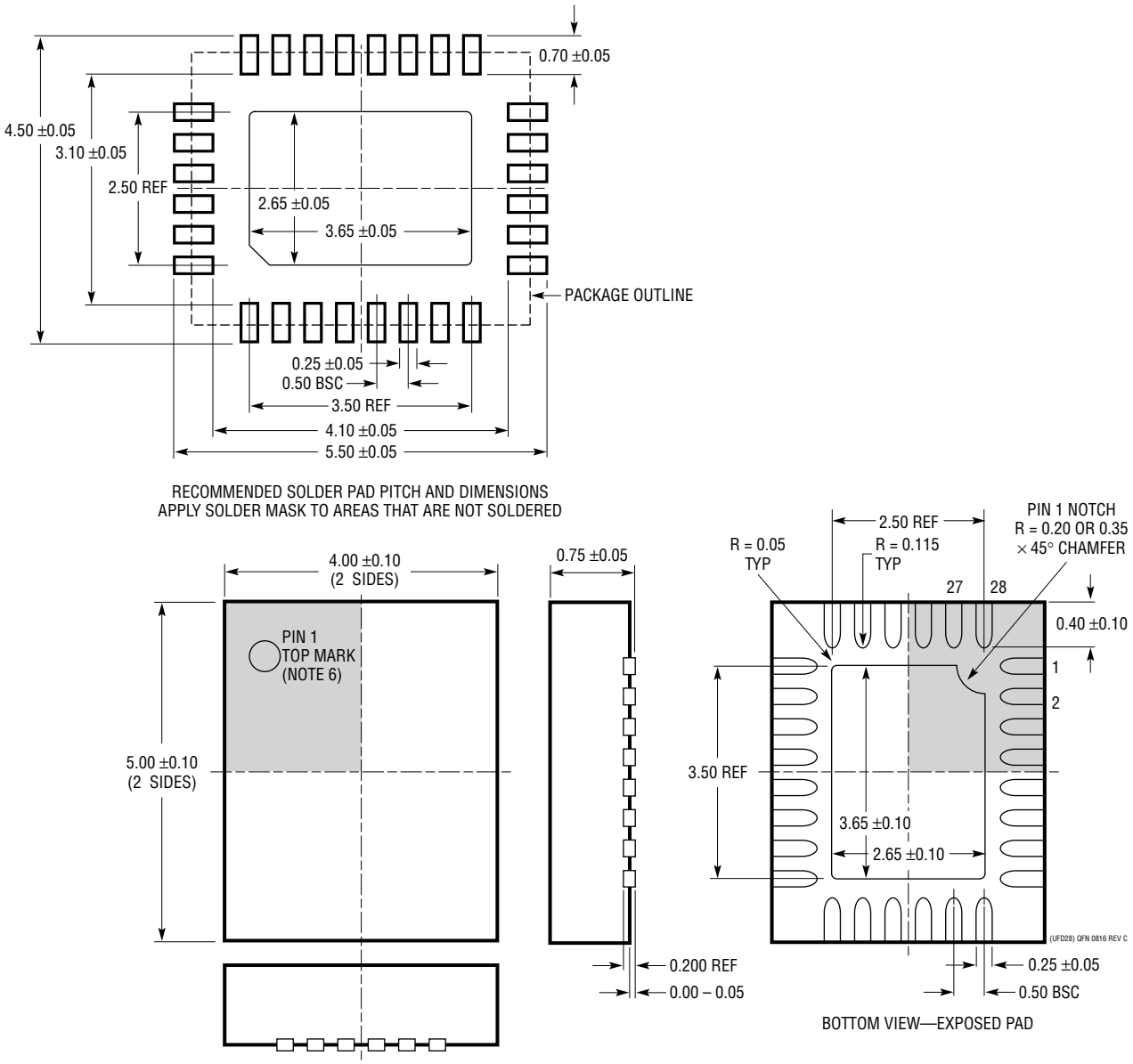

### Wall Adapter Disconnect Transient



# PACKAGE DESCRIPTION

**Please refer to http://www.linear.com/product/LTC3126#packaging for the most recent package drawings.**

**UFD Package**
**28-Lead Plastic QFN (4mm × 5mm)**
(Reference LTC DWG # 05-08-1712 Rev C)

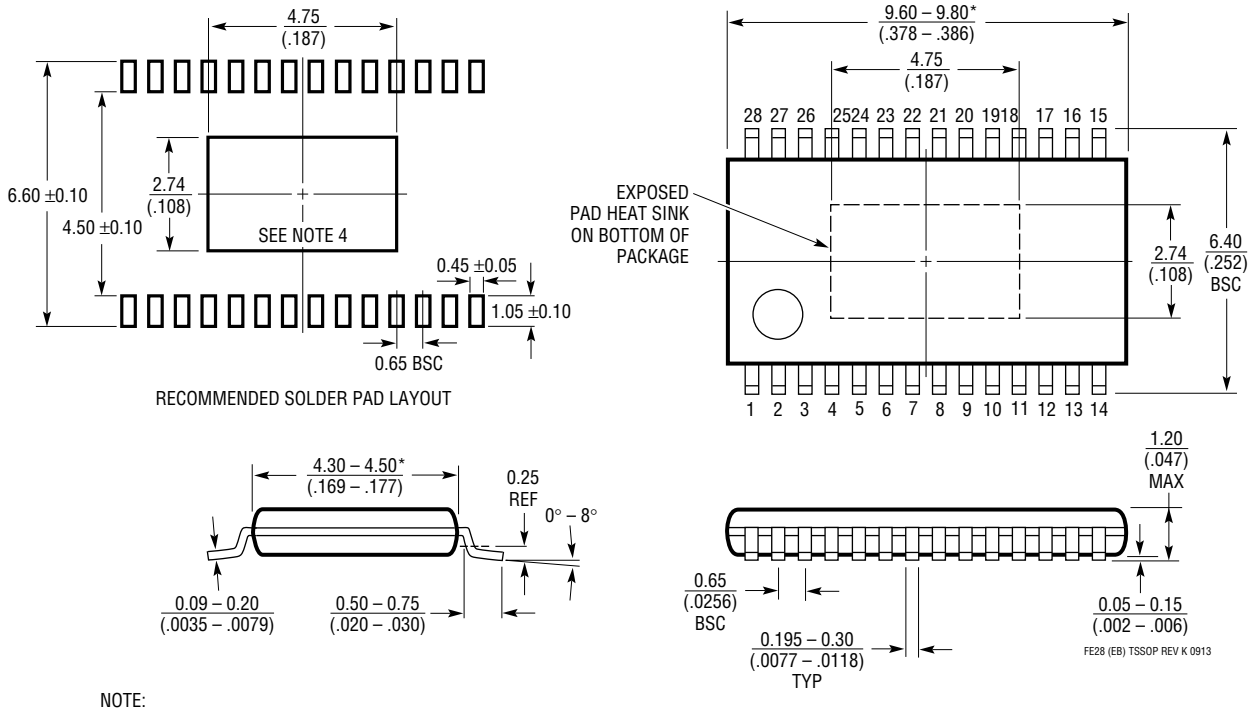



NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGHD-3).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

# PACKAGE DESCRIPTION

**Please refer to http://www.linear.com/product/LTC3126#packaging for the most recent package drawings.**

**FE Package**
**28-Lead Plastic TSSOP (4.4mm)**
(Reference LTC DWG # 05-08-1663 Rev K)
**Exposed Pad Variation EB**

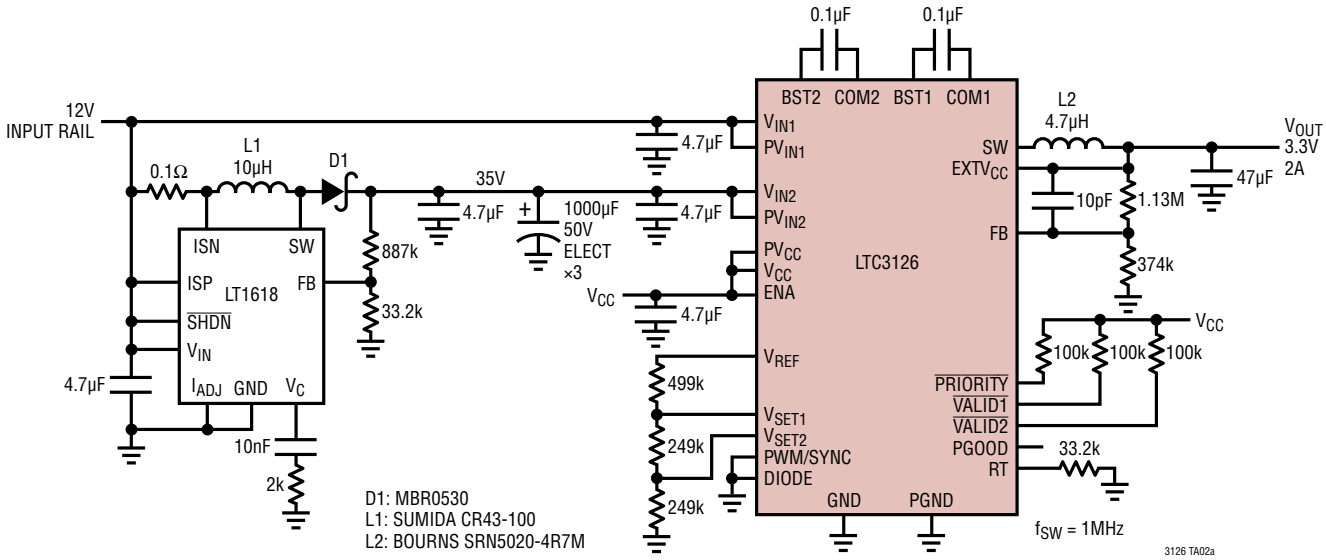



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN MILLIMETERS (INCHES)
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT

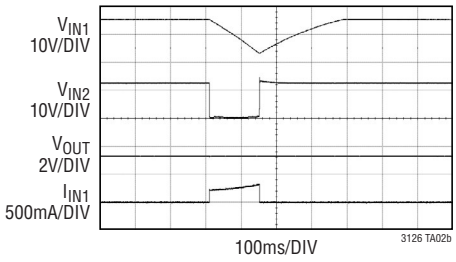
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

## TYPICAL APPLICATION

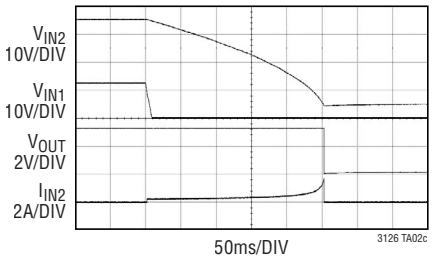
**3.3V Supply with 200ms Transient Ride-Through Capability**



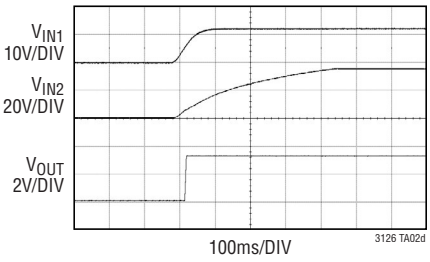

**Transient Ride-Through**




**$V_{OUT}$ Hold-Up with Loss of Input Supply**




**Power-Up Waveforms**




## RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LT®8609 | 42V, 2A (3A Peak) 2MHz Synchronous Step-Down Regulator with $I_Q$ = 2.5µA | $V_{IN}$: 3V to 42V, $I_Q$ = 2.5µA, $I_{SD}$ = 1µA, MSOP-10E Package |
| LTC3118 | 18V, 2A Buck-Boost DC/DC Converter with Low Loss Dual Input PowerPath | $V_{IN}$: 2.2V to 18V, $I_Q$ = 50µA, $I_{SD}$ = 2µA, TSSOP-28, QFN-24 Packages |
| LT8610 | 42V, 2.5A Synchronous Step-Down Regulator | $V_{IN}$: 3.4V to 42V, $I_Q$ = 2.5µA, $I_{SD}$ = 1µA, MSOP-16 Package |
| LTC4417 | Prioritized PowerPath Controller | Controller for External P-Channel MOSFETs, Three Channels, $V_{IN}$: 2.5V to 36V, $I_Q$ = 28µA, SSOP-24, QFN-24 Packages |
| LTC3114-1 | 40V, 1A Synchronous 4-Switch Monolithic Buck-Boost DC/DC Converter | $V_{IN}$: 2.2V to 40V, $V_{OUT}$: 2.7V to 40V, $I_Q$ = 30µA, $I_{SD}$ = 3µA, TSSOP-16, DFN-16 Packages |
| LTC3115-1 | 40V, 2A Synchronous 4-Switch Monolithic Buck-Boost DC/DC Converter | $V_{IN}$: 2.7V to 40V, $V_{OUT}$: 2.7V to 40V, $I_Q$ = 30µA, $I_{SD}$ = 3µA, TSSOP-20, DFN-16 Packages |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