SAM D20 Family

SAM D20 Family Silicon Errata and Data Sheet Clarification

SAM D20 Family

The SAM D20 family of devices that you have received conform functionally to the current Device Data Sheet (DS60001504B), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1 and Table 2.

The errata described in this document will be addressed in future revisions of the SAM D20 family silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Data Sheet clarifications and corrections (if applicable) are located in Data Sheet Clarifications, following the discussion of silicon issues.

Table 1. SAM D20 Family Silicon Device Identification (Device Variant A)

Device Variant	Device ID (DID[31:0])	Revision(DID.Revision[3:0])				
		B	C	D	E	G
SAMD20J16A	0x1000xx02	0x1	0x2	0x3	0x4	N/A
SAMD20J15A	0x1000xx03					
SAMD20J14A	0x1000xx04					
SAMD20G16A	0x1000xx07					
SAMD20G15A	0x1000xx08					
SAMD20G14A	0x1000xx09					
SAMD20E16A	0x1000xx0C					
SAMD20E15A	0x1000xx0D					
SAMD20E14A	0x1000xx0E					
SAMD20J18A	0x1000xx00					
SAMD20J17A	0x1000xx01					
SAMD20G18A	0x1000xx05					
SAMD20G17A	0x1000xx06					
SAMD20E18A	0x1000xx0A					
SAMD20E17A	0x1000xx0B					
SAMD20G18A-U	0x1000xx10					
SAMD20G17A-U	0x1000xx11					

Table 2. SAM D20 Family Silicon Device Identification (Device Variant B)

Device Variant	Device ID (DID[31:0])	Revision(DID.Revision[3:0])				
		B	C	D	E	G
SAMD20E14B	0x1000xx0E	N/A	N/A	N/A	N/A	0x6
SAMD20E15B	0x1000xx0D					
SAMD20E16B	0x1000xx0C					
SAMD20G14B	0x1000xx09					
SAMD20G15B	0x1000xx08					
SAMD20G16B	0x1000xx07					
SAMD20J14B	0x1000xx04					
SAMD20J15B	0x1000xx03					
SAMD20J16B	0x1000xx02					

Note: Refer to the “Device Service Unit” chapter in the current Device Data Sheet (DS60001504B) for detailed information on Device Identification and Revision IDs for your specific device.

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1. SAM D20 Errata Issues

The device variant (last letter of the ordering number) is independent of the die revision (DSU.DID.REVISION): The device variant denotes functional differences, whereas the die revision marks evolution of the die.

1.1 32.768 kHz Crystal Oscillator (XOSC32K)

1.1.1 Amplitude Control

The automatic amplitude control of the XOSC32K does not work.

Workaround
Use the XOSC32K with Automatic Amplitude control disabled (XOSC32K.AAMPEN = 0).

Affected Silicon Revisions

B	C	D	E	G		
X	X	X	X	X		

1.2 48 MHz Digital Frequency-Locked Loop (DFLL48M)

1.2.1 DFLL Clock

The DFLL clock must be requested before being configured otherwise a write access to a DFLL register can freeze the device.

Workaround
Write a zero to the DFLL ONDEMAND bit in the DFLLCTRL register before configuring the DFLL module.

Affected Silicon Revisions

B	C	D	E	G		
X	X	X	X	X		

1.2.2 Calibration Bits

Changing the DFLLVAL.FINE calibration bits of the DFLL48M Digital Frequency Locked Loop might result in a short output frequency overshoot. This might occur both in Open Loop mode while writing DFLLVAL.FINE by software and Closed Loop mode when the DFLL adjusts its output frequency.

Workaround
When using DFLL48M in Open Loop mode, ensure that DFLL48M is not used by any other module while DFLLVAL.FINE is written.

When using DFLL48M in Closed Loop mode, ensure that DFLLCTRL.STABLE is written to '1'. The DFLL clock should not be used by any modules until the DFLL locks are set.

If the application requires On-the-Fly DFLL calibration (temperature/VCC drift compensation), the firmware should perform either periodically or when the DFLL48M frequency differ too much from the target frequency (indicated by DFLLVAL.DIFF), the following:

- Switch system clock/module clocks to different clock than DFLL48M
- Reinitiate a DFLL48M closed loop lock sequence by disabling and re-enabling the DFLL48M
- Wait for fine lock (PCLKSR.DFLLLCKF set to 1)
- Switch back system clock/module clocks to the DFLL48M

Better accuracy is achieved using a high multiplier for the DFLL48M, using a scaled down or slow clock as reference. A multiplier of 6 will have a theoretical worst case frequency deviation from the reference clock of +/- 8.33%. A multiplier of 500 will have a theoretical worst case frequency deviation from the reference clock of +/- 0.1%.

Affected Silicon Revisions

B	C	D	E	G		
X	X					

1.2.3 Firmware Writes

If the firmware writes to the DFLLMUL.MUL register in the same cycle as the Closed Loop mode tries to update it, the fine calibration will first be reset to midpoint and then incremented/decremented by the Closed Loop mode. The coarse calibration will be performed with the updated fine value. If this happens before the dfll have gotten a lock, the new fine calibration value can be between 128-DFLLMUL.FSTEP and 128+DFLLMUL.FSTEP, which could give smaller calibration range for the fine calibration.

Workaround
Always wait until the DFLL48M has locked before writing the DFLLMUL.MUL register.

Affected Silicon Revisions

B	C	D	E	G		
X	X					

1.2.4 Locking Sequence

If the DFLL48M reaches the maximum or minimum COARSE or FINE calibration values during the locking sequence, an out of bounds interrupt will be generated. These interrupts will be generated even if the final calibration values at DFLL48M lock are not at maximum or minimum, and therefore might be false out-of-bounds interrupts.

Workaround
Ensure that the lockbits, DFLLLCKC and DFLLLCKF, in the SYSCTRL Interrupt Flag Status and Clear register (INTFLAG) are set before enabling the DFLLOOB interrupt.

Affected Silicon Revisions

B	C	D	E	G		
X	X	X	X	X		

1.3 Analog-to-Digital Converter (ADC)

1.3.1 ADC Samples

The automatic right shift of the result when accumulating/averaging ADC samples does not work.

Workaround
To accumulate or average more than 16 samples, users must add the number of automatic right shifts to AVGCTRL.ADJRES to perform the correct number of right shifts. For example, for averaging 128 samples, AVGCTRL.ADJRES must be written to 7 instead of 4, as the automatic right shift of 3 is not done. For oversampling to 16 bits resolution, AVGCTRL.ADJRES must be written to 4 instead of 0 as the automatic right shift of 4 is not done.

The maximum number of right shifts that can be done using ADJRES is 7. This means that when averaging more than 128 samples, the result will be more than 12 bits, and the additional right shifts to get the result down to 12 bits must be done by firmware.

Affected Silicon Revisions

B	C	D	E	G		
X	X					

1.3.2 Bus Clock Frequency

When the ADC bus clock frequency (CLK_ADC_APB) is smaller than the ADC asynchronous clock frequency (GCLK_ADC), issuing an ADC SWRST (ADC.CTRLA.SWRST) will lock up the ADC with the SYNCBUSY (ADC.STATUS.SYNCBUSY) flag always set.

Workaround
Do not issue an ADC SWRST if the ADC bus clock frequency (CLK_ADC_APB) is smaller than the ADC asynchronous clock frequency(GCLK_ADC).

Affected Silicon Revisions

B	C	D	E	G		
X	X					

1.4 Brown-out Detection (BOD)

1.4.1 BOD33 HYST Bit

The BOD33 HYST bit is not updated from NVM user row at power on. The reset value of this bit is zero.

Workaround
None.

Affected Silicon Revisions

B	C	D	E	G		
X	X					

1.4.2 BOD12 HYST Bit

The BOD12 HYST bit is not updated from NVM user row at power on. The reset value of this bit is zero.

Workaround
None.

Affected Silicon Revisions

B	C	D	E	G		
X	X					

1.5 Device

1.5.1 Maximum Toggle Frequency

Maximum toggle frequency on all pins in worst case operating condition is 8 MHz. This affects all operations on the pins, including serial communications.

Workaround
None.

Affected Silicon Revisions

B	C	D	E	G		
X	X					

1.5.2 APB Clock

If APB clock is stopped and GCLK clock is running, APB read access to read-synchronized registers will freeze the system. The CPU and the DAP AHB-AP are stalled, as a consequence debug operation is impossible.

Workaround
Do not make read access to read-synchronized registers when APB clock is stopped and GCLK is running. To recover from this situation, power cycle the device or reset the device using the $\overline{\text{RESET}}$ pin.

Affected Silicon Revisions

B	C	D	E	G		
X	X	X	X	X		

1.5.3 VDDIN

When V_{DDIN} is lower than the POR threshold during power rise or fall, an internal pull-up resistor is enabled on pins with PTC functionality (see PORT Function Multiplexing). This behavior will be present even if the PTC functionality is not enabled on the pin. The POR level is defined in the “Power-On Reset (POR) Characteristics” chapter in the device data sheet.

Workaround
Use a pin without PTC functionality if the pull-up could damage your application during power up.

Affected Silicon Revisions

B	C	D	E	G		
X	X	X				

1.5.4 Missing Bit Groups

The DFLLVAL.COARSE, DFLLVAL.FINE, DFLLMUL.CSTEP and DFLLMUL.FSTEP bit groups are not correctly located in the register map. DFLLVAL.COARSE has only 5 bits and located in DFLLVAL[12..8]. DFLLVAL.FINE has only 8 bits and located in DFLLVAL[7:0]. DFLLMUL.CSTEP has only 5 bits and located in DFLLMUL[28:24]. DFLLMUL.FSTEP has only 8 bits and located in DFLLMUL[23:16].

Workaround
DFLLVAL.COARSE, DFLLVAL.FINE, DFLLMUL.CSTEP and DFLLMUL.FSTEP should not be used if code compatibility is required with future device revisions.

Affected Silicon Revisions

B	C	D	E	G		
X	X					

1.5.5 Standby Mode

With default bit and register settings, the device does not work as specified in Standby mode if load current exceeds 100 µA.

Workaround
Set the FORCELDO bit in the VREG register.

Affected Silicon Revisions

B	C	D	E	G		
X	X					

1.5.6 Temperature Sensor

The temperature sensor is not accurate. No value is written into the Temperature Log row during production test.

Workaround
None

Affected Silicon Revisions

B	C	D	E	G		
X	X					

1.5.7 External XOSC32K State

If the external XOSC32K is broken, neither the external pin RST nor the GCLK software reset can reset the GCLK generators using XOSC32K as source clock.

Workaround
Do a power cycle to reset the GCLK generators after an external XOSC32K failure.

Affected Silicon Revisions

B	C	D	E	G		
X	X	X	X	X		

1.5.8 Voltage Regulator

The voltage regulator in Low-Power mode is not functional at temperature above 85°C.

Workaround
Enable normal mode on the voltage regulator in Standby Sleep mode.

Example code:

```
// Set the voltage regulator in normal mode configuration in standby sleep mode
SYSCTRL->VREG.bit.RUNSTDBY = 1;
```

Affected Silicon Revisions

B	C	D	E	G		
		X	X			

1.5.9 Standby Sleep Mode

Digital pin outputs from Timer/Counters, AC (Analog Comparator), GCLK (Generic Clock Controller), and SERCOM (I^2C and SPI) do not change values during Standby Sleep mode.

Workaround
Set the voltage regulator in Normal mode before entering Standby Sleep mode to keep the digital pin output enabled. This is done by setting the RUNSTDBY bit in the VREG register.

Affected Silicon Revisions

B	C	D	E	G		
		X				

1.5.10 PORT Output Driver Strength Feature

The PORT output driver strength feature is not available.

Workaround
None

Affected Silicon Revisions

B	C	D	E	G		
X	X					

1.5.11 Clock Failure Detection

After a clock failure detection (INTFLAG.CFD = 1), if INTFLAG.CFD is cleared while the clock is still broken, the system is stuck.

Workaround
After a clock failure detection, do not clear INTFLAG.CFD or perform a system reset.

Affected Silicon Revisions

B	C	D	E	G		
X	X	X	X	X		

1.5.12 Clock Failure Detection for External OSC

Clock Failure detection for external OSC does not work in Standby mode.

Workaround
Before entering Standby mode, move the CPU clock to an internal RC, disable the external OSC, and disable the Clock Failure detector. Upon CPU wake up, restart the external OSC (if it does not start, the failure occurred during Standby mode), enable the Clock Failure detector, and move the CPU clock to the external OSC.

Affected Silicon Revisions

B	C	D	E	G		
X	X	X	X	X		

1.5.13 Digital Output Control in Standby Sleep Mode

Do not enable Timers/Counters, AC (Analog Comparator), GCLK (Generic Clock Controller), and SERCOM (I2C and SPI) to control Digital outputs in Standby Sleep mode.

Workaround
Set the voltage regulator in Normal mode before entering Standby Sleep mode. This is done by setting the RUNSTDBY bit in the VREG register.

Affected Silicon Revisions

B	C	D	E	G		
X	X					

1.5.14 Invalid DFLL Calibration Values

The values stored in the NVM software calibration area for the DFLL calibration are not valid.

Workaround
None.

Affected Silicon Revisions

B	C	D	E	G		
X	X					

1.5.15 Sleep Modes

In Standby, Idle1 and Idle2 Sleep modes, the device might not wake up from sleep. An External Reset, Power-On Reset, or Watchdog Reset will start the device again.

Workaround
The SLEEPPRM bits in the NVMCTRL.CTRLB register must be written to 3 (NVMCTRL - CTRLB.bit.SLEEPPRM = 3) to ensure correct operation of the device. The average power consumption of the device will increase with 20 µA compared to values given in the Electrical Characteristics chapter of the specific device data sheet.

Affected Silicon Revisions

B	C	D	E	G		
X	X	X				

1.5.16 Single-Shot mode at 105°C

In Single-Shot mode and at 105°C, the ADC conversions have linearity errors.

Workarounds

1. At 105°C, do not use the ADC in Single-Shot mode. Instead, use the ADC in Free Running mode only.
2. At 105°C, use the ADC in Single-Shot mode only with VDDANA > 2.7V.

Affected Silicon Revisions

B	C	D	E	G		
		X	X	X		

1.5.17 I²C Slave Mode

In I²C Slave mode, writing the CTRLB register when in the AMATCH or DRDY interrupt service routines can cause the state machine to reset.

Workaround
Write CTRLB.ACKACT to '0' using the following sequence:

```
 // If higher priority interrupts exist, then disable so that the following two writes are
atomic.
SERCOM - STATUS.reg = 0;
SERCOM - CTRLB.reg = 0;
// Re-enable interrupts if applicable.
```

Write CTRLB.ACKACT to '1' using the following sequence:

```
 SERCOM - CTRLB.reg = SERCOM_I2CS_CTRLB_ACKACT;
```

Otherwise, write to CTRLB in the AMATCH or DRDY interrupts if it is to close out a transaction.

When not closing a transaction, clear the AMATCH interrupt by writing a '1' to it's bit position instead of using CTRLB.CMD. The DRDY interrupt is automatically cleared by reading/writing to the DATA register in smart mode. If not in smart mode, DRDY should be cleared by writing a '1' to its bit position.

Code replacements examples:

Current:

```
SERCOM - CTRLB.reg |= SERCOM_I2CS_CTRLB_ACKACT;
```

Change to:

```
SERCOM - STATUS.reg = 0;
SERCOM - CTRLB.reg = SERCOM_I2CS_CTRLB_ACKACT;
SERCOM - CTRLB.reg &= ~SERCOM_I2CS_CTRLB_ACKACT;
SERCOM - CTRLB.reg = 0;
/* ACK or NACK address */
SERCOM - CTRLB.reg |= SERCOM_I2CS_CTRLB_CMD(0x3);
// CMD=0x3 clears all interrupts, so to keep the result similar,
// PREC is cleared if it was set.
if (SERCOM - INTFLAG.bit.PREC) SERCOM - INTFLAG.reg = SERCOM_I2CS_INTFLAG_PREC;
SERCOM - INTFLAG.reg = SERCOM_I2CS_INTFLAG_AMATCH;
```

Affected Silicon Revisions

B	C	D	E	G		
		X	X			

1.5.18 NVM User Row Mapping

In the table "NVM User Row Mapping", bits 40 and 41 default values on silicon are not as specified in the device data sheet. The data sheet defines the default value as '0'; however, it is '1' for both bits on silicon.

Workaround
None.

Affected Silicon Revisions

B	C	D	E	G		
		X	X	X		

1.5.19 WDT Window Bits

In the table "NVM User Row Mapping", the WDT Window bit field default value on silicon is not as specified in the device data sheet. The device data sheet defines the default value as '0x5' while it is '0xB' on silicon.

Workaround
None.

Affected Silicon Revisions

B	C	D	E	G		
X	X	X	X	X		

1.5.20 Incorrect SYSTICK Calibration Value

The SYSTICK calibration value is incorrect.

Workaround
The correct SYSTICK calibration value is 0x40000000. This value should not be used to initialize the Systick RELOAD value register, which should be initialized instead with a value depending on the main clock frequency and on the tick period required by the application. For a detailed description of the SYSTICK module, refer to the ARM Cortex-M0+ documentation.

Affected Silicon Revisions

B	C	D	E	G		
X	X	X	X	X		

1.6 Device Service Unit (DSU)

1.6.1 Debugging

If a debugger has issued a DSU Cold-Plugging procedure and then released the CPU from the resulting "CPU Reset Extension", the CPU will be held in "CPU Reset Extension" after any upcoming reset event.

Workaround
The CPU must be released from the "CPU Reset Extension" either by writing a one in the DSU STATUSA.CRSTEXT register or by applying an external reset with SWCLK high or by power cycling the device.

Affected Silicon Revisions

B	C	D	E	G		
X	X	X				

1.6.2 Non-functional MBIST "Pause-on-Error" Feature

The MBIST "Pause-on-Error" feature is not functional on this device.

Workaround
Do not use the "Pause-on-Error" feature.

Affected Silicon Revisions

B	C	D	E	G		
X	X	X	X	X		

1.7 Digital-to-Analog Converter (DAC)

1.7.1 Standby Sleep Mode

When DAC.CTRLA.RUNSTDBY = 0 and DATABUF is written (not empty), if the device goes to Standby Sleep mode before a Start Conversion event, DAC.INTFLAG.EMPTY will be set after exit from Sleep mode.

Workaround
After waking from Standby mode, ignore and clear the flag DAC.INTFLAG.EMPTY.

Affected Silicon Revisions

B	C	D	E	G		
X	X	X	X	X		

1.8 External Interrupt Controller (EIC)

1.8.1 Edge Configuration

When the EIC is configured to generate an interrupt on a low level or rising edge or both edges (CONFIGn.SENSEx) with the filter enabled (CONFIGn.FILTENx), a spurious flag might appear for the dedicated pin on the INTFLAG.EXTINT[x] register as soon as the EIC is enabled using the CTRLA ENABLE bit.

Workaround
Clear the INTFLAG bit once the EIC is enabled and before enabling the interrupts.

Affected Silicon Revisions

B	C	D	E	G		
X	X	X	X	X		

1.9 Event System (EVSYS)

1.9.1 Channel Generator Change

Changing the selected generator of a channel can trigger a spurious interrupt/event.

Workaround
To change the generator of a channel, first write with EDGESEL written to zero, then perform a second write with EDGESEL written to its target value.

Affected Silicon Revisions

B	C	D	E	G		
X	X					

1.9.2 Overrun Condition

Using synchronous or resynchronized paths, some channels (0,3,6,7) detect an overrun on every event even if no overrun condition is present.

Workaround
Ignore overrun detection bit for channels 0,3,6,7 and use channels 1,2,4,5 if overrun detection is required.

Affected Silicon Revisions

B	C	D	E	G		
X	X					

1.10 General Clock (GCLK)

1.10.1 GCLK Lock State

When a GCLK is locked and the generator used by the locked GCLK is not GCLK generator 1, issuing a GCLK software reset will lock up the GCLK with the SYNCBUSY flag always set.

Workaround
Do not issue a GCLK SWRST or map GCLK generator 1 to ""locked"" GCLKs.

Affected Silicon Revisions

B	C	D	E	G		
X	X					

1.10.2 Division Factor

The GCLK Generator clock is stuck when disabling the generator and changing the division factor from '1' to a different value while the GCLK generator is set as output. When the GCLK generator is enabled (GENCTRL.GENEN=1), set as output (GENCTRL.OE = 1) and use a division factor of one (GENDIV.DIV = 1 or 0 and GENCTRL.DIVSEL = 0), if the division factor is written to a value different of '1' or '0' after disabling the GCLK generator (GENCTRL.GENEN=0), the GCLK generator will be stuck.

Workaround
Disable the OE request of the GCLK generator (GENCTRL.OE=0) before disabling the GCLK generator (GENCTRL.GENEN=0).

Affected Silicon Revisions

B	C	D	E	G		
X	X					

1.10.3 Division Factor

When the GCLK generator is enabled (GENCTRL.GENEN = 1), set as output (GENCTRL.OE = 1) and use a division factor of one (GENDIV.DIV = 1 or 0 and GENCTRL.DIVSEL=0), the GCLK_IO might not be set to the configured GENCTRL.OOV value after disabling the GCLK generator (GENCTRL.GENEN=0).

Workaround
Disable the OE request of the GCLK generator (GENCTRL.OE = 0) before disabling the GCLK generator (GENCTRL.GENEN = 0).

Affected Silicon Revisions

B	C	D	E	G		
X	X					

1.11 I/O Pin Controller (PORT)

1.11.1 PORT Read and Write

PORT read/write attempts on non-implemented registers, including addresses beyond the last implemented register group (PA, PB,...), do not generate a PAC protection error.

Workaround
None.

Affected Silicon Revisions

B	C	D	E	G		
X	X	X	X	X		

1.12 Non-Volatile Memory Controller (NVMCTRL)

1.12.1 Erase or Write

When NVMCTRL issues either erase or write commands and the NVMCTRL cache is not in LOW_POWER mode, CPU hardfault exception may occur.

Workaround
Either turn off cache before issuing Flash commands, by setting the NVMCTRL CTRLB.CACHEDIS bit to '1', or configure the cache in LOW_POWER mode by writing '0x1' into the NVMCTRL CTRLB.READMODE bit.

Affected Silicon Revisions

B	C	D	E	G		
X	X					

1.12.2 Cache Read Mode

When Cache Read mode is set to deterministic (READMODE=2), setting CACHEDIS=1 does not lead to 0 wait states on Flash access.

Workaround
When disabling the cache (CTRLB.CACHEDIS=1), the user must also set READMODE to 0 (CTRLB.READMODE=0).

Affected Silicon Revisions

B	C	D	E	G		
X	X					

1.12.3 EEPROM Emulation Area Configuration

When the device is secured and EEPROM emulation area configured to none, the CRC32 is not executed on the entire Flash area but up to the on-chip Flash size minus half a row.

Workaround
When using CRC32 on a protected device with EEPROM emulation area configured to none, compute the reference CRC32 value to the full chip Flash size minus half row.

Affected Silicon Revisions

B	C	D	E	G		
X	X	X				

1.12.4 Default MANW Value

Default value of MANW in NVM.CTRLB is 0.

Workaround
This can lead to spurious writes to the NVM if a data write is done through a pointer with a wrong address corresponding to NVM area.

Set MANW in the NVM.CTRLB to 1 at startup.

Affected Silicon Revisions

B	C	D	E	G		
X	X	X	X	X		

1.12.5 High Leakage Current

When external reset is active, it causes a high leakage current on VDDIO.

Workaround
Minimize the time external reset is active.

Affected Silicon Revisions

B	C	D	E	G		
X	X	X	X	X		

1.13 Peripheral Touch Controller (PTC)

1.13.1 Gain Settings

Some gain settings for the PTC in self-capacitance mode do not work. The two lowest gain settings are not selectable and an attempt by the QTouch Library to set enable of these may result in a higher sensitivity than optimal for the sensor. The PTC will not detect all touches. This errata does not affect mutual-capacitance mode which operates as specified.

Workaround
Use SAM D20 revision C or later for self-capacitance touch sensing.

Affected Silicon Revisions

B	C	D	E	G		
X						

1.13.2 WCOMP Interrupt Flag

WCOMP interrupt flag is not stable. The WCOMP interrupt flag will not always be set as described in the data sheet.

Workaround
Do not use the WCOMP interrupt instead use the WCOMP event.

Affected Silicon Revisions

B	C	D	E	G		
X	X	X				

1.14 Power Manager (PM)

1.14.1 SysTick Timer

The SysTick timer does not generate a wake up signal to the Power Manager, and therefore cannot be used to wake up the CPU from Sleep mode.

Workaround
None.

Affected Silicon Revisions

B	C	D	E	G		
X	X					

1.14.2 Watchdog Reset During Debug Mode

In Debug mode, if a Watchdog Reset occurs, the debug session is lost.

Workaround
A new debug session must be restart after a Watchdog Reset.

Affected Silicon Revisions

B	C	D	E	G		
X	X	X				

1.15 Serial Communication Interface (SERCOM)

1.15.1 SPI BUFOVF Bit

The SERCOM SPI BUFOVF status bit is not set until the next character is received after a buffer overflow, instead of directly after the overflow has occurred. In addition, the CTRLA.IBON bit will always be zero and cannot be changed.

Workaround
None.

Affected Silicon Revisions

B	C	D	E	G		
X	X					

1.15.2 BUFOVF Flag

When the SERCOM is in Slave SPI mode, the BUFOVF flag is not automatically cleared when CTRLB.RXEN is set to zero.

Workaround
The BUFOVF flag must be manually cleared by software.

Affected Silicon Revisions

B	C	D	E	G		
X	X					

1.15.3 SPI CTRLA Register

The SERCOM SPI CTRLA register bit 17 (DOPO Bit 1) will always be zero, and cannot be changed. Therefore, the SERCOM SPI cannot be switched between master and slave mode on the same DI and DO pins.

Workaround
Connect the alternate DI and DO pins externally and use the port MUX to switch between pin configurations for master and slave functionality.

Affected Silicon Revisions

B	C	D	E	G		
X	X					

1.15.4 TWI Master Mode

In TWI master mode, an ongoing transaction should be stalled immediately when DBGCTRL.DBGSTOP is set and the CPU enters debug mode. Instead, it is stopped when the current byte transaction is completed and the corresponding interrupt is triggered if enabled.

Workaround
In TWI master mode, keep DBGCTRL.DBGSTOP=0 when in debug mode.

Affected Silicon Revisions

B	C	D	E	G		
X	X	X	X			

1.16 Timer/Counter (TC)

1.16.1 Spurious Events

Spurious TC overflow and Match/Capture events may occur.

Workaround
Do not use the TC overflow and Match/Capture events. Use the corresponding Interrupts instead.

Affected Silicon Revisions

B	C	D	E	G		
X	X	X				

1.16.2 TC3

When enabled, the TC3 may not start automatically.

Workaround
After TC3 has been enabled, the TC3 must be retriggered by software (using command TC_CTRLBSET_CMD_RETRIGGER in register CTRLBSET[7:6]). This ensures that TC3 starts in any case.

Affected Silicon Revisions

B	C	D	E	G		
			X			

2. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS60001504B):

Note: Corrections in tables, registers, and text are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

No clarifications to report at this time.

3. Appendix A: Revision History

Rev A Document (8/2017)
Initial release of this document.

Rev B Document (12/2017)
Updated the Data Sheet revision from A to B.

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