



## Production-Ready Design for IoT and Industrial Gateway Applications

# IoT Gateway Reference Design

The IoT gateway reference design based on the QorIQ LS1021A processor (LS1021A-IOT-B) is a purpose-built, small footprint hardware platform equipped with a wide array of high speed connectivity and low speed serial interfaces engineered to support the secure delivery of IoT services to end users in a home, business or other commercial location.

### OVERVIEW

The affordable reference design combines standards-based, open source software together with a feature-rich IoT gateway design, to establish a common, open framework for secure IoT service delivery and management.

### VERSATILE DESIGN

Setting the LS1021A-IoT gateway apart is the wide assortment of high speed and serial based connectivity it offers in a compact, highly secure design, delivering an impressive level of versatility. An additional innovation of the reference design is its support for Arduino Shield™ modules, which further enable support for a variety of communication solutions offered by the family of Arduino modules. High efficiency is achieved through the use of the ARM®-based QorIQ LS1021A embedded processor, which delivers over 5,000 CoreMarks® of performance at a typical power of under 3 Watts. The MC34VR500 regulator powers the complete LS1021A-IoT gateway design.

This device is ideally suited to power system solutions with unique programmable multiple DC/DC and LDO outputs. In addition to its outstanding performance efficiency and high level of integration, the LS1021A-IoT gateway design offers HDMI, SATA3 and USB3 connectors as well as a complete Linux® software developers package.

The LS1021A-IoT reference design supports a comprehensive level of security, which includes secure boot, Trust Architecture and tamper detection for both standby and active power modes. Together, these features safeguard customer designs from the point of manufacture to the

point of deployment, providing continuous protection from malicious attacks and ensures end products deliver the highest level of security and reliability.

### KEY FEATURES:

- ▶ 1 Gb QSPI NOR Flash
- ▶ 1 GB DDR3L
- ▶ SDHC slot—up to 32 GB
- ▶ 4 GB populated
- ▶ 1x One Gb/s Ethernet (SGMII)
- ▶ 1x One Gb/s Ethernet (RGMII)
- ▶ 2x mini PCIe (x1) slots
- ▶ 1x mSATA slot
- ▶ 1x Terminal (USB to UART)
- ▶ 1x Four wire LP-UART to Arduino connector (ZigBee®)
- ▶ Muxed LCD/QE interface
- ▶ 24-bit LVDS LCD interface
- ▶ QE UART to header for PROFIBUS or RS485 (external transceiver required)





### FEATURES

- ▶ 2x ports—USB-A
- ▶ 2x ports to mini PCIe slots
- ▶ 13x GPIO or 8x FTM (PWM)
- ▶ 6x Interrupts
- ▶ 1x SPI
- ▶ I<sup>2</sup>C<sup>1</sup> bus
- ▶ Board EEPROM
- ▶ Boot EEPROM
- ▶ Arduino Connector
- ▶ Sensors/PHYs, etc., TBD
- ▶ I<sup>2</sup>C<sup>2</sup>
- ▶ GPIO expansion
- ▶ ADC
- ▶ Sensors/PHYs, etc., TBD
- ▶ Certification: FCC Class B and CE
- ▶ Included in Kit:
- ▶ Linux and OpenWRT software included
- ▶ Reference design (schematics, layout and BOM available)
- ▶ Hardware Quick Start Guide and User Guide

### READY-TO-MANUFACTURE DESIGN

The LS1021A-IoT gateway reference design can significantly reduce investment costs for OEM or ODM manufacturers seeking to address new IoT market needs or deploy new IoT services. As new standards emerge, the IoT gateway design enables them to be quickly supported through a standards based design approach without significant investment costs. Combined with a comprehensive software development kit that has been optimized to support the platform wide variety of interfaces and protocols ensures maximum usability. We make available to customers purchasing the IoT gateway platform the complete design files, as well as detailed bill of materials (BOM) at no additional charge.

### BOARD ENCLOSURE

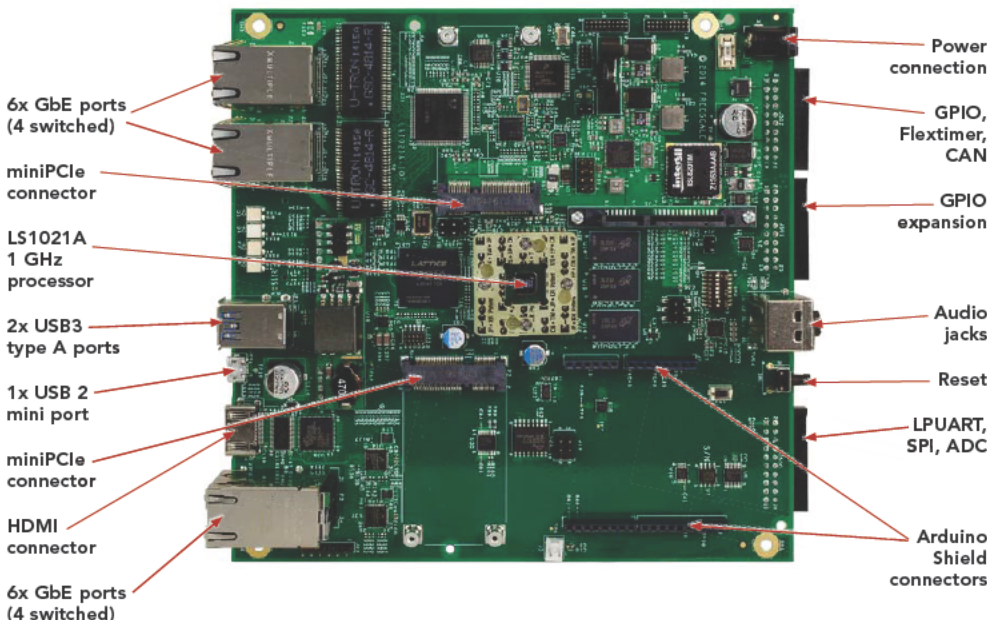


### RELATED PRODUCTS

- ▶ VR500 multi-output DC/DC regulator
- ▶ MMA8451Q 3-axis MEMS sensor
- ▶ Kinetis K20 MCU
- ▶ Audio codec

To learn more, visit [www.nxp.com/QorIQ](http://www.nxp.com/QorIQ)

### TOP OF BOARD



# QorIQ LS1021A-IOT GATEWAY SYSTEM BLOCK DIAGRAM

