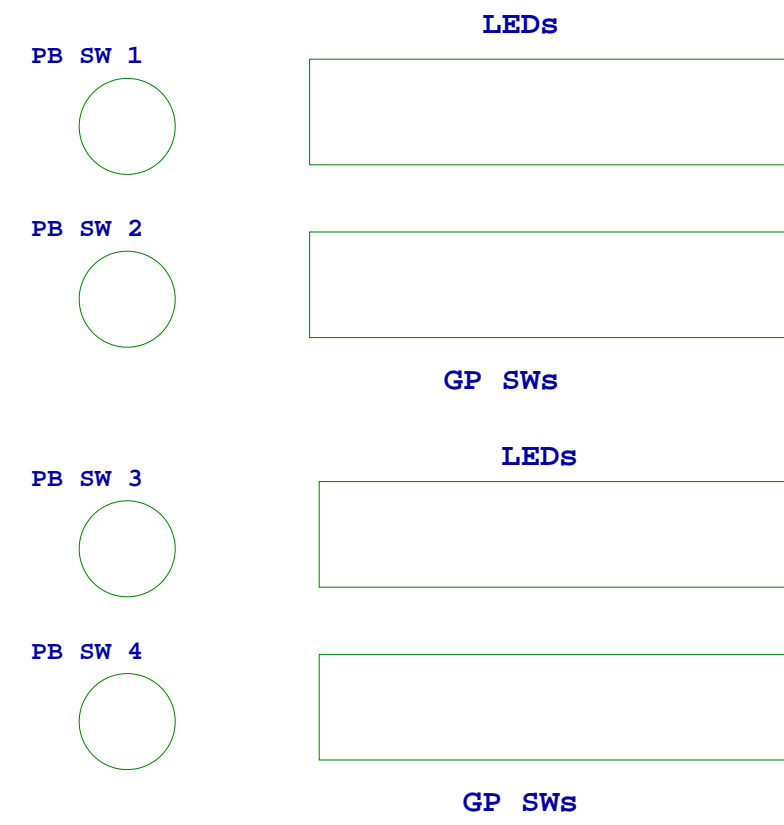
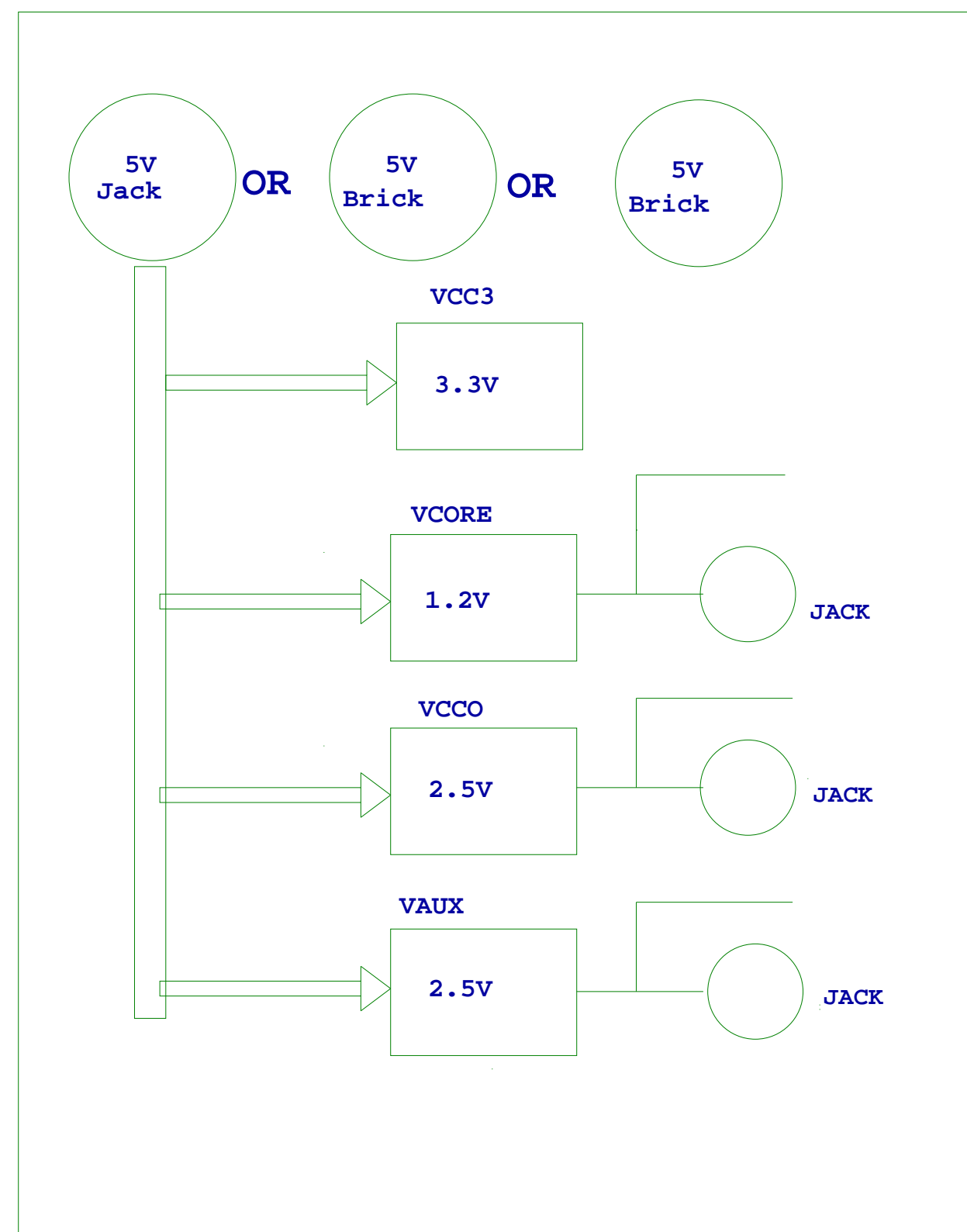
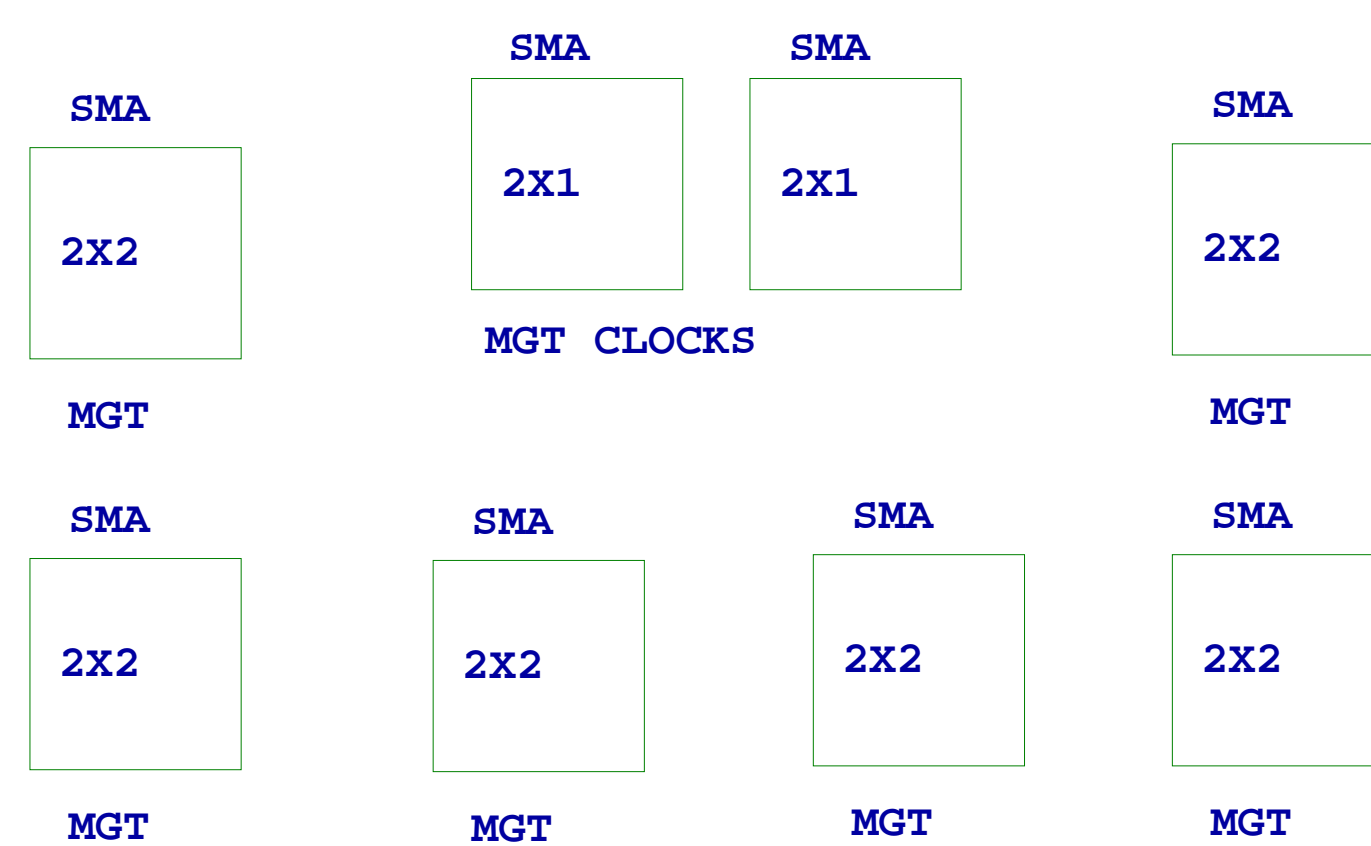
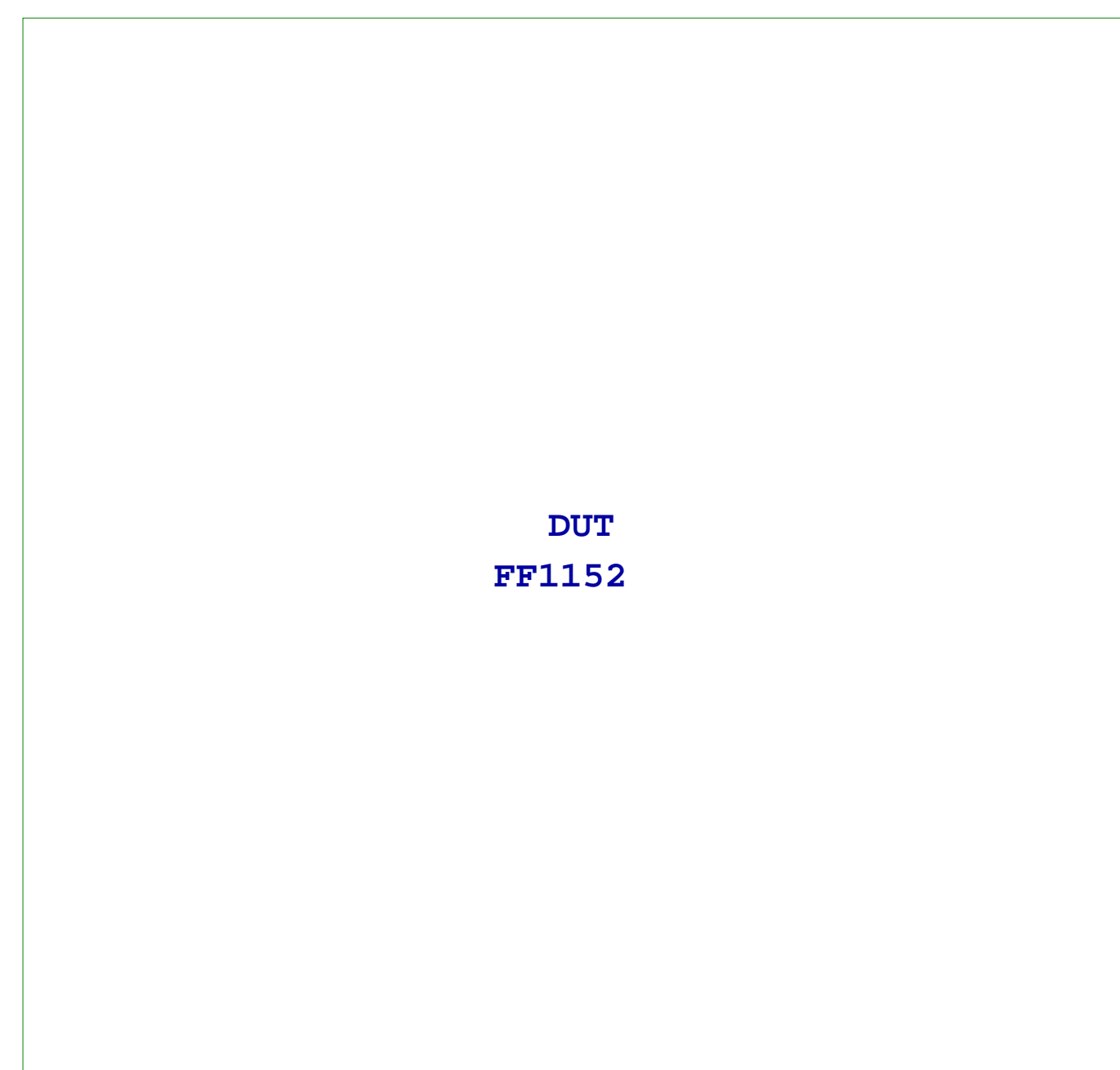
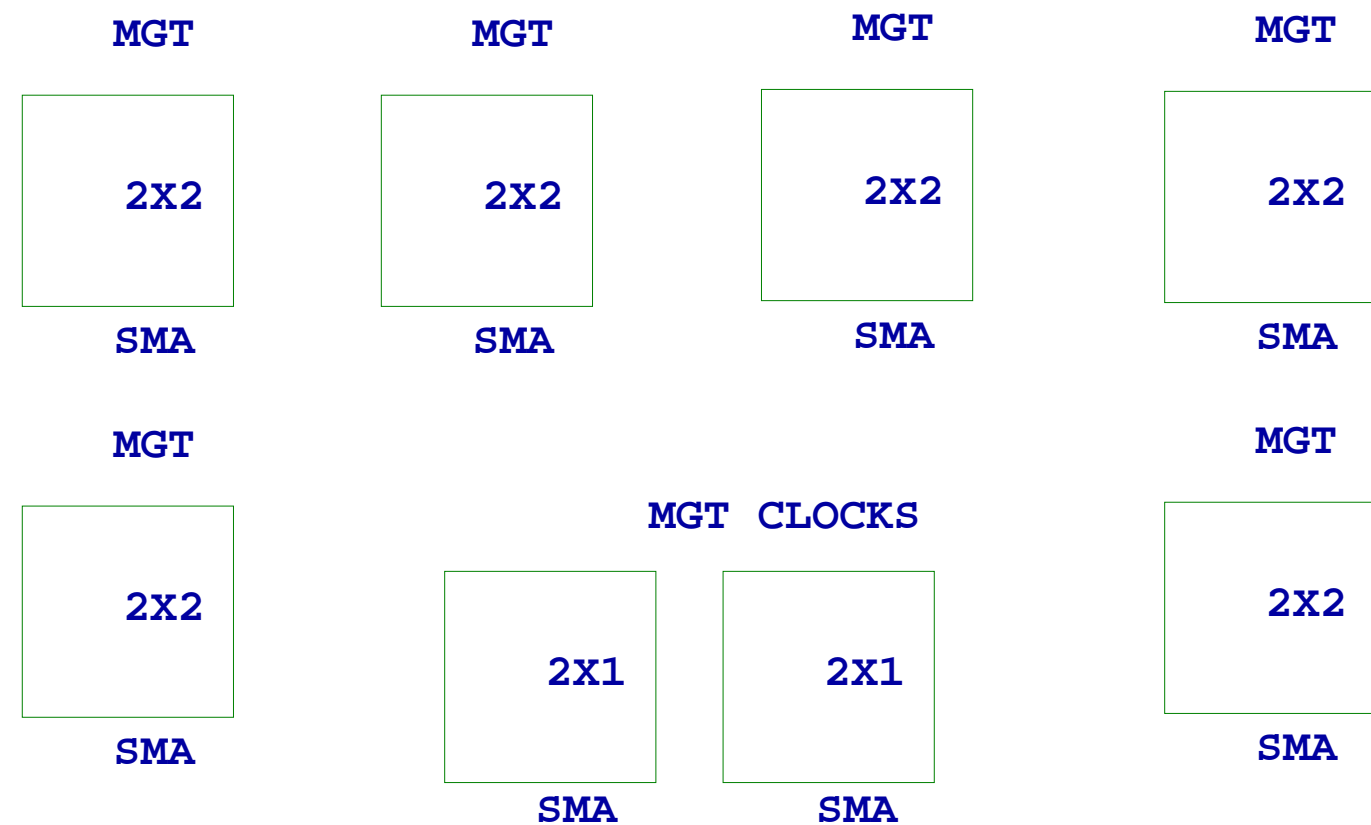
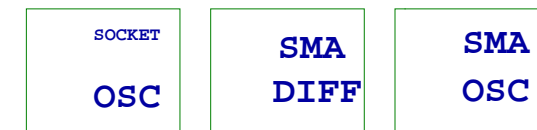


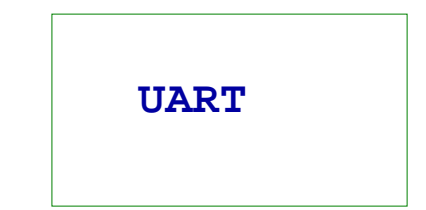
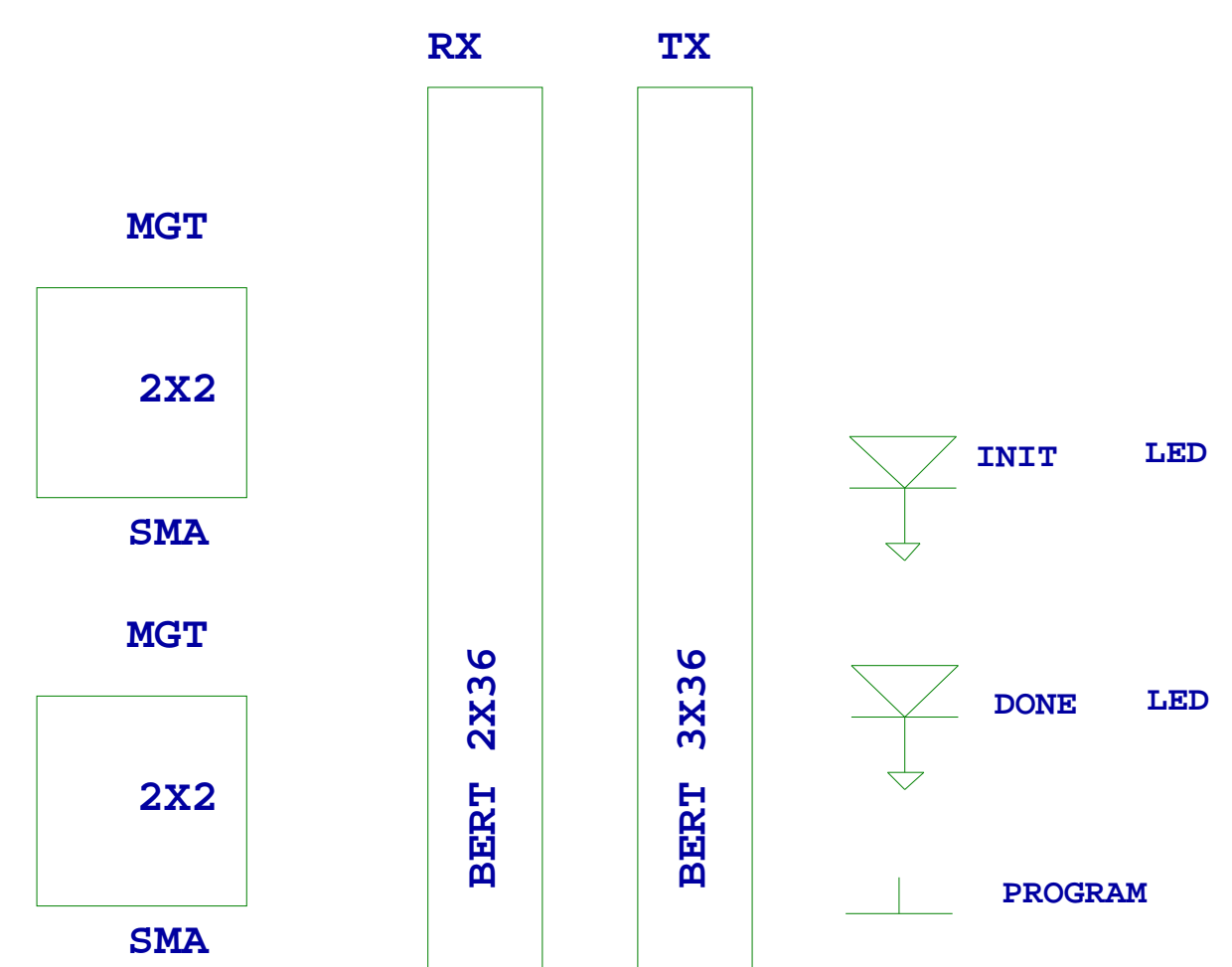
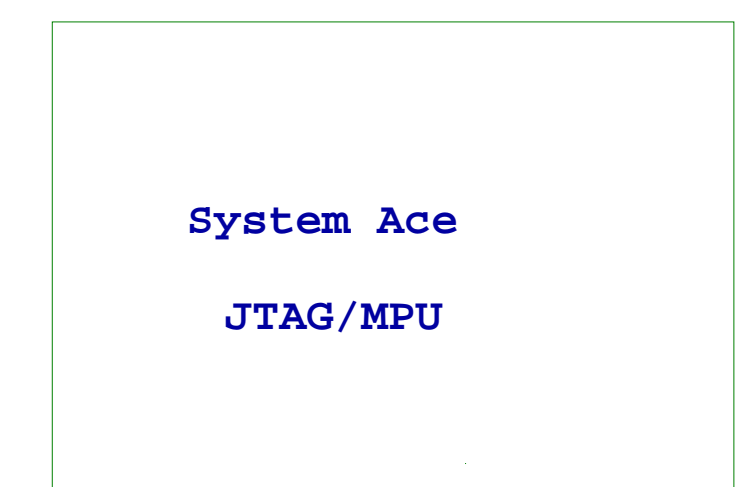
ON BOARD FPGA SUPPLIES



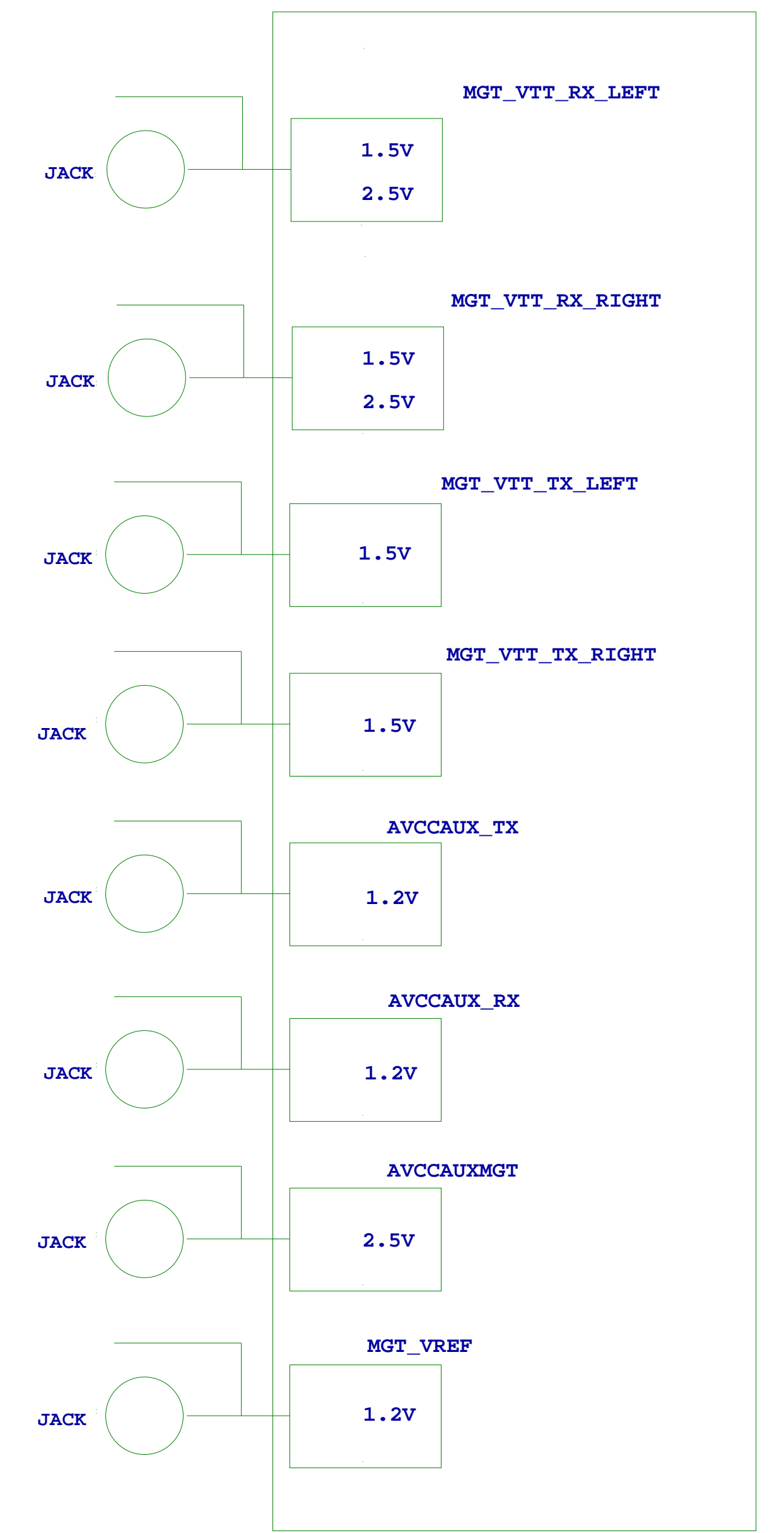
STANDARD CLOCKS

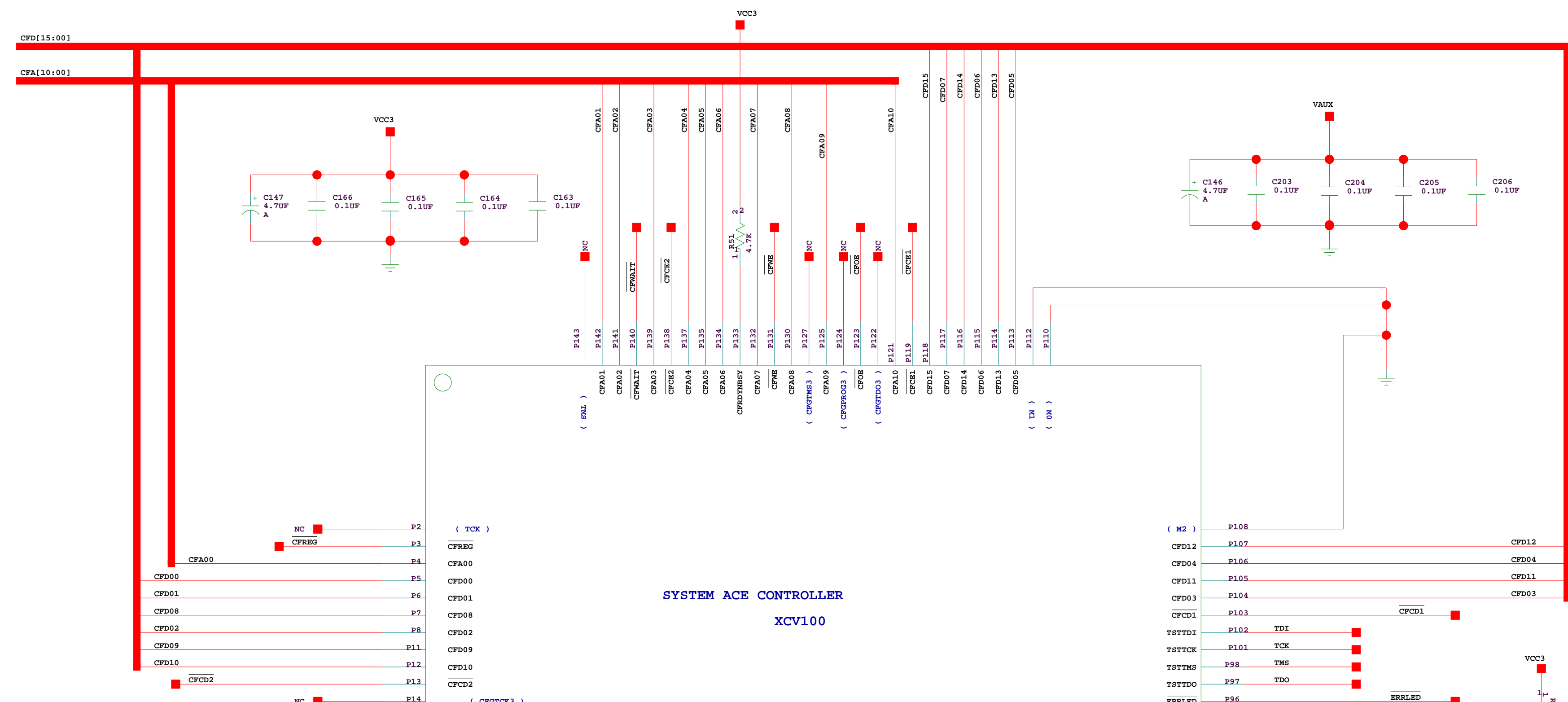


STANDARD CLOCKS



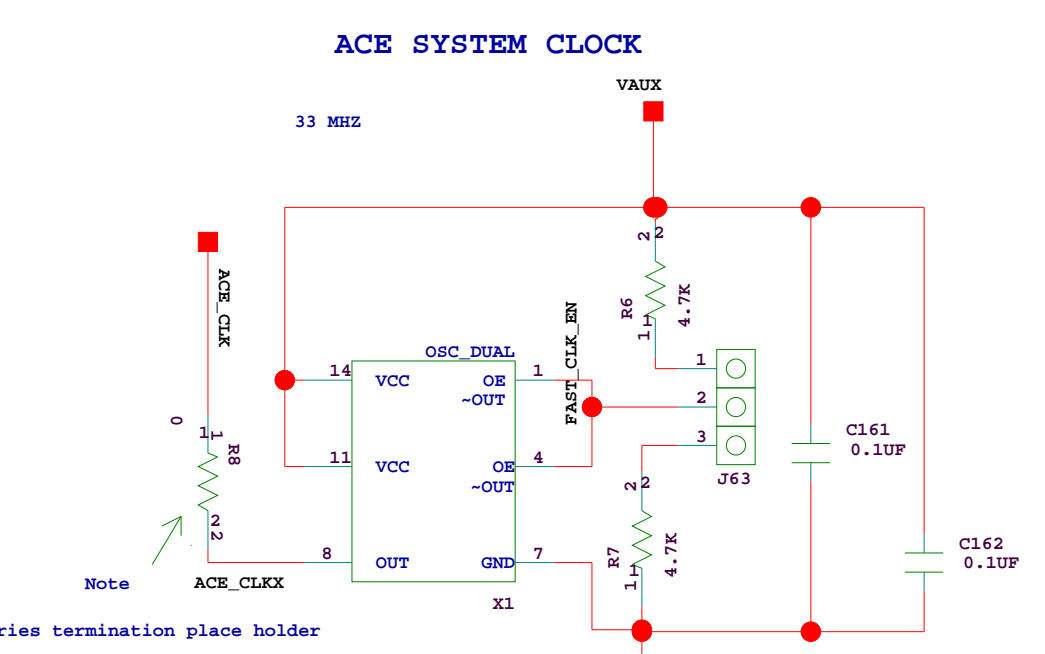
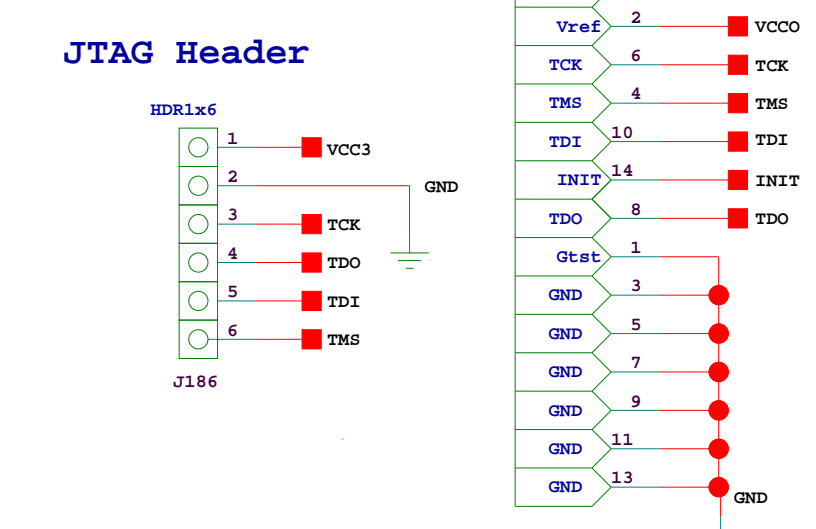
MGT POWER MODULE



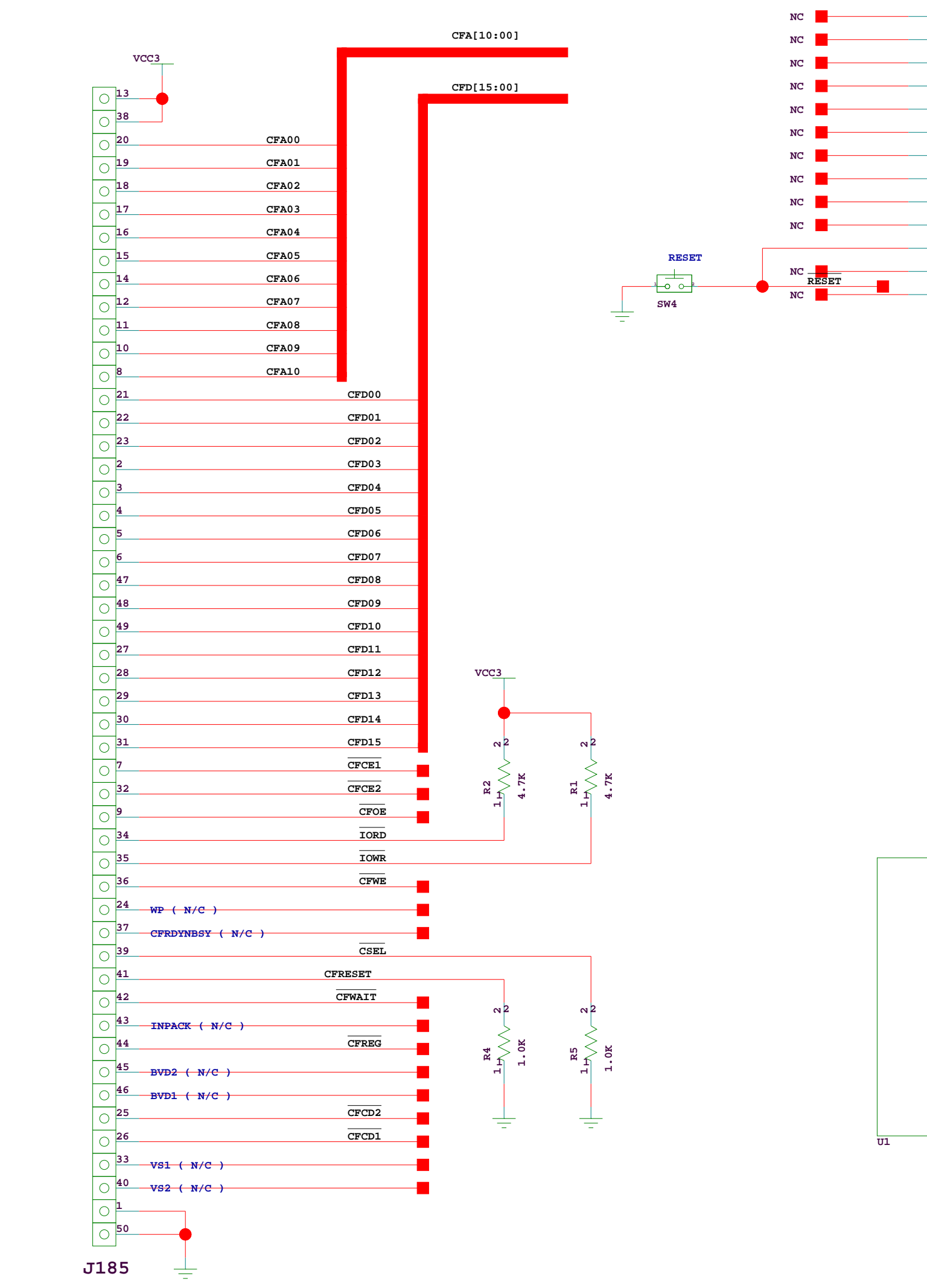


SW5	FUNCTION
1	CONFIG FILE ADDRESS_2
2	CONFIG FILE ADDRESS_1
3	CONFIG FILE ADDRESS_0
1	SELECTION
2	FILE INDEX 0
3	FILE INDEX 1
4	FILE INDEX 2
5	FILE INDEX 7

NOTATION:
 OPEN
 CLOSED

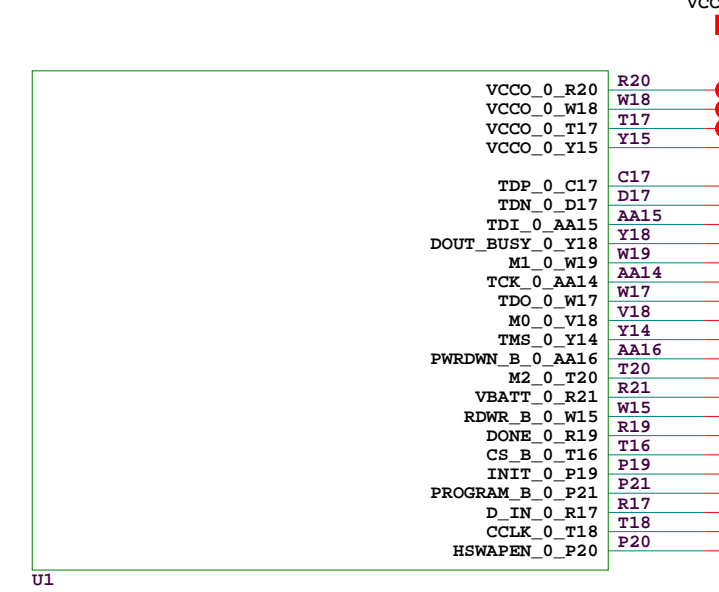
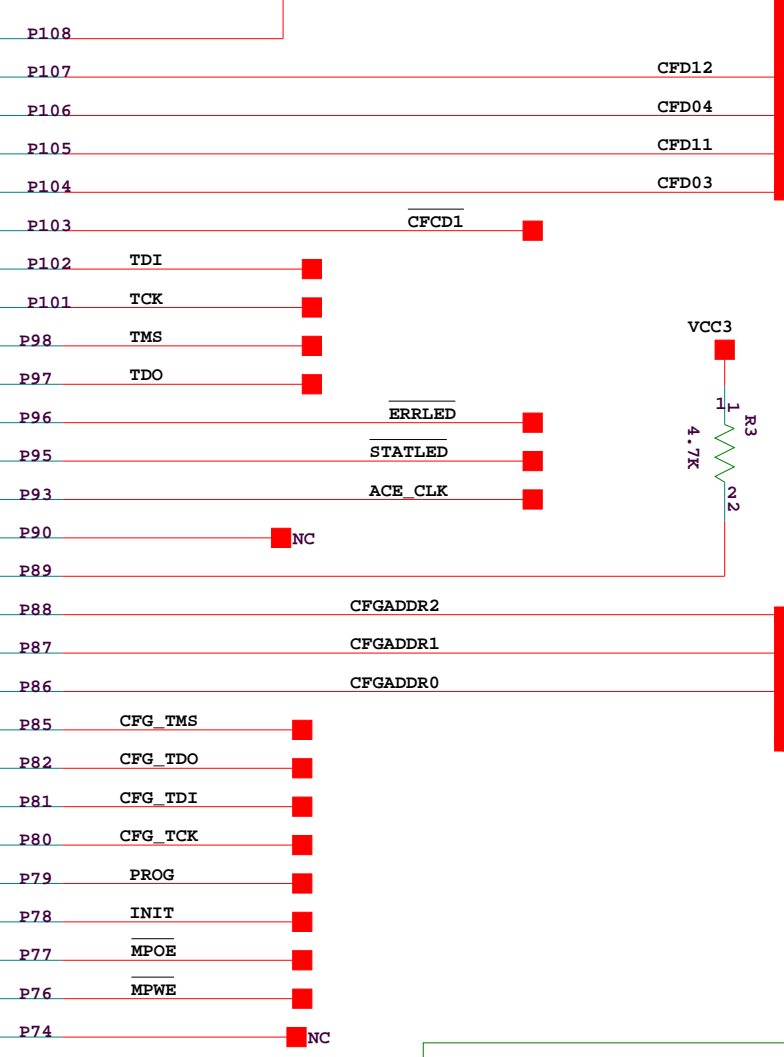
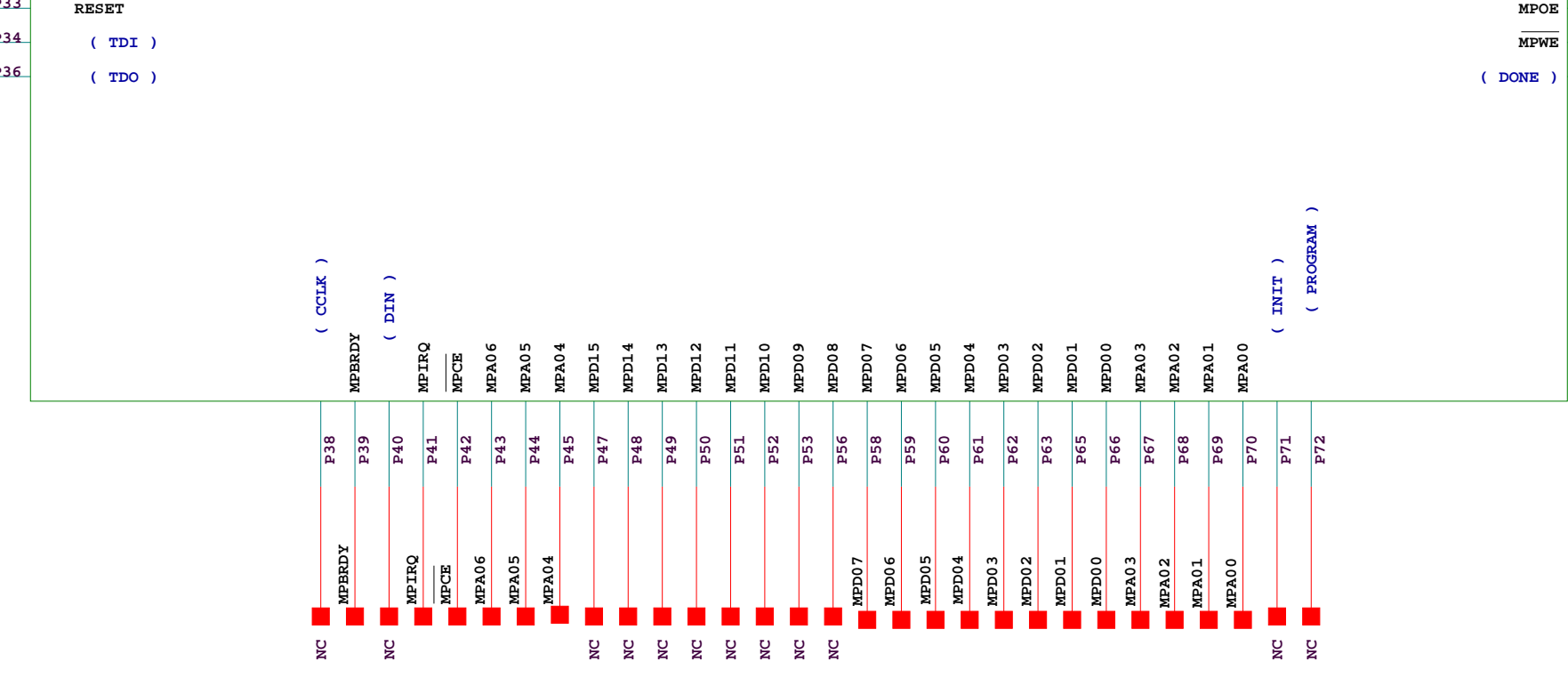


COMPACT FLASH CARD INTERFACE

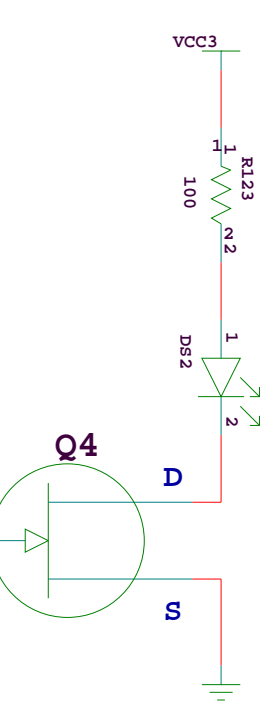


(DIE UP) TQ144

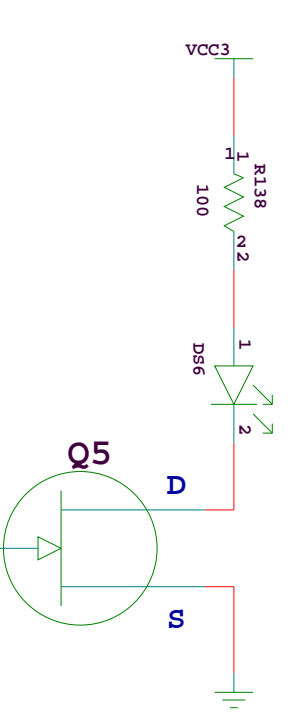
NOTE: SIGNALS IN PARENTHESES ARE INTERNAL 'NO-CONNECTS' IN ASIC



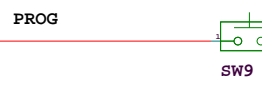
DONE LED



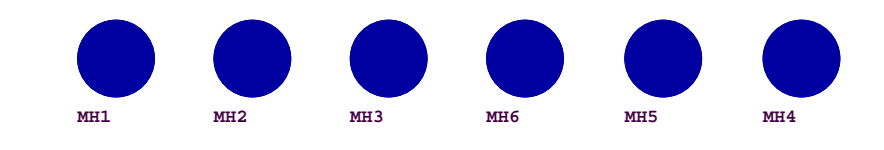
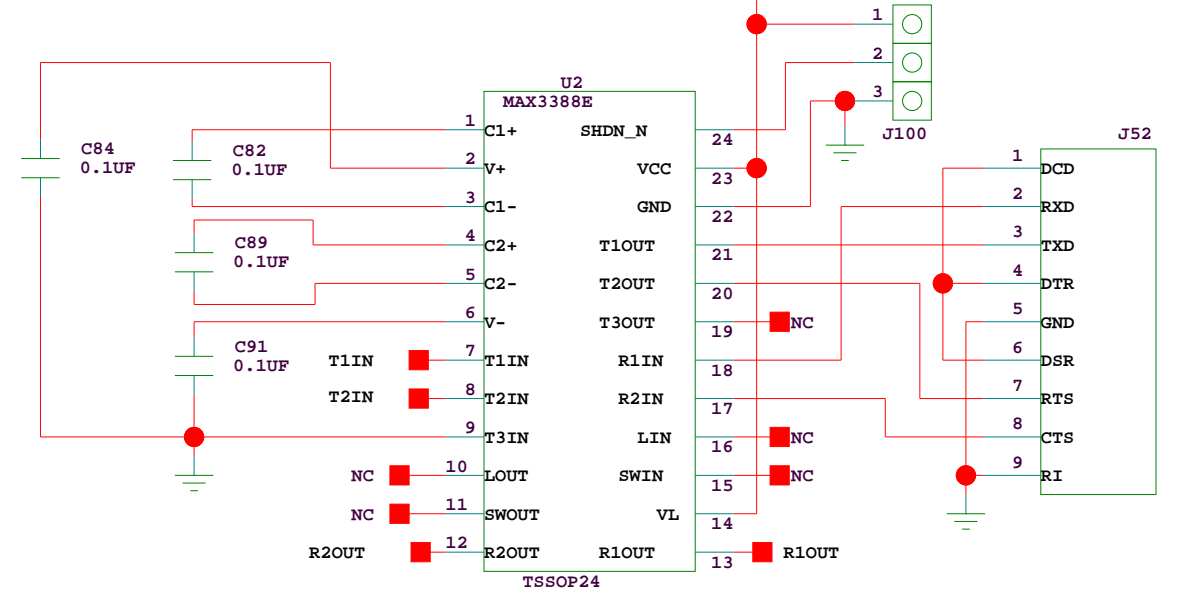
INIT LED



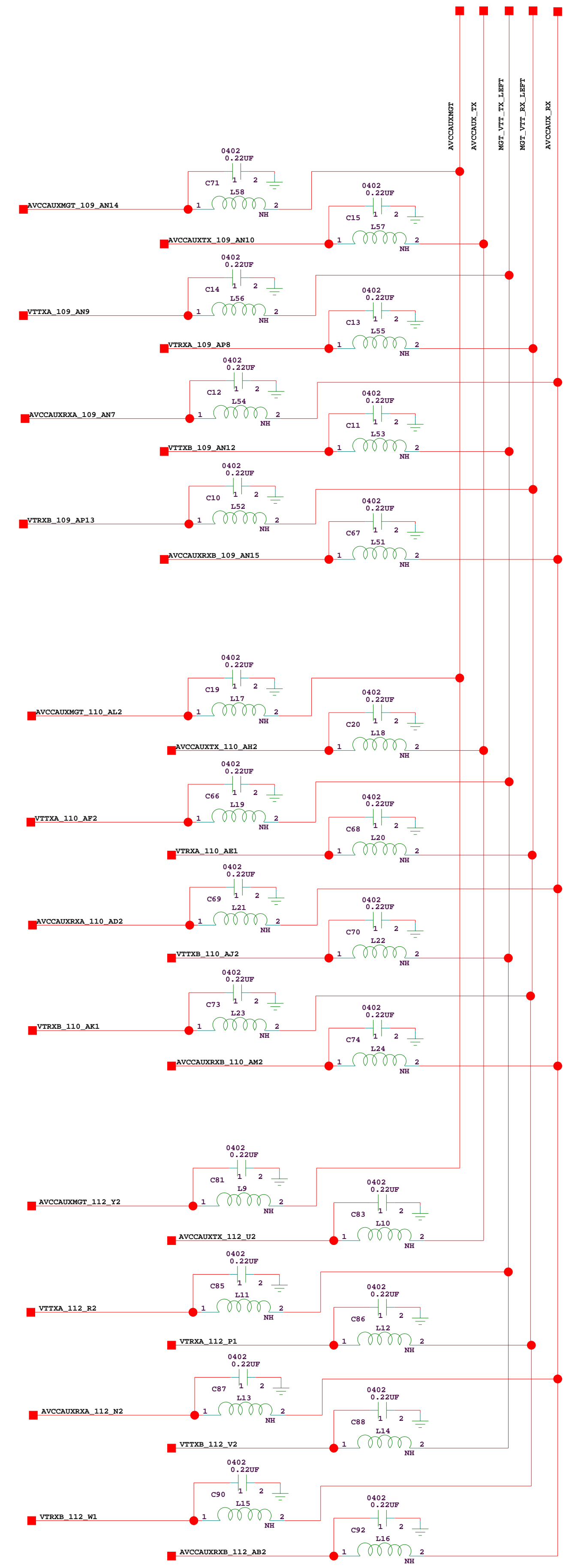
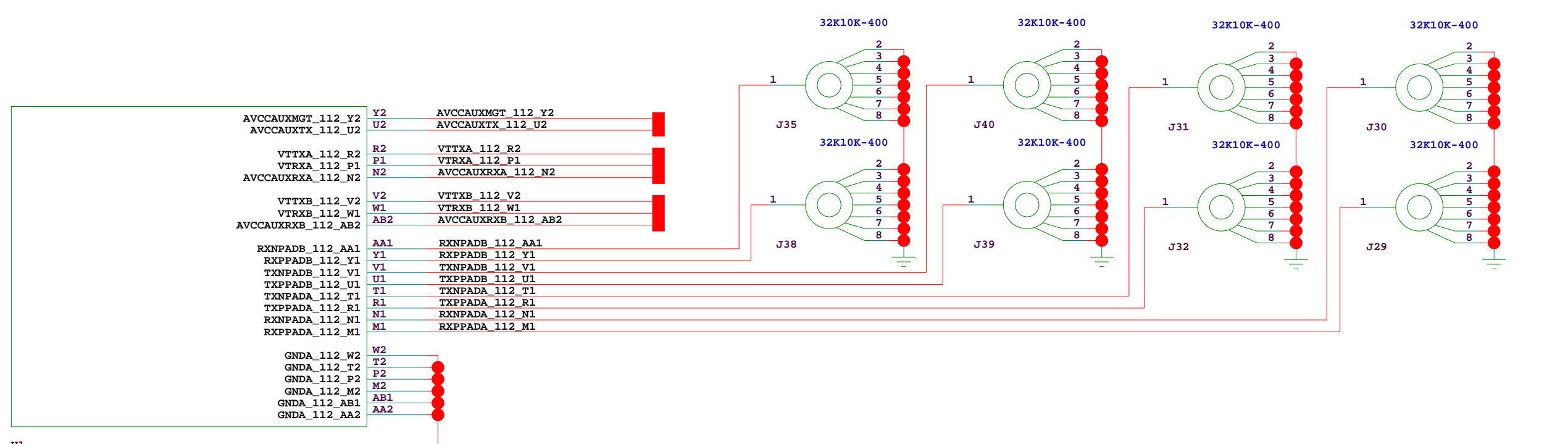
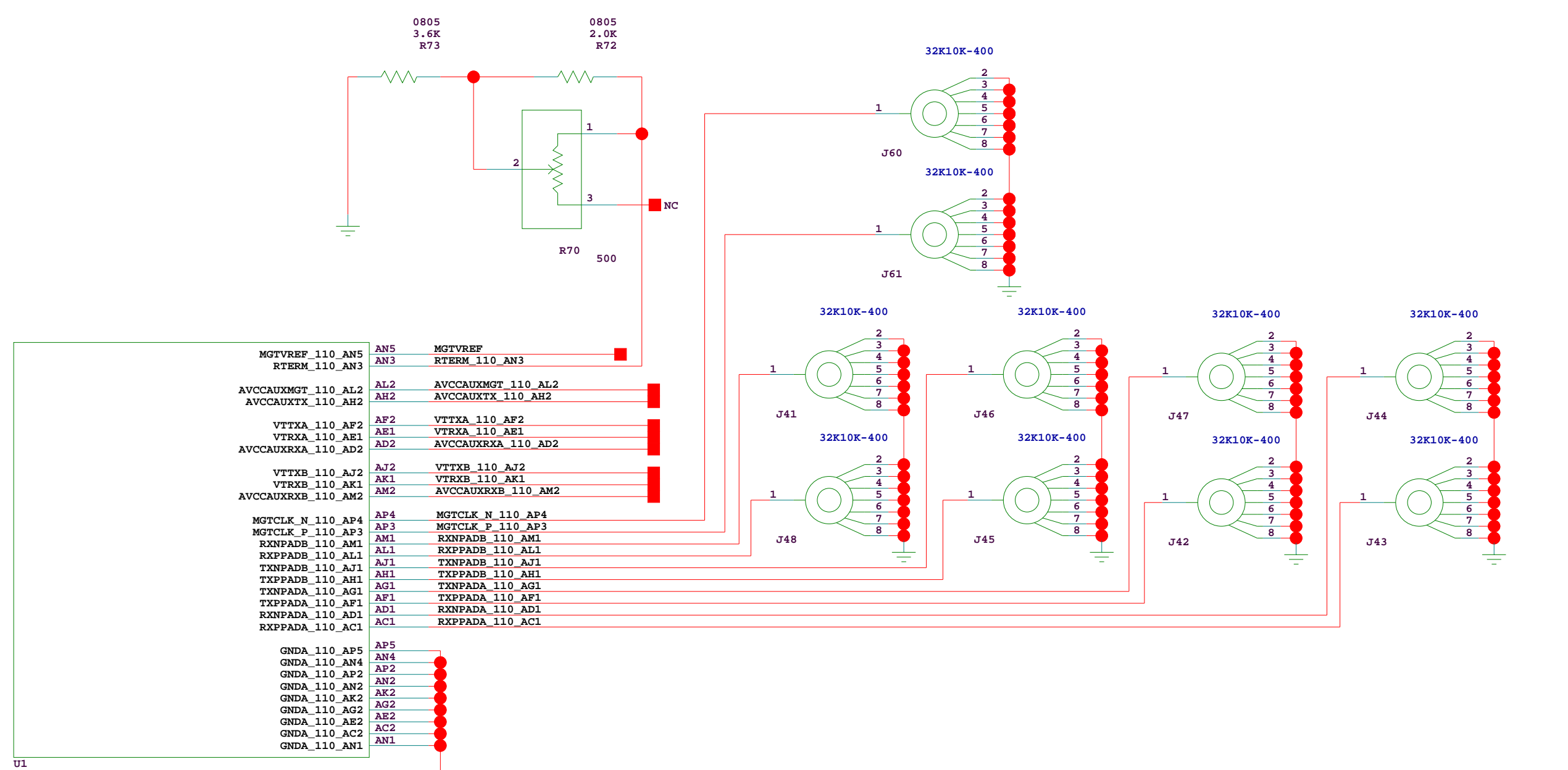
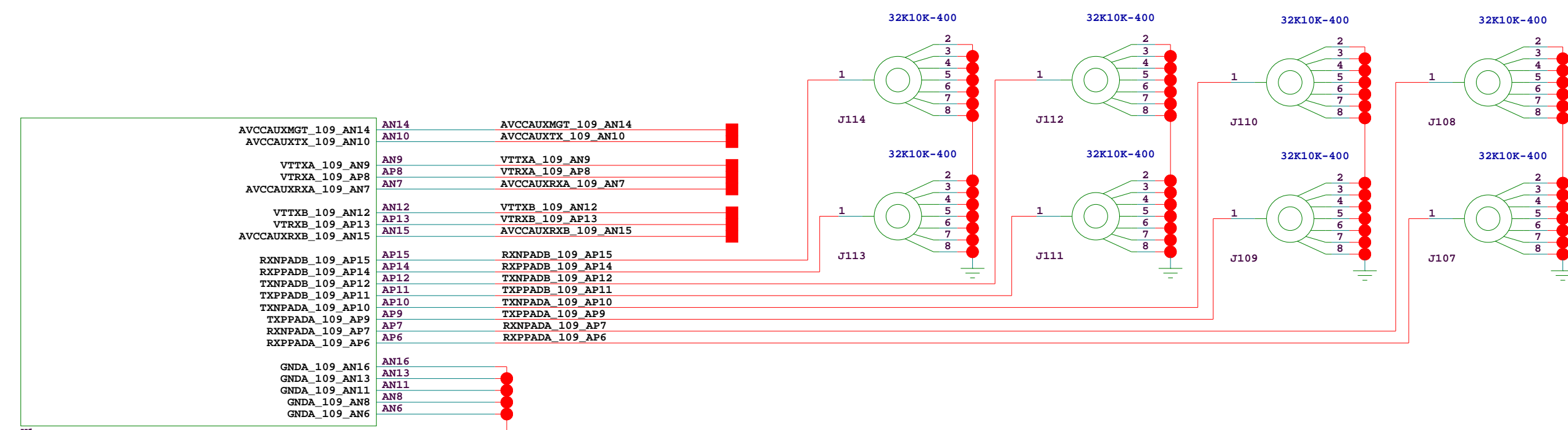
PROGRAM

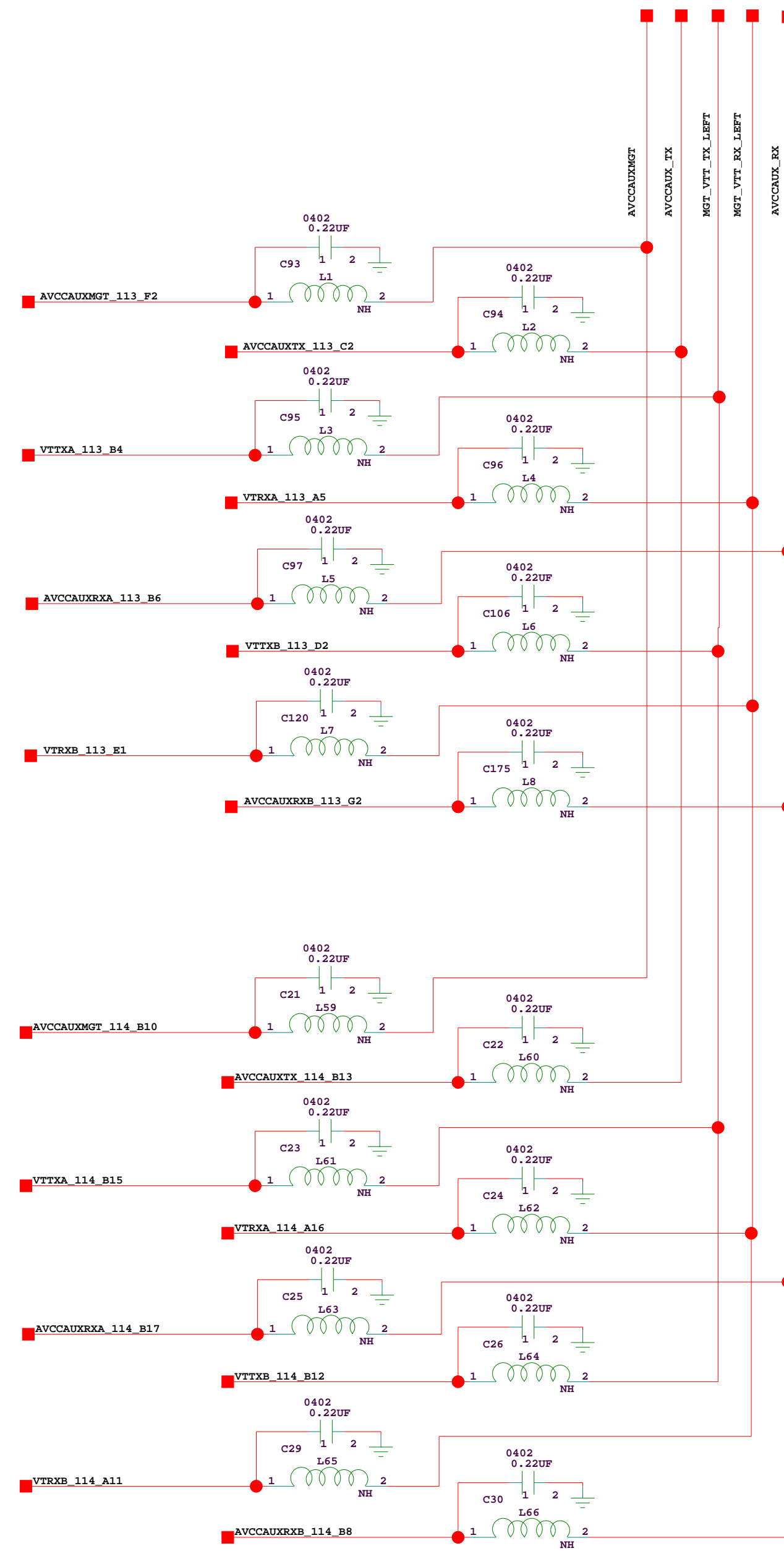
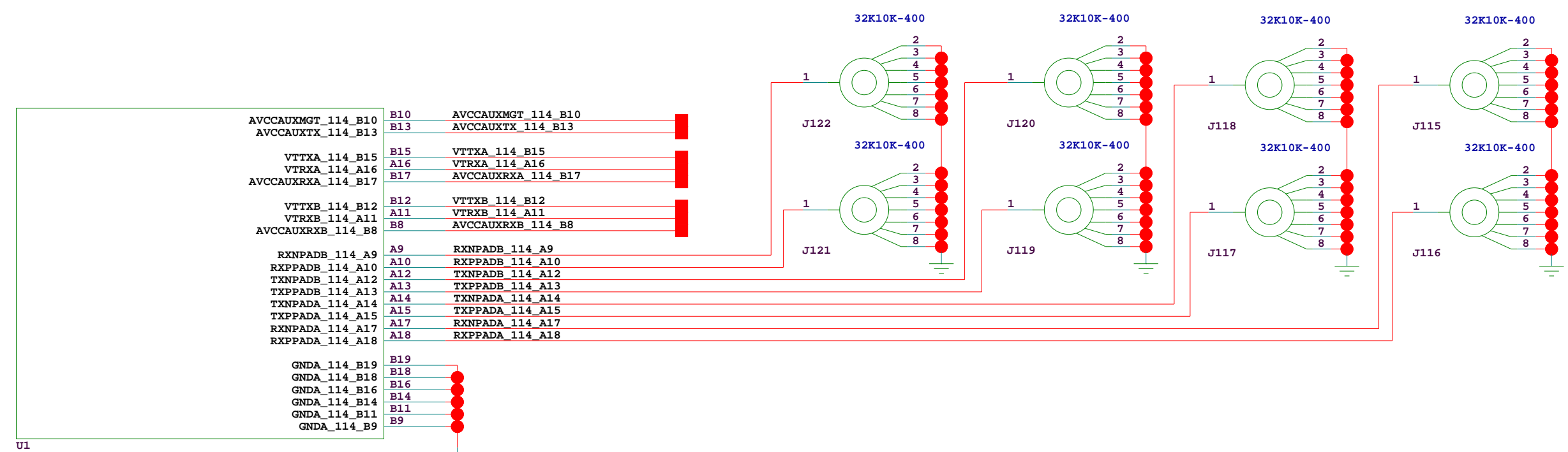
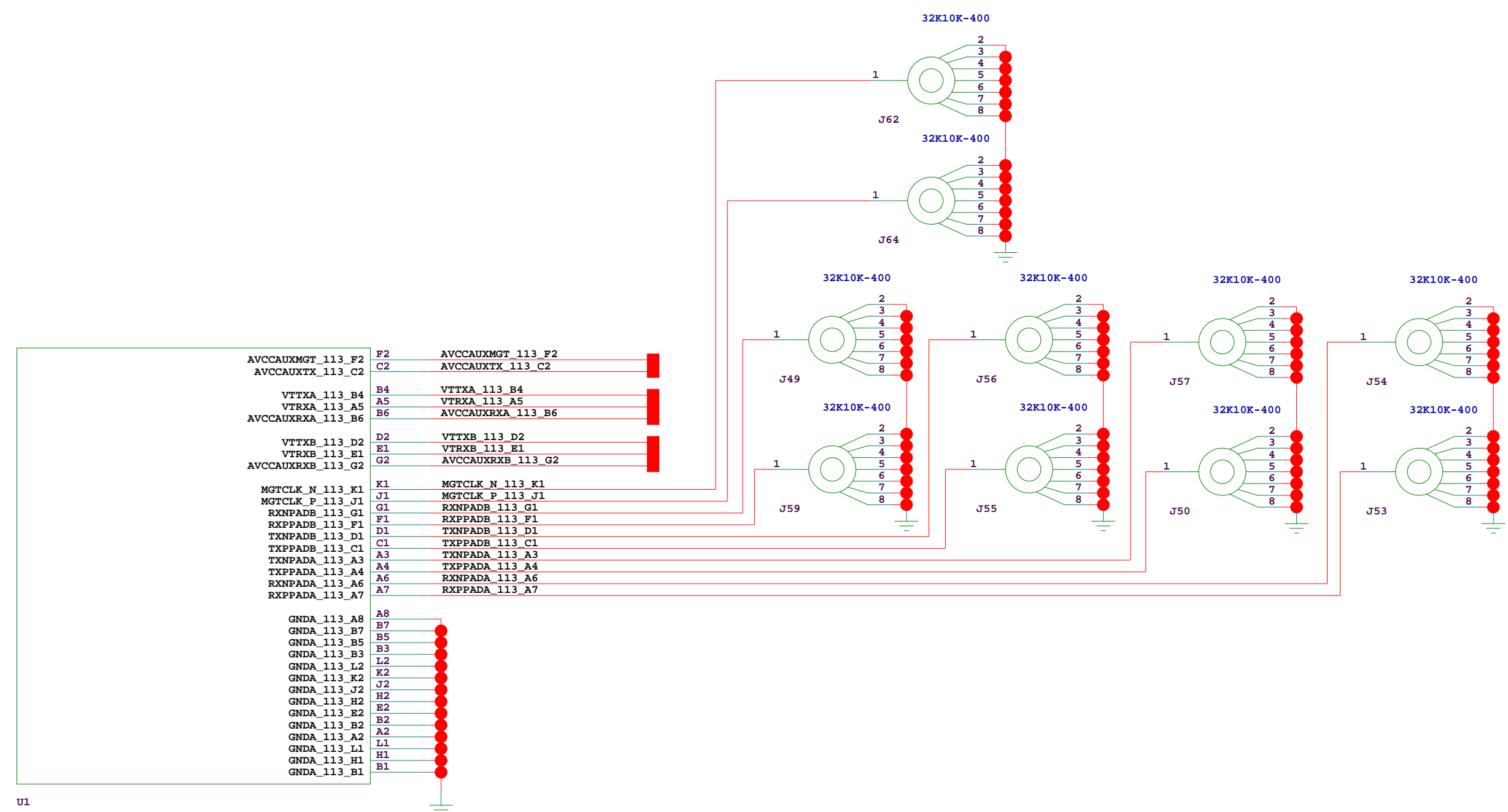


RS232

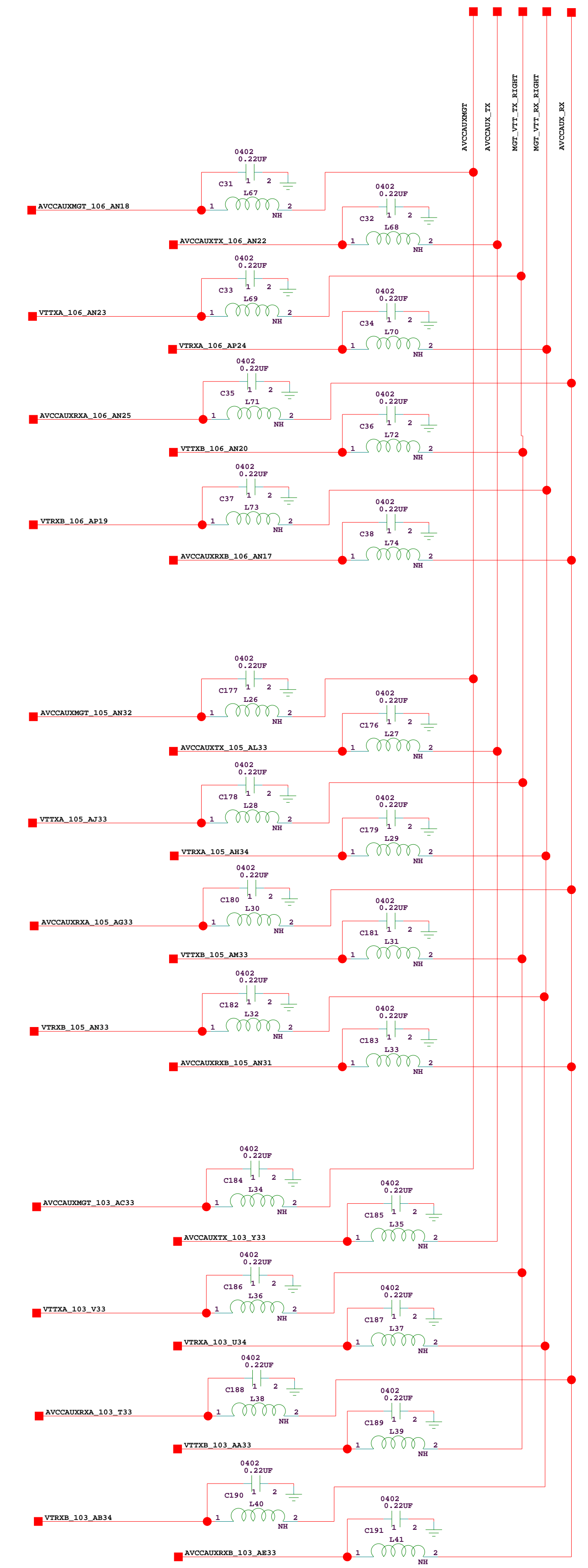
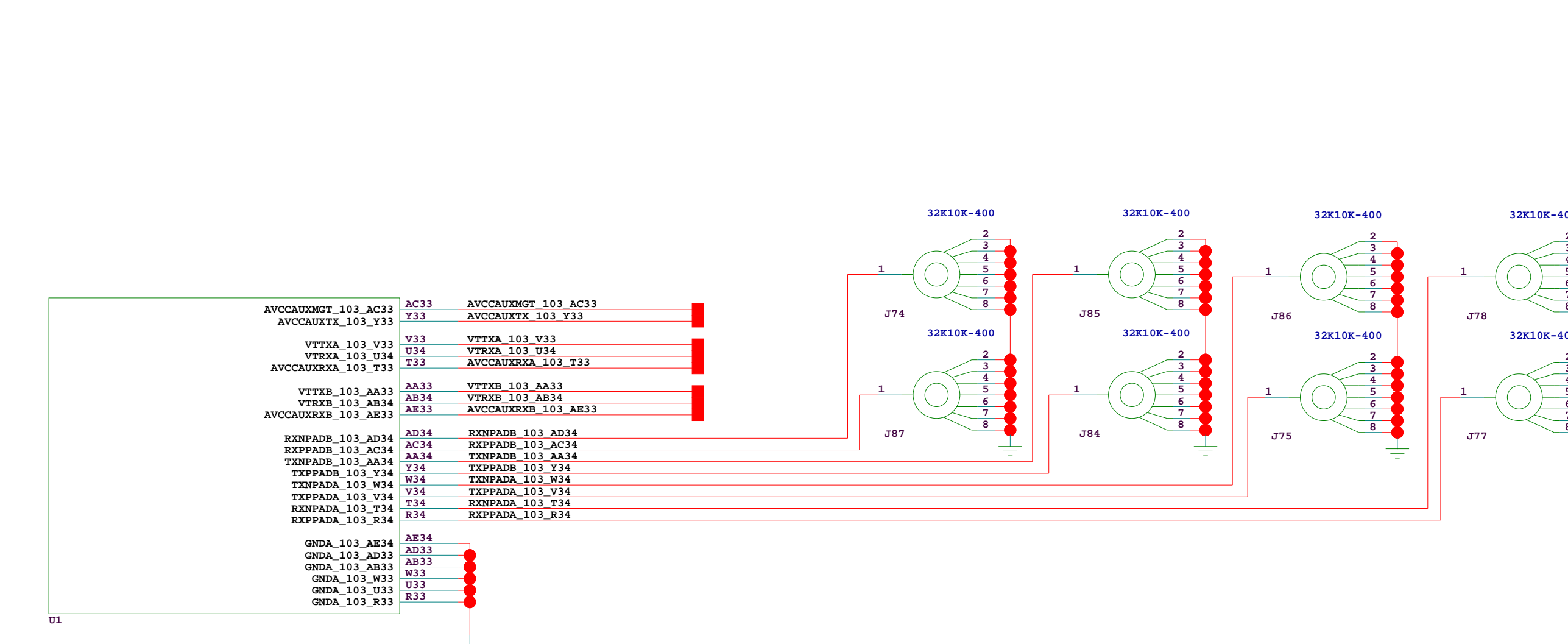
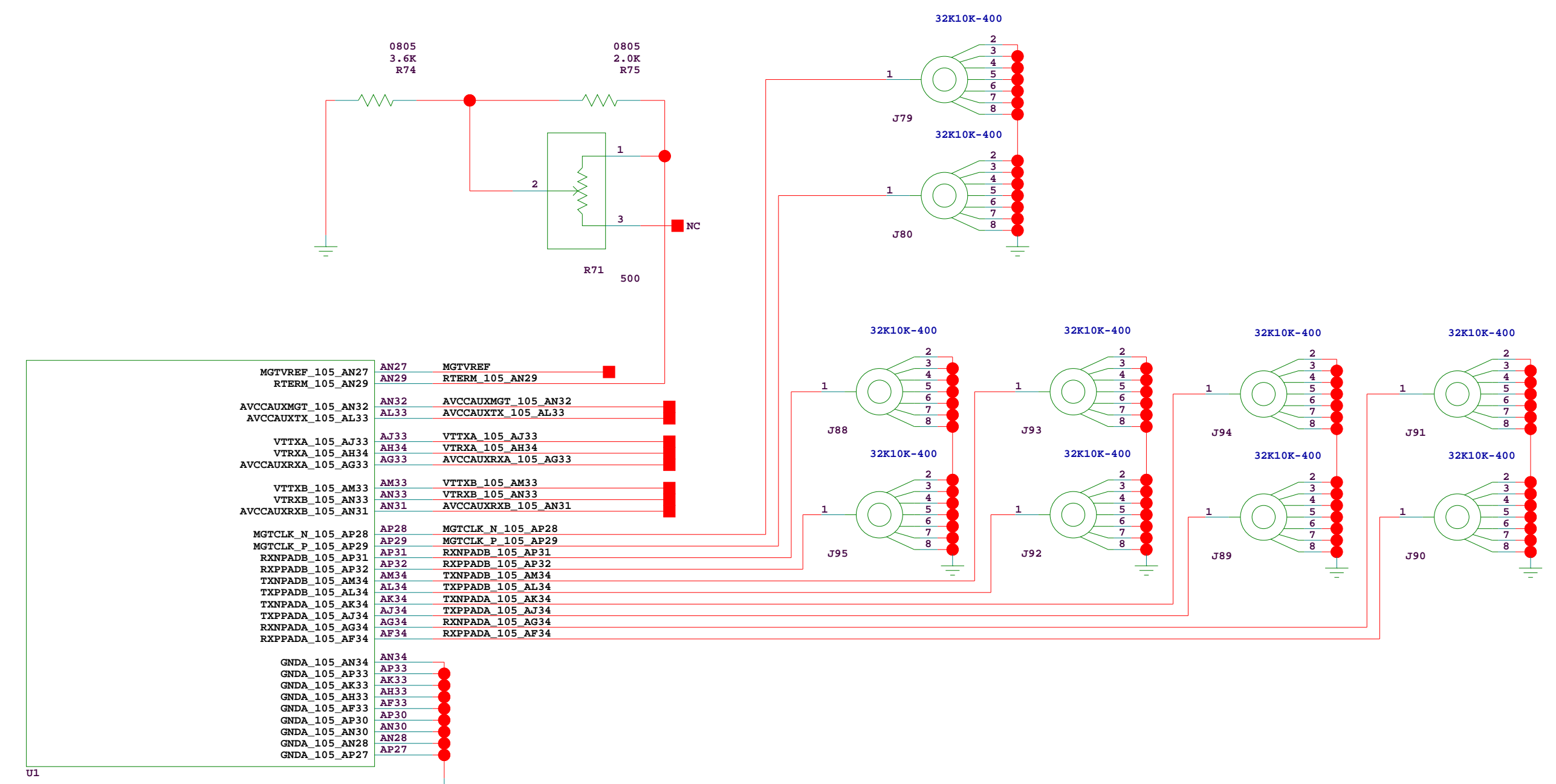
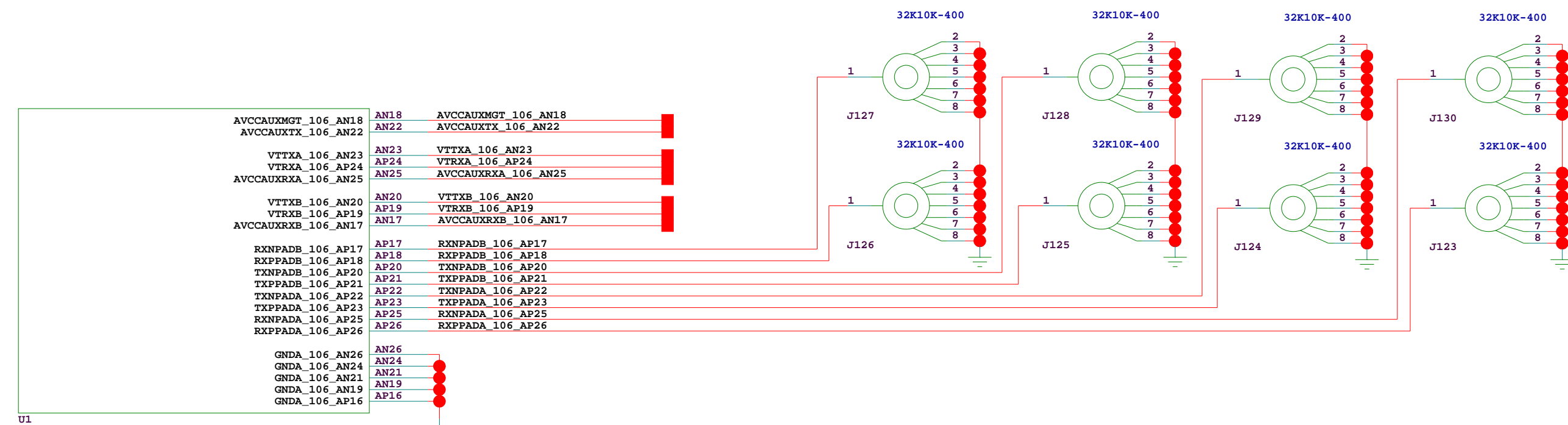


System Ace / UART / Configuration Pins

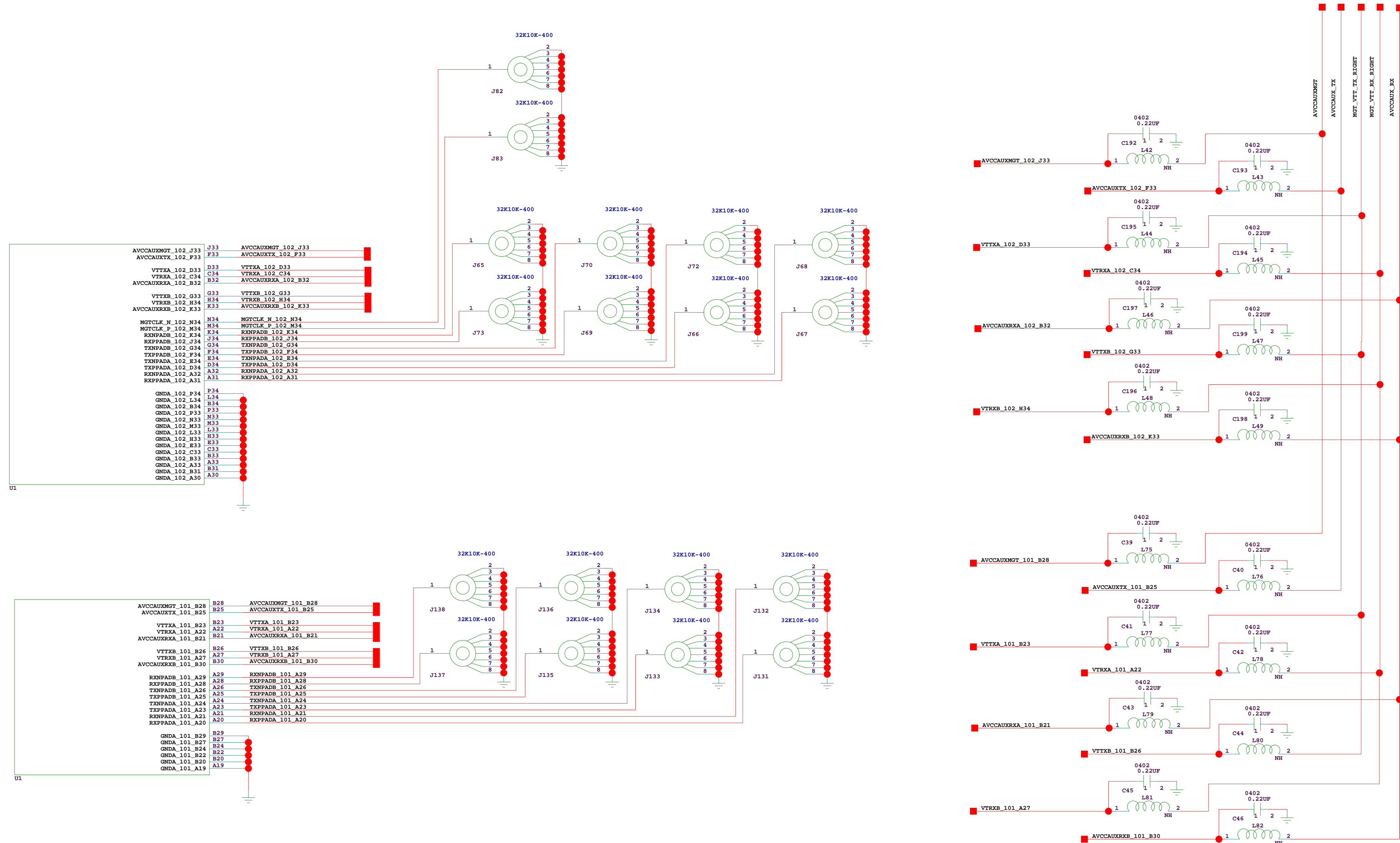




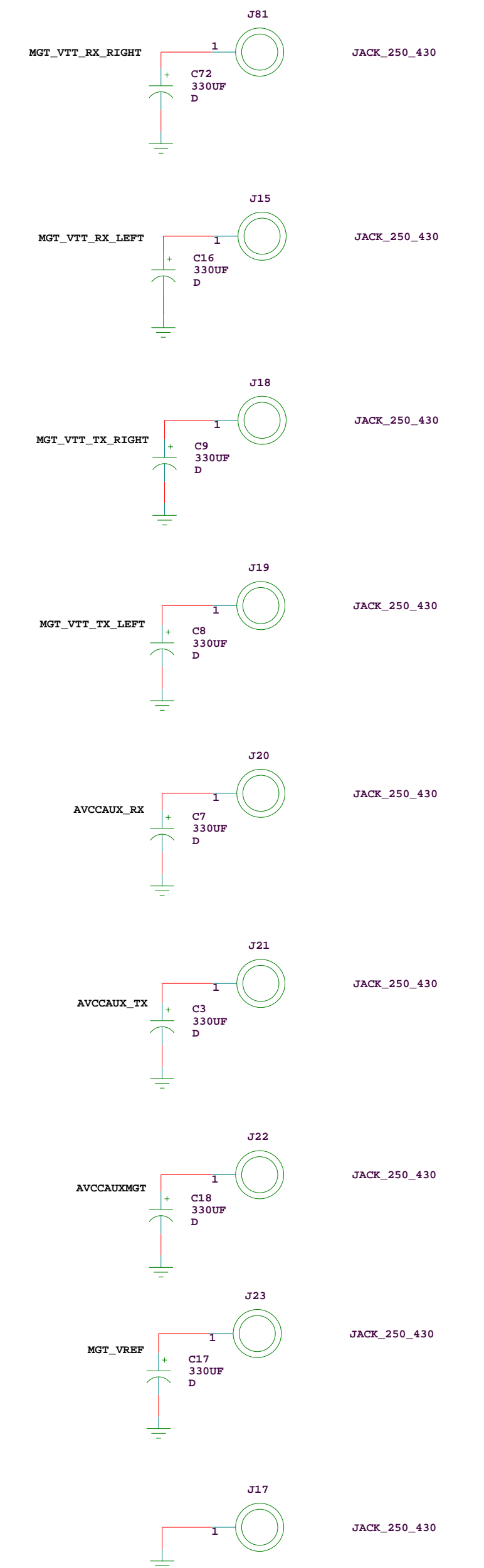
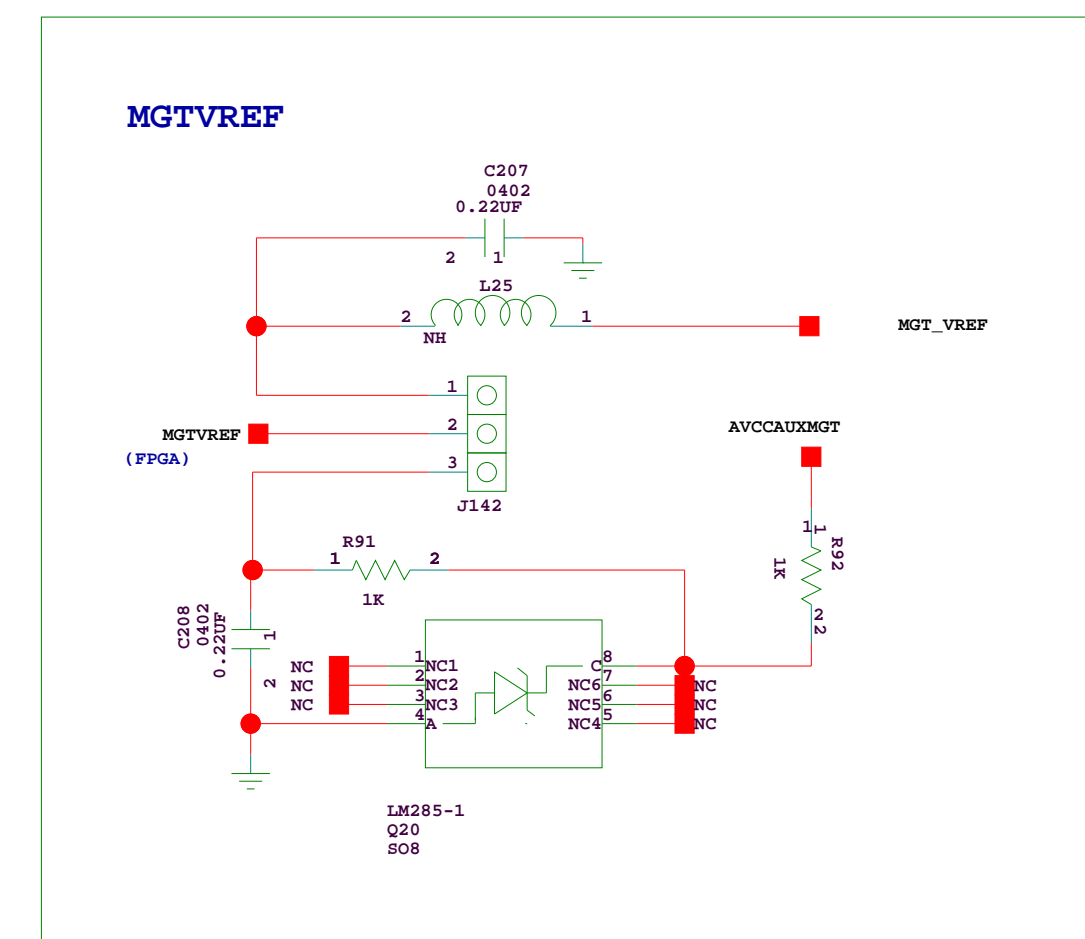
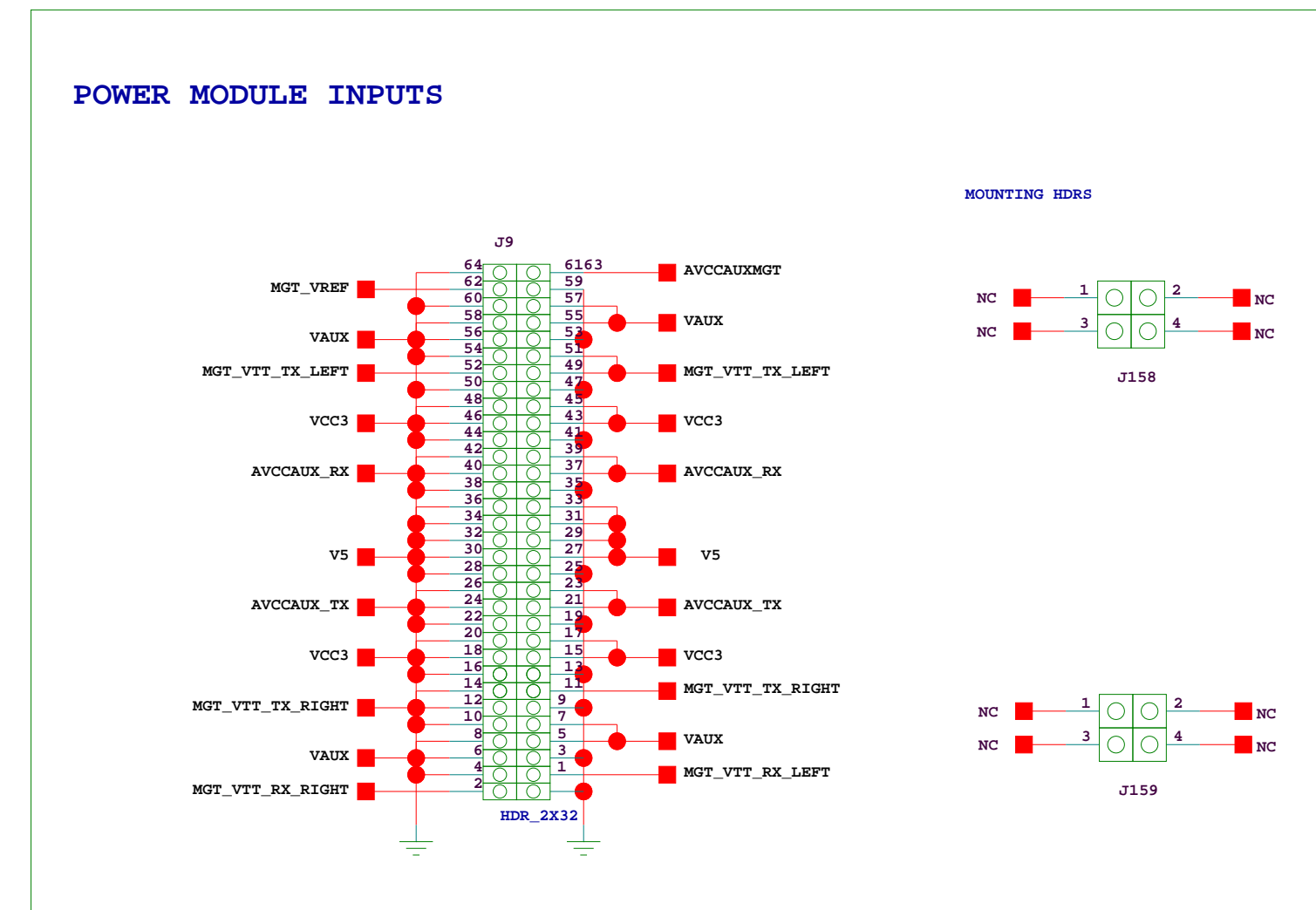
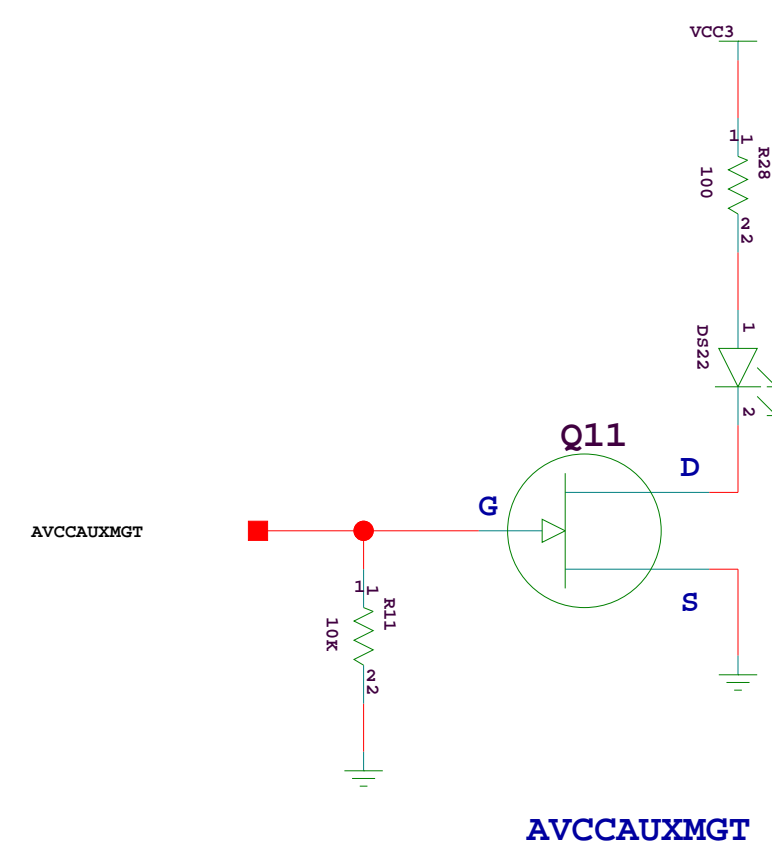
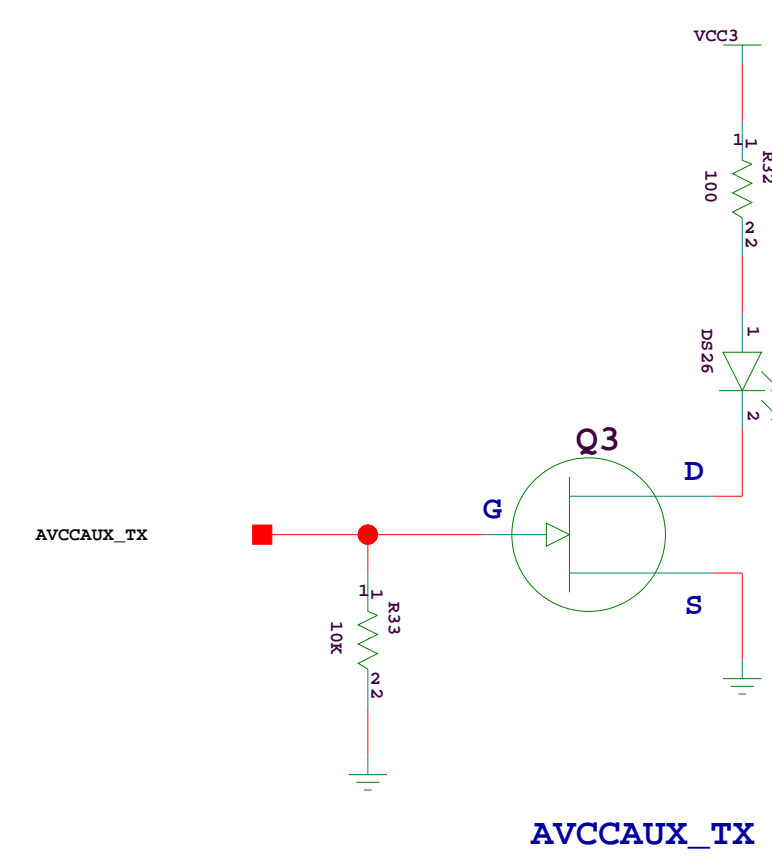
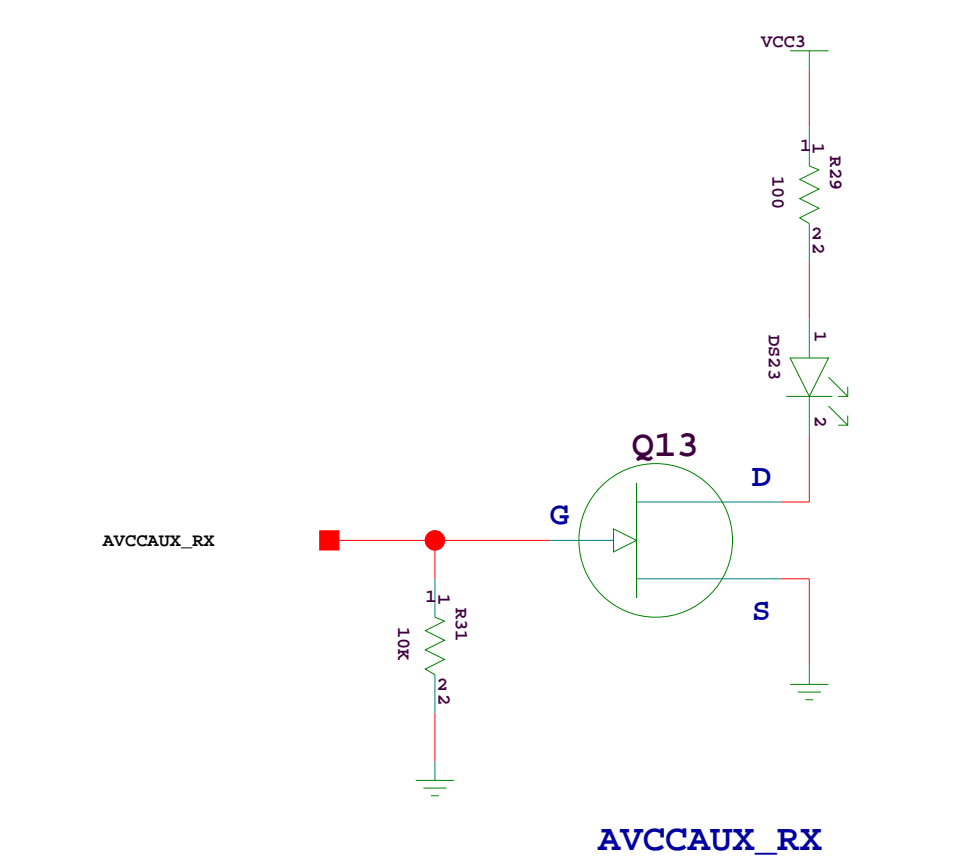
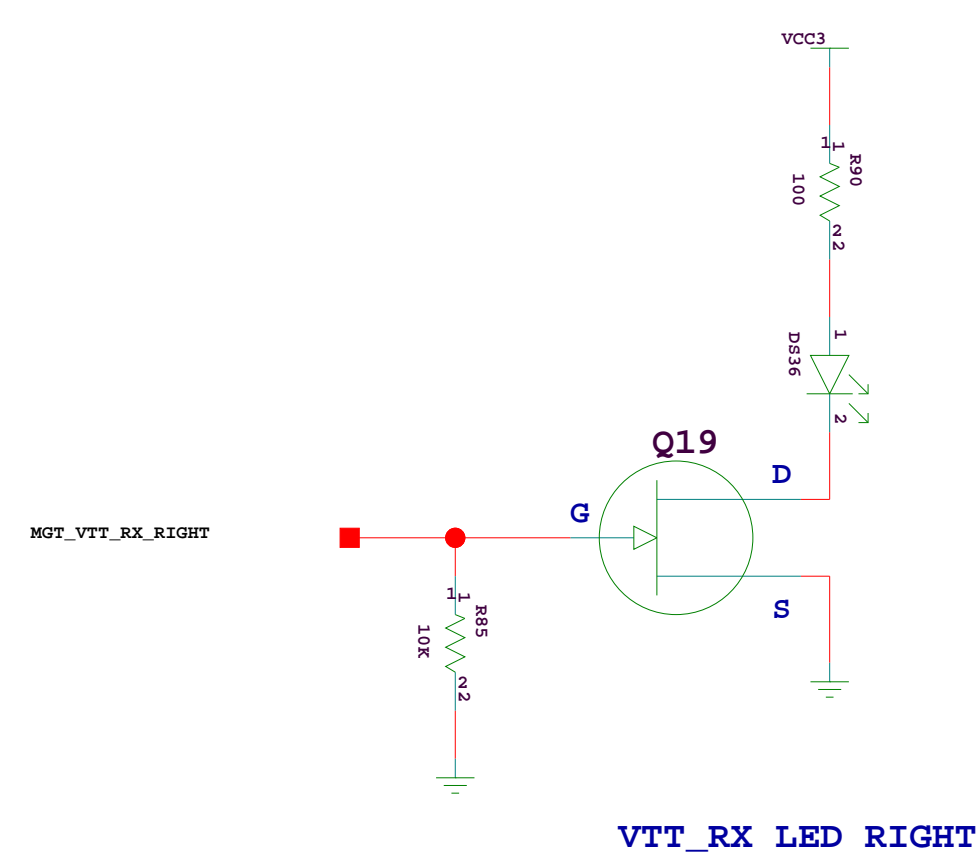
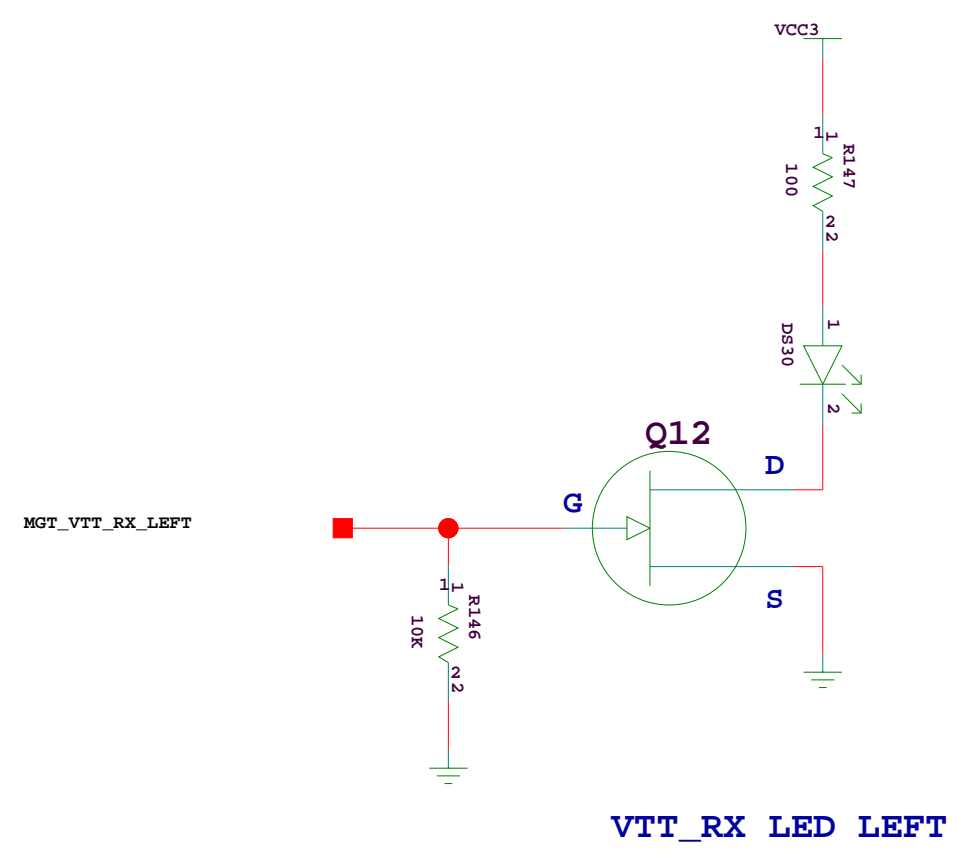
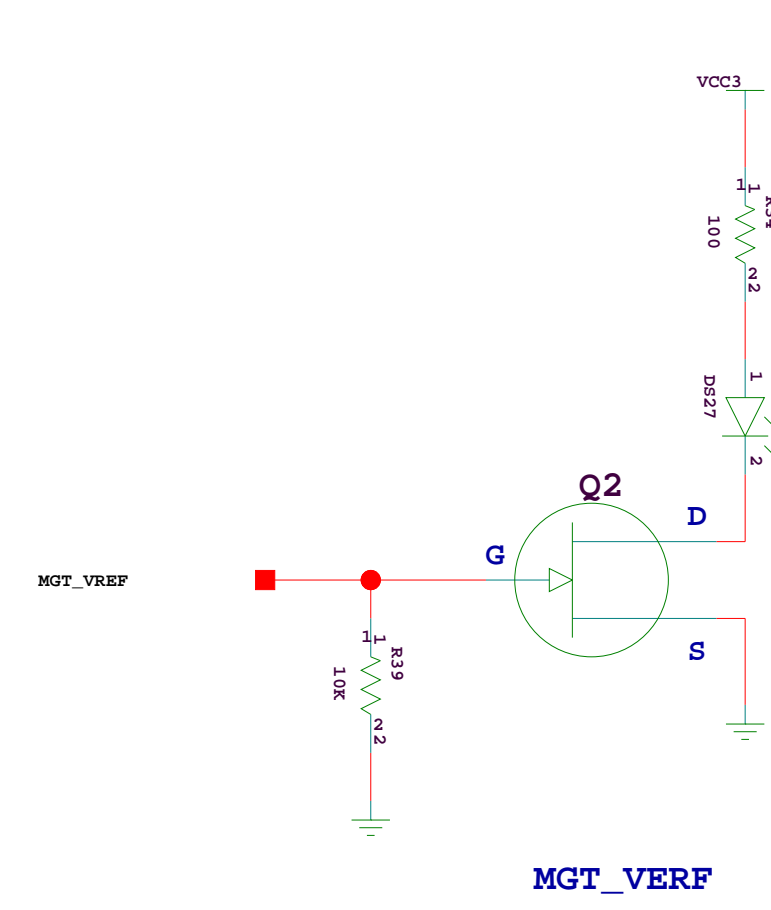
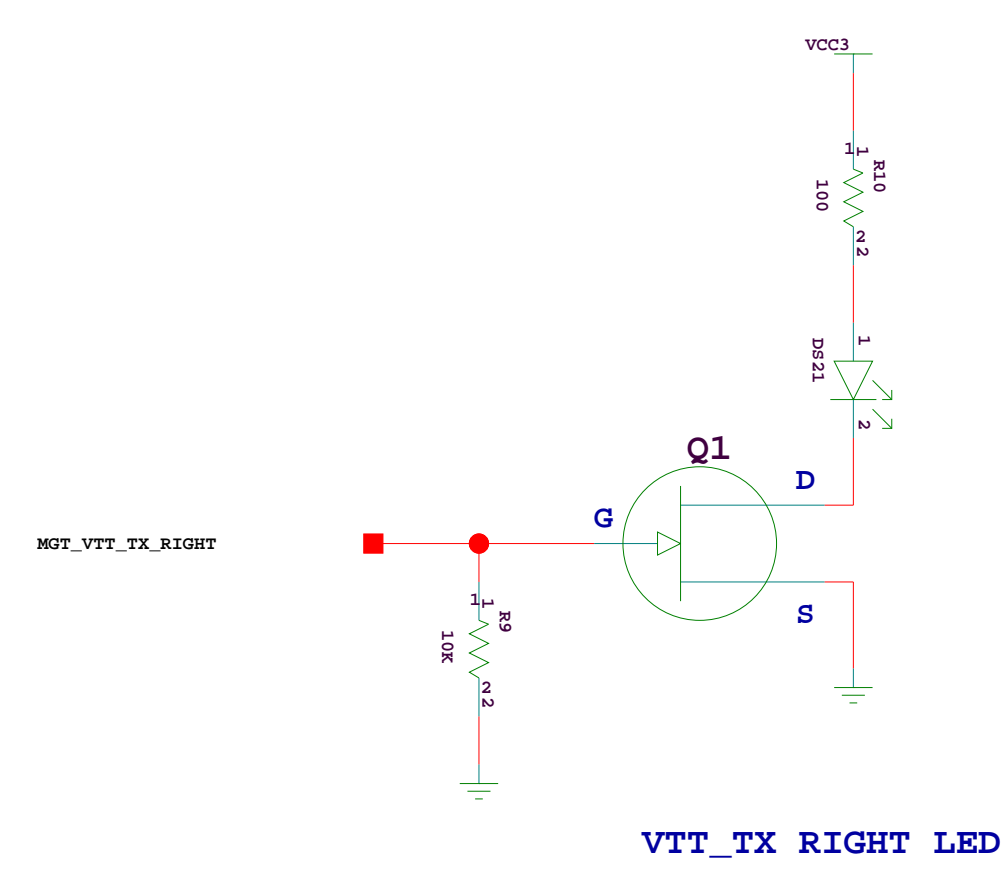
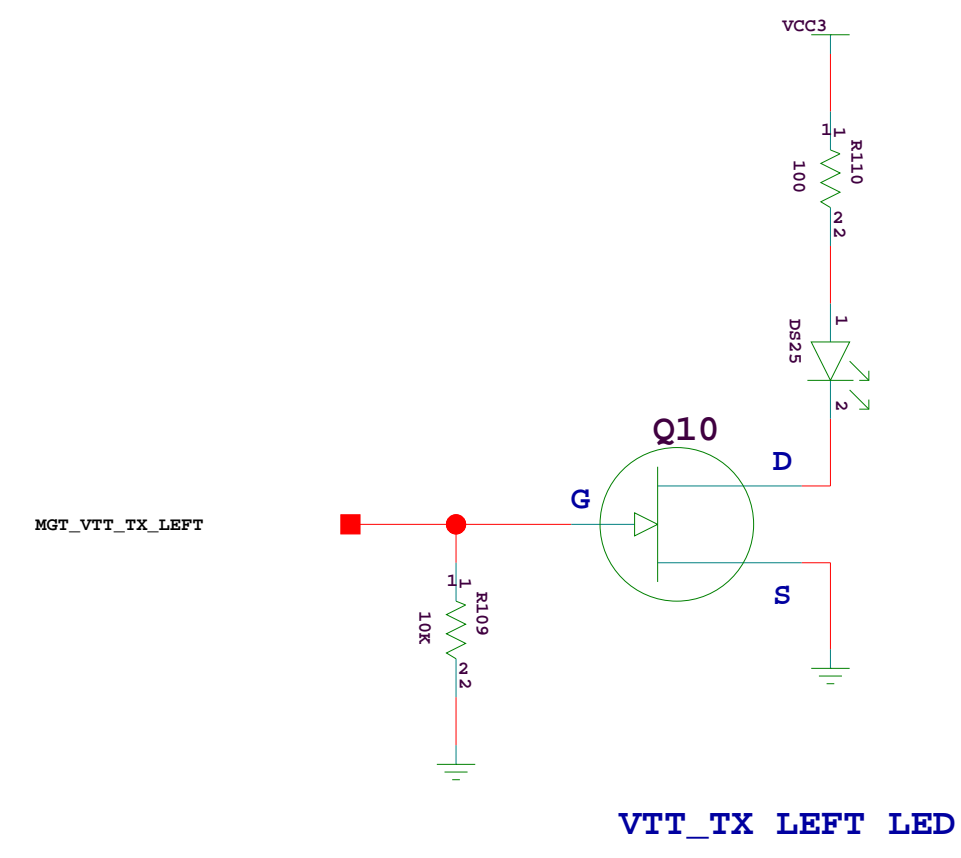
MGTS RIGHT SIDE



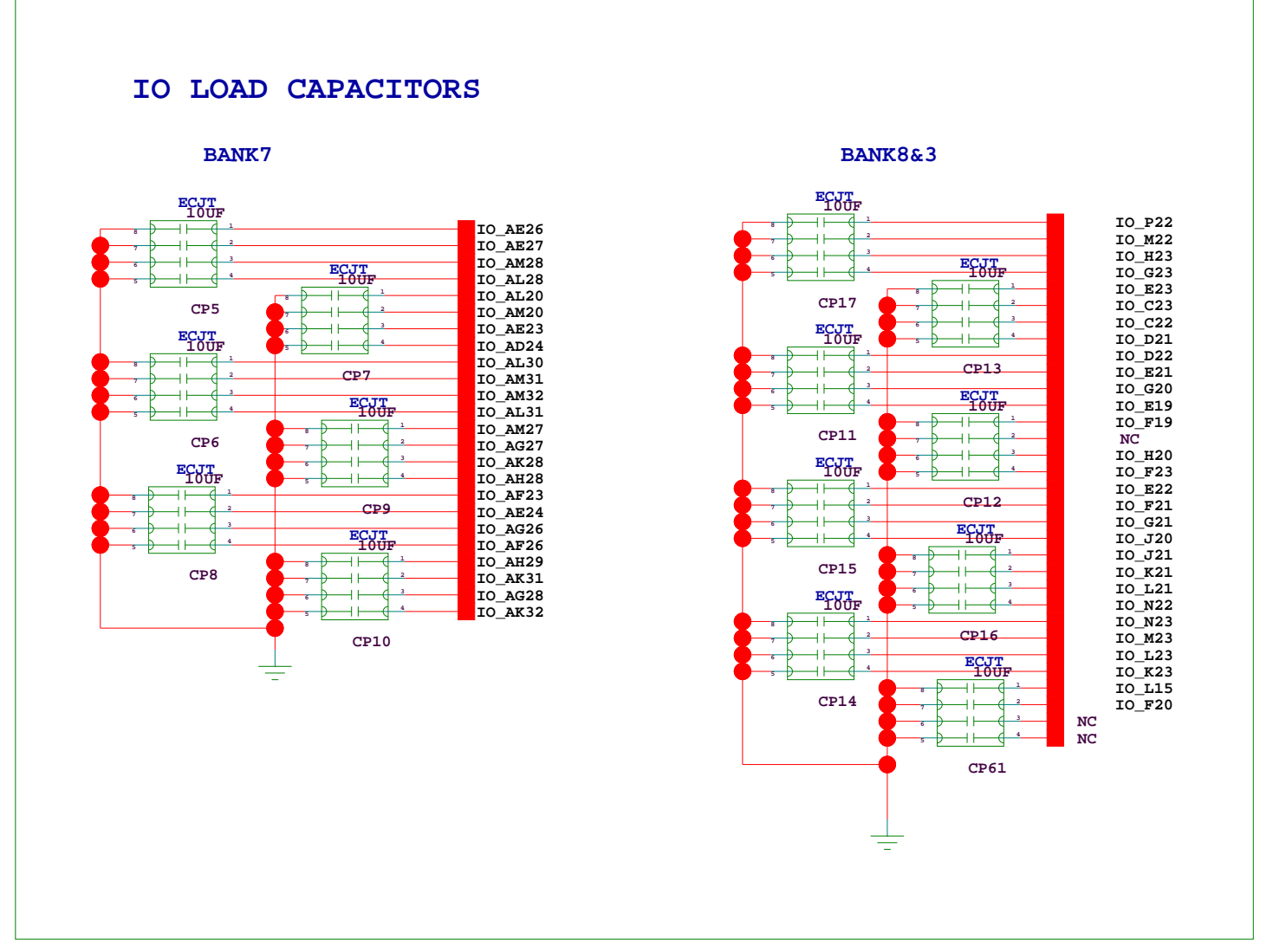
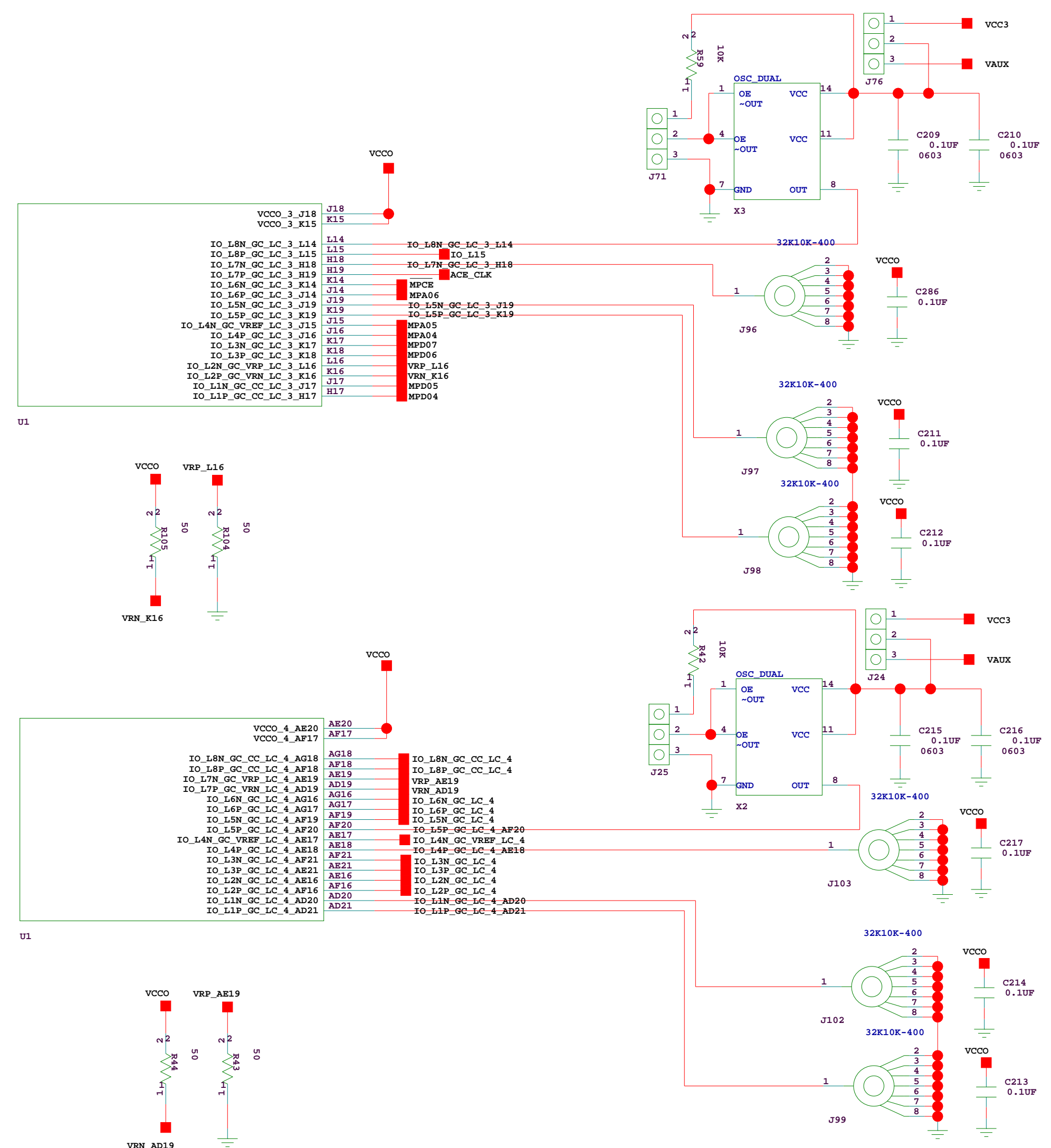
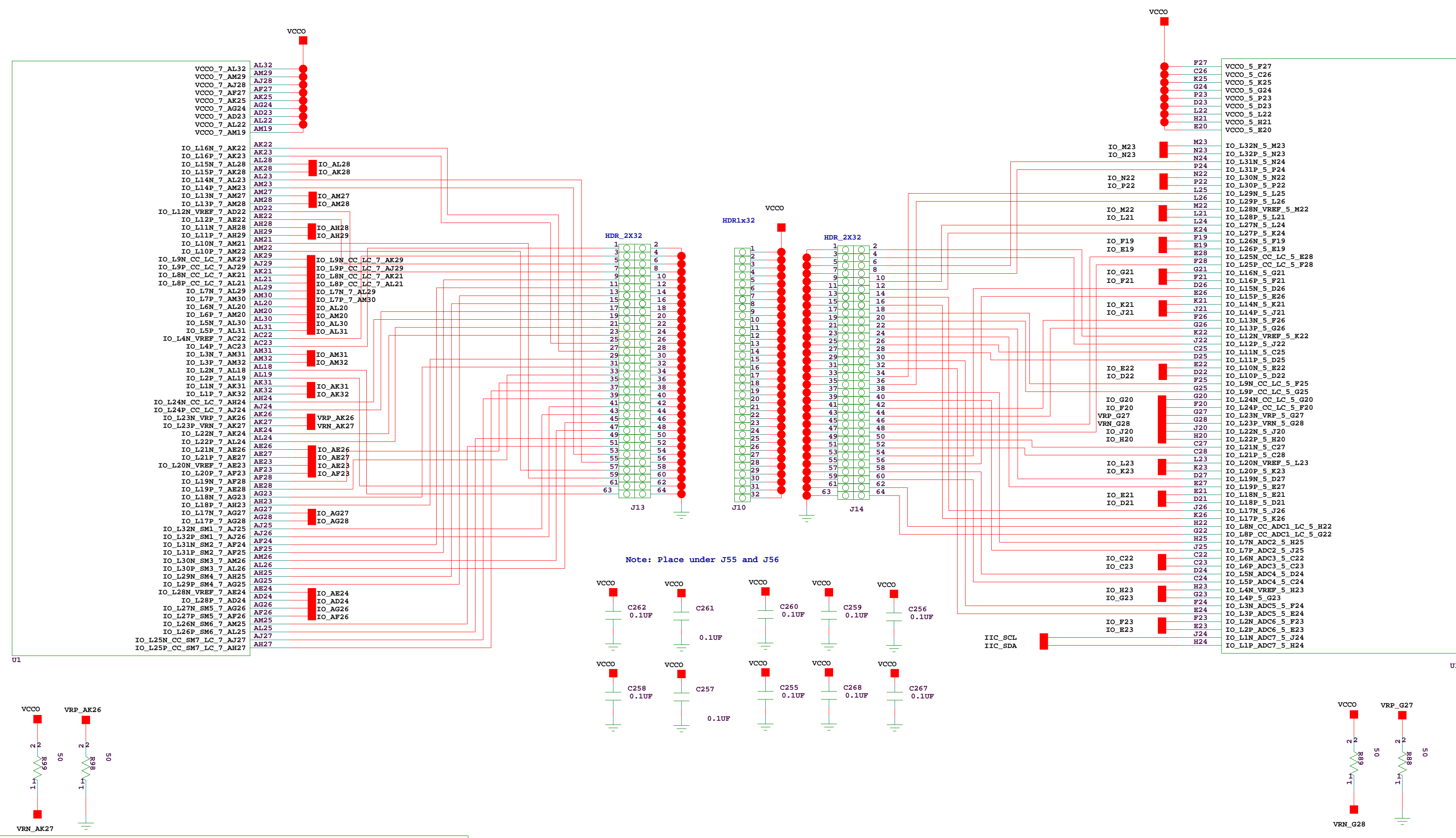
MGTs LEFT SIDE



MGTs LEFT SIDE



Rocket I/O Power Supply Module



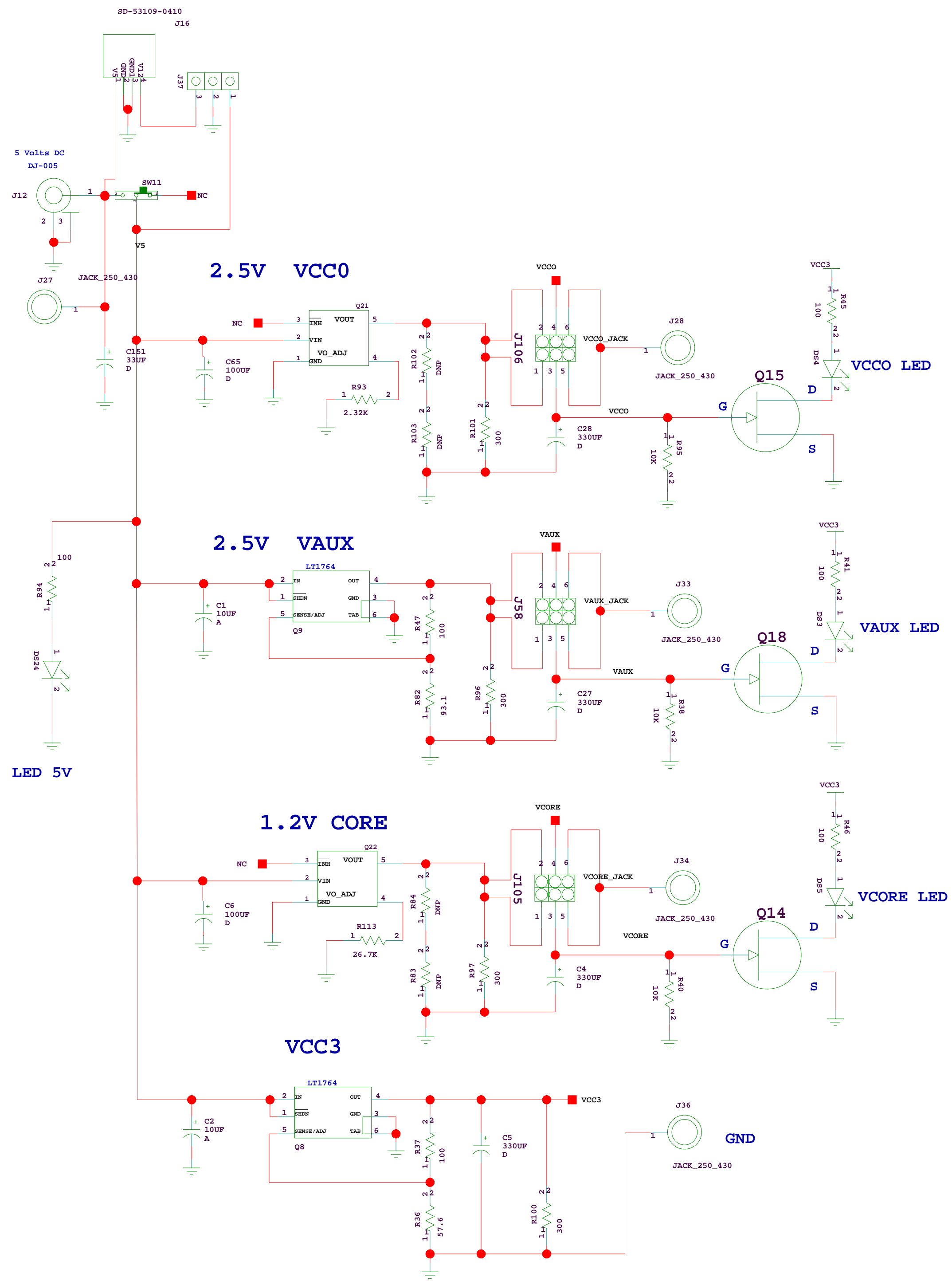
GLOBAL CLOCKS AND BERT HEADERS

XILINX

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0381190

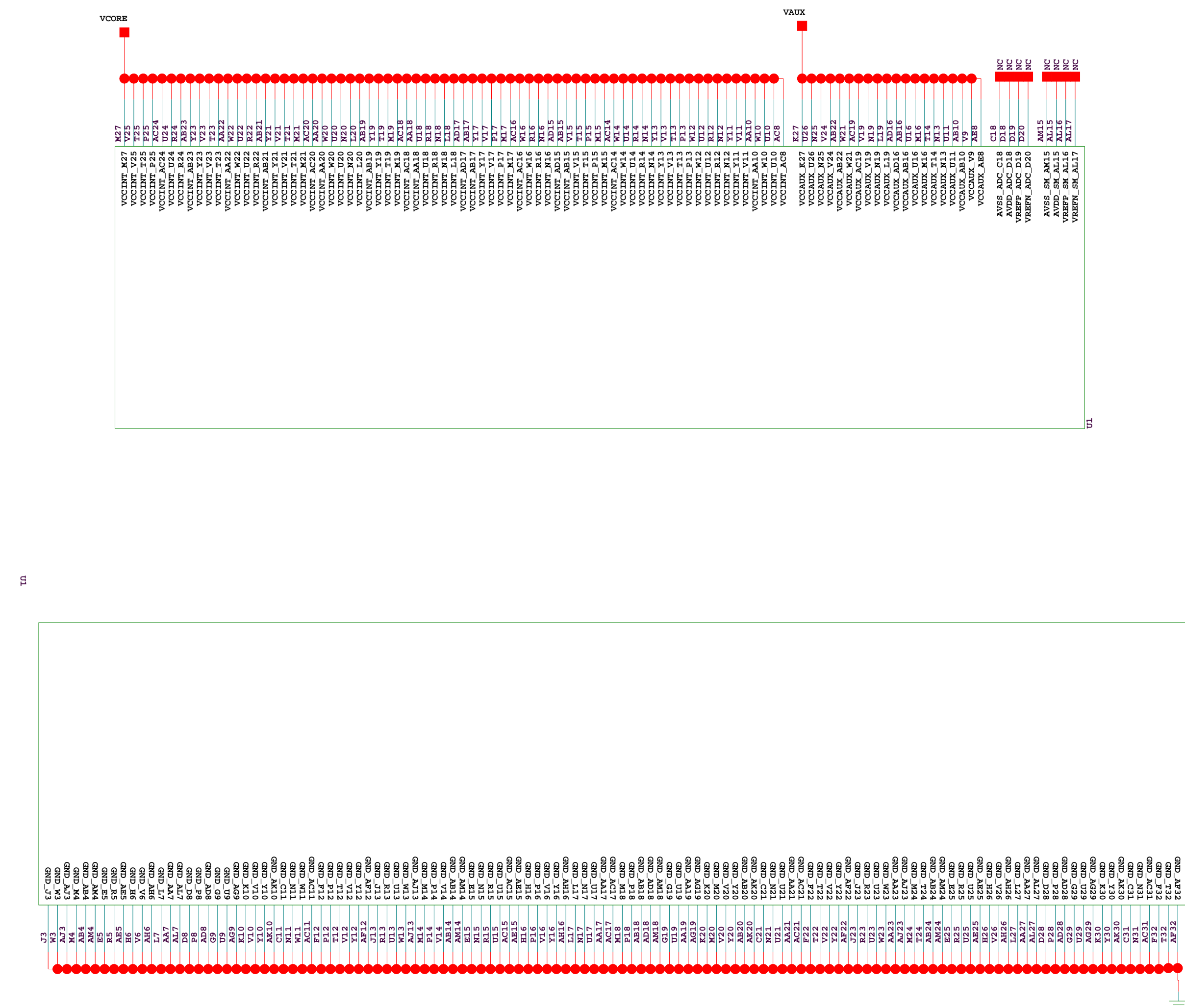
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 Sheet Size: B Rev: 01
 Sheet 8 of 11 Drawn By: B.M/S/S

$$V_{out} = 1.21 (1 + R2/R1)$$

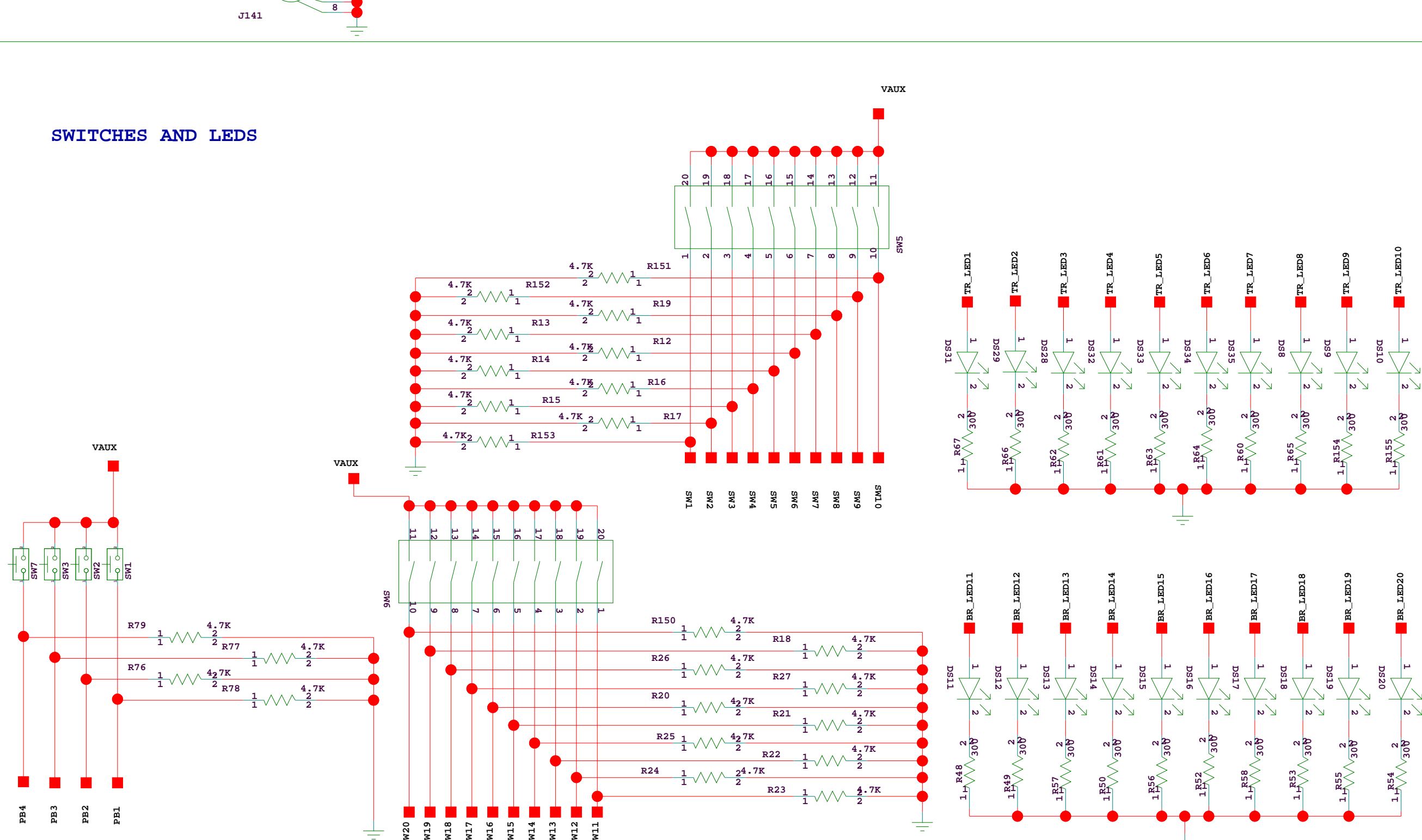
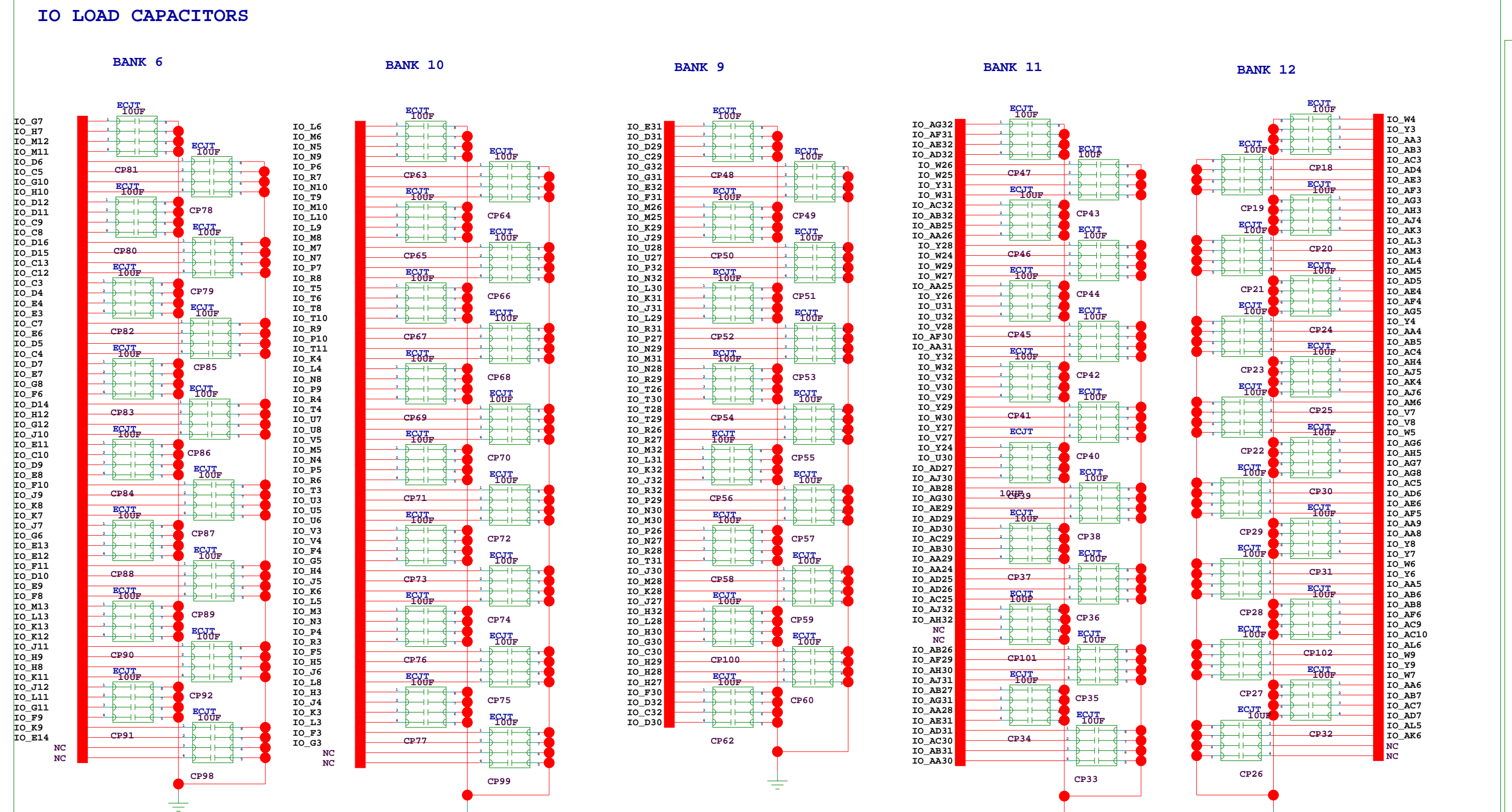
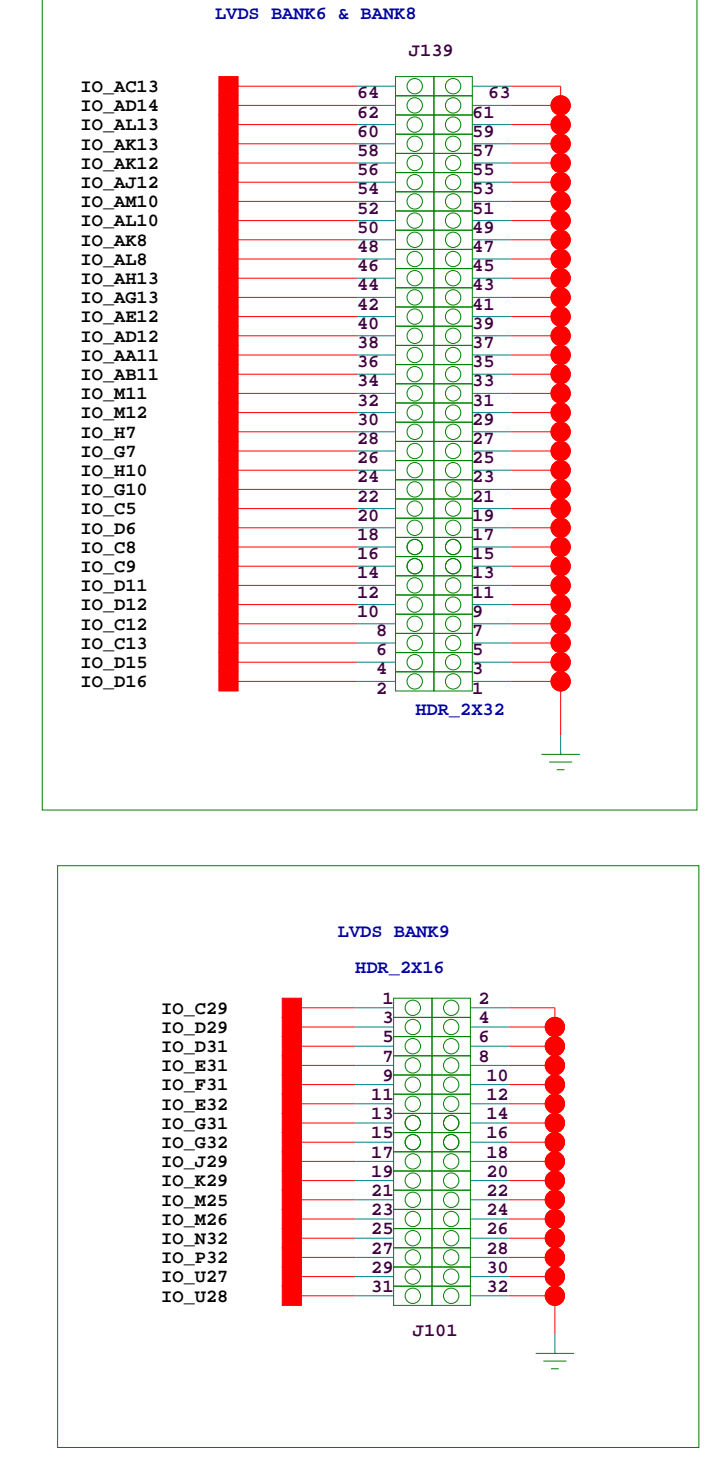
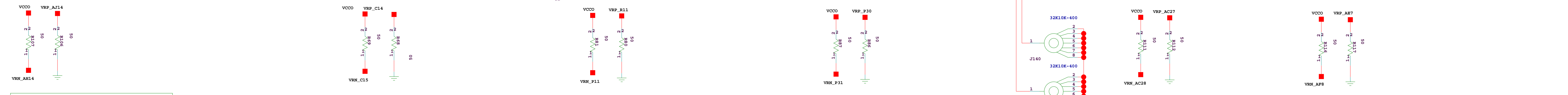
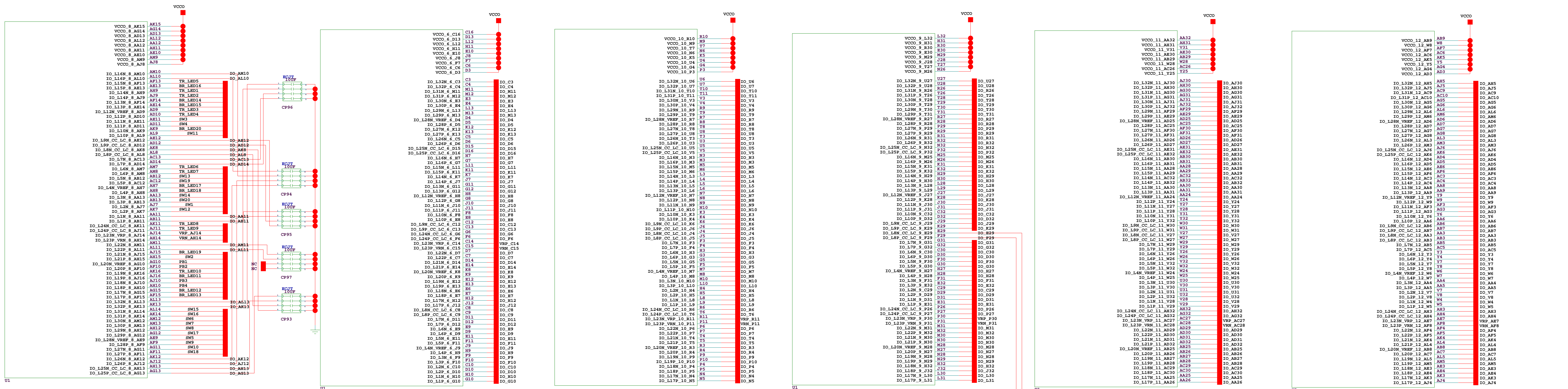


DUT POWER PINS

FPGA Power Supply Section



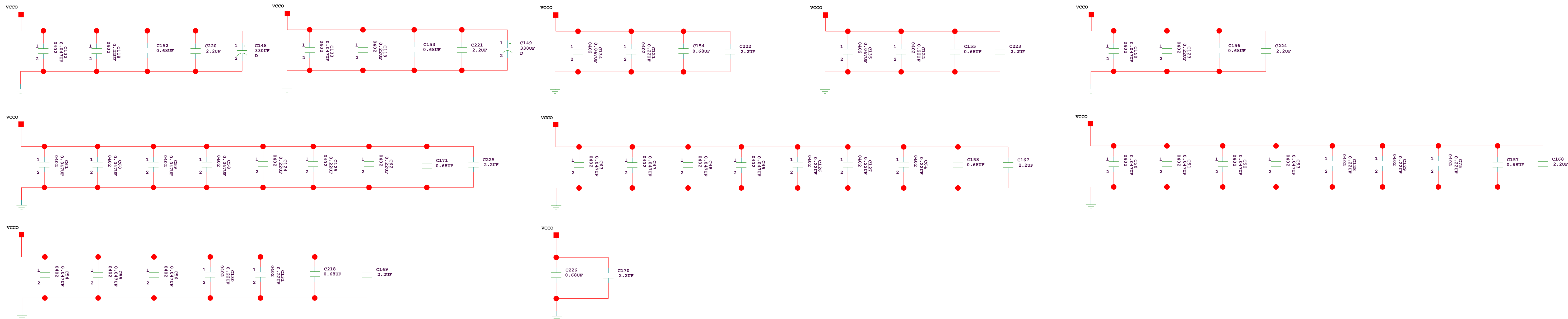
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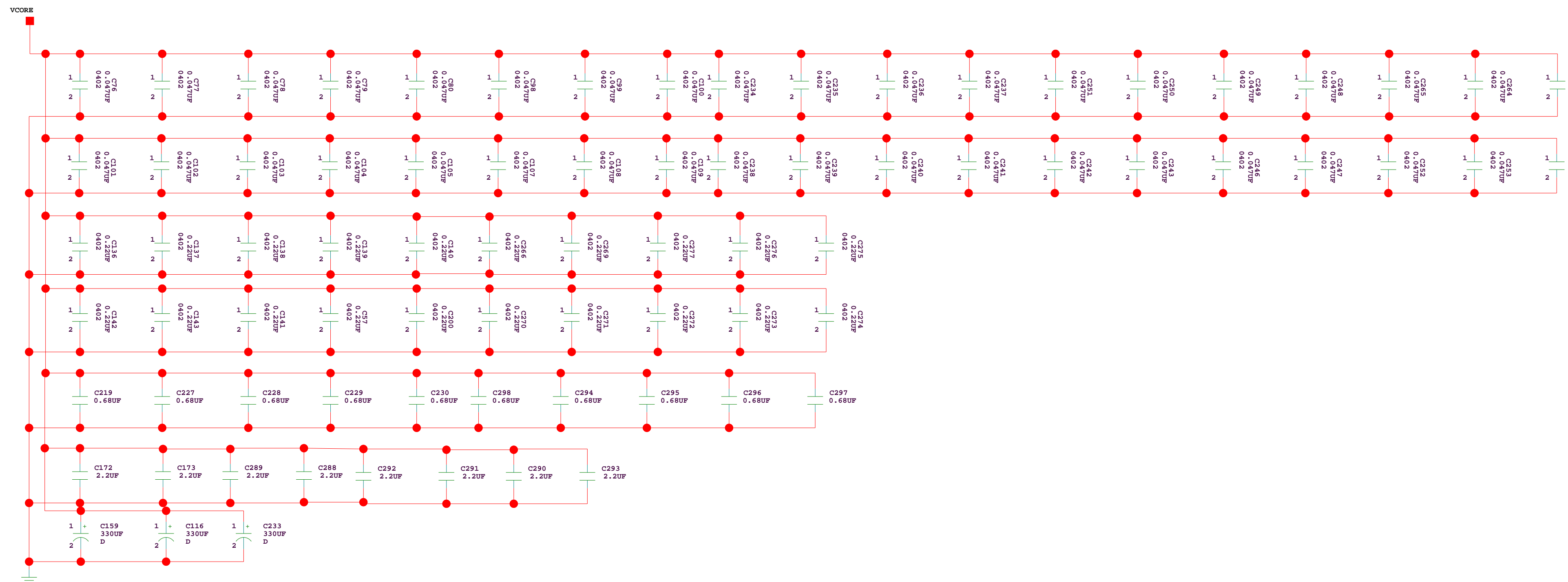
GENERAL PURPOSE SWITCHES AND LEDS

U1 DECOUPLING

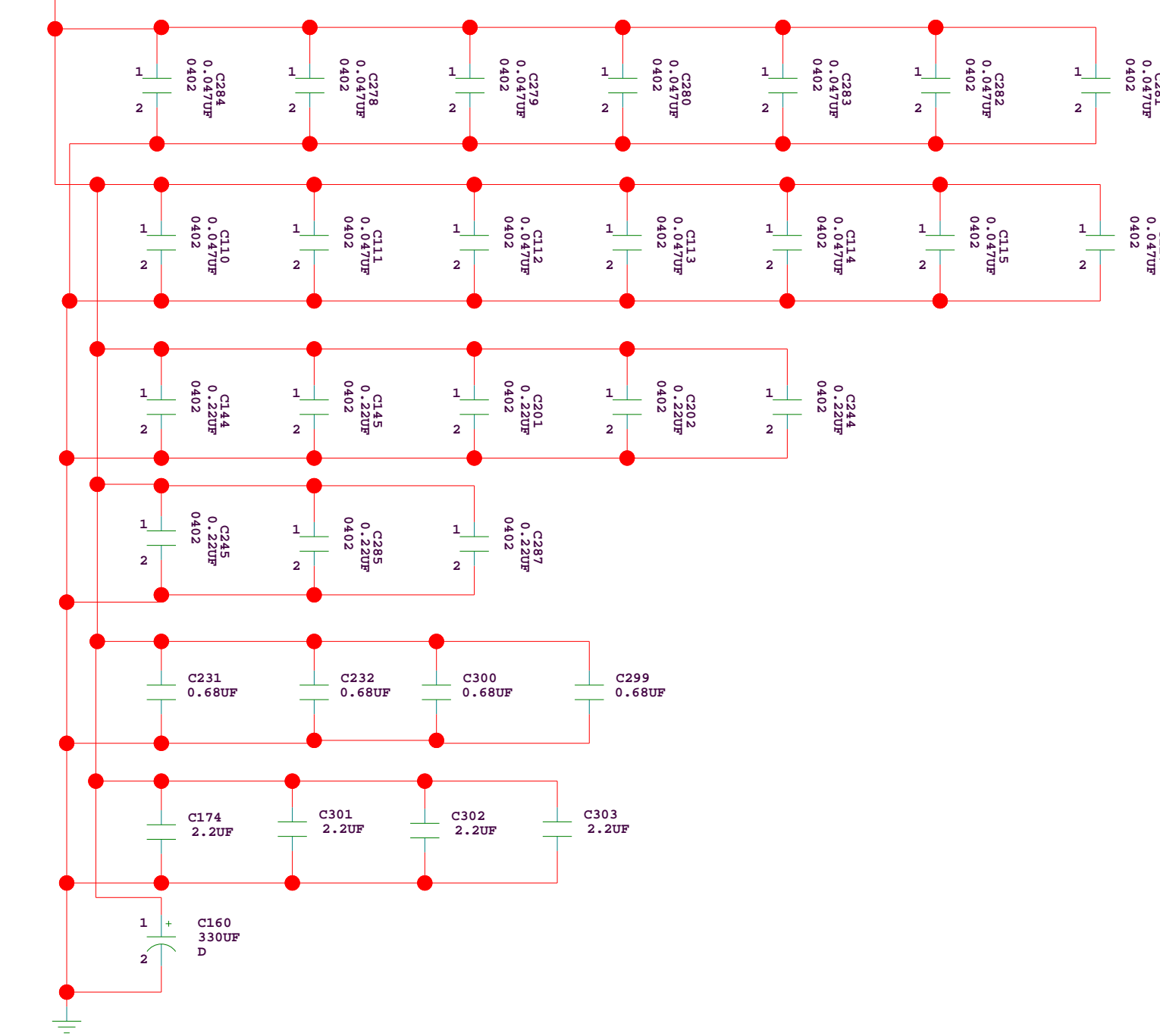
U1 VCCO BANK DECOUPLING



U1 VCCINT DECOUPLING



U1 VCCAUX DECOUPLING



DECOUPLING CAPACITORS

Title: Schematic, ROHS COMPLIANT, ML423 PF1152, 1280358	
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Sheet Size: B	Rev: 01
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