MAX77752
Programmer's Guide

UG6627; Rev 0; 3/18

Abstract

This programmer's guide complements the data sheet for the MAX77752. Whereas the data sheet provides detailed descriptions of the MAX77752 hardware and electrical specifications, this document focuses on register descriptions and provides general advice for programmers

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Overview

The MAX77752 provides multiple step-down regulators, flexible power sequencing, and external regulator enables in a compact package for applications where size is critical. While the data sheet for the device goes into detail describing the hardware and electrical characteristics of the device, this programmer's guide focuses on register descriptions and provides general advice for programmers.

Reset Values

The table below provides a quick summary of reset values based on the One-Time Programmable (OTP) version. See the table at the end of this document for a full list.

Table 1: Reset Values Summary Table

Register	MAX77752A	MAX77752B
CID4	0x07	0x0D
GLBL_CNFG1	Reset threshold = 2.65V	Reset threshold = 2.85V
GLBL_CNFG2	Brownout threshold = 2.8V	Brownout threshold = 2.9V
OTP_PHUP_1	Master mode	Slave mode
	Enable pull-up resistors to all logic pins	Enable pull-up resistors to all logic pins
INRUSH_OPTION	Inrush function selected	Inrush function selected
BUCK1CNFG1	Buck 1 Out = 1.8V	Buck 1 Out = 1.8V
BUCK2CNFG1	Buck 2 Out = 1.350V	Buck 2 Out = 1.200V
BUCK3CNFG1	Buck 3 Out = 1.05V	Buck 3 Out = 0.9V
LDOCNFG1	LDO Out = 1.800V	LDO Out = 1.875V

Global Resources

Register Reset Conditions

SYS Undervoltage Lockout Comparator (SYSUVLO_F_I)

When V_{SYS} falls below $V_{SYSUVLO}$, SYSUVLO is asserted and the On/Off controller forces a system reset. The reset disables all functions of the power management integrated circuit (PMIC), shutting down the central bias and clocks. Check for this event with the SYSUVLO_F_I flag bit in the GLBL_INT1 register.

System Reset Comparator (SYSRSTTH and SYSRSTHYS)

In addition to the fixed POR and undervoltage thresholds, there is a programmable system reset threshold, or VSYS_RST, that generates an internal SYSGOOD signal. The threshold is programmable through SYSRSTTH[3:0] and hysteresis through SYSRSTHYS[1:0], both of which are in the GLBL_CNFG1 register.

- SYSGOOD Assertion
  - SYSGOOD is asserted when VSYS is above the rising VSYS_RST threshold. This triggers the On/Off controller to trigger the power-up sequence.
- SYSGOOD De-Assertion
  - When VSYS falls below the VSYS_RST threshold, SYSGOOD is de-asserted, which triggers the On/Off controller to initiate a power-down sequence.
  - The event is also recorded in the SYSRST_F_I flag in the GLBL_INT1 register.
  - In the GLBL_INTM register, use the SYSRST_F_M bit to mask SYSRST_F_I in the GLBL_INT0 register and to mask the event itself from causing a power-down sequence. See the PGOOD Logic Diagram (Figure 1) for details.

System Brownout Comparator (SYSBO)

In the GLBL_CNFG2 register, program the system brownout comparator with SYSBOTH[3:0] and its hysteresis with SYSBOHYS[1:0]. The brownout comparator's threshold is meant to be programmed higher than the SYS reset threshold. The SYS brownout comparator issues an early warning indication to the system controller of a falling supply voltage, so the system can react appropriately before power fails.

- SYSBO Assertion
  - When the system voltage falls below the falling brownout threshold ($V_{SYS} < V_{SYSBO\ (FALLING)}$), SYSBO is asserted. This causes the external PGOOD output to de-assert (LOW) immediately.
  - If the brownout timer is enabled (setting the T_BO_EN bit in the GLBL_CNFG0 register), the system voltage is allowed a certain time period (t_{BO}) to recover above the rising brownout threshold. If the timer expires and the system voltage has not recovered, the On/Off controller initiates a power-down sequence.
  - If the brownout timer is disabled, no further action is taken in addition to the de-assertion of the PGOOD output.
  - The event is also recorded by the SYSBO_F_I flag in the GLBL_INT1 register.

- SYSBO De-Assertion
    - When the system voltage rises above the rising threshold ($V_{SYS} > V_{SYSBO\ (RISING)}$), SYSBO de-asserts. This results in the external PGOOD output being allowed to assert (HIGH). Note that PGOOD is also controlled by other events. See the PGOOD Logic Diagram (Figure 1), for more details.

Thermal Monitor (TOLVD)

TOVLD is recorded in the TOVLD_I flag in the GLBL_INT1 register.

Chip Identification (CID)

The chip identification feature allows software to recognize different revisions of the MAX77752. When contacting Maxim for assistance with a given device, you might be asked for the values of the CID registers. Note that the serial number contained in CID0, CID1, and CID2 might not be unique for each device; however, the serial number, purchase order, top mark, and date code can improve Maxim's ability to provide customer support.

PGOOD Output (PG_DLY)

- During a power-up sequence, PGOOD is asserted once the power up sequence is complete and the internal PGOOD signal (PGOOD_INT which denotes the POK status of all regulators as well as the system voltage) is asserted. There is an assertion delay programmed by PG_DLY[1:0] in the GLBL_CNFG3 register. Refer to the power-up sequence example timing diagram (Figure 5) for details.
- PGOOD is always left asserted including in the DevSlp state.
- PGOOD can de-assert at any time if a regulator's undervoltage (UV), overvoltage(OV), or overcurrent (OC) (overcurrent only for Bucks) status signals assert and they are unmasked. Refer to the PGOOD Logic Diagram (Figure 1) below for complete details.

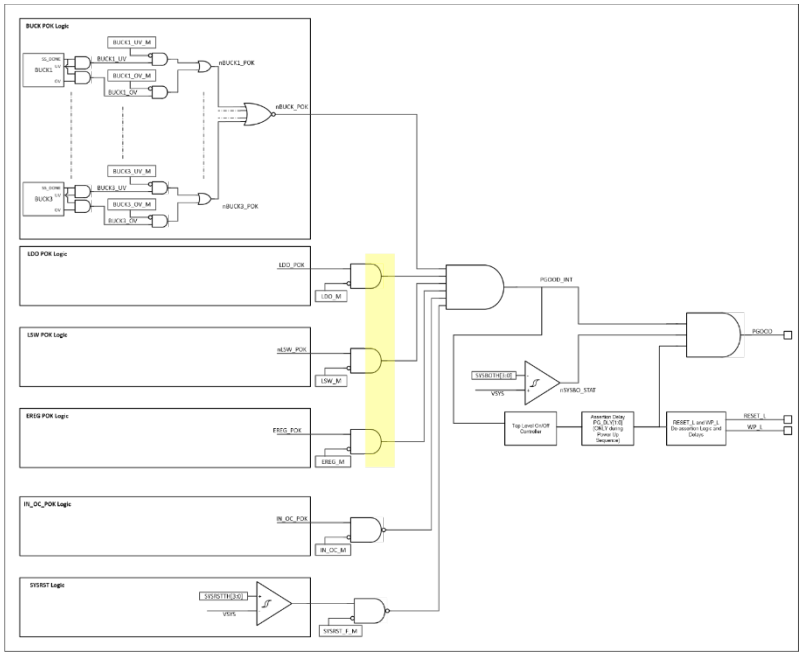

Figure 1. PGOOD logic: Different POK signals, their masks, and the overall PGOOD signal.

Low Power (OTP_PHUP_1)

This device supports Low Power mode and DevSlp mode, to further reduce power consumption when the system itself is entering a sleep state. Low Power mode implies the regulators' (BUCK1, BUCK2, BUCK3, etc.) behavior in low power; DevSlp mode implies the On/Off controller's behavior in low power. Depending on the OTP option, certain rails can be powered down and Buck 3 might transition to its Low Power mode voltage. Controllers can use three pins depending on whether the PMIC is configured to be in Master mode or Slave mode.

If this device is in Master mode, the application uses the LP_MODE, LP_REQ, and LP_ACK pins. Otherwise, if the device is in Slave mode, only LP_ACK is used.

The OTP_SLP_MSTR_SLV bit in the OTP_PHUP_1 register configures the mode as follows:

- 0—Master mode
- 1—Slave mode

See the Reset Value Reference Table (Table 7) at the end of this document to determine whether your device is in Master mode or Slave mode.

LP_MODE Input

If this device is in Slave mode, then the LP_MODE input is a "don't care" and can be left unconnected or tied high or low.

LP_MODE is the pin that the controller uses to make a Low Power mode request to the MAX77752. After the controller requests Low Power mode, this device sends the same request to other devices it is powering with the LP_REQ pin. The other devices respond to the MAX77752 through the LP_ACK pin.

- LP_MODE is a push-pull input.
- LP_MODE is referenced to the IN_VIO to set its logic high and low thresholds.
- LP_MODE is debounced and sent to the On/Off controller to request entry into DevSlp mode.
- Set this pin high to request this device to enter DevSlp mode.
- Setting LP_MODE low while this device is waiting for acknowledgement (LP_ACK) from other devices aborts entry into DevSlp mode and returns the device to the On state.
- Setting LP_MODE low while the device is already in DevSlp mode triggers the On/Off controller to exit DevSlp mode. It also triggers the LP_REQ de-assertion timer to start.

LP_REQ Output (OTP_INT_PU and ALT_LP_REQ)

LP_REQ is an open-drain output that this device uses to send a Low Power mode request signal to other devices it is powering. Those devices can then acknowledge the request through the LP_ACK pin. See the description above of the LP_MODE pin to learn when the LP_REQ pin is asserted.

In an example application in which one or more rails power down in Low Power mode or DevSlp mode, this device might send a Low Power mode request to a system, letting the system know to finish its tasks or shut down anything it is controlling. Then the system acknowledges this device, letting the PMIC know that the system is ready for power to be removed.

- LP_REQ is an active-high output with an optional internal 100kΩ pull-up resistor to IN_VIO. The OTP_INT_PU bit in the OTP_PHUP_1 register determines if the internal resistor is used.
- LP_REQ is relevant when the PMIC is configured in Master mode (OTP_SLP_MSTRSLV = 0).

- If the PMIC is configured to be in the Slave mode (OTP_SLP_MSTRSLV = 1), then LP_REQ is kept de-asserted, or logic low. Not populating an external pull-up resistor is acceptable in this case.
- The ALT_LP_REQ_EN bit configures LP_REQ to work in an I^2C controlled alternate mode in Slave mode. The logic level during this mode can be set high by ALT_LP_REQ = 1. Both the ALT_LP_REQ_EN and ALT_LP_REQ flags are in the GLBL_CNFG0 register.

LP_ACK Input (OTP_LPACK_POL)

LP_ACK is a push-pull input from a controller to the MAX77752 representing the Low Power mode acknowledge. In Master mode, the acknowledge is a response caused by assertion of the LP_REQ output. Otherwise, in Slave mode, the signal triggers the PMIC to immediately go into Low Power mode, or DevSlp mode.

- LP_ACK is an active-high input with an optional, internal 100kΩ pull-up resistor to VIO (OTP_INT_PU = 1).
- LP_ACK is configured to be active low or high by the OTP_LPACK_POL bit in the SPARE_OTP register.
  - OTP_LPACK_POL = 0 configures LP_ACK as active high.
  - OTP_LPACK_POL = 1 configures LP_ACK as active low.
- When configured in Master mode (OTP_SLP_MSTRSLV = 0), the PMIC asserts LP_REQ upon a LP_MODE assertion and waits for a LP_ACK assertion indefinitely. This is the DevSlp Wait state. Once a LP_ACK assertion is received, the PMIC goes into DevSlp mode.
- When configured in Slave mode (OTP_SLP_MSTRSLV = 1), the PMIC remains in the ON state until an LP_ACK is asserted by a controller.

WP_L Output

WP_L is an open-drain output to the memory in the system that represents a write-protect function.

- WP_L is an active-low output with an optional, internal 100kΩ pull-up resistor to VIO (OTP_INT_PU = 1).
- During the power-up sequence (see the figures and timing diagrams in the On/Off Controller section), WP_L is asserted after the RESET_L output assertion.
  - There is a WP_L de-assertion delay programmed by WP_L_DLY[1:0] in the GLBL_CNFG3 register that is started when the RESET_L output is asserted.
- During the power-down sequence, WP_L is asserted without any delay along with the PGOOD and RESET_L outputs.
- When the PMIC is configured in Master mode or Slave mode (OTP_SLP_MSTRSLV = 0 or 1), WP_L is asserted without any delay along with RESET_L outputs.
- While exiting from DevSlp state, WP_L is de-asserted after the power-up sequence is complete. The de-assertion delay is programmed by WP_L_DLY[1:0].

External Regulator Enable/Disable Control

The PMIC has three I/O pins: EREG_EN1, EREG_EN2, and EREG_POK. These are intended to enable two external regulators and process their power okay (POK) signals. If the POK signals indicate an issue, the

PMIC transitions to the Off state and sets an internal flag (EREG_I) in the BLGL_INT0 register, indicating that an issue occurred.

External Regulator Enable/Disable Outputs (EREG_EN1, EREG_EN2)

- See the Register Descriptions section at the end of this document for additional details on the bit descriptions.
- EREG_EN1 and EREG_EN2 can be operated independently in one of two modes:
  - Control EREG_ENx manually by clearing the master assign bit (EREGxMSTRASGN = 0) from the EREGxFPS registers and then control the logic level with EREGxOPMD flags from the OPMD2 register.
  - Set the master assign bit (EREGxMSTRASGN = 1) to allow the flexible power sequencer to automatically control EREG_ENx
    - Choose active-high or active low (EREGxOPMD)
    - Program the desired master (EREGxMSTR[2:0])
    - Choose the power-up slot (EREGxUPSLT[1:0])
    - Choose the power down slot (EREGxDNSLT[1:0])
- During the On state, if EREG_POK is pulled low by an EREG_ENx pin, which is assigned to an FPS Master (EREGxMSTRASGN = 1), a power-down event is initiated.
- EREG_POK is pulled low when transitioning from the On state to DevSlp and back to the On state if any of the EREG_ENx resources on the FPS Master (EREGxMSTRASGN = 1) is disabled. Use the OTP_EREG_POK_AUTO_MASK_DIS bit in the SPARE_OTP register to choose the behavior of the PMIC.
  - OTP_EREG_POK_AUTO_MASK_DIS = 0: EREG_POK pin output is internally masked and power-down event does NOT initiate
  - OTP_EREG_POK_AUTO_MASK_DIS = 1: EREG_POK pin output is not masked and power-down event initiates
- EREG_ENx has optional internal pull-up resistors:
  - When OTP_INT_PU = 1, EREG_ENx is internally pulled up through RPU_EREG_POK.
  - When OTP_INT_PU = 0, EREG_ENx is not internally pulled up.
- Output Drive Capability:
  - When the pin voltage is driven greater than V_{SYS}, set the ALT_EREG2EN_EN bit in the GLBL_CNFG1 register to avoid internal leakage path.

EREG_POK Input

- The functional logic for EREG_POK is shown in the figure below (Figure 2). See the Register Descriptions section for additional details on the bit descriptions.
- EREG_POK has an optional internal pull-up resistor configurable with the OTP_INT_PU flag in the OTP_PHUP_1 register.

- When OTP_INT_PU = 1, EREG_POK is internally pulled up to IN_VIO through RPU_EREG_POK.
- When OTP_INT_PU = 0, EREG_POK is not internally pulled up.

- EREG_POK is capable of affecting the PGOOD and On/Off controller logic.
  - When EREG_M = 0 in the GLBL_INTM register, EREG_POK being low causes PGOOD_INT to be low.
  - EREG_POK is allowed to affect the PGOOD and On/Off controller logic when it is unmasked (EREG_M = 0). Any EREG_ENx outputs controlled by the flexible power sequencer (EREG1MSTRASGN OR EREG2MSTRASGN = 1) and EREG_POK go low while the On/Off controller logic enables the POK interrupt (EREG_INT_EN = 1). If EREG_I is driven high to the PGOOD and On/Off control logic, PGOOD goes low and the On/Off controller transitions to the Off state.
- If the EREG_POK input is not required for a given application:
  - Leave EREG_POK unconnected if the device has the internal pull-up resistor enabled (OTP_INT_PU = 1).
  - Connect EREG_POK to SYS if the device has the internal pull-up resistor disabled (OTP_INT_PU = 0).

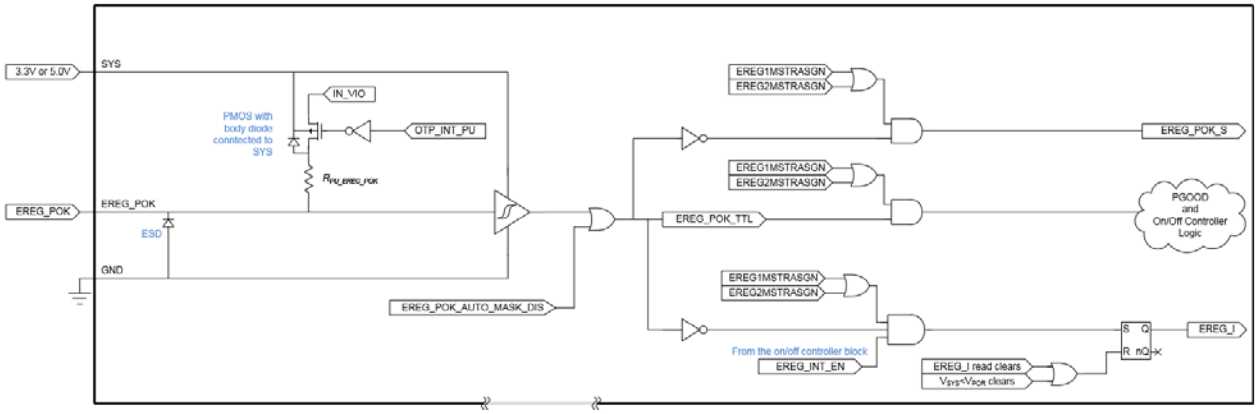

Figure 2. External regulator logic: How the external regulator's POK signal is handled logically.

Use Case—Two external regulators in the system that are both being driven by the flexible power sequencer:

- Set the EREG1MSTRASGN and EREG2MSTRASGN bits to place both regulators on the flexible power sequencer output.
- If EREG_POK is logic high when the On/Off controller sets EREG_POK_EN = 1, everything is okay with the external regulators and the system operates normally.
- If EREG_POK ever goes low while the On/Off controller has EREG_POK_EN = 1, the external regulators have a problem, and the On/Off controller transitions to the OFF state. The EREG_I flag is set internally, so software can learn that there was an external regulator issue on the subsequent power up.

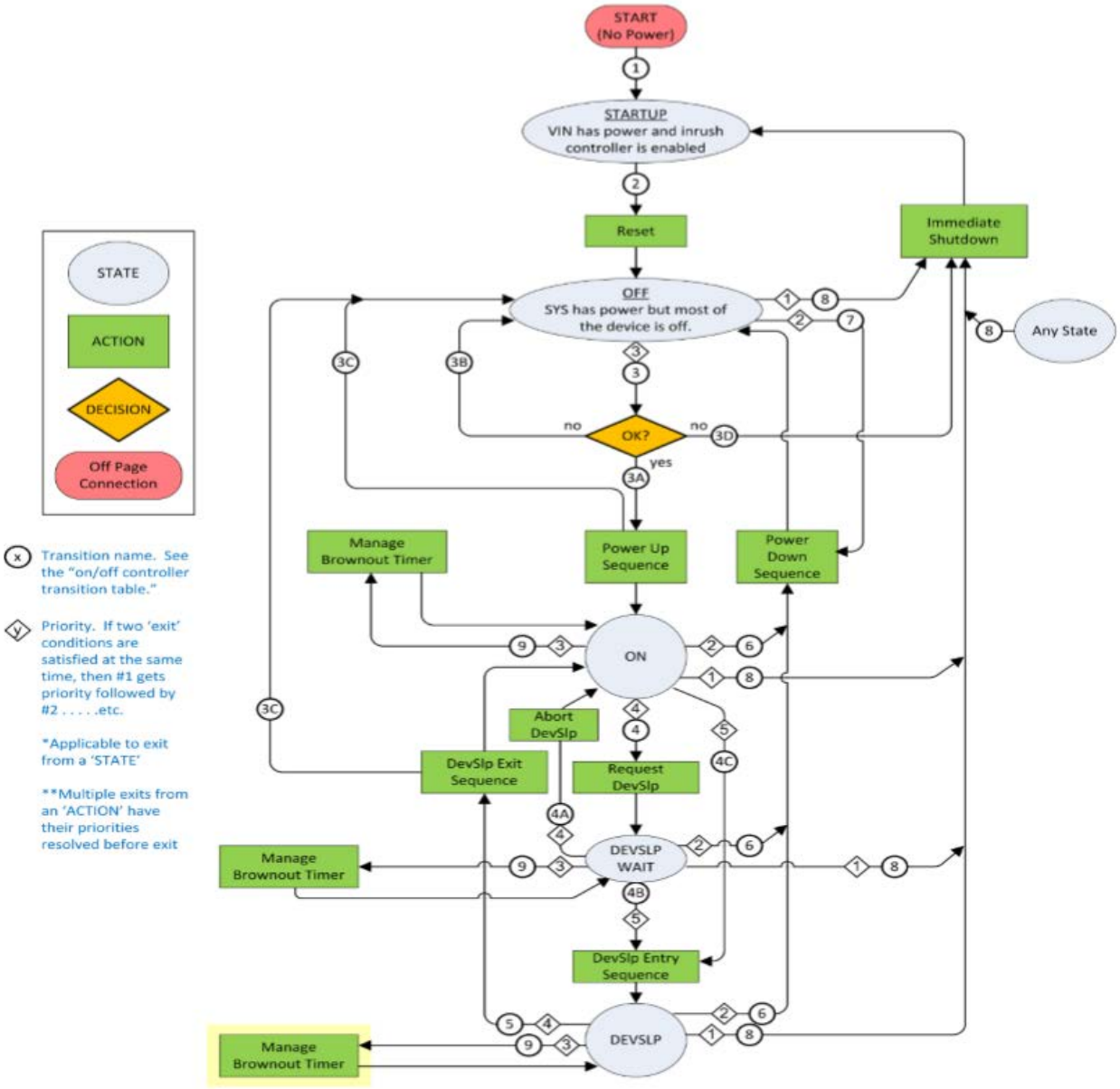

Figure 3. External regulator connections with External POK signals: Example of how to control external regulators' enables.

On/Off Controller

The following diagram is a top-level description of a flow for an On/Off controller that is controlling the state of the PMIC and, consequently, the individual regulators.
Figure 4. On/Off controller flow: When the device shuts down and powers up.

The following table lists the detailed transition conditions for the On/Off controller flow.

Table 2: On/Off Controller Flow

Transition	Condition
1	Input voltage to the system is above V_{in} UVLO threshold (sensed by VIN_SNS). $V_{IN} > V_{IN\_UVLO}$
2	The fundamental system voltages and resources are available. Move to the OFF state. The system voltage (V_{SYS}) is not undervoltage. SYSUVLO = 0 The inrush controller has completed soft-start. IN_SS_DONE = 1
3	A wake-up signal has been received. Move to the "OK?" state to check if the system is okay to wake up. $V_{SYS} > V_{SYS\_RESET}$ (rising threshold) threshold. SYSGOOD = 1 The Disable Wake Up bit is 0. DISWK = 0 See the GLBL_CNFG0 register in the Register Descriptions section for more details. Hiccup counter is less than the hiccup counter limit. HICCUP_CNT < HICCUP_CNT_LIM See the HICCUP_CNFG register in the Register Descriptions section for more details.
3A	The basic system resources are okay. The system voltage is above the required threshold. SYSGOOD = 1 The junction temperature is below the temperature overload threshold. TOVLD = 0
3B	Failed attempt to power up because the system voltage was below the required threshold. SYSGOOD = 0
3C	Failed attempt to power up successfully. At least one of the regulators in the power-up sequence did not assert its POWERGOOD (POK) output before the Power Good period expired. TPGOOD_EXP = 1 and PGOOD = 0
3D	Failed attempt to power up because the junction temperature was too high, or the system voltage was too high. TOVLD = 1
4	Enter DevSlp Wait state. The PMIC is in Master mode (See the OTP_PHUP_1 register in the Register Description section) OTP_SLP_MSTRSLV = 0 LP_MODE (de-bounced) is high. LP_MODE_DEB = 1
4A	Abort DevSlp entry. The PMIC is in Master mode OTP_SLP_MSTRSLV = 0 LP_MODE (de-bounced) is low. LP_MODE_DEB = 0
4B	Enter DevSlp Wait state (Master mode). The PMIC is in Master mode. OTP_SLP_MSTRSLV = 0 LP_MODE (de-bounced) remained high from 4A. There is a rising edge on LP_ACK. LP_ACK = 0→1
4C	Enter DevSlp State (Slave mode). The PMIC is in Slave mode. OTP_SLP_MSTR_SLV = 1 There is a rising edge on LP_ACK. LP_ACK = 0→1

5	Exit DevSlp mode. The PMIC is in Master mode and LP_MODE is low. OTP_SLP_MSTRSLV = 0 LP_MODE = 0 Or the PMIC is in slave mode and LP_ACK is low. OTP_SLP_MSTRSLV = 1 LP_ACK=0
6	Enter the Power-Down sequence. This state is initiated when "Start_Power_Down = True" in the pseudo code shown below in the Hiccup Count Algorithm section.
7	Enter the Power-Down sequence from the Off state. Software Power Off. SFT_OFF_NORST = 1 OR SFT_OFF_SYSRST = 1 See the GLBL_CNFG0 register in the Register Description section for more details.
8	Move to the Immediate Shutdown state. The junction temperature is too high. TOVLD_I = 1 The system voltage is low. SYSUVLO_I = 1 Bias is not stable. BRDY_I = 0
9	Manage Brownout Timer. System voltage has dropped below brownout threshold and brownout timer is enabled. $V_{SYS} < V_{SYS\_BO\ (Falling)}$ T_BO_EN = 1 See the GLBL_CNFG0 register in the Register Description section for more details. System voltage has risen above brownout threshold, brownout timer is enabled, and brownout timer has not expired. $V_{SYS} > V_{SYS\_BO\ (Rising)}$ T_BO_EN = 1 BO_TMR_EXP = 0

Hiccup Count Algorithm

```
for buck in [BUCK1, BUCK2, BUCK3]:
        if BUCK_M==0 & SS_DONE_buck==1 & ((UV_buck==1 & buck_UV_M==0) | (OV_buck==1 & buck_OV_M==0)) :
                HICCUP_CNT+=1
                PGOOD=0
                Start_Power_Down = True
for lsw in [LSW1, LSW2, LSW3]:
        if lsw_M==0 & SS_DONE_lsw==1 & (UV_lsw==1 & lsw_UV_M==0) :
                HICCUP_CNT+=1
                PGOOD=0
                Start_Power_Down = True
if LDO_M==0 & SS_DONE_LDO==1 & (UV_LDO==1 & LDO_UV_M==0) :
        HICCUP_CNT+=1
        PGOOD=0
        Start_Power_Down = True
if EREG_M==0 & t_PG_DLY==DONE & EREG_POK==0:
        HICCUP_CNT+=1
        PGOOD=0
        Start_Power_Down = True
if IN_OC_M==0 & t_PG_DLY==DONE & IN_OC==1:
        HICCUP_CNT+=1
        PGOOD=0
        Start_Power_Down = True
if T_BO_EN==1 & BO_TMR_EXP==1 & SYS_BO==1 & PG_DLY==DONE :
        HICCUP_CNT+=1
        PGOOD=0
        Start_Power_Down = True
if SYSRST_F_M=0 & SYS_RST==1:
        # the design intentionally excludes incrementing the hiccup counter here
        PGOOD=0
        Start_Power_Down = True
if IN_OVLO==1:
        # the design intentionally excludes incrementing the hiccup counter here
        PGOOD=0
        Disable_Inrush = True
if SFT_OFF_NORST==1:
        Start_Power_Down = True
if SFT_OFF_SYSRST==1:
        Start_Power_Down = True
```

Flexible Power Sequencer

The Flexible Power Sequencer (FPS) allows resources to power up under hardware or software control. Additionally, each resource can power up independently or among a group of other regulators with an adjustable power-up and power-down delays (sequencing). However, if there is an event that initiates immediate shutdown (e.g., input undervoltage) the device does not go through sequenced power-down. See the On/Off Controller Flow diagram (Figure 4) for more details on when the sequencing occurs.

The flexible sequencing structure consists of six master sequencing timers and nine resources. Each master sequencing timer is programmable through its configuration register (MSTRx_yFPS). When enabled/disabled, a master sequencing timer generates four sequencing slots. The time between each slot is programmable within the FPS register, as described below.

The signals to turn on a resource rise at the end of a slot duration. For example, if master 0's (FPS0) slot duration is programmed to 31µs and master 1's (FPS1) slot duration is programmed to 63µs, the power up sequence is as follows:

1. The power-up sequence starts.
2. 31µs pass
3. FPS0 Slot 0 resources power on.
4. 31µs pass
5. FPS0 Slot 1 resources power on.
6. 31µs pass
7. FPS0 Slot 2 resources power on.
8. 31µs pass
9. FPS0 Slot 3 resources power on.
10. 63µs pass
11. FPS1 Slot 0 resources power on.
12. 63µs pass
13. FPS1 Slot 1 resources power on.
14. Etc.

Nine resources within the MAX77752 have centrally based flexible power sequence enable/disable capabilities. With the MSTRASGN bits in the [Buckx, LDO, LSWx, EREGx]FPS registers, specify any of these nine resources to be enabled/disabled by the flexible power sequencer.

The figure below shows an example of four resources powering up under the control of flexible power sequencer 0.

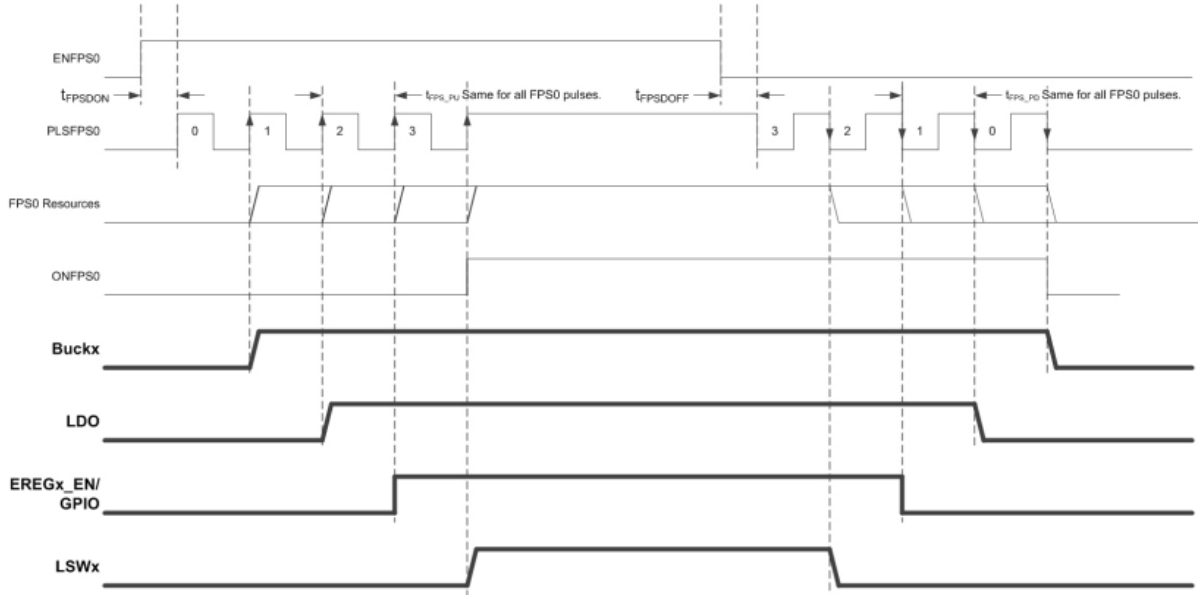

Figure 5. Power-up and power-down sequencing example: How the power-down sequence is the reverse of the power-up sequence.

Masters

There are six masters from FPS0 to FPS5 that control the power-up and power-down sequence of resources. These masters are also paired, e.g., masters FPS0 and FPS3 are paired as FPS0_3. See Figure 6 for a visualization.

- FPS0, FPS1, and FPS2 power down during the entry to DevSlp State and power up again when exiting from DevSlp back to the ON state.
- The pairs of masters are: FPS0_3, FPS1_4, and FPS2_5.
- Each pair of masters provides four sequencing slots.
- When enabled, a total of 12 slots (three pairs with four slots each) allows a sequenced power up.
- Each pair of masters powers on or down sequentially—that is, master 0 and master 3 power on or down in parallel, then master 1 and master 4, and then master 2 and master 5.
- Each pair of masters has independently programmable power-up and power-down slot durations using the MSTRx_y FPS registers, where x = 0, 1, 2, and y = x + 3.
    - Power-up and power-down slots are programmable through register bits MSTRx_yUPF[2:0] and register bits MSTRx_yDNF[2:0], respectively.
    - Power-up and power-down slot duration range is from 30µs to 3906µs in eight binary weighted steps.

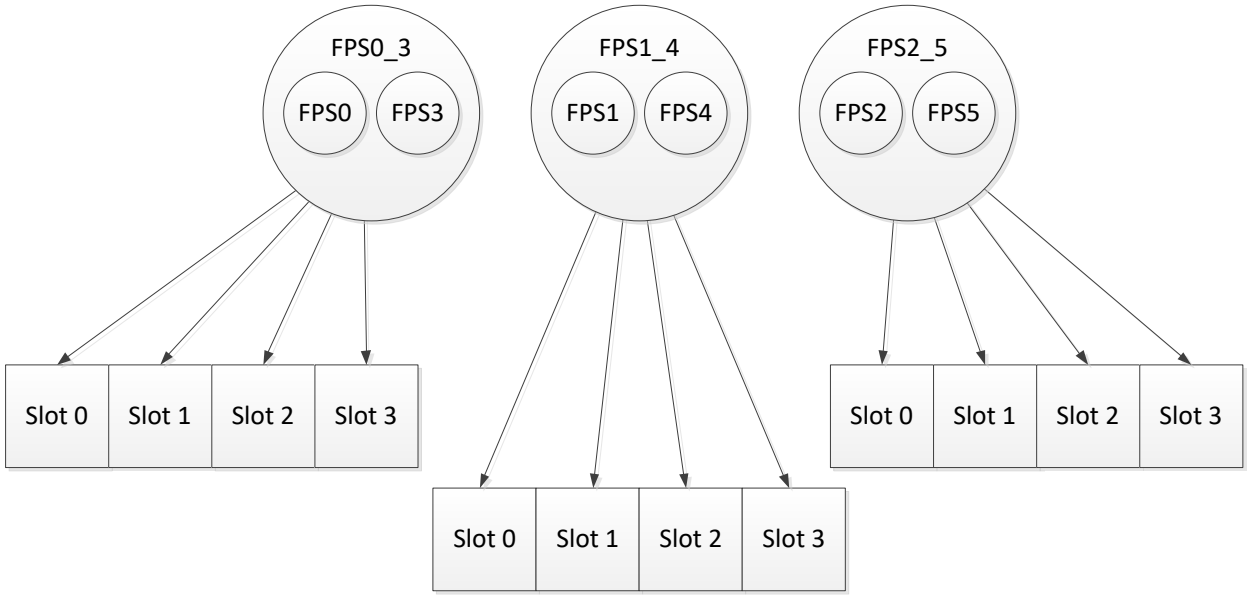

Figure 6. Flexible power sequencing—masters diagram: Visualization of the available number of FPS masters and the number of slots provided by each pair of masters.

Available Resources

The device contains the following resources that can be part of the flexible power sequencer with the following programmable options:

- 3x buck converters through the BUCKxFPS registers
  - Independently programmable power-down slot number within the master through BUCKxDNSLT[1:0]
  - Independently programmable power-up slot number within the master through BUCKxUPSLT[1:0]
  - Independently programmable master assignment for power-up AND power-down through BUCKxMSTR[2:0]
  - Independently programmable ability to be part of a master or not through BUCKxMSTRASGN
- 1x low dropout (LDO) linear regulator through the LDOFPS register
  - Independently programmable power-down slot number within the master through LDO_DNSLT[1:0]
  - Independently programmable power-up slot number within the master through LDO_UPSLT[1:0]
  - Independently programmable master assignment for power up AND power down through LDO_MSTR[2:0]
  - Independently programmable ability to be part of a master or not through LDO_MSTRASGN
- 3x load switch controllers through the LSWxFPS registers

- Independently programmable power-down slot number within the master through LSWxDNSLT[1:0]
- Independently programmable power-up slot number within the master through LSWxUPSLT[1:0]
- Independently programmable master assignment for power up AND power down through LSWxMSTR[2:0]
- Independently programmable ability to be part of a master or not through LSWxMSTRASGN

- 2x dedicated (external regulator control) through the EREGxFPS registers
  - Independently programmable power-down slot number within the master through EREGxDNSLT[1:0]
  - Independently programmable power-up slot number within the master through EREGxUPSLT[1:0]
  - Independently programmable master assignment for power-up AND power-down through EREGxMSTR[2:0]
  - Independently programmable ability to be part of a master or not through EREGxMSTRASGN

Pitfalls to Avoid

The flexible power sequencer provides for a tremendous amount of configurability and flexibility. However, this comes at the risk of unforeseen situations in a system. Here are some guidelines to avoid such risks:

- Because internal regulator POK signals are masked to be high (i.e., power is OK) while they are soft-starting, the PGOOD output asserts high immediately for a regulator configured to power up in the last slot (i.e., Slot 3 of FPS2 or FPS5). This is observable as a rising edge on the PGOOD output before the regulator in the last slot has completed its soft-start and reached its valid output voltage.
  - If the desired power-up sequence requires a regulator in the last power-up slot as described above, program the PGOOD assertion delay through PG_DLY[1:0] in the GLBL_CNFG3 register to insert a delay between the regulator soft-start and the PGOOD assertion.
- If a regulator's output is the input for another regulator, configure the first to be enabled early enough in the sequence, so it has completed its soft-start before the other regulator is enabled.
- If a regulated output from the MAX77752 serves as a pull-up supply for a signal on an external regulator in the system, Maxim recommends configuring the sequence such that the internal regulator is enabled first, before the external regulator.
  - Ex: LSW2 is a pull-up voltage for an external regulator's POK output. Enable LSW2 before the external regulator and disable it after the external regulator.
- Enable the regulator that supplies the VIO pin at least 2µs after the supply at VIO has reached the nominal level and before executing any I^2C commands.

- Ex: If LSW1 supplies VIO, avoid configuring LSW1 on slot 3 of FPS2 for FPS5 masters during a power-up sequence or DevSlp exit sequence. Even if this is done, ensure that LSW1 soft-start is complete at least 2µs before RESET_L de-assert.

Resources

The above-mentioned slave resources are grouped by common characteristics and configuration. Each resource type has different I/O signals to control the resource, depending on the usage, power state and special cases. The resources are as follows:

- Buck resource through the OPMD1 register
  - Output Signal—Controls buck regulator enable/disable through register bits BUCKxOPMD[1:0]
  - Output Signal—Controls Low Power mode (LPM) enable/disable signals
  - Input Signal—Power Good/VOK from buck regulator
- LDO resource through the OPMD2 register
  - Output Signal—Controls linear regulator enable/disable through register bits LDOOPMD[1:0]
  - Output Signal—Controls Low Power mode (LPM) enable/disable signals
  - Input Signal—Power Good/VOK from linear regulator
- Load switch resource
  - Output Signal—Controls load switch enable/disable through register bit LSWxOPMD - through external pin
  - Input Signal—Power Good/VOK from load switch; through external pin
- External Regulator Resource through the OPMD2 register
  - Output Signal—Controls external regulator enable/disable through register bit EREGxOPMD; through external pin
  - Input Signal—Power Good/VOK from external regulator; through external pin

Buck and LDO Power Mode Control

The following table enumerates the various possible modes that the buck converter or LDO linear regulator can be placed in based on the sequencer configuration and the individual buck/LDO power mode configurations. Do NOT change the BUCKxMSTRASGN/LDOMSTRASGN bit while the regulator is already enabled in the ON state, because this can cause a glitch on the regulator output.

Table 3: Decode Logic for Buck and LDO Resources

#	Register Bit	Internal Signal		Register Bit	Register Bit	Internal Signal	Internal Signal		
0	BUCKxMSTRASGN / LDOMSTRASGN	FPS_EN_BUCKx / FPS_EN_LDO	DEVSLP_FLAG	BUCKxOPMD[1] / LDOxOPMD[1]	BUCKxOPMD[0] / LDOxOPMD[0]	BUCKx_ENLDO EN	BUCKx_LPMEN / LDO_LPMEN	BUCK3DVS_DEVSLP	Mode
1	0	x	x	0	0	0	0	0	OFF
2	0	x	0	0	1	1	0	0	Enabled, Normal Power
3	0	x	1	0	1	1	1	Based on OTP	Enabled, Low Power
4	0	x	x	1	0	1	1	0	Enabled, Low Power
5	0	x	x	1	1	1	0	0	Enabled, Normal Power
6	1	0	x	x	x	0	0	0	OFF
7	1	1	x	0	0	1	0	0	OFF
8	1	1	0	0	1	1	0	0	Enabled, Normal Power
9	1	1	0	0	1	1	1	Based on OTP	Enabled, Low Power
10	1	1	1	1	0	1	1	0	Enabled, Low Power
11	1	1	1	1	1	1	0	0	Enabled, Normal Power

Load Switch Power Mode Control

The following table enumerates the various possible modes that the load switch can be placed in based on the sequencer configuration and the individual load switch power mode configurations. Do NOT change the LSWxMSTRASGN bit while the regulator is already enabled in the ON state, because this can cause a glitch on the load switch output.

Table 4: Decode Logic for Load Switch Resources

#	Register Bit	Internal Signal	Register Bit	Internal Signal	
0	LSWxMSTRASGN	FPS_EN_LSWx	LSWxOPMD[0]	LSWx_EN	Mode
1	0	x	0	0	OFF
2	0	x	1	1	ON
3	1	0	x	0	OFF
4	1	1	x	1	ON

Dedicated Output Power Mode Control

The following table enumerates the various possible modes that dedicated output (EREG_ENx) can be placed in through the configuration in the flexible power sequencer.

Do NOT change the EREGxMSTRASGN bit while in the ON state, because this can cause a glitch on the EREG_ENx output.

Table 5: Decode Logic for Dedicated Output Resource

#	Register Bit	Internal Signal	Register Bit	Internal Signal	
0	EREGxMSTRASGN	FPS_EN_EREGx	EREGxOPMD	EREG_Enx	EREGx Logic State
1	0	x	0	0	LOW
2	0	x	1	1	HIGH
3	1	0	0	0	LOW (Active High)
4	1	1	0	1	HIGH (Active High)
5	1	0	1	1	HIGH (Active Low)
6	1	1	1	0	LOW (Active Low)

Power Holdup Functionality (IN_PHUP)

IN_PHUP is an analog power input pin. This pin is connected to the output of the power holdup IC. This pin provides power to a selected internal block that maintains the logic level of EREG_EN1, WP_L, and PGOOD (internal) during a SYS power fail event. The power holdup flow can be accessed in the On/Off Controller section. If this function should be disabled, the OTP_PHUP_EN flag in the OTP_PHUP_1 register must be cleared.

In case of a fault condition in which the HICCUP_CNT_EXPIRE = 1 in the HICCUP_CNFG register, this pin can be used to provide power to the I^2C block.

Current Sense Amplifier

The current sense amplifier (CSA) circuit monitors the input current into the system by comparing against a set threshold. If the input current exceeds the threshold for more than the debounce timer period, an interrupt is generated, IN_OC_I = 1 in the GLBL_INT0 register, and a power-down event initiates if IN_OC_M = 0 in the GLBL_INTM register. Configure OTP_CSA_DBNC in the SPARE_OTP register to set the debounce timer period to 50µs or 100µs. The default is 100µs. Two register bits (CSTH_OTP[1:0] in the CNFG_CSA register) are available to set the current threshold, the default is 45mV (2.25A), and a R_{SENSE} resistor of 20mΩ ±1% is recommended for the application.

Buck Regulators (BUCK1/2 – 2A Output)

BUCK1 and BUCK2 are step-down converters with the following:

- Programmable output voltage from 0.600V to 2.194V in 6.25mV steps
- Programmable brownout and overvoltage comparators

Setting Output Voltage

Set the output voltage with BUCKxVOUT[7:0] in the BUCKxCNFG1 register, where each step is 6.25mV. For example, to set BUCK1 to output 1.2V, BUCK1CNFG1 = 0x53.

Output Monitoring

BUCK1 and BUCK2 have multiple ways of ensuring the health of their output.

- There is a programmable brownout monitor that sets an interrupt flag (BUCKx_UV_I) in the BUCK_INT register when the output voltage falls below the programmed brownout threshold.
    - To have the brownout on the output of the buck initiate a power-down sequence, clear the BUCKx_UV_M bit in the BUCK_INTM register.
    - When the buck is first enabled, either through I^2C or by the sequencer, the buck control circuit attempts to ramp the output voltage as fast as possible to the target output (programmed by BUCKxVOUT[7:0] in the BUCKxCNFG1 register) limited only by the PMOS peak current limit. During this process of output voltage ramp, the brownout output is prevented from being triggered until the end of the soft-start period (determined by the specified ramp-up slew rate).
    - However, if the output capacitance is large enough, the soft-start process completes before the output reaches the rising UV threshold and thereby the UV interrupt sets, although the output would eventually rise above the UV threshold.
    - When the output voltage for BUCK1 or BUCK2 is decreased through I^2C after they have been enabled, the buck control circuit changes the output voltage target directly to the final value. In such a case, the brownout comparator naturally provides an undervoltage assertion, which if not masked by BUCKx_UV_M, causes a power-down sequence. If such a use case is foreseen, set the mask bits first and then change the output voltage. Alternatively, the change in output voltage should be done in small steps. Note that even if the mask bit is set, the corresponding interrupt bit is still set.
    - Note that a load transient on the output of the buck at a fast slew rate and a large magnitude has the capability to cause an output voltage droop that causes the UV comparator to trip and flag an undervoltage event, if the brownout threshold is set high (such as 90%).

- There is a programmable overvoltage monitor that sets an interrupt flag (BUCKx_OV_I) when the output voltage rises above the programmed overvoltage threshold.
- To allow the overvoltage on the output of the buck to initiate a power-down sequence, clear the BUCKx_OV_M bit.
- When the buck is first enabled, either through I^2C or by the sequencer, the buck control circuit attempts to ramp the output voltage as fast as possible to the target output (programmed by BUCKxVOUT[7:0]), limited only by the PMOS peak current limit. During this process of output voltage ramp, the overvoltage output is prevented from triggering until the end of the soft-start period (determined by the specified ramp-up slew rate).
- When the output voltage for BUCK1 or BUCK2 is increased through I^2C (programmed by BUCKxVOUT[7:0]) after they have been enabled, the buck control circuit changes the output voltage target directly to the final value. The buck output voltage then increases as a function of the output capacitance and load. In such a case, the overvoltage comparator provides an overvoltage assertion, which if not masked by BUCKx_OV_M, causes a power-down sequence. If such a use case is foreseen, set the mask bits first and then change the output voltage. Alternatively, change output voltage in small steps. Note that even if the mask bit is set, the corresponding interrupt bit is still set.
- A sudden load release with a high slew rate and magnitude might cause a momentary over-shoot on the output of the buck that can trip the OV comparator output. If such use cases are expected, set the OV threshold as high as allowed.

- All the above conditions have associated status bits in the BUCK_STAT register that provide a real-time status of the conditions.

Enable and Power Mode Control

- Enable or disable BUCK1/2 either by the flexible power sequencer or by I^2C.
- The BUCKxFPS register determines if they are part of the power-up and power-down sequence as well as the master and slot numbers they are assigned to.
- Control whether the buck is in Normal Power mode or Low Power mode with the BUCKxOPMD[1:0] bits in the OPMD1 register.
  - By setting BUCKxOPMD[1:0] = 0b00, the buck regulator is disabled.
  - The buck can be configured to dynamically transition to low power mode when the PMIC transitions to the DevSlp state.
  - The buck can also be forced to transition to low-power mode through an I^2C command. See the Buck and LDO Decode Logic in the Flexible Power subsection in the Global Resources section.

Active Discharge Resistor

BUCK1/2 have an active-discharge resistance that can be enabled and disabled with BUCKxADDIS in the BUCKxCNFG2 register. Enabling the active discharge feature helps ensure a complete and timely power down of all system peripherals. The default condition of the active-discharge resistor feature is enabled, such that when the buck converter is disabled, an internal 100Ω discharge resistor is connected to the output to discharge the energy stored in the output capacitor. When the buck converter is enabled, the discharge resistor is disconnected from the output.

Buck Regulators (BUCK3—3A Output)

BUCK3 is a step-down converter with the following:

- Programmable output voltage from 0.26V to 1.52V in 10mV steps
- Programmable Low Power mode (LPM) to enable efficient low power PMIC states
- Programmable brownout and overvoltage comparators

Setting Output Voltage

Set the output voltage with BUCK3VOUT[6:0] in the BUCK3CNFG1 register. For example, to set BUCK3 to output 0.8V, set BUCK3CNFG1 = 0x37.

Active Discharge

To enable a 100Ω active discharge resistance from the output to ground while the buck is disabled, set BUCK3ADDIS = 0.

Output Monitoring

BUCK3 has multiple ways of ensuring the health of its output:

- There is a programmable brownout monitor that sets an interrupt flag (BUCK3_UV_I) in the BUCK_INT register when the output voltage falls below the programmed brownout threshold.
    - To allow the brownout on the output of the buck to initiate a power down sequence, clear the BUCK3_UV_M bit.
    - When the buck is first enabled, either through I^2C or by the sequencer, the brownout condition is not asserted until the soft-start is complete. However, if the output capacitance is large enough, the soft-start process completes before the output reaches the rising UV threshold, so the UV interrupt would get set, although the output would eventually rise above the UV threshold.
    - However, when the output voltage target is increased through I^2C (write to BUCK3VOUT[6:0]) and the buck converter is in the process of performing the controlled ramp to the new target, a brownout condition is not triggered until the controlled ramp is complete.
- There is a programmable overvoltage monitor that sets an interrupt flag (BUCK3_OV_I) when the output voltage rises above the programmed overvoltage threshold.
    - To allow the overvoltage on the output of the buck to initiate a power-down sequence, clear the BUCK3_OV_M bit.
    - However, when the output voltage target is decreased through I^2C (write to BUCK3VOUT[6:0]) and the buck converter is performing the controlled ramp to the new target (if BUCK3FSREN = 1), an overvoltage condition is not triggered until the controlled ramp is complete. Note that if the controlled ramp for decreasing output voltage target is disabled (BUCK3FSREN = 0), then the overvoltage condition is triggered and could cause a power-down sequence if unmasked (BUCK3_OV_M = 0). If this situation is expected, mask it by setting BUCK3_OV_M.
- All the above conditions have associated status bits in the BUCK_STAT register that provide a real-time status of the condition.

Enable and Power Mode Control

Enabled BUCK3 either by the flexible power sequencer or by I^2C.

- The BUCK3FPS register determines if it is part of the power-up and power-down sequence as well as the master and slot numbers that it is assigned to.
- Control whether the buck is in Normal Power mode or Low Power mode with the BUCK3OPMD[1:0] bits in the OPMD1 register.
    - By setting BUCK3OPMD[1:0] = 0b00, the buck regulator is disabled.
    - The buck can be configured to dynamically transition to Low Power mode when the PMIC transitions to the DevSlp state.
    - The Buck can also be forced to transition to Low Power mode through an I^2C command. See the Buck and LDO Decode Logic in the Flexible Power subsection in the Global Resources section.

Load Switch Driver (LSW1/2)

There are two dedicated external load-switch controllers. When the inrush feature is disabled (OTP_INRUSH_DISABLE = 1) in the OTP_2B_INRUSH register, the inrush block can be configured to be the third Load Switch controller by setting the LSW_OTP_SEL flag in the INRUSH_OPTION register. In this configuration, the inrush block pins INR_DRV and INR_OUT function as LSW3_DRV and FBLSW3, respectively. The soft-start circuit to minimize inrush current is also programmable.

Input Selection

For the load-switch controllers to report POK status at the output (measured by the FBLSWx pin), select the inputs to each of the load switch controllers with the CNFG_LSWx register.

- Provided LSWx_INP_EXT = 0, select among three internal buck regulators with LSWx_INP_SEL[1:0].
- If LSWx_INP_EXT = 1, the input to the load switch is assumed to be VSYS.

Output Drive

- Upon enabling either through I^2C or by the sequencer (see the Load Switch Power Mode Control section), the load switch controller's output stage drives the gate of the switch in a controlled manner using an internal oscillator. See the Load Switch Power Mode Control section for details on enabling/disabling.
- Program the frequency of this oscillator through LSWx_DRV_FREQ[2:0], where x = 1,2. For LSW3, the oscillator frequency is set by OTP_INR_FREQ[2:0] in the OTP_2B_INRUSH register.
- Different frequencies result in varying gate drive strengths, resulting in differing inrush currents through the switch.

Programming Soft-Start

Program the soft-start of the load switch by setting the drive frequency (LSWx_DRV_FREQ[2:0]) and following the equation:

$$t_{SS\_DONE\_LSW} = \frac{256}{f_{LSWx\_DRV}}$$

Refer to the Load Switch Controller Timing Diagram for a visual representation of the soft-start.

Load Switch Controller Timing

The following diagram shows the load switch controller's start-up timing while driving an external load switch.

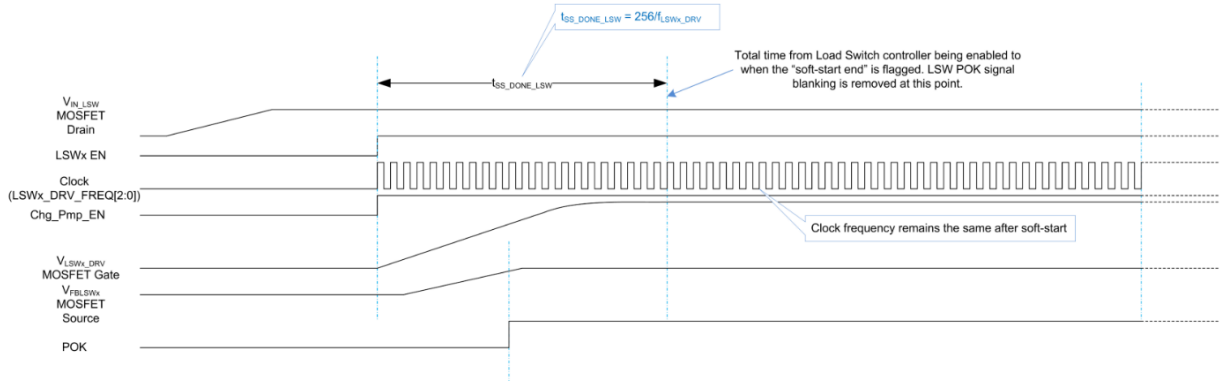

Figure 7. Load switch start-up timing: Soft-start behavior of a load switch.

Load Switch Driver (LSW3)

When the inrush feature is disabled (OTP_INRUSH_DISABLE = 1) in the OTP_2B_INRUSH register, the inrush block can be configured to be the third Load Switch controller by setting LSW3_ENABLE = 1 in the INRUSH_OPTION register. In this configuration, inrush block pins INR_DRV and INR_OUT function as LSW3_DRV and FBLSW3, respectively.

Input Selection

For the load switch controllers to report POK status at the output (measured by the FBLSWx pin), each of the load switch controllers features programmable input selection.

- Provided LSWx_INP_EXT = 0, select among the three internal buck regulators with LSWx_INP_SEL[1:0] in the CNFG_LSW3 register.
- If LSWx_INP_EXT = 1, the input to the load switch is assumed to be VSYS.

Output Drive

The load switch controller comprises an integrated charge pump that uses the voltage at SYS to drive the gate of the external N-channel MOSFET such that in steady state the external MOSFET is driven to saturation (completely ON).

- Upon enabling either through I^2C or by the sequencer (see the Load Switch Power Mode Control section), the load switch controller's output stage drives the gate of the switch in a controlled manner using an internal oscillator.
- Program the frequency of this oscillator through OTP_INR_FREQ[2:0] in the OTP_2B_INRUSH register.
- Different frequencies result in varying gate drive strengths, which results in differing inrush currents through the switch.

Programming Soft-Start

- Program the soft-start of the load switch by setting the drive frequency (OTP_INR_FREQ [2:0]), which follows the equation:

$$t_{SS\_DONE\_LSW} = \frac{256}{f_{LSWx\_DRV}}$$

- Refer to the Load Switch Controller Timing Diagram for a visual representation of the soft-start.

Linear Regulator

The device includes one on-chip LDO linear regulator. Programmability includes:

- On/Off control
- Output voltage
- Low Power mode

Setting the Output Voltage

Program the output voltage of the LDO by setting the VOUT_LDO[6:0] bits in the LDOCNFG1 register. The voltage can range from 0.8V to 3.95V in 25mV increments.

Active Discharge Resistor

The LDO has an active-discharge resistance that can be enabled and disabled with ADE_LDO in the LDO_CNFG1 register. Enabling the active discharge feature ensures a complete and timely power down of all system peripherals. The default condition of the active-discharge resistor feature is enabled such that whenever V_{SYS} is below $V_{SYSUVLO}$, the LDO is disabled with its active discharge resistors turned on. When V_{SYS} is less than 1.0V, the NMOS transistor controlling the active discharge resistor loses its gate drive and becomes open. See the Register Description section for additional details.

Enable and Power Mode Control

Enable and disable the LDO either by the flexible power sequencer or by I^2C.

- The LDOFPS register determines if it is part of the power-up and power-down sequence as well as the master and slot numbers that it is assigned to.
- Control whether the linear regulator is in Normal Power mode or Low Power mode with the LDOOPMD[1:0] bit in the OPMD2 register control.
    - By setting LDOOPMD[1:0] = 0b00, the buck regulator is disabled.
    - The LDO can be configured to dynamically transition to Low Power mode when the PMIC transitions to the DevSlp state.
    - The LDO can also be forced to transition to low-power mode through an I^2C command. Refer to the Buck and LDO Decode Logic in the Flexible Power subsection of the Global Resources section.

I²C Serial Communications Interface

The MAX77752 features revision 4.0 of the I²C-compatible, 2-wire serial interface consisting of a bidirectional serial data line (SDA) and a serial clock line (SCL). The MAX77752 acts as a slave-only device relying on the master to generate a clock signal. SCL clock rates from 0Hz to 3.4MHz are supported. Optional resistors (24Ω) in series with SDA and SCL protect the device inputs from high-voltage spikes on the bus lines. Series resistors also minimize cross-talk and undershoot on bus signals. For additional information on I²C, refer the I²C-bus specification and user manual that is available from NXP (document title: UM10204).

I²C Interface Power

The MAX77752's I²C interface derives its power from V_{IO}. V_{IO} accepts voltages from 1.7V to 3.6V (V_{VIO}). Cycling V_{IO} does not reset the I²C registers. When V_{IO} is less than V_{IO_UVLO} and V_{SYS} is less than VSYSUVLO, SDA, and SCL are high-Z. Ensure the supply at V_{IO} is at the nominal voltage for at least 2µs before an I²C transaction is sent to the MAX77752. Also ensure the configurations of the power-up sequence do not cause a situation that violates this.

I²C Acknowledge Bit

The MAX77752 issues an ACK for all register addresses in the possible address space even if the register does not exist.

I²C Clock Stretching

In general, the master device is responsible for generating the clock signal for the I²C bus. The I²C specification allows slow slave devices to alter the clock signal by holding down the clock line. The process in which a slave device holds down the clock line is typically called clock stretching. The MAX77752 does not use any form of clock stretching to hold down the clock line.

I²C General Call Address

The MAX77752 does not implement the I²C specification's "general call address." If the MAX77752 sees the general call address (0b0000_0000) it does not issue an acknowledge.

I²C Device ID

The MAX77752 does not support the I²C Device ID feature.

I²C Watchdog Timer

The MAX77752 contains an I²C watchdog timer to ensure reliable operation of the I²C bus. This I²C watchdog timer helps the system recover from I²C bus hang-ups that occur when devices on an I²C bus operate out of sync from each other due to noise, poor system design, or poor IC design. In many cases, I²C bus hang-ups can be cleared by the master. The master can clear the I²C bus by issuing nine consecutive clock pulses. In all known cases, the MAX77752 I²C state machine is cleared whenever the master issues nine consecutive clock pulses. However, to account for unforeseen system issues, the I²C watchdog timer serves as a back-protection method for I²C bus hang-ups. With the I²C watchdog timer disabled, the MAX77752 meets the 0Hz SCL frequency requirements in the I²C specification (UM10204). In many cases, this 0Hz capability is not needed. Activating the I²C watchdog timer defeats the 0Hz specification of I²C. Enable the I²C watchdog timer with the WD_EN bit in I2C_CTRL1 register. With the I²C watchdog timer enabled, the MAX77752 monitors the time between consecutive SCL

edges. If this time exceeds the I²C watchdog timer period of 35ms, the MAX77752 I²C state machine is reset. If a STOP condition is detected when the watchdog timer is running, the timer is reset until the next START condition. The I²C watchdog timer also generates an interrupt signal that can be used at top-level to indicate an I²C watchdog timer interrupt. Any SCL line transition (rising edge or falling edge) clears the watchdog timer. This SCL line monitoring capability prevents any unexpected wrong reset of the I²C controller during very long burst mode transactions.

I²C Communication Speed

The MAX77752 is compatible with four communication speed ranges as defined by the I²C 4.0 specification:

- 0Hz to 1MHz (Fast Mode Plus)
- 0Hz to 3.4MHz (High-Speed Mode)

The MAX77752 does not support the Ultra Fast mode data rate (5Mbit/s) defined in the I²C 4.0 specification. Operating in standard mode, fast mode, and fast mode plus does not require special protocols. The main consideration when changing the bus speed through this range is the combination of bus capacitance and pull-up resistors. Higher time constants created by the bus capacitance and pull-up resistance (C*R) slow the bus operation. Therefore, when increasing bus speeds, the pull-up resistance must be decreased to maintain a consistent time constant. See the “pull-up resistor sizing” section of the I²C 4.0 specification (UM10204) for detailed guidance on the pull-up resistor selection. In general, for bus capacitances of 200pF, a 100kHz bus needs 5.6kΩ pull-up resistors, a 400kHz bus needs approximately 1.5kΩ pull-up resistors, and a 1MHz bus needs 680Ω pull-up resistors. When the open drain bus is low, the pull-up resistor is dissipating power, lower value pull-up resistors dissipate more power (V^2/R).

Operating in high-speed mode requires some special considerations. For a full list of considerations, see the I²C 4.0 specification (UM10204). The major considerations with respect to the MAX77752 device are:

- The I²C bus master must use current source pull-ups to shorten the signal rise times.
- The I²C slave must use a different set of input filters on its SDA and SCL lines to accommodate for the higher bus speed.
- The communication protocols utilize the high-speed master code. At power-up and after each stop condition, the MAX77752 I²C inputs filters are set for Standard mode, Fast mode, and Fast mode plus (i.e., 0Hz to 1MHz). To switch the input filters for high-speed mode, use the high-speed master code protocols that are described in the I²C Communication Protocols section. The MAX77752 allows the slave to remain in High Speed mode and retain the input filters for High Speed mode after a stop condition when High Speed mode extension is enabled.

Write Protection

The MAX77752 incorporates write protection for all the registers in the PMIC. When the I2CWP bit in the I2C_CTRL2 register is set, writes to any register are ignored. However, the I²C configuration registers I2C_CTRL1 and I2C_CTRL2 are not subject to write protection even if I2CWP = 1. The I2CWP bit is also reset to its default value of 1 (write protect enabled) upon receiving a STOP condition over the I²C lines (SDA and SCL).

Writing to registers using the I2CWP bit

To write to a register, the first write must be to the register containing the I2CWP bit followed by the write to the appropriate data registers with a REPEAT START condition in between.

I²C Communication Protocols

The MAX77752 supports both writing and reading from its registers. Although the I²C slave in the MAX77752 allows single register writes as well as multiple register writes, the I²C write protection feature requires utilizing the "Write to Multiple Registers Using Register-Data Pairs." This is due to the I2CWP (write protect bit) being reset upon a STOP condition. A STOP condition at the end of a single register write to clear I2CWP would reset it back to 1. To write to any register in the MAX77752, the following is the recommended order of transactions:

1. Execute a "Writing to a Single Register" protocol to the I2C_CTRL1 register to set the PAIR bit (bit 4) to 1.
    a. The I2C_CTRL1 and I2C_CTRL2 registers are not write protected even if I2CWP = 1, so this is possible.
    b. Note that this I²C write to the PAIR bit is required only once after power-up and will retain its value if there is no power down sequence or immediate shutdown.
    c. A power-down sequence initiated by writing a 1 to the SFT_OFF_NORST bit does not reset the PAIR bit and it retains its value.
2. Execute a "Writing Multiple Bytes Using Register-Data Pairs" protocol, with the first register being I2C_CTRL2 with the data byte 0x00 (clear the I2CWP bit).
    a. Subsequent register-data pairs can address any register within the MAX77752.
    b. A STOP condition at the end of the transaction resets I2CWP back to 1, thereby enabling write protection again.

Writing Multiple Bytes

There are two protocols within the MAX77752 to write or read multiple bytes. The PAIR bit in the I2C_CTRL1 register configures the protocol to be used. All slave IDs default to this protocol at power-up and after a system reset event.

Note: Because the MAX77752 provides I²C write protection (I2CWP), the first write command must be to the register with I2CWP to clear the bit (write to 0), followed by a REPEAT START condition.

Note: Because the PAIR register bit's default value corresponds to Sequential Register Write mode, write the I2C_CTRL1 register after the I2CWP bit is cleared to enable the Register-Data Pair mode protocol. There must be a REPEAT START condition in between the command to clear I2CWP and the command to set PAIR so I2CWP is not reset back to 1.

Reading from a Single Register

Because there is a write protection bit (I2CWP) reset to its default value of 1 (enable write protection) upon a STOP condition, always write to the register containing I2CWP first using this protocol. If not, any writes to registers are ignored.

Reading from Sequential Registers

When the MAX77752 receives a stop (P), it does not modify its register pointer.

I²C High-Speed Mode Extension

As defined by the I²C 4.0 specification, enter High Speed mode by transmitting the high-speed master code of 0b0000 1XXX and exit with a STOP condition. To eliminate overhead for entering high-speed mode using the master code, the I²C master can choose to allow the slave to remain in high-speed mode after a STOP condition. When the HS_EXT bit is set to 1 (bit 0 in the I2C_CTRL1 register), the MAX77752 extends high-speed mode even if a STOP condition is entered and the I²C master can freely use any type of transactions with STOP conditions. The table below demonstrates how the HS_EXT bit can be used. For situations when the extended high-speed mode is not desired, HS_EXT is kept at 0.

Table 6: Behavior of MAX77752 After Configuring HS_EXT

State	HS_EXT	Current Mode (Data Rate)	Comment/Behavior
1	0	Standard mode Fast mode Fast mode Plus	Issue HS Code to enter HS mode (Go to state 2) Write HS_EXT = 1 (Go to state 4)
2	0	HS mode	Issue STOP to exit HS mode (Go to state 1) Write HS_EXT = 1 (Go to state 3)
3	1	HS mode	Issue STOP and continue in HS mode (Go to state 3) Write HS_EXT = 0 (Go to state 2)
4	1	Standard mode Fast mode Fast mode Plus	Issue Hs-Code to enter HS mode (Go to state 3) Write HS_EXT = 0 (Go to state 2)

Register Descriptions

This section provides detailed descriptions of the registers for the MAX77752. Undocumented register locations are reserved.

Reset types (conditions):

- S—$V_{SYS} < V_{POR}$
- O—PORB = 0 OR $T_J < T_{J,MAX}$ OR $V_{SYS} < V_{UVLO}$

Access types:

- R—Read only. Writes are ignored.
- W—Write only.
- R/W—Read and Write.
- RC—Read only. Writes are ignored. The bit is cleared after reading.

Register types:

- CNFG—Configuration registers for the adjustment of device parameters.
- DATA—Data registers to provide information. One example would be the CID registers.
- INT—Read only, interrupt registers that indicate an event occurring. When an interrupt event has occurred, the corresponding interrupt bit is set in the register. Each interrupt event has a corresponding interrupt mask that determines whether an interrupt event affects the hardware interrupt output. Interrupt registers are cleared when read.
- INTM—Interrupt mask registers for preventing ("masking") an interrupt event from affecting the hardware interrupt output. The interrupt mask settings have no effect on the interrupt registers. If an interrupt mask is cleared and an interrupt event happens, that event is reported on the corresponding hardware interrupt output. Otherwise, if an interrupt mask is set, then an interrupt event is not reported on the hardware interrupt output.
- MIXED—A mixed register contains more than one type, such as configuration and status.
- OTP—One-Time Programmable.
- STTS—Read only, status registers that reflect the actual condition of an event or input.

Global Resources

GLBL_INT0

Register Name	GLBL_INT0
I²C Slave Address	0x60
Register Address	0x00
Reset Value (HEX)	0x00
Reset Value (BIN)	0b00000000
Reset Type	S
Access Type	RC
Register Type	INT

Bit	Default	Bit Name	Description	Reset	Access Type
7	0	RSVD	Reserved. Unutilized bit. Write to 0. Reads are don't care.	S	RC
6	0	RSVD	Reserved. Unutilized bit. Write to 0. Reads are don't care.	S	RC
5	0	RSVD	Reserved. Unutilized bit. Write to 0. Reads are don't care.	S	RC
4	0	RSVD	Reserved. Unutilized bit. Write to 0. Reads are don't care.	S	RC
3	0	RSVD	Reserved. Unutilized bit. Write to 0. Reads are don't care.	S	RC
2	0	UV_LDO_I	LDO Output Undervoltage Interrupt. 0 = LDO output has not been enabled with an undervoltage condition since the last time this bit was read. 1 = LDO output has been enabled with an undervoltage condition since the last time this bit was read.	S	RC
1	0	IN_OC_I	Input Overcurrent Interrupt. 0 = The input overcurrent has not occurred since the last time this bit was read. 1 = The input overcurrent has occurred since the last time this bit was read.	S	RC
0	0	EREG_I	External Regulator Output Flag. 0 = EREG_POK is high. Either the regulators are OK, or EREG_POK is not monitored (EREG_M = 1). 1 = EREG_POK has had a falling edge while EREG_EN1 or EREG_EN2 are assigned to a flexible power sequencer (EREG1MSTRASGN OR EREG2MSTRASGN) and the On/Off controller was listening to the EREG_POK signal (EREG_INT_EN = 1). This means that the device powered down due to EREG_POK.	S	RC

GLBL_INT1

Register Name	GLBL_INT1
I²C Slave Address	0x60
Register Address	0x01
Reset Value (HEX)	0x00
Reset Value (BIN)	0b00000000
Reset Type	S
Access Type	RC
Register Type	INT

Bit	Default	Bit Name	Description	Reset	Access Type
7	0	INOVLO_R_I	Input Overvoltage Flag. 0 = The Input Voltage to the inrush controller has NOT risen above OVLO (V_{IN} < V_{INOVLO} (Rising)) since the last time this bit was read. 1 = The Input Voltage to the inrush controller has risen above OVLO (V_{IN} > V_{INOVLO} (Rising)) since the last time this bit was read.	S	RC
6	0	SYSUVLO_F_I	System Undervoltage Flag. 0 = The system voltage has NOT fallen below UVLO (V_{SYS} > $V_{SYSUVLO}$ (falling)) since the last time this bit was read. 1 = The system voltage has fallen below UVLO (V_{SYS} < $V_{SYSUVLO}$ (falling)) since the last time this bit was read.	S	RC
5	0	SYSRST_F_I	System Reset Falling Flag. 0 = The system voltage has NOT dropped below the reset threshold (V_{SYS} > V_{SYS_RESET} (falling)) since the last time this bit was read. 1 = The system voltage has dropped below the reset threshold (V_{SYS} < V_{SYS_RESET} (falling)) since the last time this bit was read.	S	RC
4	0	SYSBO_F_I	System Brownout Falling Flag. 0 = The system voltage has NOT dropped below the brownout threshold (V_{SYS} > V_{SYS_BO} (falling)) since the last time this bit was read. 1 = The system voltage has dropped below the brownout threshold (V_{SYS} < V_{SYS_BO} (falling)) since the last time this bit was read.	S	RC
3	0	TOVLD_I	Junction Temperature Overload Flag. 0 = The junction temperature has NOT risen above the shutdown threshold (T_J < T_{JOVLD}) since the last time this bit was read. 1 = The junction temperature has risen above the shutdown threshold (T_J > T_{JOVLD}) since the last time this bit was read.	S	RC
2	0	SFT_OFF_I	Software Initiated Power Down Flag. 0 = Neither the SFT_OFF_SYSRST nor the SFT_OFF_NORST flags were set to 1 since the last time this bit was read. 1 = Either the SFT_OFF_SYSRST or the SFT_OFF_NORST flags were set to 1 since the last time this bit was read.	S	RC

1	0	I2CWD_I	I²C Watchdog Timer Interrupt. 0 = The I²C Watchdog timer interrupt has NOT occurred since the last time this bit was read. 1 = The I²C Watchdog timer interrupt has occurred since the last time this bit was read.	S	RC
0	0	BRDY_I	BIAS Ready OK Interrupt. 0 = Bias ready interrupt has not occurred since the last time this bit was read. 1 = Bias ready interrupt has occurred since the last time this bit was read.	S	RC

GLBLCNFG0

Register Name	GLBL_CNFG0
I²C Slave Address	0x60
Register Address	0x16
Reset Value (HEX)	0x18
Reset Value (BIN)	0b00011000 (CID4=0x7)
Reset Type	O
Access Type	Mixed
Register Type	CNFG

Bit	Default	Bit Name	Description	Reset	Access Type
7	0	DEVSLP_BLEED_ENB	Enables Bleed Function During DevSlp. 0 = Bleed function is On during DevSlp, BLEED_OK_Comparator is turned on during DevSlp exit, and not available during the whole DevSlp state. 1 = Bleed Function is OFF during DevSlp.	O	R/W
6	0	ALT_LP_REQ_EN	ALT_LPREQ_EN Mode (Slave Mode Only). 0 = LP_REQ is controlled by CLOGIC 1 = LP_REQ is controlled by I²C	O	R/W
5	0	ALT_LP_REQ	The LP_REQ output value when ALT_LP_REQ_EN = 1 (open drain) 0 = Programmed logic Low 1 = Programmed logic High	O	R/W
4	x	LP_REQ_T_EN	Enable LP_REQ De-Assertion Timer. 0 = LP_REQ de-assertion delay timer disabled. LP_REQ de-asserts as soon as DevSlp Exit Flow is entered. 1 = LP_REQ De-assertion delay timer enabled. LP_REQ de-asserts 20ms after the DevSlp Exit Flow is entered. NOTE: There is a 1 clock (@31.5kHz) delay between LP_MODE's debounced falling edge and LP_REQ falling.	O	R/W
3	x	T_BO_EN	Enable Brownout Timer. 0 = Brownout timer is disabled. When system voltage (V_{SYS}) falls below the brownout threshold (V_{SYS_BO}), the PMIC waits in the Brownout state until either it rises above the rising brownout threshold or a condition to initiate power down is satisfied. 1 = Brownout timer is enabled. When system voltage (V_{SYS}) falls below the brownout threshold (V_{SYS_BO}), the PMIC waits in the Brownout state only until the brownout timer expires or another condition to initiate power down sequence is satisfied.	O	R/W

2	0	DISWK	Disable Wake Up. 0 = When the system voltage (V_{SYS}) is above the reset threshold (V_{SYS_RESET}), the PMIC proceeds with the power-up sequence. See On/Off controller for details. 1 = The PMIC remains in the OFF state even when the system voltage (V_{SYS}) is above the reset threshold (V_{SYS_RESET}).	O	R/W
1	0	SFT_OFF_NORST	Software Power-Off Reset Configuration. 0b00 = No Action (No power-down sequence or reset) 0b01 = Initiate the software power-off sequence with full register reset. 0b10 = Initiate the software power-off sequence without any register reset. Note that both these bits are self-clearing and so always read 0 when read. Note that the setting of 0b11 is reserved. Only one of SFT_OFF_SYSRST, SFT_OFF_NORST is intended to be set during any given write.	O	W
0	0	SFT_OFF_SYSRST		O	W

GLBL_CNFG1

Register Name	GLBL_CNFG1
I²C Slave Address	0x60
Register Address	0x17
Reset Value (HEX)	0x00
Reset Value (BIN)	0b00000000 (CID4=0x7)
Reset Type	O
Access Type	R/W
Register Type	CNFG

Bit	Default	Bit Name	Description	Reset	Access Type
7	0	RSVD	Reserved. Unutilized bit. Write to 0. Reads are don't care.	O	R/W
6	0	ALT_EREG2EN_EN	ALT_EREG2EN_EN Mode. 0 = EREG_EN2 is controlled by CLOGIC. 1 = EREG2_EN is controlled by I²C OPMD bits, Force disable EREG_EN2's pull-up resistor path, EPI is selected to (V_{OUT}-V_{diode}).	O	R/W
5	x	SYSRSTTH[3:0]	SYS Reset Threshold Voltage (V_{SYS_RESET}). This 4-bit configuration is a linear transfer function for the "falling" threshold that starts at 2.650V and ends at 4.150V, with 100mV increments.	O	R/W
4	x			O	R/W
3	x			O	R/W
2	x			O	R/W
1	x	SYSRSTHYS[1:0]	SYS Reset Threshold Hysteresis. This 2-bit configuration is a linear transfer function that starts at 150mV and ends at 300mV, with 50mV increments.	O	R/W
0	x			O	R/W

GLBL_CNFG2

Register Name	GLBL_CNFG2
I²C Slave Address	0x60
Register Address	0x18
Reset Value (HEX)	0xC0
Reset Value (BIN)	0b11000000 (CID4=0x7)
Reset Type	O
Access Type	R/W
Register Type	CNFG

Bit	Default	Bit Name	Description	Reset	Access Type
7	1	SYS_BO_PR[1:0]	System Voltage Brownout Comparator Response Time and Quiescent Current. This 2-bit configuration provides four response times with corresponding supply currents. Refer to the electrical characteristics table for details on the response time and Iq for each setting. 2'b00 = Fast 2'b01 = Med-Fast 2'b10 = Med-Slow 2'b11 = Slow	O	R/W
6	1			O	R/W
5	x	SYSBOTH[3:0]	SYS Brownout Threshold Voltage (V_{SYS_BO}). This 4-bit configuration is a linear transfer function for the falling threshold that starts at 2.800V and ends at 4.300V, with 100mV increments. See the SYS_BO_THR tab in this spreadsheet for a complete table of values.	O	R/W
4	x			O	R/W
3	x			O	R/W
2	x			O	R/W
1	x	SYSBOHYS[1:0]	SYS Brownout Threshold Hysteresis. This 2-bit configuration is a linear transfer function that starts at 150mV, ends at 300mV, with 50mV increments.	O	R/W
0	x			O	R/W

GLBL_CNFG3

Register Name	GLBL_CNFG3
I²C Slave Address	0x60
Register Address	0x19
Reset Value (HEX)	0x80
Reset Value (BIN)	0b10000000 (CID4=0x7)
Reset Type	O
Access Type	R/W
Register Type	CNFG

Bit	Default	Bit Name	Description	Reset	Access Type
7	x	HICCUP_EN	Enable Hiccup Counter Feature. 0 = Disable Hiccup counter 1 = Enable Hiccup counter	O	R/W
6	0	RSVD	Reserved. Unutilized bit. Write to 0. Reads are don't care.	O	R/W
5	x	WP_L_DLY[1:0]	Write Protect Output De-Assert Delay Time. This 2-bit configuration provides programmable delay options between the WP_L internal signal de-assertion and the external pin de-assertion. Note: When this delay is 0, WP_L and RESET_L outputs rise at the same time. 2'b00 = 0µs 2'b10 = 508µs 2'b10 = 508µs 2'b11 = 1016µs	O	R/W
4	x			O	R/W
3	x	RST_L_DLY[1:0]	RESET_L Output De-Assert Delay Time. This 2-bit configuration provides programmable delay options between the RESET_L internal signal de-assertion and the external pin de-assertion. Refer to the Flexible Power Sequencer Timing Diagrams (Figure 6) for a visual representation of this delay. Note: When this delay is 0, RESET_L and PGOOD outputs rise at the same time. 2'b00 = 0µs 2'b01 = 254µs 2'b10 = 508µs 2'b11 = 1016µs	O	R/W
2	x			O	R/W
1	x	PG_DLY[1:0]	PGOOD Output De-Assert Delay Time. This 2-bit configuration provides programmable delay options between the PGOOD internal signal de-assertion and the external pin de-assertion. Refer to the Flexible Power Sequencer Timing Diagrams (Figure 6) for a visual representation of this delay. 2'b00 = 31µs 2'b01 = 254µs 2'b10 = 508µs 2'b11 = 1016µs	O	R/W
0	x			O	R/W

GLBL_INTM

Register Name	GLBL_INTM
I²C Slave Address	0x60
Register Address	0x06
Reset Value (HEX)	0x02
Reset Value (BIN)	0b00000010 (CID4=0x7)
Reset Type	O
Access Type	R/W
Register Type	INTM

Bit	Default	Bit Name	Description	Reset	Access Type
7	0	RSVD	Reserved. Unutilized bit. Write to 0. Reads are don't care.	O	R/W
6	0	RSVD	Reserved. Unutilized bit. Write to 0. Reads are don't care.	O	R/W
5	0	RSVD	Reserved. Unutilized bit. Write to 0. Reads are don't care.	O	R/W
4	0	SYSRST_F_M	Mask for SYSRST_F_I Flag to PGOOD_INT. 0 = Unmasked. SYSRST_F_I is unmasked for PGOOD_INT, when SYSRST_F_I = 1 it causes a power-down event. 1 = Masked. SYSRST_F_I is masked for PGOOD_INT, when SYSRST_F_I = 1 it does not cause a power-down event.	O	R/W
3	x	UV_LSW_M	Output Undervoltage Interrrupt Mask to PGOOD. 0 = LSW_POK is unmasked for PGOOD, hence when UV_LSW1_I or UV_LSW2_I or UV_LSW3_I is set it causes a power-down event. 1 = LSW_POK is masked for PGOOD, hence when UV_LSW1_I or UV_LSW2_I or UV_LSW3_I is set it does not cause a power-down event.	O	R/W
2	x	UV_LDO_M	Output Undervoltage Interrrupt Mask to PGOOD 0 = LDO_POK is unmasked for PGOOD, hence the UV_LDO_I causes a power-down event. 1 = LDO_POK is masked for PGOOD, hence the UV_LDO_I does not cause a power-down event.	O	R/W
1	x	IN_OC_M	Input Overcurrent Interrupt Mask to PGOOD. 0 = IN_OC_POK is unmasked for PGOOD, hence the IN_OC_I causes a power-down event. 1 = IN_OC_POK is masked for PGOOD, hence the IN_OC_I does not cause a power-down event.	O	R/W
0	x	EREG_M	Mask for EREG_POK Output Flag to PGOOD and On/Off Controller. 0 = EREG_POK going low causes the device to power down. 1 = The EREG_POK signal does not cause the device to power down. See the EREG_POK section for more information.	O	R/W

HICCUP_CNFG

Register Name	HICCUP_CNFG
I²C Slave Address	0x60
Register Address	0x28
Reset Value (HEX)	0x1C
Reset Value (BIN)	0b00011100
Reset Type	S
Access Type	Mixed
Register Type	CNFG

Bit	Default	Bit Name	Description	Reset	Access Type
7	0	HICCUP_CNT_LIM[5:0]	Hiccup Counter Limit. This is an abbreviated explanation. See the data sheet for more information. HICCUP_CNT_LIM = 0: If an issue occurs that drives the device into the power-down cycle, it stays in the Off state. In other words, there are no hiccup retry events. HICCUP_CNT_LIM = 1 to 31: If an issue occurs that drives the device into a power-down cycle, the device increments the hiccup count (HICCUP_CNT + 1) and then initiates the power-down sequence to enter the Off state. Once in the Off state, if HICCUP_CNT < HICCUP_CNT_LIM, then the device automatically turns back on. If in the Off state and HICCUP_CNT == HICCUP_CNT_LIM, then the device stays in the Off state. To recover a system that has HICCUP_CNT == HICCUP_CNT_LIM while in the Off state, either power cycle the system or reset the hiccup counter through software (HICCUP_CNT_RESET=1).	S	R/W
6	0			S	R/W
5	0			S	R/W
4	1			S	R/W
3	1			S	R/W
2	1			S	R/W
1	0	HICCUP_CNT_RESET	Hiccup Counter Reset. Write 1 to clear the HICCUP_CNT_EXPIRE_RONLY Note: This register bit always returns 0 on read access.	S	R/W
0	0	HICCUP_CNT_EXPIRE_ROnly	Hiccup Counter Status. 0 = Hiccup counts have not reached the hiccup counter limit. 1 = Hiccup counts have reached the hiccup counter limit.	S	R

GLBL_STAT

Register Name	GLBL_STAT
I²C Slave Address	0x60
Register Address	0x05
Reset Value (HEX)	0x0F
Reset Value (BIN)	0b00001111
Reset Type	O
Access Type	R
Register Type	STTS

Bit	Default	Bit Name	Description	Reset	Access Type
7	0	RSVD	Reserved. Unutilized bit. Write to 0. Reads are don't care.	O	R
6	0	RSVD	Reserved. Unutilized bit. Write to 0. Reads are don't care.	O	R
5	0	RSVD	Reserved. Unutilized bit. Write to 0. Reads are don't care.	O	R
4	0	RSVD	Reserved. Unutilized bit. Write to 0. Reads are don't care.	O	R
3	1	UV_LDO_S	Output Undervoltage Status. 0 = LDO is enabled and LDO output has not fallen below the falling UV threshold or has risen above the rising UV threshold, OR, LDO is disabled. 1 = LDO is enabled and LDO output HAS fallen below the falling UV threshold or has NOT risen above the rising UV threshold.	O	R
2	1	EREG_POK_S	External Regulator POK Status. This bit is an inverted reflection of the logic state of the EREG_POK input pin. 0 = EREG_POK=1 AND (EREG1MSTRASGN = 1 OR EREG2MSTRASGN=1) 1 = EREG_POK=0 OR (EREG1MSTRASGN = 0 AND EREG2MSTRASGN = 0)	O	R
1	1	SYSBO_S	SYS Brownout Status. 0 = System voltage is not in brownout. V_{SYS} has risen above V_{SYS_BO} (Rising) and not fallen below V_{SYS_BO} (falling) 1 = System voltage is in brownout. V_{SYS} has not risen above V_{SYS_BO} (Rising) or has fallen below the V_{SYS_BO} (falling)	O	R
0	1	IN_OC_S	SYS Reset Status. 0 = Input current is lower than the Overcurrent limit. 1 = Input current is higher than the Overcurrent limit.	O	R

MSTRx_yFPS [x=0,1,2; y=x+3]

Register Name	MSTRx_yFPS		
I²C Slave Address	0x60		
Register Address	0x1A – 0x1C		
Reset Value (HEX)	0x52	0x03	0x00
Reset Value (BIN)	0b01010010 (CID4=0x7)	0b00000011 (CID4=0x7)	0b00000000 (CID4=0x7)
Reset Type	O		
Access Type	R/W		
Register Type	CNFG		

Bit	Default	Bit Name	Description	Reset	Access Type
7	0	RSVD	Reserved. Unutilized bit. Write to 0. Reads are don't care.	O	R/W
6	x	MSTRx_yDNF[2:0]	Power-Down Sequence Slot Duration Options for Master x and Master y. 3'b000 = 31µs 3'b001 = 63µs 3'b010 = 127µs 3'b011 = 253µs 3'b100 = 508µs 3'b101 = 984µs 3'b110 = 1936µs 3'b111 = 3904µs	O	R/W
5	x			O	R/W
4	x			O	R/W
3	0	RSVD	Reserved. Unutilized bit. Write to 0. Reads are don't care.	O	R/W
2	x	MSTRx_yUPF[2:0]	Power-Up Sequence Slot Duration Options for Master x and Master y. 3'b000 = 31µs 3'b001 = 63µs 3'b010 = 127µs 3'b011 = 253µs 3'b100 = 508µs 3'b101 = 984µs 3'b110 = 1936µs 3'b111 = 3904µs	O	R/W
1	x			O	R/W
0	x			O	R/W

BUCKxFPS [x=1,2,3]

Register Name	BUCKxFPS		
I²C Slave Address	0x60		
Register Address	0x1D – 0x1F		
Reset Value (HEX)	0x97	0xC3	0x83
Reset Value (BIN)	0b10010111 (CID4=0x7)	0b11000011 (CID4=0x7)	0b10000011 (CID4=0x7)
Reset Type	O		
Access Type	R/W		
Register Type	CNFG		

Bit	Default	Bit Name	Description	Reset	Access Type
7	x	BUCKxMSTRASGN	Assign to a Flexible Power Sequencer Master. 0 = BUCKx is not assigned to any FPS Master. BUCKxMSTR[2:0] is ignored. 1 = BUCKx is assigned to the FPS master configured by BUCKxMSTR[2:0].	O	R/W
6	x	BUCKxMSTR[2:0]	BUCKx Master Assignment. 3'b000 = FPS Master 0 3'b001 = FPS Master 1 3'b010 = FPS Master 2 3'b011 = FPS Master 3 3'b100 = FPS Master 4 3'b101 = FPS Master 5 3'b110 = Reserved 3'b111 = Reserved	O	R/W
5	x			O	R/W
4	x			O	R/W
3	x	BUCKxUPSLT[1:0]	BUCKx Power-Up Sequence Slot Number. 2'b00 = Slot 0 2'b01 = Slot 1 2'b10 = Slot 2 2'b11 = Slot 3	O	R/W
2	x			O	R/W
1	x	BUCKxDNSLT[1:0]	BUCKx Power-Down Sequence Slot Number. 2'b00 = Slot 0 2'b01 = Slot 1 2'b10 = Slot 2 2'b11 = Slot 3	O	R/W
0	x			O	R/W

LDOFPS

Register Name	LDOFPS
I²C Slave Address	0x60
Register Address	0x20
Reset Value (HEX)	0x97
Reset Value (BIN)	0b10010111 (CID4=0x7)
Reset Type	O
Access Type	R/W
Register Type	CNFG

Bit	Default	Bit Name	Description	Reset	Access Type
7	x	LDOMSTRASGN	Assign to a Flexible Power Sequencer Master. 0 = LDO is not assigned to any FPS Master. LDOMSTR[2:0] is ignored. 1 = LDO is assigned to the FPS master configured by LDOMSTR[2:0].	O	R/W
6	x	LDOMSTR[2:0]	LDO Master Assignment. 3'b000 = FPS Master 0 3'b001 = FPS Master 1 3'b010 = FPS Master 2 3'b011 = FPS Master 3 3'b100 = FPS Master 4 3'b101 = FPS Master 5 3'b110 = Reserved 3'b111 = Reserved	O	R/W
5	x			O	R/W
4	x			O	R/W
3	x	LDOUPSLT[1:0]	LDO Power Up Sequence Slot Number. 2'b00 = Slot 0 2'b01 = Slot 1 2'b10 = Slot 2 2'b11 = Slot 3	O	R/W
2	x			O	R/W
1	x	LDODNSLT[1:0]	LDO Power Down Sequence Slot Number. 2'b00 = Slot 0 2'b01 = Slot 1 2'b10 = Slot 2 2'b11 = Slot 3	O	R/W
0	x			O	R/W

LSWxFPS [x=1,2,3]

Register Name	LSWxFPS		
I²C Slave Address	0x60		
Register Address	0x21 – 0x23		
Reset Value (HEX)	0x97	0x00	0x00
Reset Value (BIN)	0b10010111 (CID4=0x7)	0b00000000 (CID4=0x7)	0x00000000 (CID4=0x7)
Reset Type	O		
Access Type	R/W		
Register Type	CNFG		

Bit	Default	Bit Name	Description	Reset	Access Type
7	x	LSWxMSTRASGN	Assign to a Flexible Power Sequencer Master. 0 = LSWx is not assigned to any FPS Master. LSWxMSTR[2:0] is ignored. 1 = LSWx is assigned to the FPS master configured by LSWxMSTR[2:0].	O	R/W
6	x	LSWxMSTR[2:0]	LSWx Master Assignment. 3'b000 = FPS Master 0 3'b001 = FPS Master 1 3'b010 = FPS Master 2 3'b011 = FPS Master 3 3'b100 = FPS Master 4 3'b101 = FPS Master 5 3'b110 = Reserved 3'b111 = Reserved	O	R/W
5	x			O	R/W
4	x			O	R/W
3	x	LSWxUPSLT[1:0]	LSWx Power-Up Sequence Slot Number. 2'b00 = Slot 0 2'b01 = Slot 1 2'b10 = Slot 2 2'b11 = Slot 3	O	R/W
2	x			O	R/W
1	x	LSWxDNSLT[1:0]	LSWx Power-Down Sequence Slot Number. 2'b00 = Slot 0 2'b01 = Slot 1 2'b10 = Slot 2 2'b11 = Slot 3	O	R/W
0	x			O	R/W

EREGxFPS [x=1,2]

Register Name	EREGxFPS	
I²C Slave Address	0x60	
Register Address	0x24 – 0x25	
Reset Value (HEX)	0x85	0x97
Reset Value (BIN)	0b10000101 (CID4=0x7)	0b10010111 (CID4=0x7)
Reset Type	O	
Access Type	R/W	
Register Type	CNFG	

Bit	Default	Bit Name	Description	Reset	Access Type
7	x	EREGxMSTRASGN	Assign to a Flexible Power Sequencer Master. 0 = EREGx is not assigned to any FPS Master. EREGxMSTR[2:0] is ignored. 1 = EREGx is assigned to the FPS master configured by EREGxMSTR[2:0].	O	R/W
6	x	EREGxMSTR[2:0]	EREGx Master Assignment. 3'b000 = FPS Master 0 3'b001 = FPS Master 1 3'b010 = FPS Master 2 3'b011 = FPS Master 3 3'b100 = FPS Master 4 3'b110 = Reserved 3'b101 = FPS Master 5 3'b111 = Reserved	O	R/W
5	x			O	R/W
4	x			O	R/W
3	x	EREGxUPSLT[1:0]	EREGx Power Up Sequence Slot Number. 2'b00 = Slot 0 2'b01 = Slot 1 2'b10 = Slot 2 2'b11 = Slot 3	O	R/W
2	x			O	R/W
1	x	EREGxDNSLT[1:0]	EREGx Power Down Sequence Slot Number. 2'b00 = Slot 0 2'b01 = Slot 1 2'b10 = Slot 2 2'b11 = Slot 3	O	R/W
0	x			O	R/W

OPMD1

Register Name	OPMD1
I²C Slave Address	0x60
Register Address	0x26
Reset Value (HEX)	0x55
Reset Value (BIN)	0b01010101 (CID4=0x7)
Reset Type	O
Access Type	R/W
Register Type	CNFG

Bit	Default	Bit Name	Description	Reset	Access Type
7	0	SLPEN_RST	Enable the RESET_L Signal in DevSlp Mode (Slave Mode Only). 0 = The DevSlp Entry sequence does not do anything with RESET_L. 1 = The DevSLP Entry sequence sets RESET_L low.	O	R/W
6	1	SLPEN_WP	Enable the WP_L Signal in DevSlp Mode (Slave Mode Only). 0 = The DevSlp Entry sequence does not do anything with WP_L. 1 = The DevSlp Entry sequence sets WP_L low.	O	R/W
5	x	BUCK3OPMD[1:0]	BUCK3 Output Power Mode. See the Buck and LDO Power Mode Control section for a full description of this control.	O	R/W
4	x			O	R/W
3	x	BUCK2OPMD[1:0]	BUCK2 Output Power Mode. See the Buck and LDO Power Mode Control section for a full description of this control.	O	R/W
2	x			O	R/W
1	x	BUCK1OPMD[1:0]	BUCK1 Output Power Mode. See the Buck and LDO Power Mode Control section for a full description of this control.	O	R/W
0	x			O	R/W

OPMD2

Register Name	OPMD2
I²C Slave Address	0x60
Register Address	0x27
Reset Value (HEX)	0x01
Reset Value (BIN)	0b00000001 (CID4=0x7)
Reset Type	O
Access Type	R/W
Register Type	CNFG

Bit	Default	Bit Name	Description	Reset	Access Type
7	0	RSVD	Reserved. Unutilized bit. Write to 0. Reads are don't care.	O	R/W
6	x	EREG1OPMD	EREG1 Output Power Mode. See the Dedicated Output Power Mode Control section for a full description of this control. NOTE: Do not change this bit on during operation through I²C because it changes the polarity of EREG_EN1 pin, which could cause unforeseen operation of the system.	O	R/W
5	x	EREG2OPMD	EREG2 Output Power Mode. See the Dedicated Output Power Mode Control section for a full description of this control. NOTE: Do not change this bit on during operation through I²C because it changes the polarity of EREG_EN2 pin, which could cause unforeseen operation of the system.	O	R/W
4	x	LSW3OPMD	LSW3 Output Power Mode. See the Load Switch Power Mode Control section for a full description of this control.	O	R/W
3	x	LSW2OPMD	LSW2 Output Power Mode. See the Load Switch Power Mode Control section for a full description of this control.	O	R/W
2	x	LSW1OPMD	LSW1 Output Power Mode. See the Load Switch Power Mode Control section for a full description of this control.	O	R/W
1	x	LDOOPMD[1:0]	LDO Output Power Mode. See the Buck and LDO Power Mode Control section for a full description of this control.	O	R/W
0	x			O	R/W

CID0

Register Name	CID0
I²C Slave Address	0x60
Register Address	0x08
Reset Value (HEX)	OTP
Reset Value (BIN)	0bxxxxxxxx
Reset Type	S
Access Type	R
Register Type	DATA

Bit	Default	Bit Name	Description	Reset	Access Type
7	x	SR[7:0]	Serial Number Least Significant Byte. SR[23:16]+SR[15:8]+SR[7:0] form a 24-bit serial number.	S	R
6	x			S	R
5	x			S	R
4	x			S	R
3	x			S	R
2	x			S	R
1	x			S	R
0	x			S	R

CID1

Register Name	CID1
I²C Slave Address	0x60
Register Address	0x09
Reset Value (HEX)	OTP
Reset Value (BIN)	0bxxxxxxxx
Reset Type	S
Access Type	R
Register Type	DATA

Bit	Default	Bit Name	Description	Reset	Access Type
7	x	SR[15:8]	Serial Number Middle Byte. SR[23:16]+SR[15:8]+SR[7:0] form a 24-bit serial number.	S	R
6	x			S	R
5	x			S	R
4	x			S	R
3	x			S	R
2	x			S	R
1	x			S	R
0	x			S	R

CID2

Register Name	CID2
I²C Slave Address	0x60
Register Address	0x0A
Reset Value (HEX)	OTP
Reset Value (BIN)	0bxxxxxxxx
Reset Type	S
Access Type	R
Register Type	DATA

Bit	Default	Bit Name	Description	Reset	Access Type
7	x	SR[23:16]	Serial Number Most Significant Byte. SR[23:16]+SR[15:8]+SR[7:0] form a 24-bit serial number.	S	R
6	x			S	R
5	x			S	R
4	x			S	R
3	x			S	R
2	x			S	R
1	x			S	R
0	x			S	R

CID3

Register Name	CID3
I²C Slave Address	0x60
Register Address	0x0B
Reset Value (HEX)	OTP & Metal
Reset Value (BIN)	0byyyy0xxx
Reset Type	S
Access Type	R
Register Type	DATA

Bit	Default	Bit Name	Description	Reset	Access Type
7	y	DIDM[3:0]	Device Identification Metal. 4'b0000 = Initial Metal Mask (Device Version 1). 4'b0001 = First metal revision (Device Version 2). 4'b0010 and above are reserved for future revisions	S	R
6	y			S	R
5	y			S	R
4	y			S	R
3	0	MT_OTP	Metal Option Read. 0=Original Buck Spike; read back 6 1=Reduced Buck Spike; read back 5	S	R
2	x	SBT[2:0]	Maxim Production Test Code. 3'b011 or 3'b101 indicate a production part that has passed Maxim's end-of-line test procedure. Values other than 3'b011 or 3'b101 indicate a pre-production part that has been released as an engineering sample. Engineering samples might not be fully tested.	S	R
1	x			S	R
0	x			S	R

CID4

Register Name	CID4
I²C Slave Address	0x60
Register Address	0x0C
Reset Value (HEX)	OTP
Reset Value (BIN)	0b00000111 (CID4=0x7)
Reset Type	S
Access Type	R
Register Type	DATA

Bit	Default	Bit Name	Description	Reset	Access Type
7	x	DRV[7:0]	Device OTP Version. These bits track the OTP configuration for each part.	S	R
6	x			S	R
5	x			S	R
4	x			S	R
3	x			S	R
2	x			S	R
1	x			S	R
0	x			S	R

Current Sense Amplifier

CNFG_CSA

Register Name	CNFG_CSA
I²C Slave Address	0x60
Register Address	0x79
Reset Value (HEX)	0x03
Reset Value (BIN)	0b00000011 (CID4=0x7)
Reset Type	O
Access Type	R/W
Register Type	CNFG

Bit	Default	Bit Name	Description	Reset	Access Type
7	0	RSVD	Reserved for future use.	O	R/W
6	0	RSVD	Reserved for future use.	O	R/W
5	0	RSVD	Reserved for future use.	O	R/W
4	0	RSVD	Reserved for future use.	O	R/W
3	0	RSVD	Reserved for future use.	O	R/W
2	0	RSVD	Reserved for future use.	O	R/W
1	x	CSTH_OPT[1:0]	Current Sense Level. 2'b00 = 1.50A 2'b01 = 1.75A 2'b10 = 2.00A 2'b11 = 2.25A	O	R/W
0	x			O	R/W

Buck Regulators

BUCK_INT

Register Name	BUCK_INT
I²C Slave Address	0x60
Register Address	0x02
Reset Value (HEX)	0x00
Reset Value (BIN)	0b00000000
Reset Type	S
Access Type	RC
Register Type	INT

Bit	Default	Bit Name	Description	Reset	Access Type
7	0	RSVD	Reserved. Unutilized bit. Write to 0. Reads are don't care.	S	RC
6	0	RSVD	Reserved. Unutilized bit. Write to 0. Reads are don't care.	S	RC
5	0	BUCK3_OV_I	Output Overvoltage Interrupt. 0 = BUCK3 output HAS NOT risen above the rising OV threshold since the last time this bit was read. 1 = BUCK3 output HAS risen above the rising OV threshold since the last time this bit was read.	S	RC
4	0	BUCK3_UV_I	Output Undervoltage Interrupt. 0 = BUCK3 was enabled and BUCK3 output HAS NOT fallen below the falling UV threshold since the last time this bit was read, OR, BUCK3 was disabled. 1 = BUCK3 was enabled and BUCK3 output HAS fallen below the falling UV threshold since the last time this bit was read.	S	RC
3	0	BUCK2_OV_I	Output Overvoltage Interrupt. 0 = BUCK2 output HAS NOT risen above the rising OV threshold since the last time this bit was read. 1 = BUCK2 output HAS risen above the rising OV threshold since the last time this bit was read.	S	RC
2	0	BUCK2_UV_I	Output Undervoltage Interrupt. 0 = BUCK2 was enabled and BUCK2 output HAS NOT fallen below the falling UV threshold since the last time this bit was read, OR, BUCK2 was disabled. 1 = BUCK2 was enabled and BUCK2 output HAS fallen below the falling UV threshold since the last time this bit was read.	S	RC
1	0	BUCK1_OV_I	Output Overvoltage Interrupt. 0 = BUCK1 output HAS NOT risen above the rising OV threshold since the last time this bit was read. 1 = BUCK1 output HAS risen above the rising OV threshold since the last time this bit was read.	S	RC
0	0	BUCK1_UV_I	Output Undervoltage Interrupt. 0 = BUCK1 was enabled and BUCK1 output HAS NOT fallen below the falling UV threshold since the last time this bit was read, OR, BUCK1 was disabled. 1 = BUCK1 was enabled and BUCK1 output HAS fallen below the falling UV threshold since the last time this bit was read.	S	RC

BUCK_INTM

Register Name	BUCK_INTM
I²C Slave Address	0x60
Register Address	0x07
Reset Value (HEX)	0x00
Reset Value (BIN)	0b00000000 (CID4=0x7)
Reset Type	O
Access Type	R/W
Register Type	INTM

Bit	Default	Bit Name	Description	Reset	Access Type
7	0	RSVD	Reserved. Unutilized bit. Write to 0. Reads are don't care.	O	R/W
6	0	RSVD	Reserved. Unutilized bit. Write to 0. Reads are don't care.	O	R/W
5	x	BUCK3_OV_M	Output Overvoltage Interrupt Mask to Only Mask PGOOD_INT. 0 = During an Output Overvoltage event, BUCK3_OV_I is set to 1 along with PGOOD_INT and initiates a power-down event. 1 = During an Output Overvoltage event, BUCK3_OV_I is set to 1 but NOT PGOOD_INT and does not initiate a power-down event.	O	R/W
4	x	BUCK3_UV_M	Output Undervoltage Interrrupt Mask to Only Mask PGOOD_INT. 0 = During an Output Undervoltage event, BUCK3_UV_I is set to 1 along with PGOOD_INT and initiates a power-down event. 1 = During an Output Undervoltage event, BUCK3_UV_I is set to 1 but NOT PGOOD_INT and does not initiate a power-down event.	O	R/W
3	x	BUCK2_OV_M	Output Overvoltage Interrrupt Mask to Only Mask PGOOD_INT. 0 = During an Output Overvoltage event, BUCK2_OV_I is set to 1 along with PGOOD_INT and initiates a power-down event. 1 = During an Output Overvoltage event, BUCK2_OV_I is set to 1 but NOT PGOOD_INT and does not initiate a power-down event.	O	R/W
2	x	BUCK2_UV_M	Output Undervoltage Interrrupt Mask to Only Mask PGOOD_INT. 0 = During an Output Undervoltage event, BUCK2_UV_I is set to 1 along with PGOOD_INT and initiate a power-down event. 1 = During an Output Undervoltage event, BUCK2_UV_I is set to 1 but NOT PGOOD_INT and does not initiate a power-down event.	O	R/W

1	x	BUCK1_OV_M	Output Overvoltage Interrrupt Mask to Only Mask PGOOD_INT. 0 = During an Output Overvoltage event, BUCK1_OV_I is set to 1 along with PGOOD_INT and initiate a power-down event. 1 = During an Output Overvoltage event, BUCK1_OV_I is set to 1 but NOT PGOOD_INT and does not initiate a power-down event.	O	R/W
0	x	BUCK1_UV_M	Output Undervoltage Interrrupt Mask to Only Mask PGOOD_INT. 0 = During an Output Undervoltage event, BUCK1_UV_I will be set to 1 along with PGOOD_INT and initiate a power-down event. 1 = During an Output Under-Voltage event, BUCK1_UV_I will be set to 1 but NOT PGOOD_INT and will not initiate a power-down event.	O	R/W

BUCK_STAT

Register Name	BUCK_STAT
I²C Slave Address	0x60
Register Address	0x04
Reset Value (HEX)	0x00
Reset Value (BIN)	0b00000000
Reset Type	O
Access Type	R
Register Type	STTS

Bit	Default	Bit Name	Description	Reset	Access Type
7	0	RSVD	Reserved. Unutilized bit. Write to 0. Reads are don't care.	O	R
6	0	RSVD	Reserved. Unutilized bit. Write to 0. Reads are don't care.	O	R
5	0	BUCK3_OV_S	Output Overvoltage Interrupt. 0 = BUCK3 output HAS NOT risen above the rising OV threshold. 1 = BUCK3 output HAS risen above the rising OV threshold.	O	R
4	0	BUCK3_UV_S	Output Undervoltage Interrupt. 0 = BUCK3 is enabled and BUCK3 output HAS NOT fallen below the falling UV threshold OR, BUCK3 is disabled. 1 = BUCK3 is enabled and BUCK3 output HAS fallen below the falling UV threshold.	O	R
3	0	BUCK2_OV_S	Output Overvoltage Interrupt. 0 = BUCK2 output HAS NOT risen above the rising OV threshold. 1 = BUCK2 output HAS risen above the rising OV threshold.	O	R
2	0	BUCK2_UV_S	Output Undervoltage Interrupt. 0 = BUCK2 is enabled and BUCK2 output HAS NOT fallen below the falling UV threshold OR, BUCK2 is disabled. 1 = BUCK2 is enabled and BUCK2 output HAS fallen below the falling UV threshold.	O	R
1	0	BUCK1_OV_S	Output Overvoltage Interrupt. 0 = BUCK1 output HAS NOT risen above the rising OV threshold. 1 = BUCK1 output HAS risen above the rising OV threshold.	O	R
0	0	BUCK1_UV_S	Output Undervoltage Interrupt. 0 = BUCK1 is enabled and BUCK1 output HAS NOT fallen below the falling UV threshold OR, BUCK1 is disabled. 1 = BUCK1 is enabled and BUCK1 output HAS fallen below the falling UV threshold.	O	R

BUCKxCNFG1 [x=1,2,3]

Register Name	BUCKxCNFG1		
I²C Slave Address	0x60		
Register Address	0x46, 0x4A, 0x4E		
Reset Value (HEX)	0xC0	0x78	0x50
Reset Value (BIN)	0b11000000 (CID4=0x7)	0b01111000 (CID4=0x7)	0b01010000 (CID4=0x7)
Reset Type	O		
Access Type	R/W		
Register Type	CNFG		

Bit	Default	Bit Name	Description	Reset	Access Type
7	x	BUCKxVOUT[7:0] (BUCK1/2) or BUCKxVOUT[6:0] (BUCK3)	BUCK1/2 Output Voltage. This 8-bit configuration is a linear transfer function that starts at 0.6V and ends at 2.194V, with 6.25mV increments. V_{BUCK1}=0.6V+(BUCK1VOUT[7:0]*6.25mV) or BUCK3 Output Voltage. This 8-bit configuration is a linear transfer function that starts at 0.26V and ends at 1.52V, with 10mV increments. V_{BUCK1}=0.26V+(BUCK1VOUT[7:0]*10mV)	O	R/W
6	x			O	R/W
5	x			O	R/W
4	x			O	R/W
3	x			O	R/W
2	x			O	R/W
1	x			O	R/W
0	x			O	R/W

BUCKxCNFG2 [x=1,2,3]

Register Name	BUCKxCNFG2		
I²C Slave Address	0x60		
Register Address	0x47, 0x4B, 0x4F		
Reset Value (HEX)	0x40	0x40	0x24
Reset Value (BIN)	0b01000000 (CID4=0x7)	0b01000000 (CID4=0x7)	0b00100100 (CID4=0x7)
Reset Type	O		
Access Type	Mixed		
Register Type	CNFG		

Bit	Default	Bit Name	Description	Reset	Access Type
7	0	BLANK	Blank. There is no physical bit at this location. Write to 0. Reads are don't care.	O	R
6	1	BLANK	Blank. There is no physical bit at this location. Write to 0. Reads are don't care.	O	R
5	0	BLANK	Blank. There is no physical bit at this location. Write to 0. Reads are don't care.	O	R
4	0	BLANK	Blank. There is no physical bit at this location. Write to 0. Reads are don't care.	O	R
3	0	RSVD	Reserved. Unutilized bit. Write to 0. Reads are don't care.	O	R/W
2	0	RSVD (BUCK1/2) BUCK3FSREN (BUCK3)	Reserved. Unutilized bit. Write to 0. Reads are don't care. (BUCK1/2) Falling Slew Rate Active-Discharge Enable (BUCK3). 0 = Active Discharge Disabled. BUCK3 is allowed to operate in Skip mode during the time the output voltage decreases (only if BUCK3FPWMEN = 0). In Skip mode, BUCK3 cannot sink current from the output capacitor and the output voltage falling slew rate is a function of the external load. If the external load is heavy, then the output voltage falling slew rate is the fixed output voltage ramp rate. If the external load is light, then the output voltage falling slew rate is a function of the output capacitance and the external load. Note that the internal feedback string always imposes a 2µA load on the output. 1 = Active-Discharge Enabled. BUCK3 operates in forced PWM mode during the time the output voltage decreases. With forced PWM mode enabled, BUCK3 can sink current from the output capacitor to ensure that the output voltage falls at the rate fixed for output voltage ramp. To ensure a smooth output voltage decrease, the PWM mode remains engaged for 50µs after the output voltage decreases to its target voltage.	O	R/W

1	x	BUCKxADDIS	BUCKx Converter Active Discharge Disable. 0 = The active discharge function is enabled. When BUCKx converter is disabled, an internal 100Ω discharge resistor is connected to the output to discharge the energy stored in the output capacitor. When BUCKx converter is enabled, the discharge resistor is disconnected from the output. 1 = The active discharge function is disabled. When BUCKx converter is disabled, the internal 100Ω discharge resistor is not connected to the output, and the discharge rate is dependent on the output capacitance and the load present.	O	R/W
0	0	BUCKxFPWMEN	BUCKx Forced PWM Mode Enable. 0 = BUCKx converter automatically skips pulses under light load conditions, and transfers to fixed frequency operation as the load current increases. 1 = BUCKx converter operates with fixed frequency under all load conditions.	O	R/W

BUCKxCNFG3 [x=1,2,3]

Register Name	BUCKxCNFG3		
I²C Slave Address	0x60		
Register Address	0x48, 0x4C, 0x50		
Reset Value (HEX)	0x46	0x46	0x06
Reset Value (BIN)	0b01000110 (CID4=0x7)	0b01000110 (CID4=0x7)	0b00000110 (CID4=0x7)
Reset Type	O		
Access Type	Mixed		
Register Type	CNFG		

Bit	Default	Bit Name	Description	Reset	Access Type
7	0	BLANK	Blank. There is no bit at this location. Write to 0. Reads are don't care.	O	R
6	1	BLANK	Blank. There is no bit at this location. Write to 0. Reads are don't care.	O	R
5	0	BLANK	Blank. There is no bit at this location. Write to 0. Reads are don't care.	O	R
4	0	BLANK	Blank. There is no bit at this location. Write to 0. Reads are don't care.	O	R
3	0	RSVD	Reserved. Unutilized bit. Write to 0. Reads are don't care.	O	R/W
2	1	BUCKx_BO_PR[1:0]	BUCKx Output Brownout Comparator Pulse Rejection Period. This 2-bit configuration provides four settings for response time (and Iq). 2'b00 = Fast 2'b01 = Medium-Fast 2'b10 = Medium-Slow 2'b11 = Slow	O	R/W
1	1			O	R/W
0	x	BUCKx_OV_THR	BUCKx Output Overvoltage Threshold. This 1-bit configuration provides two options for BUCKx output overvoltage comparator rising threshold, expressed as a % of the output voltage setting (BUCKxVOUT[7:0]) 0 = 108.3% 1 = 116.6% NOTE: With 13µF of effective output capacitance and the 1.2V target output voltage, corners simulations show an overshoot of 133mV (11%) for a 2A to 10mA step in 3.2µs. For prototype margin testing, the tighter 108.3% threshold to screen for potential issues. However, for production devices, use the 116.6% setting.	O	R/W

BUCKxCNFG4 [x=1,2,3]

Register Name	BUCKxCNFG4		
I²C Slave Address	0x60		
Register Address	0x49, 0x4D, 0x51		
Reset Value (HEX)	0x49	0x49	0x59
Reset Value (BIN)	0b01001001 (CID4=0x7)	0b01001001 (CID4=0x7)	0b01011001 (CID4=0x7)
Reset Type	O		
Access Type	Mixed		
Register Type	CNFG		

Bit	Default	Bit Name	Description	Reset	Access Type
7	0	BLANK	Blank. There is no bit at this location. Write to 0. Reads are don't care.	O	R
6	1	BLANK	Blank. There is no bit at this location. Write to 0. Reads are don't care.	O	R
5	0	BLANK	Blank. There is no bit at this location. Write to 0. Reads are don't care.	O	R
4	0	BLANK	Blank. There is no bit at this location. Write to 0. Reads are don't care.	O	R
3	x	BUCKx_BO_THR[1:0]	BUCKx Output Brownout Comparator Falling Threshold. This 2-bit configuration is a linear transfer function, expressed as a % of output voltage setting (BUCKxVOUT[7:0]), that starts at 75%, ends at 90% in 5% increments. 2'b00 = 77% 2'b01 = 81% 2'b10 = 86% 2'b11 = 91% NOTE: With 13µF of effective output capacitance and the 1.2V target output voltage, corners simulations show an undershoot of 195mV (16%) for a 10mA to 2A step in 3.2µs. For prototype margin testing in systems, use the 85% threshold to screen for potential issues. However, for production devices, use the 75% setting.	O	R/W
2	x			O	R/W
1	x	BUCKx_BO_HYS[1:0]	BUCKx Output Brownout Comparator Threshold Hysteresis. Expressed as a % of output voltage setting (BUCKxVOUT[7:0]) 2'b00 = 5% 2'b01 = 10% 2'b10 = 15% 2'b11 = 20%	O	R/W
0	x			O	R/W

BUCK3CNFG5

Register Name	BUCK3CNFG5
I²C Slave Address	0x60
Register Address	0x52
Reset Value (HEX)	0x37
Reset Value (BIN)	0b00110111
Reset Type	O
Access Type	R/W
Register Type	CNFG

Bit	Default	Bit Name	Description	Reset	Access Type
7	0	RSVD	Reserved. Unutilized bit. Write to 0. Reads are don't care.	O	R/W
6	0	BUCK3VDVS[6:0]	BUCK3 Output Voltage during Low Power mode. This 7-bit configuration is a linear transfer function that starts at 0.26V, ends at 1.52V, with 10mV increments. NOTE: The 0x00 setting is reserved.	O	R/W
5	1			O	R/W
4	1			O	R/W
3	0			O	R/W
2	1			O	R/W
1	1			O	R/W
0	1			O	R/W

Load Switch Drivers

LSW_INT

Register Name	LSW_INT
I²C Slave Address	0x60
Register Address	0x03
Reset Value (HEX)	0x00
Reset Value (BIN)	0b00000000
Reset Type	S
Access Type	RC
Register Type	INT

Bit	Default	Bit Name	Description	Reset	Access Type
7	0	BLANK	Blank. There is no bit at this location. Write to 0. Reads are don't care.	S	RC
6	0	BLANK	Blank. There is no bit at this location. Write to 0. Reads are don't care.	S	RC
5	0	BLANK	Blank. There is no bit at this location. Write to 0. Reads are don't care.	S	RC
4	0	BLANK	Blank. There is no bit at this location. Write to 0. Reads are don't care.	S	RC
3	0	RSVD	Reserved. Unutilized bit. Write to 0. Reads are don't care.	S	RC
2	0	UV_LSW3_I	Output Undervoltage Interrupt. 0 = Load Switch was enabled and LSW3 output HAS NOT fallen below the falling UV threshold since the last time this bit was read, OR, LSW3 was disabled. 1 = LSW3 was enabled and LSW3 output HAS fallen below the falling UV threshold since the last time this bit was read.	S	RC
1	0	UV_LSW2_I	Output Undervoltage Interrupt. 0 = Load Switch was enabled and LSW2 output HAS NOT fallen below the falling UV threshold since the last time this bit was read, OR, LSW2 was disabled. 1 = LSW2 was enabled and LSW2 output HAS fallen below the falling UV threshold since the last time this bit was read.	S	RC
0	0	UV_LSW1_I	Output Undervoltage Interrupt. 0 = Load Switch was enabled and LSW1 output HAS NOT fallen below the falling UV threshold since the last time this bit was read, OR, LSW1 was disabled. 1 = LSW1 was enabled and LSW1 output HAS fallen below the falling UV threshold since the last time this bit was read.	S	RC

CNFG_LSWx [x=1,2]

Register Name	CNFG_LSWx	
I²C Slave Address	0x60	
Register Address	0x69 – 0x6A	
Reset Value (HEX)	0x0D	0x25
Reset Value (BIN)	0b00001101 (CID4=0x7)	0b00100101 (CID4=0x7)
Reset Type	O	
Access Type	R/W	
Register Type	CNFG	

7	0	RSVD	Reserved. Unutilized bit. Write to 0. Reads are don't care.	O	R/W
6	0	RSVD	Reserved. Unutilized bit. Write to 0. Reads are don't care.	O	R/W
5	x	LSWx_INP_EXT	Load Switch External Input Select. 0 = Input to Load Switch is one of the internal bucks selected by LSWx_INP_SEL[1:0] 1 = Input to Load Switch is VSYS	O	R/W
4	x	LSWx_INP_SEL[1:0]	Load Switch Input Selection (From within internal Bucks) 2'b00 = BUCK1 2'b01 = BUCK2 2'b1x = BUCK3	O	R/W
3	x			O	R/W
2	x	LSWx_DRV_FREQ[2:0]	Load Switch Gate Drive Strength. Expressed as a charge pump oscillator frequency. 3'b000 = 12.5kHz 3'b001 = 25kHz 3'b010 = 50kHz 3'b011 = 100kHz 3'b100 = 200kHz 3'b101 = 400kHz 3'b110 = 800kHz 3'b111 = 1600kHz	O	R/W
1	x			O	R/W
0	x			O	R/W

CNFG_LSW3

Register Name	CNFG_LSW3
I²C Slave Address	0x60
Register Address	0x6B
Reset Value (HEX)	0x20
Reset Value (BIN)	0b00100000 (CID4=0x7)
Reset Type	O
Access Type	R/W
Register Type	CNFG

Bit	Default	Bit Name	Description	Reset	Access Type
7	0	RSVD	Reserved. Unutilized bit. Write to 0. Reads are don't care.	O	R/W
6	0	RSVD	Reserved. Unutilized bit. Write to 0. Reads are don't care.	O	R/W
5	x	LSW3_INP_EXT	Load Switch External Input Select. 0 = Input to Load Switch is one of the internal bucks selected by LSW3_INP_SEL[1:0] 1 = Input to Load Switch is VSYS	O	R/W
4	x	LSW3_INP_SEL[1:0]	Load Switch Input Selection (From within internal Bucks). 2'b00 = BUCK1 2'b01 = BUCK2 2'b1x = BUCK3	O	R/W
3	x			O	R/W
2	0	RSVD	Reserved. Unutilized bit. Write to 0. Reads are don't care.	O	R/W
1	0	RSVD	Reserved. Unutilized bit. Write to 0. Reads are don't care.	O	R/W
0	0	RSVD	Reserved. Unutilized bit. Write to 0. Reads are don't care.	O	R/W

Linear Regulator

LDO_CNFG1

Register Name	LDO_CNFG1
I²C Slave Address	0x60
Register Address	0x36
Reset Value (HEX)	0xA8
Reset Value (BIN)	0b10101000 (CID4=0x7)
Reset Type	O
Access Type	R/W
Register Type	CNFG

Bit	Default	Bit Name	Description	Reset	Access Type
7	x	ADE_LDO	Active Discharge Enable. 0 = Disable Active Discharge Resistor. When the LDO output is disabled, the output voltage decays as a function of the output load and capacitance. 1 = Enable Active Discharge Resistor. When the LDO output is disabled, a discharge resistor is placed between the output and ground and the output voltage is discharged through the resistor. When the LDO output is enabled, the resistor is removed from the path.	O	R/W
6	x	VOUT_LDO[6:0]	LDO Target Output Voltage (V_{LDO}). This 7-bit configuration is a linear transfer function that starts at 0.8V and ends at 3.95V, with 25mV increments. V_{LDO}=0.8V+(VOUT_LDO[6:0]*25mV).	O	R/W
5	x			O	R/W
4	x			O	R/W
3	x			O	R/W
2	x			O	R/W
1	x			O	R/W
0	x			O	R/W

I2C_CTRL1

Register Name	I2C_CTRL1
I²C Slave Address	0x60
Register Address	0x13
Reset Value (HEX)	0x00
Reset Value (BIN)	0b00000000
Reset Type	O
Access Type	R/W
Register Type	CNFG

Bit	Default	Bit Name	Description	Reset	Access Type
7	0	RSVD	Reserved for future use.	O	R/W
6	0	RSVD	Reserved for future use.	O	R/W
5	0	RSVD	Reserved for future use.	O	R/W
4	0	PAIR	Pair address mode option at burst write operation on customer registers. 0 = Pair address mode is disabled, and sequential mode is used for multiple register write protocol. 1 = Pair address mode is enabled for multiple register write protocol.	O	R/W
3	0	RSVD	Reserved for future use.	O	R/W
2	0	RSVD	Reserved for future use.	O	R/W
1	0	WD_EN	I²C Watchdog Timer Control. 0 = Watchdog function is disabled (I²C Rev 4.0 compliant). 1 = Watchdog function is enabled (SMBus compatible).	O	R/W
0	0	HS_EXT	High-Speed Mode Extension Control. 0 = High-Speed Mode Extension is disabled (I²C Rev 4.0 compliant) 1 = High-Speed Mode Extension is enabled. HS mode is enabled without HS mode entrance code and keeps HS mode during and after STOP condition	O	R/W

I2C_CTRL2

Register Name	I2C_CTRL2
I^2C Slave Address	0x60
Register Address	0x14
Reset Value (HEX)	0x01
Reset Value (BIN)	0b00000001
Reset Type	O
Access Type	R/W
Register Type	CNFG

Bit	Default	Bit Name	Description	Reset	Access Type
7	0	BLANK	There is no physical bit at this location. Write to 0. Reads are don't care.	O	R/W
6	0	BLANK	There is no physical bit at this location. Write to 0. Reads are don't care.	O	R/W
5	0	BLANK	There is no physical bit at this location. Write to 0. Reads are don't care.	O	R/W
4	0	BLANK	There is no physical bit at this location. Write to 0. Reads are don't care.	O	R/W
3	0	RSVD	Reserved for Future Use.	O	R/W
2	0	RSVD	Reserved for Future Use.	O	R/W
1	0	RSVD	Reserved for Future Use.	O	R/W
0	1	I2CWP	Write Protect Enable. 0 = Disable Write Protect for all registers in the PMIC. Writes to any register through the I^2C write protocol result in the data value being written to the register. 1 = Enable Write Protect for all registers in the PMIC. Writes to any register through the I^2C write protocol do NOT result in the data value being written to the register. The STOP condition at the end of an I^2C transaction will reset this bit back to its default value.	O	R/W

OTP Options

There is a set of one-time programmable registers that define reset values for different features. These OTP registers are programmable in the factory only and cannot be changed afterward with I^2C commands. The OTP version can be checked by looking at the part number (MAX77752x) or the CID4 register. Reference the Reset Quick Reference Table below for a list of register reset values based on OTP setting.

Table 7: Reset Value Reference Table

Register	Bit Field Name	MAX77752A		MAX77752B	
CID4	DRV[7:0]	0x07		0x0D	
GLBL_CNFG0	ALT_LP_REQ_EN	LP_REQ is controlled by CLOGIC.	0x18	LP_REQ is controlled by CLOGIC.	0x00
	ALT_LP_REQ	Programmed logic low		Programmed logic low	
GLBL_CNFG1	SYSRSTTH[3:0]	Reset threshold = 2.65V	0x00	Reset threshold = 2.85V	0x48
	SYSRSTHYS[1:0]	Hysteresis = 150mV		Hysteresis = 150mV	
GLBL_CNFG2	SYSBOTH[3:0]	Brownout Threshold = 2.8V	0xC0	Brownout Threshold = 2.9V	0xC5
	SYSBOHYS[1:0]	Hysteresis = 150mV		Hysteresis = 200mV	
GLBL_CNFG3	PG_DLY[1:0]	Power Good De-Assert Delay = 31µs	0x80	Power Good De-Assert Delay = 1016µs	0x83
	WP_L_DLY	Write Protect De-Assert Delay Time = 0µs		Write Protect De-Assert Delay Time = 0µs	
GLBL_INTM	SYSRST_F_M	SYSRST_I_F is unmasked for PGOOD_INT.	0x02	SYSRST_I_F is unmasked for PGOOD_INT.	0x00
	EREG_M	EREG_POK signal can cause device to power down.		EREG_POK signal can cause device to power down.	
	IN_OC_M	IN_OC_I (overcurrent) will cause a power down event.		IN_OC_I (overcurrent) will NOT cause a power down event.	
HICCUP_CNFG	HICCUP_CNT_LIM[5:0]	7	0x1C	7	0x1C
OTP_PHUP_1	OTP_SLP_MSTRSLV	Master mode	0x17	Slave mode	0x1B
	OTP_INT_PU	Enable Pull-up Resistors to all logic pins.		Enable Pull-up Resistors to all logic pins.	
SPARE_OTP	OTP_LPACK_POL	LP_ACK is active high.	0x40	LP_ACK is active low.	0x60
	OTP_CSA_DBNC	CSA debounce time = 100 µs		CSA debounce time = 100 µs	

OTP_2B_INRUSH	OTP_INRUSH_DISABLE	Inrush & LSW3 block disabled	0x08	Inrush and LSW3 block enabled.	0x16
	OTP_INR_FREQ[2:0]	Inrush drive frequency = 6.25kHz		Inrush drive frequency = 400kHz	
INRUSH_OPTION	LSW_OTP_SEL	INRush function selected	0x00	INRush function selected	0x02
MSTR0_3FPS	MSTR0_3UPF	Power Up slot duration = 127µs	0x52	Power Up slot duration = 253µs	0x53
	MSTR0_3DNF	Power Down slot duration = 984µs		Power Down slot duration = 984µs	
MSTR1_4FPS	MSTR1_4UPF	Power Up slot duration = 253µs	0x03	Power Up slot duration = 127µs	0x02
	MSTR1_4DNF	Power Down slot duration = 31µs		Power Down slot duration = 31µs	
MSTR2_5FPS	MSTR2_5UPF	Power Up slot duration = 31µs	0x00	Power Up slot duration = 984µs	0x05
	MSTR2_5DNF	Power Down slot duration = 31µs		Power Down slot duration = 31µs	
EREG1FPS	EREG1MSTRASGN	Assigned to FPS master	0x85	Assigned to FPS master	0x89
	EREG1MSTR[2:0]	FPS Master 0		FPS Master 0	
	EREG1UPSLT[1:0]	Slot 1		Slot 2	
	EREG1DNSLT[1:0]	Slot 1		Slot 1	
EREG2FPS	EREG2MSTRASGN	Assigned to FPS master	0x97	Assigned to FPS master	0x83
	EREG2MSTR[2:0]	FPS Master 1		FPS Master 0	
	EREG2UPSLT[1:0]	Slot 1		Slot 0	
	EREG2DNSLT[1:0]	Slot 3		Slot 3	
BUCK1FPS	BUCK1MSTRASGN	Assigned to FPS master	0x97	Assigned to FPS master	0xBF
	BUCK1MSTR[2:0]	FPS Master 1		FPS Master 3	
	BUCK1UPSLT[1:0]	Slot 1		Slot 3	
	BUCK1DNSLT[1:0]	Slot 3		Slot 3	
BUCK2FPS	BUCK2MSTRASGN	Assigned to FPS master	0xC3	Assigned to FPS master	0x9E
	BUCK2MSTR[2:0]	FPS Master 4		FPS Master 1	
	BUCK2UPSLT[1:0]	Slot 0		Slot 3	
	BUCK2DNSLT[1:0]	Slot 3		Slot 2	
BUCK3FPS	BUCK3MSTRASGN	Assigned to FPS master	0x83	Assigned to FPS master	0xB0

	BUCK3MSTR[2:0]	FPS Master 0		FPS Master 3	
	BUCK3UPSLT[1:0]	Slot 0		Slot 0	
	BUCK3DNSLT[1:0]	Slot 3		Slot 0	
LDOFPS	LDOMSTRASGN	Assigned to FPS master	0x97	Assigned to FPS master	0x80
	LDOMSTR[2:0]	FPS Master 1		FPS Master 0	
	LDOUPSLT[1:0]	Slot 1		Slot 0	
	LDODNSLT[1:0]	Slot 3		Slot 0	
LSW1FPS	LSW1MSTRASGN	Assigned to FPS master	0x97	Assigned to FPS master	0x84
	LSW1MSTR[2:0]	FPS Master 1		FPS Master 0	
	LSW1UPSLT[1:0]	Slot 1		Slot 1	
	LSW1DNSLT[1:0]	Slot 3		Slot 0	
LSW2FPS	LSW2MSTRASGN	Not assigned to FPS master	0x00	Assigned to FPS master	0x8F
	LSW2MSTR[2:0]			FPS Master 0	
	LSW2UPSLT[1:0]			Slot 3	
	LSW2DNSLT[1:0]			Slot 3	
LSW3FPS	LSW3MSTRASGN	Not assigned to FPS master	0x00	Not assigned to FPS master	0x00
OPMD1	BUCK1OPMD[1:0]	Enabled	0x55	Enabled	0x55
	BUCK2OPMD[1:0]	Enabled		Enabled	
	BUCK3OPMD[1:0]	Enabled		Enabled	
OPMD2	EREG1OPMD	Disabled	0x01	Disabled	0x00
	EREG2OPMD	Disabled		Disabled	
	LSW1OPMD	Controlled by FPS		Controlled by FPS	
	LSW2OPMD	OFF		OFF	
	LSW3OPMD	OFF		OFF	
	LDOOPMD[1:0]	Enabled		OFF	
CNFG_CSA	CSTH_OTP	2.25A	0x03	2.25A	0x03
BUCK1CNFG1	BUCK1VOUT[7:0]	Buck 1 Out = 1.8V	0xC0	Buck 1 Out = 1.8V	0xC0
BUCK2CNFG1	BUCK2VOUT[7:0]	Buck 2 Out = 1.350V	0x78	Buck 2 Out = 1.200V	0x60
BUCK3CNFG1	BUCK3VOUT[7:0]	Buck 3 Out = 1.05V	0x50	Buck 3 Out = 0.9V	0x41
BUCK1CNFG2	BUCK1ADDIS	Active Discharge Resistor enabled	0x40	Active Discharge Resistor enabled	0x40
BUCK2CNFG2	BUCK2ADDIS	Active Discharge Resistor enabled	0x40	Active Discharge Resistor enabled	0x40
BUCK3CNFG2	BUCK3ADDIS	Active Discharge Resistor enabled	0x24	Active Discharge Resistor enabled	0x04
BUCK1CNFG3	BUCK1_OV_THR	Buck 1 OV Threshold = 108.3%	0x46	Buck 1 OV Threshold = 108.3%	0x46

BUCK2CNFG3	BUCK2_OV_THR	Buck 2 OV Threshold = 108.3%	0x46	Buck 2 OV Threshold = 108.3%	0x46
BUCK3CNFG3	BUCK3_OV_THR	Buck 3 OV Threshold = 108.3%	0x06	Buck 3 OV Threshold = 108.3%	0x06
BUCK1CNFG4	BUCK1_BO_THR[1:0]	Buck 1 Brownout Threshold = 86%	0x49	Buck 1 Brownout Threshold = 86%	0x49
	BUCK1_BO_HYS[1:0]	Buck 1 BO Hysteresis = 10%		Buck 1 BO Hysteresis = 10%	
BUCK2CNFG4	BUCK2_BO_THR[1:0]	Buck 2 Brownout Threshold = 86%	0x49	Buck 2 Brownout Threshold = 86%	0x49
	BUCK2_BO_HYS[1:0]	Buck 2 BO Hysteresis = 10%		Buck 2 BO Hysteresis = 10%	
BUCK3CNFG4	BUCK3_BO_THR[1:0]	Buck 3 Brownout Threshold = 85%	0x59	Buck 3 Brownout Threshold = 85%	0x59
	BUCK3_BO_HYS[1:0]	Buck 3 BO Hysteresis = 10%		Buck 3 BO Hysteresis = 10%	
BUCK3CNFG5	BUCK3VDVS[6:0]	Buck 3 DVS = 0.81V	0x37	Buck 3 DVS = 0.81V	0x37
BUCK_INTM	BUCK1UV_M	An undervoltage event initiates a power down event.	0x00	An undervoltage event initiates a power down event.	0x00
	BUCK1OV_M	An overvoltage event initiates a power down event.		An overvoltage event initiates a power down event.	
	BUCK2UV_M	An undervoltage event initiates a power down event.		An undervoltage event initiates a power down event.	
	BUCK2OV_M	An overvoltage event initiates a power down event.		An overvoltage event initiates a power down event.	
	BUCK3UV_M	An undervoltage event initiates a power down event.		An undervoltage event initiates a power down event.	
	BUCK3OV_M	An overvoltage event initiates a power down event.		An overvoltage event initiates a power down event.	
CNFG_LSW1	LSW1_INP_EXT	Input to load switch is an internal buck	0x0D	Input to load switch is an internal buck	0x15
	LSW1_INP_SEL[1:0]	Input is from Buck 2		Input is from Buck 3	
	LSW1_DRV_FREQ[2:0]	$f_{LSW1\_DRV\_FREQ}$ = 400kHz		$f_{LSW1\_DRV\_FREQ}$ = 400kHz	
CNFG_LSW2	LSW2_INP_EXT	Input to load switch is V_{SYS}	0x25	Input to load switch is an internal buck	0x05
	LSW2_INP_SEL[1:0]			Input is from Buck 1	
	LSW2_DRV_FREQ[2:0]	$f_{LSW1\_DRV\_FREQ}$ = 400kHz		$f_{LSW1\_DRV\_FREQ}$ = 400kHz	

CNFG_LSW3	LSW3_INP_EXT	Input to load switch is V_{SYS}	0x20	Input to load switch is V_{SYS}	0x20
LDOCNFG1	VOUT_LDO[6:0]	LDO Out = 1.800V	0xA8	LDO Out = 1.875V	0xAB
	ADE_LDO	Active Discharge Resistor is enabled		Active Discharge Resistor is enabled	
I2C_CTRL1	PAIR	Pair address mode is disabled.	0x00	Pair address mode is disabled.	0x00
	HS_EXT	High speed extension is disabled.		High speed extension is disabled.	
I2C_CTRL2	I2CWP	Write protect is enabled for all registers.	0x01	Write protect is enabled for all registers.	0x01