CS42L42

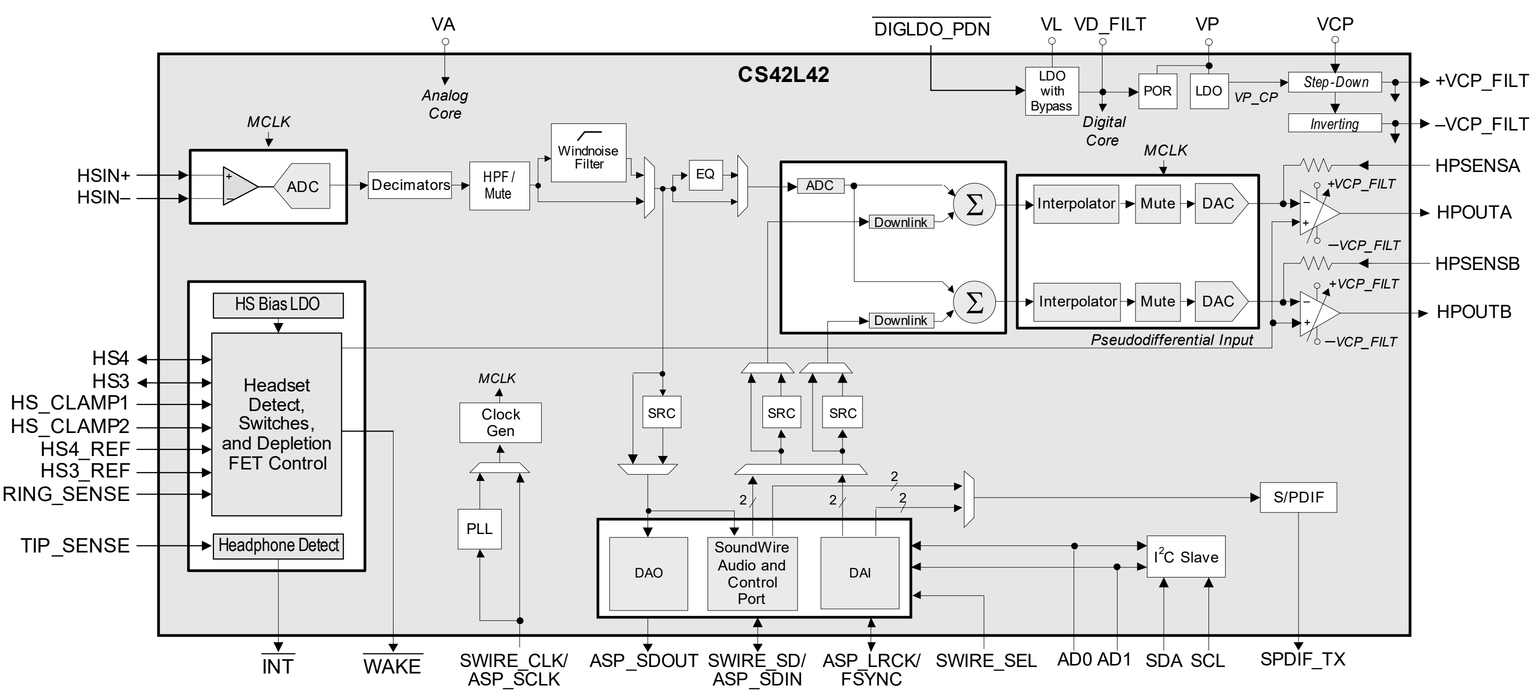
Low-Power Audio Codec with SoundWire®–I2S/TDM and Audio Processing

System Features

- Stereo headphone (HP) output with 114-dB dynamic range
  - Class H HP amplifier with four-level automatic or manual supply adjust
  - Power output 2 x 35 mW into 30 Ω
- Mono mic input with 114-dB dynamic range
  - Low-noise headset bias with integrated bias resistor
  - 1-V_{RMS} input voltage
  - Integrated AC-coupling capacitors
- Integrated detect features
  - OMTP (Open Mobile Terminal Platform) and AHJ (American headset jack) headset-type detection and configuration with low-impedance internal switches
  - Mic short (S0 Button) detect with ADC automute
  - Automatic Hi-Z of headset bias output to ground on headset bias current rise or HP/headset unplug
- System wake from headset/headphone plug/unplug or S0 button press
- Interrupt output
- Mono equalizer for side-tone mix
- MIPI® SoundWire® or I2C/I2S/TDM control and audio interface
- S/PDIF transmit (Sony/Philips digital interface format)
- Integrated fractional-N PLL
  - Increases system-clock flexibility for audio processing
  - Reference clock sourced from either I2S/TDM bit clock or MIPI SoundWire clock
- Audio serial port (ASP)
  - I2S (two channels) or TDM (up to four channels)
  - Slave or Hybrid-Master Mode (bit-clock slave and LRCK/FSYNC derived from bit clock)
  - Sample-rate converter (SRC) for two input channels, with bypass
  - SRC for one output channel, with bypass
  - User isochronous audio transport support
  - Supports up to 192-kHz sample rate to S/PDIF output
  - Sample rate support for 8 to 192 kHz
- Integrated power management
  - Digital core operates from either an external 1.2-V supply or LDO from a 1.8-V supply.
  - Step-down charge pump improves HP efficiency
  - Independent peripheral power-down controls
  - Standby operation from VP with all other supplies powered off
  - VP monitor to detect and report brownout conditions
  - Low-impedance switching suppresses ground-noise

Applications

- Ultrabooks, tablets, and smartphones
- Digital headsets



General Description

The CS42L42 is a low-power audio codec with integrated MIPI SoundWire interface or I^2C/I^2S/TDM interfaces designed for portable applications. It provides a high-dynamic range, stereo DAC for audio playback and a mono high-dynamic-range ADC for audio capture.

The CS42L42 provides high performance (up to 24-bit) audio for ADC and DAC audio playback and capture functions as well as for the S/PDIF transmitter. The CS42L42 architecture includes bypassable SRCs and a bypassable, three-band, 32-bit parametric equalizer that allows processing of digital audio data.

A digital mixer is used to mix the ADC or serial ports to the DACs. There is independent attenuation on each mixer input.

The processing along the output paths from the ADC or serial port to the two stereo DACs includes volume adjustment and mute control.

The CS42L42 is available in a 49-ball WLCSP package and a 48-pin QFN package for extended temperature range grade of –40°C to +85°C.

Table of Contents

1 Pin Assignments and Descriptions

This section shows pin assignments and describes pin functions.

1.1 WLCSP Pin Out (Through-Package View)

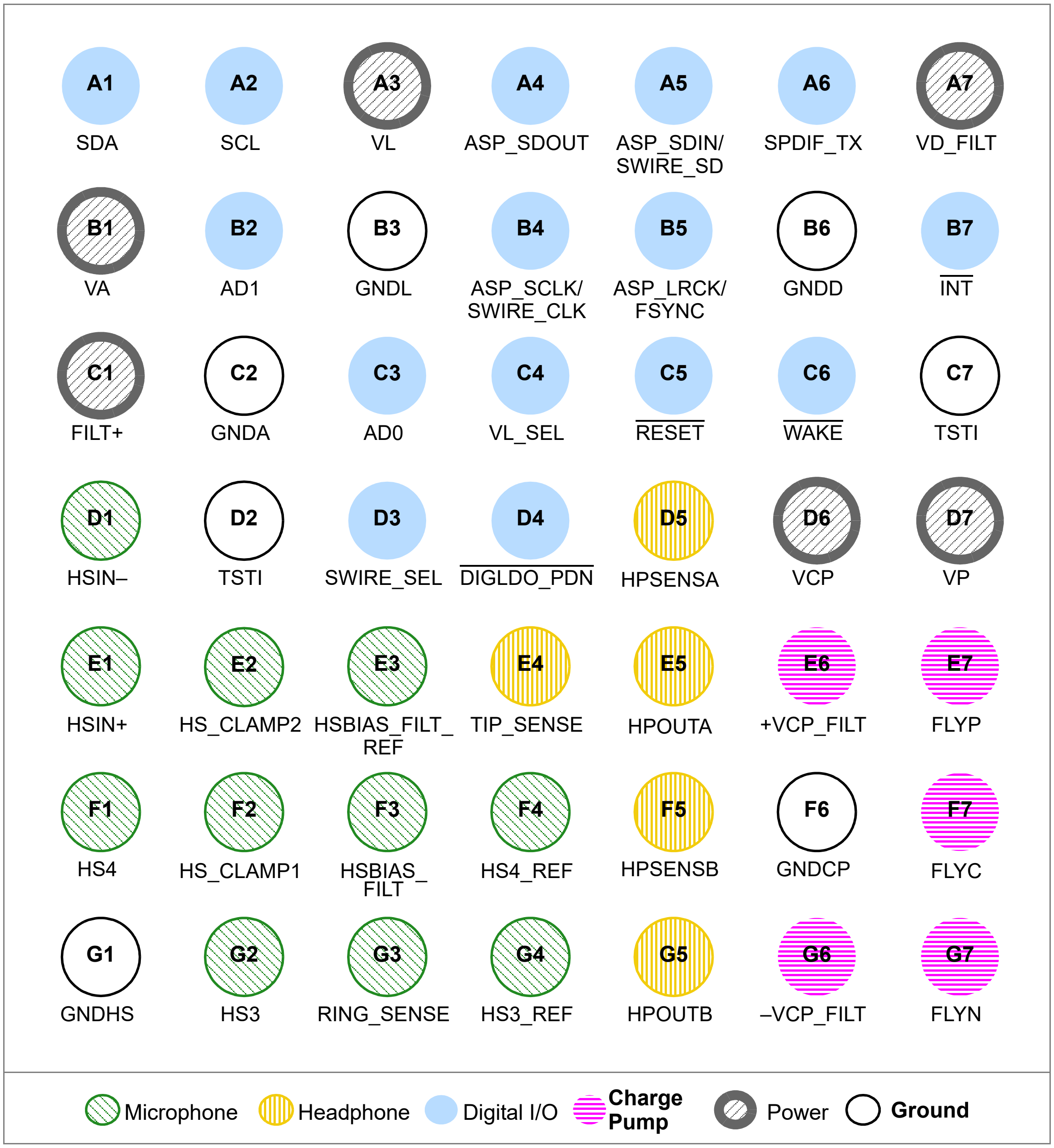


Figure 1-1. WLCSP Pin Diagram (Through-Package View)

1.2 QFN Pin Out (Through-Package View)

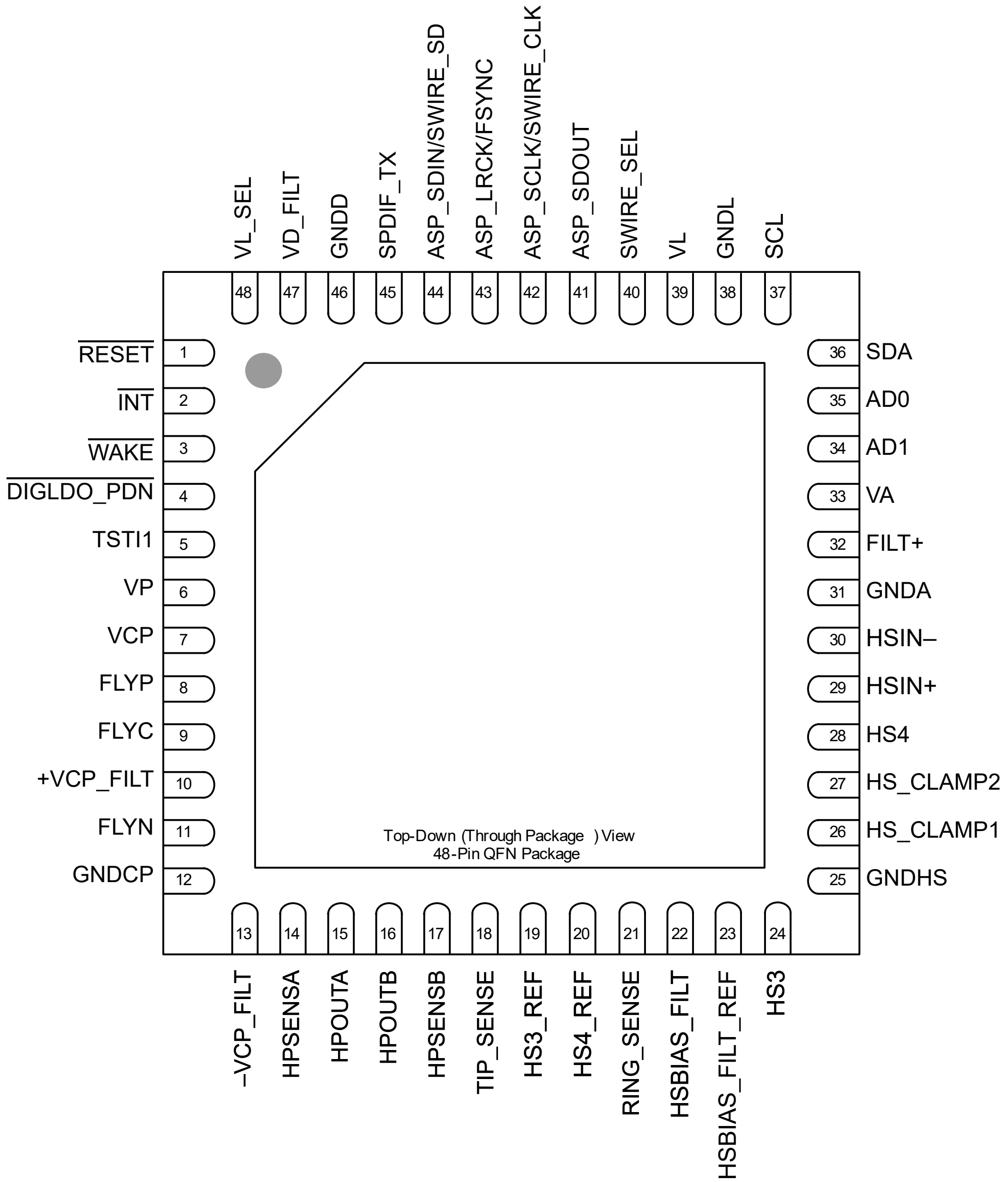


Figure 1-2. QFN Pin Diagram

1.3 Pin Descriptions

Table 1-1. Pin Descriptions

Pin Name	CSP Pin #	QFN Pin #	Power Supply	I/O	Pin Description	Internal Connection	Driver	Receiver	State at Reset
Microphone									
HS_CLAMP1 HS_CLAMP2	F2 E2	26 27	VP	I	**Headset Depletion FET Connections.** Input to drain of integrated depletion FET for ground-noise rejection.	—	—	—	Input
HS3_REF HS4_REF	G4 F4	19 20	VP	I	**Headset Connection Reference**. Input to pseudodifferential HP output reference	—	—	—	Input
HS3 HS4	G2 F1	24 28	VP	I	**Headset Connections**. Input to headset and mic-button detection functions	—	—	—	Input
HSBIAS_FILT	F3	22	VP	I	**Headset Bias Source Voltage Filter.** Filter connection for the internal quiescent voltage used for headset bias generation.	—	—	—	Input
HSBIAS_FILT_REF	E3	23	VP	I	**Headset Bias Source Voltage Filter Reference.** Input of filter connection for the internal quiescent voltage used for headset-bias generation.	—	—	—	Input
HSIN–	D1	30	VP	I	**Inverting Mic Inputs.** Inverting analog input for the ADC.	—	—	—	Input
HSIN+	E1	29	VP	I	**Noninverting Mic Inputs.** Noninverting analog input for the ADC.	—	—	—	Input
RING_SENSE	G3	21	VP	I	**Ring Sense Input.** Sense pin to detect S/PDIF or headphone plug. Can be configured to be debounced on plug and unplug events independently.	—	—	—	Input
Headphone									
HPOUTA HPOUTB	E5 G5	15 16	±VCP_FILT	O	**Headphone Audio Output.** Ground-centered audio output.	—	—	—	—
HPSENSA HPSENSB	D5 F5	14 17	±VCP_FILT	I	**Headphone Audio Sense Input.** Audio sense input.	—	—	—	Input
TIP_SENSE	E4	18	VP	I	**Tip Sense.** Output can be set to wake the system. Independently configurable to be debounced on plug and unplug events.	—	Hi-Z	—	—
Digital I/O									
AD0 AD1	C3 B2	35 34	VL	I	**I^{2}C Address Input/SoundWire Instance ID Input.** Address pins for I^{2}C or SoundWire Instance ID [1:0] input.	—	—	Hysteresis on CMOS input	Input
ASP_LRCK/FSYNC	B5	43	VL	I/O	**ASP Left/Right Clock or Frame Sync.** Left or right word select, or frame start sync for the ASP interface.	—	CMOS output	Hysteresis on CMOS input	Input
ASP_SCLK/SWIRE_CLK	B4	42	VL	I	**ASP/SoundWire Serial Data Clock.** SoundWire data-shift clock in SoundWire Mode or serial data-shift clock for the ASP interface in I^{2}S/TDM Mode. Source clock used for internal master clock generation.	—	—	Hysteresis on CMOS input	Input
ASP_SDIN/SWIRE_SD	A5	44	VL	I/O	**ASP Serial Data Input/SoundWire Serial Data Input and Output.** Serial data input and output in SoundWire mode or serial data input for the ASP interface in I^{2}S/TDM mode.	—	CMOS output	Hysteresis on CMOS input	Input
ASP_SDOUT	A4	41	VL	O	**ASP Serial Data Output.** Serial data output for the ASP interface.	Weak pull-down	CMOS output	—	Output
$\overline{\text{DIGLDO\_PDN}}$	D4	4	VP	I	**Digital LDO Power Down.** Digital core logic LDO power down.	—	—	Hysteresis on CMOS input	Input
$\overline{\text{INT}}$	B7	2	VP	O	**Interrupt output.** Programmable, open-drain, active-low programmable interrupt output.	—	CMOS open-drain output	—	Output
$\overline{\text{RESET}}$	C5	1	VP	I	**Reset.** Hardware reset.	—	—	Hysteresis on CMOS input	Input
SCL	A2	37	VL	I	**I^{2}C Clock.** Clock input for the I^{2}C interface.	—	—	Hysteresis on CMOS input	Input

Table 1-1. Pin Descriptions *(Cont.)*

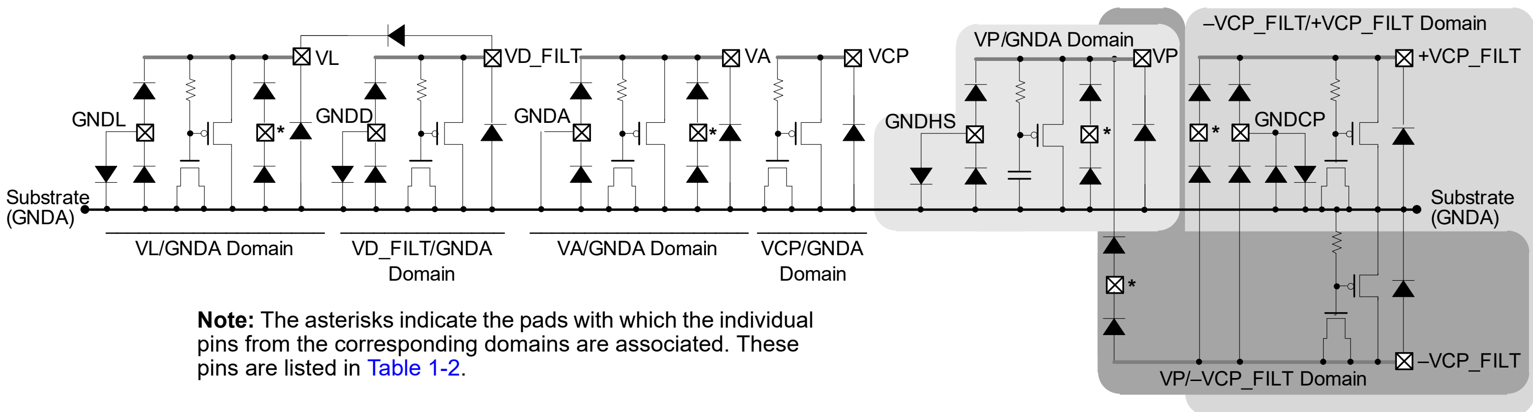
Pin Name	CSP Pin #	QFN Pin #	Power Supply	I/O	Pin Description	Internal Connection	Driver	Receiver	State at Reset
SDA	A1	36	VL	I/O	**I^2C Input/Output.** I^2C input and output.	—	CMOS open-drain output	Hysteresis on CMOS input	Input
SPDIF_TX	A6	45	VL	O	**S/PDIF Audio Serial Data Output.** Serial data output for S/PDIF interface.	—	CMOS output	—	Output
SWIRE_SEL	D3	40	VL	I	**SoundWire Select.** SoundWire interface selection input. Defines the serial and audio interface type. If asserted, SoundWire is the control and audio interface, otherwise I^2C is control and TDM/I^2S is used for audio data.	—	—	Hysteresis on CMOS input	Input
VL_SEL	C4	48	VP	I	**VL Supply Voltage Select.** Select for VL power supply voltage level. Connect to VP for 1.8-V VL supply, connect to GNDD for 1.2-V VL supply	—	—	Hysteresis on CMOS input	Input
$\overline{\text{WAKE}}$	C6	3	VP	O	**Wake up.** Programmable, open-drain, active-low output. This outputs the state of the Mic S0 or HP wake detect.	—	Hi-Z, CMOS open-drain output	—	Output
					Charge Pump				
–VCP_FILT	G6	13	VCP/ VP[1]	O	**Inverting Charge Pump Filter Connection.** Power supply for the inverting charge pump that provides the negative rail for the HP amplifier.	—	—	—	—
+VCP_FILT	E6	10	VCP/ VP[1]	O	**Step Down Charge Pump Filter Connection.** Power supply for the step down charge pump that provides the positive rail for the HP amplifier.	—	—	—	—
FLYC	F7	9	VCP/ VP[1]	O	**Charge Pump Cap Common Node.** Common positive node for the HP amplifiers' step-down and inverting charge pumps' flying capacitors.	—	—	—	—
FLYN	G7	11	VCP/ VP[1]	O	**Charge Pump Cap Negative Node.** Negative node for the inverting charge pump's flying capacitor.	—	—	—	—
FLYP	E7	8	VCP/ VP[1]	O	**Charge Pump Cap Positive Node.** Positive node for HP amps' step-down charge pump's flying capacitor.	—	—	—	—
					Power				
FILT+	C1	32	VA	I	**Positive Voltage Reference.** Positive reference voltage for internal sampling circuits.	—	—	—	—
VA	B1	33	N/A	I	**Analog Power Supply.** Power supply for the internal analog section.	—	—	—	—
VCP	D6	7	N/A	I	**Charge Pump Power.** Power supply for the internal HP amplifiers charge pump.	—	—	—	—
VD_FILT	A7	47	N/A	I	**1.2-V Digital Core Power Supply.** Power supply for internal digital logic.	—	—	—	—
VL	A3	39	N/A	I	**I/O Power Supply.** Power supply for external interface and internal digital logic.	—	—	—	—
VP	D7	6	N/A	I	**High Voltage Interface Supply.** Power supply for high voltage interface.	—	—	—	—
					Ground				
GNDA	C2	31	N/A	I	**Analog Ground.** Ground reference for the internal analog section.	—	—	—	—
GNDL	B3	38	N/A	I	**Digital Ground.** Ground reference for interface section.	—	—	—	—
GNDHS	G1	25	N/A	I	**Headset Ground.** Ground reference for the internal analog section.	—	—	—	—
GNDCP	F6	12	N/A	I	**Charge Pump Ground.** Ground reference for the internal HP amplifiers charge pump.	—	—	—	—
GNDD	B6	46	N/A	I	**Digital Ground.** Ground reference for the internal digital circuits.	—	—	—	—
					Test				
TSTI	D2, C7	—	N/A	I	**Test input.** Connect to GNDA.	—	—	—	—

1. The power supply is determined by ADPTPWR setting (see Section 7.14.1). VP is used if ADPTPWR = 001 (VP_CP Mode) or when necessary for ADPTPWR = 111 (Adapt-to-Signal Mode).

1.4 Electrostatic Discharge (ESD) Protection Circuitry

ESD-sensitive device. The CS42L42 is manufactured on a CMOS process. Therefore, it is generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken while handling and storing this device. This device is qualified to current JEDEC ESD standards.

Fig. 1-3 provides a composite view of the ESD domains showing the ESD protection paths between each pad and the substrate (GNDA) and the interrelations between some domains. Note that this figure represents the structure for the internal protection devices and that additional protections can be implemented as part of the integration into the board.



Note: The asterisks indicate the pads with which the individual pins from the corresponding domains are associated. These pins are listed in Table 1-2.

Figure 1-3. Composite ESD Topology

Table 1-2 shows the individual ESD domains and lists the pins associated with each domain.

Table 1-2. ESD Domains

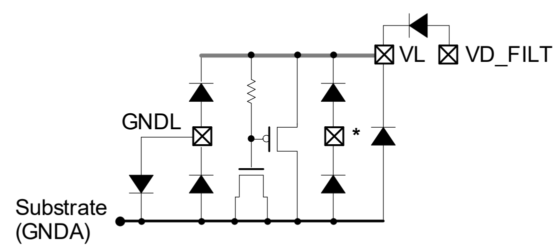
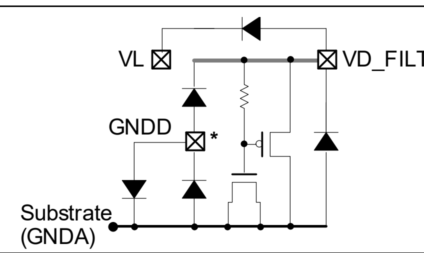
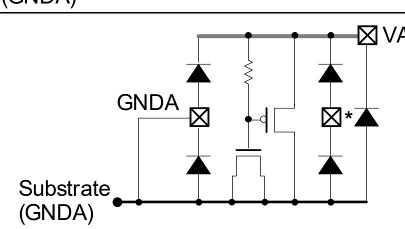
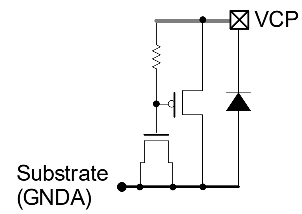
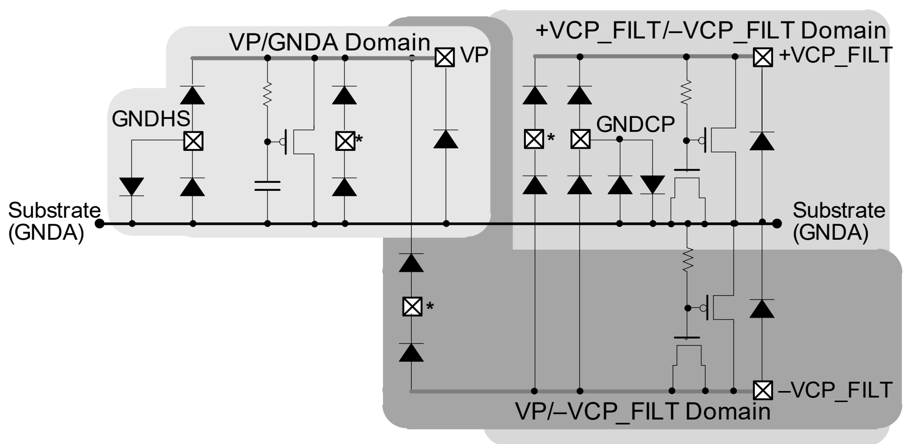
ESD Domain	Signal Name (CSP/QFN) (See * in Topology Figures for Pad)	Topology
VL/ GNDA [1]	AD0 AD1 ASP_LRCK/FSYNC GNDL SCL SDA ASP_SDOUT SPDIF_TX SWIRE_SEL ASP_SCLK/SWIRE_CLK SWIRE_SD/ASP_SDIN VD_FILT VL	
VD_FILT/ GNDA	VD_FILT GNDD TSTI	
VA/ GNDA	FILT+ GNDA VA	

Table 1-2. ESD Domains *(Cont.)*

ESD Domain	Signal Name (CSP/QFN) (See * in Topology Figures for Pad)	Topology
VCP/ GNDA	VCP	
VP/ GNDA	GNDHS HS3 HS4 HS_CLAMP1 HS_CLAMP2 HSBIAS_FILT HSBIAS_FILT_REF HSIN+ HSIN– VP VL_SEL INT WAKE RESET DIGLDO_PDN	
+VCP_ FILT/ –VCP_ FILT	+VCP_FILT –VCP_FILT FLYN HPSENSA HPSENSB HPOUTA HPOUTB GNDCP	
VP/ –VCP_ FILT	FLYC FLYP HS3_REF HS4_REF RING_SENSE TIP_SENSE	

1.See Section 5.8 for additional information regarding VD_FILT andVL.

2 Typical Connections

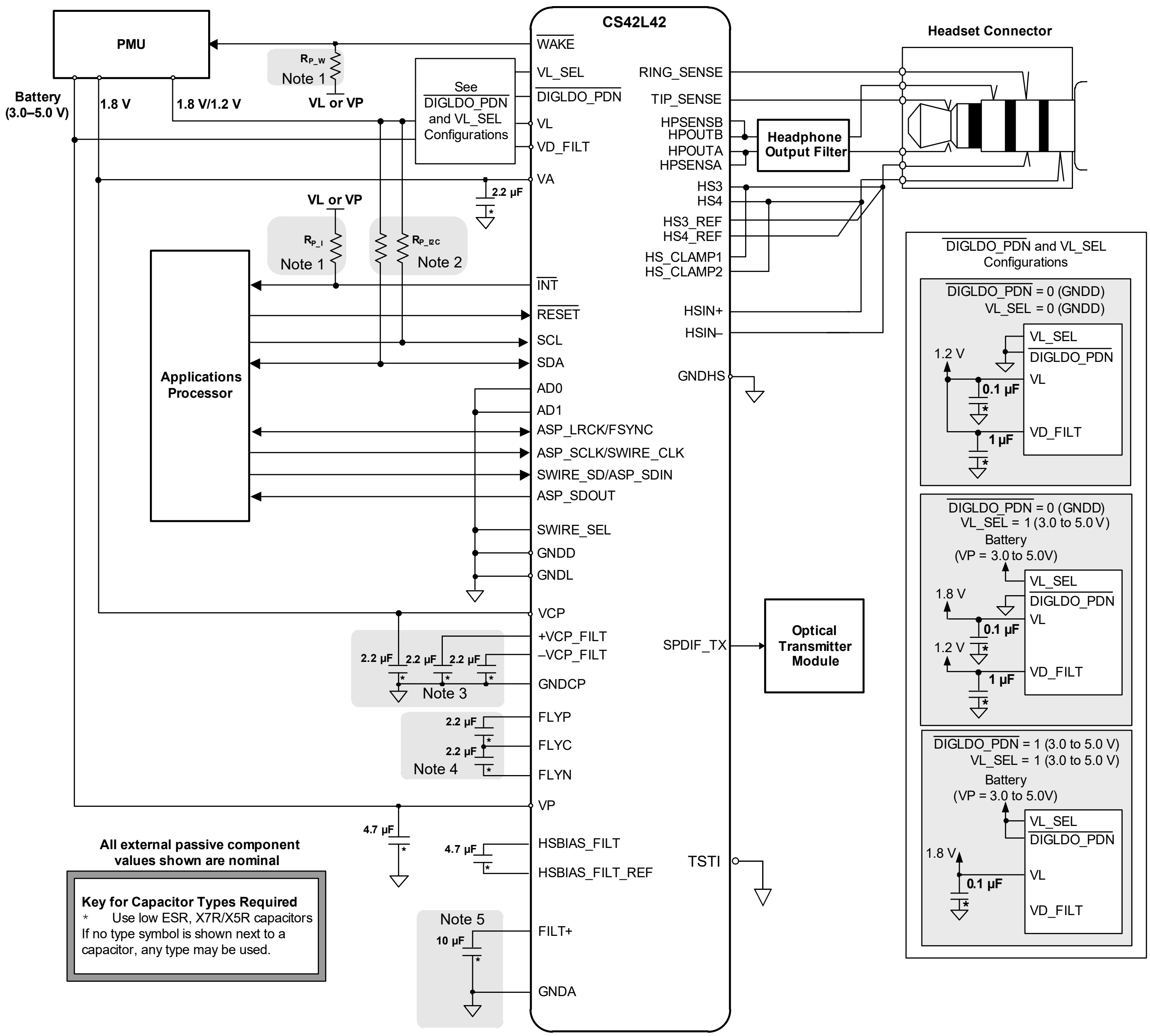


Figure 2-1. Typical Connection Diagram for I2C, I2S, or TDM

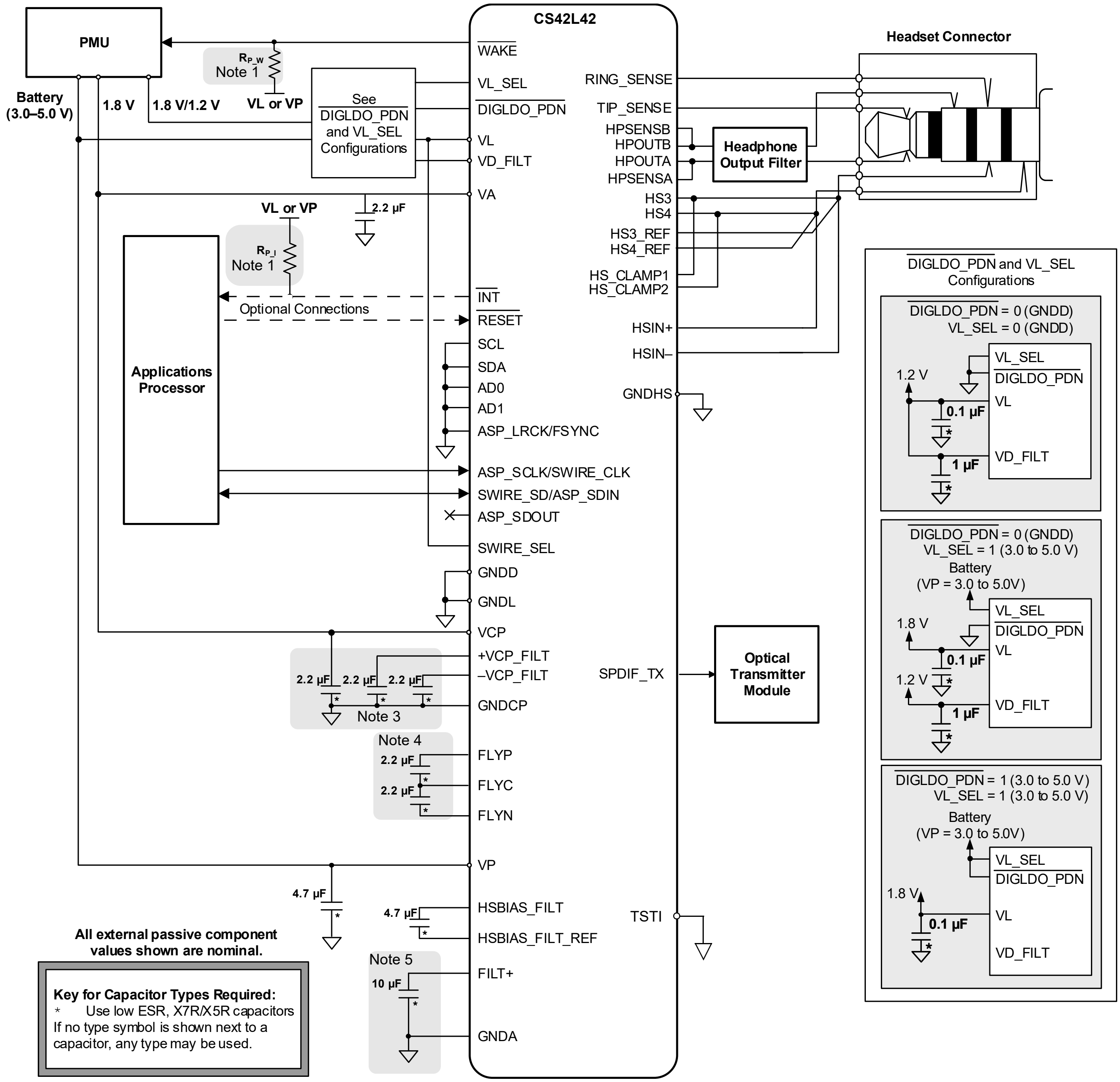


Figure 2-2. Typical Connection Diagram for SoundWire

Notes:

1. R_{P_I} and R_{P_W} values can be determined by the $\overline{\text{INT}}$ and $\overline{\text{WAKE}}$ pin specifications in Table 3-25.
2. R_{P_I2C} values can be determined by the I²C pull-up resistance specification in Table 3-24.
3. The headphone amplifier's output power and distortion ratings use the nominal capacitances shown. Larger capacitance reduces ripple on the internal amplifiers' supplies and, in turn, reduces distortion at high-output power levels. Smaller capacitance may not reduce ripple enough to achieve output power and distortion ratings. Because actual values of typical X7R/X5R ceramic capacitors deviate from nominal values by a percentage specified in the manufacturer's data sheet, capacitors must be selected for minimum output power and maximum distortion required. Higher value capacitors than those shown may be used, however lower value capacitors must not (values can vary from the nominal by ±20%). See Section 2.1.2 for additional details.
4. Series resistance in the path of the power supplies must be avoided. Any voltage drop on VCP directly affects the negative charge-pump supply (–VCP_FILT) and clips the audio output.
5. Lowering capacitance below the value shown affects PSRR, THD+N performance, ADC–DAC isolation and intermodulation, and interchannel isolation and intermodulation.

2.1 Electromagnetic Compatibility (EMC) Circuitry

The circuit in Fig. 2-3 may be applied to signals not local to the CS42L42 (i.e., that traverse significant distances) for EMC.

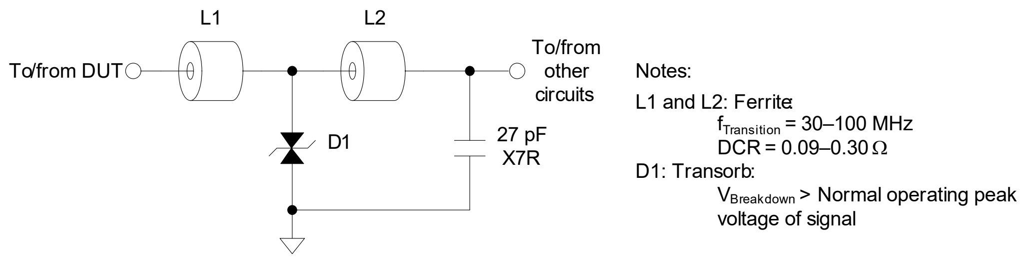


Figure 2-3. Optional EMC Circuit

2.1.1 Low-Profile Charge-Pump Capacitors

In the typical connection for analog mics (Fig. 2-1), the recommended capacitor values for the charge-pump circuitry are 2.2 µF, rated as X7R/X5R or better. The following low-profile versions of these capacitors are suitable for the application:

- Description: 2.2 µF ±20%, 6.3 V, X5R, 0201
- Manufacturer, Part Number: Murata, GRM033R60J225ME47, nominal height = 0.3 mm
- Manufacturer, Part Number: AVX, 02016D225MAT2A, nominal height = 0.33 mm

Note: Although the 0201 capacitors described are suitable, larger capacitors such as 0402 or larger may provide acceptable performance.

2.1.2 Ceramic Capacitor Derating

Note 3 in Fig. 2-1 highlights that ceramic capacitor derating factors can significantly affect in-circuit capacitance values and, in turn, CS42L42 performance. Under typical conditions, numerous types and brands of large-value ceramic capacitors in small packages exhibit effective capacitances well below their ±20% tolerance, with some being derated by as much as –50%. These same capacitors, when tested by a multimeter, read much closer to their rated value. A similar derating effect has not been observed with tantalum capacitors.

The derating observed varied with manufacturer and physical size: Larger capacitors performed better, as did ones from Kemet Electronics Corp. and TDK Corp. of any size. This derating effect is described in data sheets and in applications notes from capacitor manufacturers. For instance, as DC and AC voltages are varied from the standard test points (applied DC and AC voltages for standard test points versus PSRR test are 0 and 1 V_{RMS} @ 1 kHz versus 0.9 V and ~1 mV_{RMS} @ 20 Hz–20 kHz), it is documented that the capacitances vary significantly.

3 Characteristics and Specifications

Table 3-1 defines parameters as they are characterized in this section.

Table 3-1. Parameter Definitions

Parameter	Definition
Dynamic range	The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. A signal-to-noise ratio measurement over the specified bandwidth made with a –60 dB signal; 60 dB is added to resulting measurement to refer the measurement to full scale. This technique ensures that distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17–1991, and the Electronic Industries Association of Japan, EIAJ CP–307. Dynamic range is expressed in decibel units.
Idle channel noise	The rms value of the signal with no input applied (properly back-terminated analog input, digital zero, or zero modulation input). Measured over the specified bandwidth.
Interchannel isolation	A measure of cross talk between the left and right channel pairs. Interchannel isolation is measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Interchannel isolation is expressed in decibel units.
Load resistance and capacitance	The recommended minimum resistance and maximum capacitance required for the internal op-amp's stability and signal integrity. The load capacitance effectively moves the band-limiting pole of the amp in the output stage. Increasing load capacitance beyond the recommended value can cause the internal op-amp to become unstable.
Offset error	The deviation of the midscale transition (111…111 to 000…000) from the ideal.
Output offset voltage	The DC offset voltage present at the amplifier's output when its input signal is in a mute state. The offset exists due to CMOS process limitations and is proportional to analog volume settings. When measuring the offset out the headphone amplifier, the headphone amplifier is ON.
Total harmonic distortion + noise (THD+N)	The ratio of the rms sum of distortion and noise spectral components across the specified bandwidth (typically 20 Hz–20 kHz) relative to the rms value of the signal. THD+N is measured at –1 and –20 dBFS for the analog input and at 0 and –20 dB for the analog output, as suggested in AES17–1991 Annex A. THD+N is expressed in decibel units.

Table 3-2. Recommended Operating Conditions

Test conditions: GNDA = GNDL = GNDCP = 0 V; voltages are with respect to ground.

Parameters			Symbol	Minimum [1]	Maximum [1]	Unit
DC power supply	Charge pump		VCP	1.66	1.94	V
	LDO regulator for digital [2]	$\overline{\text{DIGLDO\_PDN}}$ = 0 and VL_SEL = 0	VD_FILT	1.10	1.30	V
	Serial interface control port and S/PDIF transmitter	$\overline{\text{DIGLDO\_PDN}}$ = 0 and VL_SEL = 0 VL_SEL = 1	VL VL	1.10 1.66	1.30 1.94	V V
	Analog		VA	1.66	1.94	V
	Battery supply		VP	2.50 [3]	5.25	V
External voltage applied to pin [4,5]		TIP_SENSE pin ±VCP_FILT domain pins [6] VL domain pins VA domain pins VP domain pins	V_{INHI} V_{VCPF} V_{VL} V_{VA} V_{VP}	–VCP_FILT – 0.3 –VCP_FILT – 0.3 –0.3 –0.3 –0.3	VP + 0.3 +VCP_FILT + 0.3 VL + 0.3 VA + 0.3 VP + 0.3	V V V V V
Ambient temperature			T_A	–40	+85	°C

1. Device functional operation is guaranteed within these limits; operation outside them is not guaranteed or implied and may reduce device reliability.
2. If $\overline{\text{DIGLDO\_PDN}}$ is deasserted, no external voltage must be applied to VD_FILT.
3. Although device operation is guaranteed down to 2.5 V, device performance is guaranteed only down to 3.0 V. The following are affected when VP < 3.0 V: HSBIAS, charge pump LDO, TIP_SENSE threshold, RING_SENSE threshold.
4. The maximum over/undervoltage is limited by the input current.
5. Table 1-1 lists the power supply domain in which each CS42L42 pin resides.
6. ±VCP_FILT is specified in Table 3-16.

Table 3-3. Absolute Maximum Ratings

Test conditions: GNDA = GNDL = GNDCP = 0 V; voltages are with respect to ground.

Parameters		Symbol	Minimum	Maximum	Unit
DC power supply	Charge pump, LDO, serial/control, analog (see Section 4.15) Digital core Battery	VL, VA, VCP VD_FILT VP	–0.3 –0.3 –0.3	2.33 1.55 6.3	V V V
Input current [1]		I_{in}	—	±10	mA
Ambient operating temperature (power applied)		T_A	–50	+115	°C
Storage temperature		T_{stg}	–65	+150	°C

Caution: Stresses beyond "Absolute Maximum Ratings" levels may cause permanent damage to the device. These levels are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Table 3-2, "Recommended Operating Conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1. Any pin except supply pins. Transient currents of up to ±100 mA on analog input pins do not cause SCR latch-up.

Table 3-4. Output Fault Rating

Test conditions: GNDA = GNDCP = 0 V; VA = 1.8 V; VP = 3.6 V; voltages are with respect to ground.

Source [1]	Fault Supply	Expected Years [2]
HPOUT(A,B)	VA GNDA +VCP_FILT –VCP_FILT VP	1.5 2 0.5 1.5 1.5
HS3/HS4 (HSx switch to ground)	HPOUT(A,B)[3]	3.2
HS3/HS4 (HSx switches to HSBIAS)	HPOUT(A,B)[3]	0.75
HS3_REF/HS4_REF (HSx connected to ground)	HPOUT(A,B)	3.2
HS3_REF/HS4_REF (HSx not connected to ground)	HPOUT(A,B)	0.75

1. Each source is individually connected directly to the specified supply during a fault condition.
2. The rating is based on foundry electromigration design rules when a perpetual fault exists on the HP outputs. When the specified time expires, analog performance is expected to degrade.
3. HPOUTx = 1 Vrms. If shorted to HSx, the headphone may be current limited in this configuration.

Table 3-5. Combined High-Performance ADC On-Chip Analog and Digital Filter Characteristics

Test conditions (unless specified otherwise): T_A = +25°C; MCLK = 12 MHz; MCLK_SRC_SEL = 0; Fs_{INT} = 48 kHz; path is HSIN to internal routing engine. All gains are set to 0 dB; HPF disabled.

Parameter [1,2]			Min	Typical	Max	Unit
Notch filter on (ADC_NOTCH_ DIS = 0)	Passband (normalized to 0.417x10^{-3} Fs_{INT})	–0.18-dB corner –3.0-dB corner	— —	0.390 0.410	— —	Fs_{int} Fs_{int}
	Passband ripple (0.417x10^{-3} Fs_{INT} to 0.390 Fs_{INT}; normalized to 0.417x10^{-3} Fs_{int})		–0.23	—	0.15	dB
	Stopband attenuation 1 (0.5 Fs_{INT} to 0.524 Fs_{INT})		45	—	—	dB
	Stopband attenuation 2 (0.524 Fs_{INT} to 3 Fs_{INT})		70	—	—	dB
	Total group delay [3]		—	5.6/Fs_{int}	—	s
Notch filter off (ADC_NOTCH_ DIS = 1)	Passband (normalized to 0.417x10^{-3} Fs_{INT})	–0.05-dB corner –3.0-dB corner	— —	0.390 0.500	— —	Fs_{int} Fs_{int}
	Passband ripple (0.417x10^{-3} Fs_{INT} to 0.417 Fs_{INT}; normalized to 0.417x10^{-3} Fs_{INT})		–0.29	—	0.15	dB
	Stopband attenuation (0.64 Fs_{INT} to 3 Fs_{INT})		70	—	—	dB
	Total group delay [3]		—	5.6/Fs_{int}	—	s

1. Response scales with Fs_{int} (internal sample rate, based on MCLK). Specifications are normalized to Fs_{int} and are denormalized by multiplying by Fs_{int}.
2. Measurements with HPF disabled require either differential configuration or single-ended configuration with –30 dBFS input signal.
3. Informational only; group delay cannot be measured for this block by itself.Total group delay includes delay through the entire ADC and decimator path total-group delay is measured at 1 kHz.

Table 3-6. ADC High-Pass Filter (HPF) Characteristics

Test conditions (unless specified otherwise): ADC_HPF_CF = 00; all gains are set to 0 dB; specifications represent the frequency response of the entire path with ADC_NOTCH_DIS = 1, SRC_ADC_BYPASS = 1, ADC_WNF_EN = 0, and ADC_HPF_EN = 1.

Parameter [1]		Minimum	Typical	Maximum	Unit
Passband (normalized to 0.2083 FS_{INT})	–0.05-dB corner –3.0-dB corner	— —	0.666 x 10^{-3} 77.0 x 10^{-6}	— —	Fs_{INT} Fs_{INT}
Phase deviation @ 0.453 x 10^{-3} Fs_{INT} [2]		—	12.37	—	Deg
Filter settling time [3]	ADC_HPF_CF = 00 (38.8 x 10^{-6} x Fs_{INT} mode) ADC_HPF_CF = 01 (2.5 x 10^{-3} x Fs_{INT} mode) ADC_HPF_CF = 10 (4.9 x 10^{-3} x Fs_{INT} mode) ADC_HPF_CF = 11 (9.7 x 10^{-3} x Fs_{INT} mode)	— — — —	2900/Fs_{INT} 170/Fs_{INT} 90/Fs_{INT} 50/Fs_{INT}	— — — —	s s s s

1. Response scales with Fs_{INT} (based on internal MCLK). Specifications are normalized to Fs_{INT} and are denormalized by multiplying by Fs_{INT}.
2. An additional –2° phase deviation may be present through the total path from HSIN to SDOUT.
3. Required time for the magnitude of the DC component present at the output of the HPF to reach 5% of the applied DC signal.

Table 3-7. Combined DAC Digital, On-Chip Analog, and HPOUTx Filter Characteristics

Test conditions (unless specified otherwise): T_A = +25°C; MCLK = 12 MHz, MCLK_SRC_SEL = 0, Fs_{INT} = 48 kHz; path is internal routing engine to HPOUTx, analog and digital gains are all set to 0 dB; HPF disabled.

Parameter [1]		Minimum	Typical	Maximum	Unit
Passband	–0.05-dB corner –3.0-dB corner	— —	0.48 0.50	— —	Fs_{INT} Fs_{INT}
Passband ripple (0.417x10^{-3} Fs_{INT} to 0.417 Fs_{INT}; normalized to 0.417x10^{-3} Fs_{INT})		–0.04	—	0.063	dB
Stopband attenuation (0.545 Fs_{INT} to Fs_{INT})		60	—	—	dB
Total group delay [2]		—	5.35/Fs_{INT}	—	s

1. Response scales with Fs_{INT} (based on internal MCLK). Specifications are normalized to Fs_{INT} and denormalized by multiplying by Fs_{INT}.
2. Informational only; group delay cannot be measured for this block by itself. An additional 5.5/Fs_{int} group delay may be present through the serial ports and internal audio bus.

Table 3-8. DAC High-Pass Filter (HPF) Characteristics

Test conditions (unless specified otherwise) Analog and digital gains are all set to 0 dB; T_A = +25°C.

Parameter [1]		Minimum	Typical	Maximum	Unit
Passband	–0.05-dB corner –3.0-dB corner	— —	0.180×10^{-3} 19.5×10^{-6}	— —	Fs_{INT} Fs_{INT}
Passband ripple (0.417×10^{-3} Fs_{INT} to 0.417 Fs_{INT}; normalized to 0.417 Fs_{INT})		—	—	0.01	dB
Phase deviation @ 0.453×10^{-3} Fs_{INT}		—	2.45	—	°
Filter settling time [2]		—	$24.5 \times 10^3/Fs_{INT}$	—	s

1. Response scales with Fs_{INT} (internal sample rate, based on MCLK). Specifications are normalized to Fs_{INT} and are denormalized by multiplying by Fs_{INT}.
2. Required time for the magnitude of the DC component present at the output of the HPF to reach 5% of the applied DC signal.

Table 3-9. HSINx to SDOUT with SRC-Enabled Datapath Characteristics

Test conditions (unless specified otherwise): LRCK = Fs_{INT} = Fs_{EXT} = 48 kHz; MCLK = 12 MHz; HPF disabled; passband/stopband levels normalized to 20 Hz; entire path characteristics including AFE + ADC + SRC + serial port.

Parameters [1,2]			Minimum	Typical	Maximum	Unit
ADC notch filter enabled	Passband	–0.22-dB corner –3.0-dB corner	— —	0.390 0.410	— —	Fs_{EXT} Fs_{EXT}
	Passband ripple (0.417×10^{-3} Fs_{EXT} to 0.390 Fs_{EXT}; normalized to 20 Hz)		–0.30	—	0.15	dB
	Stopband rejection from 0.477 Fs_{EXT} to 3 Fs_{EXT}		70	—	—	dB
	Square wave overshoot		—	—	3.1	dB
	Group delay, bark-weighted average		—	—	$38.5/Fs_{EXT}$	s
	Group delay	$Fs_{EXT} \leq 44.1$ kHz $Fs_{EXT} \geq 48$ kHz)	— —	$17.4/Fs_{INT} + (13.2 \pm 1.5)/Fs_{EXT}$ $(12.4 \pm 0.5)/Fs_{INT} + (11.9 \pm 1)/Fs_{EXT}$	— —	s s
	SRC-disabled group delay [3]		—	$(13.9 \pm 1)/Fs$	—	s
ADC notch filter disabled	Passband	–0.22-dB corner –3.0-dB corner	— —	0.444 0.466	— —	Fs_{EXT} Fs_{EXT}
	Passband ripple (0.417×10^{-3} Fs_{EXT} to 0.417 Fs_{EXT}; normalized to 20 Hz)		–0.30	—	0.15	dB
	Stopband rejection from 0.480 Fs_{EXT} to 0.521 Fs_{EXT}		55	—	—	dB
	Stopband rejection from 0.521 Fs_{EXT} to 0.640 Fs_{EXT}		14	—	—	dB
	Stopband rejection from 0.640 Fs_{EXT} to 3 Fs_{EXT}		70	—	—	dB
	Square wave overshoot		—	—	3.1	dB
	Group delay, bark-weighted average		—	—	$38.5/Fs_{EXT}$	s
	Group delay	$Fs_{EXT} \leq 44.1$ kHz $Fs_{EXT} \geq 48$ kHz)	— —	$17.4/Fs_{INT} + (13.2 \pm 1.5)/Fs_{EXT}$ $(12.4 \pm 0.5)/Fs_{INT} + (11.9 \pm 1)/Fs_{EXT}$	— —	s s
	SRC disabled group delay [3]		—	$(13.9 \pm 1)/Fs$	—	s

1. Fs_{EXT} is the external sample rate (LRCK/FSYNC frequency). Response scales with Fs_{EXT}.
2. Measurements with HPF disabled require either differential configuration or single-ended configuration with –30 dBFS input signal.
3. This value varies by up to 1 Fs. If SRC is disabled, Fs = Fs_{OUT} = Fs_{IN}.

Table 3-10. SDIN to HPOUTx with SRC-Enabled Datapath Characteristics

Test conditions (unless specified otherwise): LRCK = Fs_{INT} = Fs_{EXT} = 48 kHz; MCLK = 12 MHz; HPF disabled; passband/stopband levels normalized to 0.417×10^{-3} Fs_{EXT}; entire path characteristics including serial port + SRC + DAC + HPOUT.

Parameters [1]		Minimum	Typical	Maximum	Unit
Passband	–0.2-dB corner –3.0-dB corner	— —	0.463 0.466	— —	Fs_{EXT} Fs_{EXT}
Passband ripple (0.417×10^{-3} Fs_{EXT} to 0.417 Fs_{EXT}; normalized to 0.417×10^{-3} Fs_{EXT})		–0.16	—	0.02	dB
Response at 0.5 Fs_{EXT}		—	—	–54.9	dB
Stopband rejection from 0.480 Fs_{EXT} to 0.524 Fs_{EXT}		55	—	—	dB
Stopband rejection from 0.524 Fs_{EXT} to 0.545 Fs_{EXT}		39	—	—	dB
Stopband rejection from 0.545 Fs_{EXT} to 3 Fs_{EXT}		60	—	—	dB
Square wave overshoot		—	—	3.1	dB
Group delay, bark-weighted average		—	—	$34/Fs_{EXT}$	s
Group delay	$Fs_{EXT} \leq 48$ kHz $Fs_{EXT} \geq 88.2$ kHz)	— —	$(15.8 \pm 1.5)/Fs_{EXT} + 10.3/Fs_{INT}$ $(20.1 \pm 1)/Fs_{EXT} + (11.6 \pm 0.5)/Fs_{INT}$	— —	s s
SRC disabled group delay [2]		—	$(15 \pm 1)/Fs$	—	s

1. Fs_{EXT} is the external sample rate (LRCK/FSYNC frequency). Response scales with Fs_{EXT}.
2. This value varies by up to 1 Fs. If SRC is disabled, Fs = Fs_{OUT} = Fs_{IN}.

Table 3-11. Wind-Noise Digital Filter Characteristics

Test conditions (unless specified otherwise): MCLK = 12 MHz; MCLK_SRC_SEL = 0; Fs_{INT} = 48 kHz; ADC HPF disabled.

Parameters [1,2]		Minimum	Typical	Maximum	Unit
Passband –3.0-dB corner	ADC_WNF_CF = 000	—	160	—	Hz
	ADC_WNF_CF = 001	—	180	—	Hz
	ADC_WNF_CF = 010	—	200	—	Hz
	ADC_WNF_CF = 011	—	220	—	Hz
	ADC_WNF_CF = 100	—	240	—	Hz
	ADC_WNF_CF = 101	—	260	—	Hz
	ADC_WNF_CF = 110	—	280	—	Hz
	ADC_WNF_CF = 111	—	300	—	Hz
Passband –0.05-dB corner	ADC_WNF_CF = 000	—	280	—	Hz
	ADC_WNF_CF = 001	—	315	—	Hz
	ADC_WNF_CF = 010	—	350	—	Hz
	ADC_WNF_CF = 011	—	385	—	Hz
	ADC_WNF_CF = 100	—	420	—	Hz
	ADC_WNF_CF = 101	—	455	—	Hz
	ADC_WNF_CF = 110	—	490	—	Hz
	ADC_WNF_CF = 111	—	525	—	Hz
Passband ripple (–0.05-dB corner to 0.417 Fs_{INT}; normalized to 0.417 Fs_{INT})		—	—	0.15	dB
Filter settling time	ADC_WNF_CF = 000	—	731/Fs_{INT}	—	s
	ADC_WNF_CF = 001	—	650/Fs_{INT}	—	s
	ADC_WNF_CF = 010	—	585/Fs_{INT}	—	s
	ADC_WNF_CF = 011	—	532/Fs_{INT}	—	s
	ADC_WNF_CF = 100	—	487/Fs_{INT}	—	s
	ADC_WNF_CF = 101	—	450/Fs_{INT}	—	s
	ADC_WNF_CF = 110	—	418/Fs_{INT}	—	s
	ADC_WNF_CF = 111	—	390/Fs_{INT}	—	s

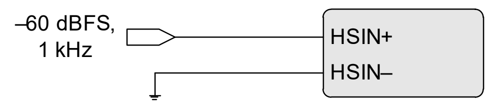
1. Responses are clock dependent and scale with Fs_{INT}. The full-band response plot (Fig. 9-28) is normalized to Fs_{INT} and is denormalized by multiplying the x-axis scale by Fs. Passband frequencies above the transition-band response plot (Fig. 9-29) are for a Fs_{INT} of 48 kHz. Frequencies for other Fs_{INT} values are determined by multiplying the x-axis scale shown in the transition band plot and passband frequencies above by a factor of Fs_{INT}/48 kHz.
2. Wind-noise HPF characteristics apply only if the given filter is enabled (ADC_WNF_EN = 1). Otherwise, the signal is unaffected by this block.

Table 3-12. HSIN-to-Serial Data Out Characteristics

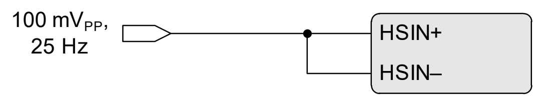
Test conditions (unless specified otherwise): Fig. 2-1 and Fig. 2-2 show CS42L42 connections; input is a full-scale 1-kHz sine wave; GNDA = GNDL = GNDCP = 0 V; voltages are with respect to ground; parameters and can vary with VA; typical performance data taken with VL = VA = 1.8 V, VP = 3.6 V; min/max performance data taken with VA = 1.66–1.94 V; VL = 1.8 V, VP = 3.6 V; T_A = +25°C; measurement bandwidth is 20 Hz–20 kHz; ASP_LRCK = Fs = 48 kHz; MCLK = 12 MHz; SRC bypassed in data path; mixer attenuation and digital volume = 0 dB. ADC_HPF_EN = 1. Specifications valid for pseudodifferential and fully differential inputs.

Parameter [1]			Minimum	Typical	Maximum	Unit
Dynamic range [2] (defined in Table 3-1)		A-weighted	108	114	—	dB
		Unweighted	105	111	—	dB
THD+N [3] (defined in Table 3-1)		Differential, –1-dBFS input	—	–85	–79	dB
		Single-ended, –1-dBFS input	—	–80	–74	dB
Common-mode rejection [4]			—	72	—	dB
DC voltage on HSIN with pin floating			—	1.35	—	V
Accuracy	Offset error (defined in Table 3-1) [5]			127		LSB
	Gain drift		—	±100	—	ppm/°C
Input	HP amp-to-analog input isolation	R_L = 3 kΩ	—	90	—	dB
		R_L = 30 Ω	—	83	—	dB
	Full-scale signal input voltage [6]		1.5•VA	1.57•VA	1.64•VA	Vpp
	Input impedance [7]		45	50	—	kΩ
	Turn-on time [8]	ADC_SOFTRAMP_EN = 0	—	—	25	ms

1. Parameters in this table are described in detail in Table 3-1.
2. (HSIN dynamic range test configuration (pseudodifferential). Input signal is –60 dB down from the corresponding full-scale voltage.



3. ADC_HPF_EN must remain asserted for proper functionality. Failure to do so may cause clipping of the ADC digital output.
4. HSIN CMRR test configuration



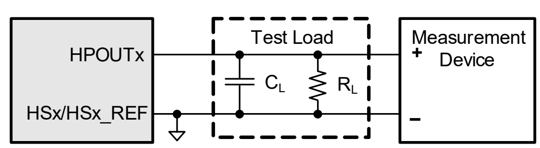
5. SDOUT code with ADC_HPF_EN = 1 (see p. 155), ADC_DIG_BOOST = 0 (see p. 154).
6. ADC full-scale input voltage is measured on between HSIN+ and HSIN–. This is for single-ended or pseudodifferential input signals.
7. Measured between HSIN+ and HSIN–.
8. Turn-on time is measured from the ADC_PDN = 0 ACK signal to when data comes through the DAO port or SoundWire port. In most cases, enabling the SRC increases the turn-on time and may exceed the maximum value specified.

Table 3-13. Serial Data In-to-HPOUTx Characteristics

Test conditions (unless specified otherwise): Fig. 2-1 and Fig. 2-2 show CS42L42 connections; input test signal is a 24-bit full-scale 997-Hz sine wave with 1 LSB of triangular PDF dither applied; GNDA = GNDL = GNDCP = 0 V; voltages are with respect to ground; parameters can vary with VA; typical performance data taken with VL = VA = 1.8 V, VP = 3.6 V; min/max performance data taken with VA = 1.66–1.94 V; VL = 1.8 V, VP = 3.6 V; VCP Mode; T_A = +25°C; measurement bandwidth is 20 Hz–20 kHz; ASP_LRCK = Fs_{INT} = 48-kHz mode; MCLK = 12 MHz, MCLK_SRC_SEL = 0; mixer attenuation and digital volume = 0 dB; FULL_SCALE_VOL = 0 (0dB); HP load: R_L = 30 Ω, C_L = 1 nF (HPOUT_LOAD = 0) and R_L = 3 kΩ, C_L = 10 nF (HPOUT_LOAD = 1)SRC bypassed.

Parameter [1]				Minimum	Typical	Maximum	Unit
R_L = 3 kΩ VP_CP Mode	Dynamic range (defined in Table 3-1)	18–24 bit	A-weighted	108	114	—	dB
			unweighted	105	111	—	dB
	THD+N [2] (defined in Table 3-1)	18–24 bit	0 dB	—	–90	–84	dB
			–20 dB	—	–83	—	dB
			–60 dB	—	–51	–48	dB
		16 bit	0 dB	—	–88	–82	dB
			–20 dB	—	–73	—	dB
			–60 dB	—	–33	–27	dB
	Idle channel noise (A-weighted)			—	2.0	—	µV
	Full-scale output voltage [3]			1.50•VA	1.58•VA	1.66•VA	V_{PP}
R_L = 30 Ω VP_CP Mode	Dynamic range (defined in Table 3-1)	18–24 bit	A-weighted	108	114	—	dB
			unweighted	105	111	—	dB
	THD+N [2] (defined in Table 3-1)		Pout = 10 mW	—	–98	—	dB
			Pout = 35 mW	—	–75	–69	dB
	Full-scale output voltage [3]			1.50•VA	1.58•VA	1.66•VA	V_{PP}
	Output power [2]			—	35.0	—	mW
R_L = 15 Ω VCP Mode (FULL_SCALE_VOL = 1 [–6 dB])	Dynamic range (defined in Table 3-1)	18–24 bit	A-weighted	102	108	—	dB
			unweighted	99	105	—	dB
	THD+N [2] (defined in Table 3-1)		Pout = 17.3 mW	—	–75	–69	dB
	Full-scale output voltage [3]			0.71•VA	0.79•VA	0.86•VA	V_{PP}
	Output power [2]			—	17.3	—	mW
R_L = 15 Ω VP_CP Mode	Dynamic range	18–24 bit	A-weighted	102	108	—	dB
			unweighted	99	105	—	dB
Other characteristics (Table 3-1 gives parameter definitions.)	Interchannel isolation [3] (3 kΩ)		217 Hz	—	90	—	dB
			1 kHz	—	90	—	dB
			20 kHz	—	80	—	dB
	Interchannel isolation [3] (30 Ω)		217 Hz	—	90	—	dB
			1 kHz	—	90	—	dB
			20 kHz	—	70	—	dB
	Output offset voltage: mute [3,4] (ANA_MUTE_x = 1, see p. 156)		HPOUTx	—	±0.5	±1.0	mV
	Output offset voltage [3,4]		HPOUTx	—	±0.5	±2.5	mV
	Load resistance (R_L)		Normal operation [3]	15	—	—	Ω
	Load capacitance (C_L) [3,5]		HPOUT_LOAD = 0	—	—	1	nF
			HPOUT_LOAD = 1	—	—	10	nF
	Turn-on time [6]		SLOW_START_EN = 000	—	—	25	ms

1. One LSB of triangular PDF dither is added to data.
2. Because VCP settings lower than VA reduce the HP amplifier headroom, the specified THD+N performance at full-scale output voltage and power may not be achieved.
3. HP output test configuration. Symbolized component values are specified in the test conditions above.



4. Assumes no external impedance on HSx/HSx_REF. External impedance on HSx/HSx_REF affects the offset and step deviation. See Section 4.4.1.
5. Amplifier is guaranteed to be stable with either headphone load setting.
6. Turn-on time is measured from when the HP_PDN = 0 ACK signal is received to when the signal appears on the HP output. In most cases, enabling the SRC increases the turn-on time and may exceed the maximum specified value.

Table 3-14. HSBIAS Characteristics

Test conditions (unless specified otherwise): Fig. 2-1 and Fig. 2-2 show CS42L42 connections; GNDHS = GNDA = GNDL = GNDCP = 0 V; voltages are with respect to ground; parameters can vary with VA and VP; typical performance data taken with VL = VA = 1.8 V, VP = 3.6 V; min/max performance data taken with VA = 1.66–1.94 V, VL = 1.8 V, VP = 3.0–5.25; I_{OUT} = 500 µA; T_A = +25°C; PDN_ALL = 0, HSBIAS_CTRL = 2.7-V Mode.

Parameters [1]				Minimum	Typical	Maximum	Unit
Output voltage [2]	PDN_ALL	DETECT_MODE	HSBIAS_CTRL				
	0/1	0x (inactive/short detect only)	10 (2.0-V Mode)	1.40	1.86	2.15	V
	0/1	01 (short detect only)	11 (2.7-V Mode)	1.75	2.30	2.70	V
	0	11 (Normal Mode)	10 (2.0-V Mode) [3]	1.80	2.00	2.10	V
	0	00/11 (inactive/Normal Mode)	11 (2.7-V Mode)	2.61	2.75	2.86	V
DC output current, I_{OUT2} [4]			HSBIAS_CTRL = 10 (2.0-V Mode)	—	0.91	—	mA
			HSBIAS_CTRL = 11 (2.7-V Mode)	—	1.2	—	mA
Integrated output noise (measured at HSx)			f = 100 Hz–20 kHz	—	—	4	µVrms
Output resistance, R_{OUTx}				2.19	2.21	2.23	kΩ
Output resistance temperature variation			–40°C to +85°C		±3		%
Current-sense trip point			HSBIAS_SENSE_TRIP = 000	—	12	—	µA
			HSBIAS_SENSE_TRIP = 001	—	23	—	µA
			HSBIAS_SENSE_TRIP = 010	—	41	—	µA
			HSBIAS_SENSE_TRIP = 011	—	52	—	µA
			HSBIAS_SENSE_TRIP = 100	—	64	—	µA
			HSBIAS_SENSE_TRIP = 101	—	75	—	µA
			HSBIAS_SENSE_TRIP = 110	—	93	—	µA
			HSBIAS_SENSE_TRIP = 111	—	104	—	µA
Capacitive load				—	—	100	µF

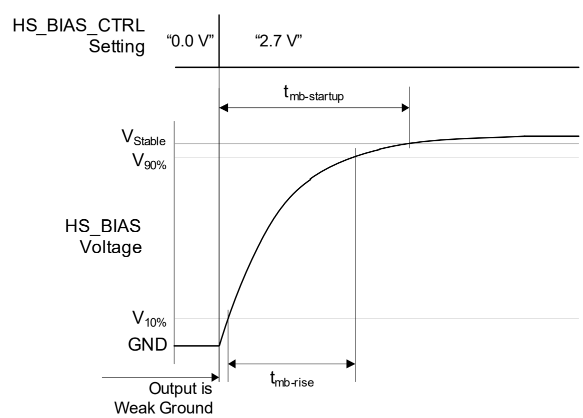
1. If HSBIAS_CTRL = 01, the internal HSBIAS node is to be shorted to ground. Output is pulled down to ground via an internal resistance of R_{OUT} to the HS3/HS4 pins, which is, in turn, connected internally or externally to ground (per Fig. 2-1).
2. The output voltage is the unloaded, open-circuit voltage present at the HSx pin selected as HSBIAS output.
3. No audio is allowed on HSIN/HSx if DETECT_MODE = 11 and HSBIAS_CTRL = 10.
4. Specifies use limits for the normal operation and HSIN short conditions.

Table 3-15. Switching Specifications—HSBIAS

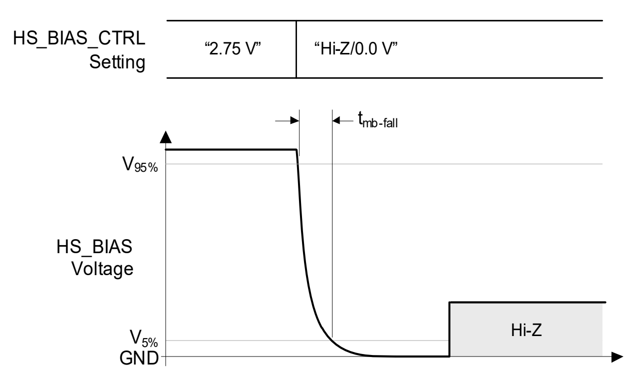
Test conditions (unless specified otherwise): Fig. 2-1 shows CS42L42 connections; GNDA = GNDP = GNDCP = GNDD = 0 V; voltages are with respect to ground; parameters can vary with VA and VP; typical performance data taken with VL = VA = VCP = 1.8 V, VP = 3.6 V; min/max performance data taken with VA = 1.66–1.94 V; VL = VCP = 1.8 V; VP = 3.0–5.25; I_{OUT} = 500 µA (not valid for fall time); T_A = +25°C; PDN_ALL = 0, DETECT_MODE = Normal Mode.

Parameters [1]			Symbol	Minimum	Typical	Maximum	Unit
HS bias rise time [2, 3]		HSBIAS_RAMP = 00	$t_{mb\text{-}rise}$	—	0.002	—	ms
		HSBIAS_RAMP = 01		—	10	—	ms
		HSBIAS_RAMP = 10		—	25	—	ms
		HSBIAS_RAMP = 11		—	50	—	ms
HS bias fall time [4]		HSBIAS_RAMP = 00	$t_{mb\text{-}fall}$	—	3	—	ms
		HSBIAS_RAMP = 01		—	15	—	ms
		HSBIAS_RAMP = 10		—	37	—	ms
		HSBIAS_RAMP = 11		—	75	—	ms
HS bias transition time [5]	Condition 1 [6]	1.8 V → Hi-Z	$t_{mb\text{-}tran}$	—	92	—	µs
		2.0 V → Hi-Z		—	92	—	µs
		2.3 V → Hi-Z		—	93	—	µs
	Condition 2 [7]	2.7 V → 2.3 V	$t_{mb\text{-}tran}$	—	23	—	µs
		1.8 V → 2.3 V		—	20	—	µs
		2.0 V → 2.3 V		—	18	—	µs
		2.0 V → 2.7 V		—	1	—	µs
	Condition 3 [8]	Hi-Z → 1.8 V	$t_{mb\text{-}tran}$	—	96	—	µs
		Hi-Z → 2.3 V		—	96	—	µs
	Condition 4 [8,9]		$t_{mb\text{-}tran}$	—	10	—	ms
	Condition 5 [10]	Hi-Z → 2.7 V, HSBIAS_RAMP = 01	$t_{mb\text{-}tran}$	—	183	—	µs
		Hi-Z → 2.3 V, HSBIAS_RAMP = 10		—	198	—	µs
		Hi-Z → 2.3 V, HSBIAS_RAMP = 11		—	220	—	µs
HS bias droop		Condition 2 [7]	$V_{mb\text{-}droop}$	—	—	500	mV
HS bias startup-to-stable time [11]		HSBIAS_RAMP = 00	$t_{mb\text{-}startup}$	—	0.01	—	ms
		HSBIAS_RAMP = 01		—	14	—	ms
		HSBIAS_RAMP = 10		—	36	—	ms
		HSBIAS_RAMP = 11		—	65	—	ms

1. HSBIAS startup timing example

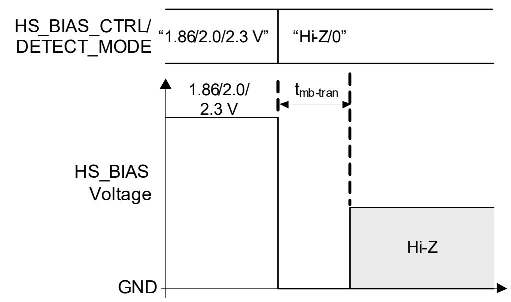


2. HSBIAS rise time is measured from 10% to 90% of the final output voltage. Transitions are specified with an HSBIAS_FILT capacitance of 4.7 µF.
3. Under the specified configuration, the HSBIAS transitions with an exponential rise time.
4. HS bias fall time is the time associated with HSBIAS falling from 95% to 5% of the programmed typical output voltage. If transitioning to Hi-Z, the output does not enter Hi-Z state until the internal digital counter completes, as determined by the HSBIAS_RAMP setting.

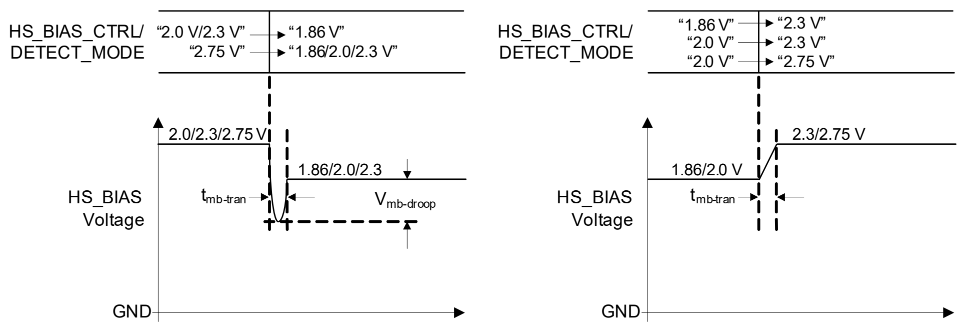


5. HS bias transitions between the GND mode and ON modes occur with no transition state.

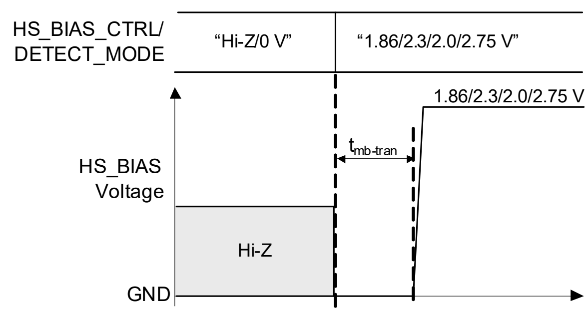
6. Condition 1 transition timing.



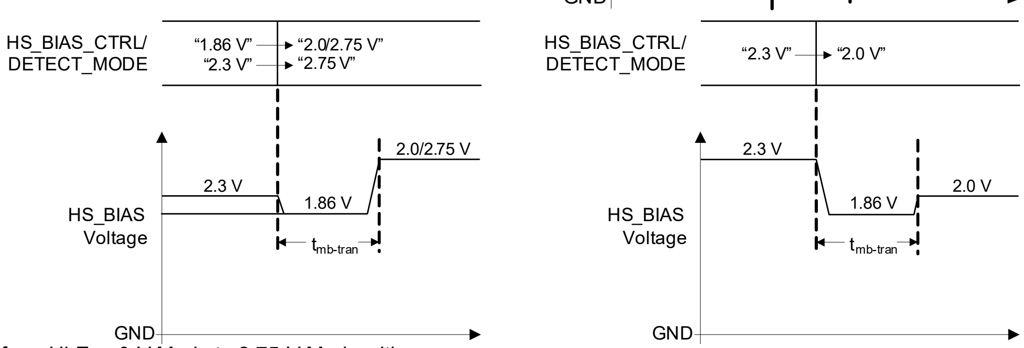
7. Condition 2 transition timing.



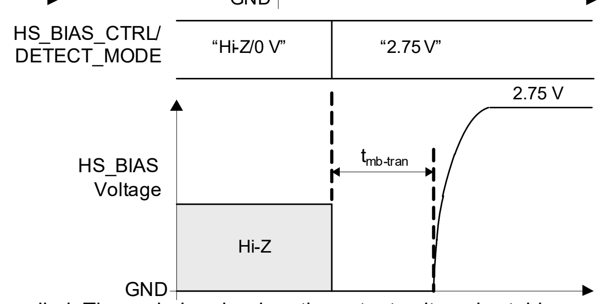
8. Due to isolation between HSBIAS internal node and HSx pins, the following is informational only and cannot be measured externally. Condition 3 applies when transitioning from Hi-Z or 0-V Mode to 1.86- or 2.30-V Mode.
Condition 4 applies when transitioning from Hi-Z or 0-V Mode to 2.0- or 2.75-V Mode with HSBIAS_RAMP = 00.



9. Condition 4 also applies when transitioning from 1.86- or 2.3-V Mode to 2.0- or 2.75-V Mode.



10. Condition 5 applies when transitioning from Hi-Z or 0-V Mode to 2.75-V Mode with HSBIAS_RAMP = 01/10/11.



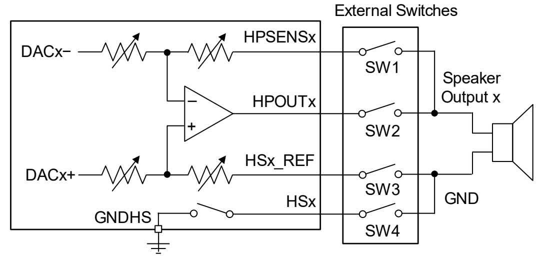
11. Mic bias startup to stable time period begins when the mic bias voltage starts to be applied. The period ends when the output voltage is stable (output voltage is at 95% of its programmed typical value).

Table 3-16. DC Characteristics

Test conditions (unless specified otherwise): Fig. 2-1 and Fig. 2-2 show CS42L42 connections; GNDA = GNDL = GNDCP = 0 V; voltages are with respect to ground; VL = VCP = VA = 1.8 V, VP = 3.6 V; T_A = +25°C.

Parameters			Minimum	Typical	Maximum	Unit
VCP_FILT (No load connected to HPOUTx.)	VP_CP Mode (ADPTPWR = 001)	+VCP_FILT –VCP_FILT	— —	2.6 –2.6	— —	V V
	VCP Mode (ADPTPWR = 010)	+VCP_FILT –VCP_FILT	— —	VCP –VCP	— —	V V
	VCP/2 Mode (ADPTPWR = 011)	+VCP_FILT –VCP_FILT	— —	VCP/2 –VCP/2	— —	V V
	VCP/3 Mode (ADPTPWR = 100)	+VCP_FILT –VCP_FILT	— —	VCP/3 –VCP/3	— —	V V
HS3/HS4 ground switch resistance (Typical values have ±25% tolerance.)			—	0.5	—	Ω
HS_CLAMPx depletion FET ground switch resistance			—	1	—	Ω
Closed-loop external switch configuration	External switch allowable ON-resistance (R_{ON}) [1]		—	—	1	Ω
	External switch ON-resistance flatness over common-mode voltage appearing at switch [1]	SW1, SW2 R_{ON} flatness SW3, SW4 R_{ON} flatness	— —	— —	0.075 0.02	Ω Ω
	External switch + PCB stray capacitance (C_{ON} + C_{OFF} + PCB_{STRAY} – C) [1]		—	100	—	pF
Other DC filter	FILT+ voltage		—	VA	—	V
	HP output current limiter on threshold. See Section 4.6.4. [2]		80	115	160	mA
	VD_FILT and VL power-on reset threshold (V_{POR})	Up Down	— —	0.777 0.628	— —	V V
HPOUT pull-down resistance [3,4]		HPOUT_PULLDOWN = 0000–0111, 1100 HPOUT_PULLDOWN = 1001 HPOUT_PULLDOWN = 1010	— — —	0.9 9.3 5.8	— — —	kΩ kΩ kΩ
Headset-Detect Comparator 1 level (Step size = 0.05 V)		HSDET_COMP1_LVL = 0000 HSDET_COMP1_LVL = 0111 HSDET_COMP1_LVL = 1111	— — —	0.65 1.0 1.4	— — —	V V V
Headset-Detect Comparator 2 level (Step size = 0.05 V)		HSDET_COMP2_LVL = 0000 HSDET_COMP2_LVL = 0111 HSDET_COMP2_LVL = 1111	— — —	1.65 2.0 2.4	— — —	V V V

1. External switches. See Section 4.4.2 for additional details.



2. The HP output current limiter threshold spec is valid only while the Class H rails are in VCP Mode.
3. Typical values have ±20% tolerance.
4. Clamp is disabled (HPOUT_CLAMP = 1) and channel is powered down (HPOUT_PDN = 1).

Table 3-17. Power-Supply Rejection Ratio (PSRR) Characteristics

Test conditions (unless specified otherwise): Fig. 2-1 and Fig. 2-2 show CS42L42 connections; input test signal held low (all zero data); GNDA = GNDL = GNDCP = 0 V; voltages are with respect to ground; VL = VA = 1.8 V, VP = 3.6 V; T_A = +25°C.

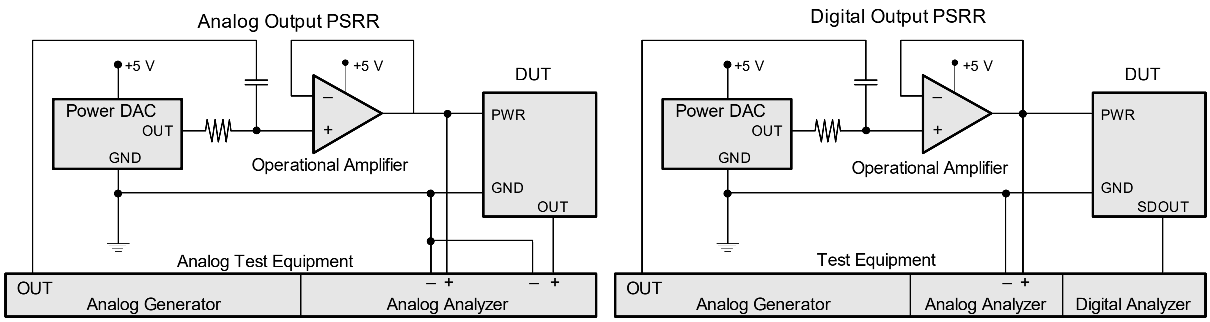
Parameters [1]		Minimum	Typical	Maximum	Unit
HSIN PSRR with 100-mVpp signal AC-coupled to VP supply	217 Hz 1 kHz 20 kHz	— — —	88 83 73	— — —	dB dB dB
HSIN PSRR with 100-mVpp signal AC-coupled to VA supply	217 Hz 1 kHz 20 kHz	— — —	70 70 55	— — —	dB dB dB
HPOUTx (–6-dB analog gain) PSRR with 100-mVpp signal AC coupled to VA supply [2]	217 Hz 1 kHz 20 kHz	— — —	75 75 70	— — —	dB dB dB
HPOUTx (–6-dB analog gain) PSRR with 100-mVpp signal AC-coupled to VCP supply [2]	217 Hz 1 kHz 20 kHz	— — —	85 85 65	— — —	dB dB dB
HPOUTx (0-dB analog gain) PSRR with 100-mVpp signal AC coupled to VP supply	217 Hz 1 kHz 20 kHz	— — —	80 80 60	— — —	dB dB dB

Table 3-17. Power-Supply Rejection Ratio (PSRR) Characteristics *(Cont.)*

Test conditions (unless specified otherwise): Fig. 2-1 and Fig. 2-2 show CS42L42 connections; input test signal held low (all zero data); GNDA = GNDL = GNDCP = 0 V; voltages are with respect to ground; VL = VA = 1.8 V, VP = 3.6 V; T_A = +25°C.

Parameters [1]		Minimum	Typical	Maximum	Unit
HSBIAS (HSBIAS = 2.7-V mode, I_{OUT} = 500 µA) PSRR with 100-mVpp signal AC coupled to VA supply [3,4]	217 Hz 1 kHz 20 kHz	— — —	105 100 83	— — —	dB dB dB
HSBIAS (HSBIAS = 2.7-V mode, I_{OUT} = 500 µA) PSRR with 1-Vpp signal AC coupled to VP supply [4]	217 Hz 1 kHz 20 kHz	— — —	108 95 70	— — —	dB dB dB
HSBIAS (Normal Mode, HSBIAS = 2.0-V mode, I_{OUT} = 500 µA) PSRR with 100-mVpp signal AC coupled to VA supply [3,4]	217 Hz 1 kHz 20 kHz	— — —	75 70 55	— — —	dB dB dB
HSBIAS (Normal Mode, HSBIAS = 2.0-V mode, I_{OUT} = 500 µA) PSRR with 100-mVpp signal AC coupled to VP supply [4]	217 Hz 1 kHz 20 kHz	— — —	75 70 55	— — —	dB dB dB

1. PSRR test configuration: Typical PSRR can vary by approximately 6 dB below the indicated values.



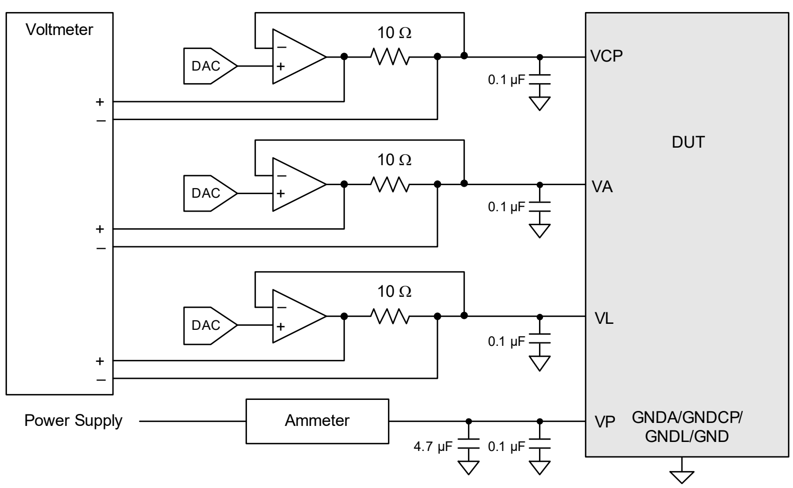
2. No load connected to any analog outputs.
3. The accurate reference, which sets the HSBIAS output voltage, is powered from VA.
4. If HS_CLAMP1/2 are connected to HS3/4, PSRR is reduced by 6 dB.

Table 3-18. Power Consumption

Test conditions (unless specified otherwise): Fig. 2-1 shows CS42L42 connections; GNDA = GNDL = GNDCP = 0 V; voltages are with respect to ground; performance data taken with VA = VCP = VL = 1.8 V; DIGLDO_PDN is deasserted; VP = 3.6 V; T_A = +25°C; ASP_LRCK = 48-kHz Mode; Fs_{INT} = 48 kHz; SCLK = 12 MHz, MCLK_SRC_SEL = 0;mixer attenuation = 0 dB; FULL_SCALE_VOL = 1 (–6 dB) for HPOUTx, TIP_SENSE_CTRL = 11, all other fields are set to defaults; no signal on any input; control port inactive; input clock/data are held low when not required; test load is R_L = 30 Ω and C_L = 1 nF for HPOUTx; measured values include currents consumed by the codec and do not include current delivered to external loads unless specified otherwise (e.g., HPOUTx); see Fig. 3-1.

		Use Cases		Class H Mode	Typical Current (µA)				Total Power (µW)
					i_{VA}	i_{VCP}	i_{VL}	i_{VP}	
1	A	Off [1]		—	0	0	0	3.1	11.16
2	A	Standby [2,3]	Depletion FETs on	—	0	0	0	20	72.0
	B		S0 Detect and tip sense active, Depletion FETs off	—	0	0	0	28	100.8
3	A	Standby (RCO Mode) [4,5]	Depletion FETs on	—	0	0	343	31	729
	B		S0 Detect and tip sense active, Depletion FETs off	—	0	0	343	37	751
4	A	Record		—	1483	0	663	58	4072
5	A	Playback	Stereo HPOUT (no signal, HPOUT_LOAD = 0)	VCP/3	1413	1204	858	58	6464
	B		Stereo HPOUT (0.1 mW, HPOUT_LOAD = 0)	VCP/3	1441	2336	965	58	8744
6	A	S/PDIF Tx (SCLK = 12.288 MHz, 48-kHz data rate, 24-bit, no S/PDIF transmitter load) [6]		—	0	0	418	26	846
7	A	Voice call	Headset (HSIN, HSBIAS_CTRL = 10)	—	3032	1200	1569	270	11414
	B	Voice call (SoundWire)	Headset (HSIN, HSBIAS_CTRL = 10)	—	3032	1200	1815	270	11857

1. Off configuration: Clock/data lines held low; RESET = LOW; VA = VL = VCP = 0 V; VP = 3.6 V.
2. Standby configuration: Clock/data lines held low; VA = VL = VCP = 0 V; VP = 3.6 V; M_MIC_WAKE = 0, M_HP_WAKE = 0 (unmasked).
3. SCLK_PRESENT = 1.
4. SCLK_PRESENT = 0 (RCO clocking).
5. Standby configuration (RCO clocking): Clock/data lines held low; VA = 0 V; VL = 1.8 V, VCP = 0 V, VP = 3.6 V; M_MIC_WAKE = 0, M_HP_WAKE = 0 (unmasked).
6. SCLK = 12.288 MHz, PLL off, SPDIF_CLK_DIV = 001 (divide factor = 2); data lines held low.



Note: The current draw on the VA, VCP, and VL power supply pins is derived from the measured voltage drop across a 10-Ω series resistor between the associated supply source and each voltage supply pin. Given the larger currents that are possible on the VP supply, an ammeter is used for the measurement.

Figure 3-1. Power Consumption Test Configuration

Table 3-19. Register Field Settings

Use Cases		PDN_ALL	ASP_DAO_PDN	ASP_DAI_PDN	ASP_DAI1_PDN	ADC_PDN	MIXER_PDN	EQ_PDN	HP_PDN	SPDIF_TX_PDN	PLL_START	RING_SENSE_PDNB	DETECT_MODE [1]	TIP_SENSE_CTRL [1]	HSBIAS_CTRL [1]	HS_CLAMP_DISABLE	Class H Mode p. 42
1	A	—	—	—	—	—	—	—	—	—	—	—	00	00	01	—	—
2	A	1	—	—	—	—	—	—	—	1	0	—	01	01	10	0	—
	B	1	—	—	—	—	—	—	—	1	0	—	01	01	10	1	—
3	A	1	—	—	—	—	—	—	—	1	0	—	01	01	10	0	—
	B	1	—	—	—	—	—	—	—	1	0	—	01	01	10	1	—
4	A	0	0	1	1	0	1	1	1	1	0	0	00	00	00	0	—
5	A	0	1	0	1	1	0	1	0	1	0	0	01	00	10	1	VCP/3
	B	0	1	0	1	1	0	1	0	1	0	0	01	00	10	1	VCP/3
6	A	0	1	0	1	1	1	1	1	0	0	0	00	00	00	1	—
7	A	Individual power downs. See definitions in Table 3-18.															—

1. LATCH_TO_VP must be set for the following settings to take effect: TIP_SENSE_CTRL, DETECT_MODE, HS_CLAMP_DISABLE, HSBIAS_CTRL.

Table 3-20. S0 Button Detect Characteristics

Test conditions (unless specified otherwise): Fig. 2-1 shows CS42L42 connections; GNDA = GNDL = GNDCP = 0 V; voltages are with respect to ground; parameters can vary with VA and VP; typical performance data taken with VL = VA = 1.8 V, VP = 3.6 V; min/max performance data taken with VA = 1.66–1.94 V, VL = 1.8 V, VP = 3.0–5.25 V; T_A = +25°C.

Parameters		Minimum	Typical	Maximum	Unit
HS DC-detection parameters	Short-detect threshold (S0 button)	100	150	200	mV
	Total group delay	—	5	—	ms
	HS DC detect threshold [1]	—	(M+1) x 1.5625	—	%
	DC level detect power-up time [2]	—	11	—	ms

1. The variable M refers to the decimal representation of the HS_DETECT_LEVEL setting (see p. 152).
2. Time for the DC level detector circuits to completely power up after PDN_MIC_LVL_DETECT transitions from 1 to 0 (see p. 151).

Table 3-21. Switching Specifications—SoundWire Port

Test conditions (unless specified otherwise): GND = 0 V; SWIRE_SEL pin = VL; voltages are with respect to ground; VD_FILT = 1.2 V; VA = 1.8 V; VP = 3.6 V; TA = +25°C; logic 0 = ground, logic 1 = VL; input timings are measured at V_{IL} and V_{IH} thresholds; output timings are measured at V_{OL} and V_{OH} thresholds for VL logic (as shown in Table 3-25).

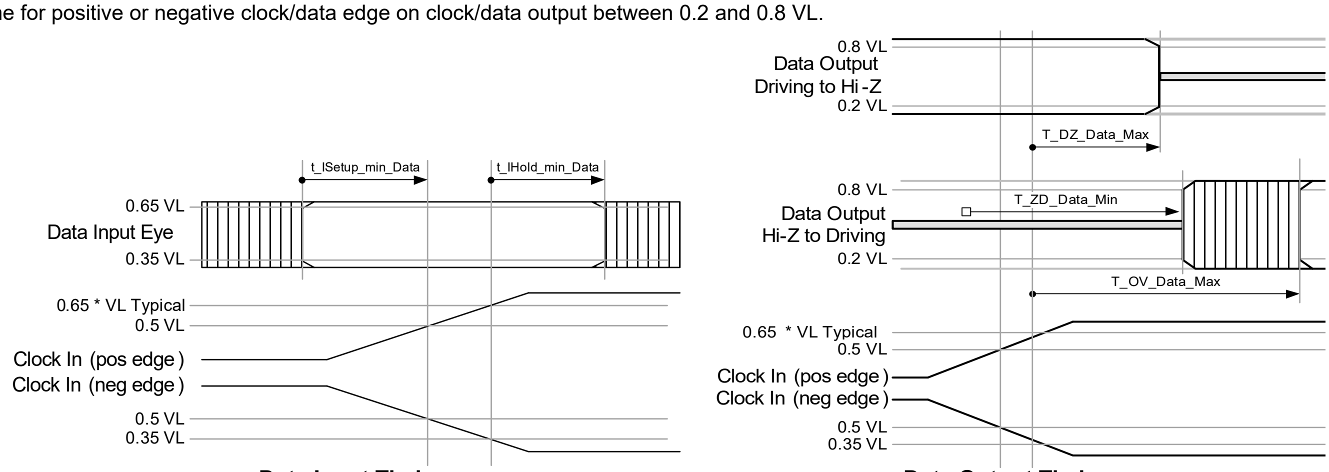
Parameter			Symbol	Minimum	Maximum	Unit
VL = 1.2	SWIRE_CLK frequency	Small data bus (10- to 60-pF capacitance) Large data bus (10- to 100-pF capacitance)	F_{SWSCLK}	— —	12.3 11.0	MHz MHz
	Input clock slew time	Small data bus Large data bus	— —	2.0 2.0	5.0 6.0	ns ns
	Data output slew time [1]		T_{SLEW}	2.0	—	ns
	Data driver disable time [2]		T_{DZ}	—	5.0	ns
	Delay from clock to active state		T_{ZD}	8.1	—	ns
	Time for data output valid	Small data bus (10- to 60-pF capacitance) Large data bus (10- to 100-pF capacitance)	T_{OV_DATA}	— —	27.9 29.0	ns ns
	Data output hold time		T_{OH_DATA}	6.7	—	ns
	Data input minimum setup time [2]		$T_{ISETUP\_MIN\_DATA}$	—	0.0	ns
	Data input minimum hold time		$T_{IHOLD\_MIN\_DATA}$	—	4.0	ns
	Clock input duty cycle		—	45	55	%
	VL logic (SWIRE_CLK and SWIRE_SD pins)	High-level output voltage Low-level output voltage High-level input voltage Low-level input voltage Input voltage threshold (rising edge) Input voltage threshold (falling edge) Hysteresis voltage	V_{OH} V_{OL} V_{IH} V_{IL} V_{TP} V_{TN} V_{HYST}	0.8*VL — 0.65*VL — 0.5*VL 0.35*VL 0.1*VL	— 0.2*VL — 0.35*VL 0.65*VL 0.5*VL —	V V V V V V V

Table 3-21. Switching Specifications—SoundWire Port *(Cont.)*

Test conditions (unless specified otherwise): GND = 0 V; SWIRE_SEL pin = VL; voltages are with respect to ground; VD_FILT = 1.2 V; VA = 1.8 V; VP = 3.6 V; TA = +25°C; logic 0 = ground, logic 1 = VL; input timings are measured at V_{IL} and V_{IH} thresholds; output timings are measured at V_{OL} and V_{OH} thresholds for VL logic (as shown in Table 3-25).

Parameter			Symbol	Minimum	Maximum	Unit
VL = 1.8	SWIRE_CLK frequency	Small data bus (10- to 60-pF capacitance) Large data bus (10- to 100-pF capacitance)	F_{SWSCLK}	— —	12.7 10.1	MHz MHz
	Input clock slew time	Small data bus Large data bus	— —	2.0 2.0	5.4 9.0	ns ns
	Data output slew time [1]		T_{SLEW}	2.0	—	ns
	Data driver disable time [2]		T_{DZ}	—	4.0	ns
	Delay from clock to active state		T_{ZD}	7.9	—	ns
	Time for data output valid	Small data bus (10- to 60-pF capacitance) Large data bus (10- to 100-pF capacitance)	T_{OV_DATA}	— —	27.6 31.6	ns ns
	Data output hold time		T_{OH_DATA}	6.7	—	ns
	Data input minimum setup time [2]		$T_{ISETUP\_MIN\_DATA}$	—	0.0	ns
	Data input minimum hold time		$T_{IHOLD\_MIN\_DATA}$	—	4.0	ns
	Clock input duty cycle		—	45	55	%
	VL logic (SWIRE_CLK and SWIRE_SD pins)	High-level output voltage Low-level output voltage High-level input voltage Low-level input voltage Input voltage threshold (rising edge) Input voltage threshold (falling edge) Hysteresis voltage	V_{OH} V_{OL} V_{IH} V_{IL} V_{TP} V_{TN} V_{HYST}	0.8*VL — 0.65*VL — 0.5*VL 0.35*VL 0.1*VL	— 0.2*VL — 0.35*VL 0.65*VL 0.5*VL —	V V V V V V V

1. Slew time for positive or negative clock/data edge on clock/data output between 0.2 and 0.8 VL.
2. Data timing



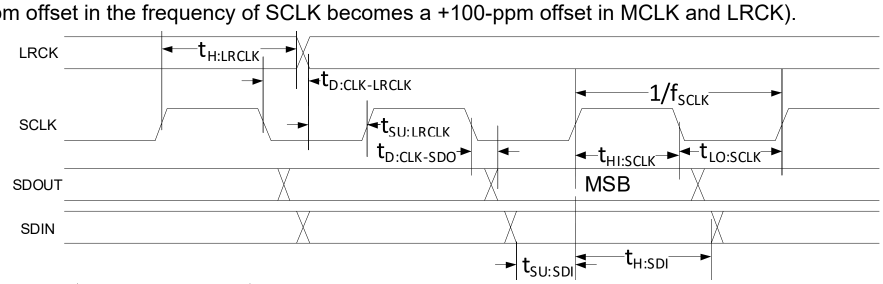
Data Input Timing **Data Output Timing**

Table 3-22. Digital Audio Interface Timing Characteristics

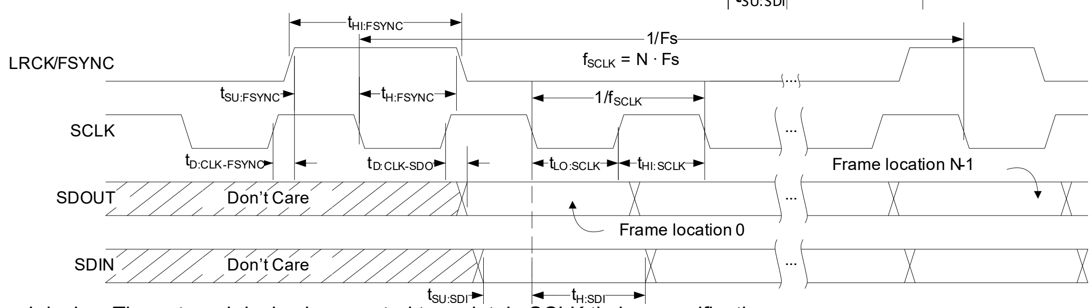
Test conditions (unless specified otherwise): GNDA = GNDL = GNDCP = 0 V; all voltages with respect to ground; values are for both VL = 1.2 and 1.8 V; inputs: Logic 0 = GNDL = 0 V, Logic 1 = VL; T_A = +25°C; C_{LOAD} = 30 pF (for VL = 1.2 V) and 60 pF (for VL = 1.8 V); input timings are measured at V_{IL} and V_{IH} thresholds; output timings are measured at V_{OL} and V_{OH} thresholds (see Table 3-25); ASP_TX_HIZ_DLY = 00.

Parameters [1,2,3]			Symbol	Minimum	Typical	Maximum	Unit
ASP_SCLK frequency [4]			f_{SCLK}	0.973 [5]	—	25.81	MHz
SCLK high period [4]			$t_{HI:SCLK}$	18.5	—	—	ns
SCLK low period [4]			$t_{LO:SCLK}$	18.5	—	—	ns
SCLK duty cycle [4]			—	45	—	55	%
Hybrid-Master Mode	FSYNC/LRCK frame rate		—	0.99	—	1.01	Fs
	LRCK duty cycle		—	45	—	55	%
	FSYNC high period [6]		$t_{HI:FSYNC}$	$1/f_{SCLK}$	—	$(n–1)/f_{SCLK}$	s
	FSYNC/LRCK delay time after SCLK launching edge [7]	VL = 1.8 V	$t_{D:CLK–LRCK}$	0	—	15	ns
		VL = 1.2 V		0	—	17	ns
	SDIN setup time before SCLK latching edge [7]		$t_{SU:SDI}$	10	—	—	ns
	SDIN hold time after SCLK latching edge [7]		$t_{H:SDI}$	5	—	—	ns
	SDOUT delay time after SCLK launching edge	VL = 1.8 V	$t_{D:CLK–SDO}$	0	—	15	ns
		VL = 1.2 V		0	—	17	ns
	SDOUT Hi-Z delay time after SCLK latching edge (TDM; ASP_TX_HIZ_DLY = 00) [8,9]		$t_{DLY:HiZ}$	—	—	22	ns
Slave Mode	FSYNC/LRCK frame rate		—	0.99	—	1.01	Fs
	FSYNC/LRCK duty cycle		—	45	—	55	%
	FSYNC/LRCK setup time before SCLK latching edge [7]		$t_{SU:LRCK}$	10	—	—	ns
	FSYNC/LRCK hold time after SCLK latching edge [7]		$t_{H:LRCK}$	5	—	—	ns
	SDIN hold time after SCLK latching edge [7]		$t_{H:SDI}$	5	—	—	ns
	FSYNC/LRCK duty cycle		—	45	—	55	%
	SDOUT delay time after SCLK launching edge	VL = 1.8 V	$t_{D:CLK–SDO}$	0	—	15	ns
		VL = 1.2 V		0	—	17	ns
	SDOUT Hi-Z delay time after SCLK latching edge (ASP_TX_HIZ_DLY = 00) [8,9]		$t_{DLY:HiZ}$	—	—	22	ns

1. Output clock frequencies follow SCLK frequency proportionally. Deviation of the bit-clock source from nominal supported rates is directly imparted to the output clock rate by the same factor (e.g., +100-ppm offset in the frequency of SCLK becomes a +100-ppm offset in MCLK and LRCK).
2. I²S interface timing



3. TDM interface timing



4. SCLK is mastered from an external device. The external device is expected to maintain SCLK timing specifications.
5. SCLK operation below 2.8224 MHz may result in degraded performance.
6. Maximum LRCK duty cycle is equal to frame length, in SCLK periods, minus 1. Maximum duty cycle occurs when LRCK_HI is set to 511 SCLK periods and LRCK period is set to 512 SCLK periods.
7. Data is latched on the rising or falling edge of SCLK, as determined by ASP_SCPOL_IN_x and ASP_FSD (See Section 7.5.7 and Section 7.5.8).
8. Data may be latched on either the rising or falling edge of SCLK.
9. TDM interface Hi-Z timing

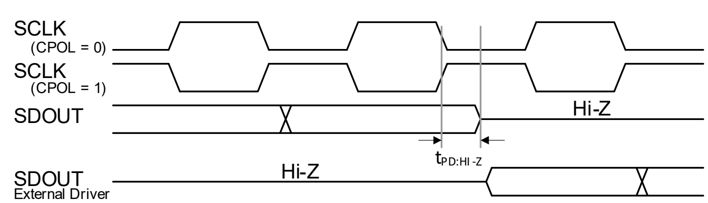


Table 3-23. Switching Characteristics—S/PDIF Transmitter

Test conditions (unless specified otherwise): Outputs: Logic 0 = 0 V, Logic 1 = VL = 1.8 V; C_L = 60 pF.

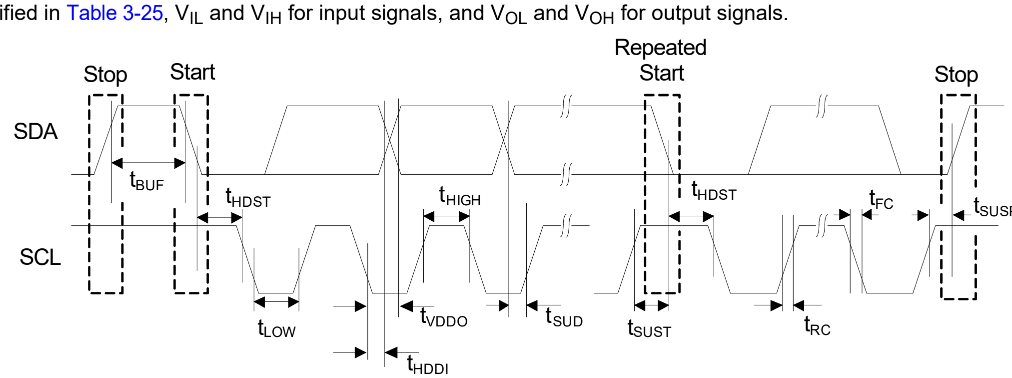
Parameter	Minimum	Typical	Maximum	Unit
Frame rate	32	—	192	kHz
S/PDIF transmitter output time-interval error (TIE) jitter	—	500	—	ps RMS

Table 3-24. I²C Slave Port Characteristics

Test conditions (unless specified otherwise): Fig. 2-1 shows typical connections; Inputs: GNDA = GNDL = GNDCP = 0 V; all voltages with respect to ground; min/max performance data taken with VL = 1.66–1.94 V (VL_SEL = VP) or VL = 1.1–1.3 V (VL_SEL = GNDD); inputs: Logic 0 = GNDA = 0 V, Logic 1 = VL; T_A = +25°C; SDA load capacitance equal to maximum value of C_B = 400 pF; minimum SDA pull-up resistance, $R_{P(min)}$.[1] Table 3-1 describes some parameters in detail. All specifications are valid for the signals at the pins of the CS42L42 with the specified load capacitance.

Parameter [2]		Symbol [3]	Minimum	Maximum	Unit
SCL clock frequency		f_{SCL}	—	1000	kHz
Clock low time		t_{LOW}	500	—	ns
Clock high time		t_{HIGH}	260	—	ns
Start condition hold time (before first clock pulse)		t_{HDST}	260	—	ns
Setup time for repeated start		t_{SUST}	260	—	ns
Rise time of SCL and SDA	Standard Mode Fast Mode Fast Mode Plus	t_{RC}	— — —	1000 300 120	ns ns ns
Fall time of SCL and SDA	Standard Mode Fast Mode Fast Mode Plus	t_{FC}	— — —	300 300 120	ns ns ns
Setup time for stop condition		t_{SUSP}	260	—	ns
SDA setup time to SCL rising		t_{SUD}	50	—	ns
SDA input hold time from SCL falling [4]		t_{HDDI}	0	—	ns
Output data valid (Data/Ack) [5]	Standard Mode Fast Mode Fast Mode Plus	t_{VDDO}	— — —	3450 900 450	ns ns ns
Bus free time between transmissions		t_{BUF}	500	—	ns
SDA bus capacitance	Fast Mode Plus Standard Mode, Fast Mode	C_B	— —	550 400	pF pF
SCL/SDA pull-up resistance [1]	VL = 1.2 V VL = 1.8 V	R_P	200 250	— —	Ω Ω
Switching time between RCO and PLL or SCLK [6]		—	150	—	µs

1. The minimum R_P value (see Fig. 2-1) is determined by using the maximum VL level, the minimum sink current strength of its respective output, and the maximum low-level output voltage, V_{OL}. The maximum R_P value may be determined by how fast its associated signal must transition (e.g., the lower the R_P value, the faster the I²C bus can operate for a given bus load capacitance). See the I²C bus specification referenced in Section 13.
2. All timing is relative to thresholds specified in Table 3-25, V_{IL} and V_{IH} for input signals, and V_{OL} and V_{OH} for output signals.
3. I²C control-port timing



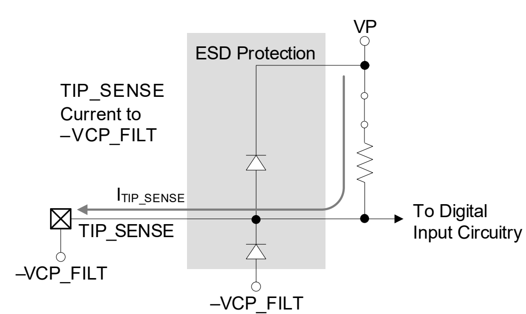
4. Data must be held long enough to bridge the SCL transition time, t_F.
5. Time from falling edge of SCL until data output is valid.
6. The switch between RCO and either SCLK or PLL occurs upon setting/clearing SCLK_PRESENT (see p. 134) and sending the I²C stop condition. An SCLK_PRESENT transition (0 to 1 or 1 to 0) starts a switch between RCO and the selected SCLK or PLL. An I²C stop condition is sent, after which a wait time of at least 150 µs is required before the next I²C transaction can begin using the newly selected clock.

Table 3-25. Digital Interface Specifications and Characteristics

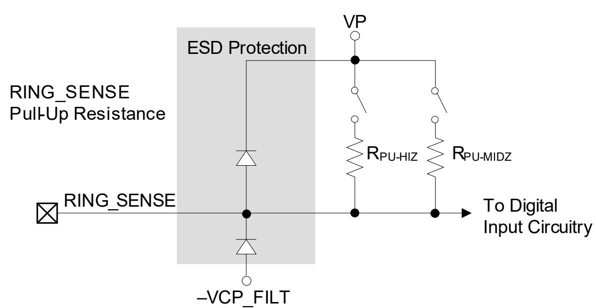
Test conditions (unless specified otherwise): Fig. 2-1 shows CS42L42 connections; GNDD = GNDCP = GNDA = 0 V; voltages are with respect to ground; parameters can vary with VL and VP; min/max performance data taken with VCP = VA = 1.8 V, VD_FILT = 1.2 V; VP = 3.0–5.25 V; VL = 1.66–1.94 V (VL_SEL = VP) or VL = 1.1–1.3 V (VL_SEL = GNDD); T_A = +25°C; C_L = 60 pF.

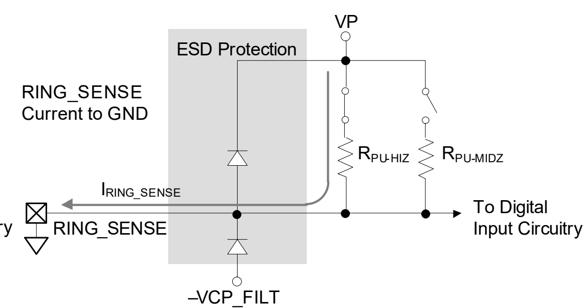
Parameters [1]		Symbol	Min	Max	Unit
Input leakage current [2,3]	ASP_SDOUT, ASP_LRCK/FSYNC	I_{in}	—	±4	µA
	ASP_SCLK/SWIRE_CLK, SWIRE_SD/ASP_SDIN		—	±3	µA
	RING_SENSE, TIP_SENSE		—	±100	nA
	SDA, SCL		—	±100	nA
	$\overline{\text{INT}}$, $\overline{\text{WAKE}}$, $\overline{\text{RESET}}$		—	±100	nA
Input leakage current (SoundWire) [2,3]	Supplies as stipulated above	I_{in}	—	±3	µA
ASP_SCLK/SWIRE_CLK and SWIRE_SD/ASP_SDIN only	VD_FILT = 0 V (VL is as stated above)		—	±3	µA
	VL = 0 V		—	[4]	mA
Internal weak pull-down		—	550	2450	kΩ
Input capacitance [2]		—	—	10	pF
$\overline{\text{INT}}$ or $\overline{\text{WAKE}}$ current sink (V_{OL} = 0.3 V maximum)		—	825	—	µA
VL Logic (non-I²C, including SPDIF_TX)	High-level output voltage (I_{OH} = –100 µA)	V_{OH}	0.9*VL	—	V
	Low-level output voltage	V_{OL}	—	0.1*VL	V
	High-level input voltage	V_{IH}	0.7*VL	—	V
	Low-level input voltage	V_{IL}	—	0.3*VL	V
VL Logic (I²C only)	Low-level output voltage	V_{OL}	—	0.2*VL	V
	High-level input voltage	V_{IH}	0.7*VL	—	V
	Low-level input voltage	V_{IL}	—	0.3*VL	V
	Hysteresis voltage	V_{HYS}	0.05*VL	—	V
VP Logic (excluding TIP_SENSE)	Low-level output voltage	V_{OL}	—	0.2	V
	High-level input voltage	V_{IH}	0.9	—	V
	Low-level input voltage	V_{IL}	—	0.2	V
TIP_SENSE [5]	High-level input voltage	V_{IH}	0.87*VP	—	V
	Low-level input voltage	V_{IL}	—	2.0	V
RING_SENSE [6]	RS_TRIM_T = 0, High-level input voltage	V_{IH}	0.15*VP	—	V
	Low-level input voltage	V_{IL}	—	0.03*VP	V
	RS_TRIM_T = 1, High-level input voltage	V_{IH}	0.40*VP	—	V
	Low-level input voltage	V_{IL}	—	0.28*VP	V
RING_SENSE pull-up resistance	RING_SENSE_PU_HIZ = 1, RS_TRIM_R = 0; R_{PU} to Hi-Z	R_{PU}-Hi-Z	1.688	2.813	MΩ
	RING_SENSE_PU_HIZ = 0; R_{PU} to Mid-Z	R_{PU}-MIDZ	12.15	20.25	kΩ
TIP_SENSE current to –VCP_FILT [5]	TIP_SENSE_CTRL = 11 (Short-Detect Mode)	I_{TIP_SENSE}	1.00	2.91	µA
RING_SENSE current to GND [6]	RS_TRIM_R = 0 (Hi-Z Mode)	I_{RING_SENSE}	1.00	3.2	µA

1. See Table 1-1 for serial and control-port power rails.
2. Specification is per pin. The CS42L42 is not a low-leakage device, per the *MIPI Specification*. See Section 13.
3. Includes current through internal pull-up or pull-down resistors on pin.
4. If VL = 0 V, the current must not exceed the values provided in Table 3-3.
5. TIP_SENSE input circuit. This circuit allows the TIP_SENSE signal to go as low as –VCP_FILT and as high as VP. Section 4.14.2 provides configuration details.



6. RING_SENSE input circuit. This circuit allows the RING_SENSE signal to range between –VCP_FILT and VP.





4 Functional Description

This section provides a general description of the CS42L42 architecture and detailed functional descriptions of the various blocks that make up the CS42L42. Fig. 4-1 shows the flow of signals through the CS42L42 and gives links to detailed descriptions of the respective sections.

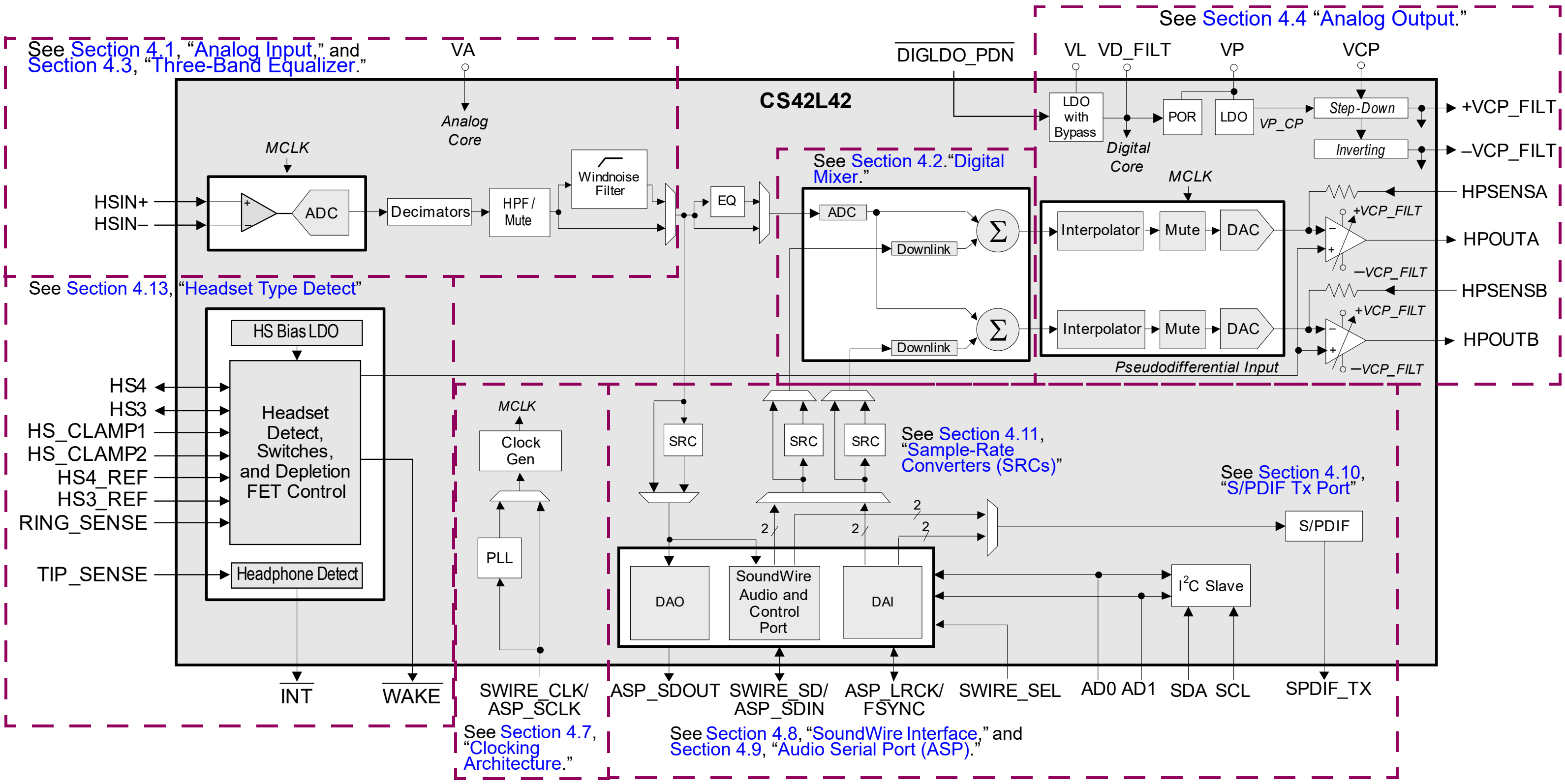


Figure 4-1. Overview of Signal Flow

The CS42L42 is an ultralow-power, 24-bit audio codec, with a single analog input ADC channel and a stereo DAC. The ADC is fed by fully differential or pseudodifferential analog input that support mic and line-level input signals. The DAC feeds a stereo pseudodifferential output amplifier. The converters operate at a low oversampling ratio, maximizing power savings while maintaining high performance.

The serial data interface ports operate either at standard audio-sample rates as timing slaves or in Hybrid-Master Mode as a bit-clock slave generating LRCK internally. An onboard fractional-N PLL can be used to generate the internal-core timing ($MCLK_{INT}$) if the SCLK source is not one of the following rates (where N = 2 or 4):

- N x 5.6448 or 6.1440 MHz
- USB rates (N x 6 MHz)

The CS42L42 significantly reduces overall power consumption, with a very low-voltage digital core and with low-voltage Class H amplifiers (powered from an integrated LDO regulator and a step-down/inverting charge pump, respectively). The CS42L42 comprises the following subblocks:

- Analog input. The analog input block, described in Section 4.1, allows selection from mono line-level or mic sources. The pseudodifferential line-input configuration provides noise rejection for single-ended analog CS42L42 inputs. Mic input supports fully differential sources and can operate with single-ended sources in a pseudodifferential configuration. Analog input requires no external DC-blocking capacitors.
- Digital mixer. The digital mixer, described in Section 4.2, facilitates the mixing and routing of the ADC and serial port audio data to the device analog. All paths have selectable attenuation before being mixed to allow relative volume control and to avoid clipping.
- Equalizer. A bypassable, three-band equalizer, described in Section 4.3, is available to process signals within the CS42L42. Each of the three fully programmable filter banks can be configured independently.

- Analog outputs. The analog output block, described in Section 4.4, includes separate pseudodifferential headphone Class H amplifiers. An on-chip step-down/inverting charge pump creates a positive and negative voltage equal to the input or to either one-half or one-third of the input supply for the amplifiers, allowing an adaptable, full-scale output swing centered around ground. The resulting internal amplifier supply can be ±VCP/3, ±VCP/2, ±VCP, or ±2.5 V.

  The inverting architecture eliminates the need for large DC-blocking capacitors and allows the amplifier to deliver more power to HP loads at lower supply voltages. The step-down architecture allows the amplifier's power supply to adapt to the required output signal. This adaptive power-supply scheme converts traditional Class AB amplifiers into more power-efficient Class H amplifiers.
- Class H amplifier. The HP output amplifiers, described in Section 4.6, use a patented Cirrus Logic four-mode Class H technology that maintains high performance and maximizes operating efficiency of a typical Class AB amplifier.
- Clocking architecture. Described in Section 4.7, the clock for the device can be supplied internally from an integrated fractional-N PLL using ASP_SCLK/SWIRE_CLK as the source clock or the internal PLL can be bypassed and derived directly from the ASP_SCLK/SWIRE_CLK input pin.
- MIPI-compliant two-wire SoundWire interface. The CS42L42 integrates a SoundWire interface to transport audio and control data, which provides an alternative to the I²C/ASP interfaces. See Section 4.8.
- Serial ports. The CS42L42 has two serial data-port options: The TDM/I²S (ASP) port is a highly configurable serial port; the MIPI-compliant SoundWire serial port can be selected to communicate audio and voice data to and from other devices in the system, such as application processors and Bluetooth® transceivers. See Section 4.9.

  The ASP can operate in TDM Mode, which includes full-duplex communication, defeatable SDOUT driver for sharing the TDM bus between multiple devices, flexible data structuring via control port registers, clock slave mode, and higher bandwidth, enabling more data to be transferred to and from the device.
- S/PDIF Tx Port. The S/PDIF output port, described in Section 4.10, is integrated to provide a pass-through of encoded (e.g., AC3) or PCM data from the serial audio ports to an external optical driver.
- Sample-rate converters (SRCs). SRCs, described in Section 4.11, are used to bridge different sample rates at the serial ports within the digital-processing core. SRCs are used for the ASP output channel, and both ASP input channels, the SoundWire output channel and both SoundWire input channels. SRCs can be bypassed. Note that the S/PDIF channels do not have SRCs in their paths.
- Headset interface. This interface is described in Section 4.12. It is a collection of low-power circuits that provide an intelligent interface to an external headset. It also communicates with an applications processor to relay command and status information. Headset-type detection is described in Section 4.13.
- The CS42L42 supports plug presence-detect capability via the two associated sense pins: TIP_SENSE and RING_SENSE. The sense pins are debounced to filter out brief events before being reported to the corresponding presence detect bit and generating an interrupt if appropriate. Plug presence detection is described in Section 4.14.
- Power management. Several control registers provide independent power-down control of the analog and digital sections of the CS42L42, allowing operation in select applications with minimal power consumption. Power management considerations are described in Section 4.15.
- Control-port operation. The control port, described in Section 4.16, provides access to the registers for configuring the codec. The control port operation may be completely asynchronous with respect to the audio sample rates. To avoid potential interference problems, control-port data pins must remain static if no operation is required.
- Resets. Section 4.17 describes the reset options—power-on reset (POR), asserting $\overline{\text{RESET}}$, and the SoundWire reset mechanism.
- Interrupts. The CS42L42 includes an open-drain interrupt output, $\overline{\text{INT}}$. Interrupt mask registers control whether an event associated with an interrupt status/mask bit pair triggers the assertion of $\overline{\text{INT}}$.A set of SoundWire interrupts is provided that is separate from the general interrupt implementation. See Section 4.18.

4.1 Analog Input

The CS42L42 analog (line in/mic) input is fed to a high-dynamic range ADC path, shown in Fig. 4-2.

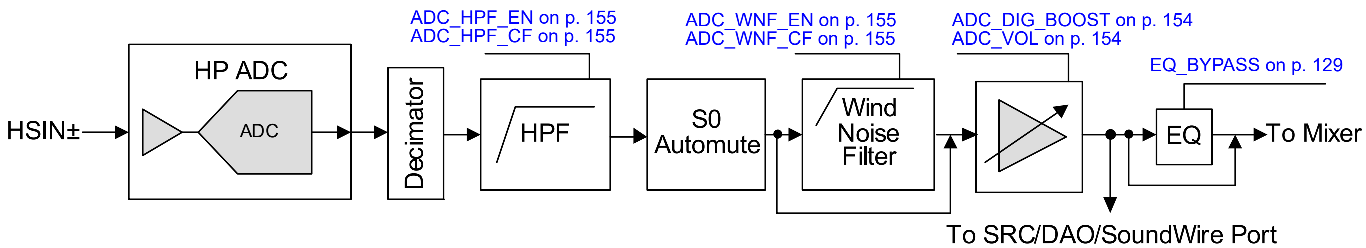


Figure 4-2. Analog-Input Signal Flow

The CS42L42 provides a mono, high-performance capture path, directly sourced from HSIN±. To optimize the path's dynamic range and power consumption, the ADC uses analog and DSP techniques to automatically adapt to input signal content. During normal operation, the high-performance ADC path channel selects either a high-input amplitude path or low-noise path. With this functionality, the path's dynamic range can be optimized without the power consumption of a single, high-amplitude, low-noise ADC path.

The ADC HSIN inputs supports fully differential, pseudodifferential, and single-ended configurations (see Fig. 4-3). Although the best performance is typically achieved with a fully differential signal input, the pseudodifferential configuration is recommended over a traditional single-ended input configuration when possible (see Fig. 4-2). This is due to cancelation of common-mode signals or noise that may appear on the signal.

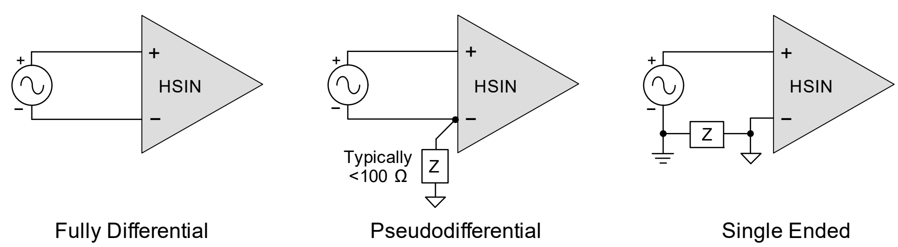


Figure 4-3. Analog Input Configurations

4.1.1 ADC High-Pass Filter

The ADC path, shown in Fig. 4-2, includes a defeatable, first-order digital high-pass filter, enabled by setting ADC_HPF_EN (see p. 155). Clearing this bit may cause clipping of the ADC digital output. ADC_HPF_CF (see p. 155) is used to configure the corner frequency. Table 3-6 lists high-pass filter specifications.

4.1.2 ADC Wind-Noise Filter

The defeatable, bypassable, fourth-order digital high-pass filter is enabled by ADC_WNF_EN (see p. 155). Its configurable corner frequency is controlled by ADC_WNF_CF (see p. 155). Table 3-11 lists wind-noise filter specifications.

4.1.3 ADC Gain Control

In traditional ADC designs, selectable gain stages or fixed-gain preamps (PGAs) commonly precede the ADC inputs. Although these offer flexibility, they are a result of ADC input limitations. If a gain is selected too high, clipping may occur in the ADC on loud passages. If the gain is too low to avoid clipping, sounds may be too low and SNR may suffer.

The CS42L42 ADC path achieves very high dynamic range with a very low noise floor with minimal power. Using patent-pending circuitry that simplifies the ADC input-path configuration, the ADC fundamentally captures the entire sound signal. The resulting SNR is typically much higher than legacy systems, without potential clipping.

The CS42L42 incorporates digital-gain capability that allows the SNR to remain constant as compared to analog gain adjustments in legacy systems. Enabling ADC_DIG_BOOST (see p. 154) adds a +20-dB digital gain to the ADC output. Additionally, the ADC_VOL control (see p. 154) allows for volume control range from +12 to –96 dB, or mute.

4.1.4 Soft Ramping Control

If ADC_SOFTRAMP_EN (see p. 154) is set, changes to ADC digital volumes are applied slowly by stepping through each volume-control setting with a delay between steps equal to an integer number of Fs periods. The delay between steps can vary from 1/Fs period to 72/Fs periods and is set via DSR_RATE (see p. 130).

4.2 Digital Mixer

The internal stereo digital mixer, shown in Fig. 4-4, can mix the ADC path output with Channel A and B from the serial port inputs. Each input can be attenuated via MIXER_CHx_VOLy. Outputs are available as a source for the DACs.

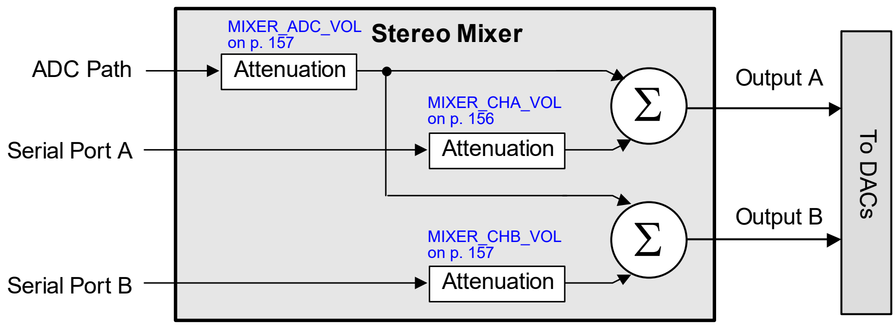


Figure 4-4. Digital Mixer Subblocks

Note: When mixing channels, to ensure that all paths are defined and known, select only active channels. Selecting a powered-down channel may cause undesirable behavior, such as clipping or high distortion.

4.2.1 Avoiding Mixer Clipping

Because digital mixers are essentially adders, when more than one input is fed into a mixer, a potential for overflow exists, depending on the bit-word length of the inputs and the mixer and the input value range used. For example, if two, full-range, signed, 4-bit channels yield a signed 4-bit result, whenever the sum of the two inputs falls outside the –8 to +7 range, the hypothetical result would overflow, causing undesired output signal distortion (i.e., wrapping).

All mixers have enough accumulator bits to avoid overflow. If any mixer's result exceeds the bit width of the signal data path, the result is forced to either the full-scale maximum or minimum value. This ensures that the signal is clipped rather than distorted (by the wrapping effect of truncating the accumulator result to fit the data path width). Attention is required to ensure that clipping does not occur within the digital mixer control. Of course, if the digital mixer control is fed a signal that was clipped elsewhere, its output retains that external clipping.

Table 4-1 lists the recommended maximum premixer volume level settings to avoiding mixer clipping.

Table 4-1. Recommended Premixer Attenuation to Avoid Clipping

Number of Active Channels into Mixer	Maximum Signal Strength Allowed per Input	Suggested Volume (dB) Setting per Input
1	1	0
2	1/2	–6

For Table 4-1, it is assumed that all inputs are at full scale (no preattenuation) and that there is no relative volume adjustment between inputs. If one or more inputs is at less than full scale, less attenuation (a higher volume) can be set while avoiding mixer clipping. If there is to be a relative volume adjustment between inputs, less attenuation can be set for one or more inputs as long as any other inputs are sufficiently attenuated to avoid clipping (e.g., with three full-scale inputs, one input could be attenuated by 6 dB, as long as the other two are attenuated by 12 dB).

Note: As noted elsewhere, to avoid clipping, select only active channels when mixing channels.

4.2.2 Mixer Attenuation Values

The digital mixer contains programmable attenuation blocks that are configured as described in the MIXER_CHx_VOLy field descriptions in Section 7.15.1—Section 7.15.3. For all settings except 0 dB, attenuation on the mixer input includes an offset that increases as attenuation increases, as follows:

- For commonly used –6*n* dB ($n = \{1, 2, \text{etc.}\}$) attenuation settings, the offset rounds the attenuation exactly to the desired $1/2^n$ factor (e.g., 20Log(1/2) = 6.021 dB, not 6.000 dB).
- For attenuation settings other than –6*n* dB, the always positive offset provides slightly more attenuation, giving enough margin to avoid mixer clipping.

4.3 Three-Band Equalizer

The mono equalizer connects as shown in Fig. 4-5. The equalizer input enters three fully programmable parametric filter banks that can be independently configured in any of the following: low-pass filter (LPF), high-pass filter (HPF), all-pass filter (APF), band-pass filter (BPF), notch filter (NF), peaking EQ (PEQ), low-shelving EQ (LSEQ), or high-shelving EQ (HSEQ).

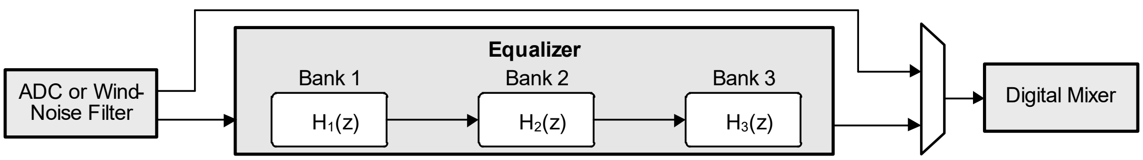


Figure 4-5. Three-Band Equalizer

The three filter banks are cascaded, such that the Filter Bank 1 output is the input to Filter Bank 2, and so on. Therefore, the overall transfer function is the product of the three functions: $H_1(z) \bullet H_2(z) \bullet H_3(z)$, as shown in Fig. 4-5. Each bank is implemented as Direct Form II transposed, as shown in Fig. 4-6.

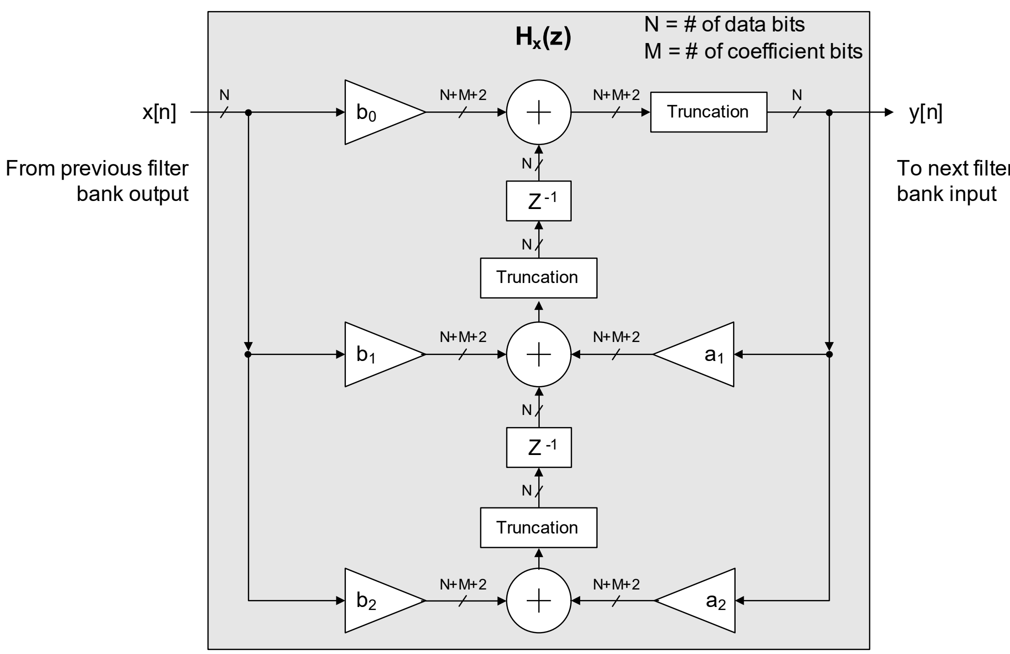


Figure 4-6. Direct Form II Transposed Filter Bank Architecture

Eq. 4-1 represents the filter bank architecture, where y[n] represents the output sample value and x[n] represents the input sample value.

$$y[n] = b_0x[n] + b_1x[n-1] + b_2x[n-2] + a_1y[n-1] + a_2y$$

Equation 4-1. Filter Equation

Note: If the conventional difference equation is used to calculate coefficients, coefficients a1 and a2 must be inverted before writing them.

To avoid audible distortion when inputs to the equalizer are extremely large, the gain must be limited to 0 dB for each filter stage and all B coefficients must be between ±1.0.

As Table 4-2 shows, coefficients are represented in binary by 32-bit signed values stored in S1.30 two's complement format. The 2 MSBs represent the sign bit and whole-number portion of the decimal coefficient. The 30 LSBs represent the fractional portion of the coefficient. Coefficients must be in the range of –2.00000 to 1.999999999 (0x8000 0000–0x7FFF FFFF).

Table 4-2. Equalizer Filter Formatting (Fs_{INT} = 48 kHz)

Precision of Coefficients	Order of Filter	Sample Rate	Coefficient Design Base	Length (in Bytes)
S1.30	3 biquads	Fs_{INT}	z^{-1} (For z^{-1}, design the coefficients at the rate of the filter.)	60

Section 7.16 describes three-band equalizer registers. All coefficients are configured as pass-through at power-up.

Note: Filters are read and written by using EQ_COEF_OUT and EQ_COEF_IN (see p. 157). However, they must be accessed only as part of a full-filter access procedure; otherwise, the three-band filter may be corrupted and audio artifacts may occur.

Use Ex. 4-1 to write EQ filter coefficients.

Example 4-1. Writing the EQ Filter Coefficients

Step	Task	Register/Bit Fields	Value	Description
1	Ensure EQ initialization is complete (EQ_INIT_DONE = 1). **Note:** polling EQ_INIT_DONE is valid only if EQ PDN = 0 (EQ is powered up.)	Equalizer Initialization Status	0x01	
		Reserved	0000 000	—
		EQ_INIT_DONE	1	EQ initialization complete.
2	Clear the equalizer start filter bit to allow writing coefficients.	Equalizer Start Filter Control	0x00	
		Reserved	0000 000	—
		EQ_START_FILTER	0	Coefficients can be read or written
3	Disable the EQ bypass.	Serial Port SRC Control	0x00	
		Reserved	000	—
		EQ_BYPASS	0	No bypass
		I2C_DRIVE	0	Normal
		ASP_DRIVE	0	Normal
		SRC_BYPASS_DAC	0	No bypass
		SRC_BYPASS_ADC	0	No bypass
4	Mute the EQ input path.	Equalizer Input Mute Control	0x01	
		Reserved	0000 000	—
		EQ_MUTE	1	Mute EQ Channel input.
5	Set the EQ write enable bit.	Equalizer Filter Coefficient Read/Write	0x02	
		Reserved	0000 00	—
		EQ_WRITE	1	Enable EQ write.
		EQ_READ	0	Disable EQ read.
6	Write input coefficients. There are 15 32-bit coefficients and four 8-bit registers, so 60 register writes are required. The biquad order is as follows: 1, 2, 3 The coefficient order is as follows: b0, b1, a1, a2, b2 The sequence shown in Steps 6.1 through 6.4 writes a single coefficient for a single biquad: This process is repeated 15 times. The order of coefficients is as follows: Biquad 1, b0 Biquad 1, b1 Biquad 1, a1 … Biquad 3, b2			
6.1	Write EQ_COEF_IN[7:0] (0x2401)	Equalizer Filter Coefficient Input 0–3	0xXX	
		EQ_COEF_IN[7:0]		Coefficient write
6.2	Write EQ_COEF_IN[15:8] (0x2402)	Equalizer Filter Coefficient Input 0–3	0xXX	
		EQ_COEF_IN[15:8]		Coefficient write
6.3	Write EQ_COEF_IN[23:16] (0x2403)	Equalizer Filter Coefficient Input 0–3	0xXX	
		EQ_COEF_IN[23:16]		Coefficient write
6.4	Write EQ_COEF_IN[31:24] (0x2404, see note below)	Equalizer Filter Coefficient Input 0–3	0xXX	
		EQ_COEF_IN[31:24]		Coefficient write

Example 4-1. Writing the EQ Filter Coefficients *(Cont.)*

Step	Task	Register/Bit Fields	Value	Description
7	Clear the EQ write enable bit.	Equalizer Filter Coefficient Read/Write	0x00	
		Reserved EQ_WRITE EQ_READ	0000 00 0 0	— Disable EQ write. Disable EQ read.
8	Set the EQ filter start bit.	Equalizer Start Filter Control	0x01	
		Reserved EQ_START_FILTER	0000 000 1	— Start EQ filter.
9	Unmute the EQ input path.	Equalizer Input Mute Control	0x00	
		Reserved EQ_MUTE	0000 000 0	— Unmute EQ Channel input.

Use Ex. 4-2 to read EQ filter coefficients. Read the coefficients only as soon as they are written (e.g., before setting EQ_START_FILTER in Step 8 in Ex. 4-1).

Notes: If EQ_START_FILTER is cleared after reading the coefficients, the b0 coefficients are set to +1.0 and the remaining coefficients are cleared. Setting the EQ_START_FILTER back to 1 does not restore the coefficients. A complete rewrite must be performed.

Writing EQ_COEF_IN[31:24] stretches the clock unless (EQ_PDN==0 && (EQ_READ==1 XOR EQ_WRITE==1))

Reading EQ_COEF_OUT[7:0] stretches the clock unless (EQ_PDN==0 && (EQ_READ==1 XOR EQ_WRITE==1))

If SoundWire is used to read the EQ coefficients, indirect access is preferred. See Section 4.8.12.

Example 4-2. Reading the EQ Filter Coefficients

Step	Task	Register/Bit Fields	Value	Description
1	Set the EQ read enable bit.	Equalizer Filter Coefficient Read/Write	0x01	
		Reserved EQ_WRITE EQ_READ	0000 00 0 1	— Disable EQ write Enable EQ read
2	Read output coefficients			
2.1	Read EQ_COEF_OUT[7:0] (0x2407, see note above)	Equalizer Filter Coefficient Output 0–3	0xXX	
		EQ_COEF_OUT[7:0]		Coefficient read from EQ
2.2	Read EQ_COEF_OUT[15:8] (0x2408)	Equalizer Filter Coefficient Output 0–3	0xXX	
		EQ_COEF_OUT[15:8]		Coefficient read from EQ
2.3	Read EQ_COEF_OUT[23:16] (0x2409)	Equalizer Filter Coefficient Output 0–3	0xXX	
		EQ_COEF_OUT[23:16]		Coefficient read from EQ
2.4	Read EQ_COEF_OUT[31:24] (0x240A)	Equalizer Filter Coefficient Output 0–3	0xXX	
		EQ_COEF_OUT[31:24]		Coefficient read from EQ
3	Clear the EQ read enable bit.	Equalizer Filter Coefficient Read/Write	0x00	
		Reserved EQ_WRITE EQ_READ	0000 00 0 0	— Disable EQ write. Disable EQ read.

4.4 Analog Output

This section describes the headphone (HP) outputs. The CS42L42 provides an analog output that is fed from the mixer. Fig. 4-7 shows the general flow of the analog outputs.

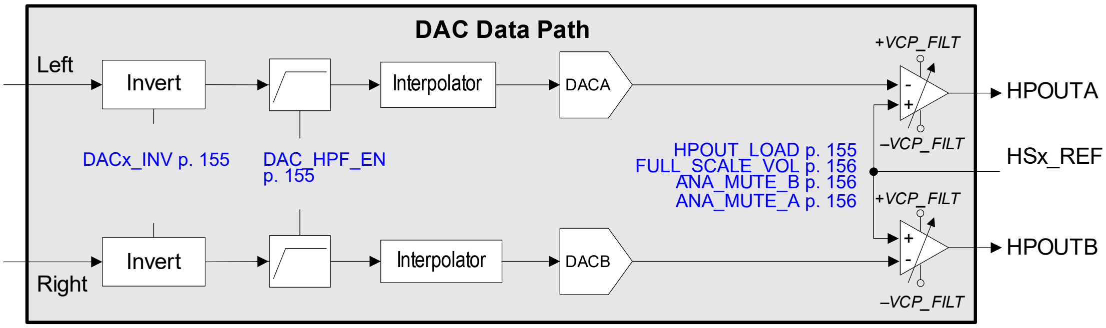


Figure 4-7. Analog-Output Signal Flow

The output path is sourced directly from the mixer output. The playback path uses advanced analog and digital signal-processing techniques to adapt to the input signal content and enhance dynamic range and power consumption of the playback path. The HP output must be muted before changing the state of FULL_SCALE_VOL (see p. 156), which sets the maximum HPOUT output voltage. See Table 3-13. HP outputs are muted by ANA_MUTE_B and ANA_MUTE_A (see p. 156).

Fig. 4-8 shows analog output flow details. Power to DACs is controlled by the related output drivers' PDN bits.

See Section 4.2 for details on DAC source selection.

Figure 4-8. Output Path

Fig. 4-9 is an op-amp–level schematic for the analog output flow.

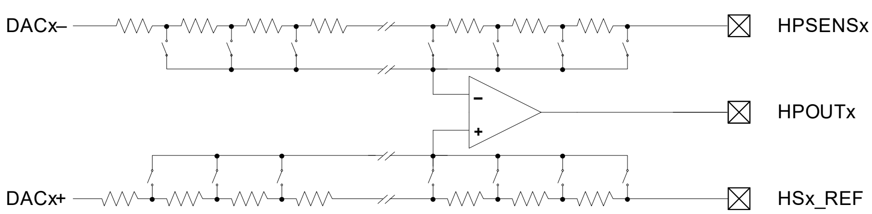


Figure 4-9. Op-Amp-Level Schematic—Analog Outputs

4.4.1 Pseudodifferential Outputs

The analog output amplifiers use a pseudodifferential output topology that allows the amplifier to monitor the ground potential at the load through the reference pins (HSx_REF, RING_SENSE). Minimize the impedance from the CS42L42 reference pin to the load ground (typically the connector ground). Impedance in this path affects analog output attenuation as well as the common-mode rejection of the output amplifier, which affects output offset and step deviation.

4.4.2 Using External Output Switches

The CS42L42 can work with external switches for the headphone outputs along with mic inputs. Fig. 4-10 shows a simplified, closed-loop example of supporting two separate headsets, including headphone and mic support. For simplicity, tip sense and ring sense connectivity is not shown.

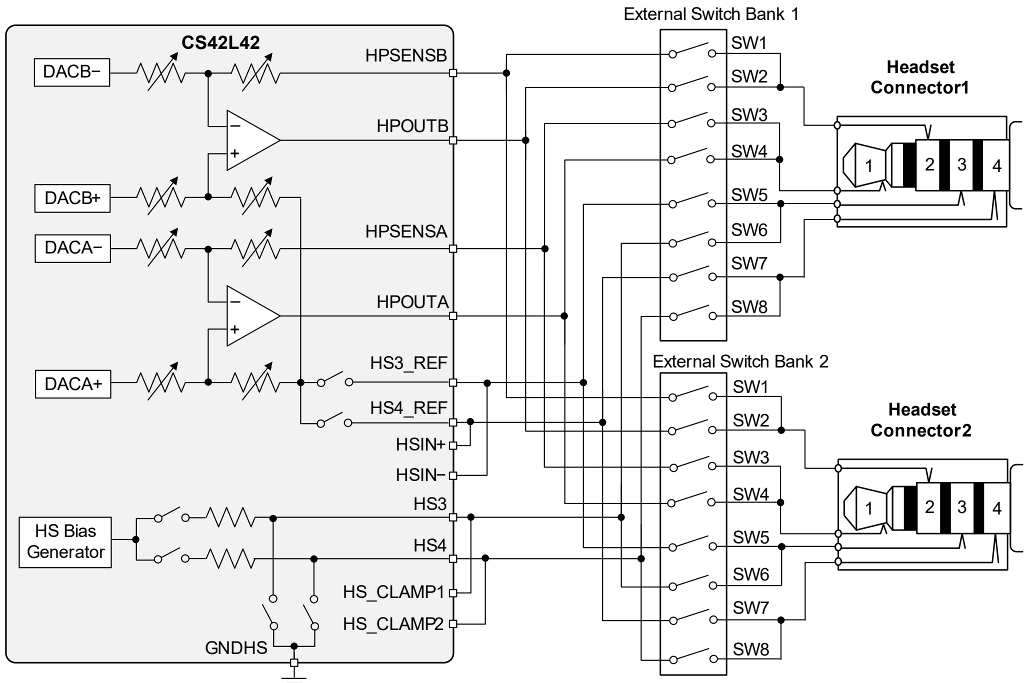


Figure 4-10. Closed-Loop External Output Switches

Fig. 4-10 shows HPSENSA and HPSENSB, pins not typically seen in the HP output. They allow the feedback point of the HP output to include the switch impedance. This closed-loop method improves output performance, although the following considerations must be adhered to when incorporating external switches:

- The combined switch ON-resistance (R_{ON}) and PCB trace resistance must be less than 1 Ω. Although any added resistance in the signal path decreases output voltage swing, keeping the total resistance below 1 Ω minimizes the voltage loss along with reducing the effect on DC offsets. For example, for a 30-Ω load, the full-scale output voltage swing is reduced by the extent of the switches' ON-resistance.
- The switch ON-resistance flatness (R_{ON} flatness) must be less than 0.02 Ω over the common-mode voltage swing of these switches. for SW6 and SW8 and less than 0.075 Ω over the common-mode voltage swing of SW2 and SW4. Failure to meet this requirements degrades THD performance.

  Note that not just the value of the switches' R_{ON} flatness, but also its shape has a considerable effect on THD performance. It is recommended that the shape be as linear as possible over the common-mode voltage swing appearing at each switch. Shapes such as "W", "N", and "M" significantly affect THD, even if their R_{ON} flatness meets the values defined here.
- The total capacitance placed on the HPOUTx pins is limited to 1 or 10 nF, depending on the HPOUT_LOAD setting (see p. 155). The combined switch capacitance (C_{ON} + C_{OFF}), PCB stray capacitance, and any headphone connector/cable/load capacitance must be within these limits, otherwise stability is reduced and THD is degraded. Because the amplifier feedback path includes the switches, HP_PDN must be set if the switches are open.

4.4.3 Using Open-Loop Configuration for Multiple HPs and Mics

The open-loop configuration shown in Fig. 4-11 offers another way to support multiple headphones and microphones.

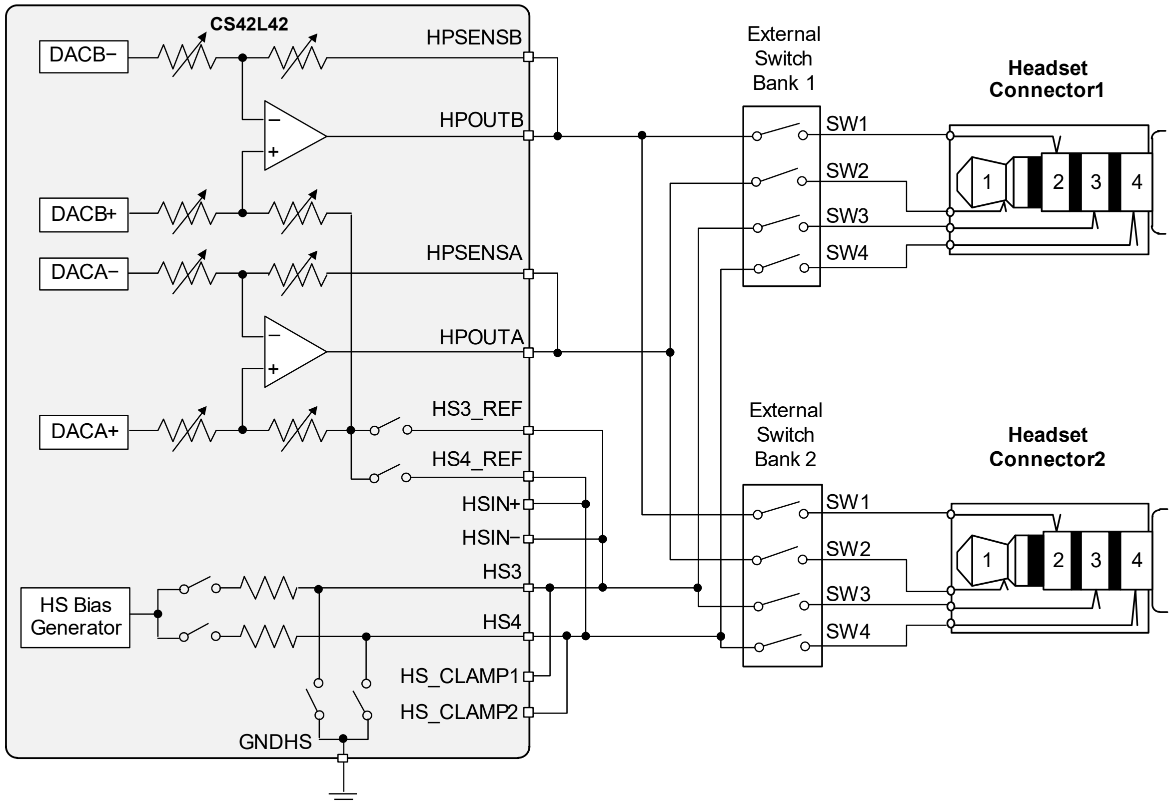


Figure 4-11. Open-Loop Configuration

This approach requires half the number of switches, saving PCB space and cost, addressing routing concerns, and decreasing the total capacitance. The drawback is that the feedback points do not account for switch characteristics, which leads to significantly degraded THD performance and an increased reduction in voltage appearing at the headphone connector. Due to these factors, this open-loop approach is not recommended for general use.

The closed-loop approach feedback point is taken at the connector. This forces the HP output amplifier to correct for switch characteristics even though the maximum output voltage swing is the same for both configurations. Additionally, the HSx_REF connection point is also at the connector in the closed-loop configuration, which improves HP performance over the open-loop method. Together, the closed-loop configuration results in the best performance if switches must be used.

4.4.4 Output Load Detection

The CS42L42 can distinguish between the following output loads:

- R_L = 15, 30, or 3 kΩ
- C_L < ~2 nF (low capacitance); C_L > ~2 nF (high capacitance)

Note: Channels A and B must have matching loads, although load detection is performed using Channel A.

Before output load detection is initiated, the following steps must be performed:

1. HS-type information must be determined to run a headset load-detection sequence, as described in Section 4.13.
2. Power down the ADC and HP blocks: ADC_PDN = 1, HP_PDN = 1 (see p. 131).
3. Mute the analog outputs: ANA_MUTE_B = ANA_MUTE_A = 1 (see p. 156).
4. Disable the DAC high-pass filter: DAC_HPF_EN = 0 (see p. 155).
   Note: Restore the previous setup after detection completes.

5. Set LATCH_TO_VP (see p. 151).
6. Set HSBIAS_CTRL to 00 (Hi-Z Mode; see p. 151).
7. Set ADPTPWR = 100 (see p. 156).
8. Set the analog soft-ramp rate (ASR_RATE = 0111; see p. 130).
9. Set the digital soft-ramp rate (DSR_RATE; see p. 130) = 0001.
10. After load detection completes, ASR_RATE, DSR_RATE, ADPTPWR, and DAC_HPF_EN must be restored to their previous values. See Section 4.6 for details.

See the detailed detection instruction sequence in Ex. 5-5 for details.

After an HP-detect event, if HP_LD_EN is set (see p. 149), the CS42L42 proceeds to detect the resistance and capacitance of the output load. A 24-kHz tone is output on HPOUTA, and HS3 or HS4 (depending on China headset detect results) is measured using an internal resistor bank as a reference.

RLA_STAT (see p. 149) reports resistance-detection results for Channel A as follows:

- 00: 15 Ω
- 01: 30 Ω
- 10: 3 kΩ
- 11: Reserved

If the typical output resistance of less than ~300 Ω is indicated, a low-capacitance load is assumed. If the resistance is greater than 300 Ω, capacitance detection proceeds. After the detection sequence completes, HPLOAD_DET_DONE (see p. 149) is set. The results of capacitor detection is reported in CLA_STAT (see p. 149). This result can be used to program the value in HPOUT_LOAD(see p. 155), which determines the compensation of the headphone amplifier.

Notes:

- The HP path must be powered down before updating the HPOUT_LOAD setting and repowered afterwards.
- Low capacitance results were determined with C_L = 1 nF; high capacitance results were determined with C_L = 10 nF.

4.4.5 Slow Start Control

Mixer, DAC, and HP soft ramping is enabled through SLOW_START_EN (p. 130). If SLOW_START_EN = 111, changes to DAC/HP volumes are applied slowly by stepping through each volume-control setting with a delay between steps equal to an integer number of Fs periods. The delay between steps, which can vary from 1/Fs to 72/Fs periods, is set via DSR_RATE and ASR_RATE (see p. 130).

If ramping is disabled, changes occur immediately with the clock edge.

4.5 System Headphone Parasitic Resistances

Parasitic resistances limit the measurements on several specs, including the following:

- Headphone-to-analog input isolation
- Headphone interchannel isolation
- Headphone mute attenuation
- Headphone DC offset

Fig. 4-12 shows the headphone-to-analog input electrical path.

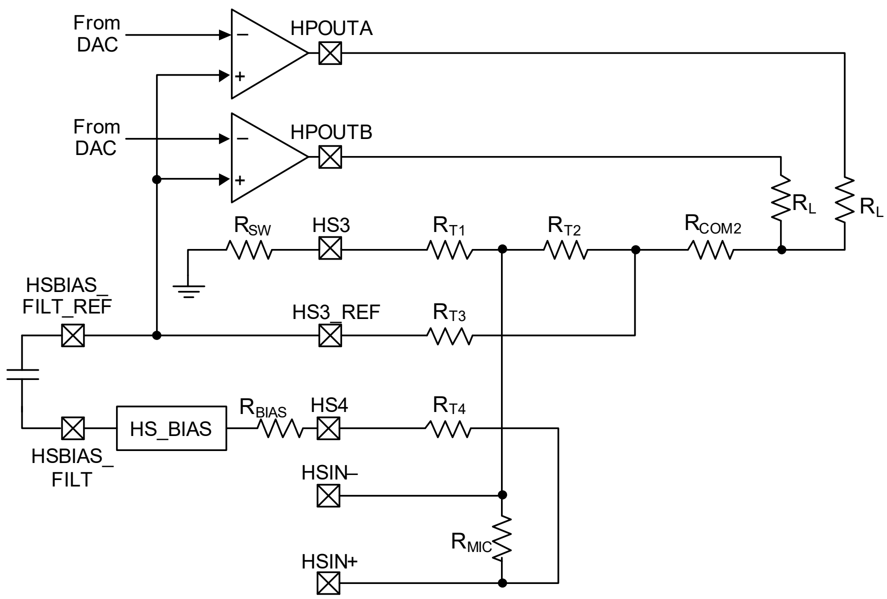


Figure 4-12. Headphone-to-ADC Electrical Path

Based on Fig. 4-12, the formula in Eq. 4-2 measures headphone-to-analog isolation.

$$\text{Isolation} = 20 \cdot \log\left(\frac{2}{R_L} \cdot R_{T2}\right)$$

Equation 4-2. Headphone-to-Analog Isolation Equation

Eq. 4-2 gives an isolation of +69.03 dB, given the following:

- $R_L = 30\ \Omega$
- $R_{T2} = 0.0053\ \Omega$
- $R_{COM2} = 0.1\ \Omega$
- $R_{BIAS} = 2.21\ k\Omega$
- $R_{MIC} = 2.21\ k\Omega$

Fig. 4-13 shows the headphone electrical path.

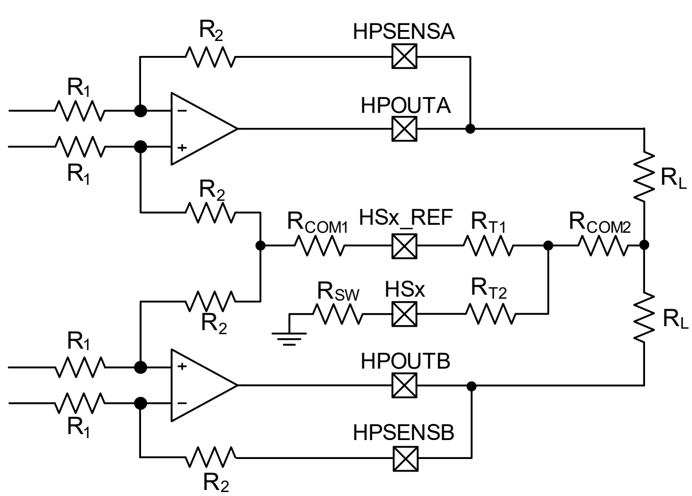


Figure 4-13. Headphone Electrical Path

Based on Fig. 4-13, the formula Eq. 4-3 can be used to measure the headphone interchannel isolation, and formula Eq. 4-4 can be used to measure the actual mute attenuation based on a measured mute attenuation.

$$\text{Interchannel Isolation} = -20 \cdot \log\left|\frac{R_{COM1} + R_{T1}}{2 \cdot (R_1 + R_2)} - \frac{R_{COM2}}{R_L}\right|$$

Equation 4-3. Headphone Interchannel Isolation (ICI) Equation

Eq. 4-3 yields a headphone interchannel isolation of +83.5 dB when the following assumptions are made:

- $R_L = 30\ \Omega$
- $R_1 = R2 = 12\ k\Omega$
- $R_{T1} = 0.002\ \Omega$
- $R_{COM1} = 0.001\ \Omega$
- $R_{COM2} = 0.002\ \Omega$‘

Eq. 4-4 can be used to measure the mute attenuation:

$$\text{Mute Attenuation} = 20 \cdot \log\left(10^{\left(\frac{(MA_M + 6)}{20}\right)} - \frac{R_{T1}}{12000}\right) - 6$$

Equation 4-4. Headphone Mute Attenuation Equation

Eq. 4-4 yields an actual mute attenuation of –87.77 dB assuming the following:

- $R_{T1} = 0.4\ \Omega$
- MA_M (Mute attenuation measured) = –84.8 dB

Because large values of R_{T1} cause increased DC offset (see Fig. 4-13), it is recommended to keep RT1 less than 1 Ω.

4.6 Class H Amplifier

Fig. 4-14 shows the Class H operation.

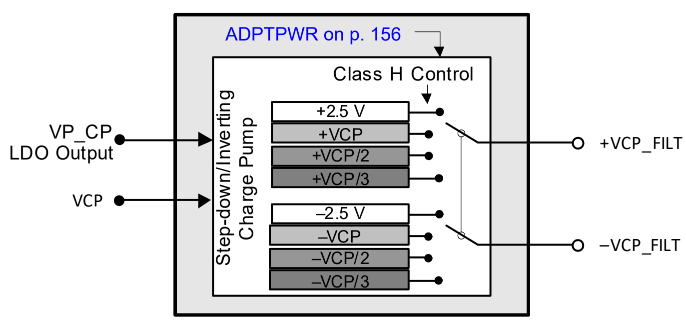


Figure 4-14. Class H Operation

The CS42L42 HP output amplifiers use a Cirrus Logic four-mode Class H technology, which maximizes operating efficiency of the typical Class AB amplifier while maintaining high performance. In a Class H amplifier design, the rail voltages supplied to the amplifier vary with the needs of the music passage being amplified. This conserves energy during low-power passages and when the program material is played back at low volume.

The internal charge pump, which creates the rail voltages for the HP amplifiers, is the central component of the four-mode Class H technology. The charge pump receives its input voltage from the voltage present on either the VCP or VP pin. From this voltage, the charge pump generates the differential rail voltages supplied to the amplifier output stages. The charge pump can supply four sets of differential rail voltages: ±2.5, ±VCP, ±VCP/2, and ±VCP/3.

Table 4-3 shows the nominal signal- and volume-level ranges if the amplifier is set to the adapt-to-signal mode explained in Section 4.6.1. In addition to adapting to the input signal, the Class H control is capable of monitoring the internal headphone amplifier supply to allow more efficient, load-dependent, automatic Smart Class H Mode selection. In fixed modes, if the signal level exceeds the maximum value of the indicated range, clipping can occur.

Table 4-3. Class H Supply Modes

Load		Mode	Class-H Supply Voltage	Signal-Level Range [1,2,3,4]
Resistance	Capacitance			
15 Ω	1 nF	0	±2.5 V	≥ –8 dB
		1	± VCP	–9 to –14 dB
		2	± VCP/2	–15 to –20 dB
		3	± VCP/3	≤ –21 dB
	10 nF	0	±2.5 V	≥ –9 dB
		1	± VCP	–10 to –14 dB
		2	± VCP/2	–15 to –19 dB
		3	± VCP/3	≤ –20 dB
30 Ω	1 or 10 nF	0	±2.5 V	≥ –4 dB
		1	± VCP	–5 to –11 dB
		2	± VCP/2	–12 to –16 dB
		3	± VCP/3	≤ –17 dB
3 kΩ	1 or 10 nF	0	±2.5 V	≥ –1 dB
		1	± VCP	–2 to –8 dB
		2	± VCP/2	–9 to –13 dB
		3	± VCP/3	≤ –14 dB

1. In Adapt-to-Signal Mode, volume level ranges are approximations but are within –0.5 dB from the values shown.
2. Relative to digital full scale with FULL_SCALE_VOL set to 0 dB.
3. In fixed modes, clipping occurs if the signal level exceeds the maximum of this range due to setting the amplifier's supply too low.
4. To optimize efficiency, smart Class H thresholds automatically vary based on load conditions.

4.6.1 Power Control Options

This section describes the supported types of operation: standard Class AB and adapt to signal. The set of rail voltages supplied to the amplifier output stages depends on the ADPTPWR setting, as described in Section 7.14.1.

4.6.1.1 Standard Class AB Operation (ADPTPWR = 001, 010, 011, or 100)

If ADPTPWR is set to 001, 010, 011, or 100, the rail voltages supplied to the amplifiers are held to ±2.5, ±VCP, ±VCP/2, or ±VCP/3, respectively. For these settings, the rail voltages supplied to the output stages are held constant, regardless of the signal level. In these settings, the CS42L42 amplifiers operate in a traditional Class AB configuration.

4.6.1.2 Adapt-to-Output Signal (ADPTPWR = 111)

If ADPTPWR = 111, the rail voltage sent to the amplifiers is based only on whether the signal sent to the amplifiers would cause the amplifiers to clip when operating on the lower set of rail voltages at certain threshold values.

- If clipping can occur, the control logic instructs the charge pump to provide the next higher set of rail voltages.
- If clipping could not occur, the control logic instructs the charge pump to provide the lower set of rail voltages, eliminating the need to advise the CS42L42 of volume settings external to the device.

4.6.2 Power-Supply Transitions

Charge-pump transitions from the lower to the higher set of rail voltages occur on the next FLYN/FLYP clock cycle. Despite the system's fast response time, the VCP_FILT pin's capacitive elements prevent rail voltages from changing instantly. Instead, the rail voltages ramp from the lower to the higher supply, based on the time constant created by the output impedance of the charge pump and the capacitor on the VCP_FILT pin (the transition time is approximately 20 µs).

Fig. 4-15 shows Class H supply switching. During this transition, a high dV/dt transient on the inputs may briefly clip the outputs before the rail voltages charge to the full higher supply level. This transitory clipping has been found to be inaudible in listening tests.

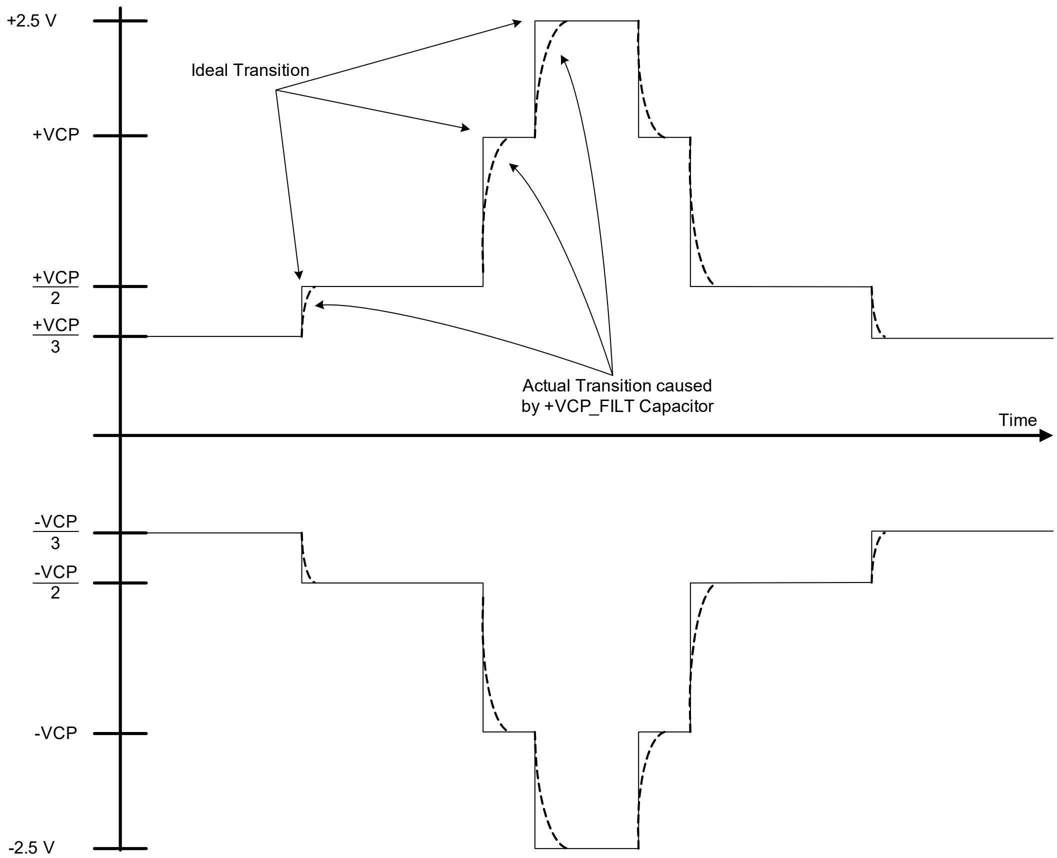


Figure 4-15. VCP_FILT Transitions—Headphone Output

When the charge pump transitions from the higher to the lower set of rail voltages, there is a 5.5-s delay before the charge pump supplies the lower rail voltages to the amplifiers. This hysteresis ensures that the charge pump does not toggle between the two rail voltages as signals approach the clip threshold. It also prevents clipping in the instance of repetitive high-level transients in the input signal. Fig. 4-16 shows this transitional behavior.

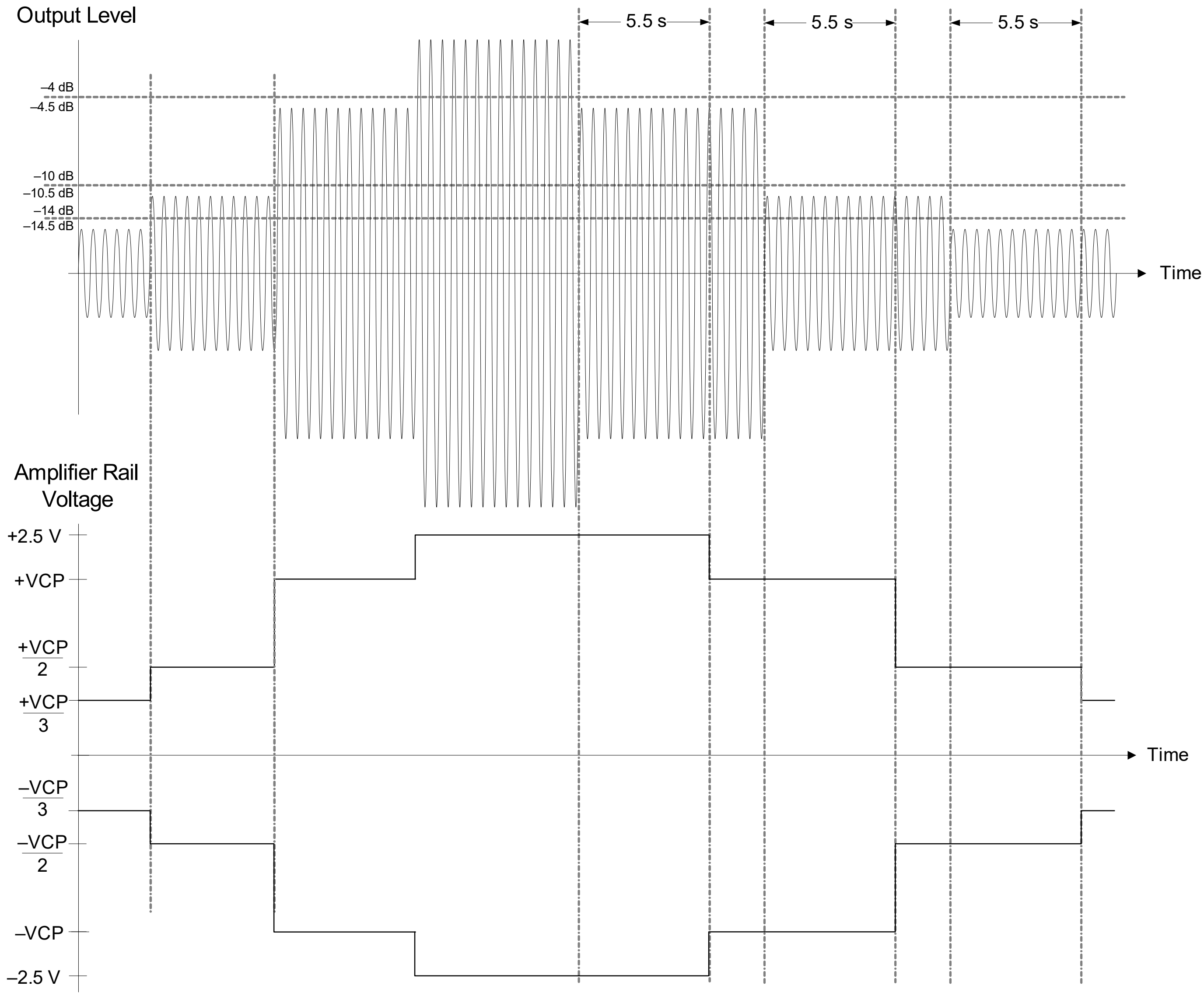


Figure 4-16. VCP_FILT Hysteresis—Headphone Output

4.6.3 Efficiency

As discussed in previous sections, amplifiers internal to the CS42L42 operate from one of four sets of rail voltages, based on the needs of the signal being amplified. Fig. 4-17 and Fig. 4-18 show power curves for all modes of operation and provides details regarding the power supplied to 15- and 30-Ω stereo loads versus the power drawn from the supply for each Class H mode.

If rail voltages are set to ±2.5 V, the amplifiers operate in their least efficient mode for low-level signals. If they are held at ±VCP, ±VCP/2, or ±VCP/3, amplifiers operate more efficiently, but are clipped if required to amplify a full-scale signal.

The adapt-to-signal trace shows the benefit of four-mode Class H operation. At lower output levels, amplifier output is represented by the ±VCP/3 or ±VCP/2 curve, depending on the signal level. At higher output levels, amplifier output is represented by the ±VCP or ±2.5-V curve. The duration for which the amplifiers operate within any of the four curves (±VCP/3, ±VCP/2, ±VCP, or ±2.5 V) depends on both the content and the output level of the material being amplified. The highest efficiency operation results from maintaining an output level that is close to, without exceeding, the clip threshold of the particular supply curve.

Note that the Adapt-to-Signal Mode trace in Fig. 4-17 shows that it never transitions to Mode 0, because FULL_SCALE_VOL = 1 (–6 dB) due to a 15-Ω stereo load.

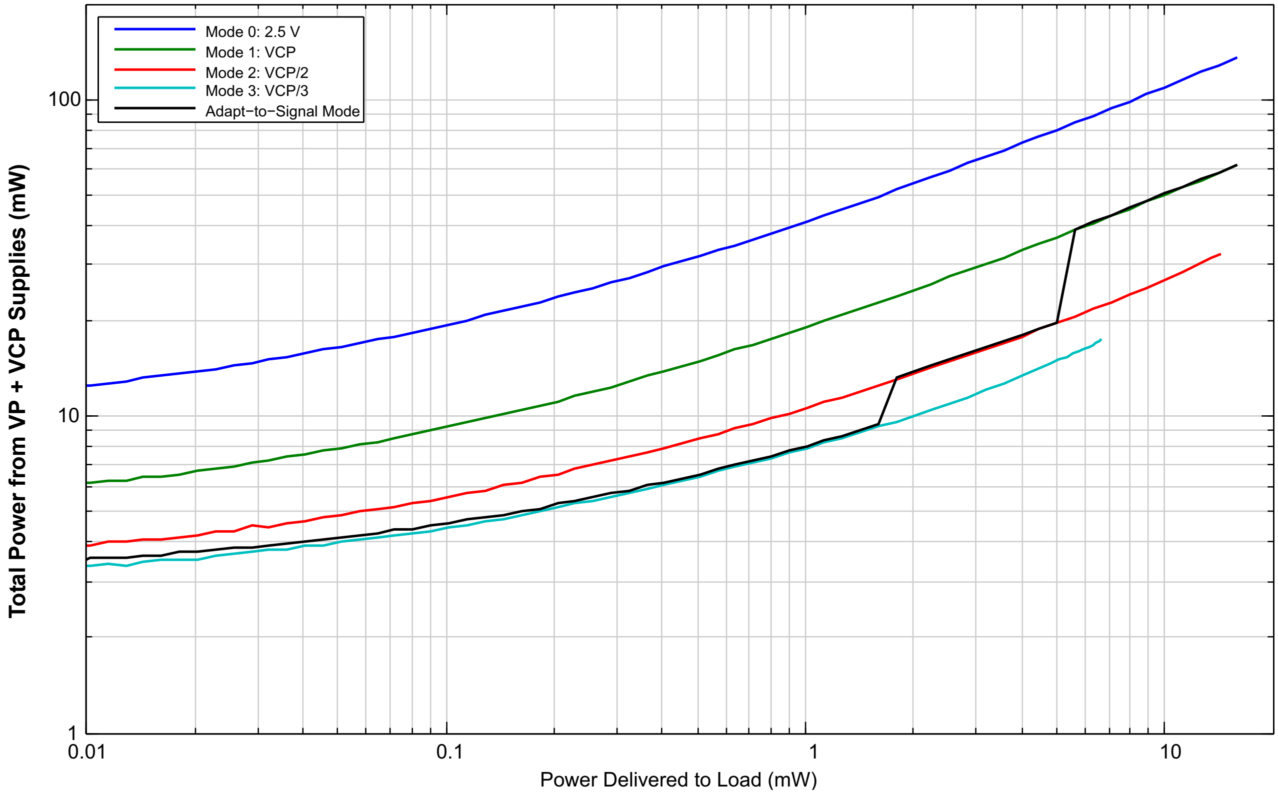


Figure 4-17. Class H Power-to-Load Versus Power from Supply (15 Ω, Stereo)

The Adapt-to-Signal Mode trace in Fig. 4-18 shows the transition to Mode 0, because FULL_SCALE_VOL = 0 (0 dB) due to a 30-Ω stereo load.

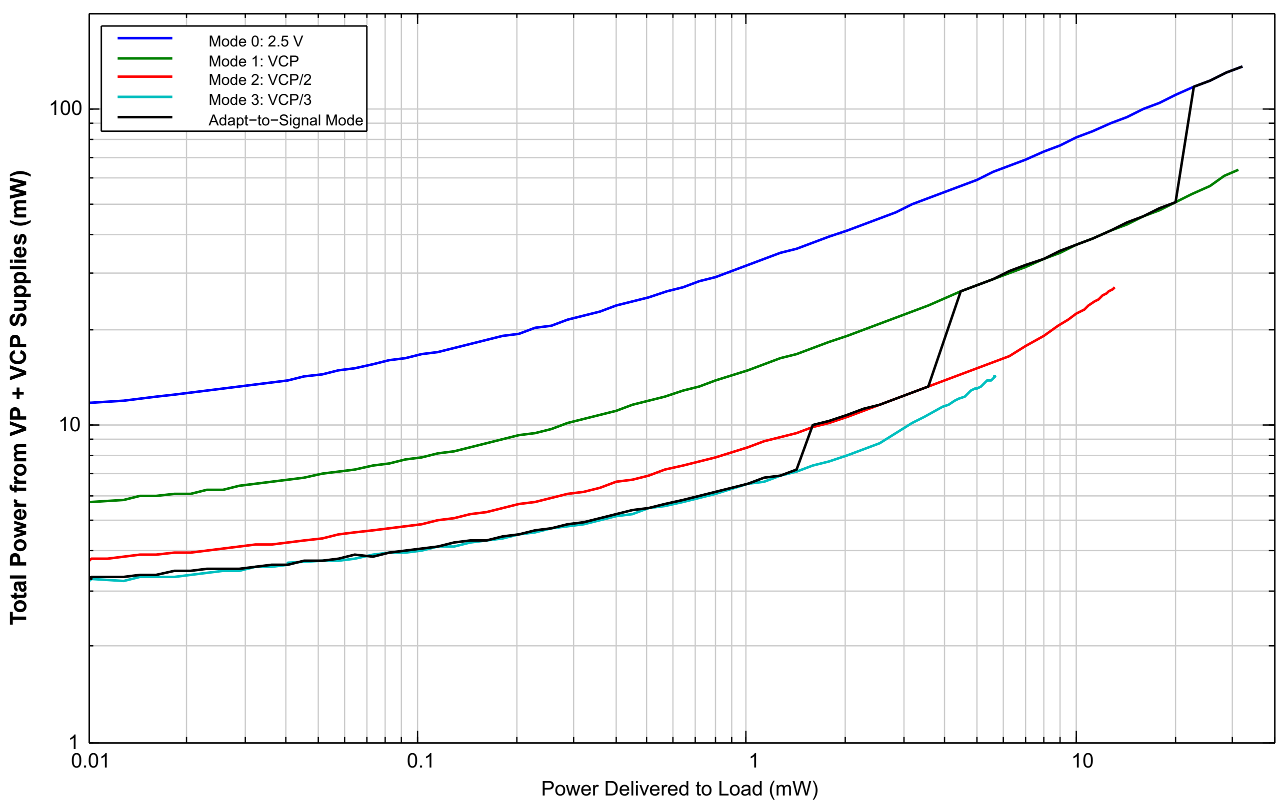


Figure 4-18. Class H Power-to-Load Versus Power from Supply (30 Ω, Stereo)

4.6.4 HP Current Limiter

The CS42L42 features built-in current-limit protection for the HP output. Table 3-16 lists the current limit threshold during the short-circuit conditions shown in Fig. 4-19. For HP amplifiers, current is from the internal charge-pump output, and, as such, applies the current from VCP or VP, depending on the mode.

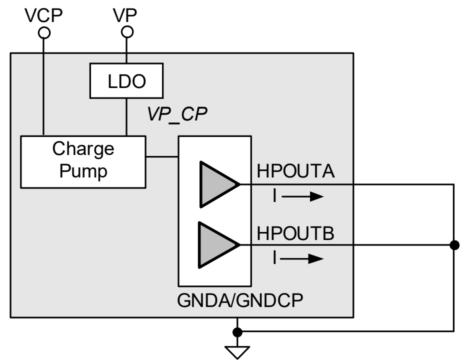
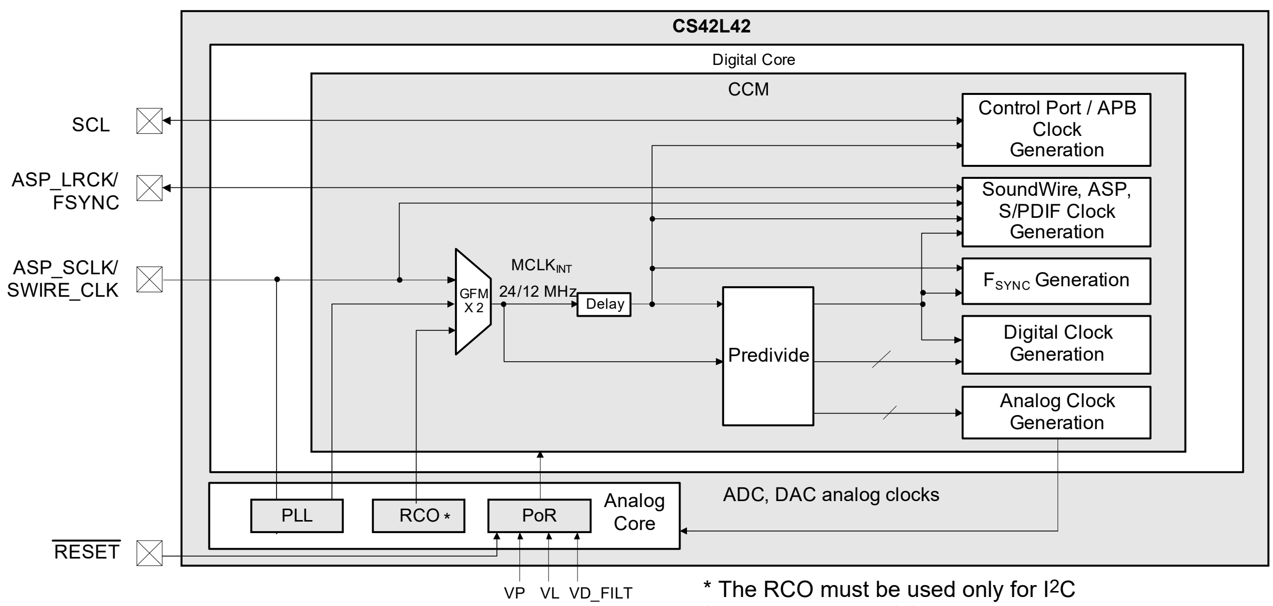


Figure 4-19. HP Short-Circuit Setup

4.7 Clocking Architecture

The CS42L42 offers several ways to support control, ASP operation, data conversion, and signal processing. Internal clocks are generated either from SCLK (ASP_SCLK/SWIRE_CLK) or from the integrated fractional-N PLL; see Fig. 4-20. Depending on the MCLK_SRC_SEL setting (see Fig. 4-21), $MCLK_{INT}$ is provided by one of the following methods:

- Externally sourced directly from the ASP_SCLK/SWIRE_CLK input pin
- Internally generated from an integrated fractional-N PLL with ASP_SCLK/SWIRE_CLK as a reference clock



* The RCO must be used only for I2C functionality when SCLK is not available.

Figure 4-20. Clock Architecture Block Diagram

4.7.1 Start-Up Clocking Using the RC Oscillator (RCO)

At power on, an integrated low-power RCO, shown in Fig. 4-20, functions as the default clock for the digital core of the CS42L42, during which time SCLK is unavailable. A reset event always returns it to running off of the RCO. If SCLK is unavailable, RCO clocking must be used only for I2C functionality.

RCO is multiplexed with $MCLK_{INT}$ and fed to the I2C slave control port. The SCLK must become active and the RCO must be disabled before data conversion.

Note the following:

- OSC_SW_SEL_STAT (see p. 134) indicates the status of the clock switching (in transition, RCO, or SCLK/PLL). With the existing encoding, only one bit can physically change at a time, and the bit changing is always synchronous to the clock that is currently selected.
- OSC_PDNB_STAT (see p. 134) indicates the RCO power-down status.
- SCLK_PRESENT is used to determine the internal MCLK source. See Section 7.4.6 for details.

The clock-switch state machine uses the transition of SCLK_PRESENT to both initiate switches between the selected internal MCLK between the SCLK pin (SCLK_PRESENT = 1) or the internal RCO (SCLK_PRESENT = 0) and to send the I2C stop condition that each switching event requires. During switching, a delay of at least 150 µS is needed before additional successful I2C communication can begin to use the new clocking source.

Notes:

- Muting the system is recommended when a new clock source is chosen.
- For normal operation, SCLK—not RCO—must be used (SCLK_PRESENT = 1) for running the ASP data path.

4.7.1.1 Switching from RCO

With SCLK running, an SCLK_PRESENT 0-to-1 transition starts a switch from the RCO to the selected SCLK or PLL. This switch is superseded by any outstanding I2C transactions. After the I2C stop condition is sent, the transition begins, taking 150 µs to complete, during which time the system requires that no new I2C transactions be initiated. The next I2C transaction can begin after this 150-µs delay.

4.7.1.2 Switching to RCO

To stop SCLK, the system must revert to RCO clocking to ensure that I2C communications function properly. To power the RCO back up, SCLK_PRESENT must be cleared before stopping SCLK. A 1-to-0 SCLK_PRESENT transition generates a glitch-free mux switch timing from SCLK to RCO. SCLK must remain running during the transition and new I2C transactions must not be initiated for at least 150 µs after an I2C stop is received. The next I2C transaction cannot begin until after this 150-µs delay.

Failure to account for this could cause communications to fail.

4.7.2 $MCLK_{INT}$ Sources

The $MCLK_{INT}$ source is supplied directly from ASP_SCLK/SWIRE_CLK input pin or from the fractional-N PLL. MCLKDIV must be set according to the $MCLK_{INT}$ frequency, which must be set to either the 12-MHz region (11.2896–12.288 MHz) or the 24-MHz region (22.5792–24.576 MHz). Table 4-6 shows several examples. Table 4-4 lists further restrictions.

Table 4-4. $MCLK_{INT}$ Source Restrictions

$MCLK_{INT}$ Source	MCLK_SRC_SEL (see p. 137)	MCLKDIV (see p. 137)	Nominal ASP_SCLK/SWIRE_CLK Pin Frequency
ASP_SCLK/ SWIRE_CLK	0	0	12 MHz
		1	24 MHz
Fractional-N PLL	1	0	12 MHz
		1	24 MHz

$MCLK_{INT}$ is switched through internal glitchless clock muxing. Doing so during operation may cause audible artifacts, but does not put the device into an unrecoverable state. Therefore, it is recommended to mute the system for at least 150 µs.

If $MCLK_{INT}$ is sourced from the PLL, on-the-fly frequency changes to the source may cause the PLL to go out of phase lock with the clock source. To reduce the risk of audible artifacts, it is recommended to mute the system first. Any necessary configuration changes based on the new clock source frequency must occur before unmuting the system.

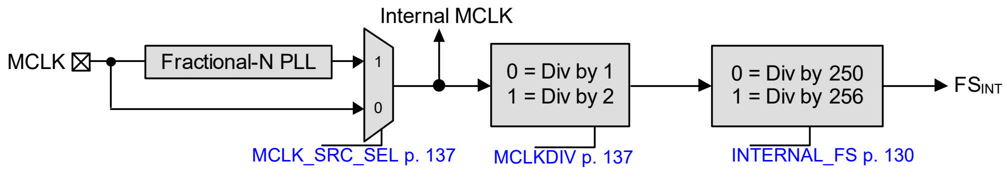


Figure 4-21. MCLK INT Source Switching

For proper internal Fs clocking, the INTERNAL_FS and MCLKDIV bits must be configured, as shown in Table 4-4.

Table 4-5. Determining Fs_{INT}

$MCLK_{INT}$ (MHz)	MCLKDIV (see p. 137	INTERNAL_FS (see p. 130)	Resulting Fs_{INT} (kHz)
11.2896	0	1	44.1
12	0	0	48
12.288	0	1	48
22.5792	1	1	44.1
24	1	0	48
24.576	1	1	48

Note: The control-port/advanced peripheral bus (APB) frequency is equal to the $MCLK_{INT}$ frequency.

4.7.3 Fractional-N PLL

The CS42L42 has an integrated fractional-N PLL to support the clocking requirements of the internal analog circuits and converters. This PLL can be enabled or bypassed to suit system-clocking needs. The input reference clock for the PLL is the ASP_SCLK/SWIRE_CLK input pin. The reference clock frequency must be between 2.8224 and 25 MHz.

The PLL can be configured for a wide range of combinations of SCLK and $MCLK_{INT}$. PLL_REF_INV (see p. 140) can be used to invert the PLL reference clock. Table 4-6 lists common settings.

Table 4-6. Common PLL Setting Examples

SCLK (MHz)	MCLK_SRC_SEL (see p. 137) [1]	SCLK_PREDIV (see p. 140) [2]	PLL_DIV_INT (see p. 148)	PLL_DIV_FRAC (see p. 148) [2]	PLL_MODE (see p. 148)	PLL_DIVOUT (see p. 148) [3]	$MCLK_{INT}$ (MHz)	PLL_CAL_RATIO (see p. 148)	*n* [4]
1.024	1	00	0xAC	0x44 0000	01	0x10	11.2896	118	3
	1	00	0xBB	0x80 0000	11	0x10	12	125	3
	1	00	0xC0	0x00 0000	11	0x10	12.288	128	3
1.536	1	00	0x72	0xD8 0000	01	0x10	11.2896	118	2
	1	00	0x7D	0x00 0000	11	0x10	12	125	2
	1	00	0x80	0x00 0000	11	0x10	12.288	128	2
	1	00	0x7D	0x00 0000	11	0x08	24	125	4
	1	00	0x80	0x00 0000	11	0x08	24.576	128	4
2.048	1	00	0x56	0x22 0000	01	0x10	11.2896	88	2
	1	00	0x5D	0xC0 0000	11	0x10	12	94	2
	1	00	0x60	0x00 0000	11	0x10	12.288	96	2
2.8224	1	00	0x40	0x00 0000	11	0x10	11.2896	128	1
	1	00	0x40	0x00 0000	11	0x08	22.5792	128	2
3	1	00	0x3C	0x36 1134	11	0x10	11.2896	120	1
	1	00	0x40	0x00 0000	11	0x10	12	128	1
	1	00	0x40	0x00 0000	01	0x10	12.288	131	1
	1	00	0x40	0x00 0000	11	0x08	24	128	2
	1	00	0x40	0x00 0000	01	0x08	24.576	131	2
3.072	1	00	0x39	0x6C 0000	01	0x10	11.2896	118	1
	1	00	0x3E	0x80 0000	11	0x10	12	125	1
	1	00	0x40	0x00 0000	11	0x10	12.288	128	1
	1	00	0x3E	0x80 0000	11	0x08	24	125	2
	1	00	0x40	0x00 0000	11	0x08	24.576	128	2

Table 4-6. Common PLL Setting Examples ***(Cont.)***

SCLK (MHz)	MCLK_SRC_SEL (see p. 137) [1]	SCLK_PREDIV (see p. 140) [2]	PLL_DIV_INT (see p. 148)	PLL_DIV_FRAC (see p. 148) [2]	PLL_MODE (see p. 148)	PLL_DIVOUT (see p. 148) [3]	$MCLK_{INT}$ (MHz)	PLL_CAL_RATIO (see p. 148)	*n* [4]
4.00	1	00	0x2D	0x28 8CE7	11	0x10	11.2896	90	1
	1	00	0x30	0x00 0000	11	0x10	12	96	1
	1	00	0x30	0x00 0000	01	0x10	12.288	98	1
4.096	1	00	0x2B	0x11 0000	01	0x10	11.2896	88	1
	1	00	0x2E	0xE0 0000	11	0x10	12	94	1
	1	00	0x30	0x00 0000	11	0x10	12.288	96	1
5.6448	1	01	0x40	0x00 0000	11	0x10	11.2896	128	1
	1	01	0x40	0x00 0000	11	0x08	22.5792	128	2
6	1	01	0x3C	0x36 1134	11	0x10	11.2896	120	1
	1	01	0x40	0x00 0000	11	0x10	12	128	1
	1	01	0x40	0x00 0000	01	0x10	12.288	131	1
	1	01	0x40	0x00 0000	11	0x08	24	128	2
	1	01	0x40	0x00 0000	01	0x08	24.576	131	2
6.144	1	01	0x39	0x6C 0000	01	0x10	11.2896	118	1
	1	01	0x3E	0x80 0000	11	0x10	12	125	1
	1	01	0x40	0x00 0000	11	0x10	12.288	128	1
	1	01	0x3E	0x80 0000	11	0x08	24	125	2
	1	01	0x40	0x00 0000	11	0x08	24.576	128	2
9.6	1	10	0x49	0x80 0000	01	0x10	11.2896	150	1
	1	10	0x50	0x00 0000	11	0x10	12	80	2
	1	10	0x50	0x00 0000	01	0x10	12.288	82	2
	1	10	0x49	0x80 0000	01	0x08	22.5792	150	2
	1	10	0x50	0x00 0000	11	0x08	24	107	3
	1	10	0x50	0x00 0000	01	0x08	24.576	109	3
11.2896	0	—	—	—	—	—	11.2896	—	—
	1	10	0x40	0x00 0000	11	0x08	22.5792	128	2
12	1	10	0x3C	0x36 1134	11	0x10	11.2896	120	1
	0	—	—	—	—	—	12.0000	—	—
	1	10	0x40	0x00 0000	01	0x10	12.288	131	1
	1	10	0x40	0x00 0000	11	0x08	24	128	2
	1	10	0x40	0x00 0000	01	0x08	24.576	131	2
12.2880	1	10	0x39	0x6C 0000	01	0x10	11.2896	118	1
	1	10	0x3E	0x80 0000	11	0x10	12	125	1
	0	—	—	—	—	—	12.2880	—	—
	1	10	0x3E	0x80 0000	11	0x08	24	125	2
	1	10	0x40	0x00 0000	11	0x08	24.576	128	2
13	1	10	0x39	0xAB 52B5	01	0x11	11.2896	111	1
	1	10	0x3B	0x13 B13B	11	0x10	12	118	1
	1	10	0x3B	0x13 B13B	01	0x10	12.288	121	1
19.2	1	11	0x49	0x80 0000	01	0x10	11.2896	150	1
	1	11	0x50	0x00 0000	11	0x10	12	80	2
	1	11	0x50	0x00 0000	01	0x10	12.288	82	2
	1	11	0x49	0x80 0000	01	0x08	22.5792	150	2
	1	11	0x50	0x00 0000	11	0x08	24	107	3
	1	11	0x50	0x00 0000	01	0x08	24.576	109	3
22.5792	1	11	0x40	0x00 0000	11	0x10	11.2896	128	1
	0	—	—	—	—	—	22.5792	—	—
24	1	11	0x3C	0x36 1134	11	0x10	11.2896	120	1
	1	11	0x40	0x00 0000	11	0x10	12	128	1
	1	11	0x40	0x00 0000	01	0x10	12.288	131	1
	0	—	—	—	—	—	24	—	—
	1	11	0x40	0x00 0000	01	0x08	24.576	131	2
24.576	1	11	0x39	0x6C 0000	01	0x10	11.2896	118	1
	1	11	0x3E	0x80 0000	11	0x10	12	125	1
	1	11	0x40	0x00 0000	11	0x10	12.288	128	1
	1	11	0x3E	0x80 0000	11	0x08	24	125	2
	0	—	—	—	—	—	24.576	—	—

Table 4-6. Common PLL Setting Examples *(Cont.)*

SCLK (MHz)	MCLK_SRC_SEL (see p. 137) [1]	SCLK_PREDIV (see p. 140) [2]	PLL_DIV_INT (see p. 148)	PLL_DIV_FRAC (see p. 148) [2]	PLL_MODE (see p. 148)	PLL_DIVOUT (see p. 148) [3]	$MCLK_{INT}$ (MHz)	PLL_CAL_RATIO (see p. 148)	*n* [4]
26	1	11	0x39	0xAB 52B5	01	0x11	11.2896	111	1
	1	11	0x3B	0x13 B13B	11	0x10	12	118	1
	1	11	0x3B	0x13 B13B	01	0x10	12.288	121	1

1. If MCLK_SRC_SEL = 0, the PLL is bypassed and can be powered down by clearing PLL_START (see p. 147).
2. Refer to the register description for the decode.
3. The text following this table explains the use of PLL_DIVOUT, shown by the example configurations in Section 4.7.3.1 and Section 4.7.3.2.
4. The variable *n* represents the divide ratio. See Eq. 4-6.

Powering up the PLL can be accomplished in several configurations. Table 4-6 shows example configurations; the sequences in Section 4.7.3.1 and Section 4.7.3.2 can be used as models.

$MCLK_{INT}$ combinations not shown in Table 4-6 can be determined by Eq. 4-5:

Equation 4-5. Configuring SCLK, $MCLK_{INT}$ Configurations

$$MCLK_{INT} = \frac{SCLK}{SCLK\_PREDIV} \times \frac{(PLL\_DIV\_INT + PLL\_DIV\_FRAC)}{(500/512 \text{ or } 1029/1024 \text{ or } 1)} \times \frac{1}{PLL\_DIVOUT}$$

The internal PLL output must be between ~150 and ~300 MHz. The PLL_DIVOUT value must be an even integer. To maximize flexibility in sample-rate choice, $MCLK_{INT}$ must be nominally 12 or 24 MHz.

PLL_CAL_RATIO determines the operating point for the internal VCO. For most configurations, the default value gives proper performance. However, to keep the VCO within range, some scenarios require PLL_CAL_RATIO to be set during the PLL power-up sequence (see Section 4.7.3). Use Eq. 4-6 to calculate the proper VCO setting at PLL start-up:

Equation 4-6. Calculating the PLL_CAL_RATIO

$$PLL\_CAL\_RATIO = \frac{MCLKINT \times 32 \times SCLK\_PREDIV}{n \times SCLK}$$

The value of *n* in Eq. 4-6 is determined by the following:

- If the result is less than or equal to 151, by default, *n* equals 1.
- If the result is less than 151, use the result to determine the PLL_CAL_RATIO setting.
- If the result is greater than 151, select another divide factor of *n* configurations for SCLK (where *n* = 2,3, …). The result must be between 50 and 151 (see the power-up sequence in Section 4.7.3.2). Use the same *n* value to multiply PLL_DIVOUT during the power-up sequence; see Step 2 in Section 4.7.3.1. The functional value must be restored (Step 8). The same is shown in both standard examples.

4.7.3.1 PLL Power-Up Sequence (Example: SCLK = 4.096 MHz and MCLKINT = 12.288 MHz)

In this example, SCLK = 4.096 MHz and MCLKINT = 12.288 MHz.

1. Set SCLK_PREDIV to Divide-by-1 Mode (0x00).
2. Set PLL_DIVOUT to Divide-by-16 Mode (0x10). This reflects a value of *n* = 1, because the PLL_CAL_RATIO generated by Eq. 4-6 equals 96. See that the PLL_DIVOUT entry for this configuration in Table 4-6 used a Divide-by-16 Mode (0x10).
3. Clear the three fractional factor registers, PLL_DIV_FRAC (see Section 7.7.2).
4. Set the integer factor, PLL_DIV_INT to 48 (0x30).
5. Set the PLL Mode multipliers, PLL_MODE to 11 to bypass both 500/512 and 1029/1024 factors (0x03).
6. Set the PLL_CAL_RATIO to 96 (0x60, see Section 7.7.5).
7. Turn on the PLL by setting PLL_START (see p. 147).
8. As part of a standard sequence, after at least 800 µs, the PLL_DIVOUT value would need to restored to 16 (0x10), which is unnecessary here because that value did not change.

4.7.3.2 PLL Power-Up Sequence (Example: SCLK = 12 MHz and MCLKINT = 24 MHz)

In this example, SCLK = 12 MHz and $MCLK_{INT}$ = 24 MHz.

1. Set SCLK_PREDIV to Divide-by-4 Mode (0x02).
2. Set PLL_DIVOUT to Divide-by-16 Mode (0x10). This reflects a value of *n* = 2, because the PLL_CAL_RATIO generated by Eq. 4-6 was greater than 151. See that the PLL_DIVOUT entry for this configuration in Table 4-6 used a Divide-by-8 Mode (0x08).
3. Clear the three fractional factor registers, PLL_DIV_FRAC.
4. Set the integer factor, PLL_DIV_INT to 64 (0x40).
5. Set the PLL mode multipliers, PLL_MODE to 11 to bypass both 500/512 and 1029/1024 factors (0x03).
6. Set the PLL_CAL_RATIO to 128 (0x80).
7. Turn on the PLL by setting PLL_START.
8. After at least 800 µs, the PLL_DIVOUT value must be restored from 16 to 8 (0x08).

4.7.3.3 Nonstandard PLL Setting (Example: SCLK = 19.2 MHz and MCLKINT = 12 MHz)

In this example, SCLK = 19.2 MHz and $MCLK_{INT}$ = 12 MHz. (Note that a power-up sequence similar to Section 4.7.3.2 is required for this configuration due to *n* = 1.)

- SCLK = 19.2 MHz = available reference clock.
- $MCLK_{INT}$ = 12 MHz = desired internal MCLK.
- SCLK_PREDIV = 11 = divide SCLK by 8 as reference to PLL.
- PLL_DIV_INT = 0x50 = multiply reference clock by 80, yielding PLL out = 192 MHz.
- PLL_DIV_FRAC = 0x00 0000 = fractional portion equal to zero.
- PLL_MODE = 11 = 500/512 and 1029/1024 multipliers are bypassed.
- PLL_DIVOUT = 0x10 = divide PLL out by 16 to achieve $MCLK_{INT}$ of 12 MHz.

Table 4-7 shows nonstandard PLL configurations.

Table 4-7. Nonstandard PLL Settings

SCLK (MHz)	MCLK_SRC_SEL (see p. 137)	SCLK_PREDIV (see p. 140)	PLL_DIV_INT (see p. 148)	PLL_DIV_FRAC (see p. 148)	PLL_MODE (see p. 148)	PLL_DIVOUT (see p. 148)	$MCLK_{INT}$ (MHz)	PLL_CAL_RATIO (see p. 148)	*n* [1]
9.6	1	10	0x6E	0x40 0000	01	0x18	11.2896	75	1
	1	10	0x50	0x00 0000	11	0x10	12	80	1
	1	10	0x50	0x00 0000	01	0x10	12.288	82	1
	1	10	0x6E	0x400000	01	0x0C	22.5792	150	1
	1	10	0x50	0x00 0000	11	0x08	24	80	2
	1	10	0x50	0x00 0000	01	0x08	24.576	82	2
19.2	1	11	0x6E	0x40 0000	01	0x18	11.2896	150	1
	1	11	0x50	0x00 0000	11	0x10	12	80	2
	1	11	0x50	0x00 0000	01	0x10	12.288	82	2
	1	11	0x6E	0x40 0000	01	0x0C	22.5792	150	2
	1	11	0x50	0x00 0000	11	0x08	24	107	3
	1	11	0x50	0x00 0000	01	0x08	24.576	109	3

1. The variable *n* represents the divide ratio. See Eq. 4-6.

As shown in Fig. 4-22, the input to the PLL is the ASP_SCLK/SWIRE_CLK input pin.

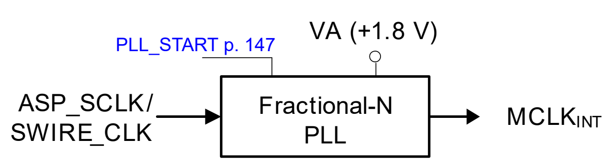


Figure 4-22. Clocking Architecture

4.7.3.4 Powering Down the PLL

To power down the PLL, clear PLL_START.

4.8 SoundWire Interface

The MIPI-compliant SoundWire slave interface transports control and audio data. The external SoundWire master interface communicates with the CS42L42 SoundWire slave using SWIRE_SD and SWIRE_CLK (described in Table 1-1), which are shared with all devices on the SoundWire bus. The interface is an alternative to the ASP and I^2C interfaces for audio and control-data transfer. SoundWire allows connection of all compatible audio sources and audio sinks over a single two-wire connection. The system includes the following features:

- Transporting payload, control, and setup data on a single two-wire interface
- Double data rate (DDR) transmission
- Direct slave-to-slave data transport
- Isochronous and asynchronous audio streams
- Asynchronous wake events can be generated as part of Clock Stop Mode

See the *MIPI SoundWire Specification* for details regarding features such as framing and synchronization.

4.8.1 Physical Interface and Data Encoding

The SoundWire interface has two logical signals:

- SWIRE_CLK—A system clock signal that is distributed from the master.
- SWIRE_SD—Data signal that can be driven by master or slave.

The interface uses conventional single-ended voltage-level signaling. The data encoding is modified NRZI, where an unchanging physical value (i.e., an encoded logic zero) is not actively driven, but is maintained by a bus keeper within the master. The bus keeper facilitates detection of undriven bit-symbol periods to identify errors and to handle systems that are not fully populated.

DDR signaling halves the required frequency of the clock signal, which reduces overall system power consumption.

4.8.2 Frame Structure

A SoundWire bit stream is a continuous stream of bits encoded using the modified-NRZI scheme. The bit stream is divided into a repetitive sequence of blocks of bits (i.e., *frames*). A frame consists of bit-symbol periods (i.e., *bit slots*) that correspond to one-half cycle of the clock signal. Each frame is constructed as a two-dimensional array of these bit slots made from 48 to 256 rows with 2 to 16 columns. The number of rows and columns is programmable. This provides a simple way to identify periodic positions within the bit stream to multiplex data from multiple sources.

Fig. 4-23 shows examples of frame organization.

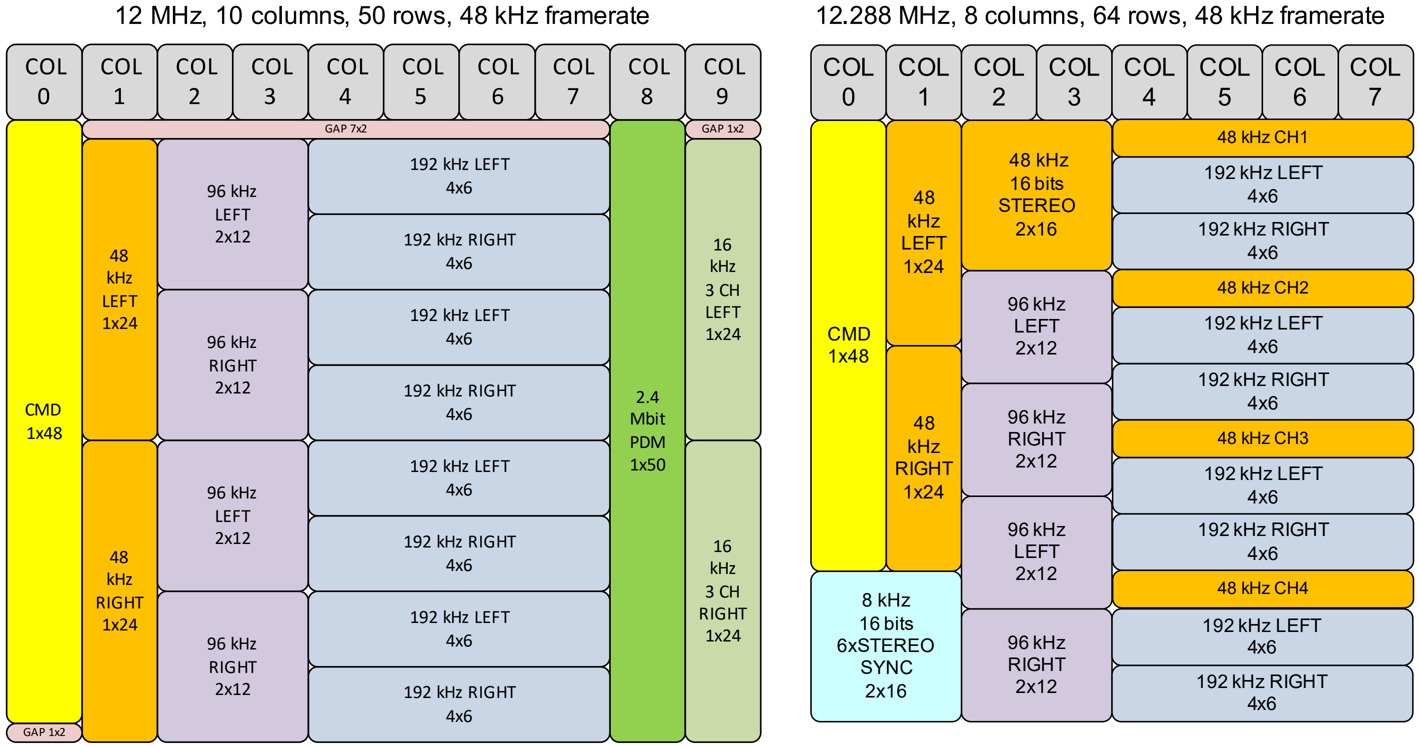


Figure 4-23. Examples of SoundWire Frame Payload Organization

Rows and columns are numbered from zero upwards. The transmission sequence of bit slots is done by an increasing order of rows, and, within each row, an increasing order of columns. The bit slots can be identified with a notation of [<Row>,<Column>]. Thus the first bit of a frame is [0,0], followed by [0,1], [0,2], up to [MaxRow,MaxCol].

The values on successive bit slots form a bit stream that interleaves all of the following:

- Control bits from the master
- Command bits from the master or monitor, and corresponding response bits from slaves or master
- Status bits from the slaves
- Payload data that can be transferred master to slave, slave to master, or slave to slave.

4.8.3 Control Word

A control word occupies the first 48 bits of Column 0 in any frame. Remaining bits of the frame not occupied by the control word are available for payload data. There are many options for organizing the payload data amongst the various channels and devices in the system. The control word is a 48-bit field in every SoundWire frame used by the master to read or write registers, control operations, and query slave status. It also provides frame synchronization information used by the slaves to keep in sync with the SoundWire Bus. The control word is split into multiple fields.

There are three types of commands:

- Ping—Every slave attached to the bus returns its status. The master sends a ping in any frame that is not performing a read or write command.
- Write—Writes an 8-bit value from the command owner to one or more registers in one or more devices.
- Read—Reads an 8-bit value from a register in one or more devices.

Each control word field has an owner, defining which device can drive the bus during that bit slot. Some slots have multiple owners. This multiple ownership uses the modified NRZI scheme to avoid bus contention. For example, if multiple slaves assert PREQ (ping request, see Table 4-6) to pass a Logic 1 symbol by toggling the data pin in the same bit slot, all drivers on the bus are driving the data to the same value, so there is no contention. Attached slaves not asserting PREQ pass a Logic 0 symbol by not driving the bus, so there is no contention if other slaves assert PREQ at the same time.

Fig. 4-24 shows field assignments for each command. Table 4-8 lists similar information, with explanations for each field.

Bit		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Command	Ping	PREQ	OPCODE[2:0] Command owner (Master or Monitor)			—	SSP Master Only	BREQ Attached monitor	BREL Master Only	SlvStat_11[1:0] Slave 11		SlvStat_10[1:0] Slave 10		SlvStat_9[1:0] Slave 9		SlvStat_8[1:0] Slave 8	
	Read					DevAddr[3:0] Command owner (master or monitor)				RegAddr[15:8] Command owner (master or monitor)							
	Write																
	Reserved		Five reserved opcodes			—											

Bit		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Command	Ping	SlvStat_7[1:0] Slave 7		SlvStat_6[1:0] Slave 6		SlvStat_5[1:0] Slave 5		SlvStat_4[1:0] Slave 4		StaticSync[7:0] (Master Only)							
	Read	RegAddr[7:0] Command Owner (Master or Monitor)															
	Write									1	0	1	1	0	0	0	1
	Reserved	—															

Bit		32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
Command	Ping	PHY_SYNC (Master Only) 0	SlvStat_3[1:0] Slave 3		SlvStat_2[1:0] Slave 2		SlvStat_1[1:0] Slave 1		SlvStat_0[1:0] Slave 0		DynamicSync[3:0] (Master Only)				Parity Master or Monitor	NAK Master, Slave, or Monitor	ACK Master, Slave, or Monitor
	Read		RegData[7:0] Addressed Slave(s)														
	Write		RegData[7:0] Command Owner (Master or Monitor)														
	Reserved		—														

Figure 4-24. Control Word Bit Assignments

Bit 0 is the first bit transferred in the bit stream. If a field spans multiple bit slots, the most significant bit is sent first. For example, in Fig. 4-24, OPCODE[2] corresponds to Bit 1 (bit slot[1,0]), OPCODE[1] corresponds to Bit 2 (bit slot[2,0]), and so on.

The monitor arbitrates for control of some fields of the command using the BREQ bit slot, which allows it to become the current command owner. The master acknowledges that it is giving up the bus through the BREL bit slot. The modified NRZI scheme ensures that, if neither the master nor monitor drive the command, the data pin is unchanged, causing OPCODE to be read as 000 (the Ping command). If the monitor drops off or releases the bus, it results in a frame with a Ping command but no BREQ; the master should react by regaining control on the next frame. The slave is not involved with, and is unaffected by, the identity of the command owner.

Table 4-8 describes control-word bit slot fields.

Table 4-8. Control Word Bit Slot Fields

Field	Command	Bit Slot Owner	Description
PREQ	All	All attached slaves	Any attached slave can assert a ping request during this bit slot to notify the master of interesting status in Slv_Stat_x[1:0]. The master must perform a Ping command within 32 frames of the request.
OPCODE[2:0]	All	Command owner	Identifies the type of command. Values not shown are reserved. 000 Ping 010 Read 011 Write
BREQ	Ping	Monitor	Bus request from monitor requesting ownership of command fields in subsequent frames
BREL	Ping	Master	Bus release from master acknowledging that monitor has ownership of command fields in subsequent frames.
SSP	Ping	Master	Stream synchronization point. Setting SSP forces all active ports to synchronize their sample interval counters to the SoundWire frame boundary.
SlvStat_x[1:0] (X = 0–11)	Ping	Slave with DevID = X	Each slave has a unique 2-bit field to report status. 00 Slave not present or not attached. 01 Slave attached but not in an interrupt condition. 10 Slave attached and in an interrupt condition. 11 Reserved
DevAddr[3:0]	Read/ Write	Command owner	Device address identifying which master or slaves are being accessed by the command, 0 Devices first attach as Device 0 1–11 Enumerated slaves are assigned a value in the range 12–13 Slaves can be programmed to also respond to these group addresses. 14 Reserved 15 Group alias to all slaves on the bus.

Table 4-8. Control Word Bit Slot Fields *(Cont.)*

Field	Command	Bit Slot Owner	Description
RegAddr[15:0]	Read/ Write	Command owner	Register address identifying which register is being accessed by the command. Bits 14:0 contain the address. Section 4.8.9 describes how RegAddr is formed.
RegData	Read	Addressed slave	Register data sent from the addressed device (slave or master) to command owner (master or monitor)
RegData	Write	Command owner	Register data sent from command owner (master or monitor) to the addressed device (slave or master)
StaticSync	All	Master	Fixed pattern 1011_0001 that facilitates the slave synchronizing to the bit stream and determining frame shape.
PhySync	All	Master	Identifies whether the physical layer interface is running in Basic PHY or High PHY Mode. 0 Basic PHY This device supports only Basic PHY. 1 High PHY
DynamicSync[3:0]	All	Master	Cyclic pattern that facilitates the slave synchronizing to the bit stream and determining frame shape.
PAR	All	Command owner	Parity checksum generated by the owner of the command fields (master or monitor), checked by the other interfaces (slave, and monitor or master).
NAK	All	All attached devices	Negative acknowledge
ACK	All	All attached devices	Positive acknowledge

4.8.4 Register Access Response

The SoundWire slave provides a response to each command in the Control Word NAK and ACK fields. A component of the response is derived from the result of the register access command, as listed in Table 4-9.

Table 4-9. Command Response

Command Response (Priority Order)	NAK	ACK	SoundWire Address Range (RegAddr[15:0])	Conditions
COMMAND_ FAIL	1	0	All	• Parity error • A bus clash is detected in the Control Word, except for shared bits: PREQ, NAK, ACK, and shared group read data or slave status (when DevAddr = {0,12,13,15}) where bus clash is expected and not reported.
			0x1000–0xFFFF	• APB bridge access is rejected because the bridge was busy with a previous access and could not accept a new one. Section 4.8.12 describes the APB. **Note:** This behavior is not compliant with the *The MIPI SoundWire Specification 1.0.*
COMMAND_ IGNORED	0	0	All	• Slave is not attached to the SoundWire Bus. • Response to a Ping command • Response to reserved opcodes • Response to Read/Write command whose DevAddr value does not address this slave
			0x0000–0x0FFF	• Access to an address where no register is implemented, including any register address associated with the unimplemented data ports (Ports 4–14). • Read from address containing only write-only register bits. • Write to address containing only read-only register bits • Read from Port 15 group alias • Read of any slave control port (SCP) device ID register if the slave is out of enumeration • Write to the SCP device number register if the slave is out of enumeration
COMMAND_ OK	0	1	0x0000–0x0FFF	• A read or write access to an existing register is not constrained by the conditions above
			0x1000–0xFFFF	• An APB bridge access was accepted and a COMMAND_OK response acknowledges that the internal memory access has begun. This response does not convey whether the access was to an implemented address or whether the address is valid for the command. **Note:** For accesses within the range 0x1000–0x1FFF, the COMMAND_OK response is specific to the CS42L42. *The MIPI SoundWire Specification 1.0* requires a COMMAND_ IGNORED response to be returned instead of the COMMAND_OK.

A command response to register access restrictions does not depend on the data value being written, but is governed by whether the read or write access is allowed to that address. Writing an unsupported value to a register address does not cause the write command to be rejected. If multiple entries of Table 4-9 apply to the same SoundWire frame, any condition that triggers a COMMAND_FAIL overrides a COMMAND_IGNORED or COMMAND_OK. Conditions that trigger a COMMAND_IGNORED override conditions that trigger COMMAND_OK.

4.8.5 Frame Synchronization

On initialization, the CS42L42 is unattached, makes no assumptions about frame size, does not react to control words, and does not drive values on the data pin. Instead, it performs a search for the static and dynamic sync words within the control word to determine the size of the frame and identify the frame boundaries before attaching to the SoundWire bus.

When synchronization is confirmed, the CS42L42 attaches to the SoundWire bus with device number = 0 and waits for the master to perform the slave enumeration sequence to assign a unique nonzero device number.

If attached to the SoundWire Bus, the CS42L42 constantly monitors the static and dynamic synchronization words of each frame to verify it is still in sync with the bus. If the CS42L42 detects two bit errors in the synchronization words within two SoundWire frames, it drops off the SoundWire bus and becomes unattached. The device then restarts its frame synchronization search to resynchronize to the SoundWire bus.

4.8.6 Slave Enumeration

The CS42L42 initially attaches to the bus with a device number of zero (Slave0). Because multiple slaves can do so simultaneously, the master must perform an enumeration process to assign each a unique nonzero device number before the slave can be used.

The master determines that a slave has attached as Slave0 through the SlvStat_0 control word status bits. The master then begins reading the six slave control port (SCP) device ID registers in sequence (0x0050–0x0055). To account for possible multiple CS42L42 devices on the same bus, the AD0 and AD1 pins respectively determine the Instance ID bits [1:0] for each device. Note that AD0/AD1 pin values are latched on reset. Enumeration relies on the modified-NRZI bus property that one slave's Logic 1 overrides another slave's Logic 0 on the data bus. If a Slave0 detects a bus clash where its read data value of Logic 0 was overridden by another slave's Logic 1, it drops out of this enumeration sequence. At the end of the sequence, only one slave remains, to which the master assigns a unique, nonzero device number.

Slave0 devices that fell out of the enumeration sequence do not respond to the attempt to set a device number until after a new sequence begins, starting with a read of the SCP device ID 0 register. Slaves out of enumeration also do not respond to reads of the device ID registers.

After a slave is enumerated, and if SlvStat_0 indicates remaining attached slaves, the master should repeat the sequence to enumerate remaining slaves.

4.8.7 Payload Transport

This section describes how payload data is organized within a SoundWire frame and the control registers that define where each port's payload data is located in the frame. Fig. 4-25 shows examples of how the data is positioned.

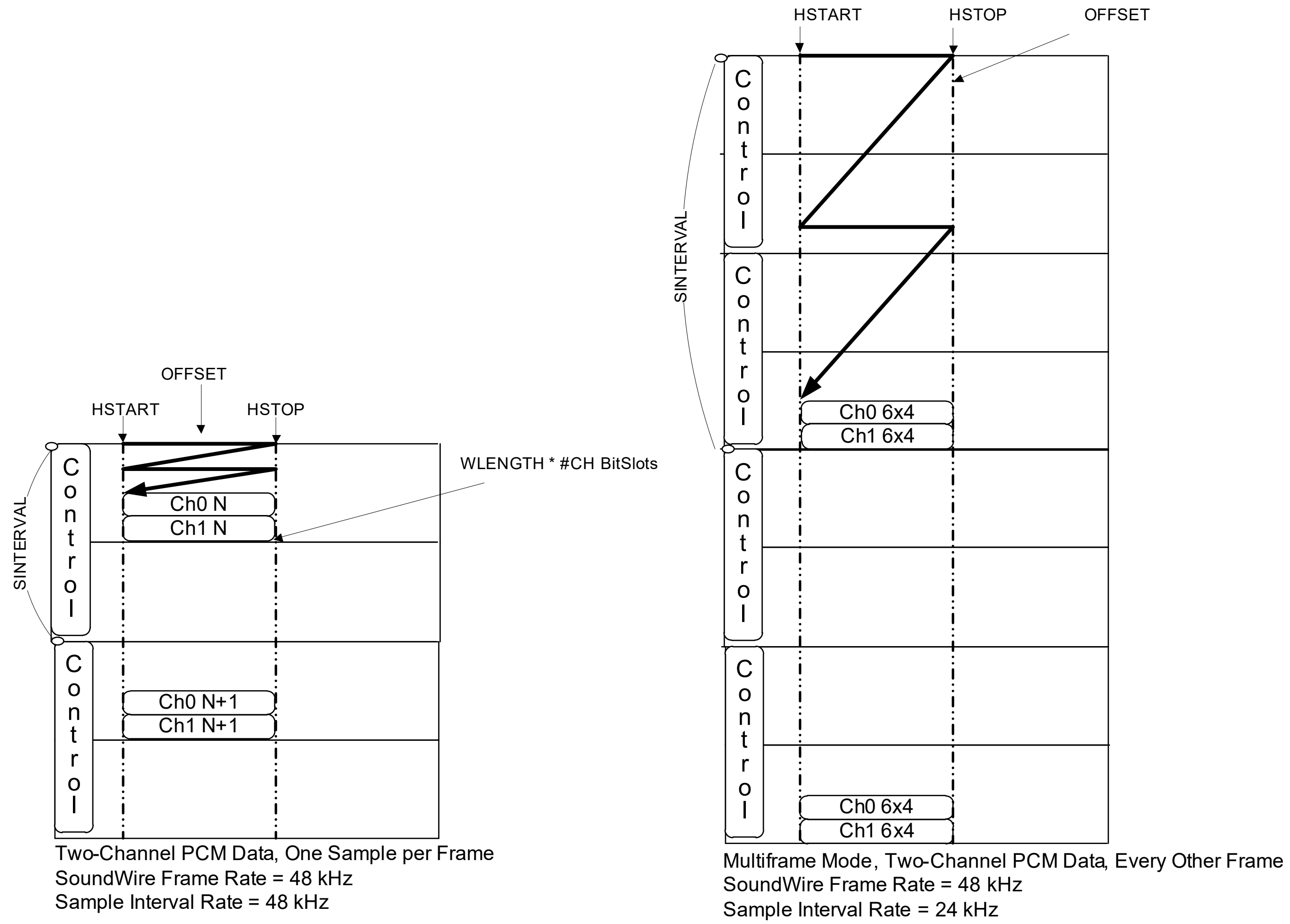


Figure 4-25. Examples of Register Settings Defining a Port's Payload Data Location

Basic parameters in Fig. 4-25 include the following:

- SINTERVAL—Defines the sample interval in units of bit slots.
- HSTART and HSTOP—Define the column boundaries of the transport window.
- OFFSET—Defines the offset in units of bit slots from the start of the transport window where the data is located.
- WORD_LENGTH—Number of bits in each channel minus 1.

Additional parameters are described in the SoundWire register descriptions in Section 7.1 and Section 7.2.

- Payload channel sample—Refers to one sample per channel per sample interval.
- Payload data block refers to blocks of data within a frame, as controlled by BLOCK_PACKING_MODE (see p. 128) and shown in Fig. 4-26:
  - — Blocks-per-Channel Mode—Each payload data block contains one channel sample. There may be multiple payload data blocks per frame, each containing a sample from a different channel.
  - — Blocks-per-Port Mode—One block for the port in the frame contains all the port's channel samples concatenated.

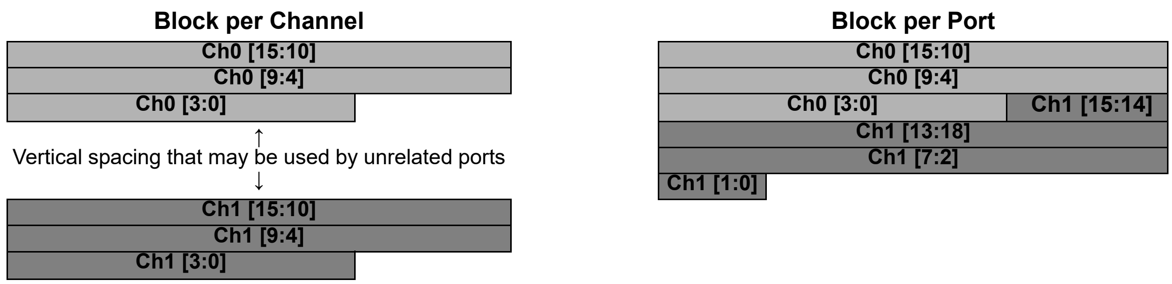


Figure 4-26. Block Packing Mode

- Payload window—A contiguous set of columns in the frame, within which data is transferred for the respective port defined by the HSTART/HSTOP fields. Transport windows may overlap, with different data streams transferred in different bit slots.

  The payload subwindow is the subset of a payload window where the port's data resides, as controlled by the block-spacing mode.
- There are two types of payload data:
  - — Normal payload (isochronous payload streams)
  - — Flow-controlled (asynchronous payload streams)—Not supported on the CS42L42.

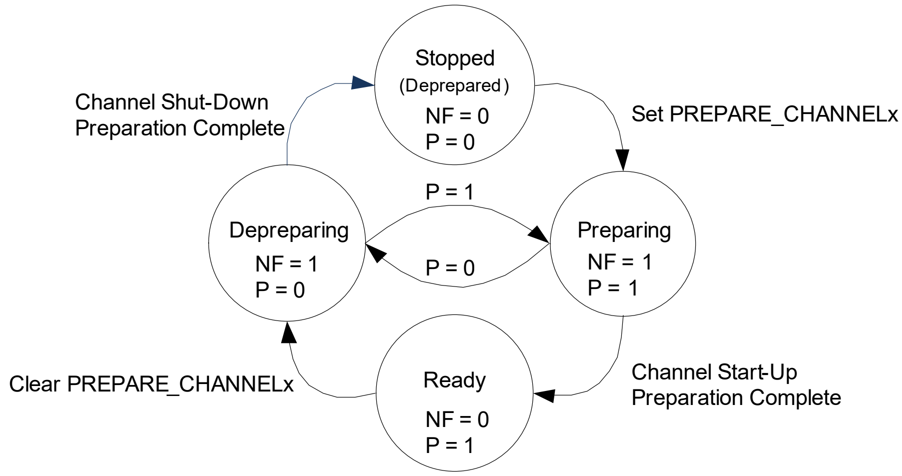
4.8.8 Prepare/Enable Control

The programming model of the state diagram of Fig. 4-27 must be followed to enable each channel within a port. This requires the following procedure to enable the channel:

1. The master first prepares a channel by setting the channel's PREPARE_CHANNELx register bit (see p. 126).

   If the channel is running and ready to transfer data on the SoundWire bus, data-path logic within the chip sets the input port STAT_PORT_READY (see p. 124). This value is reflected in the DPn prepare status register (see p. 126).
2. The master waits until it reads the corresponding NOT_FINISHED_CHANNELx status bit (see p. 126) as cleared.
3. The master sets the CHANNEL_ENx bit (see p. 126) of the inactive bank.
4. Master initiates a bank switch to enable the channel set in Step 3 by writing to the inactive bank SCP frame control register.
5. Data transfer on the SoundWire bus begins in the next frame after the bank switch.

It would be invalid programming for the master to set CHANNEL_EN without waiting for the DPn_PREPARE_STATUS bit to indicate that the channel is ready for operation. Operation cannot be guaranteed in this case.



- “NF” is the channel’s NOT_FINISHED status bit (see Section 7.2.5).
- “P” is the channel’s PREPARE_CHANNELx bit (see Section 7.2.6).

Figure 4-27. Prepare/Enable Control

4.8.9 SoundWire Memory Map

The SoundWire protocol specification requires some device-level register address blocks for each control/data port. Each port has a reserved address window, within which some register spaces are defined by the MIPI SoundWire Specification and others are implementation specific.

Table 4-10 lists base addresses for the SoundWire control and data ports implemented on the CS42L42. Table 6-1 shows how the SoundWire register space fits into the CS42L42 register map.

The “Page” value of Table 6-1 maps to the address field (RegAddr[15:0]) of SoundWire read/write commands as follows:

- RegAddr[15] = Context switch between internal SoundWire registers and the non-SoundWire registers accessed using nonzero page values.
  0 = SoundWire register access
  1 = Advanced peripheral bus (APB, or “Page”) register access
- RegAddr[14:8] = 7 LSB bits of the 8-bit “Page” value from Table 6-1 (Page[7:0])
- RegAddr[7:0] = 8-bit register address

For example, to access the register at page = 0x14 and address = 0x02, the SoundWire RegAddr[15:0] would be 0x9402

Table 4-10. Base Addresses for Data Port Registers

Port Number	Port Name	Base Address	Notes
0	Control Port	0x0000	Control and status functions common to the whole slave
1	Data Port 1	0x0100	Control and status functions specific to Data Port 1 (ADC output channel)
2	Data Port 2	0x0200	Control and status functions specific to Data Port 2 (DAC channels)
3	Data Port 3	0x0300	Control and status functions specific to Data Port 3 (S/PDIF input channels)
4–14	Data Ports 4–14	0x0400–0x0EFF	Reserved
15	Data Ports 1–14	0x0F00	Addressing alias used to write to Data Ports 1–14 with a single write command

4.8.10 Register Banking

Some registers in the control and data ports are banked, meaning that there are two copies that can be accessed through different addresses. A bank switch to all SoundWire slaves connected to the master can be performed simultaneously using a device address = 15 group alias in the SoundWire control word.

The banking mechanism allows the SoundWire master to set up new configurations in advance in the inactive register bank and then command all the slaves to change to that configuration simultaneously. This mechanism is required to apply changes simultaneously in frame shape or payload transport configurations to all slave devices on the SoundWire bus.

Changing banked register values in the active bank for some registers can cause unpredictable behavior (e.g., changing payload location in the middle of the frame). When updating banked registers, the bank switch mechanism must be used to apply the changes on the next frame boundary.

4.8.10.1 Bank Switch

Bank switching allows the master to change which of two register banks is active. This mechanism is used to enable channels, change the SoundWire frame size, or rearrange payload data for all slaves and all ports at the same moment. If any ports have a sample interval that spans multiple SoundWire frames, to avoid audio glitches, a bank switch must be applied on a frame boundary that is also a stream-synchronization point (SSP).

The bank change is performed by writing to the SCP frame control register (see Section 7.1.12) in either Bank 0 or Bank 1. It can be performed to all slave devices at once using the DevAddr = 15 group alias in the control word.

The recommended procedure to perform a bank switch while the data port is enabled and streaming is as follows:

1. Update configuration registers in the inactive bank of all active SoundWire ports with new configuration. If a setting must remain the same, the inactive bank register must be programmed to the same value as the active bank.
2. In the frame preceding a normal SSP alignment, using the device address = 15 alias to all SoundWire slaves, write to the inactive bank's SCP frame control register in either Bank 0 or Bank 1. This write causes the bank change to occur on the next SoundWire frame boundary to the bank whose SCP frame control register was written.

4.8.11 SoundWire Data Port Map

Port 0 functions as SCP, which provides control for the slave. Section 6.1 lists each data port's registers, Table 4-10 lists the base addresses. Table 4-11 shows data-port mapping.

Table 4-11. Data Port Mapping

Data Port	Resource	Channel 2	Channel 1
Port 1	ADC	—	Channel A
Port 2	DAC	Channel B	Channel A
Port 3	S/PDIF	Channel B	Channel A

Table 4-12 describes the supported read/write characteristics for SoundWire bit fields.

Table 4-12. Register Bit Types

Type	Abbreviation	Description
Read/Write	R/W	Register value can be read or written by software
Read/Write/Modified	RWM	Register value can be read or written by software, or modified by hardware.
Read Only	R/O	Read-only status register, can be read but not written by software.
Write One to Clear	R/W1C	Status register is cleared by software writing 1 to the bit.
Write Only	W/O	Write-only bits trigger an action when written, but its value cannot be read.

4.8.12 Advanced Peripheral Bus (APB) Bridge Access Procedures

Read/write commands to addresses 0x1000–0xFFFF outside the SoundWire IP pass through a translation bridge to the device's internal APB. The APB protocol and delays through the bridge do not allow the commands to complete within the SoundWire frame for all cases and require special procedures to perform read/write commands to this memory space. A consequence of the delay through the bridge is that register writes to locations outside the SoundWire IP are not aligned to a SoundWire frame boundary. Read-only status registers manage these transfers in the memory-access status and memory-read-last-address registers (see Section 7.1.17 and Section 7.1.20).

If an access is attempted through the bridge before the previous transfer completes (indicated by CMD_IN_PROGRESS = 1, see p. 123), a COMMAND_FAIL response is returned on the SoundWire bus. Otherwise, a COMMAND_OK response is returned to acknowledge any other access through the bridge, regardless of whether the registers exist outside the SoundWire IP.

By default, a timeout occurs after 8 bus cycles. TIMEOUT_CTRL (seep. 124) can be used to extend this period. The period is 0 bus cycles if TIMEOUT_DISABLE (see p. 124) is set. If issues arise in transferring information, unmasking M_LATE_RESP and M_TIMEOUT_ERR (see p. 122) allows timeout conditions to generate the corresponding interrupts.

Section 4.8.12.2 and Section 4.8.12.3 describe procedures for accessing registers outside the SoundWire IP. These apply only to access to registers above address 0x1000. SoundWire registers within the address range 0x0000–0x0FFF can be accessed directly without special procedures.

4.8.12.1 Indirect versus Direct Access Procedures

Depending on system configuration, there are two ways of access through the APB master. Both add access latency:

- Indirect access: APB read data cannot be returned in time to be part of the control word RegData response field. Read data must be read from MEM_READ_DATA (see p. 124) later, as described in subsequent sections.
- Direct access: APB read data can be returned in time to be included in the RegData response field of the control word. For direct access, no special procedures are required.

Whether an access must use the indirect or direct procedure depends on operating parameters, such as the following:

- The ratio of clock frequencies between the SoundWire and APB clocks. The control port/APB frequency is equal to the $MCLK_{INT}$ frequency.
- Whether any APB slaves add wait cycles to the APB access.
- The number of columns in the SoundWire frame. More columns in the frame allow more time for the APB access to complete in time to return data within a single SoundWire read command.

Indirect access procedures are avoided if the access can be guaranteed to work with direct access. This is possible when the following relation evaluates as TRUE:

Time in SoundWire command between the last Address bit and first RegData bit (10 rows) > Internal time required to process the APB read command (including synchronization delay)

The elements of this relation are calculated as follows:

SoundWire clock period
* 10 Rows
* (Number of columns)/2
>
4.75 SoundWire Clock Periods
\+ 4.25 APB clock periods
\+ APB clock periods clock periods for wait cycles added by APB slave (if needed)

To avoid issues occurring on the edge of the maximum delay, the 0.25 * clock period provides margin.

The number of APB cycles added due to wait states depends on the access desired. The only access requiring extra wait states is the reading and writing of EQ coefficients. For this function, indirect access must be used. However, for all other access functions, no extra APB wait states are required and direct access is allowed. The examples in Table 4-13 show how to use the calculation to determine whether direct access is allowed.

Table 4-13. Direct- and Indirect-Access Comparison

Parameters	Example A Direct Access	Example B Indirect Access—Example A with APB clock frequency halved	Example C Direct Access—Double the columns in Example B	Example D Indirect Access—Example A, APB slave requests wait state	Example E Direct Access—Example D, increasing number of columns
Frame size	48 row x 2 column	48 row x 2 column	48 row x 4 column	48 row x 2 column	48 row x 4 column
Wait state	Always zero wait-state access on APB.	Always zero wait-state access on APB.	Always zero wait-state access on APB.	One wait state might be added to the APB.	One wait state might be added to the APB.
SoundWire clock frequency	SoundWire clock frequency = APB clock frequency.	SoundWire clock frequency = 12 MHz	SoundWire clock frequency = 12 MHz	SoundWire clock frequency = APB clock frequency.	SoundWire clock frequency = APB clock frequency.
APB clock frequency [1]		APB clock = 6 MHz (APB period = 2*SoundWire clock period)	APB clock = 6 MHz (APB period = 2*SoundWire clock period)		
Time for 10 rows to run on SoundWire bus	10*2/2 = 10 SoundWire clock cycles.	10*2/2 = 10 SoundWire clock cycles.	10*4/2 = 20 SoundWire clock cycles.	10*2/2 = 10 SoundWire clock cycles	10*4/2 = 20 SoundWire clock cycles.
Processing time	4.75 + 4.25 = 9	4.75 + 2*4.25 = 13.25	4.75 + 2*4.25 = 13.25	4.75 + 4.25 + 1 = 10	4.75 + 4.25 + 1 = 10
Outcome	Time for 10 rows > processing time.	Time for 10 rows < processing time.	Time for 10 rows > processing time.	Time for 10 rows $\leq$ processing time.	Time for 10 rows > processing time.
Direct access allowed?	Direct access allowed	Not guaranteed; indirect access must be used.	Direct access allowed	Not guaranteed; indirect access must be used.	Direct access allowed

1.The control port/APB frequency is equal to the MCLKINT frequency.

4.8.12.2 Control-Word Write through the APB Bridge

The following procedure for writing data through the APB bridge is required only if indirect access procedures are used. This is not needed if direct access is available.

1. Verify that a prior command is not still active on the bridge by polling the memory access status register (Section 7.1.17) until CMD_IN_PROGRESS = 0.
2. Perform a SoundWire write command via control word to the desired address. The responses are as follows:
   — COMMAND_OK: Acknowledges that the APB transaction was initiated.
   — COMMAND_FAIL: If CMD_IN_PROGRESS = 1, a new write could not be accepted due to a previous command still in progress and a SoundWire command response of COMMAND_FAIL is returned.
3. (Optional) Confirm transaction completion by reading CMD_DONE = 1 (see p. 123).

4.8.12.3 Control-Word Read through the APB Bridge (Indirect Access Only)

This section describes how to read control words if indirect access is used.

A register read requires two read commands because read data cannot be fetched in time for the SoundWire response in the same command. The attempt to read from memory (address above 0x1000) triggers the access to begin across the bridge, while returning an initial response to the SoundWire COMMAND_OK command and a data value of zero.

When the read operation completes, the RDATA_RDY status flag is set (see p. 123), the read data is stored in the memory read data register, and the address from where the data was read is stored in MEM_READ_LAST_ADDR (see p. 124).

Note: This procedure must be an atomic operation; that is, system software must ensure that no other process interrupts. A read or write access to other addresses through the APB bridge during this procedure risks overwriting the read data captured in MEM_READ_DATA (see p. 124).

The following procedure is for reading from a register through the APB bridge:

1. Verify that the bridge is not still active with a previous command by polling the memory access status register until CMD_IN_PROGRESS = 0.
2. Perform the SoundWire read command via control word to the desired address, as normal.
   — The SoundWire command returns response COMMAND_OK to acknowledge the APB transaction was initiated, regardless of whether the register exists.
   — If CMD_IN_PROGRESS = 1, a new read could not be accepted and a SoundWire command response of COMMAND_FAIL is returned.
3. Poll the memory access status to verify the read transaction completed. (CMD_DONE = 1 and RDATA_RDY = 1).
   The address the data was read from is also stored in MEM_READ_LAST_ADDR for optional reference.
4. Read MEM_READ_DATA to return the data last read from the address stored in MEM_READ_LAST_ADDR.

4.8.13 SoundWire Clock Stop Mode and Wake-Up Event

The Clock Stop Mode provides a mechanism allowing the master to shut off the SoundWire clock. The flow to enter Clock Stop Mode is as follows:

1. The CS42L42 does not automatically change any functional states when going through the clock-stop process. As a result, if any function needs to be shut down or reconfigured, the master must first send the appropriate commands to configure the device
   Clear SCLK_PRESENT. When SCLK_PRESENT transitions from 1 to 0, the RCO becomes the system's MCLK. In addition to the plug insertion/removal and S0 button press events,
   Note the following behavior under this condition:
   — To meet the RCO power-up latency requirement, SWIRE_SCLK must remain present for at least 150 µs before entering Clock Stop Mode.
2. The SoundWire master writes to CLOCK_STOP_PREPARE (see p. 119) to begin the shutdown.

3. The SW_CLK_STP_STAT_SEL setting (see p. 133) determines which functional blocks report as powered down before CLOCK_STOP_NOT_FINISHED (see p. 119) is cleared. This ensures that the desired functions within the device are complete before clock stop can proceed.
4. The CS42L42 clears CLOCK_STOP_NOT_FINISHED to indicate it is ready for the clock to be stopped.
5. The master performs a group status read until all slaves report ready for the clock to be turned off (CLOCK_STOP_NOT_FINISHED = 0).
6. The master performs a group write to CLOCK_STOP_NOW (see p. 119), indicating the clock is about to stop.
7. Immediately after Step 6, the master sends a stopping frame. The master owns all payload bits and must drive the data pin on the last bit slot to a physical low level. The CS42L42 does not drive payload bits associated with data ports.
8. The master stops the SoundWire clock at the frame boundary at the end of the stopping frame.

Note: If WAKE_UP_ENABLE = 1 and SW_CLK is stopped, an S0 button press, a headphone plug, or a headphone unplug can cause the SoundWire wake event to occur.

CLOCK_STOP_NOT_FINISHED = 1 indicates that the slave is not ready to be shut off. A value of 0 indicates the slave is ready for the clock to be shut off. This allows for group reads of all slave devices to report whether any slave is not ready for the shutdown due to the modified NRZI encodings.

If WAKE_UP_ENABLE is set (see p. 119) while the SoundWire clock is stopped, the wake event signal is triggered to the master to wake the SoundWire bus. If the wake event occurs in Clock Stop Mode, SWIRE_SD is asserted. After the wake event signal is triggered, SCLK_PRESENT must be set to transition from 0 to 1 (that is, from the internal RCO to the SWIRE_SCLK/PLL). The transition can take 150 µS. If the PLL is used, SCLK_PRESENT must wait for the PLL to settle.

The last opportunity to send an interrupt during a clock-stop sequence is the PREQ of the frame that writes to CLOCK_STOP_NOW. If the internal wake event described previously occurs in either that frame or the stopping frame, the wake event signal is latched and stored. After the clock is stopped at the end of the stopping frame, a SoundWire wake-up event occurs. This ensures that no internal wake event is missed. A wake event is seen by the master as the next PREQ bit.

Fig. 4-28 shows clock-off timing.

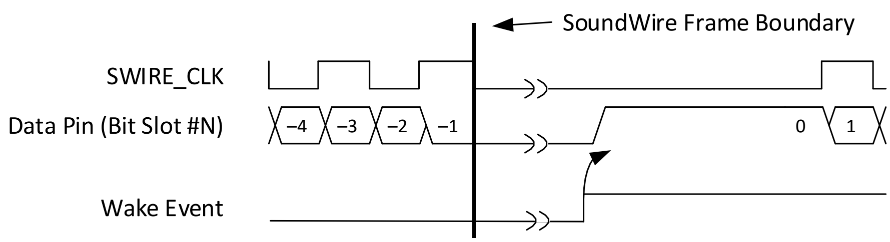


Figure 4-28. Clock Off Timing

4.8.14 Programming Restrictions

The following restrictions must be observed:

- For registers that are banked, operation is not guaranteed when writing to the active bank of a register. The SCP frame control register is the only banked register that supports writes to the active bank.
- Configuration changes must not be done in an on-the-fly method—bank changes must be used.
- To ensure that new register values are not applied in the middle of a sample interval, bank changes must correspond to the SSP.
- Although the MIPI specification allows the master to assert an SSP at any time, the CS42L42 does not allow the assertion if the sample interval ends in the next-to-last bit slot of the SoundWire frame such that a new interval would start in the last bit slot of that frame (e.g., preceding the frame boundary where the SSP is applied). This rare scenario could happen in a system where the master and slaves are already out-of-sync and data is already corrupt.
- Nonbanked register fields, PORT_DATA_MODE and WORD_LENGTH, must not be modified if the port is enabled.

4.8.15 Configuration Guidelines with Examples

Ex. 4-3 and Ex. 4-4 describe configurations for programming three data ports for 48- and 96-kHz operations, each with 24-bit data. Data Port 1 has one 24-bit channel; Data Ports 2 and 3 have two channels each. Fig. 4-29 shows the resulting frame structure, with details for each port (HSTART, HSTOP, OFFSETS, and WORD_LENGTH). For each data port, registers are programmed to indicate the location in the SoundWire frame where each payload data is stored. Each port must be configured with a location such that its payload location does not overlap another port. The SoundWire master must also be configured with the same settings for each port.

	Example 4-3. Sample Interval Rate: 48 kHz			Example 4-4. Sample Interval Rate: 96 kHz		
Parameter	Data Port 1	Data Port 2	Data Port 3	Data Port 1	Data Port 2	Data Port 3
WORD_LENGTH [1]	23	23	23	23	23	23
HSTART	1	1	1	1	1	1
HSTOP	7	7	7	7	7	7
OFFSET1	0	28	84	0	28	84
OFFSET2	0	0	0	0	0	0
Offset (combined)	0	28	84	0	28	84
SAMPLE_INTERVAL_LOW	255	255	255	255	255	255
SAMPLE_INTERVAL_HIGH	1	1	1	0	0	0
Sample Interval	512	512	512	256	256	256

1.WORD_LENGTH is the number of bits in each channel minus 1.

Both examples have the same configuration—SoundWire clock = 12.288 MHz, 64 rows, 8 columns, 512 bits per frame, SoundWire frame rate = 48 kHz.

Configuration details are summarized in Ex. 4-3 and Ex. 4-4.

The WORD_LENGTH is the number of bits minus 1 in each channel's sample per port.

The HSTART and HSTOP values define the payload transport window, the columns in the SoundWire frame that bound the port's payload data. Both examples set HSTART = 1 and HSTOP = 7, so that the payload data is in Columns 1–7. To avoid overlap with the control word, Column 0 is not included.

The OFFSETx fields define the number of bits within the payload transport window that the start of the sample is delayed from the sample interval boundary. Each port has a different offset to avoid overlap. Note that this example uses the Block-per-Port Mode. The definition of the offset registers would change if Block-per-Channel Mode were used.

Although spaces appear between each port's payload, shown in different colors in Fig. 4-29, that spacing is not required.

Both examples start with the SoundWire frame rate set to 48 kHz. Using a 12.288-MHz SoundWire clock, a 64 x 8 frame yields a 48-kHz SoundWire frame rate. Setting the sample interval (the time in units of bit slots defining the rate at which the port's data samples are transferred) to match the SoundWire frame rate, as shown in Ex. 4-3, yields a 48-kHz sample interval. There are two bit slots per SoundWire clock cycle. Other sample interval rates can be multiplied or divided from this sample rate without changing the same SoundWire frame rate.

Note the following:

- The sample interval and the frame can have different lengths.
- The sample interval must be a multiple or divide factor from the SoundWire frame length. Note that this does not have to be an integer multiple, but rather a common multiple, where periodically the SoundWire frame boundary aligns to the sample interval boundary. The SSP is the point at which all sample interval boundaries of all ports in the system align to the same SoundWire frame boundary.
- Each port can have a different sample interval.

The sample interval is calculated in units of bit slots according to the following formula:

Sample Interval = 256 * SAMPLE_INTERVAL_HIGH + SAMPLE_INTERVAL_LOW + 1.

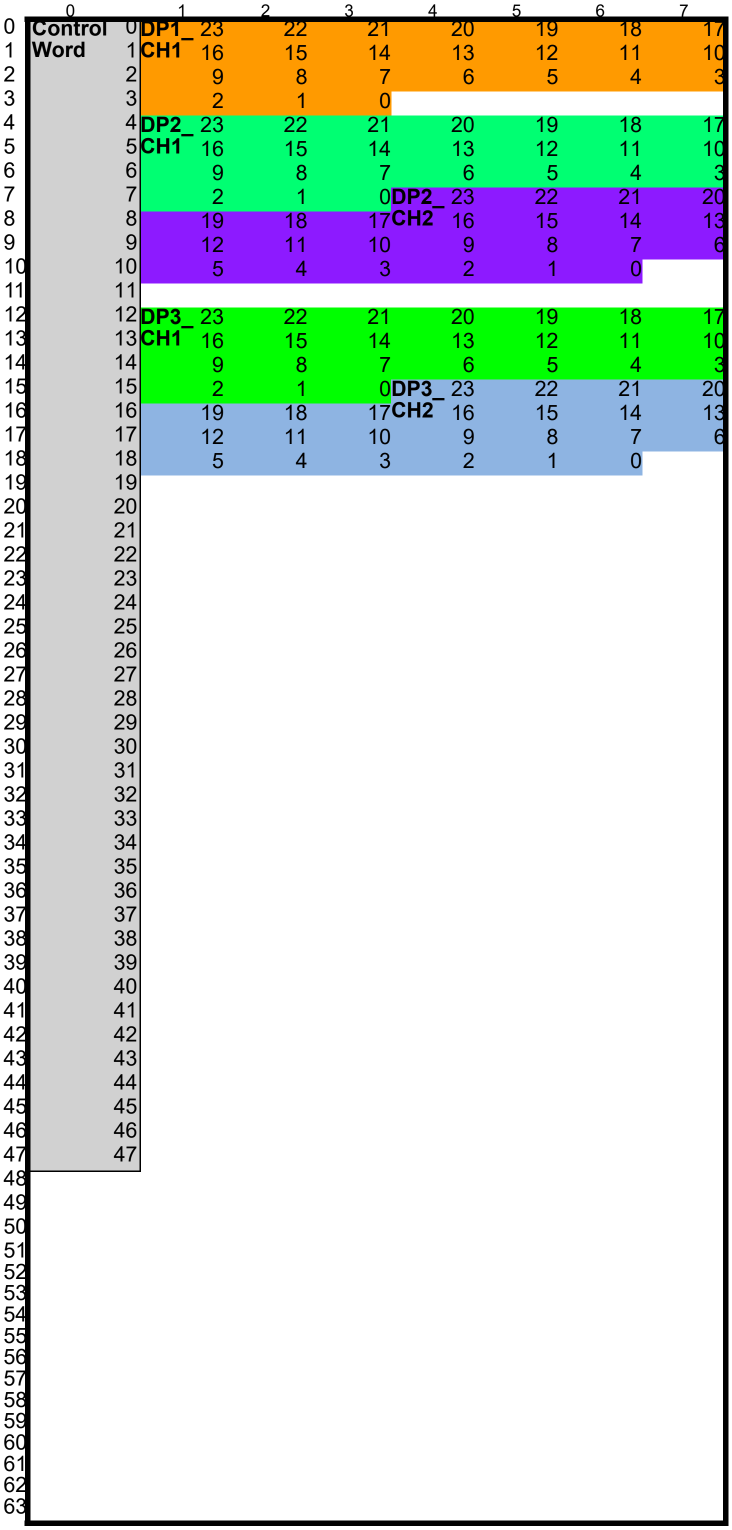
Setting SAMPLE_INTERVAL_HIGH = 1 and SAMPLE_INTERVAL_LOW = 255 results in a sample interval for a 48-kHz frame at 12.288 MHz of 512 bit slots. Note that this also coincides with a frame size of 64 x 8 = 512.

Table 4-14 describes using different sample intervals with SoundWire frame rate of 48 kHz:

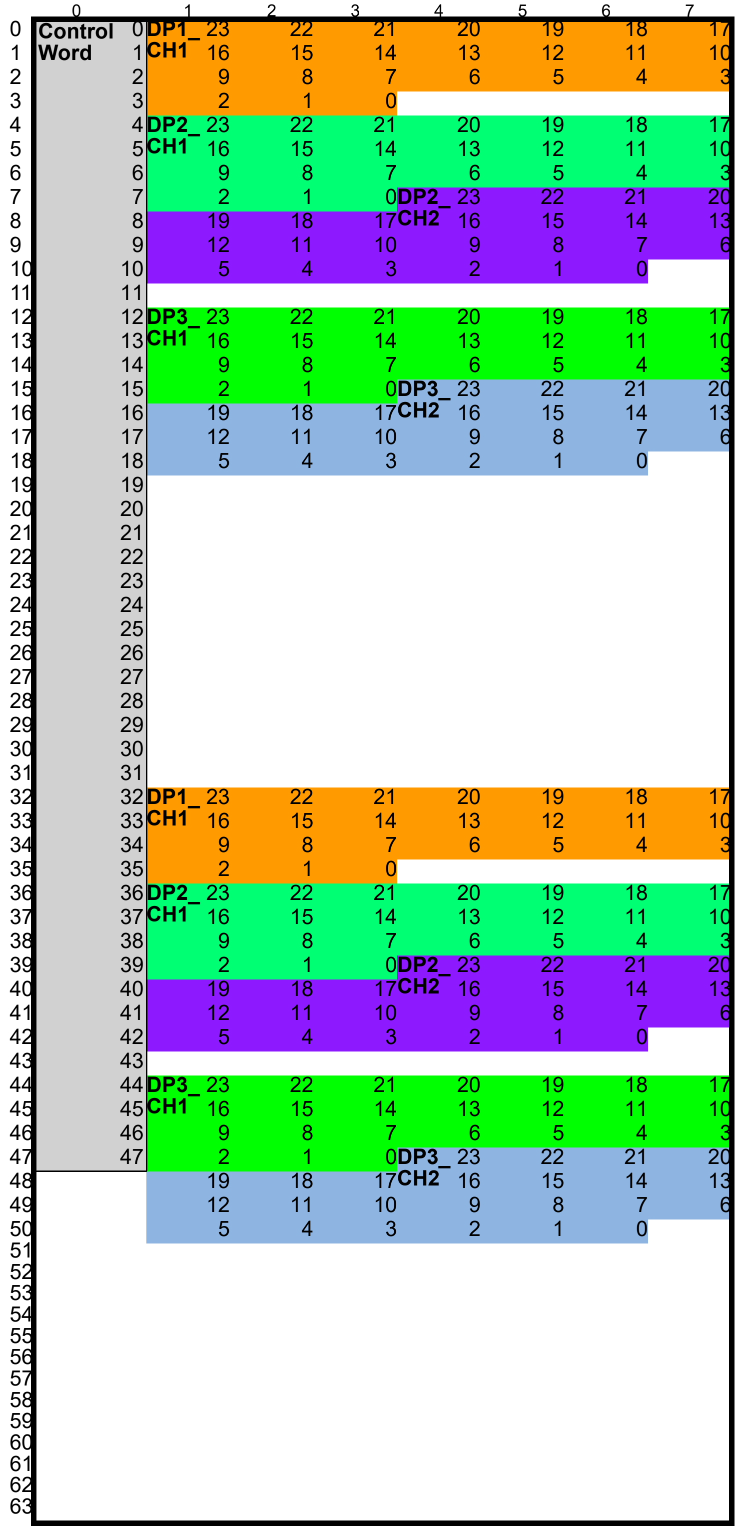
Table 4-14. Sample interval/Sample Rate Examples

Sample Interval	Sample Rate
Length of the SoundWire frame	48-kHz sample rate with one sample for each channel per frame.
Half the SoundWire frame length	Two samples per frame for a 96-kHz sample rate. (see Ex. 4-4)
Twice the SoundWire frame length	One sample every second frame for a 24-kHz rate.
N times the SoundWire frame length	One sample every Nth frame, generating a 48/N-kHz rate. 8 kHz is the minimum rate for the CS42L42.

Running all ports with 44.1 kHz requires a different SoundWire clock or frame shape that matches 44.1 kHz along with adjusting other parameters accordingly. An 11.2896-MHz SoundWire clock with a 64 x 8 frame shape works well with a frame rate of 44.1 kHz. Note that this does not apply to isochronous streams, which are converted to 48 kHz before being sent to the SoundWire block.



Ex. 4-3: 48-kHz Sample Interval Rate



Ex. 4-4: 96-kHz Sample Interval Rate

Figure 4-29. Configuration Examples for a 64 x 8 SoundWire Frame—SoundWire Frame Visualization

4.9 Audio Serial Port (ASP)

The CS42L42 has an ASP to communicate audio and voice data between system devices, such as application processors and Bluetooth transceivers. ASP_SCLK_EN (see p. 139) must be set whenever DAO and DAI are used. The ASP can be configured to TDM, I2S, and left justified (LJ) audio interfaces.

Note: A maximum of four input channels and two output channels are supported in TDM Mode. Any two input channels can be mapped to SPDIF TX, and they always bypass the ASRC.

Although two output channels exist, the information from Channel 1 is replicated onto Channel 2 when enabled (ASP_TX_CH2_EN, p. 164). As a result, Channel 2 can be used only if Channel 1 is used. This is targeted for 50/50 use, but can be used in any transmit situation. Bit resolution must be the same for both channels (ASP_TX_CH2_RES = ASP_TX_CH1_RES) along with matching MSB/LSB bit starts (ASP_TX_CH2_BIT_ST_MSB = ASP_TX_CH1_BIT_ST_MSB and ASP_TX_CH2_BIT_ST_LSB = ASP_TX_CH1_BIT_ST_LSB).

However, in 50/50 Mode, the active phase for each channel must not match (ASP_TX_CH2_AP ≠ ASP_TX_CH1_AP).

4.9.1 Slave Mode Timing

The ASP can operate as a slave to another device's timing, requiring ASP_SCLK/SWIRE_CLK and ASP_LRCK/FSYNC to be mastered by the external device. If ASP_HYBRID_MODE is cleared (see p. 139), the serial port acts as a slave. If ASP_HYBRID_MODE is set, the port is in Hybrid-Master Mode (see Section 4.9.2).

In Slave Mode, ASP_SCLK and ASP_LRCK are inputs. Although the CS42L42 does not generate interface timings in Slave Mode, the expected LRCK and SCLK format must be programmed as it is in Hybrid-Master Mode. Table 4-17 shows supported serial-port sample rate examples. Note that some rates require use of the PLL and/or SRC.

4.9.2 Hybrid-Master Mode Timing

In Hybrid-Master Mode, ASP_LRCK is derived from ASP_SCLK; the ASP_SCLK/ASP_LRCK ratio must be N x F_S, where N is a large enough integer to support the total number of bits per ASP_LRCK period for the audio stream to be transferred. In either 50/50 Mode or I2S/LJ Mode, the ASP_SCLK/ASP_LRCK ratio must be N_E x F_S, where N_E is an even integer.

The serial port generates an internal LRCK/FSYNC from an externally mastered ASP_SCLK/SWIRE_CLK, allowing single clock-source mastering to the CS42L42. In Hybrid-Master Mode, the serial port must provide a left-right/frame sync signal (ASP_LRCK/FSYNC) given an externally generated bit clock (ASP_SCLK).

Table 4-15 shows supported serial-port sample-rate examples. Other rates are possible, but the rules stipulated above must be met. Note that some rates require use of the PLL or SRC.

Table 4-15. Supported Serial-Port Sample Rates

SCLK Frequency (MHz)	Serial Port Sample Rate (kHz)																	
	8.0	11.025	11.029	12	16	22.05	22.059	24	32	44.1	44.118	48	88.2	88.235	96	176.4	176.471	192
1.4112	—	x	—	—	—	x	—	—	—	x	—	—	x	—	—	x	—	—
2.8224	—	x	—	—	—	x	—	—	—	x	—	—	x	—	—	x	—	—
5.6448	—	x	—	—	—	x	—	—	—	x	—	—	x	—	—	x	—	—
11.2896	—	x	—	—	—	x	—	—	—	x	—	—	x	—	—	x	—	—
22.5792	—	x	—	—	—	x	—	—	—	x	—	—	x	—	—	x	—	—
1.024	x	—	—	—	x	—	—	—	x	—	—	—	—	—	—	—	—	—
2.048	x	—	—	—	x	—	—	—	x	—	—	—	—	—	—	—	—	—
4.096	x	—	—	—	x	—	—	—	x	—	—	—	—	—	—	—	—	—
8.192	x	—	—	—	x	—	—	—	x	—	—	—	—	—	—	—	—	—
2	x	—	—	—	x	—	—	—	—	—	—	—	—	—	—	—	—	—
3	x	—	x	x	—	—	x	x	—	—	x	—	—	x	—	—	x	—
4	x	—	—	—	x	—	—	—	x	—	—	—	—	—	—	—	—	—
6	x	—	x	x	x	—	x	x	—	—	x	x	—	x	—	—	x	—
12	x	—	x	x	x	—	x	x	x	—	x	x	—	x	x	—	x	—
24	x	—	x	x	x	—	x	x	x	—	x	x	—	x	x	—	x	x
1.536	x	—	—	x	x	—	—	x	x	—	—	x	—	—	x	—	—	x
3.072	x	—	—	x	x	—	—	x	x	—	—	x	—	—	x	—	—	x

Table 4-15. Supported Serial-Port Sample Rates

SCLK Frequency (MHz)	Serial Port Sample Rate (kHz)																		
	8.0	11.025	11.029	12	16	22.05	22.059	24	32	44.1	44.118	48	88.2	88.235	96	176.4	176.471	192
6.144	x	—	—	x	x	—	—	x	x	—	—	x	—	—	x	—	—	x
12.288	x	—	—	x	x	—	—	x	x	—	—	x	—	—	x	—	—	x
24.576	x	—	—	x	x	—	—	x	x	—	—	x	—	—	x	—	—	x
9.6	x	—	—	x	x	—	—	x	x	—	—	x	—	—	x	—	—	x
19.2	x	—	—	x	x	—	—	x	x	—	—	x	—	—	x	—	—	x

Fig. 4-30 and Fig. 4-31 show the serial-port clocking architectures.

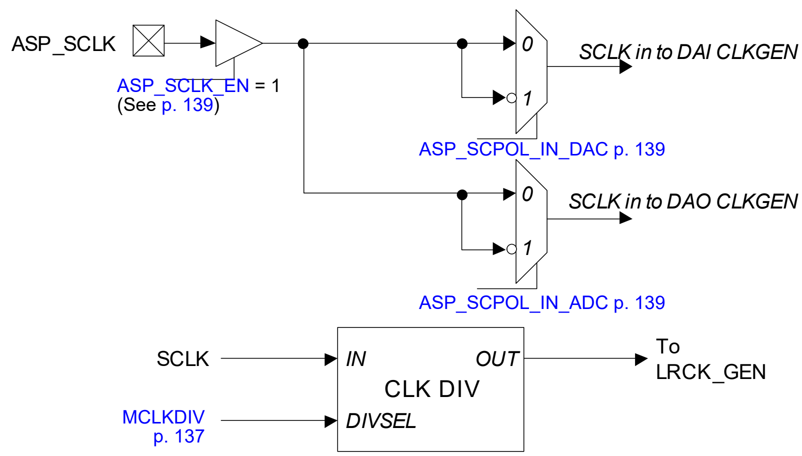


Figure 4-30. ASP SCLK Architecture

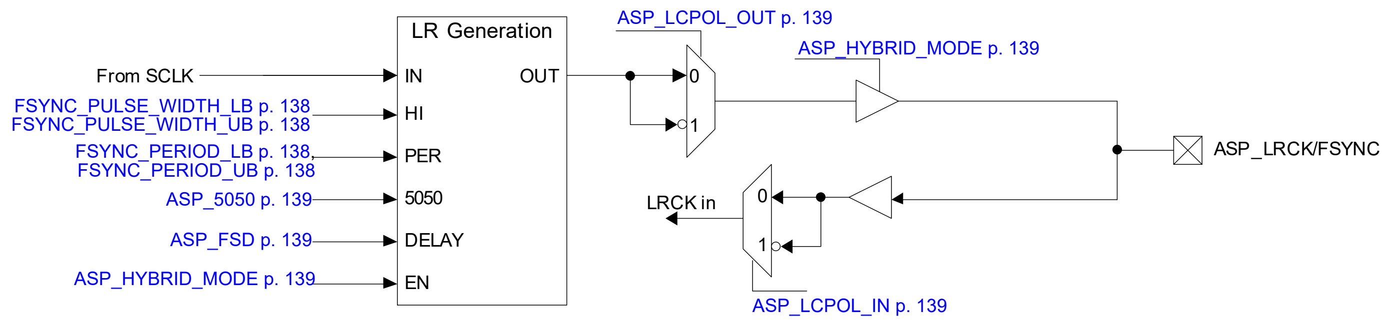


Figure 4-31. ASP LRCK Architecture

As shown in Fig. 4-32, the LRCK period (FSYNC_PERIOD_LB and FSYNC_PERIOD_UB, see p. 138) controls the number of SCLK periods per frame. This effectively sets the frame length and the number of SCLK periods per Fs. Frame length may be programmed in single SCLK period multiples from 16 to 4096 SCLK:Fs. If ASP_HYBRID_MODE (see p. 139) is set, the SCLK period multiples must be set to 2 * n * Fs, where $n \in \{8, 9, \ldots, 2048\}$.

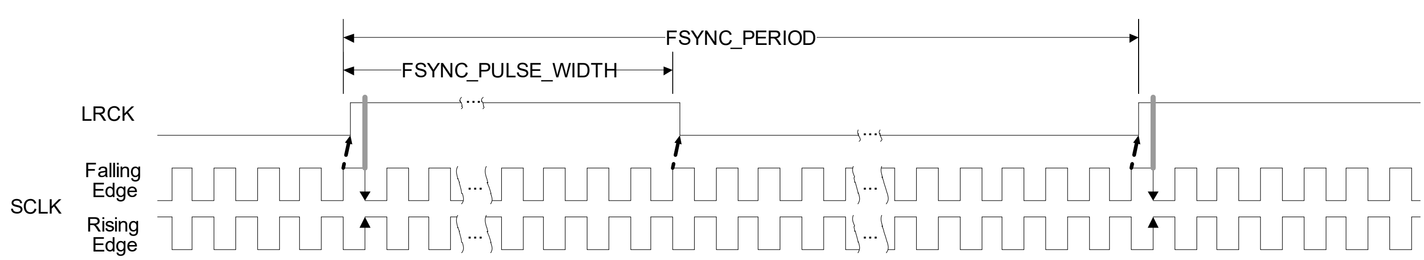


Figure 4-32. ASP LRCK Period, High Width

FSYNC_PULSE_WIDTH_LB and FSYNC_PULSE_WIDTH_UB (see p. 138) control the number of SCLK periods for which the LRCK signal is held high during each frame. Like the LRCK period, the LRCK-high width is programmable in single SCLK periods, from at least one period to at most the LRCK period minus one. That is, the LRCK-high width must be shorter than the LRCK period.

As shown in Fig. 4-33, if 50/50 Mode is enabled (ASP_5050 = 1, see p. 139), the LRCK high duration must be programmed to the LRCK period divided by two (rounded down to the nearest integer when the LRCK period is odd). When the serial port is in 50/50 Mode, setting the LRCK high duration to a value other than half of the period causes erroneous operation.

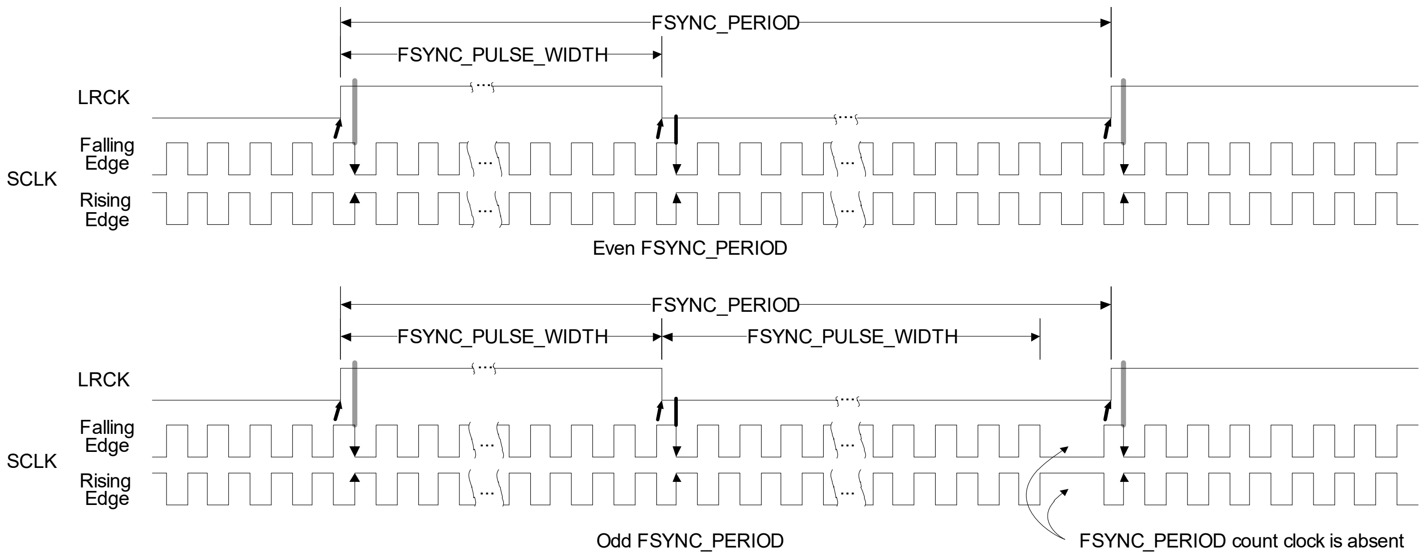


Figure 4-33. ASP LRCK Period, High Width, 50/50 Mode

Fig. 4-34 shows how LRCK frame start delay (ASP_FSD, see p. 139) controls the number of SCLK periods from LRCK synchronization edge to the start of frame data.

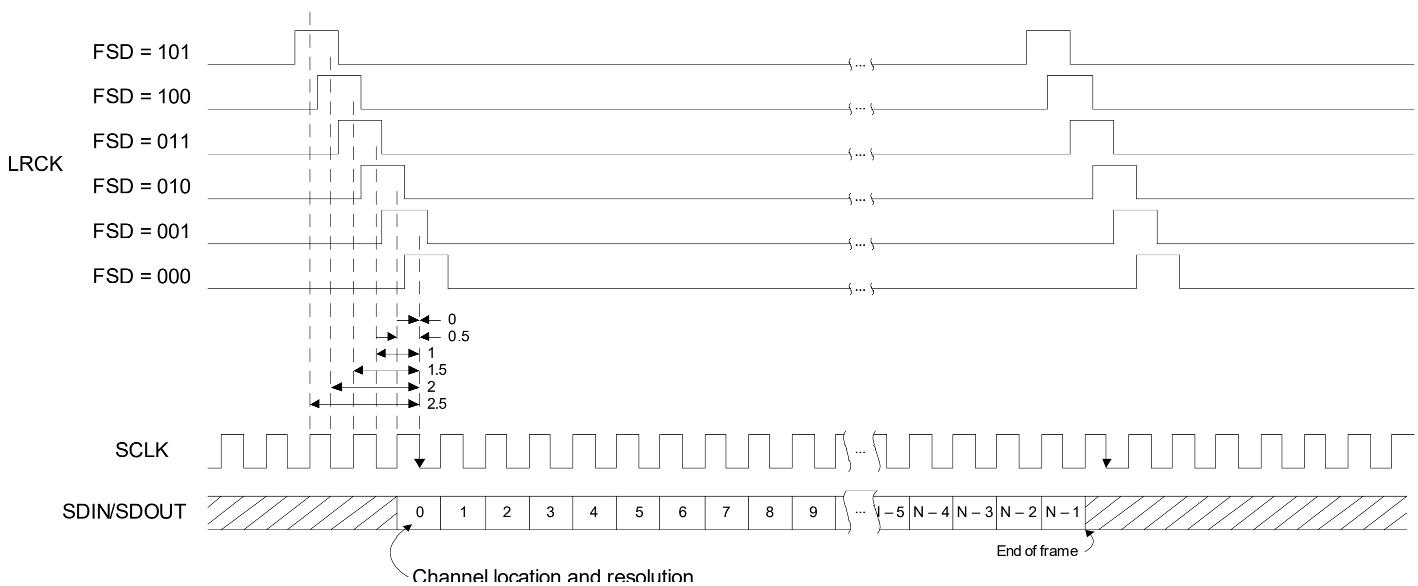


Figure 4-34. LRCK Frame-Start Delay Example Diagram

4.9.3 Channel Location and Resolution

Each serial-port channel's location and offset is configured through the registers in Table 4-16. Location is programmable in single SCLK-period resolution. If set to the minimum location offset, a channel sends or receives on the first SCLK period of a new frame. Channel size is programmable in 8- to 32-bit byte resolutions. Note that only the S/PDIF port transmits up to 32 bits. ADC and DAC ports are limited to 24 bits and truncate the 8 LSBs of a 32-bit audio stream.

Table 4-16. ASP Channel Controls

Channel	Resolution	MSB Location	LSB Location
ASP Transmit Channel 1	ASP_TX_CH1_RES	ASP_TX_BIT_CH1_ST_MSB	ASP_TX_BIT_CH1_ST_LSB
ASP Transmit Channel 2	ASP_TX_CH2_RES	ASP_TX_BIT_CH2_ST_MSB	ASP_TX_BIT_CH2_ST_LSB
ASP Receive DAI0 Channel 1	ASP_RX0_CH1_RES	ASP_RX0_CH1_BIT_ST_MSB	ASP_RX0_CH1_BIT_ST_LSB
ASP Receive DAI0 Channel 2	ASP_RX0_CH2_RES	ASP_RX0_CH2_BIT_ST_MSB	ASP_RX0_CH2_BIT_ST_LSB
ASP Receive DAI0 Channel 3	ASP_RX0_CH3_RES	ASP_RX0_CH3_BIT_ST_MSB	ASP_RX0_CH3_BIT_ST_LSB
ASP Receive DAI0 Channel 4	ASP_RX0_CH4_RES	ASP_RX0_CH4_BIT_ST_MSB	ASP_RX0_CH4_BIT_ST_LSB
ASP Receive DAI1 Channel 1	ASP_RX1_CH1_RES	ASP_RX1_CH1_BIT_ST_MSB	ASP_RX1_CH1_BIT_ST_LSB
ASP Receive DAI1 Channel 2	ASP_RX1_CH2_RES	ASP_RX1_CH2_BIT_ST_MSB	ASP_RX1_CH2_BIT_ST_LSB

Channel size and location must not be programmed such that channel data exceeds the frame boundary. In other words, channel size and offset must not exceed the expected SCLK per LRCK settings. Size and location must not be programmed such that data from a given SCLK period is assigned to more than one channel. However, an exception exists for the DAI as the same data can be used for both received channels' location, if desired. For an example, see Section 5.1.

Fig. 4-35 shows channel location and size with serial-port double-rate disabled. See ASP_RX1_2FS and ASP_RX0_2FS (p. 165).

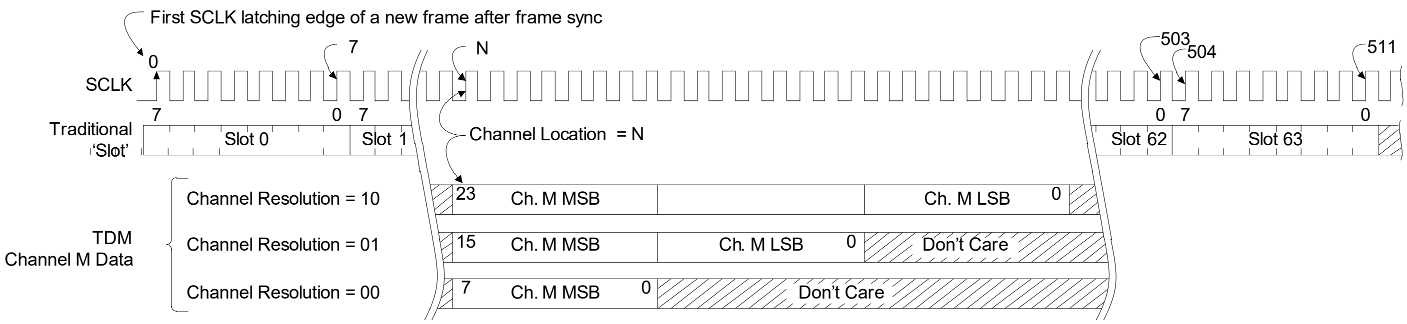


Figure 4-35. Example Channel Location and Size, ASP Double Rate Disabled

4.9.4 Isochronous Serial-Port Operation

In Isochronous Mode, audio data can be transferred between the internal audio data paths and a serial port at isochronous frequencies slower than the LRCK frequency. In all cases, the sample rate/LRCK frequency ratio must be one for which there are points at which rising edges regularly align.

Notes: Combining an isochronous audio stream on a channel (or on multiple channels) concurrently with a native audio stream on another channel (or other multiple channels) is not supported.

The S/PDIF port does not support isochronous audio streams.

In Isochronous Mode, if a stream's sample rate does not match the LRCK frequency, it must include nulls, indicated by the negative full-scale (NFS) code (1 followed by 0s) or by adding nonaudio bits (NSB Mode) to the data stream.

SP_RX_NFS_NSBB and SP_TX_NFS_NSBB (see p. 159 and p. 160) select between the NFS and NSB modes.

In NFS Mode, to achieve a desired isochronous output sample rate, a null-insert block adds NFS samples to the output stream. NFS samples input to the null-insert block are incremented and are passed to the output as valid, nonnull samples.

In NSB Mode, a null-insert block adds 8 bits to the data stream and inserts null samples to achieve a desired isochronous output sample rate. Inserted null samples are defined as NFS including the nonaudio bits. NFS samples that are input to the null-insert block are passed as valid, nonnull samples to the output. Valid samples are indicated by a nonzero value in the null sample indicator bit. The null sample indicator bit is globally defined by the SP_RX_NSB_POS (see p. 159) and SP_TX_NSB_POS (see p. 160). Total data stream sample width, including the nonaudio bits, is N + 8 bits. Therefore, the maximum HD audio sample width is 24 bits in NSB Mode.

In NFS Mode, a null-remove block deletes null samples, restoring the stream's original sample rate. NFS samples that are input to the null-remove block are removed from the data stream as invalid, null samples.

In NSB Mode, a null-remove block deletes samples that have a zero null sample indicator bit, restoring the stream's original sample rate. Furthermore, the output data has the least-significant 8 bits of nonaudio data removed. Samples with a zero null sample indicator bit are removed from the data stream as invalid, null samples.

In either NSB or NFS Mode, setting the Tx and Rx rate fields (SP_TX_FS, see p. 160, and SP_RX_FS, see p. 159) matters only if an isochronous mode is selected via SP_TX_ISOC_MODE (see p. 160) and SP_RX_ISOC_MODE (see p. 159). Supported isochronous rates are 48k, 96k, and 192k. The ASPx Tx/Rx rate bits are used only to help determine when to insert/ nulls and to provide the correct f_{SI}/f_{SO} to the SRCs while in Isochronous Mode.

For null-remove operations, the rates do not need to match the actual data rate. Likewise, if data is being rendered or captured at its native rate, these registers have no effect.

As Fig. 4-36 shows, the null-sample bit (NSB) flag may be any bit of the least-significant sample byte. NSB-encoded streams are assumed to contain 8 bits of nonaudio data as the LSB.

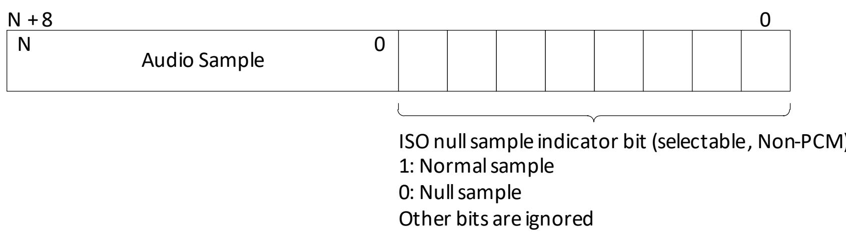


Figure 4-36. NSB Null Encoding

To send isochronous audio data to a serial port, the data pattern must be such that the LRCK/FSYNC transition preceding any given nonnull sample on the 48-kHz serial port does not deviate by more than one sample period from a virtual clock running at the desired sample rate. Use the following example to determine the data word as it appears on the serial port.

```
error = 0
for each LRCK
   if(error < 1/FLRCK)
     output = <<next sample>>
     error = error + (1/Fs - 1/FLRCK)
   else
     output = NULL
     error = error - 1/FLRCK
```

The null-sample sequences in Table 4-17 result from the example above for common sample rates. This method ensures that the internal receive data FIFO does not underrun or overrun, which would cause audio data loss. Depending on the internal audio data FIFOs' startup conditions and on the serial-port clock-phase relationships, isochronous data sent from a serial port may not adhere to the data patterns in Table 4-17. In all cases, the transmitted audio data rate matches the stream sample rate.

Table 4-17. Isochronous Input Data Pattern Examples

Sample Rate (kHz)	Isochronous Data Pattern for LRCK = 48 kHz
8.000	1_S5_N (repeat)
11.025	[[[1s3nx2]1s4n]x5 1s3n1s4n]x4 [[1s3nx2]1s4n]x4 1s3n1s4n [[[1s3nx2]1s4n]x5 1s3n1s4n]x3 [[1s3nx2]1s4n]x4 1s3n1s4n (repeat)
12.000	1_S3_N (repeat)
16.000	1_S2_N (repeat)
22.05	[[1s1nx6]1n [1s1nx6]1n [1s1nx5]1n]x8 [1s1nx6]1n [1s1nx5]1n (repeat)
24.000	1_S1_N (repeat)
32.000	2_S1_N (repeat)
44.100	[12s1n[11s1n]x2]x3 11s1n (repeat)
48.000	1_S (repeat)

Note: $_N$ = Null sample, $_S$ = Normal sample

4.9.5 50/50 Mode

Regardless of the state of ASP_LRCK/FSYNC, in 50/50 Mode (ASP_5050 = 1, see p. 139), the ASP can start a frame.

The ASP_STP setting (see p. 139) determines which LRCK/FSYNC phase starts a frame in 50/50 Mode, as follows:

- If ASP_STP = 0, the frame begins when LRCK/FSYNC transitions from high to low. See Fig. 4-37.

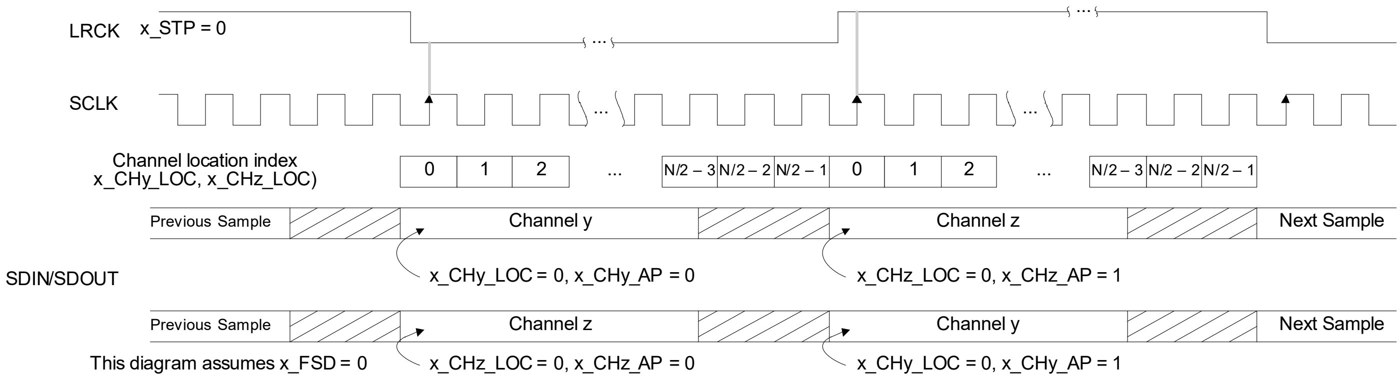


Figure 4-37. Example 50/50 Mode (ASP_STP = 0)

- If ASP_STP = 1, the frame begins when LRCK/FSYNC transitions from low to high. See Fig. 4-38.

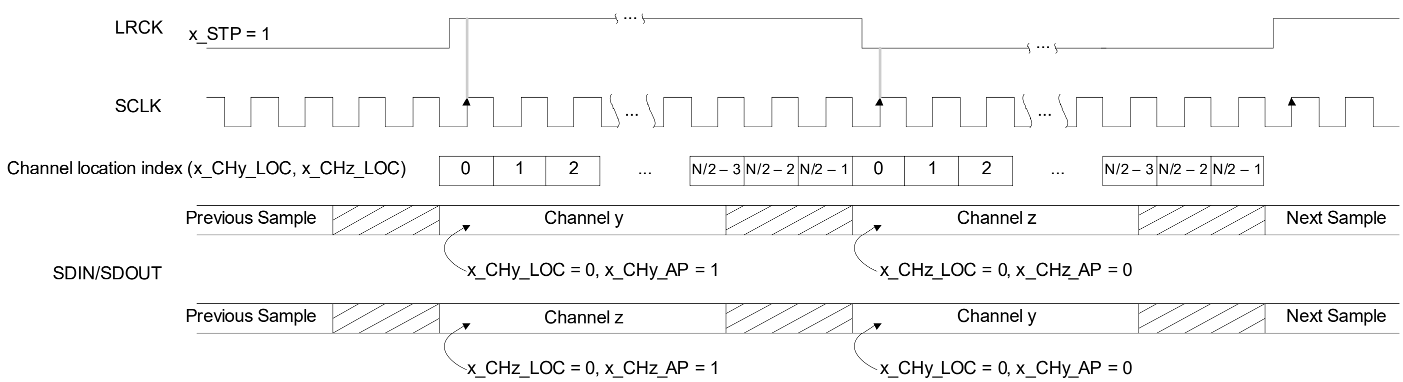


Figure 4-38. Example 50/50 Mode (ASP_STP = 1)

In 50/50 Mode, left and right channels are programmed independently to output when LRCK/FSYNC is high or low—that is, the channel-active phase. The active phase is controlled by the ASP_TX_CHx_AP (see p. 164) and ASP_RXx_CHy_AP (see Section 7.22). If x_AP = 1, the respective channel is output if LRCK/FSYNC is high. If x_AP = 0, the channel is output if LRCK/FSYNC is low.

Note: Active phase has no function if 50/50 Mode = 0, ASP_RX0_2FS = 1, or ASP_RX1_2FS = 1.

In 50/50 Mode, the channel location (see Section 4.9.3) is calculated within the channel-active phase. If there are N bits in a frame, the location of the last bit of each active phase is equal to (N/2) – 1.

4.9.6 Serial Port Status

Each serial port has sticky, write-1-to-clear status bits related to capture and render paths. These bits are described in Section 7.6.4 and Section 7.6.5. Mask bits (Section 7.6.16 and Section 7.6.17) determine whether $\overline{\text{INT}}$ is asserted when a status bit is set. Table 4-18 provides an overview.

If only one data-path direction (render/Tx or capture/Rx) of a serial port is used, the status bits of the unused direction may be set. To prevent spurious interrupts, mask the status bits of unused data path directions and of unused serial ports.

Table 4-18. Serial Port Status

Name	Direction	Description	Register Reference
Request Overload	Rx	Set when too many input buffers request processing at the same time. If all channel registers are properly configured, this error status should never be set.	ASPRX_OVLD p. 141
LRCK Error	Rx	Logical OR of LRCK Early and LRCK Late (see below).	ASPRX_ERROR p. 141

Table 4-18. Serial Port Status *(Cont.)*

Name	Direction	Description	Register Reference
LRCK Early	Tx/Rx	Set when the number of SCLK periods per LRCK phase (high or low) is less than the expected count as determined by x_LCPR and x_LCHI. **Note:** The Rx LRCK early interrupt status is set during the first receive LRCK early event. Subsequent receive LRCK early events are indicated only if valid LRCK transitions are detected.	ASPRX_EARLY p. 141 ASPTX_EARLY p. 142
LRCK Late	Tx/Rx	Set when the number of SCLK periods per LRCK phase (high or low) is greater than the expected count as determined by x_LCPR and x_LCHI.	ASPRX_LATE p. 141 ASPTX_LATE p. 142
No LRCK	Tx/Rx	**Note:** Set when the number of SCLK periods counted exceeds twice the value of LRCK period (x_LCPR) without an LRCK edge. The Tx No LRCK interrupt status is set during the first instance of a no-transmit LRCK condition. Subsequent no-transmit LRCK conditions are not indicated until after valid LRCK transitions are detected.	ASPRX_NOLRCK p. 141 ASPTX_NOLRCK p. 142
SM Error	Tx	Set if the transmit state machine cannot retrieve data from output buffers (analogous to Rx Request Overload). If all channel registers are properly configured, this status is never set. **Note:** The interrupt status is set during the first transmit SM error event. Subsequent SM error events are not indicated until after the FIFO exits the overflow state.	ASPTX_SMERROR p. 142

4.9.7 Recommended Serial-Port Power-Up and Power-Down Strategies

Although multiple safeguards and controls are implemented to prevent a run on the FIFOs involved in passing data from the input port to the output port, the following power-up sequence is recommended. Section 5 gives detailed sequences.

1. Configure all playback/record channel characteristics—bit resolution, channel select, source (DAI/DAO or SW), native/isochronous, sample rates, etc.
2. Power up playback, record path, and ASRCs.
3. Release the PDN_ALL bit.
4. Power up the serial ports (DAI/DAO).

The following power-down sequence is recommended:

1. Power down the playback and record paths.
2. Power down the serial ports.

4.10 S/PDIF Tx Port

The S/PDIF output port is integrated to provide a pass-through of encoded (e.g., AC3) or PCM data from the serial audio ports to an external optical driver. The S/PDIF port does not support isochronous audio streams.

4.10.1 S/PDIF Pass-Through Transmission

The CS42L42 S/PDIF transmitter performs pass-through retransmission of stereo samples that are generated on an external device and transported over the TDM or SoundWire port. This transmitter can be programmed to retransmit any two of the 16-, 20-, 24-, or 32-bit S/PDIF encoded samples from the serial port by programming ASP_RX0_CH1_RES (note that this is RX0 Channels 1–4 and RX1 Channels 1 and 2, see p. 166) and SPDIF_RES (see p. 161). The supported S/PDIF rates are 32, 44.1, 48, 88.2, 96, 176.4, and 192 kHz and are configured through SPDIF_TX_STAT (see p. 163).

The CS42L42 does not decode or interpret samples chosen for retransmission. Additionally, the S/PDIF path does not incorporate any SRCs in the data path.

When the data source comes from the TDM source, the CS42L42 selects between data from the DAI0 or DAI1 as follows:

- If DAI0, configure SPDIF_CHA_SEL/SPDIF_CHB_SEL (see p. 160) to map any of the four TDM slots (0–3) to the S/PDIF inputs. ASP_RX0_2FS = 0 (see p. 165).
- If ASP_RX1_2FS = 1 (see p. 165), which means there is simultaneous operation on both the TDM and S/PDIF ports at different rates, the S/PDIF transmit port gets data from the DAI1 and ignores data from the DAI0. Channel 0 of DAI1 maps to left channel and Channel 1 of DAI1 maps to right channel.

If the data source comes from the SoundWire port, signals are retimed and passed to the S/PDIF transmit port.

SPDIF_LRCK_SRC_SEL(see p. 137) selects the S/PDIF LRCK source. SPDIF_LRCK_CPOL (see p. 138) sets polarity.

Configuration bits mentioned above must be programmed before powering up the DAI ports and the S/PDIF transmit port.

4.10.2 S/PDIF, Headphone, and ADC Simultaneous Clocking Configuration

S/PDIF transmission requires an SCLK of 128 x Fs supplied either from the ASP_SCLK/SWIRE_CLK input pin or from the internal fractional-N PLL. When operating the S/PDIF transmitter with no other data converters enabled, the source of the transmission clock is freely chosen between the input pin and the PLL. When simultaneous operation of the data converters and the S/PDIF transmitter is desired, a 128 x Fs clock must be supplied from the ASP_SCLK/SWIRE_CLK input. Table 4-19 describes the supported clocks for simultaneous operation.

Table 4-19. S/PDIF, Headphone, and ADC Simultaneous Clocking Support

LRCK (kHz)	S/PDIF	HP (Isochronous)	HSIN (Isochronous)	SCLK (MHz)	PLL Output (MHz)
48	48	8, 11.025, 12, 16, 22.05, 24, 32, 44.1	8,11.025, 12, 16, 22.05, 24, 32, 44.1	6.144, 12.288, 24.576	12.288, 24.576
48	2 x 48 [1]	16, 22.05, 24, 32, 44.1, 48, 88.2	16, 22.05, 24, 32, 44.1, 48	12.288, 24.576	12.288, 24.576
96	96				
96	2 x 96 [1]	32, 44.1, 48, 88.2, 96	32, 44.1, 48	24.576	24.576
192	192				
Fs	Fs	Fs (Native)	Fs (Native)	128xFs	11.2896, 12.288, 22.8796, 24.576 MHz
	2 x Fs [1]				

1.ASP_RX1_2FS = 1.

For proper S/PDIF signal timing, the divide factor, selected with SPDIF_CLK_DIV (see p. 137), must be chosen by using the following formula:

Divide factor = $MCLK_{INT}/(128 \times Fs)$

(where Fs is the data rate to the S/PDIF block and not the external LRCK)

For example, for an S/PDIF output Fs of 192 kHz, 128 X 192 kHz = 24.576 MHz. If ASP_SCLK is 24.576 MHz, the divide factor must be 1 (SPDIF_CLK_DIV = 000).

Note: Due to SPDIF_CLK_DIV being limited to 1, 2, 3, 4, and 8, a 32-kHz S/PDIF Fs is not supported with a 24.576-MHz ASP_SCLK/SWIRE_CLK.

4.10.3 Interface Formats

This section describes the frame and subframe formats, channel coding, and Keep-Alive Mode.

4.10.3.1 Frame Format

A frame (see Fig. 4-39) is uniquely composed of two subframes (see Fig. 4-40). Samples taken from both channels are transmitted by time multiplexing in consecutive subframes. The first subframe normally starts with Preamble M; however, to identify the start of the block structure used to organize the channel status information, the preamble changes to B once every 192 frames. The second subframe always begins with Preamble W.

The frame format is the same for one- and two-channel operations. Data is carried in the first subframe and may be duplicated in the second. If the second subframe does not carry duplicate data, the validity flag (Time Slot 28) must be set to Logic 1.

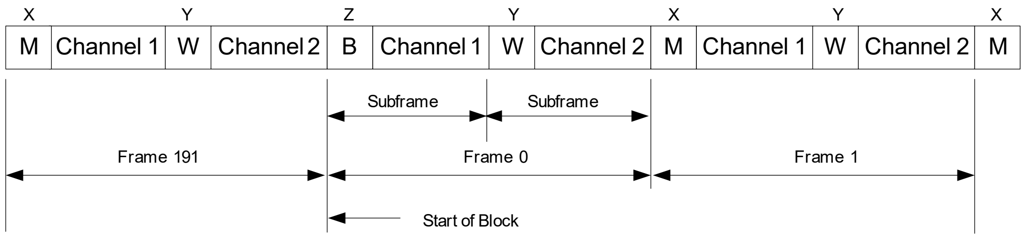


Figure 4-39. S/PDIF Frame Format

4.10.3.2 Subframe Format

Each subframe is divided into 32 time slots, numbered 0–31, as shown in Fig. 4-40.

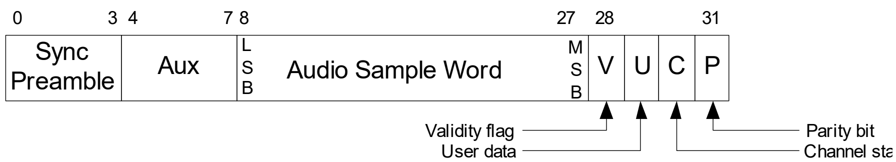


Figure 4-40. Subframe Format (Linear PCM Application)

4.10.3.3 Channel Coding

To minimize DC buildup on the transmission line, to facilitate clock recovery from the data stream, and to make the interface insensitive to the polarity of connections, Time Slots 4–31 are encoded in biphase mark.

Each bit to be sent is represented by a symbol comprising two consecutive binary states. The first state is always different from the second state of the previous symbol. The second state is identical to the first if the bit to be sent is Logic 0, but it is different if the bit is Logic 1 (see Fig. 4-41).

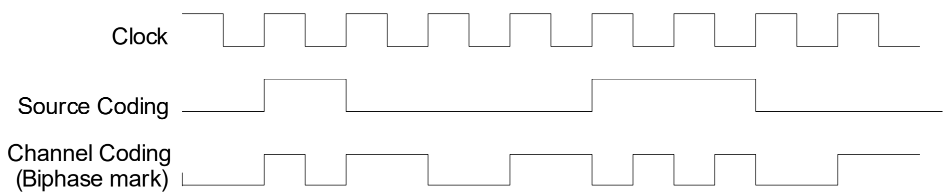


Figure 4-41. S/PDIF Channel Coding

4.10.3.4 Keep-Alive Mode

The Keep-Alive Mode in the S/PDIF transmitter output is used to force a valid S/PDIF stream (clocking and status information without data bits) to be output from the SPDIF_TX pin while the system is in a low power state. This allows an external S/PDIF receiver to remain locked to the S/PDIF stream from the CS42L42 and resume playback without delay if an output stream is later opened. The status information is provided according to the channel status bits in Table 4-20. The state of the SPDIF_TX pin depends on SPDIF_TX_DIGEN (see p. 163) and SPDIF_TX_PDN (see p. 162). Table 4-20 shows all control-bit combinations and the resulting state of the SPDIF_TX pin. Note that SPDIF_TX_KAE (see p. 162) has no function in the Keep-Alive Mode on the CS42L42.

Table 4-20. S/PDIF Output Keep-Alive Control

SPDIF_TX_DIGEN (see p. 162)	SPDIF_TX_PDN (see p. 162)	SPDIF_TX
x	1	Off (drive low)
0	0	Clock + status
1	0	Clock + status + data

4.11 Sample-Rate Converters (SRCs)

SRCs bridge different sample rates at the serial ports within the digital-processing core. SRCs are used for the following:

- Two ASP input channels (Channels 1 and 2). The other two ASP input channels are used for S/PDIF transmit and bypass the SRC.
- One ASP output channel (Channel 1).
- Two SoundWire input channels (Channels 1 and 2). The other two SoundWire input channels are used for S/PDIF transmit and bypass the SRC.
- One SoundWire output channel (Channel 1)
- SRCs are bypassable by setting either SRC_BYPASS_DAC (see p. 129) or SRC_BYPASS_ADC.

An SRC's digital-processing side (as opposed to its serial-port side) connects to the ADC or DAC. Multirate DSP techniques are used to up-sample incoming data to a very high rate and then down-sample to the outgoing rate. Internal filtering is designed so that a full-input audio bandwidth of 20 kHz is preserved if the input and output sample rates are at least 44.1 kHz. If the output sample rate becomes less than the input sample rate, the input is automatically band limited to avoid aliasing artifacts in the output signal.

The following restrictions must be met:

- The F_{SO}-to-F_{SI} ratio must be no more than 1:6 or 6:1. For example, if the DAC is at 48 kHz, the input to the SRC must be at least 8 kHz.
- SRC operation cannot be changed on-the-fly. Before changing the SRC operation (e.g., changing SRC frequencies or bypassing or adding the SRCs), the user must follow the power sequences provided in Section 4.9.7.
- The MCLK frequency must be as close as possible to, but not less than the minimum SRC MCLK frequency, $MCLK_{MIN}$, which must be at least 125 times the higher of the two sample rates (F_{SI} or F_{SO}).

  For example, if F_{SO} is 48 kHz and F_{SI} is 32 kHz, the MCLK must be as close as possible to, but not less than, an $MCLK_{MIN}$ of 6.0 MHz. The MCLK frequency for the SRCs is configured through CLK_IASRC_SEL (see p. 140) and CLK_OASRC_SEL (see p. 140).

Table 4-21 shows settings for the supported sample rates and corresponding $MCLK_{INT}$ frequencies.

Table 4-21. Supported Sample Rates and Corresponding $MCLK_{INT}$ Encodings

Fsint (kHz)	Serial Port Sample Rate (kHz)																
	8.0	11.025	11.029	12	16	22.05	22.059	24	32	44.1	44.118	48	88.2	88.235	96	176.4	176.471	192
44.1	00	00	00	00	00	00	00	00	00	00	00	00	01	01	01	10	10	10
48	00	00	00	00	00	00	00	00	00	00	00	00	01	01	01	10	10	10

Note: SRC MCLKINT Freq= 00 (6 MHz), 01 (12 MHz), 11 (24 MHz), configured in CLK_IASRC_SEL (see p. 140) and CLK_OASRC_SEL (see p. 140)

Jitter in the incoming signal has little effect on rate-converter dynamic performance. It does not affect the output clock.

A digital PLL continually measures the heavily low-pass-filtered phase difference and the frequency ratio between input and output sample rate clocks. It uses the data to dynamically adjust coefficients of a linear time-varying filter that processes a synchronously oversampled version of the input data. The filter output is resampled to the output sample rate.

For input serial ports, input and output sample-rate clocks are respectively derived from the external serial-port sample clock (x_LRCK) and the internal Fs clock. For output serial ports, they are derived in reverse order. FS_EN (see p. 139) must be set according to the F_{SI} or F_{SO} SRC sample rates.

Minimize the SRCs' lock time by programming the serial-port interface sample rates into the x_FS registers (see Section 7.18.2 and Section 7.18.1). If the rates are unknown, programming these registers to "don't know" would likely increase lock times. Proper operation is not assured if sample rates are misprogrammed.

4.12 Headset Interface

The headset interface, shown in Fig. 4-42, is a collection of low-power circuits within the CS42L42's ADC data path. It provides an intelligent interface to an external headset. It also communicates with an applications processor to relay command and status information.

The headset communicates to the interface by shorting its mic line to ground (via the S0 button)

The interface generates HSBIAS, a programmable ultrahigh PSRR headset bias output for an external microphone. A low-voltage headset bias supply (VP = 3.0–3.2 V range) mode is supported. Signaling to the headset to set its operating voltage is facilitated via the bias output

Audible transients that would occur as certain headset plugs are unplugged are minimized by using the headset bias Hi-Z feature Split digital-power domains (VD_FILT and VP) within the headset interface support an ultralow-power standby mode where only the VP supply is used. An output signal may be used to tell the system to wake from its low-power state when a headset plug is inserted or removed or a mic short event (S0 button press) occurs. The interface may be reset by three types of resets with progressively less effect.

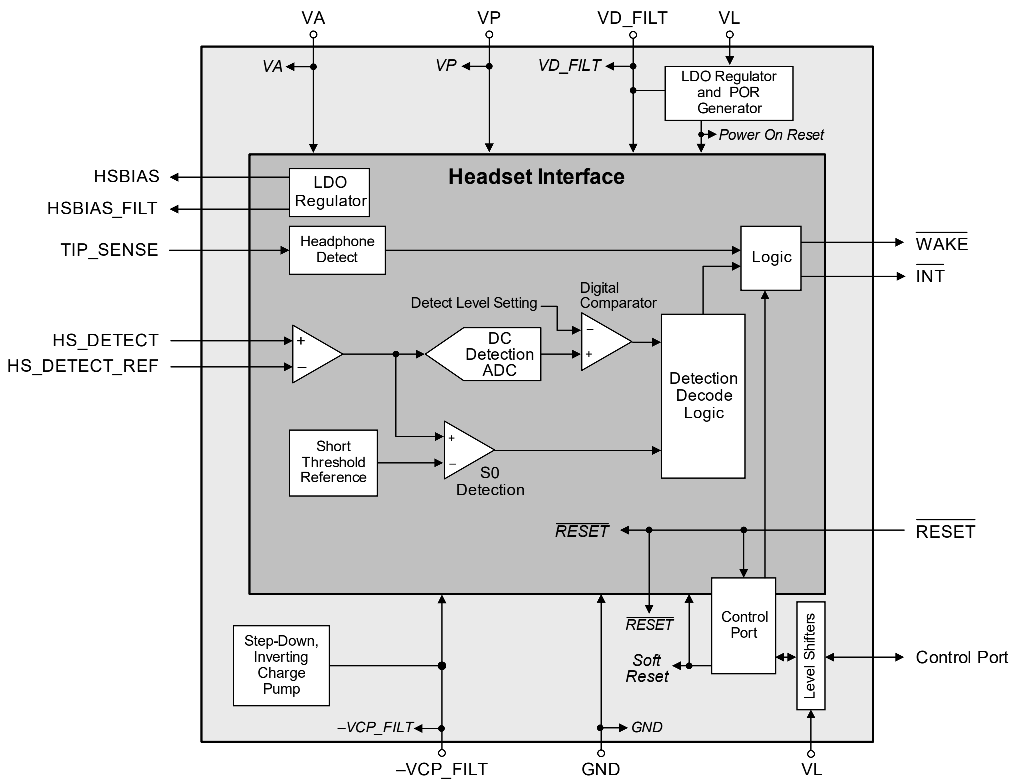


Figure 4-42. Headset Interface Block Diagram

The control port includes registers that source individually maskable interrupts. Event-change debouncing is used to filter applicable status registers. Shadow registering can record multiple events allowing for less frequent register reading. Latchable duplicate registers are used to pass information to the Standby Mode supply domain.

Notes:

- If HSBIAS is Hi-Z, the headset interface is in an invalid mode.
- PDN_ALL must not be set if any of this following is true:
  —Normal Mode is selected (DETECT_MODE ≠ 00).
  —Mic DC-level detection is enabled (PDN_MIC_LVL_DETECT = 0; see p. 151).
  —HS bias sense detection is enabled (HSBIAS_SENSE_EN = 1; see p. 149).

4.13 Headset Type Detect

The CS42L42 can detect whether headset Pins 3 and 4 are either the mic or ground signal and can set the appropriate connections via internal switches, as shown in Fig. 4-43.

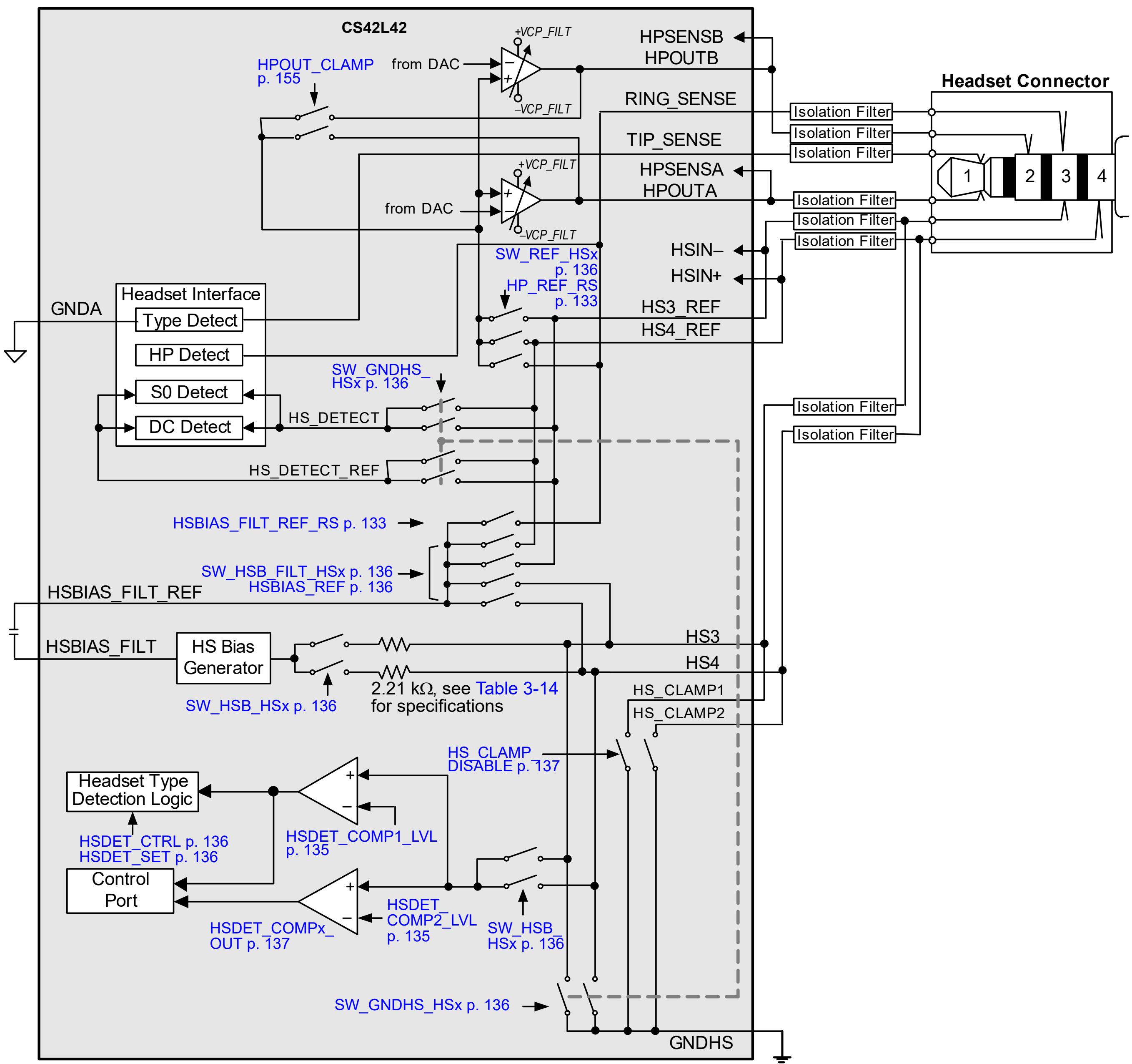


Figure 4-43. Headset Type Detect—Overview

External switches can improve system cross-talk performance by providing a lower impedance path to ground for HP and mic currents. In this case, minimize the impedance from the connection to the headset connector to ground through the external switches. This includes any switch, trace, and series filter impedance.

4.13.1 Headset-Type Detection

Operation of the headset-detect circuit is determined by the HSDET_CTRL setting (see p. 136), described as follows:

- If HSDET_CTRL = 00 or 01, any internal switches can be set manually via the headset switch control bits (SW_x_ y, see Section 7.4.13).

- If HSDET_CTRL = 10 or 11, the SW_x_y bits do not affect the state of the internal switches.

These settings are stored in the VP power domain, so that the switches remain correctly configured, even if the VCP, VL, VA, or VD_FILT supplies are powered off. The HSDET logic and status bits are stored in the VD_FILT power domain.

To prevent audible pop/clicks in the HPs, it may be desirable in some applications to precharge the HSBIAS and HSBIAS_FILT capacitors before setting the switches to their final values. Set SW_HSB_HS3/4 and SW_HSB_FILT_HS3/4 to minimize transients at the HPs associated with charging capacitors. After the capacitors are charged, the switches can be changed to their desired states.

Note that headset S0 button-detect features are not available until internal switches have been configured. Also, depending on the headset type detected, switch settings, and board connections, it may be necessary to set ADC_INV (see p. 154) to have the proper signal polarity. Section 5 provides a recommended headset-type detection sequence.

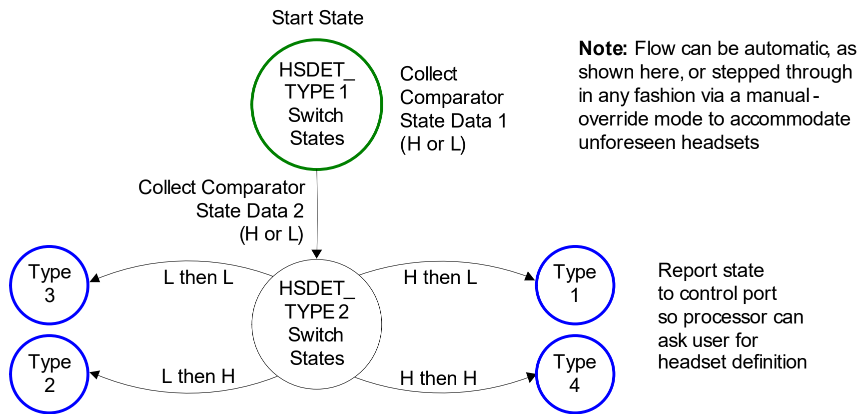


Figure 4-44. Automatic Headset Detect Flowchart

Table 4-22. Automatic Headset Detect Decode

HSDET_TYPE	Headset Plug				DC Test Comparator Results [1]	
	Pin 1	Pin 2	Pin 3	Pin 4	HSDET_TYPE 1 Switch State	HSDET_TYPE 2 Switch State
1	Left audio	Right audio	GND	MIC	High	Low
2	Left audio	Right audio	MIC	GND	Low	High
3	Left audio	Right audio	GND	GND	Low	Low
4	Optical				High	High

1. After performing an automatic headset-detection sequence, the output of the headset comparators may not be valid even if switch configurations are correct for a given plugged-in headset type.

Table 4-23. Headset Type Detect—Switch States after Autodetection (0 = Switch Open; 1 = Switch Closed)

HSDET_TYPE	SW_							
	REF_		HSB_FILT_		HSB_		GNDHS_	
	HS3	HS4	HS3	HS4	HS3	HS4	HS3	HS4
1	1	0	1	0	0	1	1	0
2	0	1	0	1	1	0	0	1
3	1	1	1	1	0	0	1	1
4	1	0	1	0	0	1	1	0

4.14 Plug Presence Detect

The CS42L42 uses TIP_SENSE and RING_SENSE to detect plug presence. The sense pins are debounced to filter out brief events before being reported to the corresponding presence-detect bit and generating an interrupt if appropriate.

4.14.1 Plug Types

The plug-sense scheme supports the following plug types:

- Tip–Ring–Sleeve (TRS)—Consists of a segmented metal barrel with the tip connector used for HPOUTA, a ring connector used for HPOUTB, and a sleeve connector used for HSGND.

- Tip–Ring–Ring–Sleeve (TRRS)—Like TRS, with an additional ring connector for the HSIN connection. There are two common pinouts for TRRS plugs:
  — One uses the tip for HPOUTA, the first ring for HPOUTB, the second ring for HSGND, and the sleeve for HSIN.
  — OMTP, or China, headset, which swaps the third and fourth connections, so that the second ring carries HSIN and the sleeve carries HSGND.

4.14.2 Tip-Sense/Ring-Sense Methods

The following methods are used to detect the presence or absence of a plug:

- Tip sense (TS)—A sense pin is connected to a terminal on the receptacle such that, if no plug is inserted, the pin is floating. If a plug is inserted, the pin is shorted to the tip (T) terminal. The tip is sensed by having a small current source in the device pull up the pin if it is left floating (no plug). If a plug is inserted and the sense pin is shorted to HPOUTA, the sense pin is assumed to be pulled low via clamps at the HP amp output when it is in power down. If the HP amp is running, the sense pin is shorted to the output signal and, therefore, is pulled below a certain threshold via the output stage of the HP amp. Thus, a low level at the sense pin indicates plug inserted, and a high level at the sense pin indicates plug removed.
- Inverted tip sense (ITS)—Like tip sense, but with a connector whose sense pin is shorted to the tip terminal if the plug is removed and is left floating if it is inserted. Therefore, a low level at the sense pin indicates plug removed and a high level at the sense pin indicates plug inserted. Inversion is controlled by the following:
  — The invert (TIP_SENSE_INV, p. 151), which goes to the analog and affects a number of other features.
  — The tip-sense invert (TS_INV, p. 135), which affects only the configuration bits in Section 6.5.
- Ring sense (RS)—Like tip sense, except that the sense pin is shorted to the second ring terminal (HS3) when a plug with a metal barrel (TRS or TRSS) is inserted, and floating when a plug with a plastic barrel (OPT) is inserted or the plug is removed. If a metal plug is inserted and the sense pin is shorted to HS3, it is assumed that the sense pin is pulled low (to HSGND) or below a certain threshold (to HSBIAS) via switches in the HS type-detect block. As a result, a low level at the sense pin indicates metal plug inserted and a high level at the sense pin indicates plug removed (plastic plug inserted or plug removed).
- Inverted ring sense (IRS)—Like ring sense, except that the connector is constructed such that the sense pin is shorted to the second ring terminal (HS3) when the plug is removed and is left floating when it is inserted. Therefore, a low level at the sense pin indicates *plug removed*; a high level indicates *metal or plastic plug inserted*.

4.14.3 Ring-Sense Configuration

The RING_SENSE pin can be used as a ground sense for the connected plug if the inserted plug is determined to be of type TRS or TRRS. If the RING_SENSE pin is used as a ground reference, the impedance between the RING_SENSE plug connector and the plug degrades the common-mode rejection of the output, which in turn affects output offset, step deviation, and pop/click attenuation. The CS42L42 includes a RING_SENSE impedance-detection circuit to aid in the decision to use the RING_SENSE input pin as a HP ground reference.

The impedance-detection circuit can be activated to test whether plug-connector-to-plug impedance exceeds ~1 kΩ. RS_TRIM_T (see p. 133) determines the detection threshold. Pull-up resistance is controlled by the bits shown in Table 4-24.

Table 4-24. Threshold Detection

RING_SENSE_PU_HIZ (see p. 133)	RS_TRIM_R (See p. 133)	Nominal Pull-Up Resistance
0	x	16.2 kΩ
1	0	2.25 MΩ
1	1	1.125 MΩ

4.14.4 Tip-Sense and Ring-Sense Debounce Settings

Fig. 4-45 shows the tip-sense and ring-sense controls and the associated interrupt, status, and mask registers.

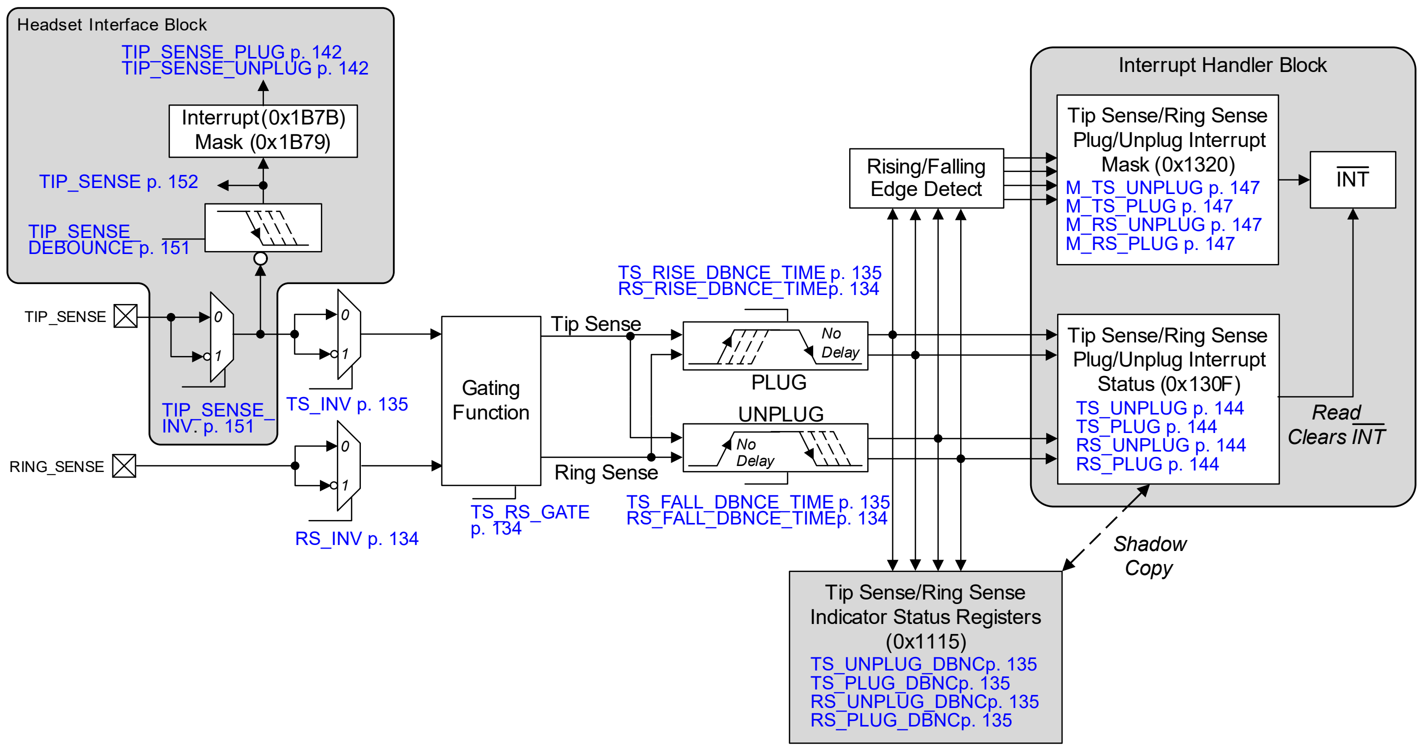


Figure 4-45. Tip-Sense and Ring-Sense Controls

The tip-and ring-sense debounce register fields behave and interact as follows:

- TS_UNPLUG_DBNC. Shows tip sense status after being unplugged with the associated debounce time.
- TS_PLUG_DBNC. Shows tip sense status after being plugged in with the associated debounce time.
- RS_UNPLUG_ DBNC. Shows ring sense status after being unplugged with the associated debounce time.
- RS_PLUG_DBNC. Shows the ring sense status after being plugged in with the associated debounce time.

Note: TS_INV must be set to have TS_PLUG/TS_PLUG_DBNC status match TIP_SENSE_PLUG status.

The debounce bits are described in Section 7.4.10. Multiple debounce settings can be configured for insertion, removal, ring sense, and tip sense:

- TIP_SENSE_DEBOUNCE (see p. 151) controls the tip-sense removal debounce time.
- TS_FALL_DBNCE_TIME and TS_RISE_DBNCE_TIME (see p. 135) and RS_FALL_DBNCE_TIME and RS_RISE_DBNCE_TIME (see p. 134) settings configure the corresponding debounce times.

4.14.5 Setup Instructions

The following steps are required to activate the tip-/ring-sense debounce interrupt status:

1. Clear PDN_ALL (see p. 132).
2. Set TIP_SENSE_EN (see p. 150) for analog front-end of tip sense.
3. Set LATCH_TO_VP (see p. 151) to latch analog controls into analog circuits.
4. Set RING_SENSE_PDNB (see p. 133) to enable debounce block for ring sense plug/unplug.
5. Write TIP_SENSE_CTRL (see p. 150) to 01 or 11 to enable debounce for tip sense plug/unplug.
6. Clear interrupt masks (0x1320, see Section 7.6.22).

Interrupt status (see Section 7.6.12) does not contain an event-capture latch—a read always yields the current condition.

Table 4-25 describes the plug/unplug status for both tip and ring.

Table 4-25. Tip and Ring Plug/Unplug Status

Plug Status	Unplug Status	Interpretation
0	0	Tip is fully unplugged/not present
1	0	Reserved
0	1	Tip connection is in a transitional state
1	1	Tip is fully plugged/present

4.14.6 Plug-Sense Gating

In some configurations, the presence of an optical plug can be determined only by the presence, or absence, of an associated plug. In the common combo plug implementation, the receptacle can accommodate either a headphone (TRS/TRRS) or an S/PDIF (OPT) connector. However, if ring sense is used to distinguish between two jacks, the absence of any plug may be falsely interpreted as the presence of an optical plug. Likewise, if the optical plug has a metal tip and tip sense is used to determine the presence of a TRS/TRSS plug, the presence of an optical plug may also be falsely interpreted as the presence of a headphone plug.

To lessen those constraints, TS_RS_GATE (p. 134) can be used to apply the following gating rules, as would be appropriate for a combo plug:

- RING_SENSE present is asserted only if both RING_SENSE detected and TIP_SENSE detected are true.
- TIP_SENSE present is not asserted if RING_SENSE detected is true.

TIP_SENSE- and RING_SENSE-detected states are derived as usual and already consider inversion. Table 4-26 shows how TIP_SENSE– and RING_SENSE–present states are determined afterwards and represent what is passed to the host.

Table 4-26. Plug Sense Gating

TS_RS_GATE (see p. 134)	TIP_SENSE Detected	RING_SENSE Detected	TIP_SENSE Present (TS_PLUG_DBNC = 0, see p. 135)	RING_SENSE Present (RS_PLUG_DBNC = 0, see p. 135)
0	0	0	F	F
0	0	1	F	T
0	1	0	T	F
0	1	1	T	T
1	0	0	F	F
1	0	1	F	F (Gating prevents a false-positive pin presence.)
1	1	0	T	F
1	1	1	F (Gating prevents a false-positive pin presence.)	T

4.15 Power-Supply Considerations

Because some power supply combinations can produce unwanted system behavior, note the following:

- Control-port transactions can occur 1 ms after VP, VD_FILT, VCP, and VL exceed the minimum operating voltage.
- If VP supply is off, it is recommended that all other supplies are also off. VP must be the first supply turned on.
- $\overline{\text{RESET}}$ must be asserted until VP is valid.
- If VD_FILT is supplied externally ($\overline{\text{DIGLDO\_PDN}}$ = GND), VL must be supplied before VD_FILT, VA, VL, and VCP can come up in any order. Due to the VD_FILT POR, VD_FILT must be turned off before VA, VL, or VCP are turned off; otherwise, current could be drawn from supplies that remain on.

Table 4-27 shows the maximum current for each supply when VP is on, but other supplies are on or off (all clocks are off and all registers are set to default values, i.e., reset).

Table 4-27. Typical Leakage Current during Nonoperational Supply States (with VP Powered On)

Supply			Current (µA)				Notes
VCP	VA	VL	I_{VP}	I_{VCP}	I_{VA}	I_{VL}	
Off	On	Off	14	0	0	0	VA may source or sink current
Off	On	On	25	0	0	328	VA may source or sink current
On	Off	Off	14	0	0	0	—
On	Off	On	25	0	0	328	—
On	On	Off	14	0	0	0	VA may source or sink current
On	On	On	25	0	0	328	—

Notes:
- Values shown reflect typical voltage and temperature. Leakage current may vary by orders of magnitude across the maximum and minimum recommended operating supply voltages and temperatures listed in Table 3-2.
- Test conditions: Clock/data lines are held low, $\overline{\text{RESET}}$ is held high, and all registers are set to their default values.

Table 4-28 shows requirements and available features for valid power-supply configurations.

Table 4-28. Valid Power-Supply Configurations

Configuration	Notes
On: VP Off: VD_FILT = VCP = VL = VA	Limited set of headset plug-detect and WAKE output features, see Section 4.12 and Section 4.13.
On: VP = VL Off: VD_FILT = VCP = VA = OFF	Limited set of headset plug-detect and WAKE output features, see Section 4.12 and Section 4.13. Digital I/O ESD diodes are powered to prevent conduction in pin-sharing applications.
On: VP = VD_FILT = VCP = VL = VA	Full chip functionality

4.15.1 VP Monitor

The CS42L42 voltage comparator monitors the VP power supply for potential brown-out conditions due to power-supply overload or other fault conditions. To perform according to specifications, VP is expected to remain above 3.0 V at all times. The VP monitor is enabled by setting VPMON_PDNB (see p. 133). Fig. 4-46 shows the behavior of the VP monitor.

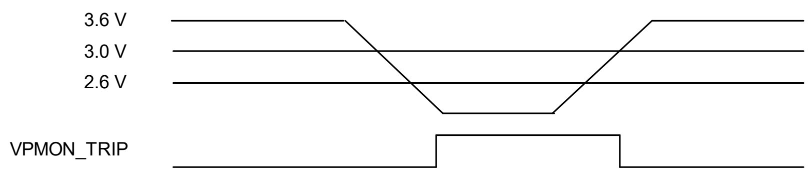


Figure 4-46. VP Monitor

The following describes the VP monitor behavior with respect to the voltage level:

- If VP drops below 3.0 V, HSBIAS, HP output, RING_SENSE, and TIP_SENSE performance may be compromised.
- If VP drops below 2.6 V, the VPMON_TRIP status bit is set (see p. 144). An interrupt is triggered if M_VPMON_TRIP = 0 (see p. 147). This bit must be unmasked/enabled only if VP is above the detection-voltage threshold. It must be masked/disabled by default to eliminate erroneous interrupts while VP is ramping or is known to be below the threshold voltage.
- A brown-out condition remains until VP returns to a voltage level above 3.0 V.
- The VP monitor circuit becomes unreliable at VP levels below 2.4 V.
- The VP monitor is intended to detect slow transitioning signals about the 2.6-V threshold. Pulses of short duration are filtered by the monitor and may not trigger at the 2.6-V threshold, but at a value much lower than expected.

4.16 Control-Port Operation

Control-port registers are accessed through the I2C or SoundWire interfaces, allowing the codec to be configured for the desired operational modes and formats. Accessing the control-port registers is mutually exclusive to the I2C port or SoundWire port, depending on the SWIRE_SEL configuration (see Table 1-1). Because the SWIRE_SEL logic state is latched at POR, dynamic switching between SoundWire and I2C control is not supported.

4.16.1 I2C Control-Port Operation

The I2C control port can operate completely asynchronously with the audio sample rates. However, to avoid interference problems, the I2C control port pins must remain static if no operation is required.

The control port uses the I2C interface, with the codec acting as a slave device. The I2C control port can operate in the following modes, which are configured through the I2C debounce register in Section 7.3.12:

- Standard Mode (SM), with a bit rate of up to 100 kbit/s
- Fast Mode (FM), with a bit rate of up to 400 kbit/s
- Fast Mode Plus (FM+), with a bit rate of up to 1 Mbit/s.

Note: ASP_SCLK is not required to be on when the control port is accessed, for state machines affected by register settings to advance.

SDA is a bidirectional data line. Data is clocked into and out of the CS42L42 by the SCL clock. Fig. 4-47–Fig. 4-50 show signal timings for read and write cycles. A Start condition is defined as a falling transition of SDA while the clock is high. A Stop condition is defined as a rising transition of SDA while the clock is high. All other SDA transitions occur while the clock is low.

The register address space is partitioned into 8-bit page spaces that each comprise up to 127 8-bit registers. Address 0x00 of each page is reserved as the page indicator, PAGE. Writing to address 0x00 of any page changes the page pointer to the address written to address 0x00.

To initiate a write to a particular register in the map, the page address, 0x00, must be written following the chip address. Subsequent accesses to register addresses are treated as offsets from the page address written in the initial transaction. To change the page address, initiate a write to address 0x00. To determine which page is active, read address 0x00.

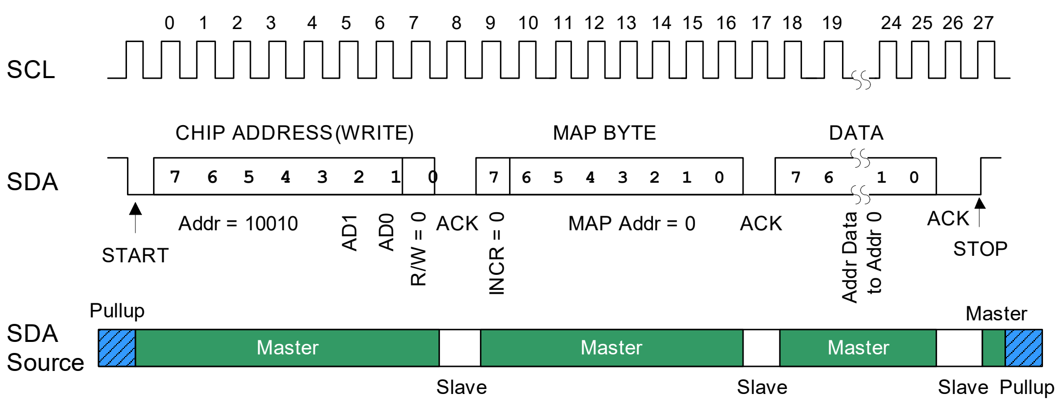


Figure 4-47. Control-Port Timing, I2C Write of Page Address

The first byte sent to the CS42L42 after a Start condition consists of a 7-bit chip address field and a R/$\overline{W}$ bit (high for a read, low for a write) in the LSB. To communicate with the CS42L42, the chip address field must match 1_0010, followed by the state of the AD1 and AD0 pins.

Note: Because AD0 and AD1 logic states are latched at POR, dynamic addressing is not supported.

If the operation is a write, the next byte is the memory address pointer (MAP); the 7 LSBs of the MAP byte select the address of the register to be read or written to next. The MSB of the MAP byte, INCR, selects whether autoincrementing is to be used (INCR = 1), allowing successive reads or writes of consecutive registers.

Each byte is separated by an acknowledge (ACK) bit, which the CS42L42 outputs after each input byte is read and is input to the CS42L42 from the microcontroller after each transmitted byte.

For write operations, the bytes following the MAP byte are written to the CS42L42 register addresses pointed to by the last received MAP address, plus however many autoincrements have occurred. Note that, while writing, any autoincrementing block accesses that go past the maximum 0x7F address write to address 0x00—the page address. The writes then continue to the newly selected page. Fig. 4-48 shows a write pattern with autoincrementing.

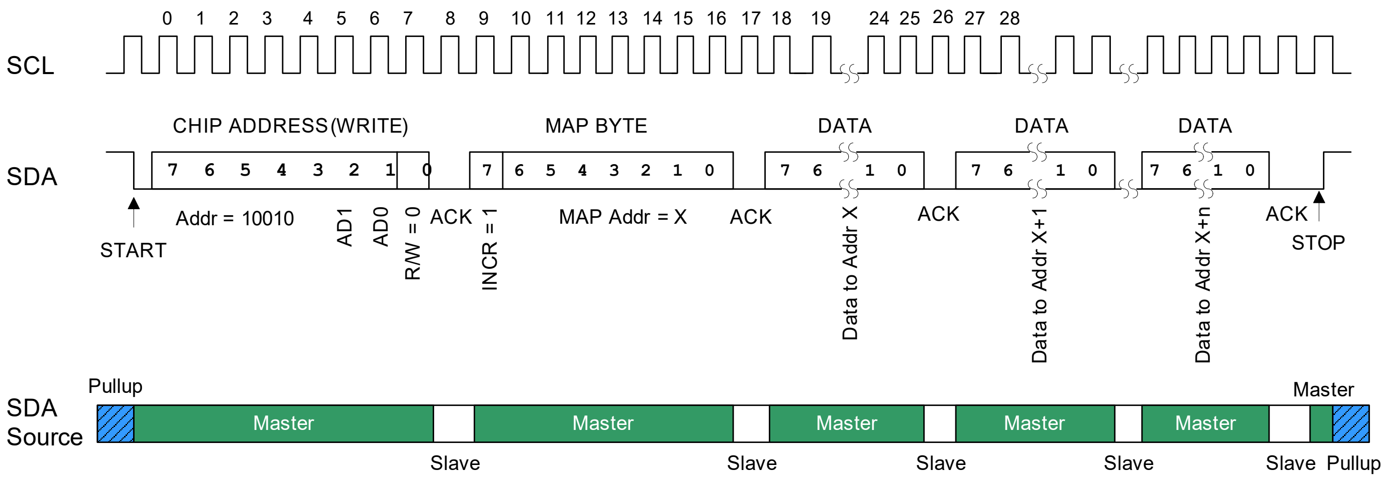


Figure 4-48. Control-Port Timing, I²C Writes with Autoincrement

For read operations, the contents of the register pointed to by the last received MAP address, plus however many autoincrements have occurred, are output in the next byte. While reading, any autoincrementing block access that goes past the maximum 0x7F address wraps around and continues reading from the same page address. Fig. 4-49 shows a read pattern following the write pattern in Fig. 4-48. Notice how read addresses are based on the MAP byte from Fig. 4-48.

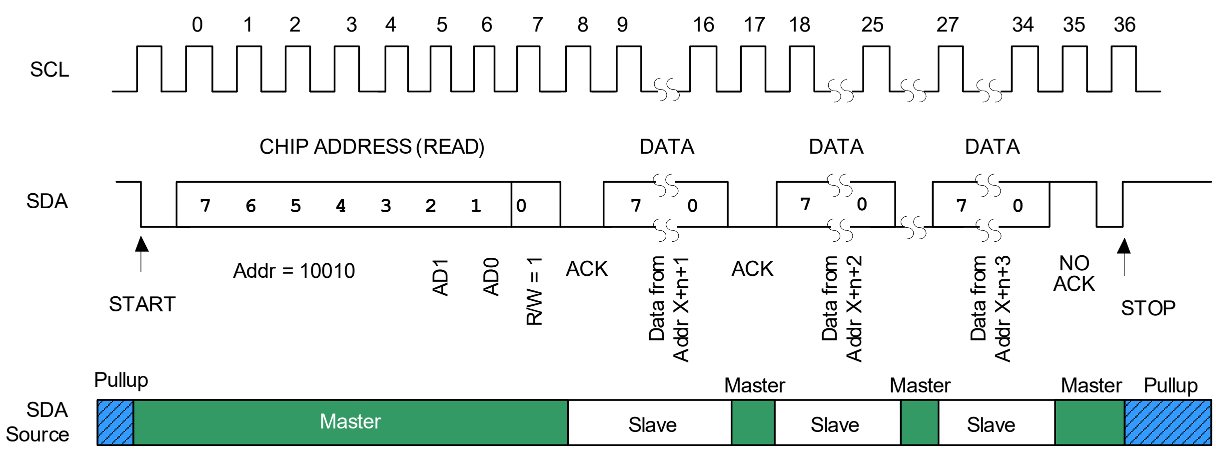


Figure 4-49. Control-Port Timing, I²C Reads with Autoincrement

To generate a read address not based on the last received MAP address, an aborted write operation can be used as a preamble (see Fig. 4-50). Here, a write operation is aborted (after the ACK for the MAP byte) by sending a Stop condition.

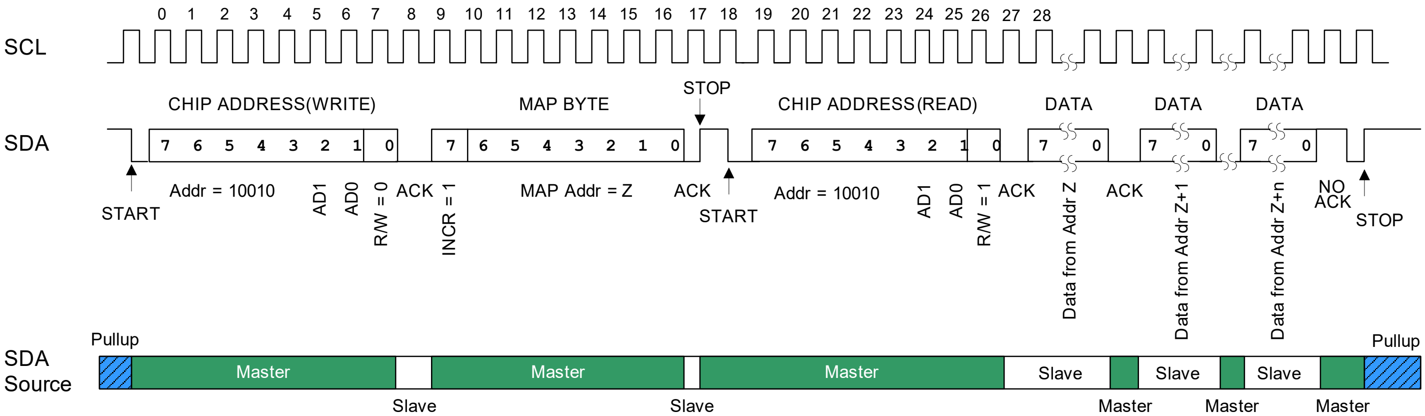


Figure 4-50. Control-Port Timing, I²C Reads with Preamble and Autoincrement

The following pseudocode illustrates an aborted write operation followed by a single read operation, assumes page address has been written. For multiple read operations, autoincrement would be set to on (as shown in Fig. 4-50).

```
Send start condition.
Send 10010(AD1)(AD0)0 (chip address and write operation).
Receive acknowledge bit.
Send MAP byte, autoincrement off.
Receive acknowledge bit.
Send stop condition, aborting write.
Send start condition.
Send 10010(AD1)(AD0)1 (chip address and read operation).
Receive acknowledge bit.
Receive byte, contents of selected register.
Send acknowledge bit.
Send stop condition.
```

4.17 Reset

The CS42L42 offers the reset options described in Table 4-29.

Table 4-29. Reset Summary

Reset	Cause	Result
Device hard reset	Asserting RESET	If RESET is asserted, all registers (both VP and VD_FILT domains) and all state machines are immediately set to their defaults. No operation can begin until RESET is deasserted. Before normal operation can begin, RESET must be asserted at least once after the VP supply is first brought up. **Note:** Table 4-30 lists how this reset affects SoundWire registers.
Power-on reset (POR)	Power up	If VD_FILT is lower than the POR threshold, the VD_FILT register fields and the state machines are held in reset, setting them to their default values/states. This does not reset the VP registers. The POR releases the reset when the VD_FILT supply goes above the POR threshold. VL and VA supplies must be turned at the same time the VD_FILT supply is turned on. **Note:** Table 4-30 lists how this reset affects SoundWire registers.
Force reset (SoundWire defined)	Setting FORCE_RESET	Setting FORCE_RESET (see p. 118) asserts a SoundWire Hard Reset, described in Table 4-30. After a FORCE_RESET, the master must issue a reboot command (set SFT_RST_REBOOT; see p. 161) and wait for 2.5 ms.
Bus reset (SoundWire defined)	Master driving 4096 Logic 1s	Bus reset asserts a SoundWire Hard Reset, described in Table 4-30. After a bus reset, the master must issue a reboot command (set SFT_RST_REBOOT; see p. 161) and wait for 2.5 ms.
Clock stop mode reset (SoundWire defined)	Exit clock stop; CLOCK_STOP_MODE = 1.	Clock Stop Mode reset asserts a SoundWire Hard Reset, described in Table 4-30. After the clock is restarted, the master must issue a reboot command (set SFT_RST_REBOOT; see p. 161) and wait for 2.5 ms. **Note:** The MIPI SoundWire specification refers to this as a *ClockStopMode1* reset source and uses *ClockStopMode0* to refer to the operation when CLOCK_STOP_MODE = 0 (see p. 119).
Sync loss reset (SoundWire defined)	Loss-of-frame synchronization	Sync loss does not reset debug related SoundWire status bits as the other resets do. Disables active serial data paths. Occurs when sync loss errors result in detachment from the bus. See Table 4-30.

Table 4-30 describes the effects of resets on register fields. The SoundWire Slave IP supports asynchronous resets, whose effects are described in Table 4-30.

Table 4-30. Register Resets

Registers	POR/Device Hard Reset	SoundWire Hard Reset [1]	SoundWire Synchronization Loss Reset
SCP/DP*n* interrupt mask (Sections 7.1.2, 7.1.14, 7.1.16, and 7.2.2) CURRENT_BANK in the SCP control register (Section 7.1.3) SCP device number (Section 7.1.5) Memory access status (Section 7.1.17) Memory read last address 0 and 1 (Section 7.1.20) INVERT_BANK bit in DP*n* Port control registers (Section 7.2.3) DP*n* channel prepare status (Section 7.2.5) DP*n* channel enable (Section 7.2.7)	Reset to default	Reset to default	Reset to default
SCP/DP*n*/general interrupt status (Section 7.1.1, Section 7.2.1, Section 7.1.13, Section 7.1.15)	Reset to default	Reset to default	Not reset
All other SoundWire registers (address range below 0x1000)	Reset to default	Not reset	Not reset
Non-SoundWire registers (address range 0x1000 and above)	Reset to default	Reset to default	Not reset

1.Bus reset, setting FORCE_RESET bit, or on exit from Clock Stop Mode if CLOCK_STOP_MODE is set. See Table 4-29.

4.18 Interrupts

The following sections describe the CS42L42 interrupt implementation.

4.18.1 SoundWire Interrupts

The SoundWire interrupt mechanism allows SoundWire slaves to alert the SoundWire master to abnormal events or error conditions. SoundWire interrupts are implemented as defined by the SoundWire Specification. Their statuses are combined into an interrupt status reported on the SoundWire bus, through the SoundWire General Interrupt Status 1 register; see Section 7.1.13). If this register indicates the presence of an interrupt condition, software must examine the standard interrupts to determine the source.

Table 4-31 lists the SoundWire interrupts and corresponding mask registers. Note that, unlike other interrupts implemented on the CS42L42, SoundWire interrupt mask bits are masked if cleared, rather than if set.

Table 4-31. SoundWire Interrupt Status Registers and Corresponding Mask Registers—Page 0x00

Interrupt Source Status Register		Interrupt Mask Register
Section	Name	
Section 7.1, "SoundWire Control Port 0 Registers"	SCP Interrupt Status 1 (Section 7.1.1) General Interrupt Status 1 (Section 7.1.13)	SCP Interrupt Mask 1 (Section 7.1.2) General Interrupt Mask 1 (Section 7.1.14)
Section 7.2, "SoundWire Data Port (1–3) Descriptions"	DPn Interrupt Status (Section 7.2.1)	DPn Interrupt Mask (Section 7.2.2)

4.18.2 Standard Interrupts

The interrupt output pin, $\overline{\text{INT}}$, is used to signal the occurrence of events within the device's interrupt status registers. Events can be masked individually by setting corresponding bits in the interrupt mask registers. Table 4-32 lists interrupt status and mask registers. The configuration of mask bits determines which events cause the immediate assertion of $\overline{\text{INT}}$:

- When an unmasked interrupt status event is detected, the status bit is set and $\overline{\text{INT}}$ is asserted.
- When a masked interrupt status event is detected, the interrupt status bit is set, but $\overline{\text{INT}}$ is not affected.

Once asserted, $\overline{\text{INT}}$ remains asserted until all status bits that are unmasked and set have been read. Interrupt status bits are sticky and read-to-clear: Once set, they remain set until the register is read and the associated interrupt condition is not present. If a condition is still present and the status bit is read, although $\overline{\text{INT}}$ is deasserted, the status bit remains set.

To clear status bits set due to initiation of a path or block, the status bits must be read after the corresponding module is enabled and before normal operation begins. Otherwise, unmasking previously set status bits causes assertion of $\overline{\text{INT}}$.

Table 4-32. Interrupt Status Registers and Corresponding Mask Registers—0x13

Interrupt Source Status Register	Interrupt Mask Register
ADC Overflow Interrupt Status (Section 7.6.1)	ADC Overflow Interrupt Status (Section 7.6.1)
Mixer Interrupt Status (Section 7.6.2)	Mixer Interrupt Mask (Section 7.6.14)
SRC Interrupt Status (Section 7.6.3)	SRC Interrupt Mask (Section 7.6.15)
ASP RX Interrupt Status (Section 7.6.4)	ASP RX Interrupt Mask (Section 7.6.16)
ASP TX Interrupt Status (Section 7.6.5)	ASP TX Interrupt Mask (Section 7.6.17)
Codec Interrupt Status (Section 7.6.6)	Codec Interrupt Mask (Section 7.6.18)
Detect Interrupt Status 1 (Section 7.6.7)	Detect Interrupt Mask 1 (Section 7.9.10)
SRC Partial Lock Interrupt Status (Section 7.6.9)	SRC Partial Lock Interrupt Mask (Section 7.6.19)
VP Monitor Interrupt Status (Section 7.6.10)	VP Monitor Interrupt Mask (Section 7.6.20)
PLL Lock Interrupt Status (Section 7.6.11)	PLL Lock Mask (Section 7.6.21)
Tip/Ring Sense Plug/Unplug Interrupt Status (Section 7.6.12)	Tip/Ring Sense Plug/Unplug Interrupt Mask (Section 7.6.22)

Note, however, that if $\overline{\text{INT}}$ is configured to operate in Short-Detect Mode (DETECT_MODE = 1, see the DETECT_MODE setting on p. 151), interrupt detection is otherwise disabled.

- If set to short-detect only, $\overline{\text{INT}}$ is dedicated to the short-detection block of the headset interface; no other sources can trigger assertion of $\overline{\text{INT}}$.
- If set to inactive (DETECT_MODE = 00) Normal Mode (DETECT_MODE = 11), $\overline{\text{INT}}$ responds to any unmasked interrupt status event.
- After exiting Short-Detect Mode, previously asserted interrupt sources may generate additional interrupts. To avoid unwanted interrupts, clear the interrupt sources before exiting Short-Detect Mode.

Note: Setting PDN_ALL clears all interrupts, unless PDN_MIC_LVL_DETECT = 0 and/or HSBIAS_SENSE_EN = 1, DETECT_MODE ≠ 00, and an interrupt has occurred. To clear an interrupt, clear DETECT_MODE.

As Table 4-33 indicates, interrupt sources are categorized into two groups:

- Condition-based interrupt source bits are set when the condition is present and they remain set until the register is read and the condition that caused the bit to assert is no longer present.
- Event-based interrupt source bits are cleared when read. In the absence of subsequent source events, reading one of these status bits returns a 0.

Table 4-33. Interrupt Source Types

Group	Status Registers	Interrupt Source Type
Tip sense and ring sense debounce (see Section 7.4.10)	TS_UNPLUG_DBNC TS_PLUG_DBNC RS_UNPLUG_DBNC RS_PLUG_DBNC	Event Event Event Event
ADC (see Section 7.6.1)	ADC_OVFL	Event
Mixer Interrupt (see Section 7.6.2)	EQ_BIQUAD_OVFL EQ_OVFL MIX_CHA_OVFL MIX_CHB_OVFL	Event Event Event Event
Serial port (see Section 7.6.3, Section 7.6.4, and Section 7.6.5)	ASPRX_OVLD ASPRX_ERROR ASPRX_LATE ASPRX_EARLY [1] ASPRX_NOLRCK [1] ASPTX_SMERROR [1] ASPTX_LATE ASPTX_EARLY ASPTX_NOLRCK SRC_OUNLK SRC_IUNLK SRC_OLK SRC_ILK	Event Event Event Event Condition Event Event Event Condition Condition Condition Condition Condition
Global (see Section 7.6.6)	HSDET_AUTO_DONE PDN_DONE	Event Condition

Table 4-33. Interrupt Source Types *(Cont.)*

Group	Status Registers	Interrupt Source Type
Headset (see Section 7.6.7 and Section 7.6.8)	HSBIAS_SENSE TIP_SENSE_PLUG TIP_SENSE_UNPLUG DETECT_TRUE_FALSE DETECT_FALSE_TRUE SHORT_RELEASE SHORT_DETECTED	All are events.
DAC and ADC (see Section 7.6.9)	DAC_LK ADC_LK	Condition Condition
VP monitor (see Section 7.6.10)	VPMON_TRIP	Condition
PLL (see Section 7.6.11)	PLL_LOCK	Condition
Tip sense and ring sense plug/unplug status (see Section 7.6.12)	TS_UNPLUG TS_PLUG RS_UNPLUG RS_PLUG	Events. Although a true event interrupt clears when read, these dynamically reflect the state of the debounced input signal.

1. Reading this bit following an early LRCK/SM error/no LRCK returns a 1. Subsequent reads return a 0. Valid LRCK transitions or exiting the transmit overflow condition rearms the detection of the corresponding event. See Table 4-18 for details.

5 System Applications

This section provides recommended procedures and instruction sequences for standard operations.

5.1 Power-Up Sequence

Ex. 5-1 is the procedure for implementing HP playback from the ASP. This example sequence configures the CS42L42 for SCLK = 12.288 MHz, LRCK = 48 kHz, and TDM playback, in Slave Mode.

Example 5-1. Power-Up Sequence

Step	Task	Register/Bit Fields	Value	Description
1	Apply all relevant power supplies, then assert $\overline{RST}$ before applying SCLK and LRCK to the CS42L42.			
2	Wait 2.5 ms.			
3	Power up the codec.	Power Down Control 2. 0x1102	0x83	
		Reserved DISCHARGE_FILT+ SRC_PDN_OVERRIDE ASP_DAI1_PDN DAC_SRC_PDNB ADC_SRC_PDNB	100 0 0 0 1 1	— FILT+ is not clamped to ground. SRC is powered up. ASP is powered up. DAC SRC is powered up. ADC SRC is powered up.
4	Configure the device's ASP and ASP SRC.			
	4.1 Configure switch from RCO to SCLK.	Oscillator Switch Control. 0x1107	0x01	
		Reserved SCLK_PRESENT	0000 000 1	— SCLK is present.
	4.2 Power down the RCO.	Oscillator Switch Status. 0x1109	0x01	
		Reserved OSC_PDNB_STAT OSC_SW_SEL_STAT	0000 0 0 01	— RCO powered down RCO selected for internal MCLK
	4.3 Configure device's internal sample rate with the applied MCLK signal.	MCLK Control. 0x1009	0x02	
		Reserved INTERNAL_FS Reserved	0000 00 1 0	— Internal sample rate is MCLK/256= 48 kHz. —
	4.4 Select MCLK source.	MCLK Source Select. 0x1201	0x00	
		Reserved MCLKDIV MCLK_SRC_SEL	0000 00 0 0	— Divide by 1. SCLK pin is MCLK source.
	4.5 Configure the FSYNC period.	FSYNC Period, Lower Byte. 0x1205	0xFF	
		FSYNC_PERIOD_LB	1111 1111	256 SCLKs per LRCK lower byte.
	4.6 Configure the FSYNC period.	FSYNC Period, Upper Byte. 0x1206	0x00	
		FSYNC_PERIOD_UB	0000 0000	0 SCLKs per LRCK upper byte
	4.7 Configure FSYNC pulse width.	FSYNC Pulse Width, Lower Byte. 0x1203	0x1F	
		FSYNC_PULSE_WIDTH_LB	0001 1111	LRCK is one SCLK Wide.

Example 5-1. Power-Up Sequence ***(Cont.)***

Step	Task	Register/Bit Fields	Value	Description
4.8	Configure the ASP clock.	ASP Clock Configuration 1. 0x1207	0x00	
		Reserved ASP_SCLK_EN ASP_HYBRID_MODE ASP_SCPOL_IN_ADC ASP_SCPOL_IN_DAC ASP_LCPOL_OUT ASP_LCPOL_IN	00 0 0 0 0 0 0	— ASP SCLK disabled. LRCK is an input from an external source. SCLK input drive polarity for ADC is normal. SCLK input drive polarity for DAC is normal. LRCK output drive polarity is normal. LRCK input polarity (pad to logic) is normal.
4.9	Configure the ASP frame.	ASP Frame Configuration. 0x1208	0x10	
		Reserved ASP_STP ASP_5050 ASP_FSD	000 1 0 000	— Frame begins when LRCK transitions low to high LRCK duty cycle per FSYNC_PULSE_WIDTH_LB/UB Zero SCLK frame start delay
4.10	Configure the AudioPort interface.	Serial Port Receive Isochronous Control. 0x2502	0x04	
		Reserved SP_RX_RSYNC Reserved SP_RX_ISOC_MODE	0 0 00 01 00	— Serial port default receive synchronization. — Serial port receive in native mode.
4.11	Configure serial port receive channel positions.	Serial Port Receive Channel Select. 0x2501	0x04	
		Reserved SP_RX_CHB_SEL SP_RX_CHA_SEL	0000 01 00	— SP RX Channel B position is 1. SP RX Channel A position is 0.
4.12	Set receive sample rate.	Serial Port Receive Sample Rate. 0x2503	0x8C	
		Reserved SP_RX_FS	100 0 1100	— SP receive sample rate = 48 kHz.
4.13	Configure the ASP receiver.	ASP Receive Enable. 0x2A01	0x00	
		ASP_RX1_CH_EN ASP_RX0_CHF_EN ASP_RX1_2FS ASP_RX0_2FS	00 00 00 0 0	RX1 buffer is disabled. RX0 buffer is disabled. ASP DAI1 is standard sample rate. ASP DAI0 is standard sample rate.
4.14	Configure Channel 1 size to 24 bits per sample.	ASP Receive DAI0 Channel 1 Phase and Resolution. 0x2A02	0x02	
		Reserved ASP_RX0_CH1_AP Reserved ASP_RX_CH1_RES	0 0 0000 10	— In 50/50 mode, channel data valid if LRCK is low. — Size is 24 bits per sample.
4.15	Configure location of the Channel 1 MSB with respect to SOF.	ASP Receive DAI0 Channel 1 Bit Start MSB. 0x2A03	0x00	
		Reserved ASP_RX0_CH1_BIT_ST_MSB	0000 000 0	— ASP receive bit start MSB = 0.
4.16	Configure location of the Channel 1 LSB with respect to SOF.	ASP Receive DAI0 Channel 1 Bit Start LSB. 0x2A04	0x00	
		ASP_RX0_CH1_BIT_ST_LSB	0000 0000	ASP transmit bit start LSB = 0.
4.17	Configure the SRC sample rate detection.	SRC Input Sample Rate. 0x2601	0x20	
		Reserved SRC_SDIN_FS	0010 0000	— ASP sample rate is autodetected.
4.18	Configure Channel 2 size to 24 bits per sample.	ASP Receive DAI0 Channel 2 Phase and Resolution. 0x2A05	0x02	
		Reserved ASP_RX0_CH2_AP Reserved ASP_RX_CH2_RES	0 0 00 00 10	— In 50/50 mode, channel data valid if LRCK is low. — Size is 24 bits per sample.
4.19	Configure location of the Channel 2 MSB with respect to SOF.	ASP Receive DAI0 Channel 2 Bit Start MSB. 0x2A06	0x00	
		Reserved ASP_RX0_CH2_BIT_ST_MSB	0000 000 0	— ASP receive bit start MSB = 0.
4.20	Configure location of the Channel 2 LSB with respect to SOF.	ASP Receive DAI0 Channel 2 Bit Start LSB. 0x2A07	0x18	
		ASP_RX0_CH2_BIT_ST_LSB	0001 1000	ASP transmit bit start LSB = 24.
4.21	Disable the SRC bypass.	Serial Port SRC Control. 0x1007	0x10	
		Reserved EQ_BYPASS I2C_DRIVE ASP_DRIVE SRC_BYPASS_DAC SRC_BYPASS_ADC	000 1 0 0 0 0	— Bypass equalizer I^2C output drive strength normal ASP output drive strength normal SRC not bypassed for DAC path SRC not bypassed for ADC path

Example 5-1. Power-Up Sequence ***(Cont.)***

Step	Task	Register/Bit Fields	Value	Description
5	Enable SCLK.	ASP Clock Configuration 1. 0x1207	0x20	
		Reserved	00	—
		ASP_SCLK_EN	1	ASP SCLK enabled.
		ASP_HYBRID_MODE	0	LRCK is an input generated from SCLK.
		ASP_SCPOL_IN_ADC	0	SCLK input drive polarity for ADC is normal.
		ASP_SCPOL_IN_DAC	0	SCLK input drive polarity for DAC is normal.
		ASP_LCPOL_OUT	0	LRCK output drive polarity is normal.
		ASP_LCPOL_IN	0	LRCK input polarity (pad to logic) is normal.
6	Enable the ASP receiver channels.	ASP Receive Enable. 0x2A01	0x3C	
		ASP_RX1_CH_EN	00	RX1 buffer is disabled.
		ASP_RX0_CH_EN	11 11	RX0 buffer is enabled.
		ASP_RX1_2FS	0	ASP DAI1 is standard sample rate.
		ASP_RX0_2FS	0	ASP DAI0 is standard sample rate.
7	Configure the DAC.	DAC Control 1. 0x1F01	0x00	
		Reserved	0000 00	—
		DACB_INV	0	DACA signal not inverted.
		DACA_INV	0	DACB signal not inverted.
8	Configure the appropriate volume controls and DAC source selects.			
	8.1 Set Mixer A input to 0 dB.	Mixer Channel A Input Volume. 0x2301	0x00	
		Reserved	00	—
		MIXER_CHA_VOL	00 0000	Input A is set to 0 dB.
	8.2 Mute the mixer ADC input	Mixer ADC Input Volume. 0x2302	0x3F	
		Reserved	00	—
		MIXER_ADC_VOL	11 1111	Mixer ADC input is muted.
	8.3 Set Mixer B input to 0 dB.	Mixer Channel B Input Volume. 0x2303	0x00	
		Reserved	00	—
		MIXER_CHB_VOL	00 0000	Input B is set to 0 dB.
9	Configure the HP control.	HP Control. 0x2001	0x03	
		Reserved	0000	—
		ANA_MUTE_B	0	Channel B is unmuted.
		ANA_MUTE_A	0	Channel A is unmuted.
		FULL_SCALE_VOL	1	Full-scale volume is -6dB for headphone output.
		Reserved	1	—
10	Power up the codec	Power Down Control 1. 0x1101	0x96	
		ASP_DAO_PDN	1	ASP output path is powered down.
		ASP_DAI_PDN	0	ASP input path is powered up.
		MIXER_PDN	0	Mixer is powered up.
		EQ_PDN	1	Equalizer powered down
		HP_PDN	0	HPOUT powered up.
		ADC_PDN	1	ADC powered down.
		Reserved	1	—
		PDN_ALL	0	Codec powered up.
11	The headphone amplifier is operational after 10 ms.			

5.2 Power-Down Sequence

Ex. 5-2 is the procedure for powering down the HP playback.

Example 5-2. Power-Down Sequence

Step	Task	Register/Bit Fields	Value	Description
1	. Configure the DAC/Mixer Channels.			
	1.1 Mute Mixer A input.	Mixer Channel A Input Volume. 0x2301	0x3F	
		Reserved MIXER_CHA_VOL	00 11 1111	— Input A is muted.
	1.2 Mute Mixer A input.	Mixer ADC Input Volume. 0x2302	0x3F	
		Reserved MIXER_ADC_VOL	00 11 1111	— Mixer ADC input is muted.
	1.3 Mute Mixer B input.	Mixer Channel B Input Volume. 0x2303	0x3F	
		Reserved MIXER_CHB_VOL	00 11 1111	— Input B is muted.
	1.4 Mute Channel A and B inputs.	HP Control. 0x2001	0x0F	
		Reserved ANA_MUTE_B ANA_MUTE_A FULL_SCALE_VOL Reserved	0000 1 1 1 1	— Channel B is muted. Channel A is muted. Full-scale volume is –6 dB for headphone output. —
	1.5 Disable ASP_TX.	ASP Receive Enable. 0x2A01	0x00	
		ASP_RX1_CH_EN ASP_RX0_CH_EN ASP_RX1_2FS ASP_RX0_2FS	00 00 00 0 0	RX1 buffer is disabled. RX0 buffer is disabled. ASP DAI1 is standard sample rate. ASP DAI0 is standard sample rate.
	1.6 Disable SCLK.	ASP Clock Configuration 1. 0x1207	0x00	
		Reserved ASP_SCLK_EN ASP_HYBRID_MODE ASP_SCPOL_IN_ADC ASP_SCPOL_IN_DAC ASP_LCPOL_OUT ASP_LCPOL_IN	00 0 0 0 0 0 0	— ASP SCLK disabled. LRCK is an output generated from SCLK. SCLK input drive polarity for ADC is normal. SCLK input drive polarity for DAC is normal. LRCK output drive polarity is normal. LRCK input polarity (pad to logic) is normal.
2	Power down the HP amplifier.	Power Down Control 1. 0x1101	0xFE	
		ASP_DAO_PDN ASP_DAI_PDN MIXER_PDN EQ_PDN HP_PDN ADC_PDN Reserved PDN_ALL	1 1 1 1 1 1 1 0	ASP output path powered down ASP SDOUT input path is powered down Mixer is powered down Equalizer powered down HPOUT powered down ADC powered down — Codec powered up
3	Power down the ASP and SRC.	Power Down Control 2. 0x1102	0x8C	
		Reserved DISCHARGE_FILT+ SRC_PDN_OVERRIDE ASP_DAI1_PDN DAC_SRC_PDNB ADC_SRC_PDNB	100 0 1 1 0 0	— FILT+ is not clamped to ground. SRC is powered down. ASP is powered down. DAC SRC is powered down. ADC SRC is powered down.
4	Power down the codec.	Power Down Control 1. 0x1101	0xFF	
		ASP_DAO_PDN ASP_DAI_PDN MIXER_PDN EQ_PDN HP_PDN ADC_PDN Reserved PDN_ALL	1 1 1 1 1 1 1 0	ASP output path powered down ASP SDOUT input path is powered down Mixer is powered down Equalizer powered down HPOUT powered down ADC powered down — Codec powered down.
5	Read PDN_DONE to confirm that the codec is completely powered down.	Codec Interrupt Status. 0x1308	0x01	
		Reserved HSDET_AUTO_DONE PDN_DONE	0000 00 0 1	— HS detection is disabled or incomplete. Power-down done.
6	Repeat Step 5 until the PDN_DONE status bit indicates the codec has powered down.			
7	Discharge the capacitor attached to the FILT+ pin.	Power Down Control 2. 0x1102	0x9C	
		Reserved DISCHARGE_FILT+ SRC_PDN_OVERRIDE ASP_DAI1_PDN DAC_SRC_PDNB ADC_SRC_PDNB	100 1 1 1 0 0	— FILT+ is clamped to ground. SRC is powered down. ASP is powered down. DAC SRC is powered down. ADC SRC is powered down.

Example 5-2. Power-Down Sequence (Cont.)

Step	Task	Register/Bit Fields	Value	Description
8	If required, remove the SCLK signal.			
9	If required, remove all relevant power supplies from the codec.			

5.3 SoundWire Power Sequences

This section provides SoundWire power-up and power-down sequences.

5.3.1 SoundWire Power-Up Sequence

Ex. 5-3 is the procedure for implementing ADC record, HP playback, and S/PDIF Tx playback from SoundWire. This sequence configures the CS42L42 for SWIRE_CLK = 12.288 MHz, 48-kHz sample interval rate, and a 64 x 8 SoundWire frame, as described in Ex. 4-3. This example is a minimum configuration specifically for Ex. 4-3. Different SWIRE_CLK, sample interval rates, or SoundWire frames may require additional configurations.

Example 5-3. SoundWire Power-Up Sequence

Step	Task	Register/Bit Fields	Value	Description
1	Apply all relevant power supplies, then assert RESET before applying SWIRE_CLK to the CS42L42.			
2	Enumerate the codec.			
2.1	Read SCP Device ID 0, 1, 2, 3, 4, and 5 and confirm the codec device IDs.			
2.2	Assign Group ID and device number	SCP Device Number. Base + 0x46	0x01	
		Reserved GROUP_ID DEVICE_NUMBER	00 00 0001	— Group ID device number
3	Wait for 2.5 ms for codec internal initialization.			
4	Configure the device's clocking			
4.1	Configure switch from RCO to SCLK.	Oscillator Switch Control. 0x1107	0x01	
		Reserved SCLK_PRESENT	0000 000 1	— SCLK is present.
4.2	Confirm the RCO is powered down	Oscillator Switch Status. 0x1109	0x01	Read (repeat until value is 0x01)
		Reserved OSC_PDNB_STAT OSC_SW_SEL_STAT	0000 0 0 01	— RCO powered down RCO selected for internal MCLK
5	Configure the appropriate volume controls and DAC source selects			
5.1	Set Mixer A input to 0 dB.	Mixer Channel A Input Volume. 0x2301	0x3F	
		Reserved MIXER_CHA_VOL	00 11 1111	— Mixer ADC is set muted.
5.2	Set Mixer B input to 0 dB.	Mixer Channel B Input Volume. 0x2303	0x00	
		Reserved MIXER_CHB_VOL	00 00 0000	— Input B is set to 0 dB.
6	Configure the HP control.	HP Control. 0x2001	0x01	
		Reserved ANA_MUTE_B ANA_MUTE_A FULL_SCALE_VOL Reserved	0000 0 0 0 1	— Channel B is unmuted. Channel A is unmuted. Full-scale volume is 0 dB for headphone output. —
7	Configure S/PDIF clocking	S/PDIF Clock Configuration. 0x1202	0x08	
		Reserved SPDIF_CLK_DIV SPDIF_LRCK_SRC_SEL SPDIF_LRCLK_CPOL Reserved	00 00 1 0 0 0	— S/PDIF clock divide factor of 2. Use internally generated LRCLK Normal LRCLK polarity —
8	Configure the S/PDIF control.	S/PDIF Control 2. 0x2802	0x01	
		SPDIF_TX_L SPDIF_TX_PRO SPDIF_TX_AUDIOB SPDIF_TX_CP SPDIF_TX_PRE SPDIF_TX_VCFG SPDIF_TX_V SPDIF_TX_DIGEN	0 0 0 0 0 0 0 1	This data stream is a copy. Consumer format PCM format Copy inhibited No preemphasis Validity bit follows internal codec status Validity bit follows internal codec status Enable S/PDIF Transmit
9	Power up S/PDIF transmitter.	S/PDIF Control 1. 0x2801	0x00	
		SPDIF_TX_RAW SPDIF_TX_KAE SPDIF_TX_PDN	0 0 0	S/PDIF outputs 24-bit data with control info Don't care Power up S/PDIF transmitter

Example 5-3. SoundWire Power-Up Sequence *(Cont.)*

Step	Task	Register/Bit Fields	Value	Description
10	Power up the codec.	Power Down Control 1. 0x1101	0xD2	
		ASP_DAO_PDN	1	ASP output path is powered down.
		ASP_DAI_PDN	1	ASP input path is powered down.
		MIXER_PDN	0	Mixer is powered up.
		EQ_PDN	1	Equalizer is powered down
		HP_PDN	0	HPOUT is powered up.
		ADC_PDN	0	ADC is powered up.
		Reserved	1	—
		PDN_ALL	0	Codec is powered up.
11	Configure Ports 1-14 common settings			
	11.1 Ports 1-14 Control	DP1-14 Port Control (Section 7.2.3). 0x0F02	0x00	
		Reserved	000	—
		INVERT_BANK	0	Use bank as directed in the control word
		PORT_DATA_MODE	00	Normal port mode
		Reserved	00	—
	11.2 Ports 1-14 Block Control	DP1-14 Block Control 1 (Section 7.2.4). 0x0F03	0x17	
		Reserved	00	—
		WORD_LENGTH	01 0111	24-bit data
	11.3 Port 1-14 Sample Control 1—Bank 1	DP1-14 Sample Control 1 (Banked, Section 7.2.8). 0x0F32	0xFF	
		SAMPLE_INTERVAL_LOW	1111 1111	Sample interval = 512
	11.4 Port 1-14 Sample Control 2—Bank 1	DP1-14 Sample Control 2 (Banked, Section 7.2.9). 0x0F33	0x01	
		SAMPLE_INTERVAL_HIGH	0000 0001	Sample interval = 512
	11.5 Ports 1-14 Horizontal Control—Bank 1	DP1-14 Horizontal Control (Banked, Section 7.2.12). 0x0F36	0x17	
		HSTART	0001	Subframe begins in Column 1
		HSTOP	0111	Subframe ends in Column 7
	11.6 Ports 1-14 Block Control 3—Bank 1	DP1-14 Block Control 3 (Banked, Section 7.2.13). 0x0F37	0x00	
		Reserved	0000 000	—
		BLOCK_PACKING_MODE	0	Block-per-Port Mode
12	Configure Ports 1 (ADC)			
	12.1 Port 1 Offset Control 1—Bank 1	DP1 Offset Control 1 (Banked, Section 7.2.10). 0x0134	0x00	
		OFFSET1	0000 0000	Block offset = 0
	12.2 Port 1 Offset Control 2—Bank 1	DP1 Offset Control 2 (Banked, Section 7.2.11). 0x0135	0x00	
		OFFSET2	0000 0000	Block offset = 0
	12.3 Port 1 Prepare Control	DP1 Prepare Control (Section 7.2.6). 0x0105	0x01	
		Reserved	0000 00	—
		PREPARE_CHANNEL2	0	Channel deactivated
		PREPARE_CHANNEL1	1	Channel commanded to prepare for activity
	12.4 Read Port 1 prepare Status. Repeat until value is 0x00.	DP1 Prepare Status (Section 7.2.5). 0x0104	0x00	
		Reserved	0000 00	—
		NOT_FINISHED_CHANNEL2	0	Channel finished
		NOT_FINISHED_CHANNEL1	0	Channel finished
	12.5 Port 1 Channel Enable—Bank 1	DP1 Channel Enable (Banked, Section 7.2.7). 0x0130	0x01	
		Reserved	0000 00	—
		CHANNEL_EN2	0	Channel disabled
		CHANNEL_EN1	1	Channel enabled
13	Configure Port 2 (headphone data)			
	13.1 Port 2 Offset Control 1—Bank 1	DP2 Offset Control 1 (Banked, Section 7.2.10). 0x0234	0x1C	
		OFFSET1	0001 1100	Block offset = 28
	13.2 Port 2 Offset Control 2—Bank 1	DP2 Offset Control 2 (Banked, Section 7.2.11). 0x0235	0x00	
		OFFSET2	0000 0000	Block offset = 28
	13.3 Port 2 Prepare Control	DP2 Prepare Control (Section 7.2.6). 0x0205	0x03	
		Reserved	0000 00	—
		PREPARE_CHANNEL2	1	Channel commanded to prepare for activity
		PREPARE_CHANNEL1	1	Channel commanded to prepare for activity
	13.4 Read Port 2 Prepare Status. Repeat until value is 0x00.	DP2 Prepare Status (Section 7.2.5). 0x0204	0x00	
		Reserved	0000 00	—
		NOT_FINISHED_CHANNEL2	0	Channel finished
		NOT_FINISHED_CHANNEL1	0	Channel finished
	13.5 Port 2 Channel Enable—Bank 1	DP2 Channel Enable (Banked, Section 7.2.7). 0x0230	0x03	
		Reserved	0000 00	—
		CHANNEL_EN2	1	Channel enabled
		CHANNEL_EN1	1	Channel enabled

Example 5-3. SoundWire Power-Up Sequence *(Cont.)*

Step	Task	Register/Bit Fields	Value	Description
14	Configure Port 3 (S/PDIF data)			
14.1	Port 3 Offset Control 1—Bank 1	DP3 Offset Control 1 (Banked, Section 7.2.10). 0x0334	0x54	
		OFFSET1	0101 0100	Block offset = 84
14.2	Port 3 Offset Control 2—Bank 1	DP3 Offset Control 2 (Banked, Section 7.2.11). 0x0335	0x00	
		OFFSET2	0000 0000	Block offset = 84
14.3	Port 3 Prepare Control	DP3 Prepare Control (Section 7.2.6). 0x0305	0x03	
		Reserved PREPARE_CHANNEL2 PREPARE_CHANNEL1	0000 00 1 1	— Channel commanded to prepare for activity Channel commanded to prepare for activity
14.4	Read Port 3 prepare status. Repeat until value is 0x00.	DP3 Prepare Status (Section 7.2.5). 0x0304	0x00	
		Reserved NOT_FINISHED_CHANNEL2 NOT_FINISHED_CHANNEL1	0000 00 0 0	— Channel finished Channel finished
14.5	Port 3 Channel Enable—Bank 1	DP3 Channel Enable (Banked, Section 7.2.7). 0x0330	0x03	
		Reserved CHANNEL_EN2 CHANNEL_EN1	0000 00 1 1	— Channel enabled Channel enabled
15	SCP Frame Control—Bank 1	SCP Frame Control (Banked, Section 7.1.12). 0x0070	0x1B	Trigger bank switch to Bank 1
		ROW_CONTROL COLUMN_CONTROL	0001 1 011	64 rows 8 columns

5.3.2 SoundWire Power-Down Sequence with Clock Stop

Ex. 5-4 powers down ADC record, HP playback, and S/PDIF Tx playback from SoundWire. This example sequence is a minimum configuration specifically for Ex. 4-3. This sequence configures the CS42L42 for SWIRE_CLK = 12.288 MHz, 48-kHz sample-interval rate, and 64 x 8 SoundWire frame, as described in Ex. 4-3.

Different SWIRE_CLK, sample interval rates, or SoundWire frames may require additional configurations.

If clock stop is not used, omit Steps 10–15.

This procedure assumes that Bank 1 is the initial active SoundWire register bank.

Example 5-4. SoundWire Power-Down Sequence

Step	Task	Register/Bit Fields	Value	Description
1	Configure the DAC/ADC mixer channels.			
1.1	Mute Mixer A input.	Mixer Channel A Input Volume. 0x2301	0x3F	
		Reserved MIXER_CHA_VOL	00 11 1111	— Input A is muted.
1.2	Mute the mixer ADC input.	Mixer ADC Input Volume. 0x2302	0x3F	
		Reserved MIXER_ADC_VOL	00 11 1111	— Mixer ADC input is muted.
1.3	Mute Mixer B input.	Mixer Channel B Input Volume. 0x2303	0x3F	
		Reserved MIXER_CHB_VOL	00 11 1111	— Input B is muted.
1.4	Mute Channel A and B inputs.	HP Control. 0x2001	0x0F	
		Reserved ANA_MUTE_B ANA_MUTE_A FULL_SCALE_VOL Reserved	0000 1 1 1 1	— Channel B is muted. Channel A is muted. Full-scale volume is –6 dB for headphone output. —
2	Disable Port 1, 2, 3 channels			
2.1	Write to inactive Bank 0. (Port 1–14 Channel Enable–Bank 0)	DP1–14 Channel Enable 0x0F20	0x00	
		Reserved CHANNEL_EN2 CHANNEL_EN1	0000 00 0 0	— Channel disabled Channel disabled
2.2	Write. Trigger bank switch to Bank 0.	SCP Frame Control (Banked, Section 7.1.12). 0x0060	0x1B	
		ROW_CONTROL COLUMN_CONTROL	0001 1 011	64 rows 8 columns

Example 5-4. SoundWire Power-Down Sequence *(Cont.)*

Step		Task	Register/Bit Fields	Value	Description
3		Deprepare Ports 1–3			
	3.1	Write Port 1–14 Prepare Control	DP1–14 Prepare Control 0x0F05	0x00	
			Reserved	0000 00	—
			PREPARE_CHANNEL2	0	Channel deactivated
			PREPARE_CHANNEL1	0	Channel deactivated
	3.2	Read Port 1 Prepare Status. Repeat until value is 0x00.	DP1 Prepare Status (Section 7.2.5). 0x0104	0x00	
			Reserved	0000 000	—
			NOT_FINISHED_CHANNEL1	0	Channel finished
	3.3	Read Port 2 Prepare Status. Repeat until value is 0x00.	DP2 Prepare Status (Section 7.2.5). 0x0204	0x00	
			Reserved	0000 00	—
			NOT_FINISHED_CHANNEL2	0	Channel finished
			NOT_FINISHED_CHANNEL1	0	Channel finished
	3.4	Read Port 3 Prepare Status. Repeat until value is 0x00.	DP3 Prepare Status (Section 7.2.5). 0x0304	0x00	
			Reserved	0000 00	—
			NOT_FINISHED_CHANNEL2	0	Channel finished
			NOT_FINISHED_CHANNEL1	0	Channel finished
4		Power down S/PDIF transmitter.	S/PDIF Control 1. 0x2801	0x01	
			Reserved	0000 0	Reserved
			SPDIF_TX_RAW	0	S/PDIF outputs 24-bit data with control info
			SPDIF_TX_KAE	0	Don't care
			SPDIF_TX_PDN	1	Power down S/PDIF transmitter
5		Power down the HP, ADC, and mixer.	Power Down Control 1. 0x1101	0xFE	
			ASP_DAO_PDN	1	ASP output path powered down
			ASP_DAI_PDN	1	ASP SDOUT input path is powered down
			MIXER_PDN	1	Mixer is powered down
			EQ_PDN	1	Equalizer powered down
			HP_PDN	1	HPOUT powered down
			ADC_PDN	1	ADC powered down
			Reserved	1	—
			PDN_ALL	0	Codec powered up
6		Power down the ASP and SRC.	Power Down Control 2. 0x1102	0x8C	
			Reserved	100	—
			DISCHARGE_FILT+	0	FILT+ is not clamped to ground.
			SRC_PDN_OVERRIDE	1	SRC is powered down.
			ASP_DAI1_PDN	1	ASP is powered down.
			DAC_SRC_PDNB	0	DAC SRC is powered down.
			ADC_SRC_PDNB	0	ADC SRC is powered down.
7		Power down the codec.	Power Down Control 1. 0x1101	0xFF	
			ASP_DAO_PDN	1	ASP output path is powered down.
			ASP_DAI_PDN	1	ASP input path is powered down.
			MIXER_PDN	1	Mixer is powered up.
			EQ_PDN	1	Equalizer powered down
			HP_PDN	1	HPOUT powered up.
			ADC_PDN	1	ADC powered up.
			Reserved	1	—
			PDN_ALL	1	Codec powered up.
8		Read PDN_DONE to confirm that the codec is completely powered down. Repeat until value is 0x01	Codec Interrupt Status. 0x1308	0x01	
			Reserved	0000 00	—
			HSDET_AUTO_DONE	0	HS detection is disabled or incomplete.
			PDN_DONE	1	Power-down done.
9		Discharge the capacitor attached to the FILT+ pin.	Power Down Control 2. 0x1102	0x9C	
			Reserved	100	—
			DISCHARGE_FILT+	1	FILT+ is clamped to ground.
			SRC_PDN_OVERRIDE	1	SRC is powered down.
			ASP_DAI0_PDN	1	ASP is powered down.
			DAC_SRC_PDNB	0	DAC SRC is powered down.
			ADC_SRC_PDNB	0	ADC SRC is powered down.
10		Configure switch from SCLK to RCO.	Oscillator Switch Control. 0x1107	0x00	
			Reserved	0000 000	—
			SCLK_PRESENT	0	SCLK not present
11		Confirm RCO is powered up. Read the Oscillator Switch Status and repeat until the value reaches 0x05.	Oscillator Switch Status. 0x1109	0x05	
			Reserved	0000 0	—
			OSC_PDNB_STAT	1	RCO powered up
			OSC_SW_SEL_STAT	01	RCO selected for internal MCLK
12		Prepare for clock stop now	SCP System Control (Section 7.1.4) 0x0045	0x01	
			Reserved	0000	—
			WAKE_UP_ENABLE	0	Asynchronous wake disabled.
			CLOCK_STOP_MODE	0	Slave must not lose context in Clock Stop Mode.
			Reserved	0	—
			CLOCK_STOP_PREPARE	1	The CS42L42 is notified to prepare for clock stop.

Example 5-4. SoundWire Power-Down Sequence *(Cont.)*

Step	Task	Register/Bit Fields	Value	Description
13	Confirm device is ready for clock stop. Read SCP Control. Repeat until CLOCK_STOP_NOT_FINISHED is 0.	SCP Control (Section 7.1.3) 0x0044	0x00	
		FORCE_RESET	0	No action
		CURRENT_BANK	0	Current register bank is Bank 0
		Reserved	00 00	—
		CLOCK_STOP_NOW	0	Normal operation
		CLOCK_STOP_NOT_FINISHED	0	Ready for clock stop
14	Send clock stop now	SCP Control (Section 7.1.3) 0x0044	0x02	
		FORCE_RESET	0	No action
		CURRENT_BANK	0	Current register bank is Bank 0
		Reserved	00 00	—
		CLOCK_STOP_NOW	1	Clock stops after one more frame.
		CLOCK_STOP_NOT_FINISHED	0	Ready for clock stop.
15	The master sends a stopping frame and stops SWIRE_CLK at the frame boundary at the end of that frame.			

5.4 Page 0x30 Read Sequence

The following sequence is required to read from Page 0x30:

1. Power up Page 0x30 by clearing bit 7 of register 0x1102.
2. Enable Page 0x30 reads by writing the value 0x01 to register 0x1801.
3. Perform the read from Page 0x30.

5.5 PLL Clocking

Data-path logic is in the MCLK domain, where SCLK is expected to be 12 or 24 MHz. For clocking scenarios where ASP_SCLK is neither 12 nor 24 MHz, the PLL must be turned on to provide the desired internal MCLK. At startup, the system sets the SCLK bypass as default mode and switches to PLL output after it settles. PLL start-up time is a maximum of 1 ms.

5.6 Standby Mode and Headset Clamps

When the CS42L42 enters Standby Mode, headset clamps must first be disabled—HS_CLAMP_DISABLE = 1, see p. 137.

5.7 Detection Sequence from Wake

Ex. 5-5 is the procedure for implementing automatic headset-type detection from Standby Mode. Following a wake event, the system responds to the WAKE being asserted, the INT pin being asserted, or both (depending on WAKE/INT configuration) by taking the audio device out of Standby Mode, as shown in Steps 1–9.

Example 5-5. Headset Type and Load-Detection Sequence

Step	Task	Register/Bit Fields	Value	Description
1	Apply all relevant power supplies to the codec.			
2	Apply a 12.0000-MHz signal to the MCLK input.			
3	Enable the $MCLK_{INT}$.	MCLK Control. 0x1009	0x00	
		Reserved	0000 00	—
		INTERNAL_FS	0	Internal sample rate is $MCLK_{INT}$/250.
		Reserved	0	—
4	Make WAKE inactive.	Wake Control. 0x1B71	0xC0	
		M_MIC_WAKE ††	1	Mask mic button detect wake.
		M_HP_WAKE ††	1	Mask HP detect wake.
		WAKEB_MODE ††	0	WAKE latched low after a trigger event.
		—	0 0400	Reserved
		WAKEB_CLEAR	0	Normal operation.
5	Set EVENT_STATUS_SEL to bring values stored in VP domain registers into VD_FILT domain registers.	Mic Detect Control 1. 0x1B75	0x5F	
		LATCH_TO_VP	0	Enable setting of VP sticky status latches.
		EVENT_STATUS_SEL	1	Sticky processed status events are selected.
		HS_DETECT_LEVEL	01 1111	Detect percentage is set to default specified level.
6	Wait 2 µs.			

Example 5-5. Headset Type and Load-Detection Sequence *(Cont.)*

Step	Task	Register/Bit Fields	Value	Description
7	Read the detect interrupt status registers.			
7.1	Monitor the HPDETECT_PLUG and HPDETECT_UNPLUG bits.	Detect Interrupt Status 1. 0x1309	0xXX	
		HSBIAS_SENSE	x	See Section 7.6.7 for decode.
		TIP_SENSE_PLUG	1	HP plug event has occurred.
		TIP_SENSE_UNPLUG	0	No HP unplug event has occurred.
		—	x xxxx	Reserved
7.2	Read Detect Interrupt Status 2 register.	Detect Interrupt Status 2. 0x130A	0xXX	
		DETECT_TRUE_FALSE	x	See Section 7.6.8 for decodes.
		DETECT_FALSE_TRUE	x	
		—	0	
		SHORT_RELEASE	x	
		SHORT_DETECTED	x	
8	Set and then clear WAKEB_CLEAR to enable normal $\overline{\text{WAKE}}$ output operation.			
8.1	Set WAKEB_CLEAR.	Wake Control. 0x1B71	0xC1	
		M_MIC_WAKE ††	1	Mask mic button detect wake.
		M_HP_WAKE ††	1	Mask HP detect wake.
		WAKEB_MODE ††	0	Output is latched low.
		—	0 000	Reserved
		WAKEB_CLEAR	1	$\overline{\text{WAKE}}$ output deasserted.
8.2	Clear WAKEB_CLEAR.	Wake Control. 0x1B71	0xC0	
		M_MIC_WAKE ††	1	Mask mic button detect wake.
		M_HP_WAKE ††	1	Mask HP detect wake.
		WAKEB_MODE ††	0	Output is latched low.
		—	0 000	Reserved
		WAKEB_CLEAR	0	Normal $\overline{\text{WAKE}}$ output operation.
9	If Step 7 indicates an HP plug event, continue with Step 10.			
10	Set LATCH_TO_VP to enable VP domain register configuration.	Mic Detect Control 1. 0x1B75	0x9F	
		LATCH_TO_VP	1	Transfer VD_FILT fields to VP fields.
		EVENT_STATUS_SEL	0	Unprocessed status events are selected.
		HS_DETECT_LEVEL	01 1111	Detect percentage is set to default specified level.
11	Configure the automatic headset-type detection.			
11.1	Power up the codec.	Power Down Control 1. 0x1101	0xFE	
		ASP_DAO_PDN	1	ASP DAO is powered down.
		ASP_DAI_PDN	1	ASP DAI is powered down.
		MIXER_PDN	1	Mixer is powered down.
		EQ_PDN	1	EQ is powered down.
		HP_PDN	1	HP is powered down.
		ADC_PDN	1	ADC is powered down.
		Reserved	1	—
		PDN_ALL	0	Codec is powered up.
11.2	Release FILT+ clamp to ground.	Power Down Control 2. 0x1102	0x87	
		Reserved	100	—
		DISCHARGE_FILT+	0	FILT+ is not clamped to ground.
		SRC_PDN_OVERRIDE	0	SRC is powered down, per smart logic.
		ASP_DAI1_PDN	1	ASP DAI1 is powered down.
		DAC_SRC_PDN	1	DAC SRC is powered down.
		ADC_SRC_PDN	1	ADC SRC is powered down.
11.3	Configure the HP ground clamp and pull-down	DAC Control 2. 0x1F06	0x86	
		HPOUT_PULLDOWN	1000	Headphone pull-down resistor disabled
		HPOUT_LOAD†	0	1-nF Mode.
		HPOUT_CLAMP	1	Headphone clamp disabled
		DAC_HPF_EN	1	DAC HPF is enabled.
		Reserved	0	—
11.4	Configure the headset-detection block.	Miscellaneous Detect Control. 0x1B74	0x07	
		—	000	Reserved
		DETECT_MODE ††	0 0	Detect mode set to inactive.
		HSBIAS_CTRL ††	11	HSBIAS set to 2.7-V Mode.
		PDN_MIC_LVL_DETECT	1	Level detect is powered down.
11.5	Wait $t_{startup} + t_{mb\text{-}rise}$ for the HSBIAS to ramp up, as specified in Table 3-15, for the HSBIAS to ramp up.			
11.6	Configure the HSDET_AUTO_DONE interrupt mask.	Codec Interrupt Mask. 0x131B	0x01	
		Reserved	0000 00	—
		M_HSDET_AUTO_DONE	0	Interrupt is unmasked.
		M_PDN_DONE	1	Interrupt is masked.
11.7	Configure the HSDET mode to ensure initial conditions.	Headset Detect Control 2. 0x1120	0x80	
		HSDET_CTRL	10	HSDET mode set to automatic, disabled.
		HSDET_SET	00	HS3 is GND, HS4 is HSBIAS (setting is ignored).
		HSBIAS_REF	0	HSx_REF is the ground reference.
		Reserved	0	—
		HSDET_AUTO_TIME	00	Cycle time set to 10 µs.
11.8	Wait 100 µs.			

Example 5-5. Headset Type and Load-Detection Sequence *(Cont.)*

Step		Task	Register/Bit Fields	Value	Description
	11.9	Configure HS DET comparator reference levels.	Headset Detect Control 1. 0x111F	0x77	
			HSDET_COMP2_LVL HSDET_COMP1_LVL	0111 0111	Reference level is set to 2.00 V. Reference level is set to 1.00 V.
	11.10	Configure the HSDET mode.	Headset Detect Control 2. 0x1120	0xC0	
			HSDET_CTRL HSDET_SET HSBIAS_REF Reserved HSDET_AUTO_TIME	11 00 0 0 00	HSDET mode set to automatic, active. HS3 is GND, HS4 is HSBIAS (setting is ignored). HSx_REF is the ground reference. — Cycle time set to 10 µs.
12	Service the HSDET_AUTO_DONE interrupt.				
	12.1	Read HSDET_AUTO_DONE to confirm the detection cycle is complete.	Codec Interrupt Status. 0x1308	0x02	
			Reserved HSDET_AUTO_DONE PDN_DONE	0000 00 1 0	— Autotype detect has completed the detection cycle. Codec is powered up.
	12.2	Read the HSDET_TYPE to confirm the headset type.	Headset Detect Status. 0x1124	—	
			HSDET_COMP2_OUT HSDET_COMP1_OUT Reserved HSDET_TYPE	x x 0000 xx	Refer to Table 4-22 for decode. Refer to Table 4-22 for decode. — Refer to Table 4-22 for decode.
	12.3	Configure the HSDET mode.	Headset Detect Control 2. 0x1120	0x80	
			HSDET_CTRL HSDET_SET HSBIAS_REF Reserved HSDET_AUTO_TIME	10 00 0 0 00	HSDET mode set to automatic, disabled. HS3 is GND, HS4 is HSBIAS (setting is ignored). HSx_REF is the ground reference. — Cycle time set to 10 µs.
13	If headset type 1–3 is detected, the switches are set to the appropriate states automatically. Go to Step 16. If a known headset type is not detected, continue with Step 14.				
14	The system manually determines the headset type.				
	14.1	Set HSDET mode to Manual—Active.	Headset Detect Control 2. 0x1120	0x40	
			HSDET_CTRL HSDET_SET HSBIAS_REF Reserved HSDET_AUTO_TIME	01 00 0 0 00	HSDET mode set to manual, active. HS3 is GND, HS4 is HSBIAS (setting is ignored). HSx_REF is the ground reference. — Cycle time set to 10 µs.
	14.2	Open the SW_HSB_HS3 switch and close SW_HSB_HS4 for a Type 1 headset.	Headset Switch Control. 0x1121	0xA6	
			SW_REF_HSx †† SW_HSB_FILT_HSx †† SW_HSB_HSx †† SW_GNDHS_HSx ††	10 10 01 10	Ref-to-HSx (HS3 closed; HS4 open) HSBIAS_FILT-to-HSx (HS3 closed; HS4 open) HSBIAS-to-HSx (HS3 open; HS4 closed) GNDHS-to-HSx (HS3 closed; HS4 open)
	14.3	Read the output of the HSDET comparator for the Type 1 headset result.	Headset Detect Status. 0x1124	—	
			HSDET_COMP2_OUT HSDET_COMP1_OUT Reserved HSDET_TYPE	xx xx 00 xx	Refer to Table 4-22 for decode. Refer to Table 4-22 for decode. — Unused in this mode
	14.4	Close the SW_HSB_HS3 switch for a Type 2 headset.	Headset Switch Control. 0x1121	0x59	
			SW_REF_HSx †† SW_HSB_FILT_HSx †† SW_HSB_HSx †† SW_GNDHS_HSx ††	01 01 10 01	Ref-to-HSx (HS3 open; HS4 closed) HSBIAS_FILT-to-HSx (HS3 open; HS4 closed) HSBIAS-to-HSx (HS3 closed; HS4 open) GNDHS-to-HSx (HS3 open; HS4 closed)
	14.5	Read the output of the HSDET comparator for the Type 2 headset result.	Headset Detect Status. 0x1124	—	
			HSDET_COMP2_OUT HSDET_COMP1_OUT Reserved HSDET_TYPE	xx xx 00 xx	Refer to Table 4-22 for decode. Refer to Table 4-22 for decode. — Unused in this mode
15	Based on the results of the comparator reading, set all of the switches to their appropriate states.				
	15.1	Set switches.	Headset Switch Control. 0x1121	0xXX	
			SW_REF_HSx †† SW_HSB_FILT_HSx †† SW_HSB_HSx †† SW_GNDHS_HSx ††	xx xx xx xx	See Section 7.4.13, "Headset Switch Control."
	15.2	Set HSDET mode to Manual—Disabled.	Headset Detect Control 2. 0x1120	0x00	
			HSDET_CTRL HSDET_SET HSBIAS_REF Reserved HSDET_AUTO_TIME	00 00 0 0 00	HSDET mode set to manual, disabled. HS3 is GND, HS4 is HSBIAS (setting is ignored). HSx_REF is the ground reference. — Cycle time set to 10 µs.
16	If external switches are used, set them according to Table 4-23, making sure to disable GNDHS_HS3 and GNDHS_HS4 after external switch states are set appropriately.				

Example 5-5. Headset Type and Load-Detection Sequence *(Cont.)*

Step	Task	Register/Bit Fields	Value	Description
17	Enable the HPOUT ground clamp and configure the HP pull-down	DAC Control 2. 0x1F06	0x02	
		HPOUT_PULLDOWN	0000	0.9 kΩ
		HPOUT_LOAD†	0	1-nF Mode.
		HPOUT_CLAMP	0	Clamp to ground if channels are powered down
		DAC_HPF_EN	1	DAC HPF is enabled.
		Reserved	0	—
18	After type detection completes, load detection is initiated to ensure proper compensation for the headphone amplifier. **Note:** Several bits must be set to ensure proper load detection; some are not explicitly set in the load-detect portion of the sequence (Steps 19–31). This is because these values are either set in the type-detection portion of the sequence or are the default values (assuming that they have not been programmed otherwise). However, ensure the bit values listed below are set when beginning the load-detection portion of the sequence: PDN_ALL = 0, ADC_PDN = 1, HP_PDN = 1, ANA_MUTE_A = 1, ANA_MUTE_B = 1, LATCH_TO_VP = 1, HSBIAS_CTRL = 00, ADPTPWR = 100, ASR_RATE = 0111, DSR_RATE = 0001. After load detection is complete, the fields listed above must be restored to their previous values.			
19	Power down the HP.	Power Down Control 1. 0x1101	0xFE	
		ASP_DAO_PDN	1	ASP DAO is powered down.
		ASP_DAI_PDN	1	ASP DAI is powered down.
		MIXER_PDN	1	Mixer is powered down.
		EQ_PDN	1	EQ is powered down.
		HP_PDN	1	HP is powered down.
		ADC_PDN	1	ADC is powered down.
		Reserved	1	—
		PDN_ALL †	0	Codec is powered up.
20	Set HSBIAS_CTRL to Hi-Z Mode.	Miscellaneous Detect Control. 0x1B74	0x01	
		Reserved	000	—
		DETECT_MODE ††	0 0	Detect mode set to inactive.
		HSBIAS_CTRL ††	00	HSBIAS set to Hi-Z Mode.
		PDN_MIC_LVL_DETECT	1	Level detect is powered down.
21	Set ADPTPWR to Fixed, Mode 3 (±VCP/3).	Class H Control. 0x1101	0x04	
		Reserved	0000 0	—
		ADPTPWR	100	Fixed, Mode 3 (±VCP/3)
22	Set the analog and digital soft ramp rates.	Soft Ramp Rate. 0x100A	0x71	
		ASR_RATE	0111	Analog soft ramp is 16 Fs periods between steps.
		DSR_RATE	0001	Digital soft ramp is 2 Fs period between steps.
23	Enable HP load detect.	HP Load Detect Enable. 0x1927	0x01	
		Reserved	0000 000	—
		HP_LD_EN	1	HP load detect enabled.
24	Read HPLOAD_DET_DONE to ensure load detection is complete. Repeat until value is 1.	HP Load Detect Done. 0x1926	0xXX	
		Reserved	0000 000	—
		HPLOAD_DET_DONE	x	0: Load detect not finished, 1: Load detect finished.
25	Read load R/C status.	Load-Detect R/C Status. 0x1925	0xXX	
		Reserved	000	—
		CLA_STAT	x	HPOUT_LOAD is programmed according to the values read back.
		Reserved	00	
		RLA_STAT	xx	
26	Set HPOUT_LOAD according to CLA_STAT and RLA_STAT values.	DAC Control 2. 0x1F06	0x0X	
		HPOUT_PULLDOWN	0000	0.9 kΩ
		HPOUT_LOAD†	x	0: 1-nF Mode, 1: 10-nF Mode.
		HPOUT_CLAMP	0	Clamp to ground if channels are powered down
		DAC_HPF_EN	1	DAC HPF is enabled.
		Reserved	0	—
27	Restore ADPTPWR Adapt-to-Signal Mode.	Class H Control. 0x2101	0x07	
		Reserved	0000 0	—
		ADPTPWR	111	Adapt to signal.
28	Set HSBIAS_CTRL back to 2.7-V Mode.	Miscellaneous Detect Control. 0x1B74	0x07	
		Reserved	000	—
		DETECT_MODE ††	0 0	Detect mode set to inactive.
		HSBIAS_CTRL ††	11	HSBIAS set to 2.7-V Mode.
		PDN_MIC_LVL_DETECT	1	Level detect is powered down.
29	Power up the HP again.	Power Down Control 1. 0x1101	0xF6	
		ASP_DAO_PDN	1	ASP DAO is powered down.
		ASP_DAI_PDN	1	ASP DAI is powered down.
		MIXER_PDN	1	Mixer is powered down.
		EQ_PDN	1	EQ is powered down.
		HP_PDN	0	HP is powered up.
		ADC_PDN	1	ADC is powered down.
		Reserved	1	—
		PDN_ALL ††	0	Codec is powered up.

Example 5-5. Headset Type and Load-Detection Sequence *(Cont.)*

Step	Task	Register/Bit Fields	Value	Description
30	Set the analog and digital soft ramp rates.	Soft Ramp Rate. 0x100A	0xA4	
		ASR_RATE DSR_RATE	1010 0100	Analog soft ramp is 33 Fs periods between steps. Digital soft ramp is 8 Fs periods between steps.
31	Disable HP load detection.	HP Load Detect Enable. 0x1927	0x00	
		Reserved HP_LD_EN	0000 000 0	— HP load detect disabled.
32	Load detection is complete.			
33	Clear LATCH_TO_VP to disable VP domain register configuration.	Mic Detect Control 1. 0x1925	0x1F	
		LATCH_TO_VP EVENT_STATUS_SEL HS_DETECT_LEVEL	0 0 01 1111	No transfer of VD_FILT fields to VP fields. Unprocessed status events are selected. Detect percentage is set to default specified level.
34	If necessary, set ADC1x_INV to correct the signal polarity.	ADC Control. 0x1D01	0x0C	
		Reserved ADC_NOTCH_DIS ADC_FORCE_WEAK_VCM Reserved ADC_INV Reserved ADC_DIG_BOOST	00 0 0 1 1 0 0	— ADC digital notch filter enabled. Normal operation — ADC signal polarity inverted. — No digital boost applied.
35	Configure the codec and begin normal operation.			

† Indicates bit fields for which the provided values are typical, but are not required for configuring the key functionality of the sequence. In the target application, these fields can be set as desired without affecting the configuration goal of this start-up sequence. The description of PDN_ALL on p. 132 describes the interdependency between LATCH_TO_VP and PDN_ALL.

†† Indicates bit fields for which changes do not take effect until LATCH_TO_VP is set.

5.8 VD_FILT/VL ESD Diode

Note the following:

- If VD_FILT is supplied externally, VL must be supplied before VD_FILT.
- If the internal LDO is enabled, it generates VD_FILT from VL.
- If the LDO is disabled ($\overline{\text{DIGLDO\_PDN}}$ asserted) and VD_FILT is supplied externally; however, the LDO diode could be forward biased in cases where VD_FILT is supplied first.
- If the LDO is disabled and VD_FILT and VL are respectively powered via separate 1.2- and 1.8-V supplies, it is recommended to have an ESD diode between VD_FILT and VL.

5.9 External Output Switch Considerations

The CS42L42 headset interface can be used with two external switches tying HPOUTA/B to HPSENSA/B, thus using a closed-loop method that enables the headphone amplifier to include the switch impedance in its feedback point. This method can improve output performance if the guidelines listed in Section 4.4.2 are followed.

However, if these switches are used, HP_PDN (see p. 131) must be managed properly. HP_PDN must be set before opening these switches and the switches must be closed before clearing HP_PDN. If the headphone amplifier is still powered up while the switches are open, improper output occurs even if the headphone output is muted.

6 Register Quick Reference

Table 6-1 lists the register page addresses for each module. Section 4.8.9 describes how the page value maps to the address field (RegAddr[15:0]) for SoundWire read/write commands.

Table 6-1. Register Base Addresses

Module Group	Page	Module	Reference
SoundWire	0x00	Control port 0	Section 6.2 on p. 105
See Section 6.1.	0x01–0x03	Data ports 1–3 (See Table 4-10. "Base Addresses for Data Port Registers")	Section 6.3 on p. 106
	0x04–0x0E	Reserved	—
	0x0F	Data port 15 (See Table 4-10. "Base Addresses for Data Port Registers")	Section 6.3 on p. 106
Chip-Level	0x10	Global	Section 6.4 on p. 107
	0x11	Power-down and headset detect	Section 6.5 on p. 108
	0x12	Clocking	Section 6.6 on p. 109
	0x13	Interrupt	Section 6.7 on p. 109
	0x14	Reserved	—
	0x15	Fractional-N PLL	Section 6.8 on p. 111
	0x16–0x18	Reserved	—
	0x19	Headphone load detect	Section 6.9 on p. 111
	0x1A	Reserved	—
Analog Input	0x1B	Headset Interface	Section 6.10 on p. 111
	0x1C	Headset bias	Section 6.11 on p. 112
	0x1D	ADC	Section 6.12 on p. 112
	0x1E	Reserved	—
Analog Outputs	0x1F	DAC	Section 6.13 on p. 113
	0x20	HP control	Section 6.14 on p. 113
	0x21	Class H	Section 6.15 on p. 113
	0x22	Reserved	—
Internal Modules	0x23	Mixer volume	Section 6.16 on p. 113
	0x24	Equalizer	Section 6.17 on p. 114
	0x25	AudioPort interface	Section 6.18 on p. 114
	0x26	SRC	Section 6.19 on p. 115
	0x27	DMA	Section 6.20 on p. 115
Serial Ports	0x28	S/PDIF	Section 6.21 on p. 113
	0x29	ASP transmit	Section 6.22 on p. 116
	0x2A	ASP receive	Section 6.23 on p. 116
—	0x2B–0x2F	Reserved	—
ID registers	0x30	ID registers	Section 6.24 on p. 117
—	0x31–0xFF	Reserved	—

Notes:

- Default values are shown below the bit field names.
- Default bits marked "x" are reserved or undetermined.
- Fields shown in red are controls that are also located in the VP power supply domain.
- Fields shown in turquoise are status indicators from the VP power supply domain that are selectively raw or sticky.
- Fields shown in orange are affected by the FREEZE bit (see p. 129).

6.1 SoundWire Address Maps

Table 6-2 provides the address maps for the SoundWire slave ports.

Table 6-2. Slave Control Port Register Address Map

Address	Name	Banked?	Access Restrictions	Notes
0x0000–0x003F	Reserved	—	None	—
0x0040	SCP Interrupt Status 1	No	R/W1C	Interrupt status
0x0041	SCP Interrupt Mask 1	No	None	Interrupt enable mask
0x0042–0x0043	Reserved	—	None	—
0x0044	SCP Control	No	None	Miscellaneous control
0x0045	SCP System Control	No	None	System control
0x0046	SCP Device Number	No	None	Device selection control
0x0047–0x004F	Reserved	—	None	—
0x0050	SCP Device ID 0	No	R/O	Device identification
0x0051	SCP Device ID 1	No	R/O	Device identification
0x0052	SCP Device ID 2	No	R/O	Device identification
0x0053	SCP Device ID 3	No	R/O	Device identification
0x0054	SCP Device ID 4	No	R/O	Device identification
0x0055	SCP Device ID 5	No	R/O	Device identification
0x0056–0x005F	Reserved	—	None	—
0x0060	SCP Frame Control	Yes (Bank 0)	W/O	(Bank 0) Controls frame shape (rows and columns)
0x0061–0x006F	Reserved	—	None	—
0x0070–0x007F	(Bank 1)	Yes (Bank 1)	Same as Bank 0	Bank 1 registers have the same bit definitions as corresponding Bank 0 registers at +0x60–+0x6F
0x0080–0x00BF	Reserved	—	None	—
0x00C0	General Interrupt Status 1 Register	No	R/O	CS42L42-defined interrupt status
0x00C1	General Interrupt Mask 1 Register	No	None	CS42L42-defined interrupt enable mask
0x00C2	General Interrupt Status 2 Register	No	R/O	CS42L42-defined interrupt status
0x00C3	General Interrupt Mask 2 Register	No	None	CS42L42-defined interrupt enable mask
0x00C4–0x00CF	Reserved	—	Reserved	Reserved
0x00D0	Memory Access Status	—	R/O	Memory access status
0x00D1	Memory Access Control	—	R/W	Memory access control
0x00D2	Memory Access Timeout	—	R/W1C	Memory access timeout control
0x00D3	Reserved	—	R/O	Reserved
0x00D4	Memory Read Last Address 0	—	R/O	Status registers reporting address of read through the APB bridge via control-word command.
0x00D5	Memory Read Last Address 1	—	R/O	
0x00D6–0x00D7	Reserved	—	R/O	Reserved
0x00D8	Memory Read Data	No	R/O	Last data value returned on a control-word read
0x00D9–0x00FF	Reserved	—	R/O	Reserved

Table 6-3. Data Port Registers Address Map

Address Offset	Name [1]	Banked?	Access Restrictions	Notes
+0x00–+0x01	Reserved	—	—	—
+0x02	DP*n* Port Control	No	None	Miscellaneous port control functions (PortFlowMode optional)
+0x03	DP*n* Block Control 1	No	None	Word length
+0x04	DP*n* Prepare Status	No	R/O	Channel prepare status
+0x05	DP*n* Prepare Control	No	None	Channel prepare control
+0x06–+0x1F	Reserved	—	—	—
+0x20	DP*n* Channel Enable	Yes	None	Bank 0 channel enables
+0x21	Reserved	—	—	—
+0x22	DP*n* Sample Control 1	Yes	None	Bank 0 payload control
+0x23	DP*n* Sample Control 2	Yes	None	Bank 0 payload control
+0x24	DP*n* Offset Control 1	Yes	None	Bank 0 payload control
+0x25	DP*n* Offset Control 2	Yes	None	Bank 0 payload control
+0x26	DP*n* Horizontal Control	Yes	None	Bank 0 payload control
+0x27	DP*n* Block Control 3	Yes	None	Bank 0 payload control
+0x28–+0x2F	Reserved	—	—	—
+0x30–+0x37	(Bank 1)	Yes	Same as Bank 0	Bank 1 registers have the same bit definitions as corresponding Bank 0 registers at +0x20–+0x2F
+0x38–+0xFF	Reserved	—	—	—

1. For real data ports, *n* is in the range 1–3.

6.2 Slave Control Port Registers

Slave Control Port Registers									
Address	**Function**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x0000–0x003F	Reserved	—							
0x0040	SCP Interrupt Status	—	PORT3_CASCADE	PORT2_CASCADE	PORT1_CASCADE	—	GEN_INT_CASCADE	STAT_BUS_CLASH	STAT_PARITY
		R/O						R/W1C	
p. 118		0	0	0	0	0	0	0	0
0x0041	SCP Interrupt Mask 1	—						MASK_BUS_CLASH	MASK_PARITY
		—						R/W	
p. 118		0	0	0	0	0	0	0	0
0x0042–0x0043	Reserved	—							
0x0044	SCP Control	FORCE_RESET	CURRENT_BANK	—				CLOCK_STOP_NOW	CLOCK_STOP_NOT_FINISHED
		W/O	R/O	R/O				W/O	R/O
p. 118		0	0	0	0	0	0	0	1
0x0045	SCP System Control	—				WAKE_UP_ENABLE	CLOCK_STOP_MODE	—	CLOCK_STOP_PREPARE
		—				R/W	R/W	—	R/W
p. 119		0	0	0	0	0	0	0	0
0x0046	SCP Device Number	—		GROUP_ID		DEVICE_NUMBER			
		—		R/W					
p. 119		0	0	0	0	0	0	0	0
0x0047–0x0049	Reserved	—							
0x0050	SCP Device ID 0	SOUNDWIRE_VERSION (DeviceID[47:44])				INSTANCE (DeviceID[43:40])			
		R/O							
p. 120		0	0	0	0	0	0	See p. 120	
0x0051	SCP Device ID 1	MIPI_MANUFACTURER_ID[15:8] (DeviceID[39:32])							
		R/O							
p. 120		0	0	0	0	0	0	0	1
0x0052	SCP Device ID 2	MIPI_MANUFACTURER_ID[7:0] (DeviceID[31:24])							
		R/O							
p. 120		1	1	1	1	1	0	1	1
0x0053	SCP Device ID 3	PART_ID [15:8] (DeviceID[23:16])							
		R/O							
p. 120		0	1	0	0	0	0	1	0
0x0054	SCP Device ID 4	PART_ID [7:0] (DeviceID[15:8])							
		R/O							
p. 121		1	0	0	0	0	0	1	1
0x0055	SCP Device ID 5	CLASS (DeviceID[7:0])							
		R/O							
p. 121		0	0	0	0	0	0	0	0
0x0056–0x005F	Reserved	—							
0x0060	SCP Frame Control	ROW_CONTROL					COLUMN_CONTROL		
		W/O							
p. 121		0	0	0	0	0	0	0	0
0x0061–0x00BF	Reserved	—							
0x00C0	General Interrupt Status 1 Register	GEN_INT_STAT2_CASCADE	—						SCP_IMP_DEF1
		R/O	—						R/W1C
p. 121		0	0	0	0	0	0	0	0
0x00C1	General Interrupt Mask 1 Register	—							M_SCP_IMP_DEF1
		—							R/W
p. 122		0	0	0	0	0	0	0	0
0x00C2	General Interrupt Status 2 Register	—					INT_STAT_LATE_RESP	INT_STAT_TIMEOUT_ERR	—
		—					R/W1C	R/W1C	—
p. 122		0	0	0	0	0	0	0	0
0x00C3	General Interrupt Mask 2 Register	—					M_LATE_RESP	M_TIMEOUT_ERR	—
		—					R/W	R/W	—
p. 122		0	0	0	0	0	0	0	0
0x00C4–0x00CF	Reserved	—							

Slave Control Port Registers

Address	Function	7	6	5	4	3	2	1	0
0x00D0	Memory Access Status	—				LAST_LATE	CMD_IN_PROGRESS	CMD_DONE	RDATA_RDY
		—				R/O			
p. 123		0	0	0	0	0	0	0	0
0x00D1	Memory Access Control	—						LATE_RESP	
		—						R/W	R/W
p. 123		0	0	0	0	0	0	0	1
0x00D2	Memory Access Timeout	—				TIMEOUT_DISABLE	TIMEOUT_CTRL		
		—				R/W			
p. 124		0	0	0	0	0	0	0	0
0x00D3	Reserved	—							
0x00D4	Memory Read Last Address 0	MEM_READ_LAST_ADDR[7:0]							
		R/O							
p. 124		0	0	0	0	0	0	0	0
0x00D5	Memory Read Last Address 1	MEM_READ_LAST_ADDR[15:8]							
		R/O							
p. 124		0	0	0	0	0	0	0	0
0x00D6–0x00D7	Reserved	—							
0x00D8	Memory Read Data 0	MEM_READ_DATA[7:0]							
		R/O							
p. 124		0	0	0	0	0	0	0	0
0x00D9–0x00FF	Reserved	—							

6.3 Slave Data Port 1–3, 15 Registers

Port 1 base address = 0x0100; Port 2 base address = 0x0200; Port 3 base address = 0x0300; Port 15 base address = 0x0F00

Slave Data Port 1–3, 15 Registers

Address	Function	7	6	5	4	3	2	1	0
+0x00	DP*n* Interrupt Status	—						STAT_PORT_READY	STAT_TEST_FAIL
		—						R/W1C	
p. 124		0	0	0	0	0	0	0	0
+0x01	DP*n* Interrupt Mask	—						PORT_READY_M	TEST_FAIL_M
		—						R/W	
p. 125		0	0	0	0	0	0	0	0
+0x02	DP*n* Port Control	—			INVERT_BANK	PORT_DATA_MODE		—	
		—			R/W				
p. 125		0	0	0	0	0	0	0	0
+0x03	DP*n* Block Control 1	—		WORD_LENGTH					
		—		R/W					
p. 125		0	0	0	0	0	0	0	0
+0x03–+0x04	Reserved	—							
+0x04	DP*n* Prepare Status	—						NOT_FINISHED_CHANNEL2	NOT_FINISHED_CHANNEL1
		R/O							
p. 126		0	0	0	0	0	0	0	0
+0x05	DP*n* Prepare Control	—						PREPARE_CHANNEL2	PREPARE_CHANNEL1
		R/W							
p. 126		0	0	0	0	0	0	0	0
+0x06–+0x1F	Reserved	—							
+0x20	DP*n* Channel Enable	—						CHANNEL_EN2	CHANNEL_EN1
		R/W							
p. 126		0	0	0	0	0	0	0	0
+0x21	Reserved	—							
+022	DP*n* Sample Control 1	SAMPLE_INTERVAL_LOW							
		R/W							
p. 126		0	0	0	0	0	0	0	1
+0x23	DP*n* Sample Control 2	SAMPLE_INTERVAL_HIGH							
		R/W							
p. 127		0	0	0	0	0	0	0	0

Slave Data Port 1–3, 15 Registers									
Address	**Function**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
+0x24	DP*n* Offset Control 1	OFFSET1							
		R/W							
p. 127		0	0	0	0	0	0	0	0
+0x25	DP*n* Offset Control 2	OFFSET2							
		R/W							
p. 127		0	0	0	0	0	0	0	0
+0x26	DP*n* Horizontal Control	HSTART				HSTOP			
		R/W							
p. 127		0	0	0	0	0	0	0	0
+0x27	DP*n* Block Control 3	—							BLOCK_ PACKING_ MODE
		—							R/W
p. 128		0	0	0	0	0	0	0	0
+0x28–+0xFF	Reserved	—							

6.4 Global Registers

I²C Address: 10010(AD1)(AD0)[R/W] through 10010(AD1)(AD0)0 = 0x94(Write); 10010(AD1)(AD0)1 = 0x95 (Read)									
Page 0x10—Global Registers									
Address	**Function**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x00	Control Port Page	PAGE							
		0	0	0	1	0	0	0	0
0x01	Device ID A and B (Read Only)	DEVIDA				DEVIDB			
p. 128		0	1	0	0	0	0	1	0
0x02	Device ID C and D (Read Only)	DEVIDC				DEVIDD			
p. 128		1	0	1	0	0	1	0	0
0x03	Device ID E and F (Read Only)	DEVIDE				—			
p. 128		0	0	1	0	x	x	x	x
0x04	Reserved	—							
		x	x	x	x	x	x	x	x
0x05	Revision ID (Read Only)	AREVID				MTLREVID			
p. 128		x	x	x	x	x	x	x	x
0x06	Freeze Control	—							FREEZE
p. 129		0	0	0	0	0	0	0	0
0x07	Serial Port SRC Control	—			EQ_BYPASS	I2C_DRIVE	ASP_DRIVE	SRC_ BYPASS_DAC	SRC_ BYPASS_ADC
p. 129		0	0	0	1	0	0	0	0
0x08	MCLK Status (Read Only)	—						INTERNAL_ FS_STAT	—
p. 129		0	0	0	0	0	0	x	0
0x09	MCLK Control	—						INTERNAL_FS	—
p. 130		0	0	0	0	0	0	1	0
0x0A	Soft Ramp Rate	ASR_RATE				DSR_RATE			
p. 130		1	0	1	0	0	1	0	0
0x0B	Slow Start Enable	—	SLOW_START_EN			—			
p. 130		0	1	1	1	0	0	0	0
0x0C–0x0D	Reserved	—							
		x	x	x	x	x	x	x	x
0x0E	I²C Debounce	I2C_SDA_DBNC_CNT			I2C_SDA_ DBNC_EN	I2C_SCL_DBNC_CNT			I2C_SCL_ DBNC_EN
p. 131		1	0	0	0	1	0	0	0
0x0F	I²C Stretch	I2C_STRETCH							
p. 131		0	0	0	0	0	0	1	1
0x10	I²C Timeout	MAS_I2C_ NACK	MAS_TO_DIS	MAS_TO_SEL		ACC_TO_DIS	ACC_TO_SEL		
p. 131		1	0	1	1	0	1	1	1
0x11–0x7F	Reserved	—							
		x	x	x	x	x	x	x	x

6.5 Power-Down and Headset-Detect Registers

I²C Address: 10010(AD1)(AD0)[R/W] through 10010(AD1)(AD0)0 = 0x94(Write); 10010(AD1)(AD0)1 = 0x95 (Read)									
Page 0x11—Power-Down and Headset-Detect Registers									
Address	**Function**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x00	Control Port Page	PAGE							
		0	0	0	1	0	0	0	1
0x01	Power Down Control 1	ASP_DAO_PDN	ASP_DAI_PDN	MIXER_PDN	EQ_PDN	HP_PDN	ADC_PDN	—	PDN_ALL
p. 131		1	1	1	1	1	1	1	1
0x02	Power Down Control 2	—			DISCHARGE_FILT+	SRC_PDN_OVERRIDE	ASP_DAI1_PDN	DAC_SRC_PDNB	ADC_SRC_PDNB
p. 132		1	0	0	0	0	1	0	0
0x03	Power Down Control 3	—	SW_CLK_STP_STAT_SEL		—		VPMON_PDNB	RING_SENSE_PDNB	
p. 133		0	0	1	0	0	0	0	0
0x04	Ring Sense Control 1	—	RING_SENSE_PU_HIZ	—		HSBIAS_FILT_REF_RS	HP_REF_RS	RS_TRIM_T	RS_TRIM_R
p. 133		0	1	0	0	0	0	0	0
0x05	Ring Sense Control 2	TS_RS_GATE	—						
p. 134		0	0	0	0	0	0	0	0
0x06	Reserved	—							
		x	x	x	x	x	x	x	x
0x07	Oscillator Switch Control	—							SCLK_PRESENT
p. 134		0	0	0	0	0	0	0	0
0x08	Reserved	—							
		x	x	x	x	x	x	x	x
0x09	Oscillator Switch Status (Read Only)	—					OSC_PDNB_STAT	OSC_SW_SEL_STAT	
p. 134		0	0	0	0	0	1	0	1
0x0A–0x11	Reserved	—							
		x	x	x	x	x	x	x	x
0x12	Ring Sense Control 3	RS_INV	RS_PU_EN	RS_FALL_DBNCE_TIME			RS_RISE_DBNCE_TIME		
p. 134		0	0	0	1	1	0	1	1
0x13	Tip Sense Control 1	TS_INV	—	TS_FALL_DBNCE_TIME			TS_RISE_DBNCE_TIME		
p. 135		0	0	0	1	1	0	1	1
0x 14	Reserved	—							
		x	x	x	x	x	x	x	x
0x15	Tip Sense/Ring Sense Indicator Status (Read Only)	—				TS_UNPLUG_DBNC	TS_PLUG_DBNC	RS_UNPLUG_DBNC	RS_PLUG_DBNC
p. 135		0	0	0	0	x	x	x	x
0x16–0x1E	Reserved	—							
		x	x	x	x	x	x	x	x
0x1F	Headset Detect Control 1	HSDET_COMP2_LVL				HSDET_COMP1_LVL			
p. 135		0	1	1	1	0	1	1	1
0x20	Headset Detect Control 2	HSDET_CTRL		HSDET_SET		HSBIAS_REF	—	HSDET_AUTO_TIME	
p. 136		0	0	0	0	0	0	0	0
0x21	Headset Switch Control	SW_REF_HS3	SW_REF_HS4	SW_HSB_FILT_HS3	SW_HSB_FILT_HS4	SW_HSB_HS3	SW_HSB_HS4	SW_GNDHS_HS3	SW_GNDHS_HS4
p. 136		1	1	1	1	0	0	1	1
0x 22–0x23	Reserved	—							
		x	x	x	x	x	x	x	x
0x24	Headset Detect Status (Read Only)	HSDET_COMP2_OUT	HSDET_COMP1_OUT	—				HSDET_TYPE	
p. 137		x	x	0	0	0	x	x	x
0x 25–0x28	Reserved	—							
		x	x	x	x	x	x	x	x
0x29	HS Clamp Disable	—							HS_CLAMP_DISABLE
p. 137		0	0	0	0	0	0	0	0
0x2A–0x7F	Reserved	—							
		x	x	x	x	x	x	x	x

6.6 Clocking Registers

I²C Address: 10010(AD1)(AD0)[R/W] through 10010(AD1)(AD0)0 = 0x94 (Write); 10010(AD1)(AD0)1 = 0x95 (Read)									
Page 0x12—Clocking Registers									
Address	**Function**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x00	Control Port Page	PAGE							
		0	0	0	1	0	0	1	0
0x01	MCLK Source Select	—						MCLKDIV	MCLK_SRC_SEL
p. 137		0	0	0	0	0	0	0	0
0x02	S/PDIF Clock Configuration	—		SPDIF_CLK_DIV			SPDIF_LRCK_SRC_SEL	SPDIF_LRCK_CPOL	—
p. 137		0	0	0	0	0	0	0	0
0x03	FSYNC Pulse Width Lower Byte	FSYNC_PULSE_WIDTH_LB							
p. 138		0	0	0	0	0	0	0	0
0x04	FSYNC Pulse Width Upper Byte	—					FSYNC_PULSE_WIDTH_UB		
p. 138		0	0	0	0	0	0	0	0
0x05	FSYNC Period Lower Byte	FSYNC_PERIOD_LB							
p. 138		1	1	1	1	1	0	0	1
0x06	FSYNC Period Upper Byte	—				FSYNC_PERIOD_UB			
p. 138		0	0	0	0	0	0	0	0
0x07	ASP Clock Configuration 1	—		ASP_SCLK_EN	ASP_HYBRID_MODE	ASP_SCPOL_IN_ADC	ASP_SCPOL_IN_DAC	ASP_LCPOL_OUT	ASP_LCPOL_IN
p. 139		0	0	0	0	0	0	0	0
0x08	ASP Frame Configuration	—			ASP_STP	ASP_5050	ASP_FSD		
p. 139		0	0	0	1	0	0	0	0
0x09	Fs Rate Enable	—				FS_EN			
p. 139		0	0	0	0	0	0	0	0
0x09	Fs Rate Enable	—						FS_EN	
p. 139		0	0	0	0	0	0	0	0
0x0A	Input ASRC Clock Select	—						CLK_IASRC_SEL	
p. 140		0	0	0	0	0	0	0	0
0x0B	Output ASRC Clock Select	—						CLK_OASRC_SEL	
p. 140		0	0	0	0	0	0	0	0
0x0C	PLL Divide Configuration 1	—						SCLK_PREDIV	
p. 140		0	0	0	0	0	0	0	0
0x0D–0x7F	Reserved	—							
		x	x	x	x	x	x	x	x

6.7 Interrupt Registers

I²C Address: 10010(AD1)(AD0)[R/W] through 10010(AD1)(AD0)0 = 0x94 (Write); 10010(AD1)(AD0)1 = 0x95 (Read)									
Page 0x13—Interrupt Registers									
Address	**Function**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x00	Control Port Page	PAGE							
		0	0	0	1	0	0	1	1
0x01	ADC Overflow Interrupt Status (Read Only)	—							ADC_OVFL
p. 140		0	0	0	0	0	0	0	x
0x02	Mixer Interrupt Status (Read Only)	—				EQ_BIQUAD_OVFL	EQ_OVFL	MIX_CHA_OVFL	MIX_CHB_OVFL
p. 140		0	0	0	0	x	x	x	x
0x03	SRC Interrupt Status (Read Only)	—				SRC_OUNLK	SRC_IUNLK	SRC_OLK	SRC_ILK
p. 141		0	0	0	0	x	x	x	x
0x04	ASP RX Interrupt Status (Read Only)	—			ASPRX_OVLD	ASPRX_ERROR	ASPRX_LATE	ASPRX_EARLY	ASPRX_NOLRCK
p. 141		0	0	0	x	x	x	x	x
0x05	ASP TX Interrupt Status (Read Only)	—				ASPTX_SMERROR	ASPTX_LATE	ASPTX_EARLY	ASPTX_NOLRCK
p. 142		0	0	0	0	x	x	x	x
0x06–0x07	Reserved	—							
		x	x	x	x	x	x	x	x
0x08	Codec Interrupt Status (Read Only)	—						HSDET_AUTO_DONE	PDN_DONE
p. 142		0	0	0	0	0	0	x	x

I^{2}C Address: 10010(AD1)(AD0)[R/$\overline{W}$] through 10010(AD1)(AD0)0 = 0x94 (Write); 10010(AD1)(AD0)1 = 0x95 (Read)									
Page 0x13—Interrupt Registers									
Address	**Function**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x09 p. 142	Detect Status 1 (Read Only)	HSBIAS_SENSE	TIP_SENSE_PLUG	TIP_SENSE_UNPLUG	—				
		x	x	x	x	x	x	x	x
0x0A p. 143	Detect Status 2 (Read Only)	DETECT_TRUE_FALSE	DETECT_FALSE_TRUE	—			HSBIAS_HIZ	SHORT_RELEASE	SHORT_DETECTED
		x	x	x	x	x	x	x	x
0x0B p. 143	SRC Partial Lock Interrupt Status (Read Only)	—	DAC_UNLK	ADC_UNLK	—		DAC_LK	—	ADC_LK
		x	x	x	x	x	x	x	x
0x0C	Reserved	—							
		x	x	x	x	x	x	x	x
0x0D p. 144	VPMON Interrupt (Read Only)	—							VPMON_TRIP
		0	0	0	0	0	0	0	x
0x0E p. 144	PLL Lock (Read Only)	—							PLL_LOCK
		0	0	0	0	0	0	0	x
0x0F p. 144	Tip/Ring Sense Plug/Unplug Interrupt Status (Read Only)	—				TS_UNPLUG	TS_PLUG	RS_UNPLUG	RS_PLUG
		x	x	x	x	x	x	x	x
0x10–0x15	Reserved	—							
		x	x	x	x	x	x	x	x
0x16 p. 144	ADC Overflow Interrupt Mask	—							M_ADC_OVFL
		0	0	0	0	0	0	0	1
0x17 p. 145	Mixer Interrupt Mask	—				M_EQ_BIQUAD_OVFL	M_EQ_OVFL	M_MIX_CHA_OVFL	M_MIX_CHB_OVFL
		0	0	0	0	1	1	1	1
0x18 p. 145	SRC Interrupt Mask	—				M_SRC_OUNLK	M_SRC_IUNLK	M_SRC_OLK	M_SRC_ILK
		0	0	0	0	1	1	1	1
0x19 p. 145	ASP RX Interrupt Mask	—			M_ASPRX_OVLD	M_ASPRX_ERROR	M_ASPRX_LATE	M_ASPRX_EARLY	M_ASPRX_NOLRCK
		0	0	0	1	1	1	1	1
0x1A p. 146	ASP TX Interrupt Mask	—				M_ASPTX_SMERROR	M_ASPTX_LATE	M_ASPTX_EARLY	M_ASPTX_NOLRCK
		0	0	0	0	1	1	1	1
0x1B p. 146	Codec Interrupt Mask	—						M_HSDET_AUTO_DONE	M_PDN_DONE
		0	0	0	0	0	0	1	1
0x1C p. 146	SRC Partial Lock Interrupt Mask		M_DAC_UNLK	M_ADC_UNLK	—		M_DAC_LK	—	M_ADC_LK
		0	1	1	1	1	1	1	1
0x1D	Reserved	—							
		0	0	0	0	0	0	0	0
0x1E p. 147	VPMON Interrupt Mask	—							M_VPMON_TRIP
		0	0	0	0	0	0	0	1
0x1F p. 147	PLL Lock Mask	—							M_PLL_LOCK
		0	0	0	0	0	0	0	1
0x20 p. 147	Tip/Ring Sense Plug/Unplug Interrupt Mask	—				M_TS_UNPLUG	M_TS_PLUG	M_RS_UNPLUG	M_RS_PLUG
		0	0	0	0	1	1	1	1
0x21–0x7F	Reserved	—							
		0	0	0	0	0	0	0	0

6.8 Fractional-N PLL Registers

I²C Address: 10010(AD1)(AD0)[R/$\overline{W}$] through 10010(AD1)(AD0)0 = 0x94 (Write); 10010(AD1)(AD0)1 = 0x95 (Read)									
Page 0x15—Fractional-N PLL Registers									
Address	**Function**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x00	Control Port Page	PAGE							
		0	0	0	1	0	1	0	1
0x01	PLL Control 1	—							PLL_START
p. 147		0	0	0	0	0	0	0	0
0x02	PLL Division Fractional Byte 0	PLL_DIV_FRAC[7:0]							
p. 148		0	0	0	0	0	0	0	0
0x03	PLL Division Fractional Byte 1	PLL_DIV_FRAC[15:8]							
p. 148		0	0	0	0	0	0	0	0
0x04	PLL Division Fractional Byte 2	PLL_DIV_FRAC[23:16]							
p. 148		0	0	0	0	0	0	0	0
0x05	Division Integer	PLL_DIV_INT[7:0]							
p. 148		0	1	0	0	0	0	0	0
0x06–0x07	Reserved	—							
		x	x	x	x	x	x	x	x
0x08	PLL Control 3	PLL_DIVOUT							
p. 148		0	0	0	1	0	0	0	0
0x09	Reserved	—							
		x	x	x	x	x	x	x	x
0x0A	PLL Calibration Ratio	PLL_CAL_RATIO							
p. 148		1	0	0	0	0	0	0	0
0x0B–0x1A	Reserved	—							
		x	x	x	x	x	x	x	x
0x1B	PLL Control 4	—						PLL_MODE	
p. 148		0	0	0	0	0	0	1	1
0x1C–0x7F	Reserved	—							
		x	x	x	x	x	x	x	x

6.9 HP Load Detect Registers

I²C Address: 10010(AD1)(AD0)[R/$\overline{W}$] through 10010(AD1)(AD0)0 = 0x94 (Write); 10010(AD1)(AD0)1 = 0x95 (Read)									
Page 0x19—HP Load Detect Registers									
Address	**Function**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x00	Control Port Page	PAGE							
		0	0	0	1	1	0	0	1
0x01–0x24	Reserved	—							
		x	x	x	x	x	x	x	x
0x25	Load Detect R/C Status (Read Only)	—			CLA_STAT	—		RLA_STAT	
p. 149		0	0	0	0	0	0	0	0
0x26	HP Load Detect Done (Read Only)	—							HPLOAD_DET_DONE
p. 149		0	0	0	0	0	0	0	0
0x27	HP Load Detect Enable	—							HP_LD_EN
p. 149		0	0	0	0	0	0	0	0
0x28–0x7F	Reserved	—							
		x	x	x	x	x	x	x	x

6.10 Headset Interface Registers

I²C Address: 10010(AD1)(AD0)[R/$\overline{W}$] through 10010(AD1)(AD0)0 = 0x94 (Write); 10010(AD1)(AD0)1 = 0x95 (Read)									
Page 0x1B—Headset Interface Registers									
Address	**Function**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x00	Control Port Page	PAGE							
		0	0	0	1	1	0	1	1
0x01–0x6F	Reserved	—							
		x	x	x	x	x	x	x	x

I^{2}C Address: 10010(AD1)(AD0)[R/$\overline{\text{W}}$] through 10010(AD1)(AD0)0 = 0x94 (Write); 10010(AD1)(AD0)1 = 0x95 (Read)									
Page 0x1B—Headset Interface Registers									
Address	**Function**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x70	HSBIAS Sense and Clamp Autocontrol	HSBIAS_SENSE_EN	AUTO_HSBIAS_HIZ	TIP_SENSE_EN	—		HSBIAS_SENSE_TRIP		
p. 149		0	0	0	0	0	0	1	1
0x71	Wake Control	M_MIC_WAKE	M_HP_WAKE	WAKEB_MODE	—				WAKEB_CLEAR
p. 150		1	1	0	0	0	0	0	0
0x72	ADC Disable Mute	ADC_DISABLE_S0_MUTE	—						
p. 150		0	0	0	0	0	0	0	0
0x73	Tip Sense Control	TIP_SENSE_CTRL		TIP_SENSE_INV	—			TIP_SENSE_DEBOUNCE	
p. 150		0	0	0	0	0	0	1	0
0x74	Miscellaneous Detect Control	—			DETECT_MODE		HSBIAS_CTRL		PDN_MIC_LVL_DETECT
p. 151		0	0	0	0	0	0	1	1
0x75	Mic Detect Control 1	LATCH_TO_VP	EVENT_STATUS_SEL	HS_DETECT_LEVEL					
p. 151		0	0	0	1	1	1	1	1
0x76	Mic Detect Control 2	DEBOUNCE_TIME			—				
p. 152		0	0	1	0	1	1	1	1
0x77	Detect Status 1 (Read Only)	TIP_SENSE	HSBIAS_CLAMPHIZ	—					
p. 152		x	x	0	x	x	x	x	x
0x78	Detect Status 2 (Read Only)	—						HS_TRUE	SHORT_TRUE
p. 152		x	x	x	x	0	x	x	x
0x79	Detect Interrupt Mask 1	M_HSBIAS_SENSE	M_TIP_SENSE_PLUG	M_TIP_SENSE_UNPLUG	—				
p. 153		1	1	1	0	0	0	0	0
0x7A	Detect Interrupt Mask 2	M_DETECT_TRUE_FALSE	M_DETECT_FALSE_TRUE	—			M_HSBIAS_HIZ	M_SHORT_RELEASE	M_SHORT_DETECTED
p. 153		1	1	1	1	1	1	1	1
0x7B–0x7F	Reserved	—							
		x	x	x	x	x	x	x	x

6.11 Headset Bias Registers

I^{2}C Address: 10010(AD1)(AD0)[R/$\overline{\text{W}}$] through 10010(AD1)(AD0)0 = 0x94 (Write); 10010(AD1)(AD0)1 = 0x95 (Read)									
Page 0x1C—Headset Bias Registers									
Address	**Function**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x00	Control Port Page	PAGE							
		0	0	0	1	1	1	0	0
0x01–0x02	Reserved	—							
		x	x	x	x	x	x	x	x
0x03	Headset Bias Control	HSBIAS_CAPLESS_EN	—		HSBIAS_PD	—		HSBIAS_RAMP	
p. 153		1	1	0	0	0	0	1	0
0x04–0x7F	Reserved	—							
		x	x	x	x	x	x	x	x

6.12 ADC Registers

I^{2}C Address: 10010(AD1)(AD0)[R/$\overline{\text{W}}$] through 10010(AD1)(AD0)0 = 0x94 (Write); 10010(AD1)(AD0)1 = 0x95 (Read)									
Page 0x1D—ADC Registers									
Address	**Function**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x00	Control Port Page	PAGE							
		0	0	0	1	1	1	0	1
0x01	ADC Control 1	—		ADC_NOTCH_DIS	ADC_FORCE_WEAK_VCM	—	ADC_INV	—	ADC_DIG_BOOST
p. 154		0	0	0	0	0	0	0	0
0x02	ADC Soft-Ramp Enable	—					ADC_SOFTRAMP_EN	—	
p. 154		0	0	0	0	0	0	1	0

I²C Address: 10010(AD1)(AD0)[R/W] through 10010(AD1)(AD0)0 = 0x94 (Write); 10010(AD1)(AD0)1 = 0x95 (Read)									
Page 0x1D—ADC Registers									
Address	**Function**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x03	ADC Volume	ADC_VOL							
p. 154		0	0	0	0	0	0	0	0
0x04	ADC Wind-Noise Filter and HPF Control	—	ADC_WNF_CF			ADC_WNF_EN	ADC_HPF_CF		ADC_HPF_EN
p. 155		0	1	1	1	0	0	0	1
0x05–0x7F	Reserved	—							
		x	x	x	x	x	x	x	x

6.13 DAC Registers

I²C Address: 10010(AD1)(AD0)[R/W] through 10010(AD1)(AD0)0 = 0x94 (Write); 10010(AD1)(AD0)1 = 0x95 (Read)									
Page 0x1F—DAC Registers									
Address	**Function**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x00	Control Port Page	PAGE							
		0	0	0	1	1	1	1	1
0x01	DAC Control 1	—						DACB_INV	DACA_INV
p. 155		0	0	0	0	0	0	0	0
0x02–0x05	Reserved	—							
		x	x	x	x	x	x	x	x
0x06	DAC Control 2	HPOUT_PULLDOWN				HPOUT_LOAD	HPOUT_CLAMP	DAC_HPF_EN	—
p. 155		0	0	0	0	0	0	1	0
0x07–0x7F	Reserved	—							
		x	x	x	x	x	x	x	x

6.14 HP Control Registers

I²C Address: 10010(AD1)(AD0)[R/W] through 10010(AD1)(AD0)0 = 0x94 (Write); 10010(AD1)(AD0)1 = 0x95 (Read)									
Page 0x20—HP Control Registers									
Address	**Function**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x00	Control Port Page	PAGE							
		0	0	1	0	0	0	0	0
0x01	HP Control	—				ANA_MUTE_B	ANA_MUTE_A	FULL_SCALE_VOL	—
p. 156		0	0	0	0	1	1	0	1
0x02–0x7F	Reserved	—							
		0	0	0	0	0	0	0	0

6.15 Class H Registers

I²C Address: 10010(AD1)(AD0)[R/W] through 10010(AD1)(AD0)0 = 0x94 (Write); 10010(AD1)(AD0)1 = 0x95 (Read)									
Page 0x21—Class H Registers									
Address	**Function**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x00	Control Port Page	PAGE							
		0	0	1	0	0	0	0	1
0x01	Class H Control	—					ADPTPWR		
p. 156		0	0	0	0	0	1	1	1
0x02–0x7F	Reserved	—							
		x	x	x	x	x	x	x	x

6.16 Mixer Volume Registers

I²C Address: 10010(AD1)(AD0)[R/W] through 10010(AD1)(AD0)0 = 0x94 (Write); 10010(AD1)(AD0)1 = 0x95 (Read)									
Page 0x23—Mixer Volume Registers									
Address	**Function**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x00	Control Port Page	PAGE							
		0	0	1	0	0	0	1	1
0x01	Mixer Channel A Input Volume	—		MIXER_CHA_VOL					
p. 156		0	0	1	1	1	1	1	1
0x02	Mixer ADC Input Volume	—		MIXER_ADC_VOL					
p. 157		0	0	1	1	1	1	1	1
0x03	Mixer Channel B Input Volume	—		MIXER_CHB_VOL					
p. 157		0	0	1	1	1	1	1	1

I2C Address: 10010(AD1)(AD0)[R/W] through 10010(AD1)(AD0)0 = 0x94 (Write); 10010(AD1)(AD0)1 = 0x95 (Read)									
Page 0x23—Mixer Volume Registers									
Address	**Function**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x04–0x7F	Reserved	—							
		x	x	x	x	x	x	x	x

6.17 Equalizer Registers

I2C Address: 10010(AD1)(AD0)[R/W] through 10010(AD1)(AD0)0 = 0x94 (Write); 10010(AD1)(AD0)1 = 0x95 (Read)									
Page 0x24—Equalizer Registers									
Address	**Function**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x00	Control Port Page	PAGE							
		0	0	1	0	0	1	0	0
0x01 p. 157	Equalizer Filter Coefficient Input 0	EQ_COEF_IN[7:0]							
		0	0	0	0	0	0	0	0
0x02 p. 157	Equalizer Filter Coefficient Input 1	EQ_COEF_IN[15:8]							
		0	0	0	0	0	0	0	0
0x03 p. 157	Equalizer Filter Coefficient Input 2	EQ_COEF_IN[23:16]							
		0	0	0	0	0	0	0	0
0x04 p. 157	Equalizer Filter Coefficient Input 3	EQ_COEF_IN[31:24]							
		0	0	0	0	0	0	0	0
0x05	Reserved	—							
		x	x	x	x	x	x	x	x
0x06 p. 157	Equalizer Filter Coefficient Read/Write	—						EQ_WRITE	EQ_READ
		0	0	0	0	0	0	0	0
0x07 p. 157	Equalizer Filter Coefficient Output 0(Read Only)	EQ_COEF_OUT[7:0]							
		0	0	0	0	0	0	0	0
0x08 p. 158	Equalizer Filter Coefficient Output 1 (Read Only)	EQ_COEF_OUT[15:8]							
		0	0	0	0	0	0	0	0
0x09 p. 158	Equalizer Filter Coefficient Output 2 (Read Only)	EQ_COEF_OUT[23:16]							
		0	0	0	0	0	0	0	0
0x0A p. 158	Equalizer Filter Coefficient Output 3 (Read Only)	EQ_COEF_OUT[31:24]							
		0	0	0	0	0	0	0	0
0x0B p. 158	Equalizer Initialization Status (Read Only)	—							EQ_INIT_DONE
		0	0	0	0	0	0	0	0
0x0C p. 158	Equalizer Start Filter Control	—							EQ_START_FILTER
		0	0	0	0	0	0	0	0
0x0D	Reserved	—							
		x	x	x	x	x	x	x	x
0x0E p. 158	Equalizer Input Mute Control	—							EQ_MUTE
		0	0	0	0	0	0	0	0
0x0F–0x7F	Reserved	—							
		x	x	x	0	x	x	x	x

6.18 AudioPort Interface Registers

I2C Address: 10010(AD1)(AD0)[R/W] through 10010(AD1)(AD0)0 = 0x94 (Write); 10010(AD1)(AD0)1 = 0x95 (Read)									
Page 0x25—AudioPort Interface Registers									
Address	**Function**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x00	Control Port Page	PAGE							
		0	0	1	0	0	1	0	1
0x01 p. 159	Serial Port Receive Channel Select	—				SP_RX_CHB_SEL		SP_RX_CHA_SEL	
		0	0	0	0	0	1	0	0
0x02 p. 159	Serial Port Receive Isochronous Control	—	SP_RX_RSYNC	SP_RX_NSB_POS			SP_RX_NFS_NSBB	SP_RX_ISOC_MODE	
		0	0	0	0	0	1	0	0
0x03 p. 159	Serial Port Receive Sample Rate	—			SP_RX_FS				
		1	0	0	0	1	1	0	0
0x04 p. 160	S/PDIF Channel Select					SPDIF_CHB_SEL		SPDIF_CHA_SEL	
		0	0	0	0	1	1	1	0

I²C Address: 10010(AD1)(AD0)[R/$\overline{\text{W}}$] through 10010(AD1)(AD0)0 = 0x94 (Write); 10010(AD1)(AD0)1 = 0x95 (Read)									
Page 0x25—AudioPort Interface Registers									
Address	**Function**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x05	Serial Port Transmit Isochronous Control		SP_TX_RSYNC	SP_TX_NSB_POS			SP_TX_NFS_NSBB	SP_TX_ISOC_MODE	
p. 160		0	0	0	0	0	1	0	0
0x06	Serial Port Transmit Sample Rate	—			SP_TX_FS				
p. 160		1	1	0	0	1	1	0	0
0x07	S/PDIF/SoundWire Control 1	—		SPDIF_RES		SW_RES_INPUT		SW_RES_OUTPUT	
p. 161		0	0	1	1	1	1	1	1
0x08–0x7F	Reserved	—							
		x	x	x	x	x	x	x	x

6.19 SRC Registers

I²C Address: 10010(AD1)(AD0)[R/$\overline{\text{W}}$] through 10010(AD1)(AD0)0 = 0x94 (Write); 10010(AD1)(AD0)1 = 0x95 (Read)									
Page 0x26—SRC Registers									
Address	**Function**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x00	Control Port Page	PAGE							
		0	0	1	0	0	1	1	0
0x01	SRC Input Sample Rate	—			SRC_SDIN_FS				
p. 161		0	1	0	0	0	0	0	0
0x02–0x08	Reserved	—							
		x	x	x	x	x	x	x	x
0x09	SRC Output Sample Rate	—			SRC_SDOUT_FS				
p. 161		0	1	0	0	0	0	0	0
0x0A–0x7F	Reserved	—							
		x	x	x	x	x	x	x	x

6.20 DMA Registers

I²C Address: 10010(AD1)(AD0)[R/$\overline{\text{W}}$] through 10010(AD1)(AD0)0 = 0x94 (Write); 10010(AD1)(AD0)1 = 0x95 (Read)									
Page 0x27—DMA Registers									
Address	**Function**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x00	Control Port Page	PAGE							
		0	0	1	0	0	1	1	1
0x01	Soft Reset Reboot	—						SFT_RST_REBOOT	—
p. 161		0	0	0	1	1	1	0	0
0x02–0x7F	Reserved	—							
		x	x	x	x	x	x	x	x

6.21 S/PDIF Registers

I²C Address: 10010(AD1)(AD0)[R/$\overline{\text{W}}$] through 10010(AD1)(AD0)0 = 0x94 (Write); 10010(AD1)(AD0)1 = 0x95 (Read)									
Page 0x28—S/PDIF Registers									
Address	**Function**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x00	Control Port Page	PAGE							
		0	0	1	0	1	0	0	0
0x01	S/PDIF Control 1	—					SPDIF_TX_RAW	SPDIF_TX_KAE	SPDIF_TX_PDN
p. 162		0	0	0	0	0	0	0	1
0x02	S/PDIF Control 2	SPDIF_TX_L	SPDIF_TX_PRO	SPDIF_TX_AUDIOB	SPDIF_TX_CP	SPDIF_TX_PRE	SPDIF_TX_VCFG	SPDIF_TX_V	SPDIF_TX_DIGEN
p. 162		0	0	0	0	0	0	0	0
0x03	S/PDIF Control 3	—	SPDIF_TX_CC						
p. 163		0	0	0	0	0	0	0	0
0x04	S/PDIF Control 4	—					SPDIF_TX_STAT		
p. 163		0	1	0	0	0	0	1	0
0x05–0x7F	Reserved	—							
		x	x	x	x	x	x	x	x

6.22 Serial Port Transmit Registers

I²C Address: 10010(AD1)(AD0)[R/$\overline{W}$] through 10010(AD1)(AD0)0 = 0x94 (Write); 10010(AD1)(AD0)1 = 0x95 (Read)									
Page 0x29—Serial Port Transmit Registers									
Address	**Function**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x00	Control Port Page	PAGE							
		0	0	1	0	1	0	0	1
0x01	ASP Transmit Size and Enable	—						ASP_TX_2FS	ASP_TX_EN
p. 164		0	0	0	0	0	0	0	0
0x02	ASP Transmit Channel Enable	—						ASP_TX_CH2_EN	ASP_TX_CH1_EN
p. 164		0	0	0	0	0	0	0	0
0x03	ASP Transmit Channel Phase and Resolution	ASP_TX_CH1_AP	ASP_TX_CH2_AP	—		ASP_TX_CH2_RES		ASP_TX_CH1_RES	
p. 164		0	0	0	0	1	1	1	1
0x04	ASP Channel 1 Transmit Bit Start MSB	—							ASP_TX_CH1_BIT_ST_MSB
p. 164		0	0	0	0	0	0	0	0
0x05	ASP Channel 1 Transmit Bit Start LSB	ASP_TX_CH1_BIT_ST_LSB							
p. 164		0	0	0	0	0	0	0	0
0x06	ASP Transmit Hi-Z and Delay Configuration	—		ASP_TX_DRV_Z		ASP_TX_HIZ_DLY		—	
p. 165		0	0	0	0	0	0	0	0
0x07–0x09	Reserved	—							
		x	x	x	x	x	x	x	x
0x0A	ASP Channel 2 Transmit Bit Start MSB	—							ASP_TX_CH2_BIT_ST_MSB
p. 165		0	0	0	0	0	0	0	0
0x0B	ASP Channel 2 Transmit Bit Start LSB	ASP_TX_CH2_BIT_ST_LSB							
p. 165		0	0	0	0	0	0	0	0
0x0C–0x7F	Reserved	—							
		0	0	0	0	0	0	0	0

6.23 Serial Port Receive Registers

I²C Address: 10010(AD1)(AD0)[R/$\overline{W}$] through 10010(AD1)(AD0)0 = 0x94 (Write); 10010(AD1)(AD0)1 = 0x95 (Read)									
Page 0x2A—Serial Port Receive Registers									
Address	**Function**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x00	Control Port Page	PAGE							
		0	0	1	0	1	0	1	0
0x01	ASP Receive DAI0 Enable	ASP_RX1_CH_EN		ASP_RX0_CH_EN				ASP_RX1_2FS	ASP_RX0_2FS
p. 165		0	0	0	0	0	0	0	0
0x02	ASP Receive DAI0 Channel 1 Phase and Resolution	—	ASP_RX0_CH1_AP	—				ASP_RX0_CH1_RES	
p. 166		0	0	0	0	0	0	1	1
0x03	ASP Receive DAI0 Channel 1 Bit Start MSB	—							ASP_RX0_CH1_BIT_ST_MSB
p. 166		0	0	0	0	0	0	0	0
0x04	ASP Receive DAI0 Channel 1 Bit Start LSB	ASP_RX0_CH1_BIT_ST_LSB							
p. 166		0	0	0	0	0	0	0	0
0x05	ASP Receive DAI0 Channel 2 Phase and Resolution	—	ASP_RX0_CH2_AP	—				ASP_RX0_CH2_RES	
p. 166		0	0	0	0	0	0	1	1
0x06	ASP Receive DAI0 Channel 2 Bit Start MSB	—							ASP_RX0_CH2_BIT_ST_MSB
p. 166		0	0	0	0	0	0	0	0
0x07	ASP Receive DAI0 Channel 2 Bit Start LSB	ASP_RX0_CH2_BIT_ST_LSB							
p. 167		0	0	0	0	0	0	0	0
0x08	ASP Receive DAI0 Channel 3 Phase and Resolution	—	ASP_RX0_CH3_AP	—				ASP_RX0_CH3_RES	
p. 167		0	0	0	0	0	0	1	1

I²C Address: 10010(AD1)(AD0)[R/W] through 10010(AD1)(AD0)0 = 0x94 (Write); 10010(AD1)(AD0)1 = 0x95 (Read)									
Page 0x2A—Serial Port Receive Registers									
Address	**Function**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x09	ASP Receive DAI0 Channel 3 Bit Start MSB	—							ASP_RX0_CH3_BIT_ST_MSB
p. 167		0	0	0	0	0	0	0	0
0x0A	ASP Receive DAI0 Channel 3 Bit Start LSB	ASP_RX0_CH3_BIT_ST_LSB							
p. 167		0	0	0	0	0	0	0	0
0x0B	ASP Receive DAI0 Channel 4 Phase and Resolution	—	ASP_RX0_CH4_AP	—				ASP_RX0_CH4_RES	
p. 167		0	0	0	0	0	0	1	1
0x0C	ASP Receive DAI0 Channel 4 Bit Start MSB	—							ASP_RX0_CH4_BIT_ST_MSB
p. 168		0	0	0	0	0	0	0	0
0x0D	ASP Receive DAI0 Channel 4 Bit Start LSB	ASP_RX0_CH4_BIT_ST_LSB							
p. 168		0	0	0	0	0	0	0	0
0x0E	ASP Receive DAI1 Channel 1 Phase and Resolution	—	ASP_RX1_CH1_AP	—				ASP_RX1_CH1_RES	
p. 168		0	0	0	0	0	0	1	1
0x0F	ASP Receive DAI1 Channel 1 Bit Start MSB	—							ASP_RX1_CH1_BIT_ST_MSB
p. 168		0	0	0	0	0	0	0	0
0x10	ASP Receive DAI1 Channel 1 Bit Start LSB	ASP_RX1_CH1_BIT_ST_LSB							
p. 168		0	0	0	0	0	0	0	0
0x11	ASP Receive DAI1 Channel 2 Phase and Resolution	—	ASP_RX1_CH2_AP	—				ASP_RX1_CH2_RES	
p. 169		0	0	0	0	0	0	1	1
0x12	ASP Receive DAI1 Channel 2 Bit Start MSB	—							ASP_RX1_CH2_BIT_ST_MSB
p. 169		0	0	0	0	0	0	0	0
0x13	ASP Receive DAI1 Channel 2 Bit Start LSB	ASP_RX1_CH2_BIT_ST_LSB							
p. 169		0	0	0	0	0	0	0	0
0x14–0x7F	Reserved	—							
		x	x	x	x	x	x	x	x

6.24 ID Registers

I²C Address: 10010(AD1)(AD0)[R/W] through 10010(AD1)(AD0)0 = 0x94(Write); 10010(AD1)(AD0)1 = 0x95 (Read)									
Page 0x30—ID Registers									
Address	**Function**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x00	Control Port Page	PAGE							
		0	0	1	1	0	0	0	0
0x01–0x13	Reserved	—							
		x	x	x	x	x	x	x	x
0x14	Subrevision	SUBREVISION							
p. 169		x	x	x	x	x	x	x	x
0x15–0x7F	Reserved	—							
		x	x	x	x	x	x	x	x

7 Register Descriptions

The tables in this section give bit assignments, definitions, and default states after power-up or reset. Reserved register fields must maintain default states. Section 6 describes the red, turquoise, and orange indicators.

7.1 SoundWire Control Port 0 Registers

7.1.1 SCP Interrupt Status 1

Address Base + 0x40

	7	6	5	4	3	2	1	0
	—	PORT3_CASCADE	PORT2_CASCADE	PORT1_CASCADE	—	GEN_INT_CASCADE	STAT_BUS_CLASH	STAT_PARITY
	R/O						R/W1C	R/W1C
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7	—	Reserved
6:4	PORTx_CASCADE	Port x cascade. Indicates whether at least one unmasked interrupt condition is set in the corresponding DP*n* interrupt status register. The interrupt must be cleared at its source in the DP*n* interrupt status register. 0 (Default) No unmasked interrupt conditions in the DP*n* interrupt status register 1 At least one unmasked interrupt condition in DP*n* interrupt status register
3	—	Reserved
2	GEN_INT_CASCADE	General interrupt cascade. Indicates whether at least one unmasked interrupt condition is set in the general interrupt status registers 1 and 2. The interrupt must be cleared at its source in the general interrupt status registers.
1	STAT_BUS_CLASH	Bus clash status. Indicates whether an interrupt is pending due to detection of a bus clash on the SoundWire bus. If the corresponding mask bit is set, this event can generate an interrupt. Writing a 1 to the bit clears it and its associated interrupt. A sync loss reset does not clear the bit. 0 (Default) No bus collision detected. 1 Bus collision detected
0	STAT_PARITY	Parity status. Indicates whether a parity error is detected on the SoundWire bus. If the corresponding mask bit is set, the event can generate an interrupt. Writing a 1 to the bit clears it and its associated interrupt. A sync loss reset does not clear the bit. 0 (Default) No parity error detected. 1 Parity error detected

7.1.2 SCP Interrupt Mask 1

Address Base + 0x41

	7	6	5	4	3	2	1	0
	—						MASK_BUS_CLASH	MASK_PARITY
	—						R/W	R/W
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:2	—	Reserved
1	MASK_BUS_CLASH	Bus clash mask. Determines whether a bus collision event generates an interrupt 0 (Default) A bus collision does not generate an interrupt. 1 A bus collision generates an interrupt.
0	MASK_PARITY	Bus parity error mask. Determines whether a parity error event generates an interrupt 0 (Default) A parity error does not generate an interrupt. 1 A parity error generates an interrupt.

7.1.3 SCP Control

Address Base + 0x44

	7	6	5	4	3	2	1	0
	FORCE_RESET	CURRENT_BANK	—				CLOCK_STOP_NOW	CLOCK_STOP_NOT_FINISHED
	W/O	R/O	R/O				W/O	R/O
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7	FORCE_RESET	Force reset (write only). Used to trigger an internal reset. See Section 4.17 for details. 0 (Default) No action 1 Force internal reset.
6	CURRENT_BANK	Current bank. Identifies the current register bank. 0 (Default) current register bank is Bank 0 1 Current register bank is Bank 1
5:2	—	Reserved

Bits	Name	Description
1	CLOCK_ STOP_ NOW	Clock stop now (write only). Informs the slave whether the master is shutting down the SoundWire clock at the end of the next frame. 0 (Default) Normal operation 1 Clock stops after one more frame. The master is shutting down the SoundWire clock at the end of the next SoundWire frame. The master sends one more frame, which contains a Ping command where the master owns all payload data bit slots. The clock is stopped after the falling edge of the clock for that frame. The asynchronous wake event is allowed to propagate to the data pin only while the clock is stopped. To enter clock stop, the SoundWire master must first set CLOCK_STOP_PREPARE and wait for CLOCK_STOP_NOT_FINISHED to be cleared before setting this bit.
0	CLOCK_ STOP_ NOT_ FINISHED	Clock stop not finished. Indicates whether the chip completed any necessary shutdown sequence and is ready for the SoundWire master to set CLOCK_STOP_NOW and shut down the SoundWire clock. The encoding allows a SoundWire group read to identify when all SoundWire slaves are ready to enter Clock Stop State. 0 Ready for clock stop. 1 (Default) Not finished with state transition requested by the current value of CLOCK_STOP_PREPARE.

7.1.4 SCP System Control

Address Base + 0x45

	7	6	5	4	3	2	1	0
	—				WAKE_UP_ENABLE	CLOCK_STOP_MODE	—	CLOCK_STOP_PREPARE
	—				R/W	R/W	—	R/W
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:4	—	Reserved
3	WAKE_ UP_ ENABLE	Clock Stop Mode wake-up enable. Used to enable asynchronous wake from Clock Stop Mode when an S0 button press, headphone plug, or headphone unplug occurs. 0 (Default) Asynchronous wake disabled. 1 Asynchronous wake enabled.
2	CLOCK_ STOP_ MODE	Clock Stop Mode. Allow the SoundWire slave to lose context coming out of Clock Stop Mode. 0 (Default) Slave must not lose context in Clock Stop Mode 1 Slave loses context and triggers a SoundWire hard reset on exit from Clock Stop Mode
1	—	Reserved
0	CLOCK_ STOP_ PREPARE	Clock stop prepare. Indicates whether the SoundWire master intends to stop the SoundWire clock. See Section 4.8.13. 0 (Default) Clock stop not requested. 1 The CS42L42 is notified to prepare for clock stop.

7.1.5 SCP Device Number

Address Base + 0x46

	7	6	5	4	3	2	1	0
	—		GROUP_ID		DEVICE_NUMBER			
	—		R/W					
Default	0	0	0	0	0	0	0	0

Note: This register can be written only if SoundWire slave has enumeration on. See note in Section 7.1.8.

Bits	Name	Description
7:6	—	Reserved
5:4	GROUP_ ID	Group ID. Indicates whether this SoundWire slave device is addressed by a shared group alias in addition to commands targeted to its own device number. 00 (Default) Normal, not in a shared group. 01 Group 12: The device reacts to any command directed to the DevAddr = 12 alias. 10 Group 13: The device reacts to any command directed to the DevAddr = 13 alias. 11 Reserved
3:0	DEVICE_ NUMBER	Device number. This value is compared with the DevAddr field in the control word to determine whether the command is directed to this device. Attempts to write to this bit are ignored if the SoundWire slave is not in the Enumeration ON State. See note in Section 7.1.8. 0000–1011 Valid device numbers (0–11 decimal). 1100–1111 Reserved

7.1.6 SCP Device ID 0

Address Base + 0x50

	7	6	5	4	3	2	1	0
	SOUNDWIRE_VERSION (DeviceID[47:44])				INSTANCE (DeviceID[43:40]			
	R/O							
Default	0	0	0	0	0	0	x	x

Note: A read of this register puts the SoundWire Slave in the Enumeration ON State. If enumeration is ON, reads of the SCP device ID registers return the Device ID values and writes to the SCP device number register are allowed. If enumeration is OFF, reads of the device ID registers return a zero and writes to the SCP device number register do not complete. If a bus clash is detected while the device ID read data is placed on the SoundWire bus, the SoundWire slave drops out of enumeration (enumeration turns OFF) and remaining bits of the read operation return zero.

Bits	Name	Description
7:4	SOUNDWIRE_ VERSION	SoundWire version. Indicates the version of the MIPI SoundWire Specification supported by the device. A value is returned only if enumeration is ON. A zero is returned if enumeration is OFF. If enumeration goes OFF due to a SoundWire bus clash in the middle of a read, a partial value may be returned. 0000 Pre–*MIPI SoundWire Specification, v 1.0* 0001 Compliant to *MIPI SoundWire Specification, v 1.0.*
3:0	INSTANCE	Instance. Used to indicate the instance of the device if there are multiple copies of the same device on the SoundWire bus. A value is returned only if enumeration is ON; a zero is returned if it is OFF. If enumeration goes OFF due to a SoundWire bus clash in the middle of a read, a partial value may be returned. INSTANCE[3:2] default = 00 INSTANCE[1:0] indicate the AD1/AD0 pin values latched on reset, which are idle when SoundWire is selected.

7.1.7 SCP Device ID 1

Address Base + 0x51

	7	6	5	4	3	2	1	0
	MIPI_MANUFACTURER_ID[15:8] (DeviceID[39:32])							
	R/O							
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7:0	MIPI_MANUFACTURER_ ID[15:8]	MIPI manufacturer’s device ID upper byte. (Cirrus Logic is 0x01FA). The value is returned only if enumeration is ON. A zero is returned if enumeration is OFF. If enumeration goes OFF due to a SoundWire bus clash in the middle of a read, a partial value may be returned.

7.1.8 SCP Device ID 2

Address Base + 0x52

	7	6	5	4	3	2	1	0
	MIPI_MANUFACTURER_ID[7:0] (DeviceID[31:24])							
	R/O							
Default	1	1	1	1	1	0	1	0

Bits	Name	Description
7:0	MIPI_ MANUFACTURER_ ID[7:0] (DeviceID[31:24])	This is a read only field reporting the lower byte of the unique MIPI Manufacturer’s device ID value. The MIPI Manufacturer ID for Cirrus Logic is 0x01FA. A value is returned only when enumeration is ON. A zero is returned if enumeration is OFF. If enumeration goes OFF due to a SoundWire bus clash in the middle of a read, a partial value may be returned.

7.1.9 SCP Device ID 3

Address Base + 0x53

	7	6	5	4	3	2	1	0
	PART_ID [15:8] (DEVICEID[23:16])							
	R/O							
Default	0	1	0	0	0	0	1	0

Bits	Name	Description
7:0	PART_ID[15:8] (DEVICEID[23:16])	Part ID upper byte. Unique ID for each device. The value can be read only while the SoundWire Slave is in Enumeration ON State. A zero is returned if enumeration is OFF. If enumeration goes OFF due to a SoundWire bus clash in the middle of a read, a partial value may be returned. Part ID = 4242

7.1.10 SCP Device ID 4

Address Base + 0x54

	7	6	5	4	3	2	1	0
	PART_ID [7:0] (DeviceID[15:8])							
	R/O							
Default	1	0	0	0	0	0	1	1

Bits	Name	Description
7:0	PART_ID[7:0] (DeviceID[15:8])	Part ID lower byte. Unique ID for each device. The value can be read only while the SoundWire Slave is in the Enumeration ON state. A zero value is returned if enumeration is OFF. If enumeration goes OFF due to a SoundWire bus clash in the middle of a read, a partial value may be returned. Part ID = 4242

7.1.11 SCP Device ID 5

Address Base + 0x55

	7	6	5	4	3	2	1	0
	CLASS[7:0] (DeviceID[7:0])							
	R/O							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	CLASS[7:0]	Class. Reserved to indicate the device class. A value is returned only if enumeration is ON. A zero is returned if enumeration is OFF. If enumeration goes OFF due to a SoundWire bus clash in the middle of a read, a partial value may be returned.

7.1.12 SCP Frame Control

Address Base + 0x60
Address Base + 0x70 (Banked)

	7	6	5	4	3	2	1	0
	ROW_CONTROL					COLUMN_CONTROL		
	W/O							
Default	0	0	0	0	0	0	0	0

Note: A write to this register in the inactive bank triggers bank switch at the end of the current frame. A write to the Bank 0 register can trigger a bank switch to Bank 0. A write to the Bank 1 register can trigger a bank switch to Bank 1.

Bits	Name	Description
7:3	ROW_ CONTROL	Rows per frame. Selects the number of rows in the frame. This field automatically updates with frame size detected at completion of the frame synchronization search. Writes to this register change the frame shape at the end of the next frame. Writes to the inactive banked version of this register trigger a bank switch at the end of the next frame, regardless of whether the register contents have changed.
2:0	COLUMN_ CONTROL	Columns per frame. Automatically updates with frame size detected at completion of the frame synchronization search. Writes to this register change the frame shape at the end of the next frame. Writes to the inactive banked version of this register trigger a bank switch at the end of the next frame regardless of whether the register contents have changed. 000 (Default) 2 Columns 001 4 Columns … 111 16 Columns

ROW_CONTROL	Number of Rows	ROW_CONTROL	Number of Rows	ROW_CONTROL	Number of Rows
0x00	48	0x08	96	0x10	192
0x01	50	0x09	100	0x11	200
0x02	60	0x0A	120	0x12	240
0x03	64	0x0B	128	0x13	256
0x04	75	0x0C	150	0x14	72
0x05	80	0x0D	160	0x15	144
0x06	125	0x0E	250	0x16	90
0x07	147	0x0F	Reserved	0x17	180

7.1.13 General Interrupt Status 1

Address Base + 0xC0

	7	6	5	4	3	2	1	0
	GEN_INT_STAT2_CASCADE	—						SCP_IMP_DEF1
	R/O	—						R/W1C
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7	GEN_INT_ STAT2_ CASCADE	General interrupt status cascade. Reports any unmasked interrupt conditions in the general interrupt status 2 register. 0 (Default) No unmasked interrupted condition detected. 1 Unmasked interrupt condition asserted

Bits	Name	Description
6:1	—	Reserved
0	SCP_IMP_DEF1	SCP implementation defined 1. The combined interrupt from the interrupt controller is connected to this bit. 0 (Default) Interrupt not asserted. 1 Interrupt condition asserted

7.1.14 General Interrupt Mask 1

Address Base + 0xC1

	7	6	5	4	3	2	1	0
	—							M_SCP_IMP_DEF1
	—							R/W
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:1	—	Reserved
0	M_SCP_IMP_DEF1	Status bit interrupt enable 1. Enables corresponding status bit to generate an interrupt. This bit is cleared automatically on any internal reset or loss-of-frame synchronization. 0 (Default) Corresponding status bit cannot generate an interrupt. 1 Corresponding status bit may generate an interrupt.

7.1.15 General Interrupt Status 2

Address Base + 0xC2

	7	6	5	4	3	2	1	0
	—					INT_STAT_LATE_RESP	INT_STAT_TIMEOUT_ERR	—
	—					R/W1C	R/W1C	—
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:3	—	Reserved
2	INT_STAT_LATE_RESP	Late response. Reports whether any SoundWire read command did not complete in time for the response to be included in the read data response of the same command. See Section 4.8.12.1 for details. 0 (Default) Interrupt not asserted 1 Interrupt condition detected. Set on an APB read that requires indirect-access procedures. The associated interrupt can be used as a warning if direct access was expected, but indirect access was required. If set, the bit is cleared by writing a 1 to the bit. It is not cleared by the sync loss reset.
1	INT_STAT_TIMEOUT_ERR	Timeout error. Reports whether a timeout error occurs on the APB read or write access. Timeout error generation is controlled through the memory access timeout register. 0 (Default) Interrupt not asserted 1 Interrupt condition detected. If set, the bit is cleared by writing a 1 to the bit. It is not cleared by the sync loss reset.
0	—	Reserved

7.1.16 General Interrupt Mask 2

Address Base + 0xC3

	7	6	5	4	3	2	1	0
	—					M_LATE_RESP	M_TIMEOUT_ERR	—
	—					R/W	R/W	—
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:3	—	Reserved
2	M_LATE_RESP	Late response mask. Enables a late read data event to generate an generate an interrupt. This bit is automatically cleared on any internal reset or loss-of-frame synchronization. 0 (Default) Late read data does not generate an interrupt. 1 Late read data generates an interrupt.
1	M_TIMEOUT_ERR	Timeout error mask. Enables an APB timeout error event to generate an interrupt 0 (Default) Timeout error does not generate an interrupt. 1 Timeout error generates an interrupt.
0	—	Reserved

7.1.17 Memory Access Status

Address Base + 0xD0

	7	6	5	4	3	2	1	0
	—				LAST_LATE	CMD_IN_PROGRESS	CMD_DONE	RDATA_RDY
	—				R/O			
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:4	—	Reserved
3	LAST_LATE	Last command late. Indicates whether the previous read command completed in time for the response to be included in a single command for direct access. If not, indirect access procedures are required for registers. This bit is cleared at the start of a new transaction through the APB interface. 0 (Default) Previous APB read access was direct. 1 Previous APB read access did not complete in time, and indirect access procedures are required. **Note:** This bit is also used to set INT_STAT_LATE_RESP.
2	CMD_IN_PROGRESS	Command in progress. Indicates whether a read/write operation is in progress across the internal bus bridge, including register access initiated through the control word. **Note:** Applies only to read access through the internal bus bridge (address 0x1000 and above). Does not apply to internal SoundWire registers (0x0000–0x0FFF). 0 (Default) No transfer is in progress across the bridge. 1 A read or write access is in progress across the bridge.
1	CMD_DONE	Transfer done. Indicates whether the previous read/write access initiated by a control word command through the internal memory bridge completed. It is cleared at the beginning of the next access attempt to the bridge (address above 0x1000). CMD_DONE is cleared by any control word–initiated read/write to any address accessed through the internal memory bridge. CMD_DONE is cleared on a read command that returns previously fetched data. 0 (Default) Previous access through the bridge not completed or no access requested yet. 1 Previous access through the bridge completed.
0	RDATA_RDY	Read data ready. Indicates whether the previous control word–initiated read access is complete and the read data would be returned on the next control word initiated read of the same address, which is preserved in MEM_READ_LAST_ADDR. **Note:** Applies only to read access through the internal bus bridge (address 0x1000 and above) and not to internal SoundWire registers (0x0000–0x0FFF). This bit is cleared by any control word–initiated read access to any address accessed through the internal memory bridge. 0 (Default) Bridge does not contain previous read data or new read data fetch is in progress. 1 Bridge contains read data that can be read from the memory read data register (see Section 7.1.21)

7.1.18 Memory Access Control

Address Base + 0xD1

	7	6	5	4	3	2	1	0
	—						LATE_RESP	
	—						R/W	
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7:2	—	Reserved
1:0	LATE_RESP	Late response. Selects the command response supplied in the control word NAK/ACK bits for read instructions when read data is not available in time to be returned in the same command. 00 Respond with COMMAND_IGNORED 01 (Default) Respond with COMMAND_OK, which allows for indirect access. If indirect access procedures are required to access the read data at a later time in the MEM_READ_DATA, this selection allows the COMMAND_OK to acknowledge that the internal access was accepted and initiated. 10 Respond with COMMAND_FAIL 11 Reserved If operating conditions require direct access to always be allowed, the response can be programmed as either COMMAND_IGNORED or COMMAND_FAIL to provide an immediate indication of the delay. **Note:** A COMMAND_FAIL response can also be returned on APB access if the previous access did not complete.

7.1.19 Memory Access Timeout

Address Base + 0xD2

	7	6	5	4	3	2	1	0
	—				TIMEOUT_DISABLE	TIMEOUT_CTRL		
	—				R/W			
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:4	—	Reserved
3	TIMEOUT_DISABLE	Timeout disable. Disables timeout control. See Section 4.8.12 for details and examples. 0 (Default) Timeout enabled on internal memory access through the APB memory bridge. 1 Timeout disabled on internal memory access through the APB memory bridge.
2:0	TIMEOUT_CTRL	Timeout control. Selects the number of internal bus cycles after which a memory access through the APB memory bridge generates a timeout error and aborts the memory access. 000 (Default) 8 bus cycles 001 16 bus cycles 010 32 bus cycles 011 64 bus cycles 100 128 bus cycles 101 256 bus cycles 110 512 bus cycles 111 65,535 bus cycles

7.1.20 Memory Read Last Address 0 and 1

Address Base + 0xD4
Address Base + 0xD5

	7	6	5	4	3	2	1	0
	MEM_READ_LAST_ADDR[7:0]							
	MEM_READ_LAST_ADDR[15:8]							
	R/O							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	MEM_READ_LAST_ADDR	Memory read last address. Address of the last completed read access via a control word command. Valid only if RDATA_RDY is set. See Section 4.8.12 for details. Applies only to the last access through the memory access bridge to the internal APB (which requires indirect access via a SoundWire command). Not applicable to internal SoundWire registers (addresses 0x0000–0x0FFF), which are accessed directly via a SoundWire command.

7.1.21 Memory Read Data

Address Base + 0xD8

	7	6	5	4	3	2	1	0
	MEM_READ_DATA[7:0]							
	R/O							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	MEM_READ_DATA	Memory read data. Contains the data previously read from the address stored in MEM_READ_LAST_ADDR. Data is valid if the RDATA_RDY status bit of in the memory access status register is set. See Section 4.8.12 for details.

7.2 SoundWire Data Port (1–3) Descriptions

The registers in this section are replicated for each enabled data port enabled via the SW_NUM_PORTS RTL parameter. The “n” in “DP*n*” represents the appropriate port number (1–3; see Table 4-10 for port mappings).

7.2.1 DP*n* Interrupt Status

Address Base + 0x00

	7	6	5	4	3	2	1	0
	—						STAT_P‘ORT_READY	STAT_TEST_FAIL
	—						R/W1C	
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:2	—	Reserved
1	STAT_PORT_READY	Port ready status. Indicates whether the port is ready for data transfer after a prepare request. This event generates an interrupt if the corresponding mask register bit is set. It is cleared only by writing 1 to it. It is not cleared by a sync loss reset. See Section 4.8.8 for programming details. 0 (Default) Port is not ready. 1 Port is ready.

Bits	Name	Description
0	STAT_TEST_FAIL	Status test/fail. Indicates whether an error was detected during PRBS, Static0, or Static1 test modes when a sink data port (Data Ports 2 and 3) does not receive the expected value from the SoundWire bus. This bit is never set in source data ports (Data Port 1). The bit is cleared only by writing 1 to it. It is not cleared by the sync loss reset. 0 (Default) No Test Mode error detected. 1 Test Mode error detected.

7.2.2 DP*n* Interrupt Mask

Address Base + 0x01

	7	6	5	4	3	2	1	0
	—						PORT_READY_M	TEST_FAIL_M
	—						R/W	
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:2	—	Reserved
1	PORT_READY_M	Port ready mask. Enables corresponding status bit to generate an interrupt. This bit is automatically cleared on any internal reset or loss-of-frame synchronization. 0 (Default) Corresponding status bit cannot generate an interrupt. 1 Corresponding status bit may generate an interrupt.
0	TEST_FAIL_M	Test/fail mask. Enables the corresponding status bit to generate an interrupt. This bit is automatically cleared on any internal reset or loss-of-frame synchronization. 0 (Default) Corresponding status bit cannot generate an interrupt. 1 Corresponding status bit may generate an interrupt.

7.2.3 DP*n* Port Control

Address Base + 0x02

	7	6	5	4	3	2	1	0
	—			INVERT_BANK	PORT_DATA_MODE		—	
	—			R/W				
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:5	—	Reserved
4	INVERT_BANK	Invert bank. Applies to DP*n*-prefixed registers for this port, but not to SCP-prefixed banked registers. This bit is cleared on a sync loss reset. The selected value is applied at the end of the SoundWire frame with the command writing to INVERT_BANK. **Note:** This function for this bit was defined before the publication of *MIPI SoundWire Specification, v. 1.0*, in which this bit is replaced with NEXT_INVERT_BANK. 0 (Default) Use bank as directed in the control word. 1 Use the opposite bank than what is directed in the control word. Setting is applied on the next frame boundary
3:2	PORT_DATA_MODE	Port data mode. Determines whether the port is in Normal Mode or Test Mode of data transfer. 00 (Default) Normal 01 Test Mode test data 10 Static 0 test data 11 Static 1 test data
1:0	—	Reserved

7.2.4 DP*n* Block Control 1

Address Base + 0x03

	7	6	5	4	3	2	1	0
	—		WORD_LENGTH					
	—		R/W					
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	—	Reserved
5:0	WORD_LENGTH	Word length. Specifies the payload length in bits. Configure this bit before enabling channels on the port. 00 0000 (Default) 1 bit 00 0001 2 bits …

7.2.5 DP*n* Prepare Status

Address Base + 0x04

	7	6	5	4	3	2	1	0
	—						NOT_FINISHED_CHANNEL2	NOT_FINISHED_CHANNEL1
	R/O							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:2	—	Reserved
1:0	NOT_ FINISHED_ CHANNEL*x*	Not finished channel. Indicates whether each channel completed its state transition after the corresponding PREPARE_ CHANNELx bit is written to prepare or deprepare the channel. 0 (Default) Channel not finished moving to the preparedness state indicated by the CHANNEL_PREPAREx bit. 1 After PREPARE_CHANNELx is set, if NOT_FINISHED_CHANNELx = 1, the channel has not finished the transition to readiness. A 0 indicates that the channel is ready. Fig. 4-27 shows how to interpret channel status. After PREPARE_CHANNELx is cleared, if NOT_FINISHED_CHANNELx = 1, the channel is not finished with the transition to deprepared state. A 0 indicates that the channel has finished any internal process to be deprepared.

7.2.6 DP*n* Prepare Control

Address Base + 0x05

	7	6	5	4	3	2	1	0
	—						PREPARE_CHANNEL2	PREPARE_CHANNEL1
	R/W							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:2	—	Reserved
1:0	PREPARE_ CHANNEL*x*	Prepare channel. Prepares each channel so it can begin immediately when enabled. Data Ports 2 and 3 are stereo and therefore support Channels 1 and 2. Data Port 1 supports only Channel 1. Fig. 4-27 shows how to interpret channel status. 0 (Default) Channel deactivated 1 Channel commanded to prepare for activity.

7.2.7 DP*n* Channel Enable

Address Base + 0x20
Address Base + 0x30 (Banked)

	7	6	5	4	3	2	1	0
	—						CHANNEL_EN2	CHANNEL_EN1
	R/W							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:2	—	Reserved
1:0	CHANNEL_ EN*x*	Channel enable 2 and 1. Automatically cleared on internal resets and loss-of-frame synchronization. Do not set these bits unless the channel has been prepared using the DP*n* prepare control register and confirmed by reading the DP*n* prepare status register. Data Ports 2 and 3 are stereo and therefore support Channels 1 and 2. Data Port 1 supports Channel 1 only. 0 (Default) Channel disabled 1 Channel enabled

7.2.8 DP*n* Sample Control 1

Address Base + 0x22
Address Base + 0x32 (Banked)

	7	6	5	4	3	2	1	0
	SAMPLE_INTERVAL_LOW							
	R/W							
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7:0	SAMPLE_ INTERVAL_LOW	Sample interval lower byte. The sample interval is calculated in units of bit slots according to the following formula: Sample Interval = 256*SAMPLE_INTERVAL_HIGH + SAMPLE_INTERVAL_LOW + 1

7.2.9 DP*n* Sample Control 2

Address Base + 0x23
Address Base + 0x33 (Banked)

	7	6	5	4	3	2	1	0
	SAMPLE_INTERVAL_HIGH							
	R/W							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	SAMPLE_ INTERVAL_HIGH	Sample interval upper byte. The interval is calculated in units of bit slots according to the following formula: Sample Interval = 256*SAMPLE_INTERVAL_HIGH + SAMPLE_INTERVAL_LOW + 1

7.2.10 DP*n* Offset Control 1

Address Base + 0x24
Address Base + 0x34 (Banked)

	7	6	5	4	3	2	1	0
	OFFSET1							
	R/W							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	OFFSET1	Block offset control 1. Determines the number of bit slots from the start of the sample interval to the start of the port's payload data block within the SoundWire frame. • In Block-per-Channel mode, the block offset is calculated as follows: Block Offset = OFFSET1 • In Block-per-Port Mode, the block offset is calculated as follows: Block Offset = OFFSET1 + (256 * OFFSET2)

7.2.11 DP*n* Offset Control 2

Address Base + 0x25
Address Base + 0x35 (Banked)

	7	6	5	4	3	2	1	0
	OFFSET2							
	R/W							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0‘	OFFSET2	Block offset control 2. Determines either the block offset (number of bit slots from the start of the sample interval to the start of the port's payload data block) or the subblock offset (number of bit slots between individual channels), which is the number of bit slots from the start of the sample interval to the start of the port's payload data block within the SoundWire frame. • In Block-per-Channel Mode, the subblock offset is calculated as follows: Subblock offset = OFFSET2 • In Block-per-Port Mode, the block offset is calculated as follows: Block Offset = OFFSET1 + (256 * OFFSET2)

7.2.12 DP*n* Horizontal Control

Address Base + 0x26
Address Base + 0x36 (Banked)

	7	6	5	4	3	2	1	0
	HSTART				HSTOP			
	R/W							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:4	HSTART	Horizontal control start. Defines the column number within a row that is the start of the port's transport subframe. The port's payload data is bounded by the columns defined by HSTART and HSTOP. The HSTART value must not exceed HSTOP. 0x0 (Default) Subframe begins in Column 0 0x1 Subframe begins in Column 1 … 0xF Subframe begins in Column 15
3:0	HSTOP	Horizontal control stop. Defines the column number within a row that is the end of the port's transport subframe. The port's payload data is bounded by the columns defined by HSTART and HSTOP. The HSTART value must not exceed HSTOP. 0x0 (Default) Subframe ends in Column 0 0x1 Subframe ends in Column 1 … 0xF Subframe ends in Column 15

7.2.13 DP*n* Block Control 3

Address Base + 0x27
Address Base + 0x37 (Banked)

	7	6	5	4	3	2	1	0
	—							BLOCK_PACKING_MODE
	—							R/W
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:1	—	Reserved
0	BLOCK_ PACKING_ MODE	Block packing mode. Determines how the port’s channel data is positioned within the SoundWire frame. 0 (Default) Block-per-Port Mode. Each channel’s payload is adjacent (no space between channels) within the port’s payload transport window. 1 Block-per-Channel Mode. Spacing is added between individual channels within the payload transport window.

7.3 Global Registers

7.3.1 Device ID A and B

Address 0x1001

R/O	7	6	5	4	3	2	1	0
	DEVIDA				DEVIDB			
Default	0	1	0	0	0	0	1	0

7.3.2 Device ID C and D

Address 0x1002

R/O	7	6	5	4	3	2	1	0
	DEVIDC				DEVIDD			
Default	1	0	1	0	0	1	0	0

7.3.3 Device ID E and F

Address 0x1003

R/O	7	6	5	4	3	2	1	0
	DEVIDE				—			
Default	0	0	1	0	x	x	x	x

Bits	Name	Description
7:4	DEVIDA DEVIDC DEVIDE	Device ID code. Identifies the CS42L42. DEVIDA 0x4 DEVIDB 0x2 DEVIDC 0xA Represents the *L* in CS42L42. DEVIDD 0x4 DEVIDE 0x2
3:0	DEVIDB DEVIDD	

7.3.4 Revision ID

Address 0x1005

R/O	7	6	5	4	3	2	1	0
	AREVID				MTLREVID			
Default	x	x	x	x	x	x	x	x

Bits	Name	Description
7:4	AREVID	Alpha revision. CS42L42 alpha revision level. AREVID and MTLREVID form the complete device revision ID (e.g.,: A0, B2). 0x00 … 0xFF
3:0	MTLREVID	Metal revision. CS42L42 metal revision level. AREVID and MTLREVID form the complete device revision ID (e.g.,: A0, B2). 0x00 … 0xFF

7.3.5 Freeze Control

Address 0x1006

R/W	7	6	5	4	3	2	1	0
	—							FREEZE
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:1	—	Reserved
0	FREEZE	Freeze registers. Configures a hold on all volume-control and power-down register settings except PDN_MIC_LVL_DETECT (p. 151). Use this bit only during normal operation after all circuit blocks in use have powered up. Using the bit when an affected circuit block is powering up could cause the change to occur immediately when power up completes (i.e., not gated by the FREEZE bit). Bits affected by FREEZE are shown in orange throughout Section 6 and Section 7. 0 (Default) Volume-control and power-down register changes take effect immediately. 1 Modifications made to volume-control and power-down registers take effect only after this bit is cleared.

7.3.6 Serial Port SRC Control

Address 0x1007

R/W	7	6	5	4	3	2	1	0
	—			EQ_BYPASS	I2C_DRIVE	ASP_DRIVE	SRC_BYPASS_DAC	SRC_BYPASS_ADC
Default	0	0	0	1	0	0	0	0

Bits	Name	Description
7:5	—	Reserved
4	EQ_BYPASS	Bypass equalizer. Configures whether the EQ block is bypassed. See Section 4.1 for details 0 No bypass 1 (Default) Bypass
3	I2C_DRIVE	I^2C output drive strength. Selects drive strength used for the SDA output 0 (Default) Normal 1 Decreased
2	ASP_DRIVE	ASP output drive strength. Selects drive strength used for the ASP port SDOUT output. See Table 3-25 for specifications. 0 (Default) Normal 1 Decreased
1	SRC_BYPASS_DAC	Bypass SRC (DAC path). Determines the bypass of the input SRCs. See Section 4.11 for details. 0 (Default) No bypass 1 Bypass. SRC_SDIN_FS (see p. 161) must be set equal to Fs_{INT}.
0	SRC_BYPASS_ADC	Bypass SRC (ADC path). Determines the bypass of the output SRCs. See Section 4.11 for details. 0 (Default) No bypass 1 Bypass. SRC_SDIN_FS must be set equal to Fs_{INT}.

7.3.7 MCLK Status

Address 0x1008

R/W	7	6	5	4	3	2	1	0
	—						INTERNAL_FS_STAT	—
Default	0	0	0	0	0	0	x	0

Bits	Name	Description
7:2	—	Reserved
1	INTERNAL_FS_STAT	Internal sample rate status. Indicates the divide ratio from $MCLK_{INT}$ (set in INTERNAL_FS, see Section 7.3.8) to produce the internal sample rate for all converters. 0 $Fs_{INT} = MCLK_{INT}/250$. Indicates that the internal MCLK is 12 or 24 MHz. 1 $Fs_{INT} = MCLK_{INT}/256$. Indicates that the internal MCLK is 11.2896, 12.288, 22.5792, or 24.576 MHz.
0	—	Reserved

7.3.8 MCLK Control

Address 0x1009

R/W	7	6	5	4	3	2	1	0
	—						INTERNAL_FS	—
Default	0	0	0	0	0	0	1	0

Bits	Name	Description
7:2	—	Reserved
1	INTERNAL_FS	Internal sample rate (Fs_{INT}). Selects the divide ratio from $MCLK_{INT}$ to produce the internal sample rate for all converters. See Table 4-6 for programming details. This bit always returns zero when read. Reports status in INTERNAL_FS_STAT. 0 Fs_{INT} = $MCLK_{INT}$/250. Set if internal MCLK is 12 or 24 MHz. 1 (Default) Fs_{INT} = $MCLK_{INT}$/256. Set if internal MCLK is 11.2896, 12.288, 22.5792, or 24.576 MHz. If $MCLK_{INT}$ 11.2896, 12, or 12.288 MHz, MCLKDIV must be 0. If it is 22.5792, 24, or 24.576 MHz, MCLKDIV must be 1.
0	—	Reserved

7.3.9 Soft Ramp Rate

Address 0x100A

R/W	7	6	5	4	3	2	1	0
	ASR_RATE				DSR_RATE			
Default	1	0	1	0	0	1	0	0

Bits	Name	Description
7:4	ASR_RATE	Analog soft-ramp rate (number of Fs periods between steps). Selects the soft ramp rate for all analog volumes. Step size = 1 dB or 2 dB for HPOUTx. See Section 4.4.4 for details. 0000 1 0010 4 0100 8 0110 12 1000 22 1010 (Default) 33 1100 44 1110 66 0001 2 0011 6 0101 11 0111 16 1001 24 1011 36 1101 48 1111 72
3:0	DSR_RATE	Digital soft-ramp rate (number of Fs periods between steps). Selects soft ramp rate for all digital volumes. Step size = 0.125 dB. 0000 1 0010 4 0100 (Default) 8 0110 12 1000 22 1010 33 1100 44 1110 66 0001 2 0011 6 0101 1 0111 16 1001 24 1011 36 1101 48 1111 72

7.3.10 Slow Start Enable

Address 0x100B

R/W	7	6	5	4	3	2	1	0
	—	SLOW_START_EN			—			
Default	0	1	1	1	0	0	0	0

Bits	Name	Description
7	—	Reserved
6:4	SLOW_START_EN	Slow startup enable. Selects between fast and slow start-up times. See Section 4.4.5 for details. 000 Disabled. Shortens start-up time of the mixer, DAC, and HP. Useful for high-definition audio applications. 111 (Default) Enabled
3:0	—	Reserved

7.3.11 I²C Debounce

Address 0x100E

R/W	7	6	5	4	3	2	1	0
	I2C_SDA_DBNC_CNT			I2C_SDA_DBNC_EN	I2C_SCL_DBNC_CNT			I2C_SCL_DBNC_EN
Default	1	0	0	0	1	0	0	0

Bits	Name	Description
7:5	I2C_SDA_DBNC_CNT	I²C debounce count. Number of MCLKs to debounce SDA input **Note:** The I2C_SDA_DBNC_CNT and I2C_SCL_DBNC_CNT settings must be identical. 000 0 MCLKs 010 2 MCLKs 100 (Default) 4 MCLKs 110 6 MCLKs 001 1 MCLK 011 3 MCLKs 101 5 MCLKs 111 7 MCLKs
4	I2C_SDA_DBNC_EN	I²C SDA debounce enable. SDA debounce enable **Note:** The I2C_SDA_DBNC_EN and I2C_SCL_DBNC_EN settings must be identical. 0 (Default) Disabled. Must be 0 for Fast Mode or Fast-Mode Plus. 1 Enabled
3:1	I2C_SCL_DBNC_CNT	I²C SCL debounce count. Number of MCLKs to debounce SCL input **Note:** The I2C_SDA_DBNC_CNT and I2C_SCL_DBNC_CNT settings must be identical. 000 0 MCLKs 010 2 MCLKs 100 (Default) 4 MCLKs 110 6 MCLKs 001 1 MCLK 011 3 MCLKs 101 5 MCLKs 111 7 MCLKs

Bits	Name	Description
0	I2C_SCL_DBNC_EN	I²C SCL debounce count enable. **Note:** The settings of I2C_SDA_DBNC_EN and I2C_SCL_DBNC_EN must be identical. 0 (Default) Disabled. Must be 0 for Fast Mode or Fast-Plus Mode. 1 Enabled

7.3.12 I²C Stretch

Address 0x100F

R/W	7	6	5	4	3	2	1	0
	I2C_STRETCH							
Default	0	0	0	0	0	0	1	1

Bits	Name	Description
7:0	I2C_STRETCH	I²C stretch. Number of additional MCLKs to clock stretch after the slave is ready 0000 0011 (Default) 3 MCLKs

7.3.13 I²C Timeout

Address 0x1010

R/W	7	6	5	4	3	2	1	0
	MAS_I2C_NACK	MAS_TO_DIS	MAS_TO_SEL		ACC_TO_DIS	ACC_TO_SEL		
Default	1	0	1	1	0	1	1	1

Bits	Name	Description
7	MAS_I2C_NACK	APB master I²C NACK. Determines whether clock stretching or a NACK occurs if an APB access is attempted and I²C is not APB master. 0 I²C clock stretches if an APB access is attempted while I²C is not APB master. 1 (Default) I²C NACKs if APB access is attempted while I²C is not APB master.
6	MAS_TO_DIS	APB master access timeout disable 0 (Default) Enabled 1 Disabled
5:4	MAS_TO_SEL	APB master access timeout select. Determines the timeout duration. 00 64 ms 01 128 ms 10 256 ms 11 (Default) 512 ms
3	ACC_TO_DIS	APB access timeout disable. 0 (Default) Enabled 1 Disabled
2:0	ACC_TO_SEL	APB access timeout select. Determines the timeout duration in MCLKs. 000 7 MCLKs 010 31 MCLKs 100 127 MCLKs 110 511 MCLKs 001 15 MCLKs 011 63 MCLKs 101 255 MCLKs 111 (Default) 65,535 MCLKs

7.4 Power Down and Headset Detects

7.4.1 Power Down Control 1

Address 0x1101

R/W	7	6	5	4	3	2	1	0
	ASP_DAO_PDN	ASP_DAI_PDN	MIXER_PDN	EQ_PDN	HP_PDN	ADC_PDN	—	PDN_ALL
Default	1	1	1	1	1	1	1	1

Bits	Name	Description
7	ASP_DAO_PDN	ASP output path power down. Configures ASP SDOUT path power state. 0 Powered up 1 (Default) Powered down, SDOUT is Hi-Z; ASP_DAO1 is powered down. The setting does not tristate the serial port clock.
6	ASP_DAI_PDN	ASP DAI0 input path power down. Configures ASP DAI0 SDIN path power state. 0 Powered up 1 (Default) Powered down. Setting this bit does not tristate the serial port clock.
5	MIXER_PDN	Mixer power down. Configures the mixer power state. 0 The mixer is powered up. 1 (Default) The mixer is powered down.
4	EQ_PDN	Equalizer power down. Configures the equalizer power state. See the restrictions described in Section 4.3. 0 Powered up 1 (Default) Powered down. All filter state data is reset to pass-through coefficients.
3	HP_PDN	HPOUTx power down 0 The HP driver and DACx are powered up. 1 (Default) The HP driver and DACx are powered down.

Bits	Name	Description
2	ADC_PDN	ADC power down 0 Powered up. The ADC is powered up. 1 (Default) The ADC is powered down.
1	—	Reserved
0	PDN_ALL	Codec power down. Configures the entire codec's power state except for PLL_START and SPDIF_TX_PDN (which is not affected in order to support Keep-Alive Mode). After power up (PDN_ALL: 1 → 0), individual subblocks are powered according to power-control programming. This bit is affected by LATCH_TO_VP (see p. 151). **Note:** The SRC power-down state depends on the SRC_PDN_OVERRIDE setting (see p. 132). 0 Powered up, per the individual *x*_PDN controls 1 (Default) Powered down. PDN_ALL must not be set without first enabling LATCH_TO_VP. After PDN_ALL is set and the entire codec is powered down, PDN_DONE is set, indicating that SCLK can be removed.

7.4.2 Power Down Control 2

Address 0x1102

R/W	7	6	5	4	3	2	1	0
	—			DISCHARGE_FILT+	SRC_PDN_OVERRIDE	ASP_DAI1_PDN	DAC_SRC_PDNB	ADC_SRC_PDNB
Default	1	0	0	0	0	1	0	0

Bits	Name	Description
7:5	—	Reserved
4	DISCHARGE_FILT+	Discharge FILT+ capacitor. Configures the state of the FILT+ pin internal clamp. Before setting this bit, ensure that the VD_FILT device input is connected to a supply, as shown in Table 3-2. 0 (Default) FILT+ is not clamped to ground. 1 FILT+ is clamped to ground. This must be set only if PDN_ALL = 1. Discharge time with an external 2.2-µF capacitor on FILT+ is ~46 ms.
3	SRC_PDN_OVERRIDE	SRC power down override. Configures the SRCs' power states. 0 (Default) Power state control for the DAC and ADC SRCs, which are controlled by the following smart logic: • DAC SRCs are off if SRC_BYPASS_DAC = 1. • ADC SRC is off if SRC_BYPASS_ADC = 1. • If PDN_ALL = 1, all SRCs are off. • If PDN_ALL = 0 and the respective ADC or DAC bypass bits = 0, the following controls each SRC's power state: —If SWIRE _SEL pin = VL, all SRCs are ON —If SWIRE_SEL pin = GNDL the following applies: –If DAI0 is enabled, the DAC SRCs are powered up. –If DAO is enabled, the ADC SRC is powered up. 1 DAC SRCs are controlled by DAC_SRC_PDNB and the ADC SRC is controlled by ADC_SRC_PDNB.
2	ASP_DAI1_PDN	ASP DAI1power down. This applies only to the S/PDIF port.If ASP_DAI_PDN is set, DAI1 is also powered down regardless of this register setting. 0 ASP power up 1 (Default) ASP power down
1	DAC_SRC_PDNB	DAC SRC power down. Configures the DAC ASP power state if SRC_PDN_OVERRIDE = 1. 0 (Default) Power down 1 Power up audio DAC SRC only
0	ADC_SRC_PDNB	ADC SRC power down. Configures the ADC SRC power state if SRC_PDN_OVERRIDE = 1. 0 (Default) Power down 1 Power up audio ADC SRC only

7.4.3 Power Down Control 3

Address 0x1103

R/W	7	6	5	4	3	2	1	0
	—	SW_CLK_STP_STAT_SEL		—		VPMON_PDNB	RING_SENSE_PDNB	—
Default	0	0	1	0	0	0	0	0

Bits	Name	Description
7	—	Reserved
6:5	SW_ CLK_ STP_ STAT_ SEL	SoundWire clock-stop status selection. Sets which functional blocks report as powered down before clearing CLOCK_STOP_ NOT_FINISHED (see p. 119). Section 4.8.13 describes SoundWire Clock-Stop Mode and wake events. **Note:** This field does not perform power-down commands for each functional block; the user must set those commands manually through SoundWire control. 00 The device does not perform any functions before clearing CLOCK_STOP_NOT_FINISHED. 01 (Default) Complete power-down (i.e., DAC, ADC, S/PDIF_TX, HS, and MICBIAS). Follow Ex. 5-2, Steps 1–7. After completing these steps, if the PLL is in use, to ensure that no commands are missed when exiting Clock Stop Mode, clear MCLK_SRC_SEL to use the SWIRE_CLK source, then power down the PLL by clearing PLL_START. Additionally, the headset-detection sequence must be completed (HSDET_CTRL = 00 or 10) before CLOCK_STOP_ NOT_FINISHED is cleared. 10 Only ADC_PDN, HP_PDN, and SPDIF_TX_PDN must be asserted. 11 Reserved
4:3	—	Reserved
2	VPMON_ PDNB	VPMON power down. VP monitor is described in Section 4.15.1. 0 (Default) Power down VPMON. 1 Power up VPMON.
1	RING_ SENSE_ PDNB	Ring sense power down 0 (Default) Power down ring sense. 1 Power up ring sense.
0	—	Reserved

7.4.4 Ring Sense Control 1

Address 0x1104

R/W	7	6	5	4	3	2	1	0
	—	RING_SENSE_PU_HIZ	—		HSBIAS_FILT_REF_RS	HPREF_RS	RS_TRIM_T	RS_TRIM_R
Default	0	1	0	0	0	0	0	0

Bits	Name	Description
7	—	Reserved
6	RING_ SENSE_ PU_HIZ	Ring-sense pull-up to Hi-Z. Used to decrease the value of the pull-up resistor to allow detection of impedances above or below ~1 kΩ (e.g., Mid-Z Detection Mode). See Section 4.14.3 for programming details. 0 Mid-Z Detection Mode 1 (Default) Hi-Z Detection Mode.
5:4	—	Reserved
3	HSBIAS_ FILT_ REF_RS	Headset bias filter reference. Sets the state of the HSBIAS_FILT_REF_RS switch. See Section 4.13, Section 4.14.3, and SW_REF_HSx on p. 136. 0 (Default) Ring sense is not used as the ground reference. 1 Ring sense is used as the ground reference.
2	HP_ REF_RS	Headphone amp reference. Determines whether ring sense is used as a ground reference. See Section 4.13, Section 4.14.3, and SW_REF_HSx on p. 136. 0 (Default) Ring sense is not used as the headphone amplifier ground reference. 1 Ring sense is used as the headphone amplifier ground reference.
1	RS_ TRIM_T	Ring-sense trim threshold. See Section 4.14.3 for programming details. 0 (Default) V_{IH} = 0.1 * VP; V_{IL} = 0.05 * VP. 1 V_{IH} = 0.35 * VP; V_{IL} = 0.3 * VP
0	RS_ TRIM_R	Ring-sense trim resistance. See Section 4.14.3 for programming details. 0 (Default) Pull-up resistance = 2.25 MΩ. 1 Pull-up resistance = 1.125 MΩ.

7.4.5 Ring Sense Control 2

Address 0x1105

R/W	7	6	5	4	3	2	1	0
	TS_RS_GATE	—						
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7	TS_RS_GATE	Tip/ring sense gating, Configures whether tip and ring sense are interdependent. Section 4.14.4 gives programming details. 0 (Default) Individual jacks. TIP_SENSE and RING_SENSE are independent of each other. 1 Combo plug. TIP_SENSE and RING_SENSE mutually gate each other.
6:0	—	Reserved

7.4.6 Oscillator Switch Control

Address 0x1107

R/W	7	6	5	4	3	2	1	0
	—							SCLK_PRESENT
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:1	—	Reserved
0	SCLK_PRESENT	SCLK present. Used to select the internal MCLK source. See Section 4.7 for programming details. 0→1 transition starts switch from RCO to selected internal MCLK (SCLK must be running first). 1→0 transition starts switch from selected internal MCLK to RCO (SCLK must keep running during transition). 0 (Default) SCLK may be present, but the internal MCLK is sourced from the RCO. 1 SCLK is present and the internal MCLK is sourced from the SCLK pin.

7.4.7 Oscillator Switch Status

Address 0x1109

R/O	7	6	5	4	3	2	1	0
	—					OSC_PDNB_STAT	OSC_SW_SEL_STAT	
Default	0	0	0	0	0	1	x	x

Bits	Name	Description
7:3	—	Reserved
2	OSC_PDNB_STAT	RCO power-down status. Indicates the RCO power state. See Section 4.7 for programming details. 0 RCO powered down 1 (Default) RCO powered up
1:0	OSC_SW_SEL_STAT	RCO switch status. Indicates the RCO oscillator switch status. The default is determined by the state of the SWIRE_SEL pin; see Section 1.See Section 4.7 for programming details. 00 In transition 01 (Default, if SWIRE_SEL is deasserted) RCO selected for internal MCLK 10 (Default, if SWIRE_SEL is asserted) SCLK/PLL selected for internal MCLK 11 Reserved

7.4.8 Ring Sense Control 3

Address 0x1112

R/W	7	6	5	4	3	2	1	0
	RS_INV	RS_PU_EN	RS_FALL_DBNCE_TIME			RS_RISE_DBNCE_TIME		
Default	0	0	0	1	1	0	1	1

Bits	Name	Description
7	RS_INV	Ring-sense invert. Used to invert the signal from the ring-sense circuit. Reverses the meaning of RS_UNPLUG_DBNC and RS_PLUG_DBNC (see p. 135). 0 (Default) Not inverted 1 Inverted
6	RS_PU_EN	Ring-sense pull-up enable. Configures whether the ring-sense pull-up is connected. 0 (Default) Pull-up disconnected 1 Pull-up connected
5:3	RS_FALL_DBNCE_TIME	Ring sense falling debounce time. Section 4.14.4 gives programming details. 000 0 ms 001 125 ms 010 250 ms 011 (Default) 500 ms 100 750 ms 101 1.0 s 110 1.25 s 111 1.5 s
2:0	RS_RISE_DBNCE_TIME	Ring sense rising debounce time. Section 4.14.4 gives programming details. 000 0 ms 001 125 ms 010 250 ms 011 (Default) 500 ms 100 750 ms 101 1.0 s 110 1.25 s 111 1.5 s

7.4.9 Tip Sense Control 1

Address 0x1113

R/W	7	6	5	4	3	2	1	0
	TS_INV	—	TS_FALL_DBNCE_TIME			TS_RISE_DBNCE_TIME		
Default	0	0	0	1	1	0	1	1

Bits	Name	Description
7	TS_INV	Tip sense raw signal invert. Used to invert the raw signal from the tip-sense circuit. Reverses the meaning of TS_UNPLUG_DBNC and TS_PLUG_DBNC (see p. 135). 0 (Default) Not inverted 1 Inverted
6	—	Reserved
5:3	TS_FALL_DBNCE_TIME	Tip sense falling debounce time. Section 4.14.4 gives programming details. 000 0 ms 010 250 ms 100 750 ms 110 1.25 s 001 125 ms 011 (Default) 500 ms 101 1.0 s 111 1.5 s
2:0	TS_RISE_DBNCE_TIME	Tip sense rising debounce time. Section 4.14.4 gives programming details. 000 0 ms 010 250 ms 100 750 ms 110 1.25 s 001 125 ms 011 (Default) 500 ms 101 1.0 s 111 1.5 s

7.4.10 Tip Sense/Ring Sense Indicator Status

Address 0x1115

R/O	7	6	5	4	3	2	1	0
	—				TS_UNPLUG_DBNC	TS_PLUG_DBNC	RS_UNPLUG_DBNC	RS_PLUG_DBNC
Default	0	0	0	0	x	x	x	x

Bits	Name	Description
7:4	—	Reserved
3	TS_UNPLUG_DBNC	Tip sense unplug debounce status. See Section 4.14.4 for details. Setting TS_INV reverses the meaning of this bit. 0 Condition is not present. 1 Condition is present.
2	TS_PLUG_DBNC	Tip sense plug debounce status. See Section 4.14.4 for details. Setting TS_INV reverses the meaning of this bit. 0 Condition is not present. 1 Condition is present.
1	RS_UNPLUG_DBNC	Ring sense unplug debounce status. See Section 4.14.4 for details. Setting RS_INV reverses the meaning of this bit. 0 Condition is not present. 1 Condition is present.
0	RS_PLUG_DBNC	Ring sense plug debounce status. See Section 4.14.4 for details. Setting RS_INV reverses the meaning of this bit. 0 Condition is not present. 1 Condition is present.

7.4.11 Headset Detect Control 1

Address 0x111F

R/W	7	6	5	4	3	2	1	0
	HSDET_COMP2_LVL				HSDET_COMP1_LVL			
Default	0	1	1	1	0	1	1	1

Bits	Name	Description
7:4	HSDET_COMP2_LVL	Headset Detect Comparator 2 level. Sets the reference level used by the HSDET Comparator 2. Table 3-16 lists tolerances for these values. See Section 4.13 for details. 0000 1.65 V 0111 (Default) 2.0 V… 1111 2.4 V
3:0	HSDET_COMP1_LVL	Headset Detect Comparator 1 level. Sets the reference level used by the HSDET Comparator 1. Table 3-16 lists tolerances for these values. See Section 4.13 for details. 0000 0.65 V 0111 (Default) 1.0 V… 1111 1.4 V

7.4.12 Headset Detect Control 2

Address 0x1120

R/W	7	6	5	4	3	2	1	0
	HSDET_CTRL		HSDET_SET		HSBIAS_REF	—	HSDET_AUTO_TIME	
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	HSDET_CTRL	Headset type detect mode. Sets the headset type detect mode. For details, see Section 4.13.1. 00 (Default) Manual, disabled. Headset-type-detect comparator and reference voltage are powered down. Internal switch controls in Section 7.4.13 are active; the system can configure them as needed. HSDET_SET must be set appropriately. 01 Manual, active. The headset-type-detect comparators and reference voltage are enabled. Comparator outputs are reported to their HSDET_COMPx_OUT status bits. The internal switch controls in Section 7.4.13 are active and the system can configure them as needed. HSDET_SET must also be set appropriately. 10 Automatic, disabled. The headset-type-detect comparator, reference voltage, and logic are powered down. Internal switch controls in Section 7.4.13 are ignored and remain in their previous state (i.e., not set to the values in Section 7.4.13). 11 Automatic, active. Headset-type-detect comparator, reference voltage, and logic are enabled. When set to this value from another state, logic starts a sequence that detects headset type; internal switches are configured into the correct state, as reported by HSDET_TYPE. Internal switch controls in Section 7.4.13 are ignored. When detection finishes, HSDET_AUTO_DONE is set and can be configured to cause an interrupt. HSDET_CTRL must then be set to 10.
5:4	HSDET_SET	Headset detect manual mode setting. Used for setting the MIC bias switches on the headset. In manual mode (HSDET_CTRL = 00 or 01), the setting indicates to the codec which headset pin is configured for HSBIAS and which is configured for ground. See Section 4.13 for details. HS3 Pin Configuration / HS4 Pin Configuration 00 (Default) GND / HSBIAS 01 HSBIAS / GND 10 GND / GND 11 Reserved / Reserved
3	HSBIAS_REF	Selects the pin used for the internal headset microphone bias LDO reference. 0 (Default) HSx_REF selected as the ground reference 1 Closed HSx selected as the ground
3:2	—	Reserved
1:0	HSDET_AUTO_TIME	Automatic headset detect cycle time. Sets the time that the HSDET logic waits in each detection phase. 00 (Default) 10 µs 01 20 µs 10 50 µs 11 100 µs

7.4.13 Headset Switch Control

Address 0x1121

R/W	7	6	5	4	3	2	1	0
	SW_REF_HS3	SW_REF_HS4	SW_HSB_FILT_HS3	SW_HSB_FILT_HS4	SW_HSB_HS3	SW_HSB_HS4	SW_GNDHS_HS3	SW_GNDHS_HS4
Default	1	1	1	1	0	0	1	1

Bits	Name	Description
7:6	SW_REF_HSx	Ref-to-HSx switch. Sets the Ref-to-HSx switch state. See Section 4.13. This bit is affected by LATCH_TO_VP (see p. 151). 0 Open 1 (Default) Closed
5:4	SW_HSB_FILT_HSx	HSBIAS_FILT_REF-to-HSx or HSx_REF switch. Sets the state of the HSBIAS_FILT_REF-to-HSx or HSx_REF switch, depending on the HSBIAS_REF setting. See Section 4.13. This bit is affected by LATCH_TO_VP. 0 Open 1 (Default) Closed
3:2	SW_HSB_HSx	HSBIAS-to-HSx switch. Sets the HSBIAS-to-HSx switch state. See Section 4.13. This bit is affected by LATCH_TO_VP. 0 (Default) Open 1 Closed
1:0	SW_GNDHS_HSx	GNDHS-to-HSx switch. Sets the GNDHS-to-HSx switch state. See Section 4.13. This bit is affected by LATCH_TO_VP. 0 Open 1 (Default) Closed

7.4.14 Headset Detect Status

Address 0x1124

R/O	7	6	5	4	3	2	1	0
	HSDET_COMP2_OUT	HSDET_COMP1_OUT	—				HSDET_TYPE	
Default	x	x	0	0	0	x	x	x

Bits	Name	Description
7:6	HSDET_ COMPx_ OUT	Headset detect comparator output state. Based on the HSDET_COMPx_LVL setting. See HSDET_CTRL (p. 136), HSDET_ AUTO_DONE (p. 142), and Section 4.13 for details. 0 Low 1 High
5:2	—	Reserved
1:0	HSDET_ TYPE	Headset detect type. Indicates the headset type determined by automatic headset detect logic (see Section 4.13.1). Ex. 5-5 provides a sample sequence. 00 1 01 2 10 3 11 4

7.4.15 Headset Clamp Disable

Address 0x1129

R/W	7	6	5	4	3	2	1	0
	—							HS_CLAMP_DISABLE
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:1	—	Reserved
0	HS_ CLAMP_ DISABLE	Headset clamp disable. Clamping devices suppress ground-noise when connecting to an external amplifier and the CS42L42 is powered down. Section 5.6 gives a programming example. This bit is affected by LATCH_TO_VP (see p. 151). 0 (Default) HS clamps are connected and provide ground-noise suppression 1 HS clamps are disconnected and no ground-noise suppression available

7.5 Clocking Registers

7.5.1 MCLK Source Select

Address 0x1201

R/W	7	6	5	4	3	2	1	0
	—						MCLKDIV	MCLK_SRC_SEL
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:2	—	Reserved
1	MCLKDIV	Master clock divide ratio. Selects the divide ratio between the selected MCLK source and the $MCLK_{INT}$. Section 4.7.2 lists supported MCLK rates and their associated programming settings. 0 (Default) Divide by 1 (source $MCLK_{INT}$ = ~12 MHz). 1 Divide by 2 (source $MCLK_{INT}$ = ~24 MHz) **Note:** Change this field only if PDN_ALL = 1.
0	MCLK_ SRC_ SEL	Master clock source select. Selects the internal master clock source. For programming details and examples, see Section 4.7. 0 (Default) SCLK pin 1 PLL clock

7.5.2 S/PDIF Clock Configuration

Address 0x1202

R/W	7	6	5	4	3	2	1	0
	—		SPDIF_CLK_DIV			SPDIF_LRCK_SRC_SEL	SPDIF_LRCK_CPOL	—
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	—	Reserved
5:3	SPDIF_ CLK_DIV	S/PDIF clock divide factor. For proper S/PDIF timing, use the following formula to choose the divide value: Divide factor = $MCLK_{INT}$/(128 x Fs). For details, see Section 4.10.2. For example, if Fs of the S/PDIF output should be 192 kHz, 128 x 192 kHz = 24.576 MHz. If ASP_SCLK is 24.576 MHz, the divide factor must be 1 (SPIF_CLK_DIV = 000). 000 (Default) 1 010 3 100 8 001 2 011 4 101–111Reserved
2	SPDIF_ LRCK_ SRC_ SEL	S/PDIF LRCK source select. S/PDIF LRCK requires a 50% duty cycle. If the externally provided duty cycle is not 50%, an internally generated LRCK is required. See Section 4.10.1. 0 (Default) Use internally generated LRCK. Typically used for Hybrid-Master Mode or with SoundWire. 1 Use LRCK from the ASP_LRCK pin. Typically used for Slave Mode.

Bits	Name	Description
1	SPDIF_ LRCK_ CPOL	S/PDIF LRCK polarity. Selects LRCK polarity. See Section 4.10.1. 0 (Default) Normal 1 Inverted
0	—	Reserved

7.5.3 FSYNC Pulse Width, Lower Byte

Address 0x1203

R/W	7	6	5	4	3	2	1	0
	FSYNC_PULSE_WIDTH_LB							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	FSYNC_ PULSE_ WIDTH_ LB	FSYNC pulse width LB. FSYNC_PULSE_WIDTH_UB | FSYNC_PULSE_WIDTH_LB provides an 11-bit field to set the duty cycle of LRCK in Hybrid-Master Mode. These combined value forms an integer number of SCLK periods within an LRCK frame that governs the LRCK high time. See Section 4.9.2 for usage details and Section 5 for a programming example. The value must be 1 less than the desired width of the LRCK pulse, measured in SCLK counts, as illustrated by the value below. FSYNC_PULSE_WIDTH_UB | FSYNC_PULSE_WIDTH_LB yield the following setting value: 000 0000 0000 (Default) LRCK is one SCLK wide.

7.5.4 FSYNC Pulse Width, Upper Byte

Address 0x1204

R/W	7	6	5	4	3	2	1	0
	—					FSYNC_PULSE_WIDTH_UB		
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:3	—	Reserved
2:0	FSYNC_PULSE_ WIDTH_UB	FSYNC pulse width UB. See description for FSYNC_PULSE_WIDTH_LB in Section 7.5.3. 000 (Default)

7.5.5 FSYNC Period, Lower Byte

Address 0x1205

R/W	7	6	5	4	3	2	1	0
	FSYNC_PERIOD_LB							
Default	1	1	1	1	1	0	0	1

Bits	Name	Description
7:0	FSYNC_ PERIOD_ LB	FSYNC period LB. FSYNC_PERIOD_UB | FSYNC_PERIOD_LB controls frequency (number of SCLKs per LRCK) of LRCK for ASP. Section 4.9.2 for details on how this register is used and Section 5 for a programming example. The final SCLKs per LRCK count is +1 of the value set in the UB|LB register field FSYNC_PERIOD_UB | FSYNC_PERIOD_LB yield the following setting values: 0x000 1 SCLK/LRCK … 0x0F9 (Default) 250 SCLKs/ LRCK … 0xFFF 4096 SCLKs/ LRCK

7.5.6 FSYNC Period, Upper Byte

Address 0x1206

R/W	7	6	5	4	3	2	1	0
	—				FSYNC_PERIOD_UB			
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:4	—	Reserved
3:0	FSYNC_ PERIOD_UB	FSYNC period UB. See description for FSYNC_PERIOD_LB in Section 7.5.5. 0000 (Default)

7.5.7 ASP Clock Configuration 1

Address 0x1207

R/W	7	6	5	4	3	2	1	0
	—		ASP_SCLK_EN	ASP_HYBRID_MODE	ASP_SCPOL_IN_ADC	ASP_SCPOL_IN_DAC	ASP_LCPOL_OUT	ASP_LCPOL_IN
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	—	Reserved
5	ASP_SCLK_EN	ASP SCLK enable. Must be set if DAO/DAI functionality is used. 0 (Default) Disabled 1 Enabled
4	ASP_HYBRID_MODE	ASP Hybrid-Master Mode. Allows the internal LRCK to be generated from SCLK. See Fig. 4-31 for details. 0 (Default) LRCK is input from external source which is synchronous to SCLK (Slave Mode). 1 LRCK is an output generated from SCLK (Hybrid Master Mode).
3	ASP_SCPOL_IN_ADC	ASP SCLK input polarity. Determines the drive polarity for ADC path. See Fig. 4-30 for details. 0 (Default) Normal 1 Inverted
2	ASP_SCPOL_IN_DAC	ASP SCLK input polarity. Determines the polarity for the DAC path. See Fig. 4-31 for details. 0 (Default) Normal 1 Inverted
1	ASP_LCPOL_OUT	ASP LRCK output drive polarity. Determines the polarity for the ASP LRCK output drive. See Fig. 4-31 for details. 0 (Default) Normal 1 Inverted
0	ASP_LCPOL_IN	ASP LRCK input polarity. Determines ASP LRCK input polarity (pad to logic). See Fig. 4-31 for details. 0 (Default) Normal 1 Inverted

7.5.8 ASP Frame Configuration

Address 0x1208

R/W	7	6	5	4	3	2	1	0
	—			ASP_STP	ASP_5050	ASP_FSD		
Default	0	0	0	1	0	0	0	0

Bits	Name	Description
7:5	—	Reserved
4	ASP_STP	ASP start phase. Controls which LRCK/FSYNC phase starts a frame. See Section 4.9.5 for details. 0 The frame begins when LRCK/FSYNC transitions from high to low 1 (Default) The frame begins when LRCK/FSYNC transitions from low to high
3	ASP_5050	ASP LRCK fixed 50/50 duty cycle. Determines whether the duty cycle is fixed or programmable. See Section 4.9.5 for details. 0 (Default) Programmable duty cycle. Determined by FSYNC_PULSE_WIDTH_LB (see p. 138), FSYNC_PULSE_WIDTH_UB, and FSYNC_PERIOD_xSB (see p. 138). 1 50/50 Mode. Fixed 50% duty cycle
2:0	ASP_FSD	ASP frame-start delay. Determines the delay before the start of an ASP frame in ASP_SCLK periods. See Section 4.9.2. 000 (Default) 0 delay 001 0.5 delay 010 1.0 delay … 101 2.5 delay 110–111 Reserved

7.5.9 FS Rate Enable

Address 0x1209

R/W	7	6	5	4	3	2	1	0
	—				FS_EN			
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:4	—	Reserved
3:0	FS_EN	Fs rate enable. Provides enables for all internally generated Fs rates. 0 = disabled; 1 = enabled. Section 4.11 gives details. FS_EN[0] Enable IASRC 96K and lower rates. FS_EN[1] Enable OASRC96K and lower rates. FS_EN[2] Enable IASRC 192, 176.4, and 176.471 K rates FS_EN[3] Enable OASRC 192, 176.4, and 176.471 K rates 0000 (Default) All disabled

7.5.10 Input ASRC Clock Select

Address 0x120A

R/W	7	6	5	4	3	2	1	0
	—						CLK_IASRC_SEL	
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:2	—	Reserved
1:0	CLK_IASRC_SEL	Input ASRC clock select. Selects input ASRC $MCLK_{INT}$ frequency. See Section 4.11 for programming details. 00 (Default) 6 MHz 01 12 MHz 10 24 MHz 11 Reserved

7.5.11 Output ASRC Clock Select

Address 0x120B

R/W	7	6	5	4	3	2	1	0
	—						CLK_OASRC_SEL	
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:2	—	Reserved
1:0	CLK_OASRC_SEL	Output ASRC clock select. Selects output ASRC $MCLK_{INT}$ frequency. See Section 4.11 for programming details. 00 (Default) 6 MHz 01 12 MHz 10 24 MHz 11 Reserved

7.5.12 PLL Divide Configuration 1

Address 0x120C

R/W	7	6	5	4	3	2	1	0
	—					PLL_REF_INV	SCLK_PREDIV	
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:3	—	Reserved
2	PLL_REF_INV	Invert PLL reference clock. See Table 4.7.3 for programming guidelines. 0 (Default) Normal 1 Inverted
1:0	SCLK_PREDIV	PLL reference divide select. See Table 4.7.3 for programming guidelines. 00 (Default) Divide by 1 01 Divide by 2 10 Divide by 4 11 Divide by 8

7.6 Interrupt Registers

7.6.1 ADC Overflow Interrupt Status

Address 0x1301

R/O	7	6	5	4	3	2	1	0
	—							ADC_OVFL
Default	0	0	0	0	0	0	0	x

Bits	Name	Description
7:1	—	Reserved
0	ADC_OVFL	ADC overflow. Indicates the overrange status in the corresponding signal path. Rising-edge state transitions may cause an interrupt, depending on the programming of the associated interrupt mask bit. 0 No digital clipping has occurred in the data path of the respective signal source. 1 Digital clipping has occurred in the data path of the respective signal source.

7.6.2 Mixer Interrupt Status

Address 0x1302

R/O	7	6	5	4	3	2	1	0
	—				EQ_BIQUAD_OVFL	EQ_OVFL	MIX_CHA_OVFL	MIX_CHB_OVFL
Default	0	0	0	0	x	x	x	x

Bits	Name	Description
7:4	—	Reserved
3	EQ_BIQUAD_OVFL	Digital equalizer biquad overflow. Indicates the overrange status in the individual biquads in the equalizer data path. Rising-edge state transitions may cause an interrupt, depending on the programming of the associated interrupt mask bit. 0 No digital clipping occurred in one of the individual biquads in the equalizer data path 1 Digital clipping occurred in one of the individual biquads in the equalizer data path

Bits	Name	Description
2	EQ_OVFL	Digital equalizer data path overflow. Indicates the overrange status of the equalizer data path. Rising-edge state transitions may cause an interrupt, depending on the programming of the associated interrupt mask bit. 0 No digital clipping occurred in the equalizer data path. 1 Digital clipping occurred in the equalizer data path. **Note:** If EQ overflow conditions occur regularly, it is recommended that the EQ coefficients be modified.
1	MIX_CHA_OVFL	Channel overflow. Indicates the overrange status in the corresponding signal path. Rising-edge state transitions may cause an interrupt, depending on the programming of the associated interrupt mask bit. 0 No digital clipping has occurred in the data path of the respective signal source. 1 Digital clipping has occurred in the data path of the respective signal source.
0	MIX_CHB_OVFL	

7.6.3 SRC Interrupt Status

Address 0x1303

R/O	7	6	5	4	3	2	1	0
	—				SRC_OUNLK	SRC_IUNLK	SRC_OLK	SRC_ILK
Default	0	0	0	0	x	x	x	x

Bits	Name	Description
7:4	—	Reserved
3	SRC_OUNLK	SRC unlock status. Indicates SRC unlock status for the output path. Status is valid only if serial-port LRCK is toggling. 0 Locked 1 Unlocked
2	SRC_IUNLK	SRC unlock status. Indicates SRC unlock status for the input path. Status is valid only if serial-port LRCK is toggling. 0 Locked 1 Unlocked
1	SRC_OLK	SRC lock status. Indicates SRC lock status for the ASP output path. Status is valid only if serial-port LRCK is toggling. 0 Unlocked 1 Locked
0	SRC_ILK	SRC lock status. Indicates SRC lock status for the ASP input path. Status is valid only if serial-port LRCK is toggling. 0 Unlocked 1 Locked

7.6.4 ASP RX Interrupt Status

Address 0x1304

R/O	7	6	5	4	3	2	1	0
	—			ASPRX_OVLD	ASPRX_ERROR	ASPRX_LATE	ASPRX_EARLY	ASPRX_NOLRCK
Default	0	0	0	x	x	x	x	x

Bits	Name	Description
7:5	—	Reserved
4	ASPRX_OVLD	ASP RX request overload. Set when too many input buffers request processing at once. 0No interrupt 1 Interrupt detected. ASP RX cannot retrieve data from the internal input buffers because at least one of the following violations has occurred: —The ASP RX core clock frequency is less than SCLK/8. —The LRCK frame (non-50/50 Mode) or LRCK subframe (50/50 Mode) period is less than 16 SCLK periods (assuming the ASP RX core clock frequency is equal to SCLK/8).
3	ASPRX_ERROR	ASP RX LRCK error. Logical OR of ASPRX_LATE and ASPRX_EARLY, described below. 0 No interrupt 1 Interrupt detected
2	ASPRX_LATE	ASP RX LRCK late. Determines whether the number of SCLK periods per LRCK phase (high or low) is greater than the expected count, as determined by the FSYNC_PERIOD_xSB and FSYNC_PULSE_WIDTH_x fields. 0 No interrupt 1 Interrupt detected
1	ASPRX_EARLY	ASP RX LRCK early. Determines whether the number of SCLK periods per LRCK phase (high or low) is less than the expected count, as determined by FSYNC_PERIOD_xSB (see p. 138) and FSYNC_PULSE_WIDTH_x (see p. 138). 0 No interrupt 1 Interrupt detected
0	ASPRX_NOLRCK	ASP RX no LRCK. Determines whether the SCLK periods counted exceeds twice the value of LRCK period (FSYNC_PERIOD_xSB) without an LRCK edge. 0 No interrupt 1 Interrupt detected

7.6.5 ASP TX Interrupt Status

Address 0x1305

R/O	7	6	5	4	3	2	1	0
	—				ASPTX_SMERROR	ASPTX_LATE	ASPTX_EARLY	ASPTX_NOLRCK
Default	0	0	0	0	x	x	x	x

Bits	Name	Description
7:4	—	Reserved
3	ASPTX_ SMERROR	ASP TX SM error. Determines whether the transmit state machine cannot retrieve data from output buffers; it is analogous to ASP Rx request overload. If all channel size and location registers are properly configured to nonoverlapping values, this error status should never be set. 0 No interrupt 1 Interrupt detected
2	ASPTX_ LATE	ASP TX LRCK late. Determines whether the number of SCLK periods per LRCK phase (high or low) is greater than the expected count as determined by the FSYNC_PERIOD_xSB and FSYNC_PULSE_WIDTH_x fields. 0 No interrupt 1 Interrupt detected
1	ASPTX_ EARLY	ASP TX LRCK early. Determines whether the number of SCLK periods per LRCK phase (high or low) is less than the expected count indicated by FSYNC_PERIOD_xSB (see p. 138) and FSYNC_PULSE_WIDTH_x (see p. 138). 0 No interrupt 1 Interrupt detected
0	ASPTX_ NOLRCK	ASP TX no LRCK. Determines whether the number of SCLK periods counted exceeds twice the value of LRCK period (FSYNC_PERIOD_xSB) without an LRCK edge. 0 No interrupt 1 Interrupt detected

7.6.6 Codec Interrupt Status

Address 0x1308

R/O	7	6	5	4	3	2	1	0
	—						HSDET_AUTO_DONE	PDN_DONE
Default	0	0	0	0	0	0	x	x

Bits	Name	Description
7:2	—	Reserved
1	HSDET_ AUTO_ DONE	Automatic headset detect done. Indicates when HSDET logic has finished its detection cycle and the headset can be read from HSDET_COMPx_OUT. 0 HSDET is disabled or has not completed its detection cycle. 1 The HSDET logic has completed its detection cycle.
0	PDN_ DONE	Power-down done. Indicates when the codec has powered down and MCLK can be stopped, as determined by various power-control and headset-interface register settings. 0 Not completely powered down 1 Powered down as a result of PDN_ALL having been set.

7.6.7 Detect Interrupt Status 1

Address 0x1309

R/O	7	6	5	4	3	2	1	0
	HSBIAS_SENSE	TIP_SENSE_PLUG	TIP_SENSE_UNPLUG	—				
Default	x	x	x	x	x	x	x	x

Bits	Name	Description
7	HSBIAS_SENSE	HSBIAS sense. Indicates whether the HSBIAS output current falls below the HSBIAS_SENSE_TRIP value. 0 Output current has not gone below the specified threshold. 1 Output current has gone below the specified threshold.
6	TIP_SENSE_PLUG	Tip sense plug event. Indicates the undebounced status of a plug event on the TIP_SENSE pin.[1] 0 No HP plug event 1 HP plug event
5	TIP_SENSE_UNPLUG	Tip sense unplug event. Indicates the undebounced status of an unplug event on the TIP_SENSE pin.[1] 0 (Default) No HP unplug event 1 HP unplug event
4:0	—	Reserved

1. This bit is affected by EVENT_STATUS_SEL (see p. 152). It is active only if TIP_SENSE_CTRL (p. 150) is configured so the tip-sense circuit is powered up. If the system is configured for standby operation, the sticky version of this bit (that also accounts for events that occurred during standby) can be read back after a wake event. Use EVENT_STATUS_SEL to retrieve this bit's information under that scenario.

7.6.8 Detect Interrupt Status 2

Address 0x130A

R/O	7	6	5	4	3	2	1	0
	DETECT_TRUE_FALSE	DETECT_FALSE_TRUE	—			HSBIAS_HIZ	SHORT_RELEASE	SHORT_DETECTED
Default	x	x	x	x	x	x	x	x

Bits	Name	Description
7	DETECT_TRUE_FALSE	Mic detect True-to-False. Indicates whether the mic level detector transitions from True to False. 0 No transition detected 1 Transition from True to False detected
6	DETECT_FALSE_TRUE	Mic detect False-to-True. Indicates whether the mic level detector transitions from False to True. 0 No transition detected 1 Transition from False to True detected
5:3	—	Reserved
2	HSBIAS_HIZ	HSBIAS Hi-Z engaged. 0 Not engaged 1 Engaged
1	SHORT_RELEASE	Short release.[1] Indicates whether the S0 button-detect block output a low-to-high edge on the version of the short condition indicator that is sent to the control port. This status is debounced as per DEBOUNCE_TIME in Normal Mode. If M_SHORT_RELEASE = 0, a shadow register captures up to two button-press events. Reading the register once transfers shadow register contents into this register, therefore, the register can be read twice per interrupt event. Shadow bits are not available in Wake Mode (only VP present). This bit is affected by EVENT_STATUS_SEL (see p. 152). 0 HSBIAS_IN has not transitioned above the short detect threshold. 1 HSBIAS_IN transitioned above the short detect threshold.
0	SHORT_DETECTED	Short detected.[1] Indicates whether a high-to-low edge occurred on the version of the short condition indicator, sourced by the S0 button-detect block output, that is sent to the control port. Status is debounced per DEBOUNCE_TIME in Normal Mode.This bit is affected by EVENT_STATUS_SEL (see p. 152). 0 HSBIAS_IN has not transitioned below the short-detect threshold. 1 HSBIAS_IN transitioned below the short-detect threshold.

1. This bit is active only if DETECT_MODE (see p. 151) is set so the short-detection circuit is active. If the system is configured for standby operation, the sticky version of this bit (which accounts for events that occurred during standby) can be read back after a wake event. Use EVENT_STATUS_SEL to retrieve this bit's information under that scenario.

7.6.9 SRC Partial Lock Interrupt Status

Address 0x130B

R/O	7	6	5	4	3	2	1	0
	—	DAC_UNLK	ADC_UNLK	—		DAC_LK	—	ADC_LK
Default	x	x	x	x	x	x	x	x

Bits	Name	Description
7	—	Reserved
6	DAC_UNLK	ASP input SRC unlock status. 0 Locked 1 Unlocked
5	ADC_UNLK	ASP output SRC unlock status. 0 Locked 1 Unlocked
4:3	—	Reserved
2	DAC_LK	ASP input partial SRC lock status. 0 Unlocked 1 Locked
1	—	Reserved
0	ADC_LK	ASP output partial SRC lock status. 0 Unlocked 1 Locked

7.6.10 VP Monitor Interrupt Status

Address 0x130D

R/O	7	6	5	4	3	2	1	0
	—							VPMON_TRIP
Default	0	0	0	0	0	0	0	x

Bits	Name	Description
7:1	—	Reserved
0	VPMON_TRIP	VP monitor interrupt. If the VP power supply falls below 2.6 V, this bit is set. See Section 4.15.1 for details. 0 No interrupt 1 Interrupt detected

7.6.11 PLL Lock Interrupt Status

Address 0x130E

R/O	7	6	5	4	3	2	1	0
	—							PLL_LOCK
Default	0	0	0	0	0	0	0	x

Bits	Name	Description
7:1	—	Reserved
0	PLL_LOCK	PLL lock. Indicates the lock state of the PLL. 0 No interrupt 1 Interrupt detected

7.6.12 Tip/Ring Sense Plug/Unplug Interrupt Status

Address 0x130F

R/O	7	6	5	4	3	2	1	0
	—				TS_UNPLUG	TS_PLUG	RS_UNPLUG	RS_PLUG
Default	0	0	0	0	x	x	x	x

Bits	Name	Description
7:4	—	Reserved
3	TS_UNPLUG	Tip sense unplug status. See Section 4.14.4 for details. Setting TS_INV reverses the meaning of this bit. 0 Condition is not present. 1 Condition is present.
2	TS_PLUG	Tip sense plug status. See Section 4.14.4 for details. Setting TS_INV reverses the meaning of this bit. 0 Condition is not present. 1 Condition is present.
1	RS_UNPLUG	Ring sense unplug status. See Section 4.14.4 for details. Setting RS_INV reverses the meaning of this bit. 0 Condition is not present. 1 Condition is present.
0	RS_PLUG	Ring sense plug status. See Section 4.14.4 for details. Setting RS_INV reverses the meaning of this bit. 0 Condition is not present. 1 Condition is present.

7.6.13 ADC Overflow Interrupt Mask

Address 0x1316

R/W	7	6	5	4	3	2	1	0
	—							M_ADC_OVFL
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7:1	—	Reserved
0	M_ADC_ OVFL	ADC_OVFL mask. 0 Unmasked 1 (Default) Masked

7.6.14 Mixer Interrupt Mask

Address 0x1317

R/W	7	6	5	4	3	2	1	0
	—				M_EQ_ BIQUAD_OVFL	M_EQ_OVFL	M_MIX_CHA_OVFL	M_MIX_CHB_OVFL
Default	0	0	0	0	1	1	1	1

Bits	Name	Description
7:4	—	Reserved
3	M_EQ_BIQUAD_OVFL	EQ_BIQUAD_OVFL mask. 0 Unmasked 1 (Default) Masked
2	M_EQ_OVFL	EQ_OVFL mask. 0 Unmasked 1 (Default) Masked
1	M_MIX_CHA_OVFL	MIXER_CHx_OVFL mask. 0 Unmasked 1 (Default) Masked
0	M_MIX_CHB_OVFL	

7.6.15 SRC Interrupt Mask

Address 0x1318

R/W	7	6	5	4	3	2	1	0
	—				M_SRC_OUNLK	M_SRC_IUNLK	M_SRC_OLK	M_SRC_ILK
Default	0	0	0	0	1	1	1	1

Bits	Name	Description
7:4	—	Reserved
3	M_SRC_ OUNLK	SRC_OUNLK mask. 0 Unmasked 1 (Default) Masked
2	M_SRC_ IUNLK	SRC_IUNLK mask. 0 Unmasked 1 (Default) Masked
1	M_SRC_OLK	SRC_OLK mask. 0 Unmasked 1 (Default) Masked
0	M_SRC_ILK	SRC_ILK mask. 0 Unmasked 1 (Default) Masked

7.6.16 ASP RX Interrupt Mask

Address 0x1319

R/W	7	6	5	4	3	2	1	0
	—			M_ASPRX_OVLD	M_ASPRX_ERROR	M_ASPRX_LATE	M_ASPRX_EARLY	M_ASPRX_NOLRCK
Default	0	0	0	1	1	1	1	1

Bits	Name	Description
7:5	—	Reserved
4	M_ASPRX_ OVLD	ASPRX_OVFL mask. 0 Unmasked 1 (Default) Masked
3	M_ASPRX_ ERROR	ASPRX_ERROR mask. 0 Unmasked 1 (Default) Masked
2	M_ASPRX_ LATE	ASPRX_LATE mask. 0 Unmasked 1 (Default) Masked
1	M_ASPRX_ EARLY	ASPRX_EARLY mask. 0 Unmasked 1 (Default) Masked
0	M_ASPRX_ NOLRCK	ASPRX_NOLRCK mask. 0 Unmasked 1 (Default) Masked

7.6.17 ASP TX Interrupt Mask

Address 0x131A

R/W	7	6	5	4	3	2	1	0
	—				M_ASPTX_SMERROR	M_ASPTX_LATE	M_ASPTX_EARLY	M_ASPTX_NOLRCK
Default	0	0	0	0	1	1	1	1

Bits	Name	Description
7:4	—	Reserved
3	M_ASPTX_ SMERROR	ASPTX_SMERROR mask. 0 Unmasked 1 (Default) Masked
2	M_ASPTX_ LATE	ASPTX_LATE mask. 0 Unmasked 1 (Default) Masked
1	M_ASPTX_ EARLY	ASPTX_EARLY mask. 0 Unmasked 1 (Default) Masked
0	M_ASPTX_ NOLRCK	ASPTX_NOLRCK mask. 0 Unmasked 1 (Default) Masked

7.6.18 Codec Interrupt Mask

Address 0x131B

R/W	7	6	5	4	3	2	1	0
	—						M_HSDET_AUTO_DONE	M_PDN_DONE
Default	0	0	0	0	0	0	1	1

Bits	Name	Description
7:2	—	Reserved
1	M_HSDET_ AUTO_DONE	HSDET_AUTO_DONE mask. 0 Unmasked 1 (Default) Masked
0	M_PDN_ DONE	PDN_DONE mask. 0 Unmasked 1 (Default) Masked

7.6.19 SRC Partial Lock Interrupt Mask

Address 0x131C

R/W	7	6	5	4	3	2	1	0
	—	M_DAC_UNLK	M_ADC_UNLK	—		M_DAC_LK	—	M_ADC_LK
Default	0	1	1	1	1	1	1	1

Bits	Name	Description
7	—	Reserved
6	M_DAC_ UNLK	ASP input unlock mask. 0 Unmasked 1 (Default) Masked
5	M_ADC_ UNLK	ASP output unlock mask. 0 Unmasked 1 (Default) Masked
4–3	—	Reserved
2	M_DAC_LK	ASP input lock mask. 0 Unmasked 1 (Default) Masked
1	—	Reserved
0	M_ADC_LK	ASP output lock mask. 0 Unmasked 1 (Default) Masked

7.6.20 VP Monitor Interrupt Mask

Address 0x131E

R/W	7	6	5	4	3	2	1	0
	—							M_VPMON_TRIP
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7:1	—	Reserved
0	M_ VPMON_ TRIP	VP monitor mask. 0 Unmasked. Unmask/enable this bit only when VP exceeds the detection voltage threshold; applicable to power-up conditions or if VP is not at its steady-state voltage. 1 (Default) Masked

7.6.21 PLL Lock Mask

Address 0x131F

R/W	7	6	5	4	3	2	1	0
	—							M_PLL_LOCK
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7:1	—	Reserved
0	M_PLL_ LOCK	PLL lock mask. 0 Unmasked 1 (Default) Masked

7.6.22 Tip/Ring Sense Plug/Unplug Interrupt Mask

Address 0x1320

R/W	7	6	5	4	3	2	1	0
	—				M_TS_UNPLUG	M_TS_PLUG	M_RS_UNPLUG	M_RS_PLUG
Default	0	0	0	0	1	1	1	1

Bits	Name	Description
7:4	—	Reserved
3	M_TS_ UNPLUG	Tip sense unplug mask. 0 Unmasked 1 (Default) Masked
2	M_TS_ PLUG	Tip sense plug mask. 0 Unmasked 1 (Default) Masked
1:0	—	Reserved
1	M_RS_ UNPLUG	Ring sense unplug mask. 0 Unmasked 1 (Default) Masked
0	M_RS_ PLUG	Ring sense plug mask. 0 Unmasked 1 (Default) Masked

7.7 Fractional-N PLL Registers

7.7.1 PLL Control 1

Address 0x1501

R/W	7	6	5	4	3	2	1	0
	—							PLL_START
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:1	—	Reserved
0	PLL_ START	PLL start. If MCLK_SRC_SEL = 0, the PLL is bypassed and can be powered down by clearing PLL_START. See Section 4.7.3. 0 (Default) Powered off. 1 Powered on

7.7.2 PLL Division Fractional Bytes 0–2

Address 0x1502–0x1504

R/W	7	6	5	4	3	2	1	0
0x1502	PLL_DIV_FRAC[7:0]							
0x1503	PLL_DIV_FRAC[15:8]							
0x1504	PLL_DIV_FRAC[23:16]							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PLL_DIV_ FRAC[7:0]	PLL fractional portion of divide ratio LSB. See Section 4.7.3 for details. There are 3 bytes of PLL feedback divider fraction portion: This is LSB byte; e.g., 0xFF means ($2^{-17} + 2^{-18} + \ldots + 2^{-24}$) 0000 0000 (Default)
7:0	PLL_DIV_ FRAC[15:8]	PLL fractional portion of divide ratio middle byte; e.g., 0xFF means ($2^{-9} + 2^{-10} + \ldots + 2^{-16}$). See Section 4.7.3 for details. 0000 0000 (Default)
7:0	PLL_DIV_ FRAC[23:16]	PLL fractional portion of divide ratio MSB; e.g., 0xFF means ($2^{-1} + 2^{-2} + \ldots + 2^{-8}$). See Section 4.7.3 for details. 0000 0000 (Default)

7.7.3 PLL Division Integer

Address 0x1505

R/W	7	6	5	4	3	2	1	0
	PLL_DIV_INT							
Default	0	1	0	0	0	0	0	0

Bits	Name	Description
7:0	PLL_DIV_INT	PLL integer portion of divide ratio. Integer portion of PLL feedback divider. See Section 4.7.3 for details. 0100 0000 (Default)

7.7.4 PLL Control 3

Address 0x1508

R/W	7	6	5	4	3	2	1	0
	PLL_DIVOUT							
Default	0	0	0	1	0	0	0	0

Bits	Name	Description
7:0	PLL_ DIVOUT	Final PLL clock output divide value. See Section 4.7.3 for configuration details. 0001 0000 (Default)

7.7.5 PLL Calibration Ratio

Address 0x150A

R/W	7	6	5	4	3	2	1	0
	PLL_CAL_RATIO							
Default	1	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PLL_CAL_ RATIO	PLL calibration ratio. See Section 4.7.3 for configuration details. Target value for PLL VCO calibration. 1000 0000 (Default)

7.7.6 PLL Control 4

Address 0x151B

R/W	7	6	5	4	3	2	1	0
	—						PLL_MODE	
Default	0	0	0	0	0	0	1	1

Bits	Name	Description
7:2	—	Reserved
1:0	PLL_ MODE	PLL bypass mode. Configures 500/512 and 1029/1024 factor bypasses. See Section 4.7.3 for configuration details. 00 Unsupported 01 500/512 only (1029/1024 bypassed) 10 1029/1024 only (500/512 bypassed) 11 (Default) Both bypassed

7.8 HP Load-Detect Registers

7.8.1 Load-Detect R/C Status

Address 0x1925

R/O	7	6	5	4	3	2	1	0
	—			CLA_STAT	—		RLA_STAT	
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	—	Reserved
4	CLA_STAT	Capacitor load-detection result for HPA. See Section 4.4.4 for details. **Note:** Low capacitance results were determined with C_L = 1 nF; high capacitance results were determined with C_L = 10 nF. 0 (Default) High capacitance ($C_L \geq$ ~2 nF) 1 Low capacitance (C_L < ~2 nF)
1:0	RLA_STAT	Resistor load-detection result for HPA. See Section 4.4.4 for details. 00 (Default) 15 Ω 01 30 Ω 10 3 kΩ 11 Reserved

7.8.2 HP Load Detect Done

Address 0x1926

R/O	7	6	5	4	3	2	1	0
	—							HPLOAD_DET_DONE
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:1	—	Reserved
0	HPLOAD_ DET_DONE	HP load detect done. Indicates whether HP load detection is finished. See Section 4.4.4 for details. 0 (Default) HP load is not finished. 1 HP load is finished.

7.8.3 HP Load Detect Enable

Address 0x1927

R/O	7	6	5	4	3	2	1	0
	—							HP_LD_EN
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:1	—	Reserved
0	HP_LD_EN	HP load detect enable. A 0-to-1 bit transition initiates load detection. See Section 4.4.4 for details. 0 (Default) Disabled 1 Enabled

7.9 Headset Interface Registers

7.9.1 HSBIAS Sense and Hi-Z Autocontrol

Address 0x1B70

R/W	7	6	5	4	3	2	1	0
	HSBIAS_SENSE_EN	AUTO_HSBIAS_HIZ	TIP_SENSE_EN	—			HSBIAS_SENSE_TRIP	
Default	0	0	0	0	0	0	1	1

Bits	Name	Description
7	HSBIAS_ SENSE_ EN	HSBIAS current sense enable. Configures HSBIAS output current sense through the external 2.21-kΩ resistor. 0 (Default) Disabled. Must be disabled in Short Detect-Only Mode when the headset circuit disconnects the mic module. Due to the open circuit, HSBIAS_SENSE = 1 if the S0 button is not being pressed. The current sense trip point is set via HSBIAS_SENSE_TRIP. An interrupt can be configured to occur when the sensed current falls below the trip point. 1 Enabled
6	AUTO_ HSBIAS_ HIZ	HSBIAS Hi-Z autocontrol. Sets how the Hi-Z Mode on the HSBIAS output is controlled. This bit is affected by LATCH_TO_ VP (see p. 151). 0 (Default) No change to HSBIAS output. The Hi-Z Mode is also cleared if it had been previously set. 1 Sets HSBIAS to Hi-Z Mode when the current sense goes below its trip point or a HP unplug event occurs, depending on which detector is enabled. To disengage Hi-Z Mode, clear this bit before resetting it to 1.

Bits	Name	Description
5	TIP_ SENSE_ EN	Tip sense enable. Updatable only if LATCH_TO_VP is enabled. If AUTO_HSBIAS_HIZ = 1, a tip sense unplug event can be configured to affect its control. 0 (Default) TIP_SENSE unplug event does not affect the HSBIAS. 1 TIP_SENSE unplug event affects the HSBIAS Hi-Z Mode if AUTO_HSBIAS_HIZ = 1.
4:3	—	Reserved
2:0	HSBIAS_ SENSE_ TRIP	HSBIAS current sense trip point. Sets the HSBIAS current trip point sensed across the external 2.21-kΩ bias resistor. Current sense trip point in Table 3-15 lists tolerances for these values. 000 12 µA 010 41 µA 100 64 µA 110 93 µA 001 23 µA 011 (Default) 52 µA 101 75 µA 111 104 µA

7.9.2 Wake Control

Address 0x1B71

R/W	7	6	5	4	3	2	1	0
	M_MIC_WAKE	M_HP_WAKE	WAKEB_MODE	—				WAKEB_CLEAR
Default	1	1	0	0	0	0	0	0

Bits	Name	Description
7	M_MIC_ WAKE	Mask mic button detect wake.[1,2] Configures the mask for the mic-button detect wake status. 0 Unmasked. The occurrence of a wake interrupt affects WAKE. 1 (Default) Masked. The occurrence of a wake interrupt does not affect WAKE.
6	M_HP_ WAKE	Mask tip sense wake.[1,2] Configures the mask for the tip-sense wake status. 0 Unmasked. The occurrence of a wake interrupt affects WAKE. 1 (Default) Masked. The occurrence of a wake interrupt does not affect WAKE.
5	WAKEB_ MODE	WAKE output mode.[1] Configures the mode of operation for the WAKE output 0 (Default) Output is latched low after a trigger event until WAKEB_CLEAR is toggled. 1 Output follows the combination logic directly (nonlatched).
4:1	—	Reserved
0	WAKEB_ CLEAR	WAKE output clear. Applicable only if WAKEB_MODE = 0 and an event triggers the WAKE output to latch low. 0 (Default) WAKE output normal operation. If WAKEB_MODE = 1, WAKEB_CLEAR does not deassert WAKE, but clears TIP_SENSE_PLUG, TIP_SENSE_UNPLUG, SHORT_DETECTED, SHORT_RELEASE in the VP domain. 1 WAKE output deasserted (the TIP_SENSE_PLUG, TIP_SENSE_UNPLUG, SHORT_DETECTED, SHORT_RELEASE bits in the VP domain are also cleared).

1. This bit can be changed only if LATCH_TO_VP is enabled (see p. 151).
2. Before unmasking status, pending wake events must be cleared via WAKEB_CLEAR. They are also cleared when deactivating and then reactivating the relevant mode using DETECT_MODE (see p. 151). A powered-down device using the CS42L42 does not respond to the associated detect wake event.

7.9.3 ADC Disable Mute

Address 0x1B72

R/W	7	6	5	4	3	2	1	0
	ADC_DISABLE_S0_MUTE	—						
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7	ADC_ DISABLE_S0_ MUTE	Disable ADC automute on S0 button press. For S0 automute to operate, DETECT_MODE must be set to 11. 0 (Default) Enabled. If HSBIAS_IN goes below the S0 threshold, ADC mutes. If DETECT_MODE = 11 and the HSBIAS_IN pin is floating, the ADC path could be muted due to the pin floating below the S0 trip threshold. 1 Disabled
6:0	—	Reserved

7.9.4 Tip Sense Control 2

Address 0x1B73

R/W	7	6	5	4	3	2	1	0
	TIP_SENSE_CTRL		TIP_SENSE_INV	—			TIP_SENSE_DEBOUNCE	
Default	0	0	0	0	0	0	1	0

Bits	Name	Description
7:6	TIP_SENSE_ CTRL	Tip sense control.Configures operation of the tip-sense circuit. **Note:** This bit can be updated only if LATCH_TO_VP (see p. 151) is enabled. 00 (Default) Disabled. The tip-sense circuit is powered down and does not report to the status registers (TIP_ SENSE_PLUG and TIP_SENSE_UNPLUG in the VP domain are also cleared). 01 Digital input. Internal weak current source pull-up is disabled. 10 Reserved 11 Short detect. Internal weak current source pull-up is enabled.

Bits	Name	Description
5	TIP_SENSE_ INV	Tip sense invert. Used to invert the signal from the tip-sense circuit. Updatable only if LATCH_TO_VP is enabled. 0 (Default) Not inverted 1 Inverted
4:2	—	Reserved
1:0	TIP_SENSE_ DEBOUNCE	Tip sense debounce time. Sets tip sense unplug event (TIP_SENSE = 0) debounce time before status is reported. Timings are approximate and vary with $MCLK_{INT}$ and Fs_{INT}. 00 No debounce 01 200 ms 10 (Default) 500 ms 11 1000 ms

7.9.5 Miscellaneous Detect Control

Address 0x1B74

R/W	7	6	5	4	3	2	1	0
	—			DETECT_MODE		HSBIAS_CTRL		PDN_MIC_LVL_ DETECT
Default	0	0	0	0	0	0	1	1

Bits	Name	Description
7:5	—	Reserved
4:3	DETECT_ MODE	Detection mode setting.[1] Sets the appropriate mode to be used for the mic button detection. This bit is affected by LATCH_ TO_VP (see p. 151). 00 (Default) Inactive (SHORT_DETECTED and SHORT_RELEASE in the VP domain are also cleared) 01 Short detect only. Normal interrupts do not function; the INT pin follows the S0 comparator directly while the SHORT_ DETECTED mask is cleared and remains high while the SHORT_DETECTED mask is set. 10 Reserved 11 Normal Mode. HSBIAS output uses a high-performance reference for 2.0- or 2.7-V Mode. See HSBIAS_CTRL. If LATCH_TO_VP = 1, PDN_ALL = 1 overrides DETECT_MODE setting and powers down the CS42L42.
2:1	HSBIAS_ CTRL	HS bias output control.[1] Sets the mode for the HSBIAS output pin. See the DETECT_MODE description, above. 00 Output is Hi-Z. The HSBIAS output uses a low-performance, low-power reference. If the HSBIAS-to-HS4 switch is closed (SW_HSB_HS4 = 1), the HS4 pin can float unless terminated with a load of at least 100 kΩ. 01 (Default) 0.0 V (weak ground, see Table 3-14, Footnote 1). 10 2.0 V. Wait for circuits to completely power up. A setting of 10 or 11 is required for headset interface functionality. 11 2.7 V. Wait for circuits to completely power up. A setting of 10 or 11 is required for headset interface functionality. **Note:** If DETECT_MODE = 11, the HSBIAS output uses a high-performance reference. If DETECT_MODE ≠ 11, the HSBIAS output uses a low-performance, low-power reference. • To avoid audible artifacts if the HS path is active, the path must be muted before changing the HSBIAS settings. • LATCH_TO_VP = 1, PDN_ALL = 1 overrides HSBIAS_CTRL settings and powers down the CS42L42. • Table 3-15 more precisely specifies voltages present on the HSBIAS output for each HSBIAS_CTRL setting, accounting for the effect of DETECT_MODE. It also documents HS bias power-up time.
0	PDN_MIC_ LVL_ DETECT	Power-down mic DC level detect. Configures the power state of the mic-level detect circuit. 0 Powered up. See Table 3-14 for the level detect power-up time. 1 (Default) Powered down This feature can be used at any time (set in parallel with any other detection mode), but should not be continuously enabled if the HS input is enabled because the HS noise performance is degraded.

1. This bit can be updated only if LATCH_TO_VP is enabled.

7.9.6 Mic Detect Control 1

Address 0x1B75

R/W	7	6	5	4	3	2	1	0
	LATCH_TO_VP	EVENT_STATUS_SEL	HS_DETECT_LEVEL					
Default	0	0	0	1	1	1	1	1

Bits	Name	Description
7	LATCH_ TO_VP	Latch to VP registers. Controls the transfer of writable control registers in the VD_FILT supply domain to duplicate registers in the VP supply domain. Can be used to enable setting sticky status bits in the VP domain. 0 (Default) Inhibits the transfer of VD_FILT registers to VP registers (latched mode). Enables the setting of VP sticky status latches. 1 Transfers VD_FILT fields to VP fields (transparent mode). Disables setting of VP sticky status latches. Affected registers: • DETECT_MODE on p. 151 • TIP_SENSE_EN on p. 150 • M_MIC_WAKE on p. 150 • M_HP_WAKE on p. 150 • M_SHORT_DETECTED on p. 153 • HSBIAS_CTRL on p. 151 • SW_REF_HSx on p. 136 • SW_HSB_FILT_HSx on p. 136 • SW_HSB_HSx on p. 136 • SW_GNDHS_HSx on p. 136 • WAKEB_MODE p. 150 **Note:** The description of PDN_ALL on p. 132 describes the interdependency between LATCH_TO_VP and PDN_ALL.

Bits	Name	Description
6	EVENT_STATUS_SEL	Event status selection. Selects the level of processing on readable status originating in the VP supply domain. 0 (Default) Raw (unprocessed) status events are selected. 1 Sticky processed status events are selected. Affected registers: • TIP_SENSE_PLUG on p. 142 • TIP_SENSE_UNPLUG on p. 142 • SHORT_DETECTED on p. 143 • SHORT_RELEASE on p. 143
5:0	HS_DETECT_LEVEL	Mic 2 voltage level-detect setting (% of HSBIAS). Sets the level of the threshold to be used for detecting headset modules. 01 1111 (Default) The DC detector can be used at any time (set in parallel with any other detection mode), but should not be continuously enabled if the HS input is enabled because the HS noise performance is degraded. DC detector settling time is 11 ms.

7.9.7 Mic Detect Control 2

Address 0x1B76

R/W	7	6	5	4	3	2	1	0
	DEBOUNCE_TIME			—				
Default	0	0	1	0	1	1	1	1

Bits	Name	Description
7:5	DEBOUNCE_TIME	Debounce time (ms). Sets the time to be used for S0 button detect (SHORT_DETECTED and SHORT_RELEASE) debounce when in Normal Mode. Timings are approximate and vary with $MCLK_{INT}$. 000 10 ms 001 (Default) 20 ms 010 30 ms 011 40 ms 100 50 ms 101 60 ms 110 70 ms 111 80 ms
4:0	—	Reserved

7.9.8 Detect Status 1

Address 0x1B77

R/O	7	6	5	4	3	2	1	0
	TIP_SENSE	HSBIAS_HIZ	—					
Default	x	x	0	x	x	x	x	x

Bits	Name	Description
7	TIP_SENSE	TIP_SENSE circuit status. The plug-to-unplug edge is debounced for the set debounce time (see TIP_SENSE_DEBOUNCE, p. 151). 0 HP not plugged in 1 HP plugged in
6	HSBIAS_HIZ	HSBIAS Hi-Z Mode. Reports whether the HSBIAS Hi-Z Mode is enabled or disabled. 0 Hi-Z Mode is disabled. 1 Hi-Z Mode is enabled.
5:0	—	Reserved

7.9.9 Detect Status 2

Address 0x1B78

R/O	7	6	5	4	3	2	1	0
	—						HS_TRUE	SHORT_TRUE
Default	x	x	x	x	0	x	x	x

Bits	Name	Description
7:2	—	Reserved
1	HS_TRUE	HS true. Reports whether voltage detected on HSBIAS_IN drops below the HS_DETECT_LEVEL threshold. 0 False. HSBIAS_IN is above the specified threshold. 1 True. HSBIAS_IN is below the specified threshold.
0	SHORT_TRUE	Short true. Reports whether the voltage detected on HSBIAS_IN is below the S0 threshold. Valid only if DETECT_MODE = Normal Mode. Table 3-20 specified the threshold as “Short-Detect Threshold (S0 Button).” DEBOUNCE_TIME does not affect this bit, because its source is not debounced. 0 False. HSBIAS_IN is above the S0 threshold 1 True. HSBIAS_IN is below the S0 threshold

7.9.10 Detect Interrupt Mask 1

Address 0x1B79

R/W	7	6	5	4	3	2	1	0
	M_HSBIAS_SENSE	M_TIP_SENSE_PLUG	M_TIP_SENSE_UNPLUG	—				
Default	1	1	1	0	0	0	0	0

Interrupt mask register bits serve as a mask for the interrupt sources in the interrupt status registers. Interrupts are described in Section 4.18.

Bits	Name	Description
7	M_HSBIAS_SENSE	HSBIAS_SENSE mask 0 Unmasked 1 (Default) Masked
6	M_TIP_SENSE_PLUG	TIP_SENSE_PLUG mask 0 Unmasked 1 (Default) Masked
5	M_TIP_SENSE_UNPLUG	TIP_SENSE_UNPLUG mask 0 Unmasked 1 (Default) Masked
4:0	—	Reserved

7.9.11 Detect Interrupt Mask 2

Address 0x1B7A

R/W	7	6	5	4	3	2	1	0
	M_DETECT_TRUE_FALSE	M_DETECT_FALSE_TRUE	—			M_HSBIAS_HIZ	M_SHORT_RELEASE	M_SHORT_DETECTED
Default	1	1	1	1	1	1	1	1

Interrupt mask register bits serve as a mask for the interrupt sources in the interrupt status registers. Interrupts are described in Section 4.18.

Bits	Name	Description
7	M_DETECT_TRUE_FALSE	DETECT_TRUE_FALSE mask 0 Unmasked 1 (Default) Masked
6	M_DETECT_FALSE_TRUE	DETECT_FALSE_TRUE mask 0 Unmasked 1 (Default) Masked
5:2	—	Reserved
2	M_HSBIAS_HIZ	HSBIAS_HIZ mask 0 Unmasked 1 (Default) Masked
1	M_SHORT_RELEASE	SHORT_RELEASE mask. A shadow register for this bit captures up to two button-press events. Reading the register once transfers the contents of the shadow register into this one; therefore, it can be read twice per interrupt event. Shadow bits are not available in Wake Mode (only VP present). 0 Unmasked 1 (Default) Masked
0	M_SHORT_DETECTED	SHORT_DETECTED mask. This bit is affected by LATCH_TO_VP (see p. 151). 0 Unmasked 1 (Default) Masked

7.10 Headset Bias Registers

7.10.1 Headset Bias Control

Address 0x1C03

R/W	7	6	5	4	3	2	1	0
	HSBIAS_CAPLESS_EN	—		HSBIAS_PD	—		HSBIAS_RAMP	
Default	1	1	0	0	0	0	1	0

Bits	Name	Description
7	HSBIAS_CAPLESS_EN	HSBIAS capless enable. Indicates whether there is a capacitive load on HS bias output. 0 External capacitor present 1 (Default) No external capacitor (Default because there is no pin on HS bias output)
6:5	—	Reserved

Bits	Name	Description
4	HSBIAS_ PD	HSBIAS pull down. Used to enable a 60-kΩ pulldown on HS bias. 0 (Default) Pulldown resistor off 1 Pulldown resistor on
3:2	—	Reserved
1:0	HSBIAS_ RAMP	HSBIAS ramp rate. Sets bidirectional output ramp rate between ground and set level. See Table 3-15 for specifications. **Note:** After setting HSBIAS_RAMP and powering up the mic bias HSBIAS_CTRL (see p. 151), HSBIAS_RAMP cannot be changed until the ramp delay count is reached. Approximate ramp delay counts for HS_BIAS_RAMP = 00/01/10/11 are, respectively, 10/40/90/170 ms. After the ramp delay count, HS_TRUE and SHORT_TRUE (see p. 152) become valid. 00 Fast rise time; slow, load-dependent fall time. 01 Fast 10 (Default) Slow 11 Slowest

7.11 ADC Registers

7.11.1 ADC Control

Address 0x1D01

R/W	7	6	5	4	3	2	1	0
	—		ADC_NOTCH_ DIS	ADC_FORCE_ WEAK_VCM	—	ADC_INV	—	ADC_DIG_ BOOST
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
5	ADC_ NOTCH_ DIS	ADC digital notch filter disable. Disables the digital notch filter on the ADC. 0 (Default) Enabled 1 Disabled
4	ADC_ FORCE_ WEAK_VCM	ADC force analog input weak VCM. Controls the status of the weak VCM for the analog input. 0 (Default) Normal operation 1 Forced on
3	—	Reserved
2	ADC_INV	ADC invert signal polarity. Configures the polarity of the ADC signal. See Section 4.13.1 for details. 0 (Default) Not inverted 1 Inverted
3	—	Reserved
0	ADC_DIG_ BOOST	ADC digital boost. Configures a +20-dB digital boost on the ADC. See Section 4.1.3 for details. 0 (Default) No boost applied 1 +20-dB digital boost applied

7.11.2 ADC Soft-Ramp Enable

Address 0x1D02

R/W	7	6	5	4	3	2	1	0
	—					ADC_ SOFTRAMP_EN	—	
Default	0	0	0	0	0	0	1	0

Bits	Name	Description
7:3	—	Reserved
2	ADC_ SOFTRAMP_ EN	ADC soft-ramp enable. Digital soft ramp enable bit for ADC. 0 (Default) Disabled 1 Enabled. The soft-ramp rate is set by DSR_RATE
1:0	—	Reserved

7.11.3 ADC Volume

Address 0x1D03

R/W	7	6	5	4	3	2	1	0
	ADC_VOL							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	ADC_ VOL	ADC volume. ADC digital volume. Sets the ADC signal volume. Step size: 1.0 dB 0111 1111–0000 1100 +12 dB 0000 1011 +11 dB … 0000 0000 (Default) 0 dB 1111 1111 –1.0 dB 1111 1110 –2.0 dB … 1010 0000 –96.0 dB 1001 1111–1000 0000 Mute

7.11.4 ADC Wind-Noise Filter and HPF

Address 0x1D04

R/W	7	6	5	4	3	2	1	0
		ADC_WNF_CF			ADC_WNF_EN	ADC_HPF_CF		ADC_HPF_EN
Default	0	1	1	1	0	0	0	1

Bits	Name	Description
7	—	Reserved
6:4	ADC_ WNF_CF	ADC wind-noise filter select. Sets the corner frequency for the wind-noise filter. See Section 4.1.2 for details. 000–111 (Default = 111). See Table 3-11.
3	ADC_ WNF_EN	Enable ADC wind-noise filter. See Section 4.1.2 for details. 0 (Default) Wind-noise filter disabled and bypassed. 1 Enabled
2:1	ADC_ HPF_CF	HS ADC HPF corner frequency. Sets the corner frequency (–3 dB point) for the internal HPF. See Section 4.1 for details. Increasing the HPF corner frequency past the default setting can introduce up to ~0.3 dB of gain error in the passband. 00 (Default) $3.88 \times 10^{-5} \times Fs_{INT}$ (1.86 Hz at Fs_{INT} = 48 kHz) 10 $4.9 \times 10^{-3} \times Fs_{INT}$ (235 Hz at Fs_{INT} = 48 kHz) 01 $2.5 \times 10^{-3} \times Fs_{INT}$ (120 Hz at Fs_{INT} = 48 kHz) 11 $9.7 \times 10^{-3} \times Fs_{INT}$ (466 Hz at Fs_{INT} = 48 kHz)
0	ADC_ HPF_EN	HS ADC HPF enable. Configures the internal HPF after the HS ADC. Change only if the ADC is in a powered down state. See Section 4.1 for details. ADC_HPF_EN must remain asserted for proper functionality. Failure to do so may cause clipping of the ADC digital output. 0 Disabled. This must be cleared only for test purposes. 1 (Default) Enabled

7.12 DAC Control Registers

7.12.1 DAC Control 1

Address 0x1F01

R/W	7	6	5	4	3	2	1	0
	—						DACB_INV	DACA_INV
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:2	—	Reserved
1:0	DACx_INV	DACx invert signal polarity. Configures the polarity of the DAC channel x signal. See Section 4.4 for details. 0 (Default) Not inverted 1 Inverted

7.12.2 DAC Control 2

Address 0x1F06

R/W	7	6	5	4	3	2	1	0
	HPOUT_PULLDOWN				HPOUT_LOAD	HPOUT_CLAMP	DAC_HPF_EN	—
Default	0	0	0	0	0	0	1	0

Bits	Name	Description
7:4	HPOUT_ PULLDOWN	Although bits 2:0 are independent, the final resistance from the resistor string is dictated by the lowest resistance chosen; e.g., if HPOUT_PULLDOWN = 1011, a nominal 6-kΩ pull-down resistance results even if 9.6-kΩ resistance is also selected. 0000 (Default) 0.9 kΩ 1000 No pulldown 1010 5.8 kΩ 1100 0.9 kΩ 0001–0111 0.9 kΩ 1001 9.3 kΩ 1011 Reserved 1101–1111 Reserved
3	HPOUT_ LOAD	HP output load. Sets HP amplifier capacitive load capability. Table 3-13 gives output specifications. See Section 4.4 for details. 0 (Default) 1 nF Mode 1 10 nF Mode **Note:** The HP path must be powered down before reconfiguring this bit and repowered afterwards. See Section 4.4.4.
2	HPOUT_ CLAMP	HPOUT clamp. Configures an override of the HPOUT clamp to ground when the channels are powered down. 0 (Default) Clamp to ground when channels are powered down. 1 Clamp is disabled when the channels are powered down. The pulldown to GNDA depends on the HPOUT_ PULLDOWN setting.
1	DAC_HPF_ EN	DAC high-pass filter enable. Configures the internal HPF before DAC. Changes to this bit must be made only if PDN_ ALL = 1. See Section 4.4 for details. 0 Disabled. This must be cleared only for test purposes. 1 (Default) Enabled. The corner frequency is set to 0.935 Hz when Fs_{INT} = 48 kHz.
0	—	Reserved

7.13 HP Control Register

7.13.1 HP Control

Address 0x2001

R/W	7	6	5	4	3	2	1	0
	—				ANA_MUTE_B	ANA_MUTE_A	FULL_SCALE_VOL	—
Default	0	0	0	0	1	1	0	1

Bits	Name	Description
7:4	—	Reserved
3	ANA_MUTE_B	Analog mute Channel B. See Section 4.4 for details. 0 Unmuted 1 (Default) Muted
2	ANA_MUTE_A	Analog mute Channel A. See Section 4.4 for details. 0 Unmuted 1 (Default) Muted
1	FULL_SCALE_VOL	Full-scale volume. Determines the maximum volume for the headphone output. See Section 4.4 for details. 0 (Default) 0 dB 1 –6 dB. This setting is recommended if the load is approximately 15 Ω.
0	—	Reserved

7.14 Class H Register

7.14.1 Class H Control

Address 0x2101

R/W	7	6	5	4	3	2	1	0
	—					ADPTPWR		
Default	0	0	0	0	0	1	1	1

Bits	Name	Description
7:3	—	Reserved
2:0	ADPTPWR	Adaptive power adjustment. Configures how power to HP output amplifiers adapts to the output signal level. Section 4.4 gives detailed descriptions of supported settings. 000 Reserved 001 Fixed, Mode 0—VP_CP Mode (±2.5V) 010 Fixed, Mode 1—VCP Mode (±VCP) 011 Fixed, Mode 2 —VCP/2 Mode (±VCP/2) 100 Fixed, Mode 3 —VCP/3 Mode (±VCP/3) 101–110 Reserved 111 (Default) Adapt to signal. The output signal dynamically determines the voltage level.

7.15 Mixer

7.15.1 Mixer Channel A Input Volume

Address 0x2301

R/W	7	6	5	4	3	2	1	0
	—		MIXER_CHA_VOL					
Default	0	0	1	1	1	1	1	1

Bits	Name	Description
7:6	—	Reserved
5:0	MIXER_CHA_VOL	Input attenuation. Sets the attenuation level to be applied to various stereo digital inputs. See Section 4.2 for details. Each input can be muted or attenuated from –62 to 0 dB in 1-dB steps. 00 0000 0 dB 00 0001 –1.0 dB … 11 1110 –62.0 dB 11 1111 (Default) Mute. If the SRC is enabled, the ASP outputs nonzero data until ASP_DAO_PDN is either toggled or set.

7.15.2 Mixer ADC Input Volume

Address 0x2302

R/W	7	6	5	4	3	2	1	0
	—		MIXER_ADC_VOL					
Default	0	0	1	1	1	1	1	1

Bits	Name	Description
7:6	—	Reserved
5:0	MIXER_ADC_VOL	Mixer input attenuation. Sets the attenuation level to be applied to various stereo digital inputs. See Section 4.2 for details. Each mixer input can be muted or attenuated from –62 to 0 dB in 1-dB steps 00 0000 0 dB 00 0001 –1.0 dB … 11 1110 –62.0 dB 11 1111 (Default) Mute. If the SRC is enabled, the ASP outputs nonzero data until ASP_DAO_PDN is either toggled or set.

7.15.3 Mixer Channel B Input Volume

Address 0x2303

R/W	7	6	5	4	3	2	1	0
	—		MIXER_CHB_VOL					
Default	0	0	1	1	1	1	1	1

Bits	Name	Description
7:6	—	Reserved
5:0	MIXER_CHB_VOL	Input attenuation. Sets the attenuation level to be applied to various stereo digital inputs. See Section 4.2 for details. Each input can be muted or attenuated from –62 to 0 dB in 1-dB steps. 00 0000 0 dB 00 0001 –1.0 dB … 11 1110 –62.0 dB 11 1111 (Default) Mute. If the SRC is enabled, the ASP outputs nonzero data until ASP_DAO_PDN is either toggled or set.

7.16 Equalizer

7.16.1 Equalizer Filter Coefficient Input 0–3

Address 0x2401–0x2404

R/W	7	6	5	4	3	2	1	0
0x2401	EQ_COEF_IN[7:0]							
0x2402	EQ_COEF_IN[15:8]							
0x2403	EQ_COEF_IN[23:16]							
0x2404	EQ_COEF_IN[31:24]							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
31:0	EQ_COEF_IN	EQ coefficient input. Data to be written to the equalizer filter coefficient pointed to by the coefficient address pointer. See Section 4.3 for programming examples. **Notes:** • With SoundWire, indirect-access procedures must be used for read/write of equalizer coefficients. • EQ_COEF_IN[31:24] always returns zeros when read. • Filters are read by using EQ_COEF_OUT (see p. 158) and written by using EQ_COEF_IN. However, they must be accessed only as part of a full-filter access procedure; otherwise, the three-band filter may be corrupted and audio artifacts may occur. • Read/write access to EQ_COEF_IN[31:24] while the equalizer block is powered down may cause an APB timeout.

7.16.2 Equalizer Filter Coefficient Read/Write

Address 0x2406

R/W	7	6	5	4	3	2	1	0
	—						EQ_WRITE	EQ_READ
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:2	—	Reserved
1	EQ_WRITE	EQ write. Enable write of the coefficients via EQ_COEF_IN. See Section 4.3 for programming examples. 0 (Default) Writes disabled. 1 Writes enabled.
0	EQ_READ	EQ read. Enable read of the coefficients via EQ_COEF_OUT. See Section 4.3 for programming examples. 0 (Default) Reads disabled. 1 Reads enabled.

7.16.3 Equalizer Filter Coefficient Output 0–3

Address 0x2407–0x240A

R/O	7	6	5	4	3	2	1	0
	EQ_COEF_OUT[7:0]							
	EQ_COEF_OUT[15:8]							
	EQ_COEF_OUT[23:16]							
	EQ_COEF_OUT[31:24]							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
31:0	EQ_COEF_OUT	EQ coefficient out. Coefficient read data from the equalizer. Data read from the equalizer filter coefficient pointed to by the coefficient address pointer. See Section 4.3 for programming examples. Filters are read by using EQ_COEF_OUT and written by using EQ_COEF_IN (see p. 157). However, they must be accessed only as part of a full-filter access procedure; otherwise, the three-band filter may be corrupted and audio artifacts may occur. **Notes:** • With SoundWire, indirect procedures must be used for read/write of equalizer coefficients. • Read/write access to EQ_COEF_OUT[7:0] while the equalizer block is powered down may cause an APB timeout. • When reading this register via the I²C bus, EQ_PDN must be cleared and EQ_READ must be set. Otherwise, reading from this register may cause the SCL to be held low, hanging the I²C bus. See the notes after Ex. 4-1 in Section 4.3.

7.16.4 Equalizer Initialization Status

Address 0x240B

R/O	7	6	5	4	3	2	1	0
	—							EQ_INIT_DONE
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:1	—	Reserved
0	EQ_INIT_DONE	Equalizer coefficient initialization done. Indicates whether initialization is complete. Section 4.3 gives programming examples. 0 (Default) Initialization is not complete. 1 Initialization complete. Coefficients may be written to the equalizer.

7.16.5 Equalizer Start Filter Control

Address 0x240C

R/W	7	6	5	4	3	2	1	0
	—							EQ_START_FILTER
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:1	—	Reserved
0	EQ_START_FILTER	Equalizer start filter. Signals whether read/write of the coefficients has completed and the equalizer can start operation. See Section 4.3 for programming examples. 0 (Default) Coefficients are being read/written. 1 The equalizer can start filtering based on current coefficients.

7.16.6 Equalizer Input Mute Control

Address 0x240E

R/W	7	6	5	4	3	2	1	0
	—							EQ_MUTE
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:1	—	Reserved
0	EQ_MUTE	Equalizer input mute. Sets the equalizer input to digital zeros with no soft ramp. See Section 4.3 for programming examples. 0 (Default) Not muted 1 Muted

7.17 AudioPort Interface Registers

7.17.1 Serial Port Receive Channel Select

Address 0x2501

R/W	7	6	5	4	3	2	1	0
	—				SP_RX_CHB_SEL		SP_RX_CHA_SEL	
Default	0	0	0	0	0	1	0	0

Bits	Name	Description
7:4	—	Reserved
3:2	SP_RX_ CHB_SEL	SP RX Channel B select for DAI0. Selects right input channel. Valid only if the SWIRE_SEL pin is deasserted.See Section 5 for programming examples. 00 Channel 0 01 (Default) Channel 1 10 Channel 2 11 Channel 3
1:0	SP_RX_ CHA_SEL	SP RX Channel A select for DAI0. Selects right input channel. Valid only if the SWIRE_SEL pin is deasserted. 00 (Default) Channel 0 01 Channel 1 10 Channel 2 11 Channel 3

7.17.2 Serial Port Receive Isochronous Control

Address 0x2502

R/W	7	6	5	4	3	2	1	0
	—	SP_RX_RSYNC	SP_RX_NSB_POS			SP_RX_NFS_NSBB	SP_RX_ISOC_MODE	
Default	0	0	0	0	0	1	0	0

Bits	Name	Description
7	—	Reserved
6	SP_RX_ RSYNC	Serial port receive synchronization. 0 (Default) Normal state 1 Recenter the FIFO. No read and writes when asserted
5:3	SP_RX_ NSB_ POS	Serial-port receive null-sample bit position. Selects the position of the null byte in the resultant 16-, 24-, or 32-bit sample. For all samples, if SP_RX_ISOC_MODE ≠ 00, SP_RX_NFS_NSBB = 0, the following applies: • For a 16-bit sample (8-bit audio + null byte), [23:16] is the null byte. • For a 24-bit sample (16-bit audio + null byte), [15:8] is the null byte. • For a 32-bit sample (24-bit audio + null byte), [7:0] is the null byte. **Note:** NSB Mode does not support 32-bit audio samples. The ASP_RXn_CHn_RES fields in Section 7.22 set the output resolution of the ASP receive channel samples. Clearing SP_RX_NSB_POS indicates that Bit 0 must be zero for the sample to be classified as a null. 000 (Default) 0 … 111 7
2	SP_RX_ NFS_ NSBB	Serial-port receive NSB/NFS Mode select. 0 NSB Mode valid only if SP_RX_ISOC_MODE ≠ 00. 1 (Default) NFS Mode
1:0	SP_RX_ ISOC_ MODE	Serial port receive isochronous mode. Selecting an isochronous mode allows for null removal. The ASP Rx rate bits (SP_RX_ FS, see p. 159) are used only to help the device determine when to insert nulls. 00 (Default) Native mode 10 96k isochronous stream 01 48k isochronous stream 11 192k isochronous stream

7.17.3 Serial Port Receive Sample Rate

Address 0x2503

R/W	7	6	5	4	3	2	1	0
	—			SP_RX_FS				
Default	1	0	0	0	1	1	0	0

Bits	Name	Description
7:5	—	Reserved
4:0	SP_ RX_ FS	SP receive sample rate. Configures the sample rate of the SRC F_{SI} when in Isochronous Mode. This setting autoscales when configuring for a isochronous rate of 96 or 192 kHz with respect to the 48-kHz isochronous rate, e.g., 24-kHz setting in isochronous rate of 48 kHz would be scaled to a 48-kHz setting in isochronous rate of 96 kHz. 0 0000 Reserved 0 0100 12.000 kHz 0 1000 24.000 kHz 0 1100 (Default) 48.000 kHz 1 0000 176.400 kHz 0 0001 8.00 kHz 0 0101 16.000 kHz 0 1001 32.000 kHz 0 1101 88.200 kHz 1 0001 176.472 kHz 0 0010 11.025 kHz 0 0110 22.050 kHz 0 1010 44.100 kHz 0 1110 88.236 kHz 1 0010 192.000 kHz 0 0011 11.0295 kHz 0 0111 22.059 kHz 0 1011 44.118 kHz 0 1111 96.000 kHz 1 0011–1 1111 Reserved

7.17.4 S/PDIF Channel Select

Address 0x2504

R/W	7	6	5	4	3	2	1	0
	—				SPDIF_CHB_SEL		SPDIF_CHA_SEL	
Default	0	0	0	0	1	1	1	0

Bits	Name	Description
7:4	—	Reserved
3:2	SPDIF_ CHB_SEL	S/PDIF Channel B select for DAI0. Selects right input channel. Valid only if the SWIRE_SEL pin is deasserted. See Section 4.10.1 for programming details. 00 Channel 0 01 Channel 1 10 Channel 2 11 (Default) Channel 3
1:0	SPDIF_ CHA_SEL	S/PDIF Channel A select for DAI0. Selects left input channel. Valid only if the SWIRE_SEL pin is deasserted. 00 Channel 0 01 Channel 1 10 (Default) Channel 2 11 Channel 3

7.17.5 Serial Port Transmit Isochronous Control

Address 0x2505

R/W	7	6	5	4	3	2	1	0
	—	SP_TX_RSYNC	SP_TX_NSB_POS			SP_TX_NFS_NSBB	SP_TX_ISOC_MODE	
Default	0	0	0	0	0	1	0	0

Bits	Name	Description
7	—	Reserved
6	SP_TX_ RSYNC	FIFO resync. Used to force the DAO FIFO into resync state, in which reads and writes are gated off. 0 Normal state (default) 1 Resync state
5:3	SP_TX_ NSB_ POS	Serial-port transmit-null-sample bit position. Selects the position of the null byte in the resultant 16-, 24-, or 32-bit sample. For all samples, if SP_TX_ISOC_MODE ≠ 00, SP_TX_NFS_NSBB = 0, the following applies: • For a 16-bit sample (8-bit audio + null byte), [23:16] is the null byte. • For a 24-bit sample (16-bit audio + null byte), [15:8] is the null byte. • For a 32-bit sample (24-bit audio + null byte), [7:0] is the null byte. **Note:** NSB Mode does not support 32-bit audio samples. The ASP_TX_CH*n*_RES fields in Section 7.21 set the output resolution of the ASP transmit channel samples. Clearing SP_TX_NSB_POS indicates that Bit 0 must be zero for the sample to be classified as a null. 000 (Default) 0 … 111 7
2	SP_TX_ NFS_ NSBB	NFS Mode select. 0 NSB Mode valid only if SP_TX_ISOC_MODE ≠ 00 1 (Default) NFS Mode
1:0	SP_TX_ ISOC_ MODE	Serial port transmit isochronous mode. Selects the mode and rate of the isochronous stream. Selecting an isochronous mode allows for null insertion. The ASP Tx rate bits (SP_TX_FS, see p. 160) are used only to help determine when to insert nulls. 00 (Default) Native mode (no null insertion) 10 96k isochronous stream 01 48k isochronous stream 11 192k isochronous stream

7.17.6 Serial Port Transmit Sample Rate

Address 0x2506

R/W	7	6	5	4	3	2	1	0
	—			SP_TX_FS				
Default	1	1	0	0	1	1	0	0

Bits	Name	Description
7:5	—	Reserved
4:0	SP_TX_ FS	SP transmit sample rate. Configures the sample rate of the SRC F_{SO} when in Isochronous Mode. This setting autoscales when configuring for a isochronous rate of 96 or 192 kHz with respect to the 48-kHz isochronous rate. Ex: 24-kHz setting in isochronous rate of 48 kHz would be scaled to a 48-kHz setting in isochronous rate of 96 kHz. 0 0000 Reserved 0 0100 12.000 kHz 0 1000 24.000 kHz 0 1100 (Default) 48.000 kHz 1 0000 176.400 kHz 0 0001 8.00 kHz 0 0101 16.000 kHz 0 1001 32.000 kHz 0 1101 88.200 kHz 1 0001 176.472 kHz 0 0010 11.025 kHz 0 0110 22.050 kHz 0 1010 44.100 kHz 0 1110 88.236 kHz 1 0010 192.000 kHz 0 0011 11.0295 kHz 0 0111 22.059 kHz 0 1011 44.118 kHz 0 1111 96.000 kHz 1 0011–1 1111 Reserved

7.17.7 S/PDIF/SoundWire Control 1

Address 0x2507

R/W	7	6	5	4	3	2	1	0
	—		SPDIF_RES		SW_RES_INPUT		SW_RES_OUTPUT	
Default	0	0	1	1	1	1	1	1

Bits	Name	Description
7:6	—	Reserved
5:4	SPDIF_RES	S/PDIF channel resolution. See Section 4.10.1 for programming details. 00 20 bits 01 16 bits 10 24 bits 11 (Default) 32 bits
3:2	SW_RES_INPUT	ADC channel resolution when using SoundWire. 00 8 bits 01 16 bits 10 24 bits 11 (Default) 32 bits
1:0	SW_RES_OUTPUT	DAC channel resolution when using SoundWire. 00 20 bits 01 16 bits 10 24 bits 11 (Default) 32 bits

7.18 SRC Registers

7.18.1 SRC Input Sample Rate

Address 0x2601

R/W	7	6	5	4	3	2	1	0
	—			SRC_SDIN_FS				
Default	0	1	0	0	0	0	0	0

Bits	Name	Description
7:5	—	Reserved
4:0	SRC_SDIN_FS	SRC input sample rate. Must equal Fs_{INT} if SRC_BYPASS_DAC = 1. 0 0000 (Default) Don't know 0 0100 12.000 kHz 0 1000 24.000 kHz 0 1100 48.000 kHz 1 0000 176.400 kHz 0 0001 8.00 kHz 0 0101 16.000 kHz 0 1001 32.000 kHz 0 1101 88.200 kHz 1 0001 176.472 kHz 0 0010 11.025 kHz 0 0110 22.050 kHz 0 1010 44.100 kHz 0 1110 88.236 kHz 1 0010 192.000 kHz 0 0011 11.0295 kHz 0 0111 22.059 kHz 0 1011 44.118 kHz 0 1111 96.000 kHz 1 0011–1 1111 Reserved

7.18.2 SRC Output Sample Rate

Address 0x2609

R/W	7	6	5	4	3	2	1	0
	—			SRC_SDOUT_FS				
Default	0	1	0	0	0	0	0	0

Bits	Name	Description
7:5	—	Reserved
4:0	SRC_SDOUT_FS	SRC audio output sample rate. Must equal Fs_{INT} if SRC_BYPASS_ADC = 1. 0 0000 (Default) Don't know 0 0100 12.000 kHz 0 1000 24.000 kHz 0 1100 48.000 kHz 1 0000 176.400 kHz 0 0001 8.00 kHz 0 0101 16.000 kHz 0 1001 32.000 kHz 0 1101 88.200 kHz 1 0001 176.472 kHz 0 0010 11.025 kHz 0 0110 22.050 kHz 0 1010 44.100 kHz 0 1110 88.236 kHz 1 0010 192.000 kHz 0 0011 11.0295 kHz 0 0111 22.059 kHz 0 1011 44.118 kHz 0 1111 96.000 kHz 1 0011–1 1111 Reserved

7.19 DMA Registers

7.19.1 Soft Reset Reboot

Address 0x2701

R/W	7	6	5	4	3	2	1	0
	—						SFT_RST_REBOOT	—
Default	0	0	0	1	1	1	0	0

Bits	Name	Description
7:2	—	Reserved
1	SFT_RST_REBOOT	Software reset reboot 0 (Default) Not initiated 1 Forces an internal configuration reboot to occur after a SoundWire reset. Reinitializes internal settings of the device. This must be done if a SoundWire reset has occurred. See Table 4-29.
0	—	Reserved

7.20 S/PDIF

7.20.1 S/PDIF Control 1

Address 0x2801

R/W	7	6	5	4	3	2	1	0
	—					SPDIF_TX_RAW	SPDIF_TX_KAE	SPDIF_TX_PDN
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7:3	—	Reserved
2	SPDIF_ TX_RAW	S/PDIF transmit raw. Used to pass 32-bit raw (software-formatted) data from the DAI port to the S/PDIF output. The control bit's information (see Section 7.20.2) is not added to the stream. **Note:** The DAI input channels must be set to 32-bit width (ASP_RX0_CH1_RES, see p. 166, where RX0 Channels 1–4 and RX1 Channels 1 and 2 are configured) along with SPDIF_RES (see p. 161). 0 (Default) S/PDIF outputs up to 24 bits of data along with the control information from the S/PDIF Control 2 register. 1 S/PDIF outputs 32-bit raw (software-formatted) data.
1	SPDIF_ TX_KAE	S/PDIF keep alive. Transmit state depends on the SPDIF_TX_DIGEN and SPDIF_TX_PDN settings. See Table 4-20. **Note:** The value of this field has no function on the CS42L42.
0	SPDIF_ TX_PDN	S/PDIF TX power-down. 0 Transmit state depends on the SPDIF_TX_DIGEN and SPDIF_TX_PDN settings. See Table 4-20. 1 (Default) Powers down the S/PDIF TX circuitry. See Table 4-20.

7.20.2 S/PDIF Control 2

Address 0x2802

R/W	7	6	5	4	3	2	1	0
	SPDIF_TX_L	SPDIF_TX_PRO	SPDIF_TX_AUDIOB	SPDIF_TX_CP	SPDIF_TX_PRE	SPDIF_TX_VCFG	SPDIF_TX_V	SPDIF_TX_DIGEN
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7	SPDIF_ TX_L	S/PDIF transmit generation-level bit. Indicates the generation of audio material. 0 (Default) This data stream is a copy. A data stream cannot be copied from this copied stream. 1 The digital audio stream comes from the original and not from a copy.
6	SPDIF_ TX_ PRO	S/PDIF transmit signal format select. See *IEC60958-3 Digital Audio Interface—Consumer* for details. 0 (Default) Consumer format. Affects operation of SPDIF_TX_CP (Bit 4). 1 Professional audio
5	SPDIF_ TX_ AUDIOB	S/PDIF transmit audio/nonaudio. Indicates whether data is audio data. 0 (Default) PCM format 1 Non-PCM format
4	SPDIF_ TX_CP	S/PDIF transmit copy permit. Applicable only if SPDIF_TX_PRO = 0 (Bit 6, Consumer Mode) 0 (Default) Copy inhibited 1 Copy permitted
3	SPDIF_ TX_PRE	S/PDIF transmit filter preemphasis. 0 (Default) No preemphasis 1 Filter preemphasis 50/15 µs
2	SPDIF_ TX_ VCFG	VCFG (validity configuration). Determines S/PDIF transmitter behavior in conjunction with SPDIF_TX_V when audio data is transmitted. When asserted, this bit forces the deassertion of the S/PDIF validity flag (V), which is bit 28 transmitted in each S/PDIF subframe. The validity bit (V, bit 28) is Logic 0 if the audio sample word is suitable for conversion to an analog audio signal and is logic "1" if it is not. The SPDIF_TX_V description below describes interactions between the two bits.

<table>
<tr><th>Bits</th><th>Name</th><th>Description</th></tr>
<tr><td>1</td><td>SPDIF_TX_V</td><td>Validity. Affects the validity flag (V) bit 28, transmitted in each subframe in conjunction with the SPDIF_TX_VCFG setting.
0 (default) enables the S/PDIF transmitter to maintain connection during error or mute conditions.
1 The V bit in the subframe is always set to indicate invalid data
<table>
<tr><th>SPDIF_TX_VCFG</th><th>SPDIF_TX_V</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>(Default) For each S/PDIF subframe (left and right), the validity flag reflects whether an internal codec error occurred (i.e., whether the S/PDIF interface received and transmitted a valid sample).
If a valid sample (left or right) is received and successfully transmitted, the V bit is cleared for that subframe. Otherwise, the V bit for that subframe must be transmitted as 1.</td></tr>
<tr><td>1</td><td>0</td><td>For each S/PDIF subframe (left and right), the V bit reflects whether an internal codec transmission error occurred (i.e., an internal codec error should set the V bit).
• If a valid sample (left or right) is received and successfully transmitted, the V bit is cleared for that subframe.
• If the S/PDIF transmitter is not receiving a sample, the S/PDIF transmitter must set the V bit and pad each S/PDIF audio sample word in question with zeros for the corresponding subframe.</td></tr>
<tr><td>0</td><td>1</td><td>Each S/PDIF subframe (left and right) is sent with the V bit set. This tags all S/PDIF subframes as invalid.</td></tr>
<tr><td>1</td><td>1</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>0</td><td>SPDIF_TX_DIGEN</td><td>S/PDIF transmit enable. Determines whether data can be driven onto the S/PDIF output.
0 (Default) Data cannot be driven onto the S/PDIF output. See Table 4-20.
1 Data can be driven onto the S/PDIF output. See Table 4-20.</td></tr>
</table>

7.20.3 S/PDIF Control 3

Address 0x2803

R/W	7	6	5	4	3	2	1	0
	—	SPDIF_TX_CC						
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7	—	Reserved
6:0	SPDIF_TX_CC	S/PDIF transmit category code. Program according to the IEC60958-3 specification. 000 0000 (Default)

7.20.4 S/PDIF Control 4

Address 0x2804

R/W	7	6	5	4	3	2	1	0
	—					SPDIF_TX_STAT		
Default	0	1	0	0	0	0	1	0

Bits	Name	Description
7:3	—	Reserved
2:0	SPDIF_TX_STAT	S/PDIF transmit state. Configures the supported S/PDIF rate. See Section 4.10.1 for details. 000 32 kHz 001 44.1 kHz 010 (Default) 48 kHz 011 88.2 kHz 100 96 kHz 101 176.4 kHz 110 192 kHz 111 Reserved

7.21 Serial Port Register Transmit Registers

7.21.1 ASP Transmit Size and Enable

Address 0x2901

R/W	7	6	5	4	3	2	1	0
	—						ASP_TX_2FS	ASP_TX_EN
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:2	—	Reserved
1	ASP_TX_2FS	ASP channel data requests per frame. Used to configure the TX into Fs or 2Fs Mode. 0 (Default) Fs Mode 1 2Fs Mode (doubles the incoming LRCK rate)
0	ASP_TX_EN	ASP TDM TX channel output enable. Configures the electrical state of the channel output phase determined by ASP_TX_CHx_RES. 0 (Default) Not enabled (Hi-Z) 1 Enabled (driven)

7.21.2 ASP Transmit Channel Enable

Address 0x2902

R/W	7	6	5	4	3	2	1	0
	—						ASP_TX_CH2_EN	ASP_TX_CH1_EN
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:2	—	Reserved
1	ASP_TX_CH2_EN	ASP Transmit Channel 2 enable. Although two output channels exist, data from Channel 1 is replicated onto Channel 2 if ASP_TX_CH2_EN is set. As a result, Channel 2 can be used only if Channel 1 is used. This is targeted for 50/50 use, but can be used in any transmit situation with the stipulation that bit resolution must be the same for Channels 1 and 0 (ASP_TX_CH2_RES = ASP_TX_CH1_RES), along with matching MSB/LSB bit starts (ASP_TX_CH2_BIT_ST_MSB = ASP_TX_CH1_BIT_ST_MSB and ASP_TX_CH2_BIT_ST_LSB = ASP_TX_ CH1_BIT_ST_LSB). However, the active phase for each channel must be different if using 50/50 Mode (ASP_ TX_CH2_AP ≠ ASP_TX_CH1_AP). See Section 4.9 for details. 0 (Default) Disabled 1 Enabled
0	ASP_TX_CH1_EN	ASP transmit Channel 1 enable. See Section 4.9 for details. 0 (Default) Disabled 1 Enabled

7.21.3 ASP Transmit Channel Phase and Resolution

Address 0x2903

R/W	7	6	5	4	3	2	1	0
	ASP_TX_CH1_AP	ASP_TX_CH2_AP	—		ASP_TX_CH2_RES		ASP_TX_CH1_RES	
Default	0	0	0	0	1	1	1	1

Bits	Name	Description
7 6	ASP_TX_CHx_AP	ASP transmit active phase. Valid only in 50/50 Mode (ASP_5050 = 1 and ASP_TX_2FS = 0). 0 (Default) Low. In 50/50 Mode, channel data is valid if LRCK/FSYNC is low. 1 High. In 50/50 Mode, channel data is valid when LRCK/FSYNC is high.
5:4	—	Reserved
3:2 1:0	ASP_TX_CH2_RES ASP_TX_CH1_RES	ASP TX channel x bit width. Sets the output resolution of the ASP TX channel x samples. 00 8 bits per sample (valid only for isochronous NFS and native mode) 01 16 bits per sample 10 24 bits per sample 11 (Default) 32 bits per sample

7.21.4 ASP Transmit Channel 1 Bit Start MSB

Address 0x2904

R/W	7	6	5	4	3	2	1	0
	—							ASP_TX_CH1_BIT_ST_MSB
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:1	—	Reserved
0	ASP_TX_BIT_CH1_ST_MSB	ASP transmit bit Channel 1 start MSB. Configures the MSB location of the channel with respect to SOF (LRCK edge + phase lag).

7.21.5 ASP Transmit Channel 1 Bit Start LSB

Address 0x2905

R/W	7	6	5	4	3	2	1	0
	ASP_TX_CH1_BIT_ST_LSB							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	ASP_TX_BIT_CH1_ST_LSB	ASP transmit Channel 1 bit start LSB. Configures the LSB location of the channel with respect to SOF (LRCK edge + phase lag).

7.21.6 ASP Transmit Hi-Z and Delay Configuration

Address 0x2906

R/W	7	6	5	4	3	2	1	0
	—		ASP_TX_DRV_Z		ASP_TX_HIZ_DLY		—	
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	—	Reserved
5:4	ASP_TX_ DRV_Z	ASP transmit drive to Hi-Z. SDA value for unselected bits. 00 (Default) Hi-Z 01 Reserved 10 Low 11 High
3:2	ASP_TX_HIZ_ DLY	ASP transmit drive to Hi-Z delay. Nominal additional delay to release of bit drive to Hi-Z from sample edge. 00 (Default) 0 ns 01 ~8 ns 10 ~16 ns 11 Reserved
1:0	—	Reserved

7.21.7 ASP Transmit Channel 2 Bit Start MSB

Address 0x290A

R/W	7	6	5	4	3	2	1	0
	—							ASP_TX_CH2_BIT_ST_MSB
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:1	—	Reserved
0	ASP_TX_BIT_ CH2_ST_MSB	ASP transmit Channel 2 bit start MSB. Configures the MSB location of the channel with respect to SOF (LRCK edge + phase lag).

7.21.8 ASP Transmit Channel 2 Bit Start LSB

Address 0x290B

R/W	7	6	5	4	3	2	1	0
	ASP_TX_CH2_BIT_ST_LSB							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	ASP_TX_BIT_ CH2_ST_LSB	ASP transmit Channel 2 bit start LSB. Configures the LSB location of the channel with respect to SOF (LRCK edge + phase lag).

7.22 Serial Port Receive Registers

7.22.1 ASP Receive Enable

Address 0x2A01

R/W	7	6	5	4	3	2	1	0
	ASP_RX1_CH_EN		ASP_RX0_CH_EN				ASP_RX1_2FS	ASP_RX0_2FS
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:6	ASP_ RX1_ CH_EN	ASP receive DAI1 enable. Determines whether the channel buffer receives data. ASP_RX1_CH_EN[0] = Channel 1 and ASP_ RX1_CH_EN[1] = Channel 2 **Note:** Enabling is needed only when using S/PDIF in 2Fs Mode and playback in Fs Mode. 0 (Default) The corresponding channel buffer is disabled. 1 The corresponding channel buffer receives data.
5:2	ASP_ RX0_ CH_EN	ASP receive DAI0 enable. Determines whether the channel buffer gets populated. ASP_RX0_CH_EN[0] = Channel 1 ASP_RX0_CH_EN[2] = Channel 3 ASP_RX0_CH_EN[1] = Channel 2 ASP_RX0_CH_EN[3] = Channel 4 0 (Default) The corresponding channel buffer does not get populated. 1 The corresponding channel buffer is populated
1	ASP_ RX1_ 2FS	ASP receive DAI1 double-rate mode. 0 (Default) Standard sample rate, Fs (not doubled) 1 Sample rate is doubled, 2 Fs
0	ASP_ RX0_ 2FS	ASP receive DAI0 double-rate mode. 0 (Default) Standard sample rate, Fs (not doubled) 1 Sample rate is doubled, 2 Fs

7.22.2 ASP Receive DAI0 Channel 1 Phase and Resolution

Address 0x2A02

R/W	7	6	5	4	3	2	1	0
	—	ASP_RX0_CH1_AP	—				ASP_RX0_CH1_RES	
Default	0	0	0	0	0	0	1	1

Bits	Name	Description
7	—	Reserved
6	ASP_RX0_CH1_AP	ASP receive DAI0 active phase. Valid only in 50/50 Mode (ASP_5050 = 1 and ASP_RXx_2FS = 0). 0 (Default) Low. In 50/50 Mode, channel data is valid if LRCK/FSYNC is low. 1 High. In 50/50 Mode, channel data is valid when LRCK/FSYNC is high.
5:2	—	Reserved
1:0	ASP_RX0_CH1_RES	ASP Receive DAI0 channel bit width. Sets output resolution of the ASP receive DAI0 channel x samples. 00 8 bits per sample (only for isochronous NFS and native modes) 01 16 bits per sample 10 24 bits per sample 11 (Default) 32 bits per sample

7.22.3 ASP Receive DAI0 Channel 1 Bit Start MSB

Address 0x2A03

R/W	7	6	5	4	3	2	1	0
	—							ASP_RX0_CH1_BIT_ST_MSB
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:1	—	Reserved
0	ASP_RX0_CH1_BIT_ST_MSB	ASP receive DAI0 Channel 1 bit start MSB. Configures the MSB location of the channel with respect to SOF (LRCK edge + phase lag)

7.22.4 ASP Receive DAI0 Channel 1 Bit Start LSB

Address 0x2A04

R/W	7	6	5	4	3	2	1	0
	ASP_RX0_CH1_BIT_ST_LSB							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	ASP_RX0_CH1_BIT_ST_LSB	ASP receive DAI0 Channel 1 bit start LSB. Configures the LSB location of the channel with respect to SOF (LRCK edge + phase lag)

7.22.5 ASP Receive DAI0 Channel 2 Phase and Resolution

Address 0x2A05

R/W	7	6	5	4	3	2	1	0
	—	ASP_RX0_CH2_AP	—				ASP_RX0_CH2_RES	
Default	0	0	0	0	0	0	1	1

Bits	Name	Description
7	—	Reserved
6	ASP_RX0_CH2_AP	ASP receive DAI0 active phase. Valid only in 50/50 Mode (ASP_5050 = 1 and ASP_RXx_2FS = 0). 0 (Default) Low. In 50/50 Mode, channel data is input when LRCK/FSYNC is low. 1 High. In 50/50 Mode, channel data is input when LRCK/FSYNC is high.
5:2	—	Reserved
1:0	ASP_RX0_CH2_RES	ASP receive DAI0 channel bit width. Sets the output resolution of the ASP receive DAI0 channel x samples. 00 8 bits per sample (valid only for isochronous NFS and native mode) 01 16 bits per sample 10 24 bits per sample 11 (Default) 32 bits per sample

7.22.6 ASP Receive DAI0 Channel 2 Bit Start MSB

Address 0x2A06

R/W	7	6	5	4	3	2	1	0
	—							ASP_RX0_CH2_BIT_ST_MSB
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:1	—	Reserved
0	ASP_RX0_CH2_BIT_ST_MSB	ASP receive DAI0 Channel 2 bit start MSB. Configures the MSB location of the channel with respect to SOF (LRCK edge + phase lag).

7.22.7 ASP Receive DAI0 Channel 2 Bit Start LSB

Address 0x2A07

R/W	7	6	5	4	3	2	1	0
	ASP_RX0_CH2_BIT_ST_LSB							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	ASP_RX0_CH2_ BIT_ST_LSB	ASP receive DAI0 Channel 2 bit start LSB. Configures the LSB location of the channel with respect to SOF (LRCK edge + phase lag).

7.22.8 ASP Receive DAI0 Channel 3 Phase and Resolution

Address 0x2A08

R/W	7	6	5	4	3	2	1	0
	—	ASP_RX0_CH3_AP	—				ASP_RX0_CH3_RES	
Default	0	0	0	0	0	0	1	1

Bits	Name	Description
7	—	Reserved
6	ASP_ RX0_ CH3_AP	ASP receive DAI0 active phase. Valid only in 50/50 Mode (ASP_5050 = 1 and ASP_RXx_2FS = 0). 0 (Default) Low. In 50/50 Mode, channel data is input when LRCK/FSYNC is low. 1 High. In 50/50 Mode, channel data is input when LRCK/FSYNC is high.
5:2	—	Reserved
1:0	ASP_ RX0_ CH3_RES	ASP receive DAI0 channel bit width. Sets the output resolution of the ASP receive DAI0 channel x samples. 00 8 bits per sample (valid only for isochronous NFS and native mode) 01 16 bits per sample 10 24 bits per sample 11 (Default) 32 bits per sample

7.22.9 ASP Receive DAI0 Channel 3 Bit Start MSB

Address 0x2A09

R/W	7	6	5	4	3	2	1	0
	—							ASP_RX0_CH3_BIT_ST_MSB
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:1	—	Reserved
0	ASP_RX0_CH3_ BIT_ST_MSB	ASP receive DAI0 Channel 3 bit start MSB. Configures the MSB location of the channel with respect to SOF (LRCK edge + phase lag)

7.22.10 ASP Receive DAI0 Channel 3 Bit Start LSB

Address 0x2A0A

R/W	7	6	5	4	3	2	1	0
	ASP_RX0_CH3_BIT_ST_LSB							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	ASP_RX0_CH3_ BIT_ST_LSB	ASP receive DAI0 Channel 3 bit start LSB. Configures the LSB location of the channel with respect to SOF (LRCK edge + phase lag)

7.22.11 ASP Receive DAI0 Channel 4 Phase and Resolution

Address 0x2A0B

R/W	7	6	5	4	3	2	1	0
	—	ASP_RX0_CH4_AP	—				ASP_RX0_CH4_RES	
Default	0	0	0	0	0	0	1	1

Bits	Name	Description
7	—	Reserved
6	ASP_ RX0_ CH4_AP	ASP receive DAI0 active phase. Valid only in 50/50 Mode (ASP_5050 = 1 and ASP_RXx_2FS = 0). 0 (Default) Low. In 50/50 Mode, channel data is input when LRCK/FSYNC is low. 1 High. In 50/50 Mode, channel data is input when LRCK/FSYNC is high.
5:2	—	Reserved
1:0	ASP_ RX0_ CH4_RES	ASP receive DAI0 channel bit width. Sets the output resolution of the ASP receive DAI1 channel x samples. 00 8 bits per sample (valid only for isochronous NFS and native mode) 01 16 bits per sample 10 24 bits per sample 11 (Default) 32 bits per sample

7.22.12 ASP Receive DAI0 Channel 4 Bit Start MSB

Address 0x2A0C

R/W	7	6	5	4	3	2	1	0
	—							ASP_RX0_CH4_BIT_ST_MSB
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:1	—	Reserved
0	ASP_RX0_CH4_ BIT_ST_MSB	ASP receive DAI0 Channel 4 bit start MSB. Configures the MSB location of the channel with respect to SOF (LRCK edge + phase lag)

7.22.13 ASP Receive DAI0 Channel 4 Bit Start LSB

Address 0x2A0D

R/W	7	6	5	4	3	2	1	0
	ASP_RX0_CH4_BIT_ST_LSB							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	ASP_RX0_CH4_ BIT_ST_LSB	ASP receive DAI0 Channel 4 bit start LSB. Configures the LSB location of the channel with respect to SOF (LRCK edge + phase lag)

7.22.14 ASP Receive DAI1 Channel 1 Phase and Resolution

Address 0x2A0E

R/W	7	6	5	4	3	2	1	0
	—	ASP_RX1_CH1_AP	—				ASP_RX1_CH1_RES	
Default	0	0	0	0	0	0	1	1

Bits	Name	Description
7	—	Reserved
6	ASP_ RX1_ CH1_AP	ASP receive DAI1 active phase. Valid only in 50/50 Mode (ASP_5050 = 1 and ASP_RXx_2FS = 0). 0 (Default) Low. In 50/50 Mode, channel data is input when LRCK/FSYNC is low. 1 High. In 50/50 Mode, channel data is input when LRCK/FSYNC is high.
5:2	—	Reserved
1:0	ASP_ RX1_ CH1_RES	ASP receive DAI1 channel bit width. Sets the output resolution of the ASP receive DAI1 channel x samples. 00 8 bits per sample (valid only for isochronous NFS and native mode) 01 16 bits per sample 10 24 bits per sample 11 (Default) 32 bits per sample

7.22.15 ASP Receive DAI1 Channel 1 Bit Start MSB

Address 0x2A0F

R/W	7	6	5	4	3	2	1	0
	—							ASP_RX1_CH1_BIT_ST_MSB
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:1	—	Reserved
0	ASP_RX1_CH1_ BIT_ST_MSB	ASP receive DAI1 Channel 1 bit start MSB. Configures the MSB location of the channel with respect to SOF (LRCK edge + phase lag)

7.22.16 ASP Receive DAI1 Channel 1 Bit Start LSB

Address 0x2A10

R/W	7	6	5	4	3	2	1	0
	ASP_RX1_CH1_BIT_ST_LSB							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	ASP_RX1_CH1_ BIT_ST_LSB	ASP receive DAI1 Channel 1 bit start LSB. Configures the LSB location of the channel with respect to SOF (LRCK edge + phase lag).

7.22.17 ASP Receive DAI1 Channel 2 Phase and Resolution

Address 0x2A11

R/W	7	6	5	4	3	2	1	0
	—	ASP_RX1_CH2_AP	—				ASP_RX1_CH2_RES	
Default	0	0	0	0	0	0	1	1

Bits	Name	Description
7	—	Reserved
6	ASP_RX1_CH2_AP	ASP receive DAI1 active phase. Valid only in 50/50 Mode (ASP_5050 = 1 and ASP_RXx_2FS = 0). 0 (Default) Low. In 50/50 Mode, channel data is input when LRCK/FSYNC is low. 1 High. In 50/50 Mode, channel data is input when LRCK/FSYNC is high.
5:2	—	Reserved
1:0	ASP_RX1_CH2_RES	ASP receive DAI1 channel bit width. Sets the output resolution of the ASP receive DAI1 Channel *x* samples. 00 8 bits per sample (valid only for isochronous NFS and native mode) 01 16 bits per sample 10 24 bits per sample 11 (Default) 32 bits per sample

7.22.18 ASP Receive DAI1 Channel 2 Bit Start MSB

Address 0x2A12

R/W	7	6	5	4	3	2	1	0
	—							ASP_RX1_CH2_BIT_ST_MSB
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:1	—	Reserved
0	ASP_RX1_CH2_BIT_ST_MSB	ASP receive DAI1 Channel 2 bit start MSB. Configures the MSB location of the channel with respect to SOF (LRCK edge + phase lag)

7.22.19 ASP Receive DAI1 Channel 2 Bit Start LSB

Address 0x2A13

R/O	7	6	5	4	3	2	1	0
	ASP_RX1_CH2_BIT_ST_LSB							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	ASP_RX1_CH2_BIT_ST_LSB	ASP receive DAI1 Channel 2 bit start LSB. Configures the LSB location of the channel with respect to SOF (LRCK edge + phase lag)

7.23 ID Registers

7.23.1 Subrevision

Address 0x3014

R/O	7	6	5	4	3	2	1	0
	SUBREVISION							
Default	x	x	x	x	x	x	x	x

Bits	Name	Description
7:0	SUBREVISION	Subrevision. Identifies the CS42L42 subrevision. The Page 0x30 read sequence in Section 5.4 must be followed to read this register. 0000 0011 Initial version.

8 PCB Layout Considerations

The following sections provide general guidelines for PCB layout to ensure the best performance of the CS42L42.

8.1 Power Supply

As with any high-resolution converter, to realize its potential, the CS42L42 requires careful attention to power supply and grounding arrangements. Fig. 2-1 and Fig. 2-2 show the recommended power arrangements, with VA and VCP connected to clean supplies. VL, which powers the digital circuitry, may be run from the system logic supply. Alternatively, VL may be powered from the analog supply via a ferrite bead. In this case, no additional devices should be powered from VL.

8.2 Grounding

Note the following:

- Extensive use of power and ground planes, ground-plane fill in unused areas, and surface-mount decoupling capacitors are recommended.
- Decoupling capacitors should be as close as possible to the CS42L42 pins.
- To minimize inductance effects, the low-value ceramic capacitor must be closest to the pin and mounted on the same side of the board as the CS42L42.
- To avoid unwanted coupling into the modulators, all signals, especially clocks, must be isolated from the FILT+ pin.
- The FILT+ capacitor must be positioned to minimize the electrical path from the pin to GNDA.
- The +VCP_FILT and –VCP_FILT capacitors must be positioned to minimize the electrical path from each respective pin to GNDCP.

8.3 QFN Thermal Pad

The CS42L42 comes in a compact QFN package, the underside of which reveals a large metal pad that serves as a thermal relief to provide maximum heat dissipation. This pad must mate with a matching copper pad on the PCB and must be electrically connected to ground. A series of vias should be used to connect this copper pad to one or more larger ground planes on other PCB layers. For best performance in split-ground systems, connect this thermal to GNDA.

9 Plots

9.1 Digital Filter Response

9.1.1 Highpass Filter—ADC

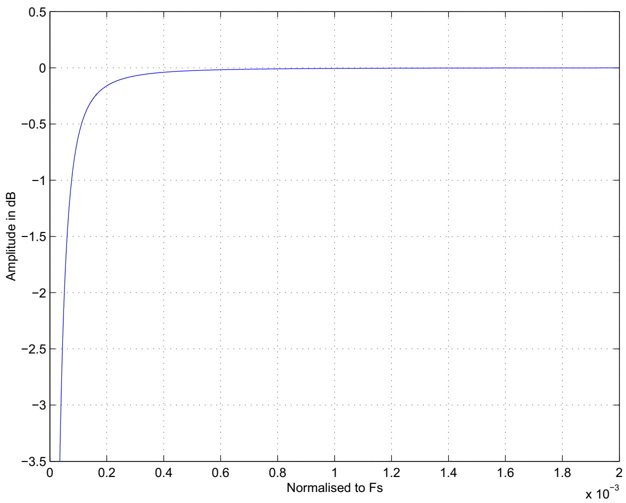


Figure 9-1. ADCx_HPF_CF = 00

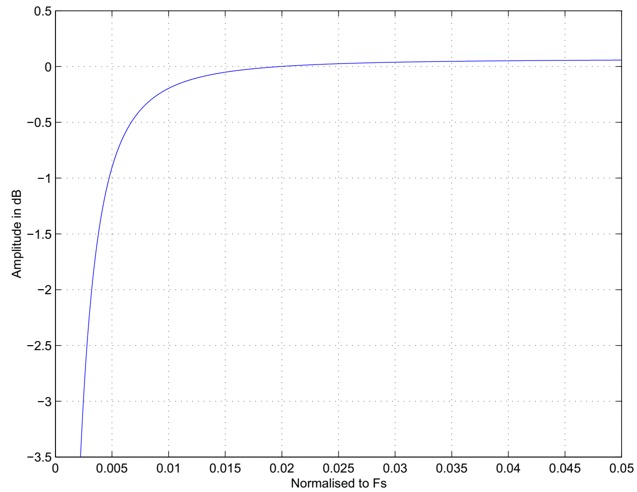


Figure 9-2. ADCx_HPF_CF = 01

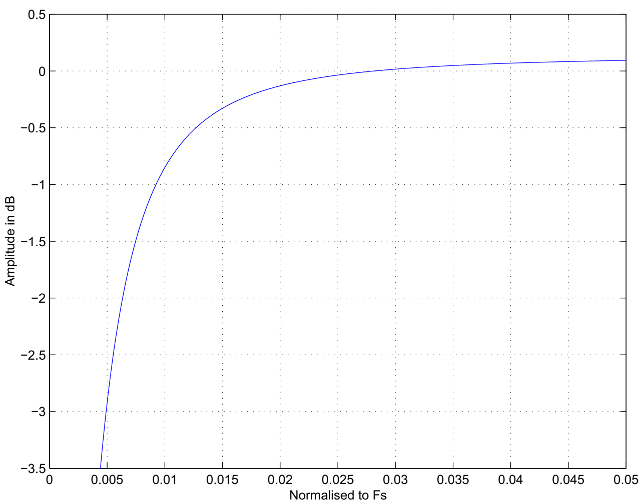


Figure 9-3. ADCx_HPF_CF = 10

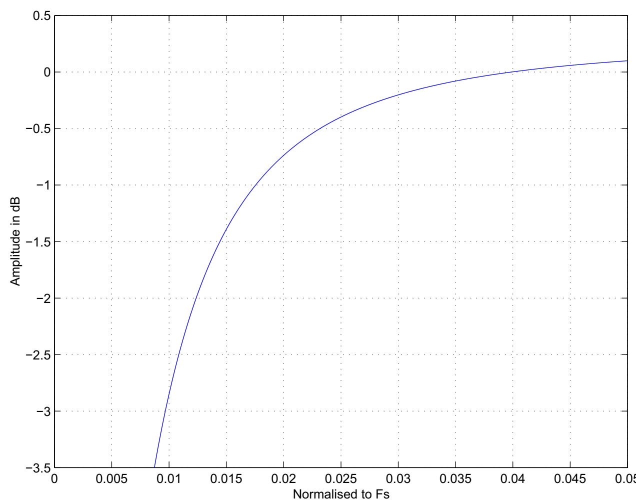


Figure 9-4. ADCx_HPF_CF = 11

9.1.2 Highpass Filter—DAC

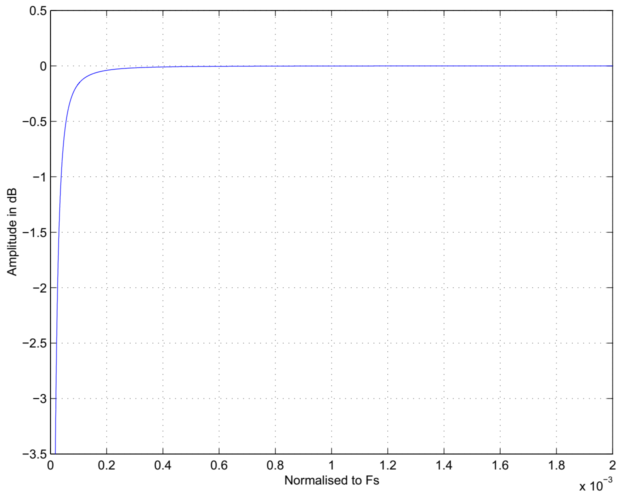


Figure 9-5. DAC HPF Response

9.1.3 ADC, Notch Filter Disabled

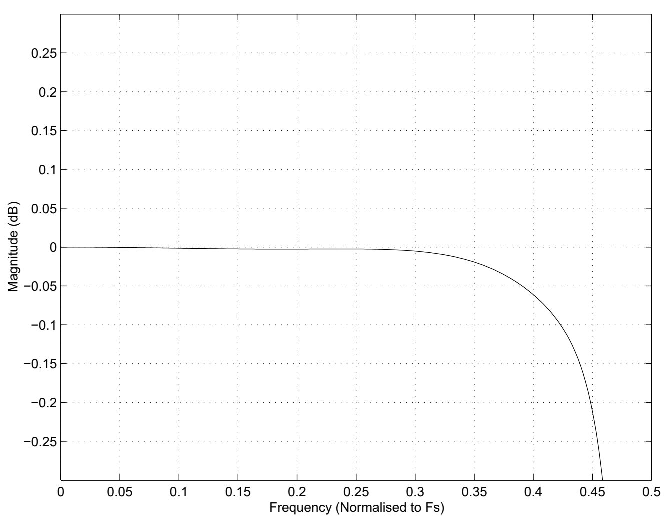


Figure 9-6. Passband—ADC, Notch Disabled

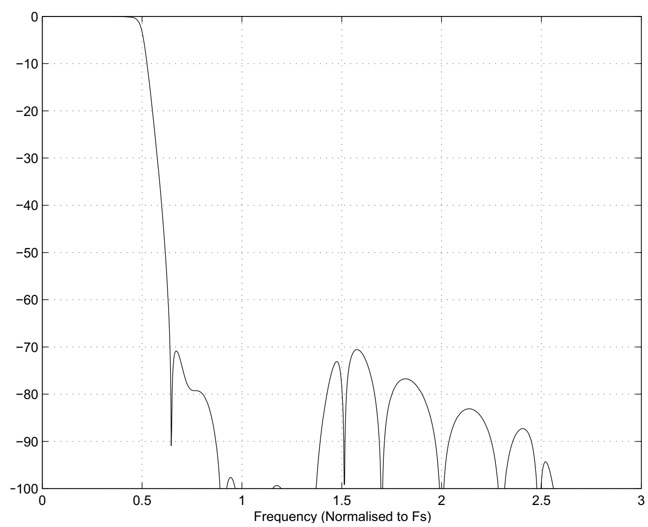


Figure 9-7. Stopband—ADC, Notch Disabled

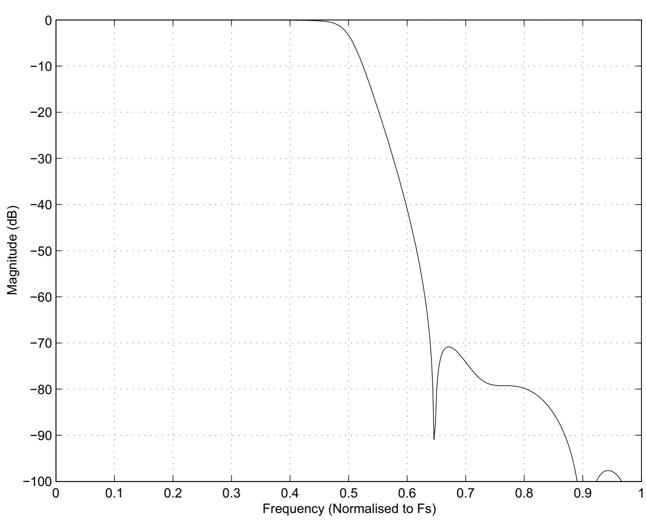


Figure 9-8. Transition Band—ADC, Notch Disabled

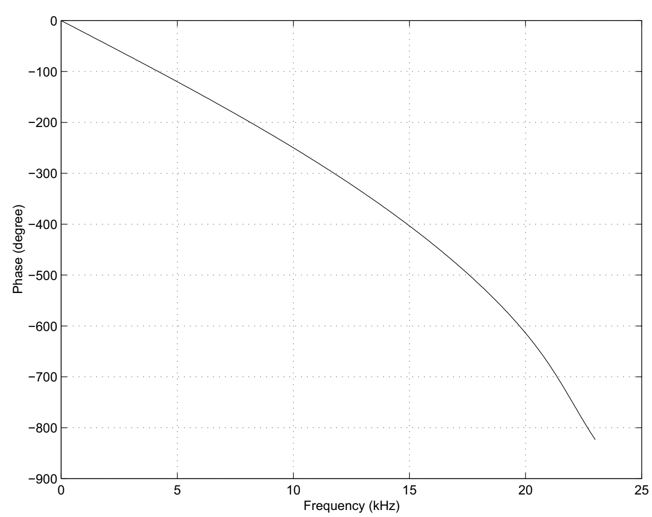


Figure 9-9. Phase Response—ADC, Notch Disabled

9.1.4 ADC, Notch Filter Enabled

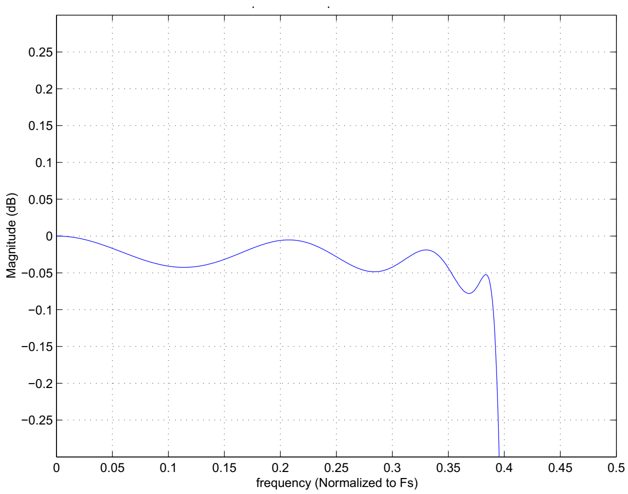


Figure 9-10. Passband—ADC, Notch Enabled

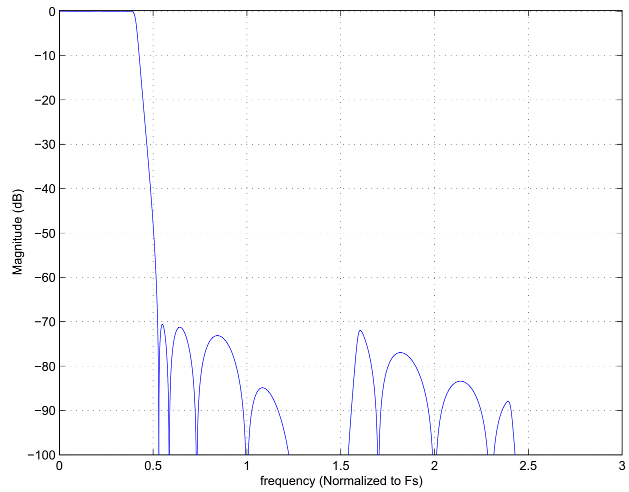


Figure 9-11. Stopband—ADC, Notch Enabled

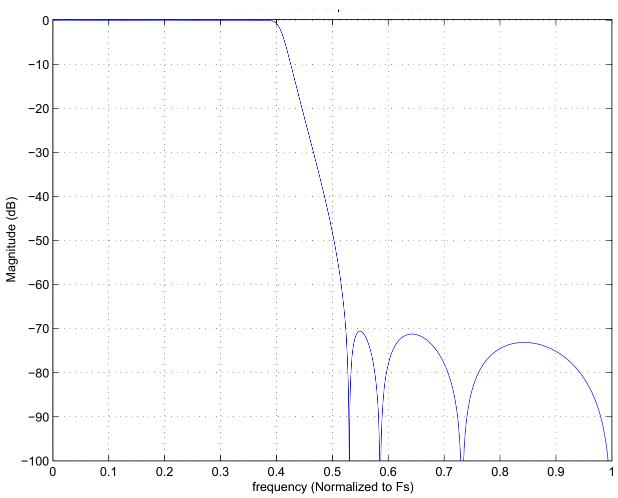


Figure 9-12. Transition Band—ADC, Notch Enabled

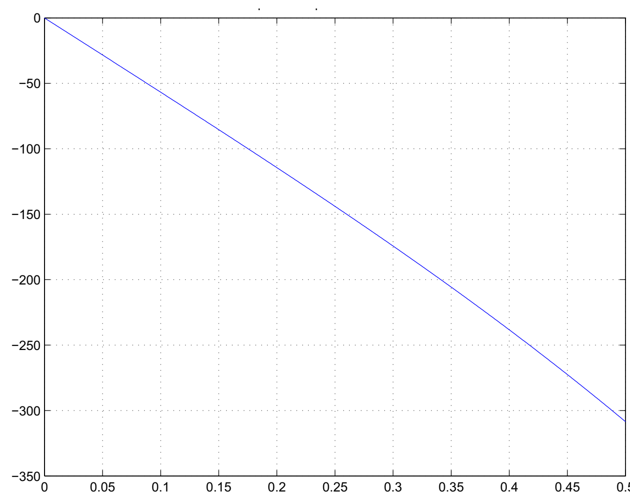


Figure 9-13. Phase Response—ADC, Notch Enabled

9.1.5 DAC to HP, Fs_{int} = 44.118 kHz, MCLK = 136 x LRCK

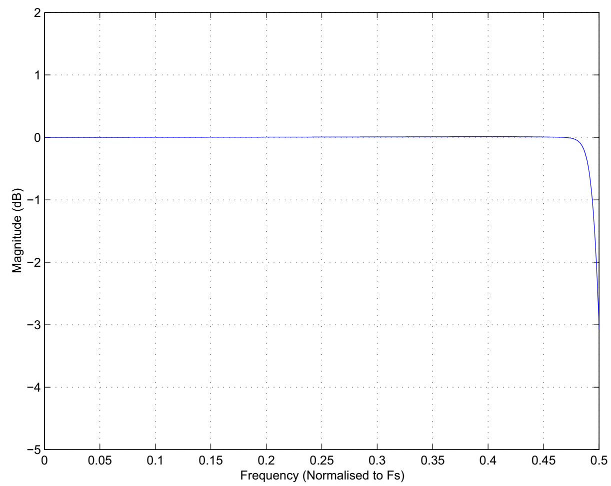


Figure 9-14. Passband—DAC, Fs_{int} = 44.118 kHz

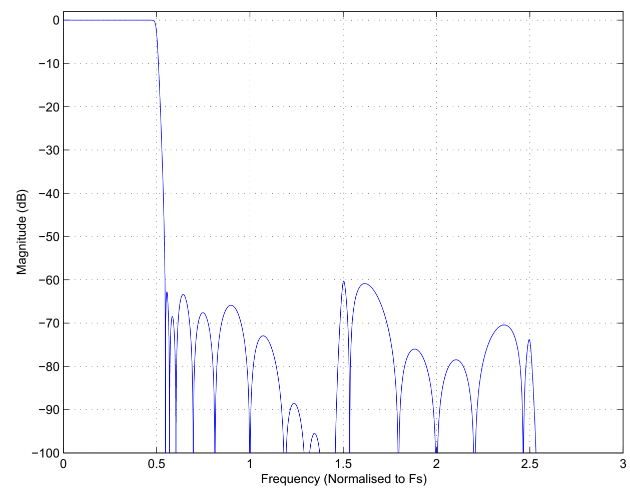


Figure 9-15. Stopband—DAC, Fs_{int} = 44.118 kHz

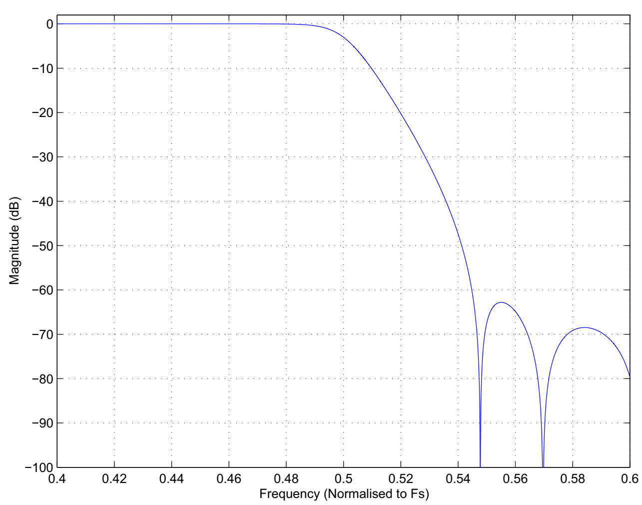


Figure 9-16. Transition Band—DAC, Fs_{int} = 44.118 kHz

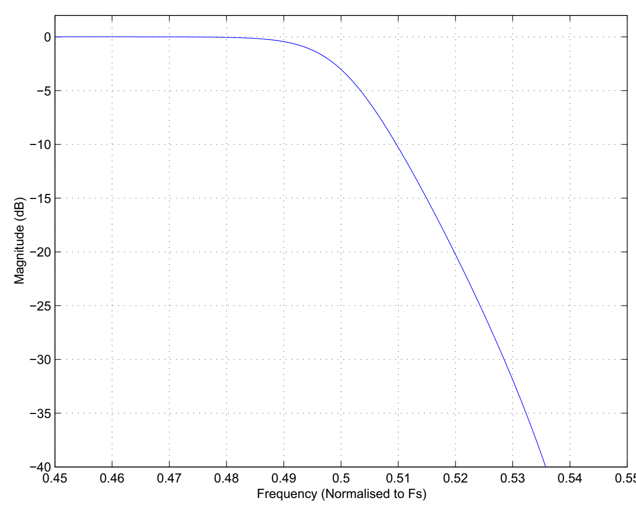


Figure 9-17. Transition Band (Detail)—DAC, Fs_{int} = 44.118 kHz

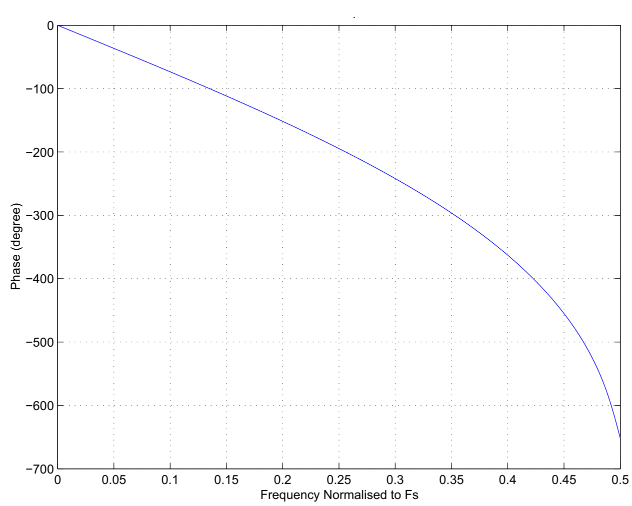


Figure 9-18. Phase Response—DAC, Fs_{int} = 44.118 kHz

9.1.6 DAC to HP, Fs_{int} = 48.000 kHz, MCLK = 125 x LRCK

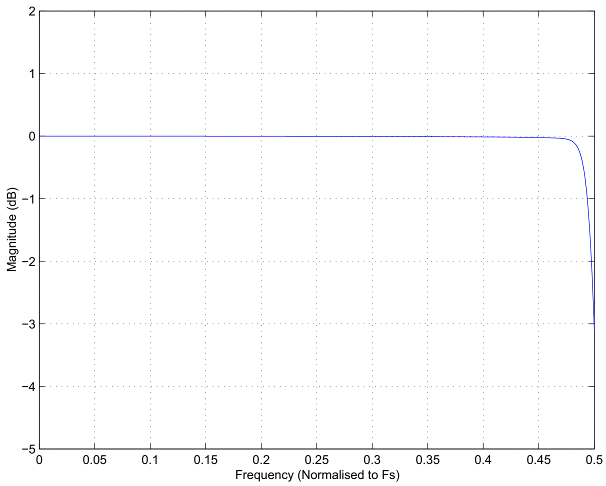


Figure 9-19. Passband—DAC, Fs_{int} = 48.000 kHz

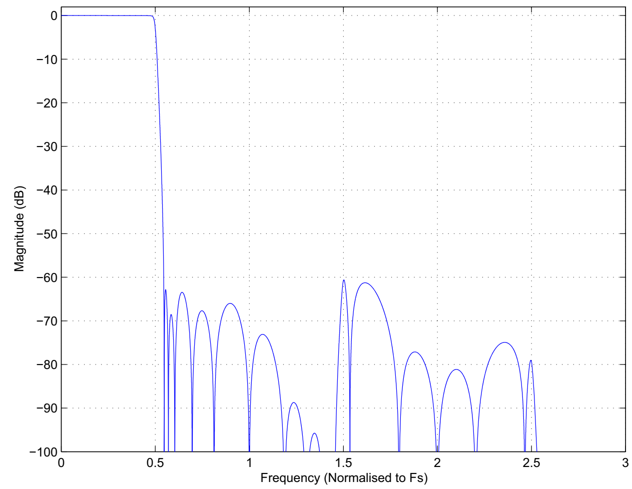


Figure 9-20. Stopband—DAC, Fs_{int} = 48.000 kHz

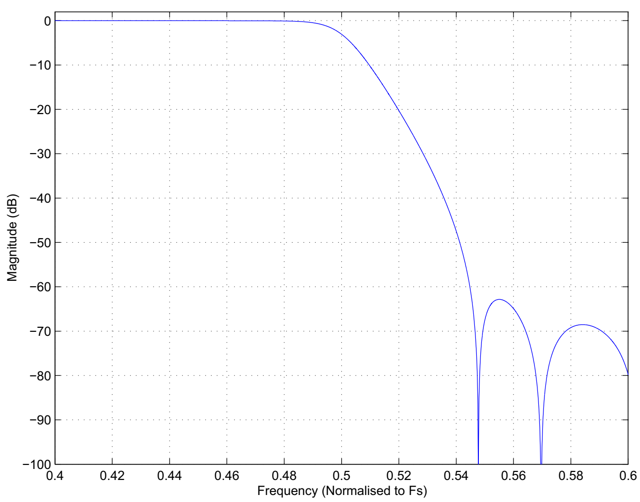


Figure 9-21. Transition Band—DAC, Fs_{int} = 48.000 kHz

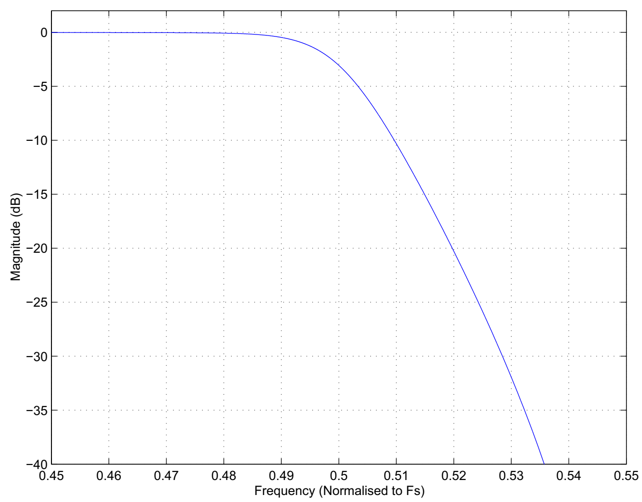


Figure 9-22. Transition Band (Detail)—DAC, Fs_{int} = 48.000 kHz

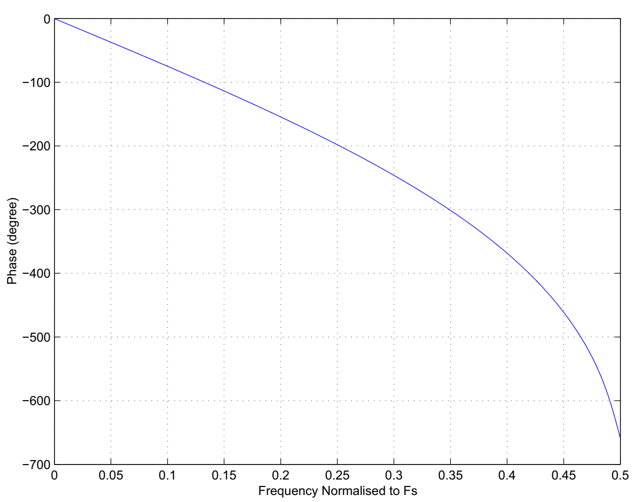


Figure 9-23. Phase Response—DAC, Fs_{int} = 48.000 kHz

9.1.7 x_SDOUT and x_SDIN ASRC, Fs_{INT} = 48 kHz

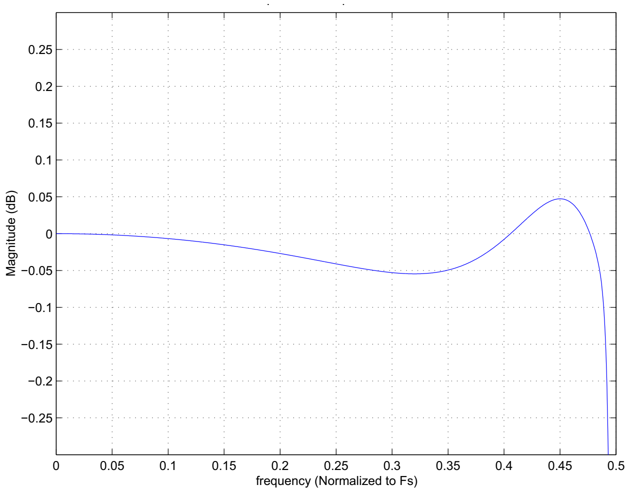


Figure 9-24. Passband—ASRC, Notch Disabled

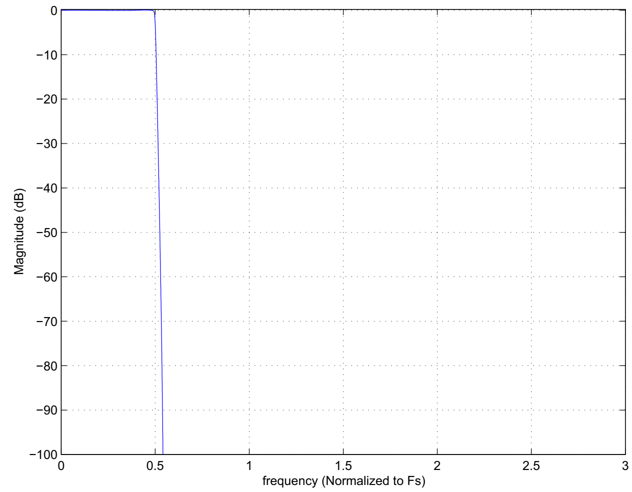


Figure 9-25. Stopband—ASRC, Notch Disabled

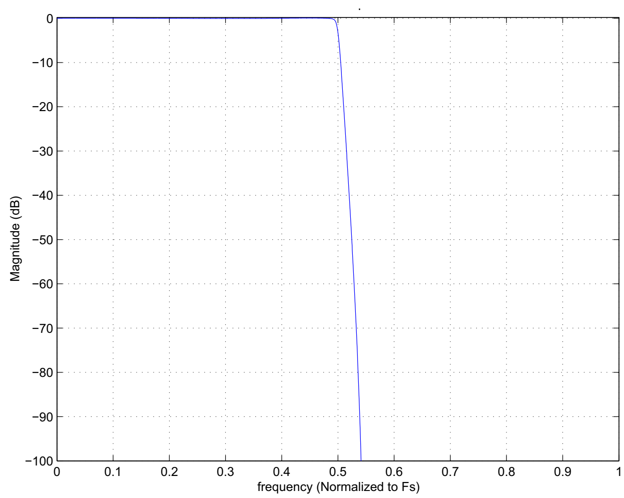


Figure 9-26. Transition Band—ASRC, Notch Disabled

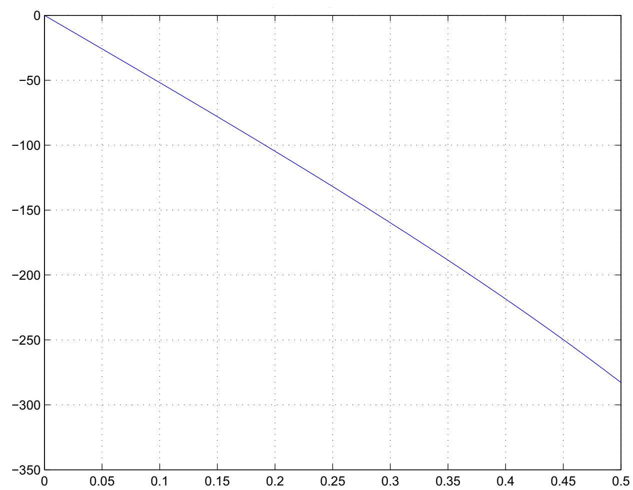


Figure 9-27. Phase Response—ASRC, Notch Disabled

9.2 Windnoise Filter Responses

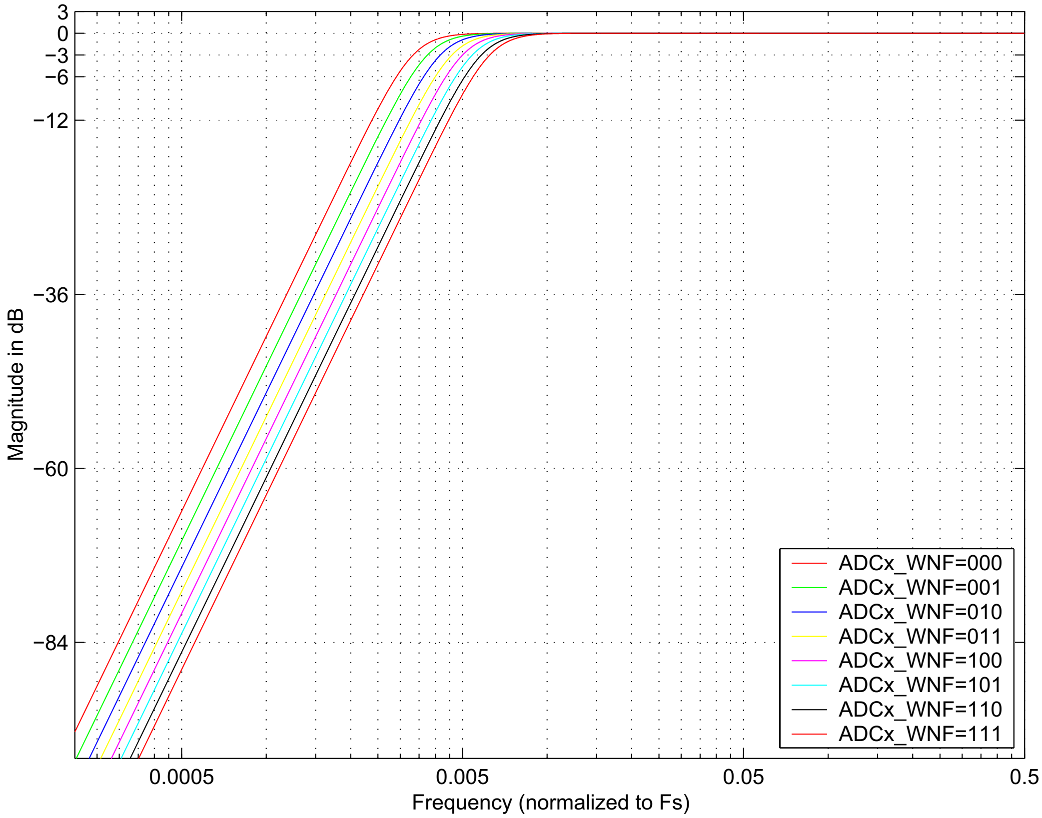


Figure 9-28. Windnoise Filter Frequency Response

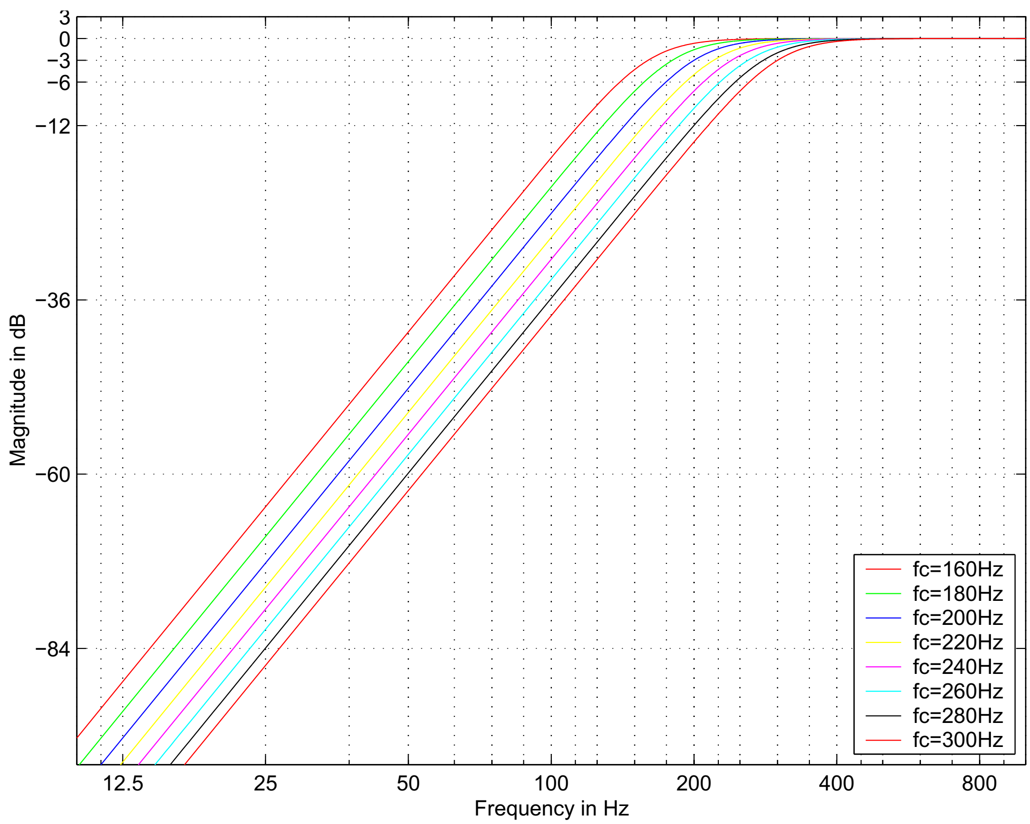


Figure 9-29. Windnoise Filter Transition Band

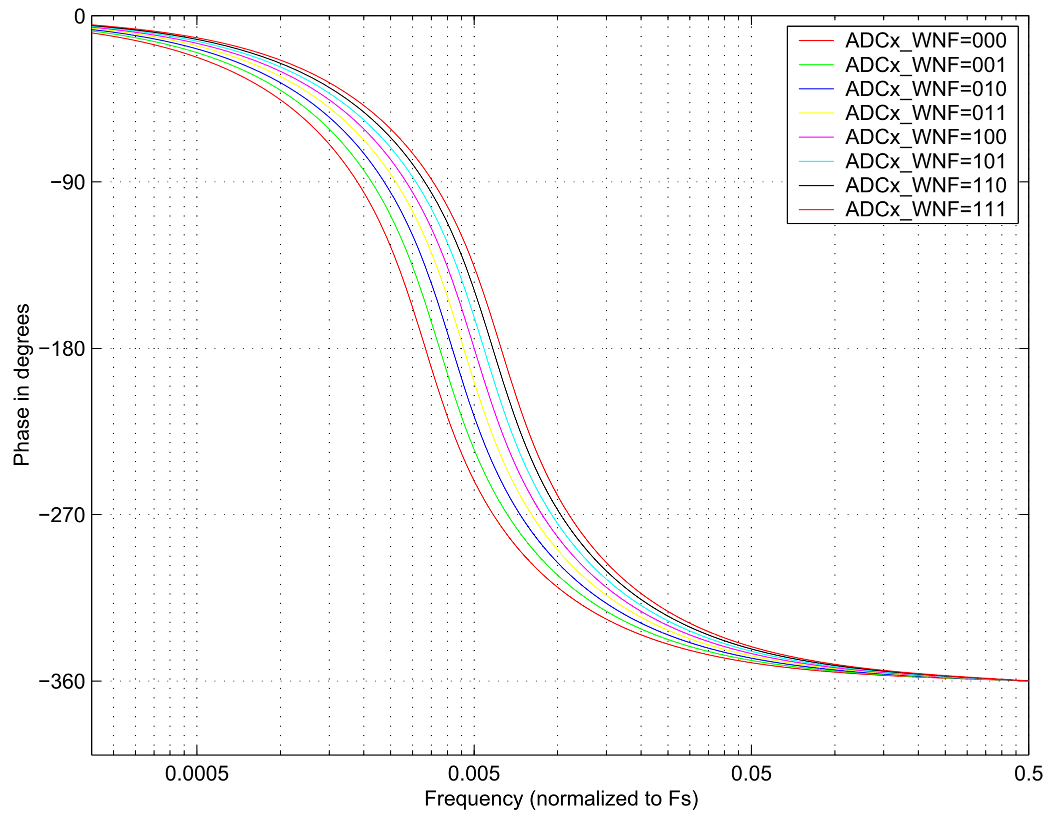


Figure 9-30. Windnoise Filter Phase Response

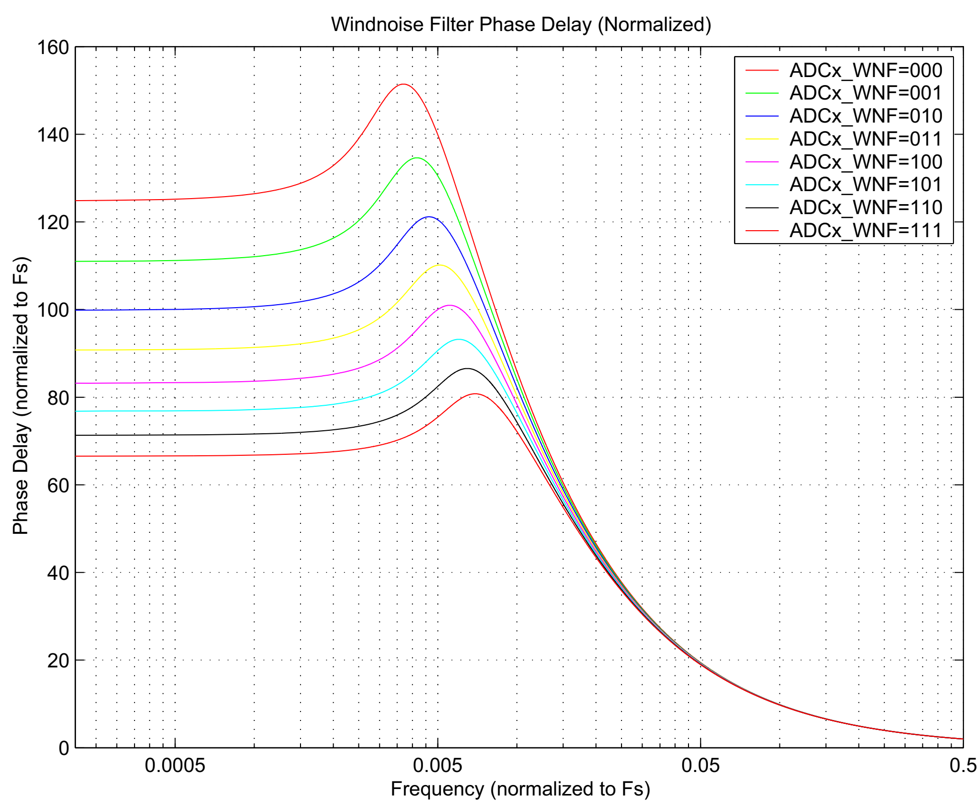


Figure 9-31. Windnoise Filter Delay

9.3 HSBIAS Current Sense vs. VP Voltage per Trip Setting

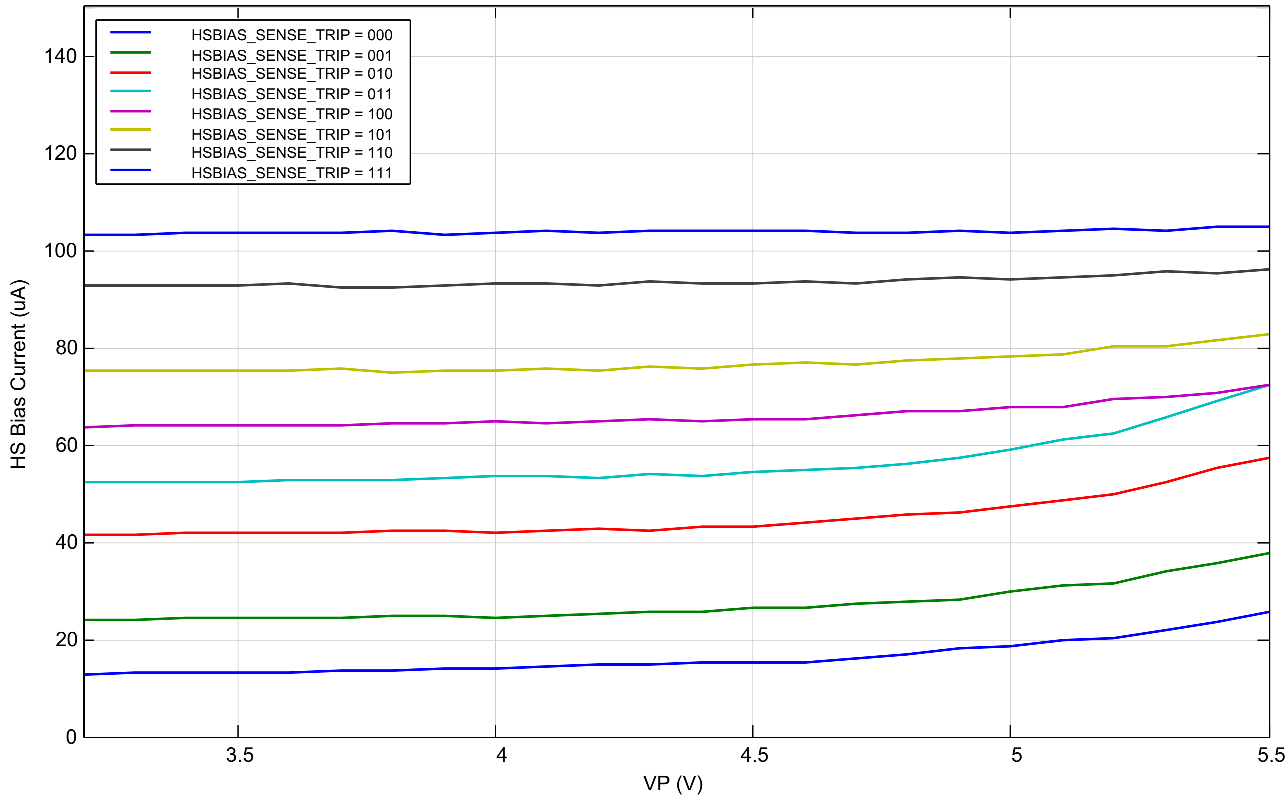
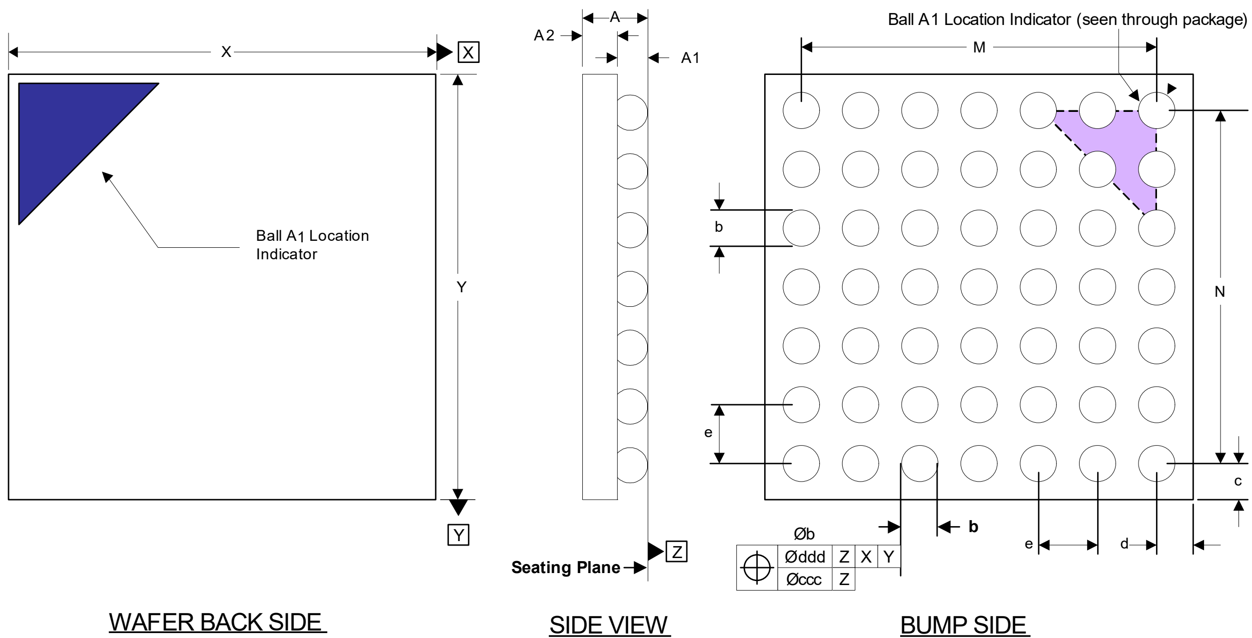


Figure 9-32. HS Bias Current Sense vs. VP Voltage for Each Trip Setting (HS BIAS = 2-V Mode)

10 Package Dimensions

10.1 WLCSP Package Dimensions



Notes:
- Dimensioning and tolerances per ASME Y 14.5M–1994.
- The Ball A1 position indicator is for illustration purposes only and may not be to scale.
- Dimension “b” applies to the solder sphere diameter and is measured at the maximum solder-ball diameter, parallel to primary Datum Z.

Table 10-1. WLCSP Package Dimensions

Dimension	Millimeters		
	Minimum	Nominal	Maximum
A	0.443	0.474	0.505
A1	0.148	0.174	0.200
A2	0.284	0.300	0.316
M	BSC	2.100	BSC
N	BSC	2.100	BSC
b	0.225	0.250	0.300
c	REF	0.272	REF
d	REF	0.272	REF
e	BSC	0.350	BSC
X	2.614	2.644	2.674
Y	2.614	2.644	2.674
ccc = 0.015 ddd = 0.015			

Note: Controlling dimension is millimeters.

10.2 QFN Package Dimensions

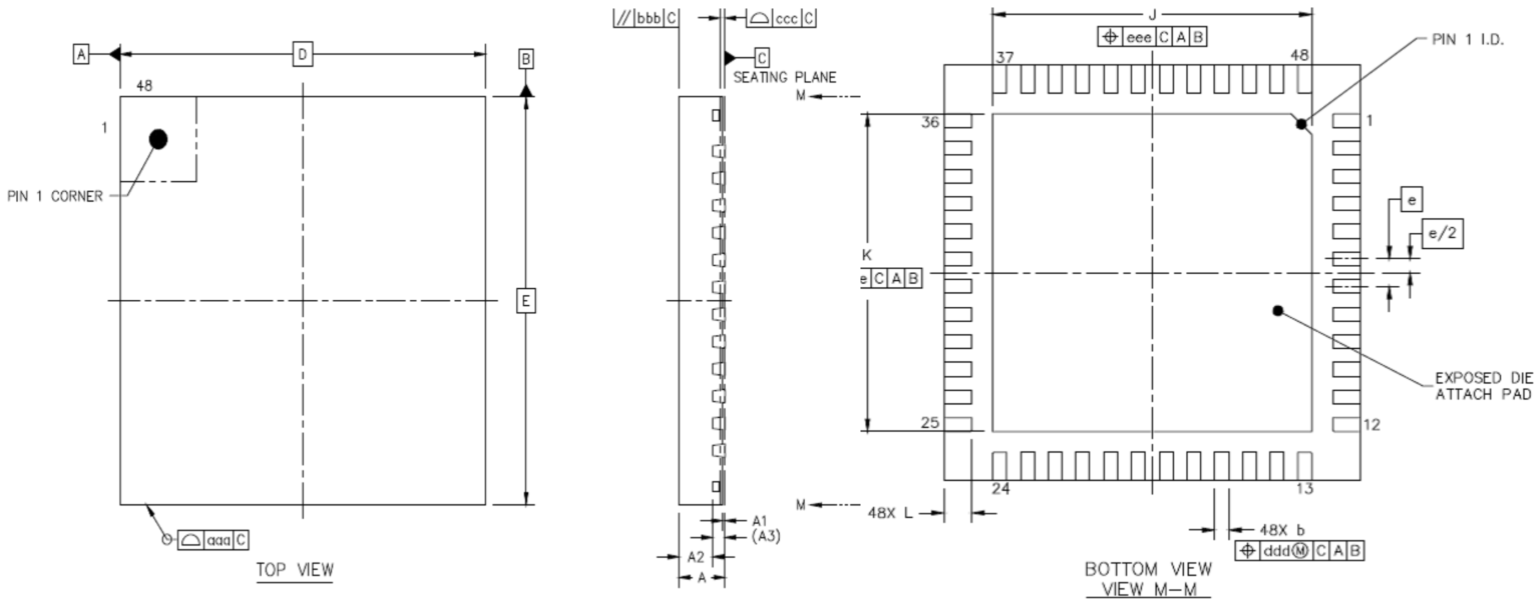


Table 10-2. QFN Package Dimensions

Dimension	mm		
	Minimum	Nominal	Maximum
A	0.70	0.75	0.80
A1	0.00	0.035	0.05
A2	—	0.55	—
A3	0.203 REF		
b	0.15	0.20	0.25
D	6.00 BSC		
K	4.4	4.5	4.6
e	0.40 BSC		
E	6.00 BSC		
J	4.4	4.5	4.6
L	0.35	0.40	0.45
aaa	0.10		
bbb	0.10		
ccc	0.08		
ddd	0.10		
eee	0.10		

11 Thermal Characteristics

Table 11-1. Typical JEDEC Four-Layer, 2s2p Board Thermal Characteristics

Parameter [1]	Symbol	QFN	WLCSP	Unit
Junction-to-ambient thermal resistance	θ_{JA}	33.3	52.0	°C/W
Junction-to-board thermal resistance	θ_{JB}	8.8	17.8	°C/W
Junction-to-case thermal resistance	θ_{JC}	0.93	0.15	°C/W
Junction-to-board thermal-characterization parameter	Ψ_{JB}	8.8	17.7	°C/W
Junction-to-package-top thermal-characterization parameter	Ψ_{JT}	0.17	0.04	°C/W

1. Thermal setup:
Still air @ maximum allowed ambient temperature
JEDEC 2s2p printed wiring board (JEDEC Standard JESD51-11, June 2001)
Size: 114.5 x 101.5 x 1.6 mm

12 Ordering Information

Table 12-1. Ordering Information[1]

Product	Description	Package	RoHS Compliant	Grade	Temperature Range	Container	Order #
CS42L42	Low-Power Audio Codec with SoundWire®–I²S/TDM and Audio Processing	49-ball WLCSP	Yes	Extended Commercial	–40 to +85°C	Tape and reel	CS42L42-CWZR
		48-pin QFN	Yes	Extended Commercial	–40 to +85°C	Tape and reel	CS42L42-CNZR
						Tray	CS42L42-CNZ

1. The Revision ID fields in Section 7.3.4, “Revision ID,” list the alpha (AREVID) and metal (MTLREVID) revision

13 References

- *MIPI SoundWire Specification, Version 1.0.*
- International Electrotechnical Commission*, IEC60958-3 Digital Audio Interface—Consumer, http://www.ansi.org/*
- NXP Semiconductors, UM10204 Rev. 06, April 2014, *The I²C-Bus Specification and User Manual*, http://www.nxp.com
- JEDEC Solid State Technology Association, *Guidelines for Reporting and Using Electronic Package Thermal Information*, *JEDEC Standard No. 51-12.01*, November 2012, http://www.jedec.org/

14 Revision History

Table 14-1. Revision History

Revision	Changes
F1 MAY '16	• Updated SWIRE_SEL connection to VL in Fig. 2-2. • Added note about options regarding 0402 capacitors to Section 2.1.1. • Added footnote about measurements with HPF disabled to Table 3-5 and Table 3-9. • Updated CMRR typical values in Table 3-13. • Updated typical values and Footnote 4 in Table 3-15. Added HPOUT pull-down resistance to Table 3-16. • Updated Table 4-27, Typical Leakage Current during Nonoperational Supply States (with VP Powered On)," in Section 4.15. • Added Section 5.3. "SoundWire Power Sequences." • Added Section 5.4, "Page 0x30 Read Sequence." • Added HPOUT_PULLDOWN to Section 6.13 and Section 7.12.2. • Refined wording for Section 7.6.12.
F2 AUG '17	• Updated SWIRE_SEL connection to VL in Fig. 2-2. • Changed references to VD to VD_FILT in Section 5.8. • Updated Fig. 4-28 in Section 4.8.13 to be more specific. • Updated VL/VD_FILT ordering in Section 4.15. • Relabelled the Y axes in Fig. 4-17 and Fig. 4-19 in Section 4.6.3.
F3 JAN '18	• Removed footnote 2 and renumbered remaining footnotes for Fig. 2-1 and Fig. 2-2. • Added missing text in first bullet in Section 5.8. • Added footnote 1 and updated package certification information in Table 12-1 (Nomenclature change only; no change to package). • Added connections for HPSENSA/B and HS_CLAMP1/2 in Fig. 2-2.

Important: Please check with your Cirrus Logic sales representative to confirm that you are using the latest revision of this document and to determine whether there are errata associated with this device.

Contacting Cirrus Logic Support

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