Double Data Rate (DDR) SDRAM Data Sheet Addendum

MT46V64M4 – 16 Meg x 4 x 4 banks
MT46V32M8 – 8 Meg x 8 x 4 banks
MT46V16M16 – 4 Meg x 16 x 4 banks

Features

- V_{DD} = 2.5V ±0.2V, VddQ = 2.5V ±0.2V
  V_{DD} = 2.6V ±0.1V, V_{DDQ} = 2.6V ±0.1V (DDR400)[1]
- Bidirectional data strobe (DQS) transmitted/received with data, that is, source-synchronous data capture (x16 has two – one per byte)
- Internal, pipelined double-data-rate (DDR) architecture; two data accesses per clock cycle
- Differential clock inputs (CK and CK#)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- DLL to align DQ and DQS transitions with CK
- Four internal banks for concurrent operation
  - Data mask (DM) for masking write data (x16 has two – one per byte)
  - Programmable burst lengths (BL): 2, 4, or 8
- Auto refresh: 64ms, 8192-cycle
- Longer-lead TSOP for improved reliability (OCPL)
- 2.5V I/O (SSTL_2-compatible)
- Concurrent auto precharge option supported
- ^{t}RAS lockout supported (^{t}RAP = ^{t}RCD)

Options — Marking

- Configuration
  - 64 Meg x 4 (16 Meg x 4 x 4 banks) — 64M4
  - 32 Meg x 8 (8 Meg x 8 x 4 banks) — 32M8
  - 16 Meg x 16 (4 Meg x 16 x 4 banks) — 16M16
- Plastic package (OCPL)
  - 66-pin TSOP — TG
  - 66-pin TSOP (Pb-free) — P
- Plastic package
  - 60-ball FBGA (8mm x 12.5mm) — CV
  - 60-ball FBGA (8mm x 12.5mm) (Pb-free) — CY
- Timing (cycle time)
  - 5ns @ CL = 3 (DDR400) — -5B
  - 6ns @ CL = 2.5 (DDR333 – FBGA only) — -6[2]
  - 6ns @ CL = 2.5 (DDR333 – TSOP only) — -6T[2]
- Special Options
  - Product Longevity Program (PLP) — X
- Self refresh
  - Standard — None
  - Low power — L
- Temperature rating
  - Commercial (0°C to +70°C) — None
  - Industrial (–40°C to +85°C) — IT
- Revision
  - x4, x8, x16 — :K[4]
  - x4, x8, x16 — :M

Notes:
1. DDR400 devices operating at < DDR333 conditions can use V_{DD}/V_{DDQ} = 2.5V +0.2V.
2. Available only on Revision K.
3. Available only on Revision M.
4. Not recommended for new designs.

Table 1: Key Timing Parameters

CL = CAS (READ) latency; MIN clock rate with 50% duty cycle at CL = 2 (-75E, -75Z), CL = 2.5 (-6, -6T, -75), and CL = 3 (-5B)

Speed Grade	Clock Rate (MHz)			Data-Out Window	Access Window	DQS–DQ Skew
	CL = 2	CL = 2.5	CL = 3			
-5B	133	167	200	1.6ns	±0.70ns	0.40ns

Table 1: Key Timing Parameters (Continued)

CL = CAS (READ) latency; MIN clock rate with 50% duty cycle at CL = 2 (-75E, -75Z), CL = 2.5 (-6, -6T, -75), and CL = 3 (-5B)

Speed Grade	Clock Rate (MHz)			Data-Out Window	Access Window	DQS–DQ Skew
	CL = 2	CL = 2.5	CL = 3			
-6	133	167	n/a	2.1ns	±0.70ns	0.40ns
6T	133	167	n/a	2.0ns	±0.70ns	0.45ns
-75E/-75Z	133	133	n/a	2.5ns	±0.75ns	0.50ns
-75	100	133	n/a	2.5ns	±0.75ns	0.50ns

Table 2: Addressing

Parameter	64 Meg x 4	32 Meg x 8	16 Meg x 16
Configuration	16 Meg x 4 x 4 banks	8 Meg x 8 x 4 banks	4 Meg x 16 x 4 banks
Refresh count	8K	8K	8K
Row address	8K (A[12:0])	8K (A[12:0])	8K (A[12:0])
Bank address	4 (BA[1:0])	4 (BA[1:0])	4 (BA[1:0])
Column address	2K (A[11, 9:0])	1K (A[9:0])	512 (A[8:0])

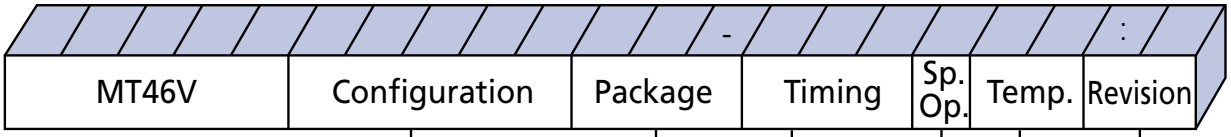
Table 3: Speed Grade Compatibility

Marking	PC3200 (3-3-3)	PC2700 (2.5-3-3)	PC2100 (2-2-2)	PC2100 (2-3-3)	PC2100 (2.5-3-3)	PC1600(2-2-2)
-5B[1]	Yes	Yes	Yes	Yes	Yes	Yes
-6	–	Yes	Yes	Yes	Yes	Yes
-6T	–	Yes	Yes	Yes	Yes	Yes
-75E	–	–	Yes	Yes	Yes	Yes
-75Z	–	–	–	Yes	Yes	Yes
-75	–	–	–	–	Yes	Yes
	-5B	-6/-6T	-75E	-75Z	-75	-75

Note: 1. The -5B device is backward compatible with all slower speed grades. The voltage range of the -5B device operating at slower speed grades is V_{DD} = V_{DDQ} = 2.5V ± 0.2V.

Figure 1: 256Mb DDR SDRAM Part Numbers

Example Part Number: MT46V16M16P-6T:M



Configuration	
64 Meg x 4	64M4
32 Meg x 8	32M8
16 Meg x 16	16M16

	Revision
:K	x4, x8, x16
:M	x4, x8, x16

Package	
400-mil TSOP	TG
400-mil TSOP (Pb-free)	P
8mm x 12.5mm FBGA	CV
8mm x 12.5mm FBGA (Pb-free)	CY

	Operating Temp.
	Commercial
IT	Industrial

Timing	
^{t}CK = 5ns, CL = 3	-5B
^{t}CK = 6ns, CL = 2.5	-6
^{t}CK = 6ns, CL = 2.5	-6T

	Special Options*
	Standard
L	Low power
X	Product Longevity Program

*Multiple processing codes are separated by a space and are listed in hierarchical order.

Revision History

Rev. A – 03/14

- Initial release based on the 256Mb x4, x8, x16 DDR SDRAM, Rev. Q 07/11 data sheet

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein.
Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.