

IRF3305PbF

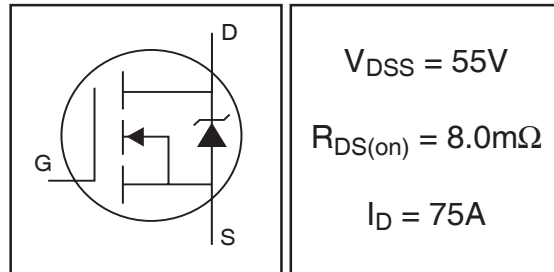
Features

- Designed to support Linear Gate Drive Applications
- 175°C Operating Temperature
- Low Thermal Resistance Junction - Case
- Rugged Process Technology and Design
- Fully Avalanche Rated
- Lead-Free

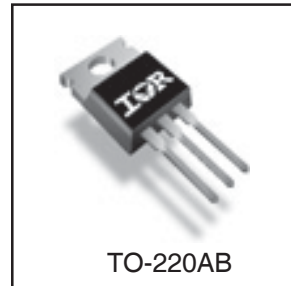
Description

This HEXFET Power MOSFET utilizes a rugged planar process technology and device design, which greatly improves the Safe Operating Area (SOA) of the device. These features, coupled with 175°C junction operating temperature and "low thermal resistance of 0.45C/W"

HEXFET® Power MOSFET



$V_{DSS} = 55V$
 $R_{DS(on)} = 8.0m\Omega$
 $I_D = 75A$



Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Silicon Limited)	140	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	99	
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Package Limited)	75	
I_{DM}	Pulsed Drain Current ①	560	
$P_D @ T_C = 25^\circ C$	Power Dissipation	330	W
	Linear Derating Factor	2.2	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS} (Thermally limited)	Single Pulse Avalanche Energy ②	470	mJ
E_{AS} (Tested)	Single Pulse Avalanche Energy Tested Value ③	860	
I_{AR}	Avalanche Current ④	See Fig.12a, 12b, 15, 16	A
E_{AR}	Repetitive Avalanche Energy ⑤		mJ
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑦	—	0.45	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient ⑧	—	62	

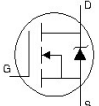
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Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

International
IR Rectifier

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	55	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.055	—	V/°C	Reference to 25°C , $I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	8.0	mΩ	$V_{GS} = 10V, I_D = 75A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
g_{fs}	Forward Transconductance	41	—	—	S	$V_{DS} = 25V, I_D = 75A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 55V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 55V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-200		$V_{GS} = -20V$
Q_g	Total Gate Charge	—	100	150		$I_D = 75A$
Q_{gs}	Gate-to-Source Charge	—	21	—	nC	$V_{DS} = 44V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	45	—		$V_{GS} = 10V$ ③
$t_{d(on)}$	Turn-On Delay Time	—	16	—		$V_{DD} = 28V$
t_r	Rise Time	—	88	—		$I_D = 75A$
$t_{d(off)}$	Turn-Off Delay Time	—	43	—	ns	$R_G = 2.6\ \Omega$
t_f	Fall Time	—	34	—		$V_{GS} = 10V$ ③
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	3650	—		$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	1230	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	450	—	pF	$f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	4720	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	930	—		$V_{GS} = 0V, V_{DS} = 44V, f = 1.0\text{MHz}$
$C_{oss\ eff.}$	Effective Output Capacitance	—	1490	—		$V_{GS} = 0V, V_{DS} = 0V\ \text{to}\ 44V$ ④

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	75	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	560		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 75A, V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	—	57	86	ns	$T_J = 25^\circ\text{C}, I_F = 75A, V_{DD} = 28V$
Q_{rr}	Reverse Recovery Charge	—	130	190	nC	$di/dt = 100A/\mu s$ ③
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).
- ② Limited by T_{Jmax} , starting $T_J = 25^\circ\text{C}$, $L = 0.17\text{mH}$
 $R_G = 25\ \Omega, I_{AS} = 75A, V_{GS} = 10V$. Part not recommended for use above this value.
- ③ Pulse width $\leq 1.0\text{ms}$; duty cycle $\leq 2\%$.
- ④ $C_{oss\ eff.}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑤ Limited by T_{Jmax} , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.
- ⑥ This value determined from sample failure population. 100% tested to this value in production.
- ⑦ R_{θ} is measured at T_J of approximately 90°C .

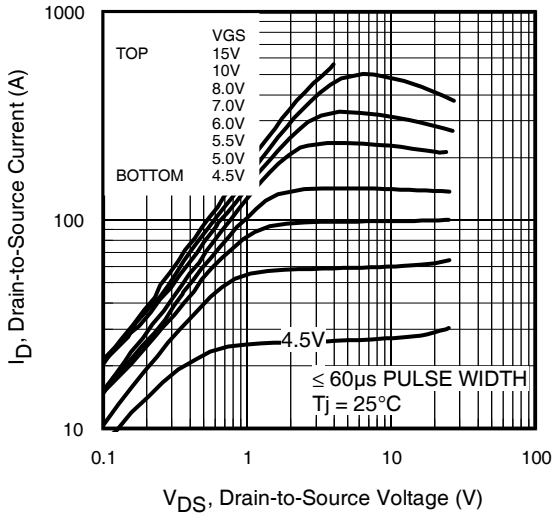


Fig 1. Typical Output Characteristics

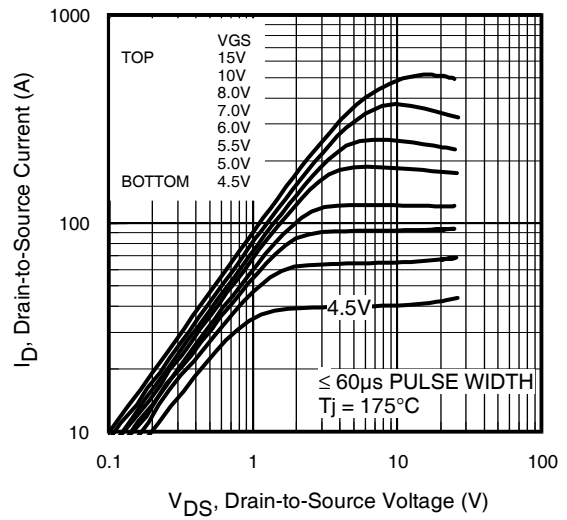


Fig 2. Typical Output Characteristics

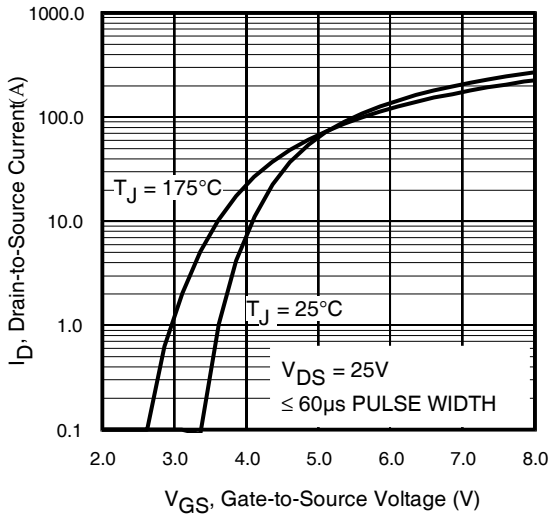


Fig 3. Typical Transfer Characteristics

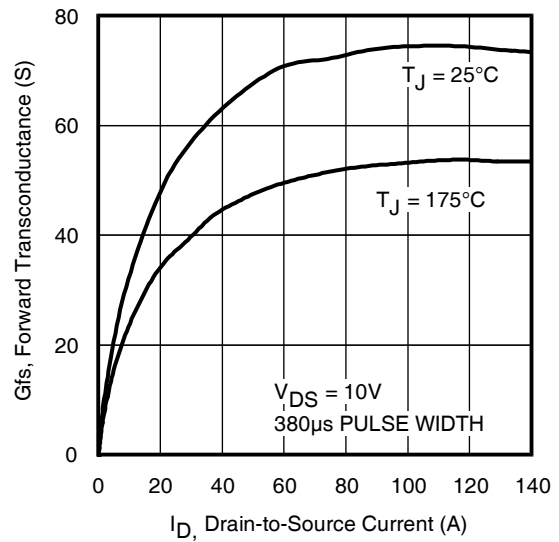


Fig 4. Typical Forward Transconductance Vs. Drain Current

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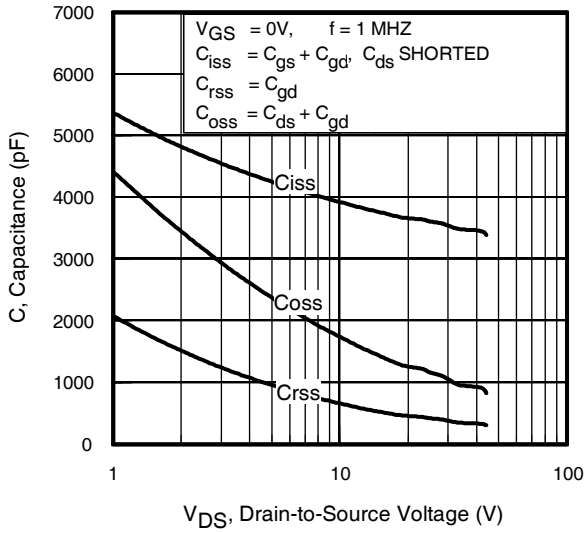


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

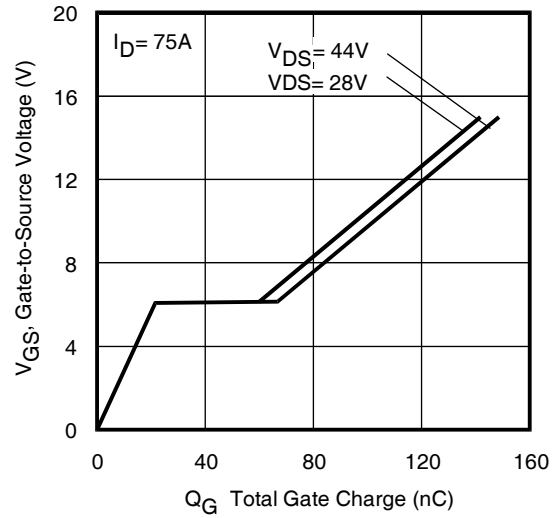


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

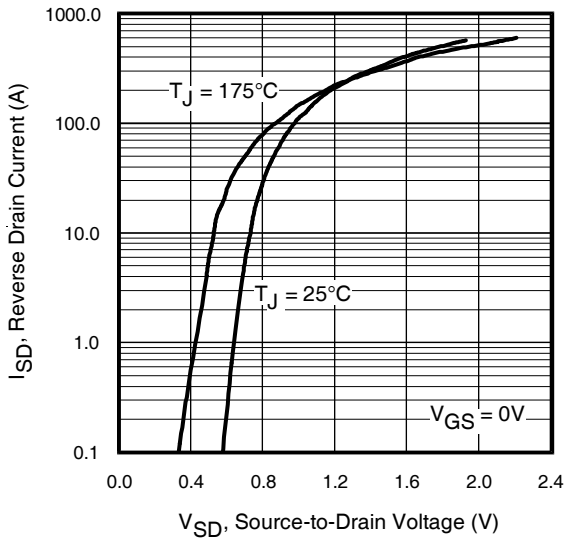


Fig 7. Typical Source-Drain Diode Forward Voltage

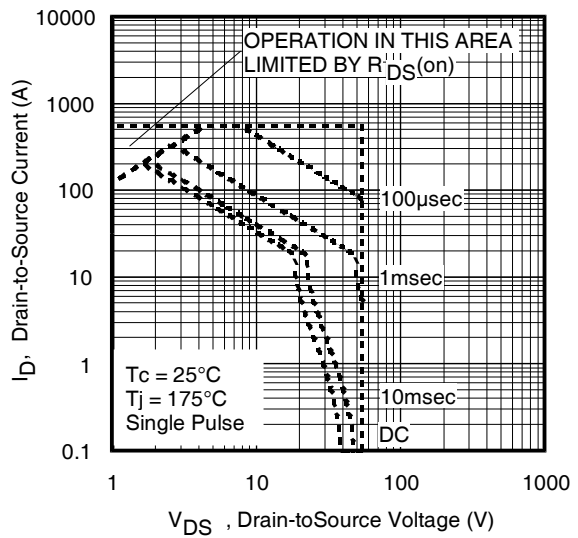


Fig 8. Maximum Safe Operating Area

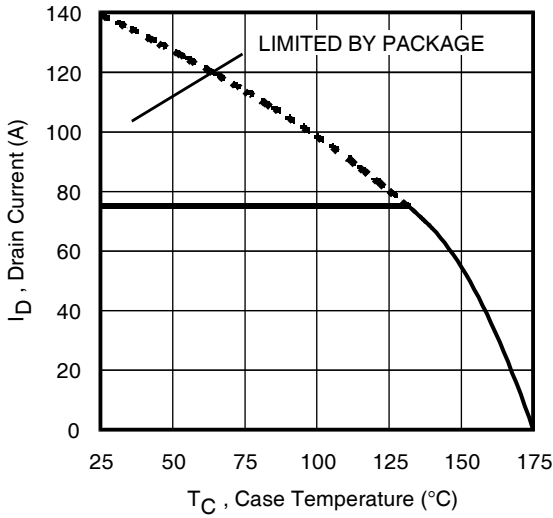


Fig 9. Maximum Drain Current Vs. Case Temperature

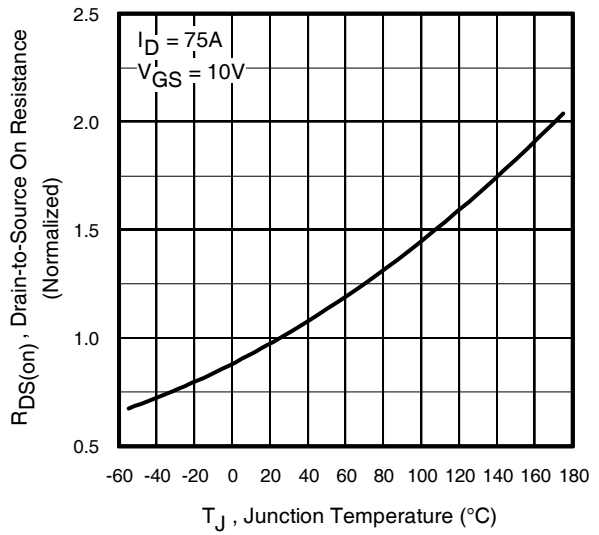


Fig 10. Normalized On-Resistance Vs. Temperature

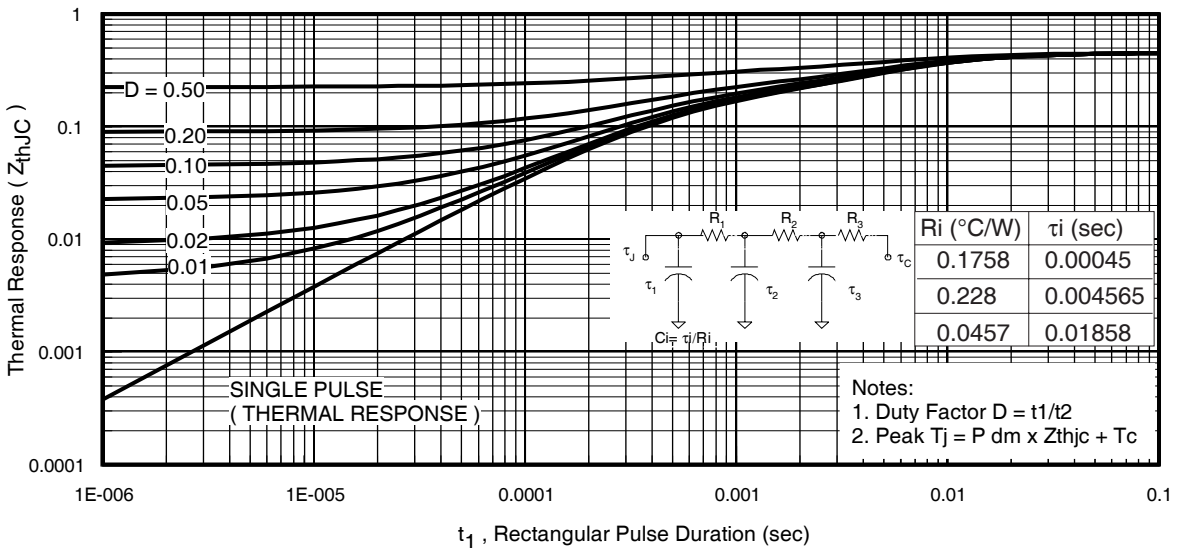


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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Fig 12a. Unclamped Inductive Test Circuit



Fig 12b. Unclamped Inductive Waveforms



Fig 13a. Basic Gate Charge Waveform

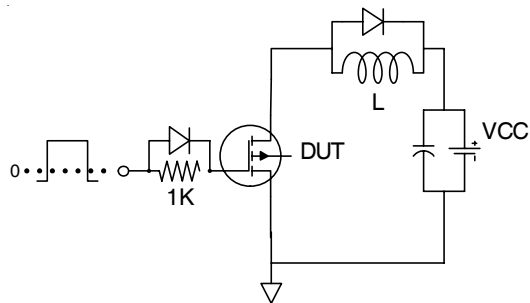


Fig 13b. Gate Charge Test Circuit

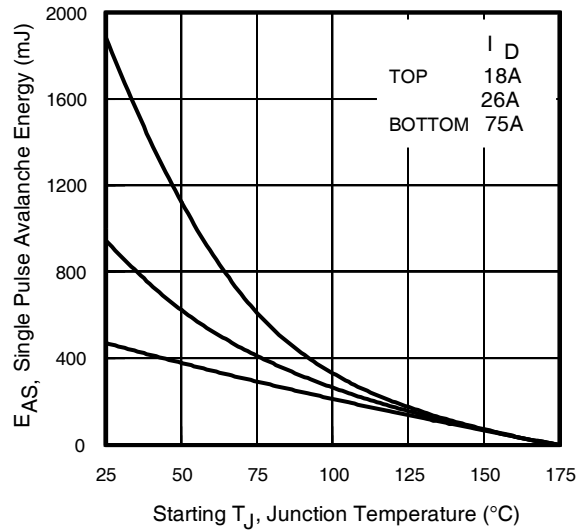


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

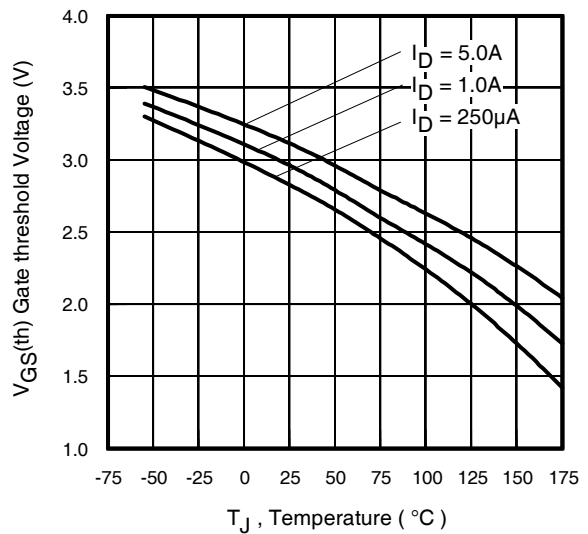


Fig 14. Threshold Voltage Vs. Temperature

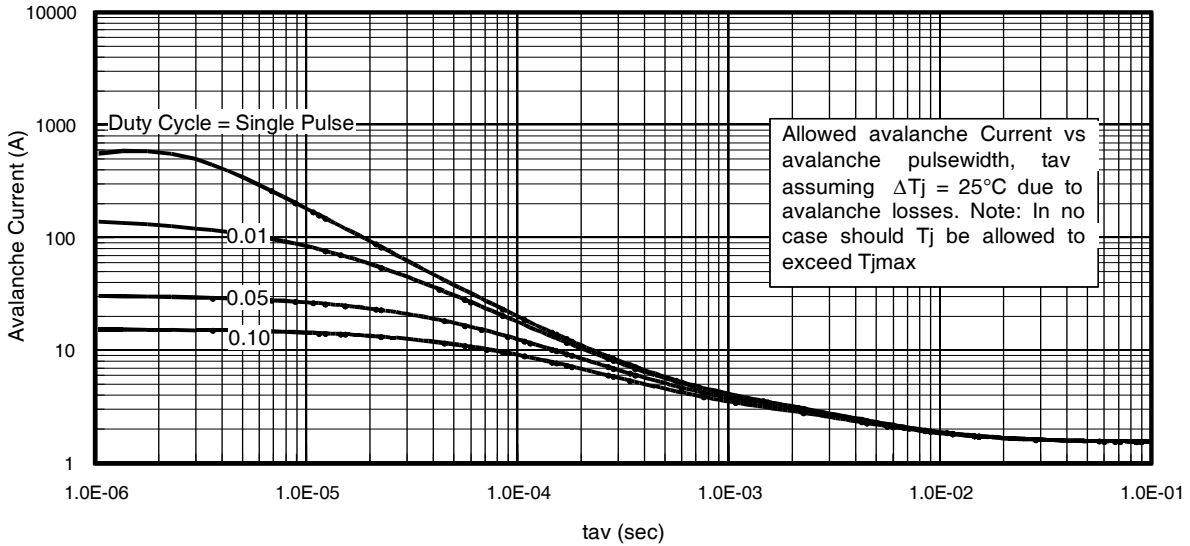


Fig 15. Typical Avalanche Current Vs.Pulsewidth

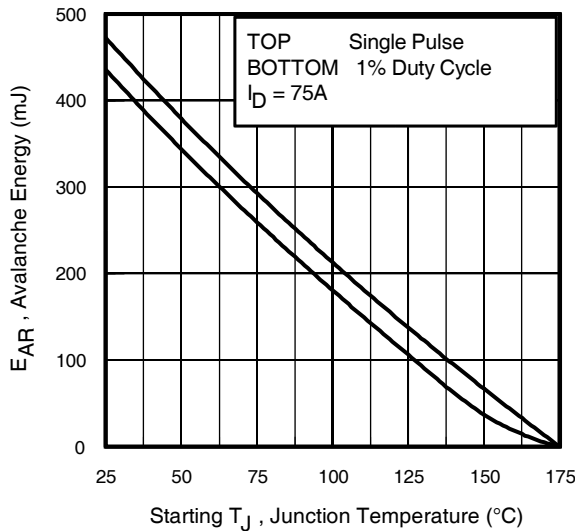


Fig 16. Maximum Avalanche Energy Vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

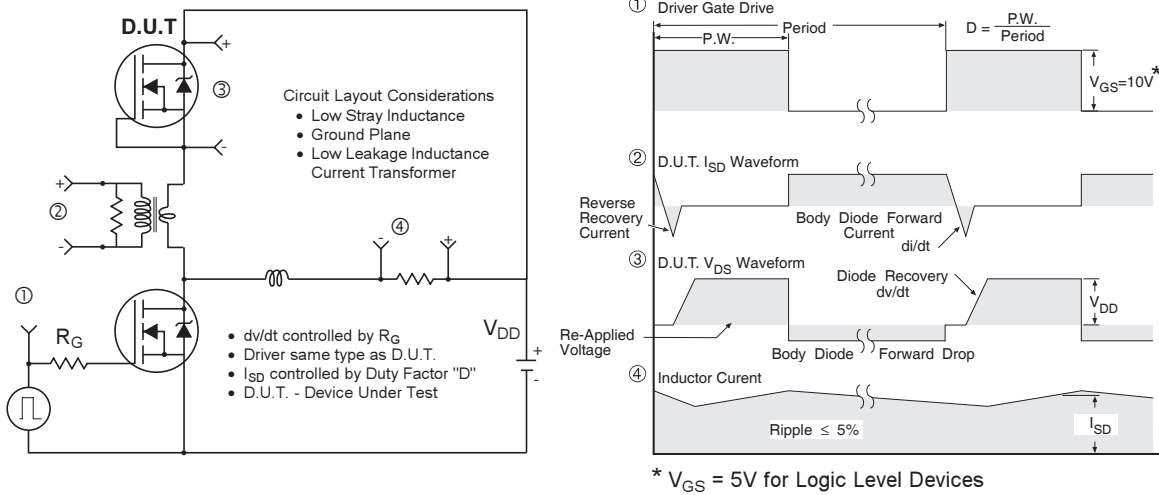


Fig 17. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs



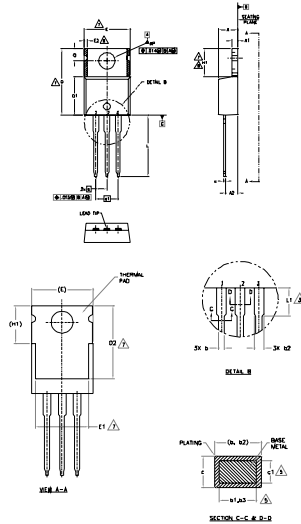
Fig 18a. Switching Time Test Circuit



Fig 18b. Switching Time Waveforms

TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



- NOTES:
- 1- DIMENSIONS AND TOLERANCING AS PER ASME Y14.5 M-1994
 - 2- DIMENSIONS ARE SHOWN IN INCHES (MILLIMETERS)
 - 3- LEAD DIMENSIONS AND PITCH DIMENSIONS IN (M)
 - 4- DIMENSION D, D1 & E DO NOT INCLUDE MOLD FLASH; MOLD FLASH SHALL NOT EXCEED .007" (0.175) PER SIDE; THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY
 - 5- DIMENSION H, H1 & H2 APPLY TO BARE METAL ONLY
 - 6- CONTROLLING DIMENSION - INCHES
 - 7- TYPICAL PITCH CORNER OPTIONS; OTHER DIMENSIONS CANNOT BE IT
 - 8- DIMENSION L2 x H1 DEFINE A ZONE; BENCH STAMPING AND SOLDERATION IRREGULARITIES ARE ALLOWED
 - 9- DUTING CORRELATION TO SPEC 70-220 (EQUIV. A2 (MIL) AND D2 (MIL)) WHERE DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE

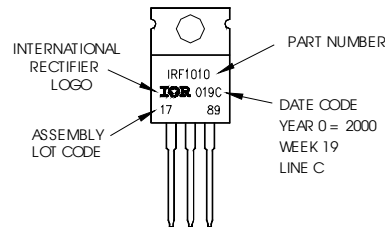
SYMBOL	MILLIMETERS		INCHES		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.83	.140	.190	
A1	0.91	1.40	.030	.055	
A2	2.03	2.82	.080	.110	
b	0.38	1.01	.015	.040	
b1	0.38	0.97	.015	.038	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.36	0.61	.014	.024	
c1	0.36	0.56	.014	.022	5
d	14.22	16.51	.560	.650	4
d1	8.90	9.52	.350	.375	
D2	1.68	12.88	.060	.507	7
E	8.65	12.87	.340	.509	4,7
E1	6.86	8.89	.270	.350	7
E2	-	0.76	-	.030	8
h	7.62	10.16	.300	.400	
h1	2.54	4.88	.100	.190	7,8
h2	12.70	14.73	.500	.580	
L	3.68	4.06	.145	.160	5
ap	2.54	4.08	.100	.161	
q	2.54	3.42	.100	.135	

- UNIT CONVERSIONS
- 1- INCH
 - 2- MILLIMETER
 - 3- INCH
 - 4- INCH
 - 5- INCH
 - 6- INCH
 - 7- INCH
 - 8- INCH
- IRF3305PbF
- 1- GATE
 - 2- COLLECTOR
 - 3- EMITTER
- IRF3305PbF
- 1- POWER
 - 2- SIGNAL
 - 3- GATE

TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
 LOT CODE 1789
 ASSEMBLED ON WW 19, 2000
 IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead-Free"



TO-220AB package is not recommended for Surface Mount Application

Notes:

1. For an Automotive Qualified version of this part please see <http://www.irf.com/product-info/automotive>
2. For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Data and specifications subject to change without notice.
 This product has been designed and qualified for the Industrial market.
 Qualification Standards can be found on IR's Web site.