

μPG2162T5N-EVAL-A

Evaluation Board

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Description:

The uPG2162T5N-EVAL-A evaluation board provides a quick and convenient means of evaluating the performance of the NEC uPG2162T5N switch. In addition to the device, the board provides DC block capacitors, power supply bypass capacitors, and RF and DC connectors.

A DC block capacitor is required at all RF ports. On this board, a 6.8pF capacitor is used for this purpose. The chosen capacitance value minimizes the mismatch effect associated with the serial capacitor over a relatively wide frequency range (2 to 6GHz). For a narrow band application or an application where the operating frequency is outside the specific frequency range, the user may select a different capacitance value. Generally the performance of the switch circuit is not sensitive, to a certain extent, to the value of DC block capacitors.

A 1000pF DC bypass capacitor is used on all control lines. For high speed applications the user may choose smaller capacitance or no capacitor at all.

DC supply connectors:

P1 is control voltage V_{cont1} , P2 is V_{cont2} and pins P3 and P4 are the ground. V_{cont1} and V_{cont2} should be connected to separate power supplies to provide the required control logic.

RF connectors:

As indicated on the board, J1 is connected to the ANT1 port, J2 is connected to the ANT2 port, J3 (OUT1) is connected to the TX, and J4 (OUT2) is connected to the RX port.

Information on Board Material:

The board material is 20 mil thick Duroid 6002. Its dielectric constant is 2.94.

Switch Logic Table:

The following table lists the logic table for switch states.

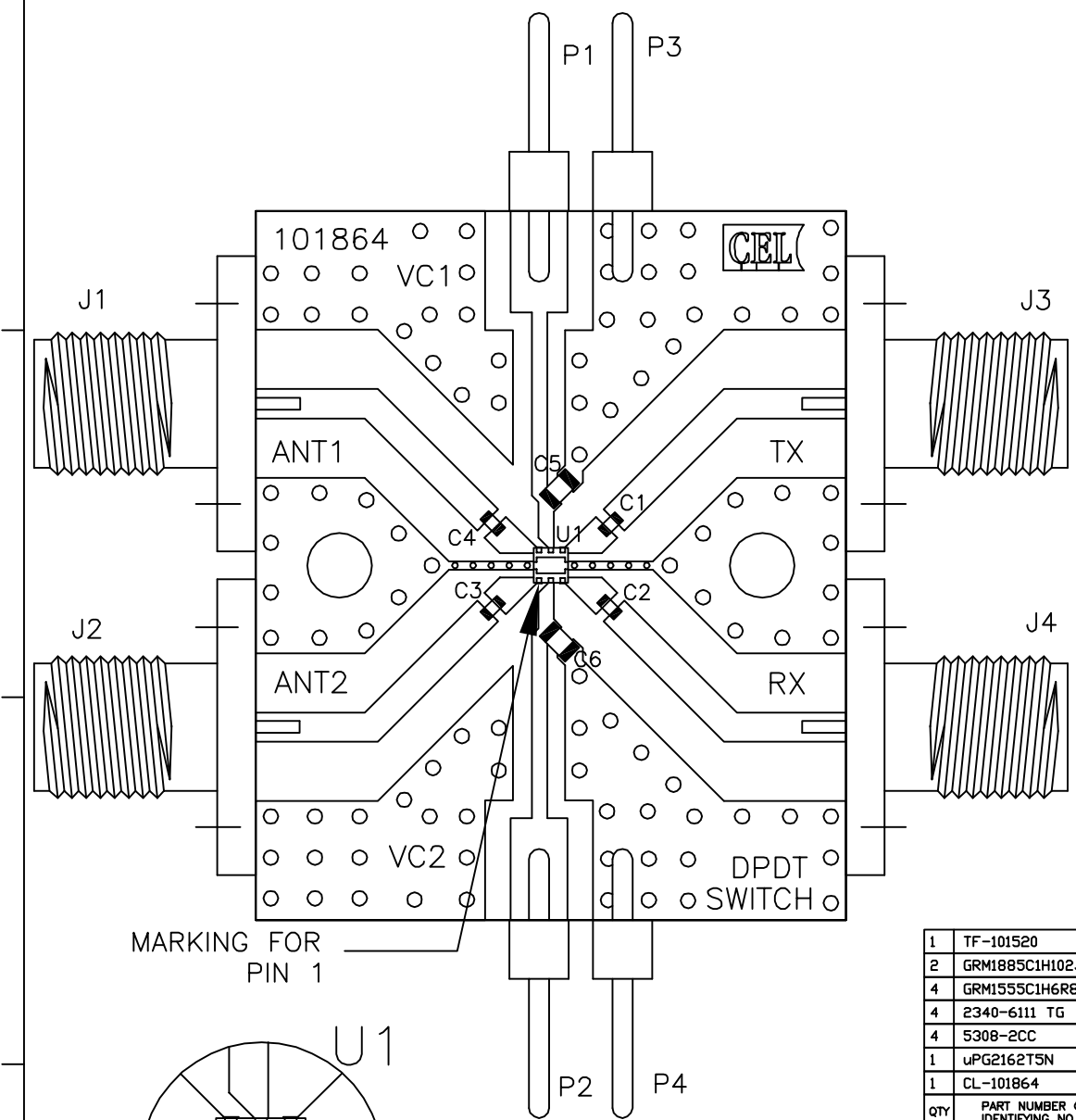
Vcont1	Vcont2	ANT1 – OUT1(TX)	ANT1 – OUT2(RX)	ANT2 – OUT1(TX)	ANT2 – OUT2(RX)	ANT1 – ANT2	TX – RX
H	L	measure ISOL	measure IL	measure IL	measure ISOL	measure ISOL2*	measure ISOL2*
L	H	measure IL	measure ISOL	measure ISOL	measure IL		

Insertion Loss of Through Board:

In assessing the insertion loss of the switch by measuring S21 of the evaluation board, it is necessary to take into account the loss through the connectors and PCB trace. To this end a through board was characterized to determine the board/connector loss. The table below lists the board loss at different frequencies.

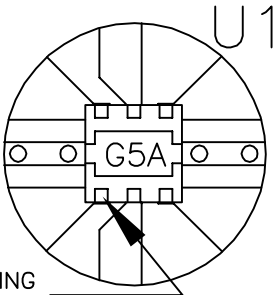
INPUT FREQUENCY (GHz)	BOARD LOSS (dB)
2.4	0.15
2.5	0.16
4.9	0.26
5.8	0.30
6.0	0.32

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



MARKING FOR
PIN 1

1	TF-101520	DRAWING	TEST BLOCK	7
2	GRM1885C1H102JA01B	C5,C6	0603 1000pF CAP MURATA	6
4	GRM1555C1H6R8CZ01B	C1,C2,C3,C4	0402 6.8pF CAP MURATA	5
4	2340-6111 TG	P1,P2,P3,P4	PIN HEADER 3M	4
4	5308-2CC	J1,J2,J3,J4	SMA FEMALE CONNECTOR TENSOLITE	3
1	uPG2162T5N	U1	NEC GaAs Switch uPG2162T5N	2
1	CL-101864	DRAWING	COMPONENT LAYOUT DRAWING	1
QTY	PART NUMBER OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL/SPECIFICATION	ITEM NO.



MARKING FOR
PIN 1

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES		APPROVALS		PARTS LIST	
TOLERANCES		Drawing by: Hugues de Saint Salvy		2005/04/22	
DECIMALS .XX± .01		Designed by: Hugues de Saint Salvy		2005/04/22	
ANGULAR .XXX± .005		Checked by:			
DO NOT SCALE DRAWING		Project Engineer:			
MATERIAL		Quality Control:			
FINISH					
NEXT ASSY USED ON					
APPLICATION					
CALIFORNIA EASTERN LABS 4590 PATRICK HENRY DR. SANTA CLARA CA. 95054				TITLE: uPG2162T5N-EVAL-A ASSEMBLY DRAWING	
		SIZE	FSCM NO.	DWG NO.	REV
		C		AD-101864	-
		SCALE NONE	RELEASE DATE	PROTOTYPE	SHEET 1 OF 1